Digital Object Identifier (DOI): (to be appear)

Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE 2013), Denver, CO, USA, 14-19 September, 2013.

Stability Analysis and Dynamic Response of a DC-Link Module with a Series Voltage Compensator

Huai Wang
Wenchao Liu
Henry S. H. Chung
Frede Blaabjerg

Suggested Citation

H. Wang, W. Liu, H. S. H. Chung, and F. Blaabjerg, "Stability analysis and dynamic response of a DC-link module with a series voltage compensator," *in Proc. IEEE Energy Convers. Congr. and Expo.*, 2013, pp. 2453-2460.

Stability Analysis and Dynamic Response of a DC-Link Module with a Series Voltage Compensator

Huai Wang, *IEEE Member*
Department of Energy Technology
Aalborg University
Aalborg, Denmark
hwa@et.aau.dk

Wenchao Liu, Henry Chung, *IEEE Senior Member*
Department of Electronic Engineering
City University of Hong Kong
Kowloon, Hong Kong
wenchliu@cityu.edu.hk; eeshc@city.edu.hk

Frede Blaabjerg, *IEEE Fellow*
Department of Energy Technology
Aalborg University
Aalborg, Denmark
fbl@et.aau.dk

***Abstract* — A DC-link module composed of a reduced value of DC-link capacitor and a series voltage compensator has been proposed. The voltage compensator processes the ripple voltage on the DC link and reactive power only, which can be implemented by low-voltage devices. The overall energy storage of the DC-link module is reduced, permitting the replacement of electrolytic capacitors by film capacitors in a cost-effective way. This paper focuses on the stability analysis and dynamic performance evaluation of the proposed DC-link module. Theoretical study and experimental verification are presented and the results are compared with the conventional DC-link design solution.**

I. INTRODUCTION

Besides the extensive research on more efficient and more compact power electronic systems, more and more efforts are devoted to better reliability performance with cost-effective and sustainable solutions [1]. Capacitors for DC-link applications are one of the critical components in terms of reliability, volume and cost in a power electronic systems [2]. Among different types of capacitors, aluminum electrolytic capacitors (E-Caps) are the most popular choice for the DC-link application because of their high volumetric efficiency and low cost. However, they suffer from short lifetime if not properly selected. Film capacitors outperform E-Caps in electrical and reliability performance. The challenge is that the volume and cost of film capacitors are usually 5-10 times of those of E-Caps with the same voltage rating and capacitance.

To overcome the above challenge, active power filters have been applied for DC-link passive components reduction [3]-[11]. In [3]-[4], an active circuit is series-connected between a three-phase diode bridge rectifier and an inductive DC-link filter for motor drive applications. The added circuit, as an electronic inductor, achieves a constant current source and therefore ensures a constant DC-link current. The purpose of the electronic inductor is to minimize the DC-link inductor and reduce the input (i.e. AC grid) side current harmonics. For capacitive DC-link applications (i.e. the major components are DC-link Capacitors), a DC-link module with a series voltage compensator has been proposed in [5] to replace E-Caps by a reduced value of film capacitor. The voltage compensator is series-connected between a capacitive DC-link and the load stage. It operates as a ripple voltage source so that the output voltage of the DC-link module is a pure DC in ideal operation, which is independent of the DC-link capacitance value.

The work described in this paper was fully supported by a grant from the Research Grants Council of the Hong Kong Special Administrative Region, China (Project No.: CityU 112512).

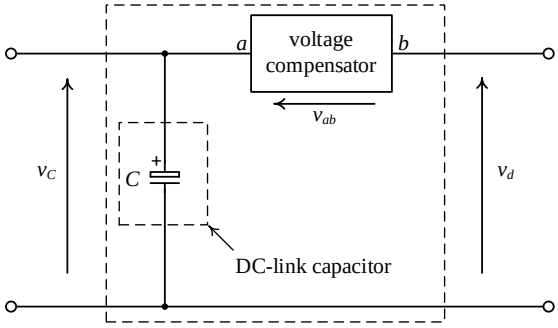


Fig. 1. Basic concept of the proposed DC-link module in [5].

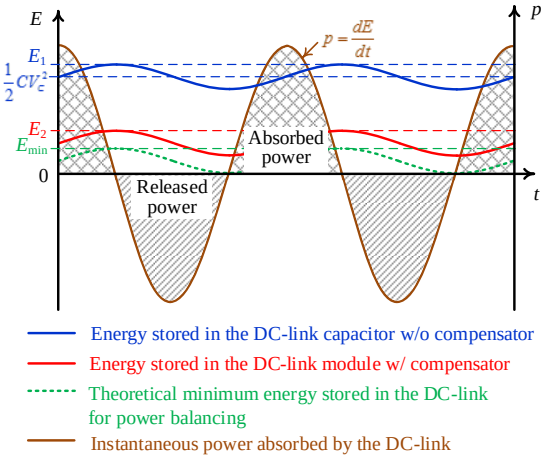


Fig. 2. Energy storage and instantaneous power of the DC link.

As illustrated in Fig. 1, the basic concept of the DC-link module is to generate an AC voltage v_{ab} of same amplitude and phase as that of the ripple component of the capacitor voltage v_C. A pure DC voltage v_d can be achieved, which is independent of the value of the capacitor C. From an energy point of view, the proposed DC-link module divides the energy storage into the capacitor C and the voltage compensator. Fig. 2 plots the energy storage requirement of the DC link for power balancing under three scenarios. An energy storage of E_1 or E_{min} could provide the same instantaneous power p. However, to maintain the DC-link voltage, E_1 is required in conventional DC-link design with capacitors only. The proposed DC-link module provides the opportunity to reduce the energy storage requirement from E_1 to E_2 as shown in Fig. 2. Compared to the

shunt active ripple reduction circuits presented in [8]-[11], the proposed voltage compensator has the advantage of low voltage and low power rating as it processes the DC-link voltage ripple only.

In [6], the concept of the proposed DC-link module has been applied in a Power Factor Corrector (PFC) front-end AC-DC-DC single-phase power conversion system. In [7], the hold-up time related characteristic of the DC-link module is investigated. The study in [6] and [7] demonstrate the effectiveness of the proposed solution for applications with or without hold-up time requirement.

As an important aspect of continuous research and development of the technology, this paper presents the stability analysis of the proposed DC-link module in [5]. The study is critical to ensure the static and dynamic control performance of the module. The paper is organized as follows: § II describes the operation principles of the DC-link module; § III and § IV perform the stability analysis from power flow and impedance perspectives, respectively; § V shows the experimental results on the dynamic responses of the DC-link module, followed by the conclusions.

II. Operation Principles of the DC-Link Module

Fig. 3 shows the implementation of the basic concpet illustrated in Fig. 1. The power stage is a DC-AC converter consisting of a full-bridge (FB) circuit and an output filter formed by the inductor L_f and the capacitor C_f. It should be noted that a half-bridge circuit can also be used if the current i_d is unidirectional. The DC side of the FB is connected to a DC voltage source v_{DC} with two possible configurations. The first one utilizes a capacitor for the DC source while the second one has an external supply connected to it. Since the first configuration gives a simpler solution, it will be studied in this paper. The control stage is composed of the sensing and condition circuits of v_C and v_{DC}, a Proportional-Integral (PI) compensation circuit, two computation circuits, and a PWM modulation circuit.

The scaling factor α is equal to the ratio between V_{tri} and $V_{DC,ref}$, where V_{tri} and $V_{DC,ref}$ are the amplitude of the triangular signal in the PWM modulator and reference voltage of v_{DC}, respectively. β is the scaling factor of v_{DC}. The difference between $V_{DC,ref}$ and βv_{DC} is processed by a PI controller to give an offset voltage v_{os}. The control signal v_{con} is derived by combining αv_C with v_{os}. The DC component of αv_C is ideally cancelled in v_{con} by v_{os} as $V_{os} = -\alpha V_C$, where V_{os} and V_C are the DC component of v_{os} and v_C, respectively. With such arrangement, it is unnecessary to use a high-pass filter to extract the AC component of v_C. At the same time, the DC component of v_{ab} can be eliminated so that the added voltage source handles the AC component only. During steady-state operation, v_{con} equals the conditioned AC component of αv_C. It is then used to compare with the triangular carrier waveform in the PWM modulator to generate the voltage v_{ab} having the same phase and amplitude of Δv_C. Without any external supply, the power consumed by the module (i.e. power losses) is obtained from the AC side of the bridge, that is, Power Converter I. Practically, instead of a pure AC voltage, v_{ab} and thus v_{con} have a small DC component due to the internal power loss in the voltage compensator.

The DC-link module shown in Fig. 3 allows a high voltage ripple on C. The value of C is compromised by the amplitude of v_{ab} and therefore the voltage stresses on the components in the voltage compensator. The design guidelines and operation principles of the module are discussed in more details in [5].

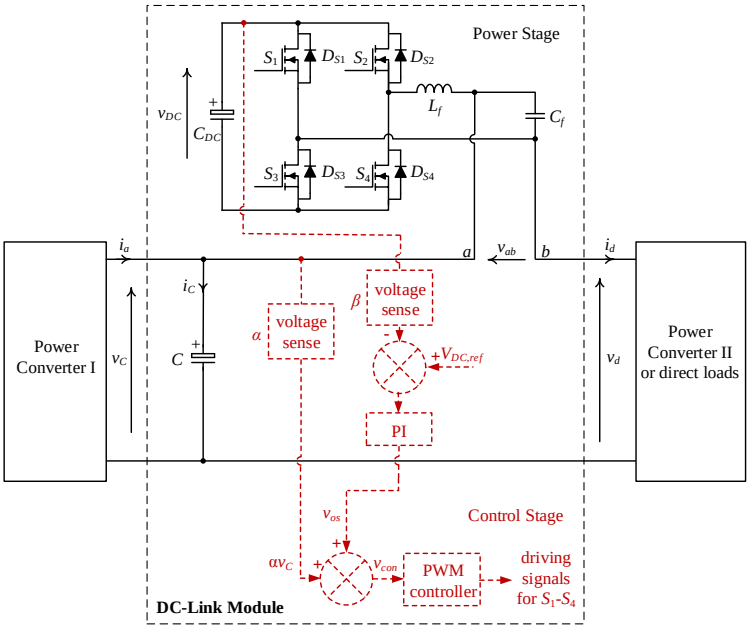


Fig. 3. Circuit schematic of the proposed dc-link module.

III. Power Flow Based Stability Analysis

A. Power Flow Analsis

Fig. 4 presents the AC circuit model of the power conversion system shown in Fig. 3. The steady-state and transient power flow are studied in phasor form. Let Z_C and Z_L be the impedance of the DC-link capacitor C and the incremental input impedance of the load (i.e. Power Converter II or direct loads in Fig. 3), respectively. $\Delta\tilde{I}_a$, $\Delta\tilde{I}_d$, $\tilde{I}_C$, $\Delta\tilde{V}_C$, $\tilde{V}_{ab}$ and $\Delta\tilde{V}_d$ are the phasor form of Δi_a, Δi_d, i_C, Δv_C, v_{ab} and Δv_d, respectively. The currents Δi_a and Δi_d are the AC component of the currents i_a and i_d defined in Fig. 3, respectively. Z_C and Z_L are defined as follows:

$$Z_C = |Z_C| \angle -90^o \tag{1}$$

$$Z_L = \frac{\Delta\tilde{V}_d}{\Delta\tilde{I}_d} = |Z_L| \angle \delta_L \tag{2}$$

where δ_L is the phase angle of Z_L.

As v_{ab} is designed to follow Δv_C, a constant parameter K is defined as

$$K = \frac{v_{ab}(t)}{\Delta v_C(t)} \tag{3}$$

In steady-state operation, K=1 as illustrated in §II.

Thus, the load current ripple is

$$\Delta\tilde{I}_d = \frac{\Delta\tilde{V}_C - \tilde{V}_{ab}}{Z_L} = \frac{1-K}{|Z_L|}\Delta\tilde{V}_C \angle -\delta_L \tag{4}$$

Therefore, the average power absorbed by the module can be obtained as

$$P_{ab} = V_{ab}\Delta I_d \cos\delta_L = \frac{K(1-K)}{2}\frac{|\Delta v_C|^2}{|Z_L|}\cos\delta_L \tag{5}$$

where $|\Delta v_C|$ is the amplitude of Δv_C, V_{ab} and ΔI_d are the Root-Mean-Square (RMS) values of v_{ab} and Δi_d, respectively.

Consider the output current of Power Converter I as shown in Fig. 3,

$$\Delta\tilde{I}_a = \tilde{I}_C + \Delta\tilde{I}_d = \frac{1}{Z_C}\Delta\tilde{V}_C + \frac{1-K}{Z_L}\Delta\tilde{V}_C \tag{6}$$

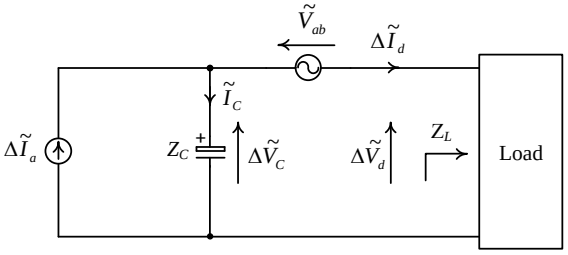


Fig. 4. Equivalent AC circuit of the conversion system shown in Fig. 3.

Based on (6), it can be shown that

$$|\Delta v_C| = \left[\sqrt{\frac{1}{|Z_C|^2} + \frac{(1-K)^2}{|Z_L|^2} - \frac{2(1-K)}{|Z_C||Z_L|}\sin\delta_L}\right]^{-1} |\Delta I_a| \tag{7}$$

By substituting (7) into (5), the average power is

$$P_{ab} = \frac{K(1-K)}{2|Z_L|}\left[\frac{1}{|Z_C|^2} + \frac{(1-K)^2}{|Z_L|^2} - \frac{2(1-K)}{|Z_C||Z_L|}\sin\delta_L\right]^{-1} |\Delta I_a|^2 \cos\delta_L \tag{8}$$

The above equation is applicable for different load types. In Part B of §III, the steady-state characteristics and stability of the whole system with two common load types, including resistive load and constant power load, will be discussed.

B. Stability Analsis

a) Case I – Resistive load

For resistive load, δ_L = 0. Therefore, according to (8),

$$P_{ab} = \frac{K(1-K)}{2|Z_L|}\left[\frac{1}{|Z_C|^2} + \frac{(1-K)^2}{|Z_L|^2}\right]^{-1} |\Delta I_a|^2 \tag{9}$$

For stable operation, $P_{ab} \geq 0$. Thus,

$$K \leq 1 \tag{10}$$

Differentiate (9) with respect to K,

$$\frac{\partial P_{ab}}{\partial K} = \frac{P_{ab}^{\ 2}|Z_L|}{2K^2|\Delta I_a|^2}\left[\frac{1}{|Z_L|^2} - \frac{2K-1}{(1-K)^2}\frac{1}{|Z_C|^2}\right] \tag{11}$$

Since $|Z_L| > |Z_C|$ and K is near unity,

$$\frac{\partial P_{ab}}{\partial K} < 0 \tag{12}$$

The interpretation of the above equation is as follows: when K is larger than its steady-state value (ΔK is positive), P_{ab} will reduce. It implies that the power absorbed by the module from the circuit will then be reduced. If the DC source is a capacitor, its voltage will decrease. Thus, both v_{ab} and K will be reduced. Therefore, K will revert back to the steady-state value. Similarly, if K is initially smaller than its steady-state value (ΔK is negative), P_{ab} will increase. Thus, v_{ab} and K will increase. Again, K will revert back to the state-state value.

b) Case II – Constant power load

For resistive load, δ_L = 180 °. Therefore, according to (8),

$$P_{ab} = \frac{K(K-1)}{2|Z_L|}\left[\frac{1}{|Z_C|^2} + \frac{(1-K)^2}{|Z_L|^2}\right]^{-1} |\Delta I_a|^2 \tag{13}$$

For stable operation, $P_{ab} \geq 0$. Thus,

$$K \leq 1 \tag{14}$$

Since the load power is regulated, it is assumed here that the ripple load power ΔP_L ($|\Delta P_L| = |\Delta v_d||\Delta i_d|$) is constant. Unlike

Case I, the input impedance of the load Z_L therefore varies with the value of K. Thus,

$$|Z_L| = \frac{|\Delta v_d|}{|\Delta i_d|} = \frac{(K-1)^2 |\Delta v_C|^2}{|\Delta P_L|} \tag{15}$$

By substituting (15) into (5),

$$P_{ab} = \frac{K\,|\Delta P_L|}{2\,(K-1)} \tag{16}$$

Differentiate (16) with respect to K,

$$\frac{\partial P_{ab}}{\partial K} = -\frac{|\Delta P_L|}{2\,(K-1)^2} = -\frac{|\Delta v_C|^2}{2\,|Z_L|} < 0 \tag{17}$$

Thus, similar behavior as in (12) is obtained. It implies that the system has stable operation.

It is worth to mention that the power flow analysis of the voltage compensator reveals the stability of the DC-link module in a qualitative way. To obtain the information for the purpose of control stage design, the following section analyzes the stability in the frequency domain based on small signal modeling.

IV. Frequency Domain Stability Analysis

There are three possible sources of perturbations for the DC-link module which come from the input (i.e. Power Converter I), the load (i.e. Power Converter II or direct loads) and the control stage SPWM modulation (i.e. modulation index M). Accordingly, small signal perturbations $\hat{v}_C(t)$, $\hat{i}_o(t)$ and $\hat{M}(t)$ are superposed on the average steady-state values of the DC-link capacitor voltage v_C, the output side load current and the modulation index M, respectively. Besides that, the dependent sources $\hat{V}_{ab}(t)$, $\hat{v}_{DC}(t)$, $\hat{v}_d(t)$, $\hat{i}_a(t)$, $\hat{i}_{DC}(t)$, $\hat{i}_{Lf}(t)$ are defined as the perturbations on V_{ab}, v_{DC}, v_d, i_a, i_{DC} and i_{Lf}, respectively.

The frequency domain small signal model of the DC-link module can be derived as shown in Fig. 5. It should be noted that the model shown in Fig. 5 is applied to analyze low frequency characteristics as the proposed DC-link module is usually applied for filtering low frequency voltage ripples (e.g. double line frequency). Therefore, the effect of the output filter of the voltage compensator is negligible within the frequency range of interest due to it has a much higher cutoff frequency. $Z_L(s)$ is the equivalent load impedance of the Power Converter II or direct loads (e.g. a full-bridge DC-DC converter or a resistive load).

The power conversion system can be considered as a cascaded system composed of the front-end stage (including the DC-link module) and the load stage (i.e. Power Converter II or direct loads). $Z_o(s)$ is defined as the output impedance of the front-end stage and $Z_{in}(s)$ is as the input impedance of the load

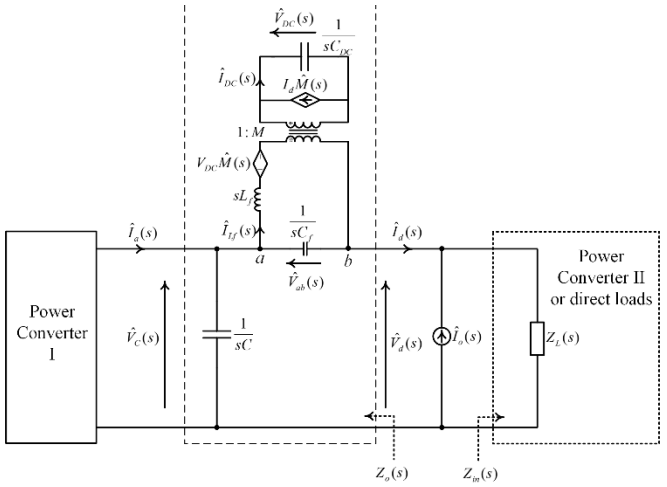


Fig. 5. Small signal model of the proposed DC-link module.

stage. The stability of the cascaded system depends on the output impedance $Z_o(s)$ and input impedance $Z_{in}(s)$ defined in Fig. 5. For stable operation, it should prevent $Z_o(s)/ Z_{in}(s)$ from circling the (-1, 0) point on S-plane. The impedance specifications for stable DC distributed power conversion systems have been well discussed in [12]. It shows that the forbidden region (i.e. unstable region) is

$$\mathrm{Re}\left(\frac{Z_o(s)}{Z_{in}(s)}\right) \geq -\frac{1}{2} \tag{18}$$

The forbidden region is represented in Fig. 6. It prevents $Z_o(s)/ Z_{in}(s)$ from circling the (-1, 0) point with a gain margin of 6 dB and a phase margin of 60 °.

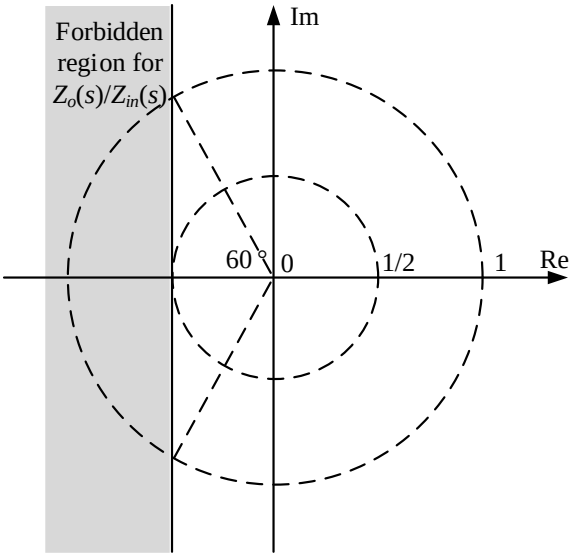


Fig. 6. Forbidden region for $Z_o(s)/Z_{in}(s)$ for stable operation of cascaded systems [12].

For frequency range much lower than the resonant frequency of the output *LC* filter of the voltage compensator, the effect of sL_f and $1/sC_f$ is negligible (i.e. $\hat{I}_{Lf}(s) = \hat{I}_d(s)$). According to Fig. 5, the output impedance of the DC-link module can be derived by $Z_o(s) = \hat{V}_d(s) / \hat{I}_o(s)$ when the Power converter II or direct loads are disconnected and $\hat{V}_C(s) = \hat{M}(s) = 0$. That is corresponding to

$$\begin{cases} \hat{V}_{ab}(s) = M\hat{V}_{DC}(s) \\ \hat{V}_{DC}(s) = \dfrac{1}{sC_{DC}} M\hat{I}_d(s) \\ \hat{I}_d(s) = -\hat{I}_o(s) \\ \hat{V}_{ab}(s) = -\hat{V}_d(s) \end{cases} \tag{19}$$

Therefore, it can be derived that

$$Z_o(s) = \frac{M^2}{sC_{DC}} \tag{20}$$

Similarly, when the DC-link module and the Power Converter I are disconnected, the input impedance of the Power Converter II or direct loads can be obtained as

$$Z_{in}(s) = Z_L(s) \tag{21}$$

a) Case I – Resistive load

For resistive load, the load impedance is equivalent to a resistance R_L, that is

$$Z_{in}(s) = R_L \tag{22}$$

Therefore,

$$\frac{Z_o(s)}{Z_{in}(s)} = \frac{M^2}{sC_{DC}R_L} \tag{23}$$

It can be noted that $Z_o(s)/ Z_{in}(s)$ is on the positive Im–axis of the *S*-plane which is located outside of the forbidden region according to Fig. 6. Therefore, the cascaded front-end stage and load stage are stable.

b) Case II – Constant power load

The constant power load can be modelled as a negative resistance in the frequency range of interest in this study. It is as

$$Z_{in}(s) = -\frac{V_d^2}{P_L} \tag{24}$$

where V_d is the average value of v_d within one steady-state double line frequency cycle and P_L is the constant power load.

Therefore,

$$\frac{Z_o(s)}{Z_{in}(s)} = -\frac{M^2 P_L}{sC_{DC}V_d^2} \tag{25}$$

Similarly, it can be noted that $Z_o(s)/Z_{in}(s)$ is on the negative Im–axis of the *S*-plane which is located outside of the forbidden region according to Fig. 6. Therefore, the cascaded front-end stage and load stage are stable under constant power load.

V. Experimental Verifications on Stability and Dynamic Response

To verify the above stability analysis, a 600W test bed of AC-DC-DC converters has been built. The Power Converter I is a PFC and the Power Converter II is a phase-shifted full-bridge DC-DC converter with constant power load. Fig. 7 shows the implementation of the DC-link module. The specifications and designed parameters are shown in Table I. The original output capacitor bank of the PFC is formed by two 330μF, 450V E-caps connected in parallel. According to the manufacturer's data, the lifetime of the capacitors is 3,000 hours at 105℃ (12,000 hours estimated under 85℃ and rated ripple current). A DC-link module with a 120μF (82% capacitance reduction) film capacitor (100,000 hours lifetime under 85℃ and rated ripple current) is used to replace the capacitor bank. The voltage across C_{DC} is designed to be 50V.

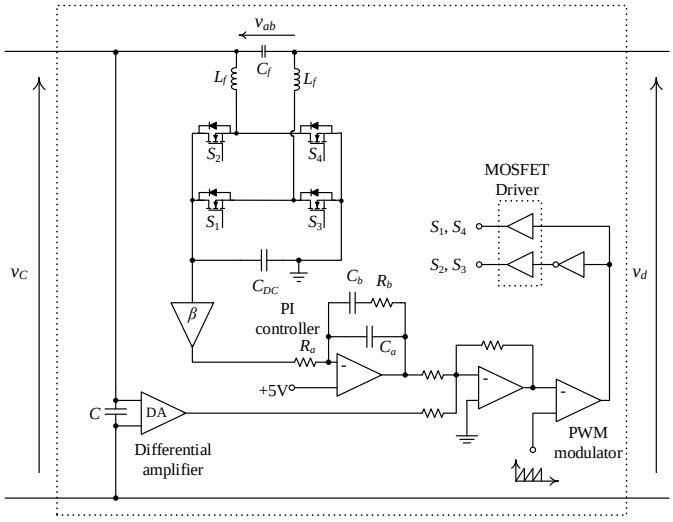


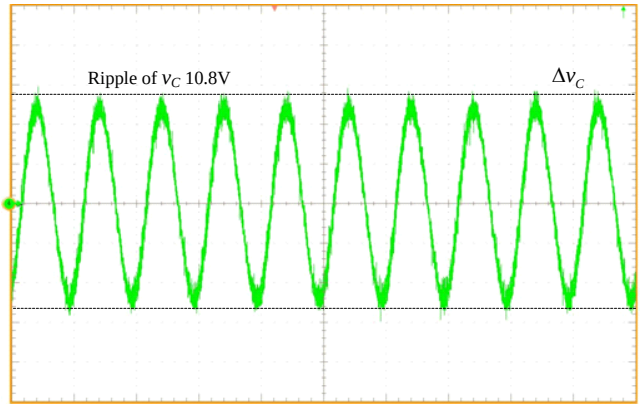
Fig. 7 Implementation of the proposed DC-link module.

Table I Specifications and designed parameters of the DC-link module.

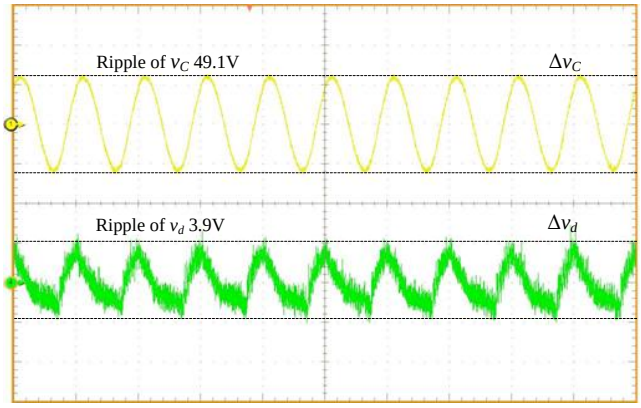
Parameter	Value / part no.	Parameter	Value / part no.
V_d	400V	P_L	600W
V_{DC}	50V	C	120μF, 450V
C_{DC}	1000μF, 63V	L_f	120μH
C_f	3.3μF, 100V	R_a	100kΩ
C_a	10μF, 35V	R_b	33kΩ
C_b	0.1μF, 50V	α	0.06
$S_1 - S_4$	FDD86102	β	0.1

Fig. 8 shows the waveforms of the DC-link with E-caps solution and DC-link module solution during steady-state operation. In both cases, the power conversion system are stable. The voltage ripple across the 660μF E-Caps are 10.8V. With the DC-link module composed of 120μF film-capacitors, the voltage ripple of v_d is limited to 3.9V.

Figs. 9 (a)-(c) show the dynamic response of the proposed DC-link module during start-up, step-up load and step-down load transients. For comparative study with the conventional E-Caps solution, Figs. 9(d)-(f) show the dynamic response of the DC-link voltage of E-Caps under the corresponding transients.

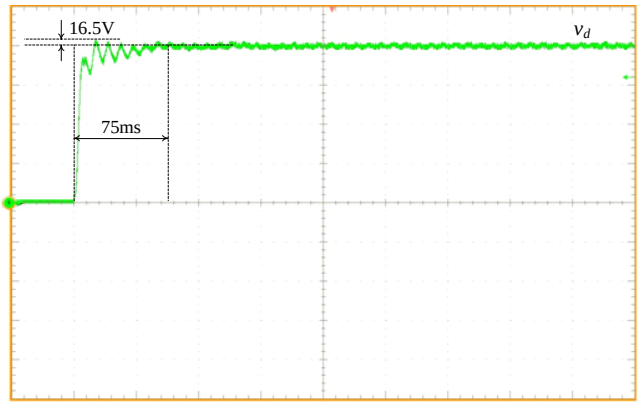


(a) Waveform of DC-link voltage ripple (with 660μF E-Caps) (Δv_C: 2V/div, Timebase: 10ms/div).

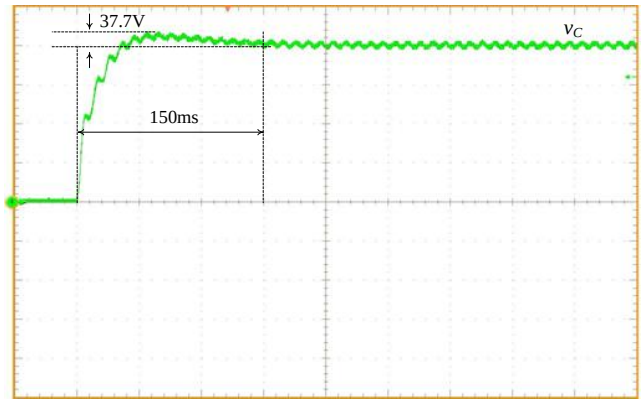


(b) Waveforms of Δv_C and Δv_d (with 120μF film capacitor) (Δv_C: 20V/div, Δv_d: 2V/div, Timebase: 10ms/div).

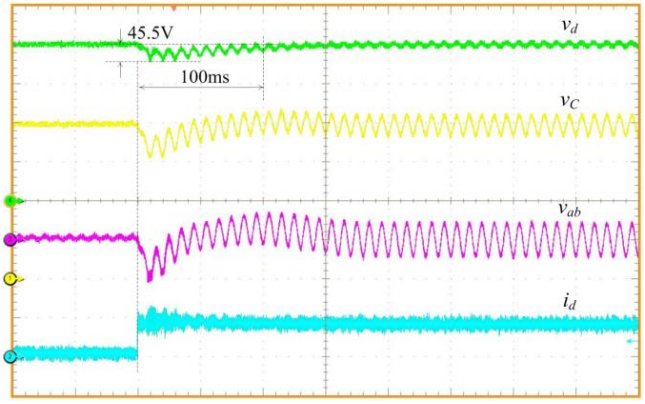
Fig. 8 Measured waveforms of the DC-link module under steady-state full-load operations (600W).



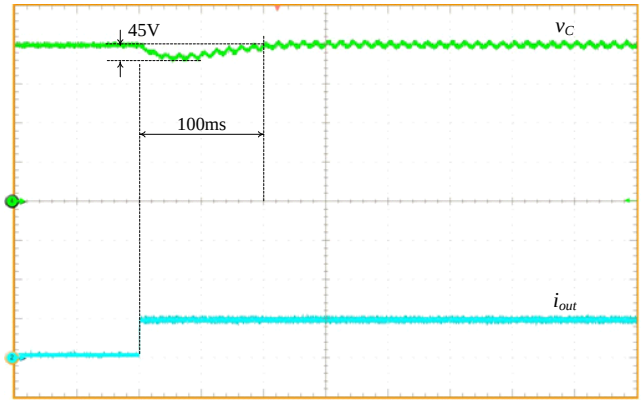
(a) Startup transient of the DC-link module under the full load condition (v_C: 100V/div, Timebase: 50ms/div).



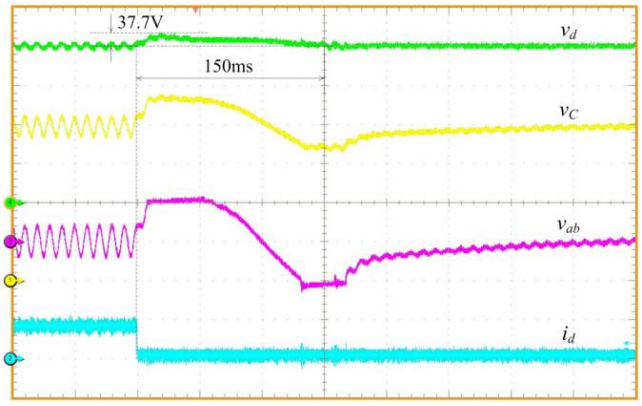
(d) Startup transient under the full load condition with 660μF E-Caps (v_C: 100V/div, Timebase: 50ms/div).



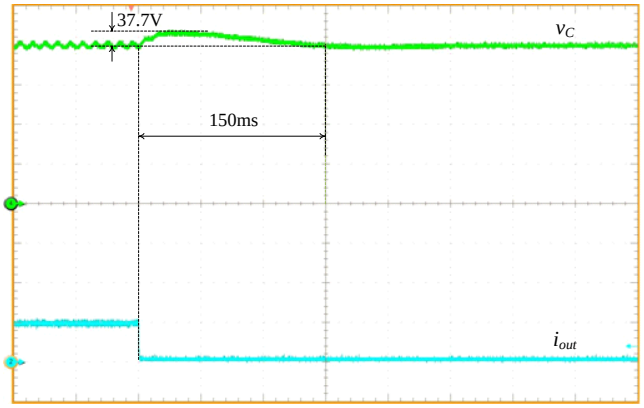
(b) Dynamic response of the DC-link module when the output is changed from 10% load to full load (v_d: 100V/div,v_C:100V/div, v_{ab}:40V/div, i_d: 2A/div, Timebase: 50ms/div).



(e) Dynamic response when the output is changed from 10% load to full load with 660μF E-Caps (v_C: 100V/div, i_{out}: 50A/div, Timebase: 50ms/div).



(c) Dynamic response of the DC-link module when the output is changed from full load to 10% load (v_d: 100V/div,v_C:100V/div, v_{ab}:40V/div, i_d: 2A/div, Timebase: 50ms/div).



(f) Dynamic response when the output is changed from full load to 10% load with 660μF E-Caps (v_C: 100V/div, i_{out}: 50A/div, Timebase: 50ms/div).

Fig. 9. Measured waveforms of the DC-link module under start-up and load changes operation (i_{out} is the output current of the load stage full-bridge DC-DC converter).

Fig. 9(a) shows the startup transient of the module output v_d. The DC value of v_d is 400V. The settling time of the startup process is 75ms and voltage overshoot is 16.5V. Fig. 9(b) shows the transient waveforms of v_d, v_C, voltage compensator output voltage v_{ab} and DC-link output current i_d, when the output is suddenly changed from 10% load to full load. v_d is momentarily reduced by 45.5V and its settling time is 100ms. Fig. 9(c) shows the corresponding waveforms when the output is suddenly changed from full load to 10% load. v_d is momentarily increased by 37.7V and its settling time is 150ms.

Fig. 9(d) show the startup transient of v_C when the output is full load with the conventional E-Caps solution. The average DC voltage is 400V. The settling time of the startup process is 150ms and the voltage overshoot is 37.7V. Fig. 9(e) shows the output current of the second stage full-bridge DC-DC converter i_{out} and v_C when the output is suddenly changed from 10% load to full load. The voltage v_C is momentarily dropped by 45V and the settling time is 100ms. Fig. 9(f) shows the corresponding waveforms when the output is suddenly changed from full load to 10% load. v_C is momentarily jumped up by 37.7V and the settling time is 150ms.

Comparing Fig. 9(a) with Fig. 9(d), the startup time is shorter and the overshoot voltage is smaller with the proposed module. As shown in Figs. 9(b) and (e), and Figs. 9(c) and (f), under the load change conditions, the transient responses of the system with the module are similar to the ones with the E-Cap bank.

CONCLUSIONS

The stability analysis and dynamic response of a DC-link module with a series voltage compensator have been studied in this paper. Prior-art research have demonstrated the DC-link module as a promising reliable and cost-effective DC-link solution. This paper performs a further in-depth investigation into the stability and dynamic response, which are also important for practical applications. Theoretical analysis reveals that a stable operation can be achieved with the proposed DC-link module from both power flow perspective and impedance perspective. For experimental validations, a DC-link module is built for a 600W AC-DC-DC test bed, which achieves 82% reduction of the DC-link capacitance and more than 8 times lifetime extension of the DC-link capacitors. The experimental results of steady-state operation, start-up, and step-up and step-down load changes are given. It reveals that the proposed DC-link module retain the control performance compared to that of conventional E-Caps solution in terms of both stability and dynamic responses. Regarding the start-up transient, the DC-link module has a faster settling time and lower overshoot than the E-Caps solution.

REFERENCES

[1] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics - challenges, design tools and opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17-26, Jun. 2013.

[2] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications – an overview," *in Proc. IEEE Energy Conversion Congress and Exposition*, 2013 (Accepted).

[3] J. Salmon and D. Koval, "Improving the operation of 3-phase diode rectifiers using an asymmetrical half-bridge DC-link active filter," *in Proc. IEEE Industry Applications Conference*, 2000, pp. 2115 - 2122.

[4] C. Klumpner, A. Timbus, F. Blaabjerg, and P. Thogersen, "Adjustable speed drives with square-wave input current: a cost effective step in development to improve their performance," *in Proc. IEEE Industry Applications Conference*, 2004, pp. 600-607.

[5] H. Wang and H. Chung, "Study of a new technique to reduce the DC-link capacitor in a power electronic system by using a series voltage compensator," i*n Proc. IEEE Energy Conversion Congress and Exposition*, 2011, pp. 4051-4057.

[6] H. Wang and H. Chung, "A novel concept to reduce the DC-link capacitor in PFC front-end power conversion systems," *in Proc. IEEE Applied Power Electronics Conference and Exposition*, 2012, pp. 1192-1197.

[7] H. Wang, W. Liu, and H. Chung, "Hold-up time analysis of a DC-link module with a series voltage compensator," *in Proc. IEEE Energy Conversion Congress and Exposition*, 2012, pp. 1095-1100.

[8] S. Li, B. Ozpineci, and L. M. Tolbert, "Evaluation of a current source active power filter to reduce the dc bus capacitor in a hybrid electric vehicle traction drive," *in Proc. IEEE Applied Power Electronics Conference*, 2009, pp. 1185-1190.

[9] H. Yoo and S. K. Sul, "A new circuit design and control to reduce input harmonic current for a three-phase AC machine drive system having a

very small dc-link capacitor," *in Proc. IEEE Applied Power Electronics Conference*, 2010, pp. 611-618.

[10] R. X. Wang, F. Wang, D. Boroyevich, R. Burgos, R. X. Lai, P. Q. Ning, and K. Rajashekara, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430-1443, May 2011.

[11] P. Krein, R. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690-4698, Nov. 2012.

[12] X. Feng, J. Liu, and F. C. Lee, "Impedance specifications for stable DC distributed power systems," *IEEE Trans. Power Electronics*, vol. 17, no. 2, pp. 157-162, Mar. 2002.