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A New Configuration for Multilevel Converters With Diode Clamped Topology

A.Nami, F.Zare, SMIEEE, G.Ledwich, SMIEEE, A.Ghosh, FIEEE, F.Blaabjerg[*]*, FIEEE*

Abstract—**Due to the increased use of renewable energy and power electronic applications, more multilevel converters (MLC) are developed. A Neutral Point Clamped (NPC) inverter is one of the most used multilevel topologies for wind turbine (WT) and photovoltaic (PV) applications. One of the most crucial points in this type of converter is dc-voltage control. In this paper, a novel multi output dc-dc converter connected to a diode clamped topology is presented. This converter, for a given duty cycles, is able to regulate the capacitor voltage to provide an appropriate input voltage for NPC regardless of load changes which can avoid neutral point balancing problem in such converters. In addition, the presented topology is suitable for renewable energy systems to boost the low rectified output-voltage. In order to verify the proposed topology, steady state analysis, modelling and simulations are carried out.**

***Index Terms*—Multilevel inverter, diode clamped inverter, neutral point voltage, dc-dc converter, multi-output converter.**

I. INTRODUCTION

SINCE wind turbine (WT) and photovoltaic (PV) systems have been addressed by many researches, the need of direct connection of these systems to a high and medium voltage grids forces modification of the multilevel topologies. Among them, (NPC) is the most common type of converter which is widely used in WT and PV applications. Fig. 1 shows a basic configuration of a three-level NPC topology. The most crucial issue in NPC is the neutral point voltage balancing and it has been studied by several authors [1-3].

Multi output dc-dc converters are such efficient and economical devices which are used instead of several separate single output converters to make up a multi output power supply [4]. Recently, several types of multi output dc-dc converters such as switched-capacitor, LLC resonant topology, cross regulation and parallel regulation techniques which are widely use in telecommunication, computers and industrial fields, are addressed in [5-8] respectively.

This paper proposes a novel dc-dc converter with series capacitors in order to generate two different voltage levels for NPC inverter. It can also be applied for more voltage levels.

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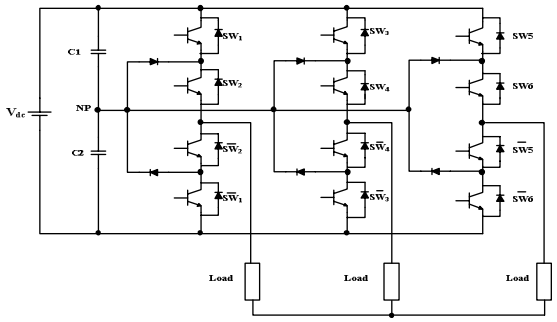

Fig.1. A circuit configuration of a traditional three-level NPC.

This converter basically operates as a boost or buck converter based on duty cycles of the switches in each subinterval of the switching period. In this converter, by controlling the duty cycles of the switches in each subinterval, the output voltage can be controlled to provide the appropriate input dc-voltage for the NPC. This can avoid the capacitors voltage unbalancing in the diode clamped topology. Moreover, by applying the presented topology in renewable energy systems, low rectified output-voltage can be boosted to a desired level.

In order to verify a feasibility of this topology and its application, steady state and dynamic analysis have been carried out. Finally simulation results are compared with the theoretical analysis both for the steady state and transient modes.

II. BASIC OF CIRCUIT

A. basic configuration and circuit diagram

A basic configuration and circuit diagram of the novel dc-dc converter with two output-voltages is shown in Fig. 2 (a). This circuit includes three switches which are named S_m, S_1 and S_2 and two capacitors C_1 and C_2 with different loads R_1 and R_2. In the subinterval zero, S_m is turned on and the inductor can be magnetized by the current flowing through it. In the next two subintervals, S_m remains off and the two switches, S_1 and S_2 work in a complimentary fashion to charge the capacitors. When S_1 is on and S_2 is off, the inductor current can charge both C_1 and C_2 to produce v_1 and v_2, respectively. On the other hand, when S_1 is off and S_2 is on in the last subinterval, C_1 is being discharged through R_1 as reverse current flow is prohibited by the diode, while C_2 is being charged by the inductor current. Consequently the output voltage level can be controlled by adjusting the duty cycle of each switch.

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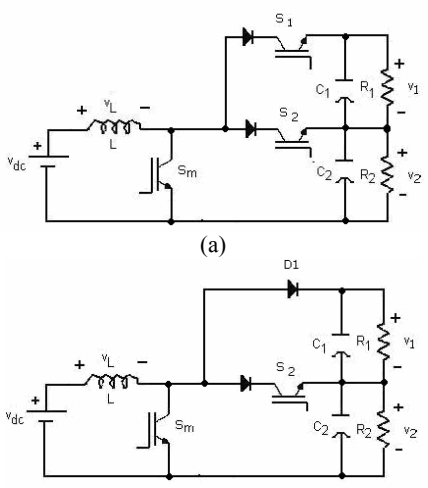


Fig.2. A circuit diagram (a) with switch S_1 (b) with diode D_1.

Corresponding to circuit operation, it is possible to replace the top switch S_1 by a diode, as shown in Fig. 2 (b). During the second subinterval, the diode can direct the inductor current to both the capacitors. However when S_2 is on in the last subinterval, the diode obstruct the charging current through C_1 because the voltage across the diode will be negative. Thus the switch S_2 conducts to direct the inductor current to C_2.

Fig.3 shows the proposed dc-dc converter connected to a three-level NPC which provides multi output voltages for the converter. As described in the previous section, by controlling the proposed dc-dc converter, the input dc-voltage of inverter can be regulated to v_1 and v_2. The following sub-section discusses the operation of the dc-dc converter in steady state.

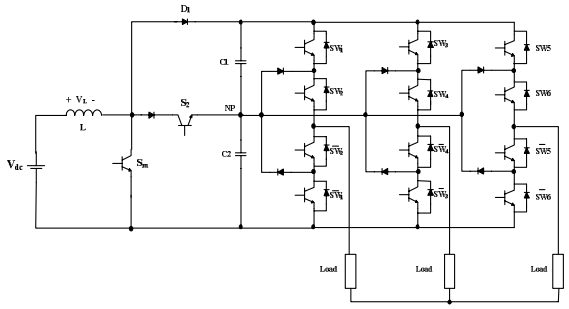


Fig.3: an application of the multi output dc-dc converter topology for a three-level NPC

B. Steady State analysis

With respect to Fig. 2 (b), different operation modes of the circuit are described as follows:

During the subinterval zero, S_m is on and S_2 is off. Fig.4 illustrates the equivalent circuit. The inductor is magnetized by the input current and the capacitors are discharged through the loads. Fig. 5 shows the capacitors currents and the inductor voltage waveforms.

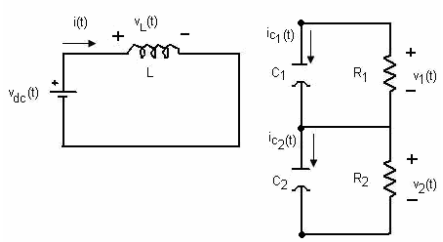


Fig.4.Equivalent circuit in first subinterval.

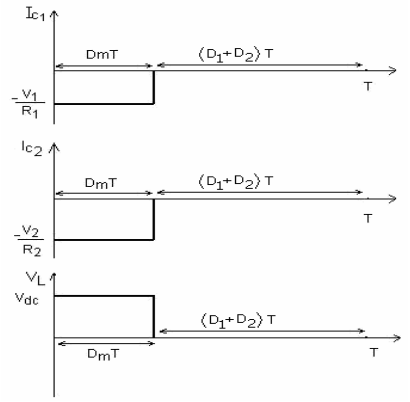


Fig.5.Capacitor currents and inductor voltage in first subinterval.

During the subinterval one, S_m and S_2 are switched off. Fig.6 shows the equivalent circuit. As shown in Fig. 6 and Fig. 7, the capacitors are being charged by the inductor current.

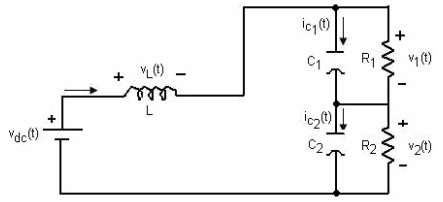


Fig.6.Equivalent circuit in second subinterval.

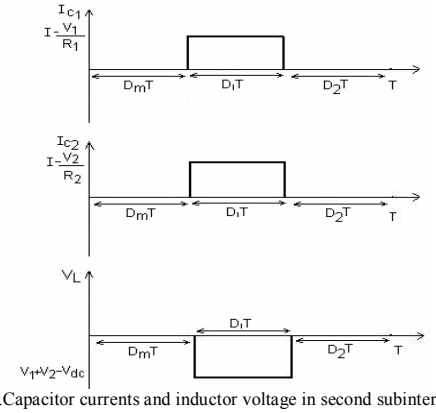


Fig.7.Capacitor currents and inductor voltage in second subinterval.

In subinterval two, S_m is off and S_2 is on. Fig. 8 shows the equivalent circuit. As illustrated in Fig. 9, C_2 is being charged by the inductor current and C_1 is discharging through R_1.

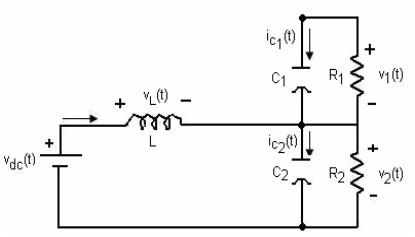


Fig.8.Equivalent circuit in third subinterval.

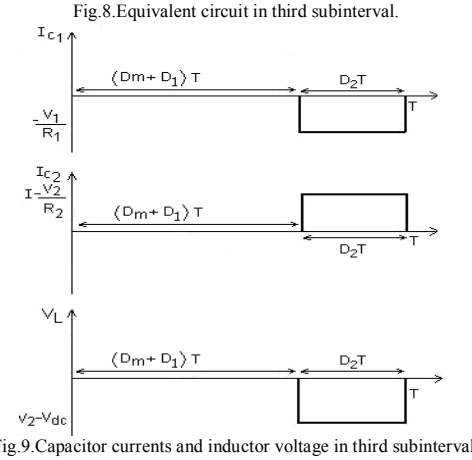


Fig.9.Capacitor currents and inductor voltage in third subinterval.

In the steady state, the average capacitor current over one switching cycle is equal to zero, thus

$$\frac{V_1}{R_1}D_mT-(i-\frac{V_1}{R_1})D_1T+\frac{V_1}{R_1}D_2T=0 \tag{1}$$

$$-\frac{V_2}{R_2}D_mT+(i-\frac{V_2}{R_2})D_1T+(i-\frac{V_2}{R_2})D_2T=0 \tag{2}$$

In above equations, T is defined as a switching period and D_m, D_1, D_2 are duty cycles for subinterval zero, one and two, respectively.

The average inductor voltage over one switching cycle is equal to zero and as a result:

$$V_{dc}D_mT-(V_1+V_2-V_{dc})D_1T-(V_2-V_{dc})D_2T=0 \tag{3}$$

Also

$$D_m+D_1+D_2=1 \tag{4}$$

By solving these three equations we have

$$V_1=\frac{nD_1V_{dc}}{n^2(D_1+D_2)^2+nD_1^2} \tag{5}$$

$$V_2=\frac{n(D_1+D_2)}{D_1}V_1 \tag{6}$$

Where n=R_2/R_1, the following relation holds for the inductor current,

$$I=\frac{(V_2^2R_1+V_1^2R_2)}{V_{dc}R_1R_2} \tag{7}$$

As it can be seen, the output voltages in the steady-state are related to V_{dc}, D_1, D_2 and R_2 to R_1 ratio.

C. Modelling of the circuit based on averaging method

To construct a small-signal ac model at the quiescent operation (I, V_1, V_2), we can assume a small perturbation at the operating point. Thus, the input variables are defined as follow

$$d_1(t)=D_1+\hat{d}_1(t), d_2(t)=D_2+\hat{d}_2(t) \text{ and } v_g(t)=V_g+\hat{v}_g(t)$$

And the output variables are given by

$$v_1(t)=V_1+\hat{v}_1(t), v_2(t)=V_2+\hat{v}_2(t) \text{ and } i(t)=I+\hat{i}(t)$$

Where each variable consists of two parameters, a dc value and a small perturbation signal. Thus, the above equations associated with the inductor voltage and the capacitors currents at different subintervals can be rewritten for this situation. In the subinterval zero (Fig. 2), we have the following equations:

$$v_l(t)=L\frac{di(t)}{dt}=\langle v_g(t)\rangle_T \tag{8}$$

$$i_{C_1}(t)=C_1\frac{dv_1(t)}{dt}=-\frac{\langle v_1(t)\rangle_T}{R_1} \tag{9}$$

$$i_{C_2}(t)=C_2\frac{dv_2(t)}{dt}=-\frac{\langle v_2(t)\rangle_T}{R_2} \tag{10}$$

Likewise from the subinterval one (Fig. 4) the equations are:

$$v_l(t)=L\frac{di(t)}{dt}=\langle v_g(t)\rangle_T-\langle v_1(t)\rangle_T-\langle v_2(t)\rangle_T \tag{11}$$

$$i_{C_1}(t)=C_1\frac{dv_1(t)}{dt}=\langle i(t)\rangle_T-\frac{\langle v_1(t)\rangle_T}{R_1} \tag{12}$$

$$i_{C_2}(t)=C_2\frac{dv_2(t)}{dt}=\langle i(t)\rangle_T-\frac{\langle v_2(t)\rangle_T}{R_2} \tag{13}$$

Also for the subinterval three (Fig. 6), we have:

$$v_l(t)=L\frac{di(t)}{dt}=\langle v_g(t)\rangle_T-\langle v_2(t)\rangle_T \tag{14}$$

$$i_{C_1}(t)=C_1\frac{dv_1(t)}{dt}=-\frac{\langle v_1(t)\rangle_T}{R_1} \tag{15}$$

$$i_{C_2}(t)=C_2\frac{dv_2(t)}{dt}=\langle i(t)\rangle_T-\frac{\langle v_2(t)\rangle_T}{R_2} \tag{16}$$

From (8 to 16), the average amounts of inductor voltage and capacitors currents over one switching cycle are computed as follows:

$$\begin{aligned}L\frac{d\langle i(t)\rangle_T}{dt}&=d_m(t)\langle v_g(t)\rangle_T\\&+d_1(t)\left[\langle v_g(t)\rangle_T-\langle v_1(t)\rangle_T-\langle v_2(t)\rangle_T\right]\\&+d_2(t)\left[\langle v_g(t)\rangle_T-\langle v_2(t)\rangle_T\right]\end{aligned} \tag{17}$$

$$\begin{aligned}C_1\frac{d\langle v_1(t)\rangle_T}{dt}&=-d_m(t)\frac{\langle v_1(t)\rangle_T}{R_1}\\&+d_1(t)\left[\langle i(t)\rangle_T-\frac{\langle v_1(t)\rangle_T}{R_1}\right]-d_2(t)\frac{\langle v_1(t)\rangle_T}{R_1}\end{aligned} \tag{18}$$

$$\begin{aligned}C_2\frac{d\langle v_2(t)\rangle_T}{dt}&=-d_m(t)\frac{\langle v_2(t)\rangle_T}{R_2}\\&+d_1(t)\left[\langle i(t)\rangle_T-\frac{\langle v_2(t)\rangle_T}{R_2}\right]\\&+d_2(t)\left[\langle i(t)\rangle_T-\frac{\langle v_2(t)\rangle_T}{R_2}\right]\end{aligned} \tag{19}$$

As the sum of the duty cycles equals one, we have

$$d_m(t)+d_1(t)+d_2(t)=1 \tag{20}$$

Consequently, by substitution of (14-16) in (17-19), the small-signal equations can be extracted as below:

$$L\frac{d\hat{i}(t)}{dt}=\hat{v}_g(t)-D_1\hat{v}_1(t)-(D_1+D_2)\hat{v}_2(t)-(V_1+V_2)\hat{d}_1(t)-V_2\hat{d}_2(t) \tag{21}$$

$$C_1 \frac{d\hat{v}_1(t)}{dt} = -\frac{\hat{v}_1(t)}{R_1} + D_1\hat{i}(t) + I\hat{d}_1(t) \quad (22)$$

$$C_2 \frac{d\hat{v}_2(t)}{dt} = -\frac{\hat{v}_2(t)}{R_2} + (D_1 + D_2)\hat{i}(t) + I\hat{d}_1(t) + I\hat{d}_2(t) \quad (23)$$

Considering these equations and choosing the capacitors voltages and the inductor current as the state vector variables, where $v_g(t)$ and $d(t)$ are the inputs of small-signal ac model of the system, the ac circuit model can be defined as shown in Fig.10.

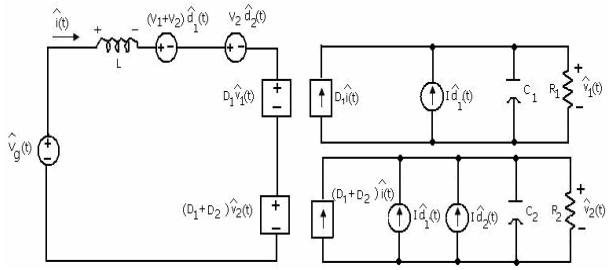


Fig.10: Small-signal ac equivalent circuit model of a multi-output converter

III. Simulation Result

The objective of this section is to verify the proposed topology by comparing the theoretical results for the steady-state and modelling with the simulation results at different conditions and operation modes. As presented in the final equations, in the steady state the output voltages can be controlled by the duty cycles of the switches and the load impedance. In order to consider the effect of the load on the output voltages, simulations have been performed for three different load conditions ($n_1=1$, $n_2=1.5$ and $n_3=0.67$) where $n=R_1/R_2$. The simulation results are shown in Fig. 11 to Fig. 13 for a wide range of variables. These simulation results show that the output voltage can be controlled by suitable duty cycles regardless of changes in the load. Another advantage of this topology is that the dc-dc converter can be either a boost or a buck boost converter.

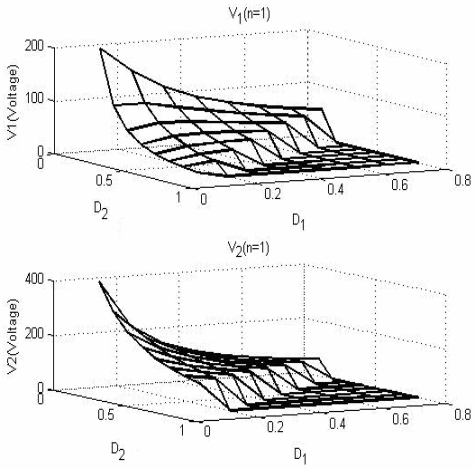


Fig.11.Variation of V_1 and V_2 in terms of D_1 and D_2 for n_1=1

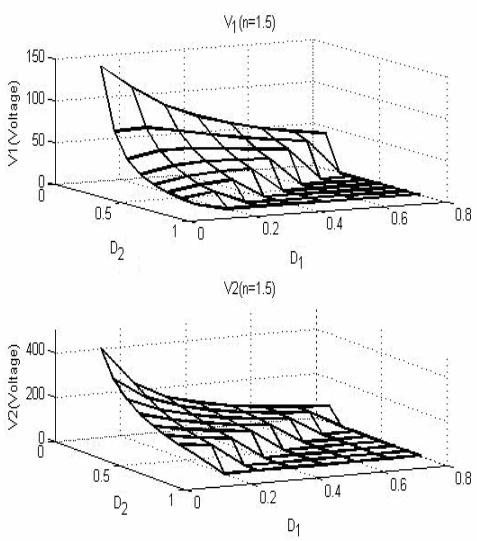


Fig.11.Variation of V_1 and V_2 in terms of D_1 and D_2 for n_2=1.5

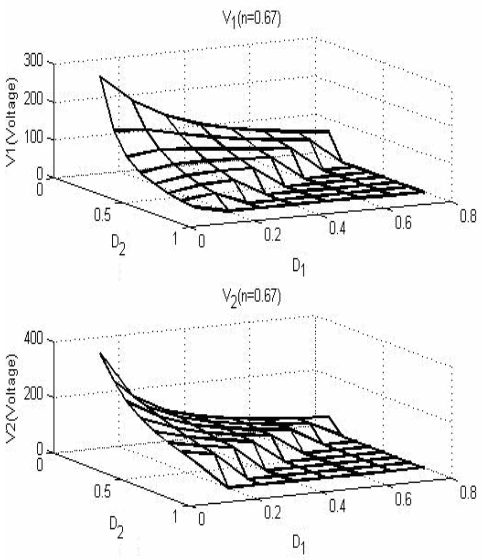
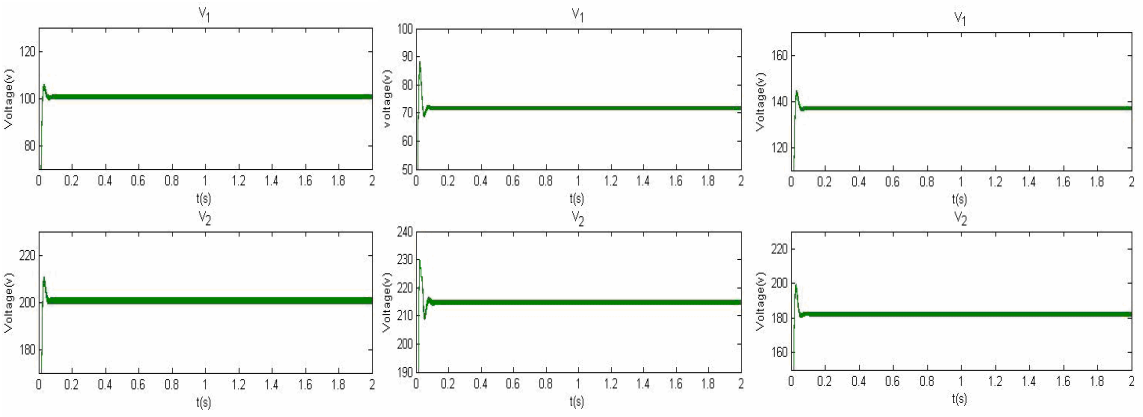


Fig.11.Variation of V_1 and V_2 in terms of D_1 and D_2 for n_3=0.67

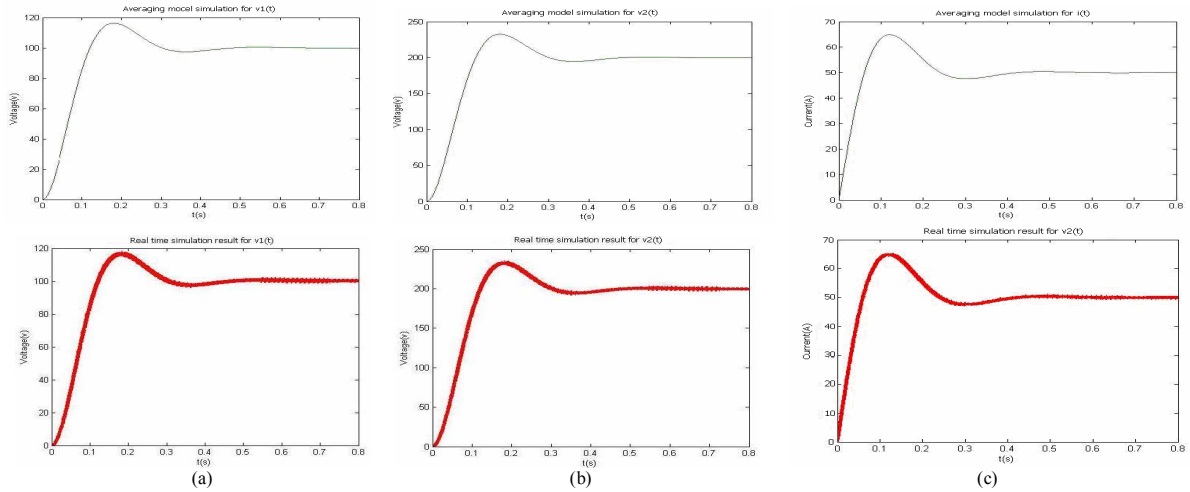
Fig.12 represents the output voltages in simulations for three different load conditions in the steady state, where $T=0.0001s$, $R_1=R_2=10\Omega$, D_1 and D_2 are 0.2. The simulation results confirm the theoretical analysis and the equations for the steady state operation.

In order to verify the small-signal ac model, two different simulations have been carried out in SIMULINK based on the averaging model and the circuit diagram shown in Fig. 13 with ideal components and same capacitors and inductor values. The simulation results are shown in Fig. 13 and the only error between these models are associated with the high frequency part of the signal which is not considered in the averaging techniques. For this case study, the load parameters chosen are $R_1=10\Omega$, $R_2=10\Omega$, D_1 and D_2 are 0.2.



(a) (b) (c)

Fig.12.Output voltages for three load conditions (a) $R_1=R_2$, (b) $R_2=1.5R_1$, (c) $R_1=1.5R_2$.



(a) (b) (c)

Fig.13. waveforms for small-signal ac model and switching circuit model (a) $v_1(t)$, (b)$v_2(t)$, (c)i(t).

IV. CONCLUSION

In this paper, a new topology for a multi output dc-dc converter is presented in order to supply input voltages for a diode-clamp multilevel inverter. Using this circuit, the input voltages of the NPC can be adjusted to a desired voltage level by the dc-dc converter thereby solving the main problem associated with balancing the capacitors voltages in the NPC topology. Furthermore, since the dc output voltage of PV or wind turbine systems are not very high, this topology is a suitable candidate for these systems as it can boost the input voltage for a transformer less grid connection based on the multilevel topology. To verify the operation of this topology, both steady-state and small-signal ac model have been compared through simulation.

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