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Tertiary Control for Optimal Unbalance Compensation in Islanded Microgrids

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***Abstract*— In order to achieve desirable power quality in the critical bus (CB) in microgrids, primary and secondary control can be used to realize unbalance compensation and at the same time, to make distributed generators (DGs) share the compensation efforts. Considering that the power quality requirements in different areas and for different consumers can be different, this paper implements a tertiary control over secondary and primary control levels so as to achieve optimal unbalance compensation control. Hardware-in-the-loop results are presented to demonstrate the effectiveness of the method.**

***Index Terms*—Microgrid, tertiary control, voltage unbalance compensation, multi-power-quality-level**

I. Introduction

As a way of actualizing the new paradigm of distribution, microgrid concept was proposed for liberalizing the operation of each system fraction so as to make proper use of distributed generators (DGs) [1]. However, the increasing number of DGs brings challenges for stability, reliability and power quality issues. Also the performance of unbalance voltage sensitive equipment, such as induction motors, is deteriorated. Conventionally, series active power filter can be a solution for compensating unbalances by adding negative sequence voltage in series with the distribution line [2]. In some works shunt active filters are used to inject current so as to balance the current and to compensate unbalances [3].

In case of islanded microgrids, DG units can be employed as active filters and compensators so as to make full use of them. In addition, the compensation efforts can be shared among DGs so as to distribute the current of a single compensator under severe unbalance conditions. hierarchical control is proposed so as to compensate unbalance voltage in the point of common coupling (PCC) in an islanded system [4]. However, the power quality in DG terminals and other buses is sacrificed. The compensation limitation of each DG and the deterioration of power quality in other buses are also not considered. Apart from technical issues, power quality related economic issues should also be considered. For instance, the power quality requirements are unequal in different areas and for different consumers. It can be more convenient to differentiate the power quality levels for different types of electric consumers. A project in the Consortium for Electric Reliability Technology Solutions (CERTS) [5] and a four-year project in Sendai, Japan, [6] have demonstrated the need for multiple power quality service for future grids.

In order to achieve multi-power-quality-level (MPQL) control in islanded microgrids this paper proposes a tertiary control, which inherently is an optimization method, on the basis of secondary and primary control for unbalance compensation. The paper is organized as follows. Section II introduces the proposed hierarchical control for unbalance compensation and MPQL control. Section III analyzes and models the unbalanced system. A 2-DG, 3-bus microgrid is also described and taken as the example system in this study. Based on this model, Section IV formulates the mathematical model for optimization. Hardware-in-the-loop results in Section V demonstrate the effectiveness of the method. Section VI gives conclusion.

II. Hierarchical Control for Voltage Unbalance Compensation and MPQL Control

The hierarchical control for microgrids is defined in [7]. Based on this definition, this paper establishes a hierarchical control for actualizing unbalance compensation and MPQL control, as shown in Fig. 1. An example islanded system is outlined in the *PLANT* part depicted in Fig. 1. The DG power stage is represented by a power electronics inverter. One or more DG units are connected to a local bus (LB) to supply local loads. A critical bus (CB), which contains critical loads and power-quality sensitive loads, may exist in the system. In order to keep the safe operation of the system and also for protecting critical loads in CB, DG units should ensure that CB has the highest power quality. However, voltage unbalances may appear when unbalanced load is connected, causing unbalance voltage in different buses. In order to achieve better power quality in the CB, DG units can be employed as distributed active compensators to share the compensation efforts by means of secondary control and primary control. Furthermore, considering the distribution line differences, DG compensation capabilities, as well as different power quality requirements in DG side and other buses, a tertiary control can be implemented to differentiate the compensation efforts among DG units so as to achieve optimal operation objectives.

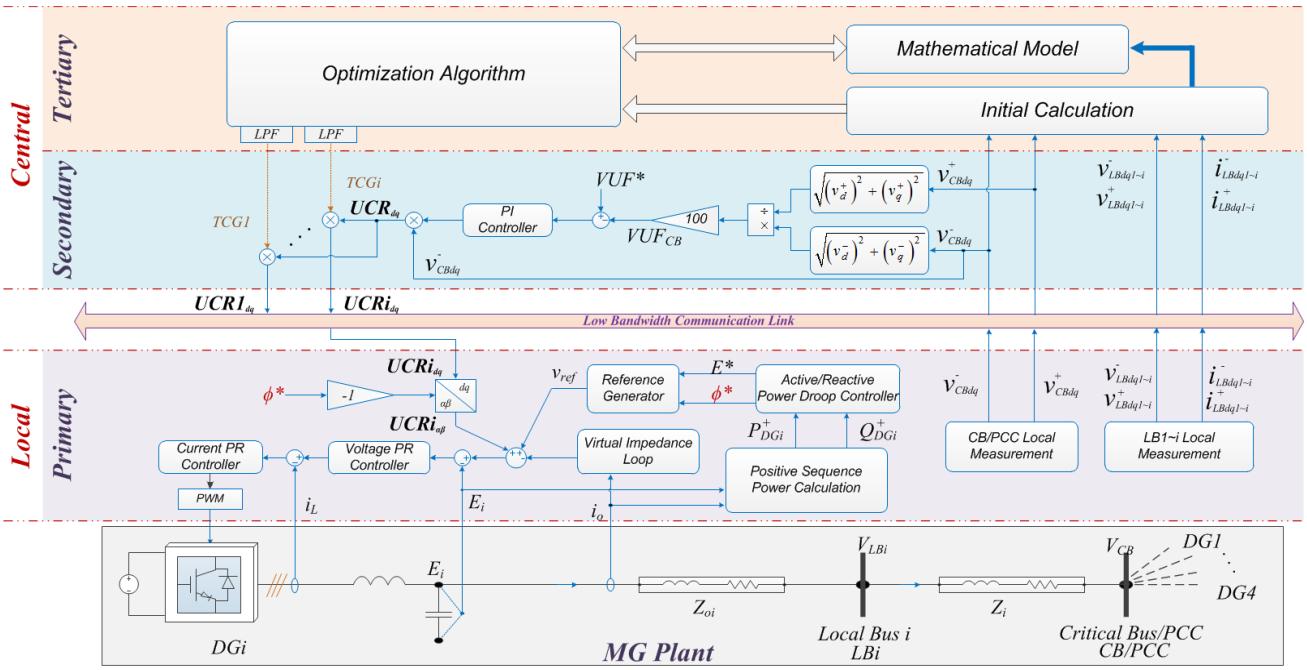


Fig. 1. Hierarchical control scheme for unbalance compensation and MPQL control.

A. Primary Control and Inner Control Loops

The control structure of local controller is shown in the *Primary* block in Fig. 1, which includes current and voltage control loops, active and reactive power droop control loops and virtual impedance loops. All the control loops are designed in $\alpha\beta$ frame. The output active and reactive power of the inverter is first calculated based on the instantaneous power theory [8]. Positive sequence active and reactive power (P^+ and Q^+) can be extracted by using low pass filters (LPF) [4]. The calculated P^+ and Q^+ are then used by droop controller for P^+/Q^+ sharing control. In addition to droop control, a virtual impedance loop is implemented in this paper to help the decoupling of P and Q, and make the system more damped without sacrificing system efficiency. In order to track non-dc variables, proportional-resonant controllers can be used to control voltage and current in the stationary reference frame. The detailed designing and description of the primary control loops can be found in [4].

B. Secondary Control Loop

Secondary control loop deals with unbalance compensation of critical bus voltage by sending UCR_{dq} to local controllers through *low bandwidth communication links*. As shown in Fig. 1, the positive and negative sequence voltage on CB (v^+_{CBdq} and v^-_{CBdq}) are first measured locally and sent to MG central controller. *VUF* at CB can be calculated as follows [9]:

$$VUF_{CB} = 100 \cdot \sqrt{\frac{(v^-_{CBd})^2 + (v^-_{CBq})^2}{(v^+_{CBd})^2 + (v^+_{CBq})^2}} \qquad (1)$$

The error between calculated *VUF* and desired VUF^* is fed to a proportional-integral (*PI*) controller. Afterwards, the output of *PI* controller is multiplied by v^-_{CBdq} to generate the common compensation reference UCR_{dq} [4]. In each local primary controller, the UCR_{dq} is transformed to $\alpha\beta$ frame where $-\phi^*$ is used as the rotation angle as the transformation is executed over negative sequence values.

C. Tertiary Control Loop

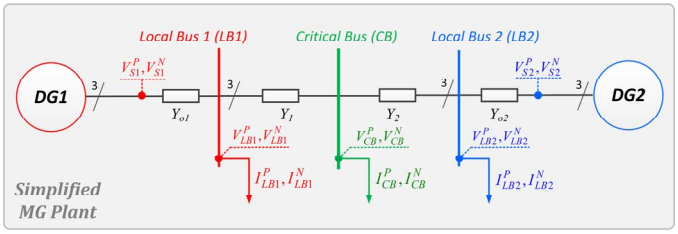
With secondary control the compensation can be performed and equally shared among DGs. However, considering DG compensation limitations and power quality requirements in different LBs, the compensation efforts can be differentiated by multiply a *TCG* to the common compensation reference UCR_{dq}.

With centralized control system, essential information can be collected by using data acquisitions and communications so as to execute optimization functions which decides the optimal values of *TCGs*. The optimization objective in this paper is that according to the different unbalance limits of different buses, the *VUF* in different LBs is controlled to different levels by changing individual *TCG*s. However, there is no simple relationship between *TCG* and *VUF* values, in other words, the challenges are the modeling and simplification of the unbalance system as well as the formulation of the mathematical problem handled by the optimization algorithm. Accordingly, mathematical model and optimization algorithm are required in tertiary level.

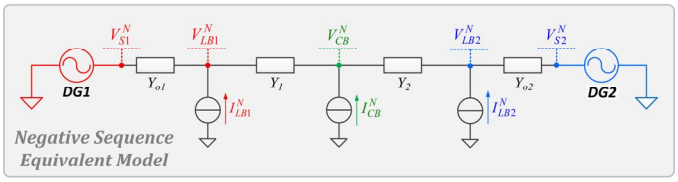
III. Unbalance System Modeling

As radial networks are often used in microgrids, a 2-DG 3-Bus islanded system is taken as an example. Its single-line diagram is shown in Fig. 2 (a). The transmission line admittance can be estimated as Y_{o1}, Y_1 and Y_{o2}, Y_2. A negative sequence equivalent circuit is built, as shown in Fig. 2 (b), so as to analyze negative sequence voltage changes in each bus.

Assuming the presence of unbalanced loads, as that shown in Fig. 3 in different buses, the sequence quantities of the system can be calculated based on classical methods [10]:



(a) Example of islanded microgrid



(b) Negative Sequence Equivalent Model

Fig. 2. Example system and its negative sequence equivalent circuit.

$$\begin{cases} Y_s = A^{-1} \cdot Y_p \cdot A \\ V_s = A^{-1} \cdot V_p \\ I_s = Y_s \cdot V_s \end{cases} \tag{2}$$

where Y_p and V_p are respectively the admittance matrix and phase voltage in 3-phase system, Y_s, V_s and I_s are respectively the sequence admittance matrix, sequence voltage and sequence current, and A is the transformation matrix between 3-phase system and sequence system. The detailed matrix can be found in the *Appendix*. The positive and negative sequence currents can be obtained by solving (2):

$$\begin{cases} \dot{I}^P = \dot{V}^P \cdot Y + (\dot{V}^P - a \cdot \dot{V}^N) \cdot Y_u \approx \dot{V}^P \cdot Y + \dot{V}^P \cdot Y_u \\ \dot{I}^N = \dot{V}^N \cdot Y + (\dot{V}^N - a^2 \cdot \dot{V}^P) \cdot Y_u \approx -a^2 \cdot \dot{V}^P \cdot Y_u \end{cases} \tag{3}$$

where $\dot{I}$ and $\dot{V}$ are respectively the current and voltage phasors, the superscripts P and N denote the positive- and negative-sequence quantities respectively. Y and Y_u are the admittances shown in Fig. 3, a is equal to $1\angle 120°$. As the positive sequence voltage is usually much larger than negative sequence voltage, V_S^N can be neglected.

Based on the equivalent model and assuming that positive- and negative-sequence voltage and current can be measured locally and sent to central controller in *dq* reference frame for tertiary optimization, the negative-sequence electrical relationship among buses can be established based on Fig. 2 (b) as follows:

$$\dot{V}_{LB1}^N = (\dot{V}_{S1}^N \cdot Y_{o1}^N + \dot{V}_{CB}^N \cdot Y_1^N + \dot{I}_{LB1}^N) / (Y_1^N + Y_{o1}^N) \tag{4}$$

$$\dot{V}_{LB2}^N = (\dot{V}_{S2}^N \cdot Y_{o2}^N + \dot{V}_{CB}^N \cdot Y_2^N + \dot{I}_{LB2}^N) / (Y_2^N + Y_{o2}^N) \tag{5}$$

$$\dot{V}_{CB}^N = \frac{\dot{I}_{CB}^N + K_1 \cdot \dot{I}_{LB1}^N + K_2 \cdot \dot{I}_{LB2}^N + K_3 \cdot \dot{V}_{S1}^N + K_4 \cdot \dot{V}_{S2}^N}{K_3 + K_4} \tag{6}$$

where the superscript N denotes negative sequence quantities, V_{S1} and V_{S2} are the voltages at DG sides, V_{LB1} and V_{LB2} are the voltage at LB1 and LB2, V_{CB} is the voltage at CB, Y_{o1}, Y_{o2}, Y_1 and Y_2 are the admittances of distribution lines. K_1, K_2, K_3, K_4 are constants (see *Appendix*).

A simplified compensation process can be sketched from (4), (5) and (6), as shown in Fig. 4. The V_S^N axis denotes the negative sequence voltage at both DG sides while the V_B^N axis

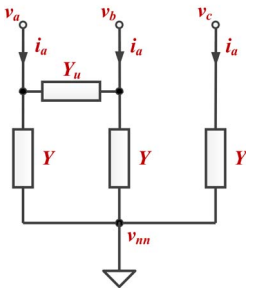


Fig. 3. Unbalanced load equivalent circuit in 3-phase 3-wire system.

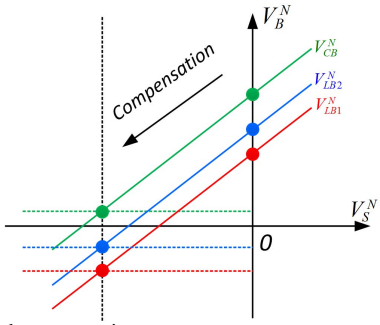


Fig. 4. Simplified compensation process.

denotes the negative sequence voltage at buses. Assuming a case that $Y_1 < Y_2 < Y_{o1} = Y_{o2}$, it can be observed that without compensation ($V_S^N = 0$), the negative sequence voltage on CB and LBs is high, and the negative sequence voltage on LB2 is higher than at LB1 because of the distribution line differences. The secondary compensation control is actually adjusting the negative sequence voltage at DG side toward negative direction so as to reduce the negative sequence voltage in CB and LBs. After compensation, the negative sequence voltage at CB is kept at a low level, while the negative sequence voltage at LB1 and LB2 can be also lower but has inversed direction before and after compensation.

In addition, from (4) and (5) we can see that by adjusting V_{S1}^N and V_{S2}^N the negative sequence voltage in LB1 and LB2 (V_{LB1}^N and V_{LB2}^N) can be modified.

As the total amount of compensation effort ($V_{S_total}^N$) is automatically controlled by secondary control aiming at compensating the unbalance level on CB to a fixed low level, $V_{S_total}^N$ can be obtained by either measuring the total negative sequence voltage at all the DG sides or acquiring from the output of secondary control. *TCG*s can be used as decision variables for changing the compensation efforts of each DG unit by applying:

$$V_{Si}^N = \frac{TCG_i}{\sum TCGs} \cdot V_{S_total}^N \tag{7}$$

which means the negative sequence voltage at the ith DG side (V_{Si}^N) is decided by the ratio of TCG_i compared with the total amount of *TCG*s. Based on (4)~(7), tertiary optimization can be implemented to vary the sharing ratio of compensation efforts according to the power quality requirements on different local buses (LB1 and LB2) as well as the limitation of unbalance level at DG side.

TABLE I. POWER STAGE AND MG PLANT PARAMETERS

Inverter Output Filter		**MG Plant Transmission Lines**				
L (mH)	*C (μF)*		*Y_{o1} (S)*	*Y_{o2} (S)*	*Y_1 (S)*	*Y_2 (S)*
1.8	*25*	*Positive Sequence*	*0 - j1.7684*	*0 - j1.7684*	*0.1096 - j0.4130*	*0.3032 - j1.7148*
		Negative Sequence	*0 + j1.7684*	*0 + j1.7684*	*0.1096 + j0.4130*	*0.3032 + j1.7148*

TABLE II. CENTRAL CONTROL SYSTEM PARAMETERS

Secondary Controller		**Tertiary Controller**									
k_p	k_i	k_F	k_{GLB}	k_{GDG}	k_{GC}	L_{LB1}	L_{LB2}	L_{DG1}	L_{DG2}	L_{C1} (A)	L_{C2} (A)
1.8	*25*	*1*	*10*	*10*	*100*	*3*	*1*	*4*	*4*	*14*	*14*
*VUF**		k_{LB1}	k_{LB2}	r_{LB1}	r_{LB2}	r_{GB1}	r_{DG2}	r_{C1}	r_{C2}	*Optimization Step*	
0.25		*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*0.5 s*	

IV. OPTIMIZATION PROBLEM FORMULATION

Based on the analysis and the model built above, in order to actualize MPQL control in an islanded system, an optimization problem can be formulated. As CB is the most sensitive bus in the system, secondary control is in charge of keeping the best power quality on CB. *TCG*s can be used as decision variables for changing the *VUF* on different LBs.

A. Objective Function

The objective function F_{obj} can be established to differentiate the power quality level of LBs, defined as [11]:

$$F_{obj} = \sum_{i=2}^{m} (k_{LB1} \cdot VUF_{LB1} - k_{LBi} \cdot VUF_{LBi})^{\alpha} \tag{8}$$

where VUF_{LBi} is the *VUF* on i^{th} LB, α is a constant set to 2, m the is total number of controlled buses, and the coefficients k_{LBi} denotes the relative importance of ith LB. The objective is actually to control the *VUF* on i^{th} LB to a proportional level compared with the reference LB (LB1).

B. Constraints

The constraints of this optimization problem can include: (a)*VUF* at each LB (VUF_{LBi}, $i=1,2,\ldots,n$) is limited to a certain value L_{LBi}; (b)*VUF* at each DG side (VUF_{DGi}, $i=1,2,\ldots,n$) is limited to a certain value L_{DGi}; (c)DG phase current (I_{oabci}, $i=1,2,\ldots,n$) are bounded to L_{Ci}. The constraint functions are formulated as follows [11],[12]:

$$(a)\ G_{LB} = \sum_{i=1}^{n} r_{LBi} \cdot \max(0, VUF_{LBi} - L_{LBi}) \tag{9}$$

$$(b)\ G_{DG} = \sum_{i=1}^{n} r_{DGi} \cdot \max(0, VUF_{DGi} - L_{DGi}) \tag{10}$$

$$(c)\ G_{C} = \sum_{i=1}^{n} r_{Ci} \cdot \max(0, I_{oabci} - L_{Ci}) \tag{11}$$

where r_{LBi} is the penalty factor for the *VUF* violation on the ith LB, r_{DGi} is the penalty factor for the *VUF* violation on the ith DG, r_{Ci} is the penalty factor for the violation of phase current constraint of ith DG. These penalty factors denote the relative importance of different constraints.

The limits L_{LBi}, L_{DGi} and L_{Ci} are defined by operators. VUF_{LBi} and VUF_{DGi} can be calculated according to (1), (4)~(6). In order to predict the phase current I_{oabci}, the negative sequence current of the DG unit is first calculated:

$$\dot{I}_{Si}^{N} = (\dot{V}_{Si}^{N} - \dot{V}_{LBi}^{N}) \cdot Y_{oi}^{N} \tag{12}$$

where $\dot{V}_{Si}^{N}$ and $\dot{I}_{Si}^{N}$ are the negative sequence output voltage and current of ith DG, $\dot{V}_{LBi}^{N}$ is the negative sequence voltage at i^{th} LB, Y_{oi}^{N} is the negative sequence line impedance between the DG and the LB. $\dot{V}_{Si}^{N}$ and $\dot{V}_{LBi}^{N}$ can be calculated according to (4), (5) and (7), Y_{oi}^{N} can be estimated with acceptable error. As the positive sequence current $\dot{I}_{Si}^{P}$ is not affected by compensation, it can be measured locally and sent to central controller. Phase current of the ith DG can be calculated as:

$$\begin{bmatrix} \dot{I}_{oai} & \dot{I}_{obi} & \dot{I}_{oci} \end{bmatrix}^{T} = A \cdot \begin{bmatrix} \dot{I}_{Si}^{Z} & \dot{I}_{Si}^{P} & \dot{I}_{Si}^{N} \end{bmatrix}^{T} \tag{13}$$

where $\dot{I}_{oai}$, $\dot{I}_{obi}$ and $\dot{I}_{oci}$ are the phase current of ith DG, $\dot{I}_{Si}^{Z}$ is the zero sequence current (it can be neglected in this case).

C. Combined Objective Function with Constraints Included

As genetic algorithm is used in this paper, the objective function and constraints are integrated in to a combined objective function defined as:

$$F = k_F \cdot F_{obj} + k_{GLB} \cdot G_{LB} + k_{GDG} \cdot G_{DG} + k_{GC} \cdot G_C \tag{14}$$

where F is the objective function with constraints integrated, F_{obj}, G_{LB}, G_{DG} and G_C are defined above. k_F, k_{GLB}, k_{GDG} and k_{GC} are the coefficients defining the influence of these objectives and constraints. For strict constraints, the penalty coefficients are usually set much larger than other ones.

In addition, as *TCG*s are used as decision variables, in order to keep the total amount of compensation efforts, the total amount of *TCG*s has to be fixed.

V. HARDWARE-IN-THE-LOOP RESULTS

In order to verify the effectiveness of the method, hardware-in-the-loop (HIL) simulation is conducted. The example system is shown in Fig. 3. The parameter settings are given in Tables I and II. In the *Tertiary Controller* part, the coefficients k_{GLB}, k_{GDG} and k_{GC} are relatively much larger than objective function coefficient k_F so as to prevent the violation of limits. The *VUF* limits on LB1 and LB2 (L_{LB1} and L_{LB2}) are

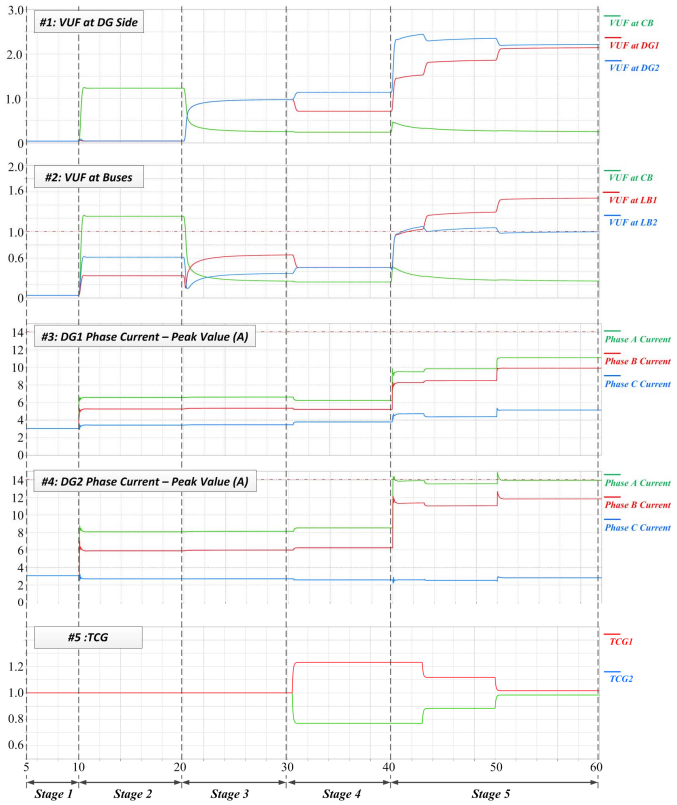


Fig. 5. Simulation Process.

set to 3% and 1% respectively, which means LB2 has a relatively higher power quality requirement than LB1. On DG side the *VUF* limitation (L_{DG1} and L_{DG2}) and phase current limitation (L_{C1} and L_{C2}) are respectively set to 4% and 14A (peak value) for both DGs. The coefficients k_{LB1} and k_{LB2} are set to 1 which means that if no constrain is violated the optimization control tends to control the *VUF* in LB1 and LB2 to the same level. Note that the ratio of k_{LB1} and k_{LB2} can be changed according to the relative importance of the buses.

As constraints and objective function are integrated into one function, genetic algorithm is used for searching for global optimum. A load changing process is given to MG plant to test the effectiveness of the method. The simulation results are shown in Fig. 5, from *Stage 1* to *Stage 5* different load conditions and control levels are activated in sequences.

A. Stage 1: Only balanced Loads

During *Stage 1*, no unbalanced load is connected to the system, only balanced 3-phase loads are connected in LB1, LB2 and CB. Voltage on DG sides and buses are all balanced and the phase currents are also balanced.

B. Stage 2: Unbalance Loads Connected to CB

During *Stage 2*, an unbalance load (Y_u=*0.0167 S*) is connected on CB which causes the increasing of *VUF* on CB, LB1 and LB2 (VUF_{CB}=1.23, VUF_{LB1}=0.33, VUF_{LB2}=0.62), while the *VUF* on DG sides remain unchanged. And because of the difference of transmission lines, *VUF* on LB1 and LB2 are different. LB2 undergoes more severe unbalance compared with LB1, because the transmission line between LB2 and CB has relatively smaller impedance than the one between LB1 and CB. This result is in accordance with the analysis in Fig. 5 that before compensation ($V_S^N = 0$), V_{LB2}^N is larger than V_{LB1}^N.

C. Stage 3: Secondary Compensation Activated

During *Stage 3*, secondary compensation control is activated to compensate the unbalance on CB, *VUF* on CB is decreased, while *VUF* on DG sides are increased (VUF_{CB}=*0.25*, VUF_{DG1}=*1*, VUF_{DG2}=*1*). However, VUF_{LB1} becomes larger than VUF_{LB2} after compensation (VUF_{LB1}=*0.65*, VUF_{LB2}=*0.37*). This process is also demonstrated in Fig. 4 that after compensation the negative sequence voltage at LB1 and LB2 are changed to inverse direction and the absolute value of VUF_{LB1} is larger than VUF_{LB2}.

D. Stage 4: Tertiary Optimization Activated

During *Stage 4*, tertiary optimization control is activated. Here the objective is to control *VUF* on LB1 and LB2 to a fixed ratio (*1:1*). It can be seen in Fig. 5 that during *Stage 4*, the phase currents are all less than the limit value 14A, *VUF* at LBs and DG sides are all within limit value, so that no constraint is violated, thus VUF_{LB1} and VUF_{LB2} are controlled to *0.46* equally which is in accordance with the pre-set ratio *1:1*. This change is achieved by the adjustment of *TCG1* and *TCG2* (changed to *0.77* and *1.23*) so as to adjust the compensation efforts of DG1 and DG2. It can be seen from *#1* in Fig. 5 that the *VUF* at DG sides are changed to 0.71 and 1.14 whose ratio is equal to the ratio between *TCG1* and *TCG2*. According to simulation results, by decreasing $\dot{V}_{S1}^N$ while increasing $\dot{V}_{S2}^N$, the *VUF* on LB1 is decreased and the *VUF* in LB2 is increased while the *VUF* on CB is kept at 0.25%.

The objective function is plotted in Fig. 6 regarding *TCG* values, the optimization is to minimize the objective function (the solution in dark green part). The diagonal dashed line is the constraint of total compensation efforts (*TCG1+TCG2=2*), which means the final solution has to be located on this line. The final solution during this phase is given as (*0.77, 1.23*) located in the middle of dark green part and on the diagonal line which demonstrates that the solution given by the optimization algorithm is located at the optimum point.

E. Stage 5: More Unbalance Load Added to CB

During *Stage 5*, more unbalance load is added to CB. It can be observed in Fig. 5 that after the loading process, *VUF* on CB is fast restored to the low level (0.25%) by secondary compensation while the *VUF* in DG terminals and LBs are all increased. However, *VUF* in LB2 exceeds the limitation of 1 (see 40s~50s in *#2* in Fig. 5). Also at 50s, the phase A current of DG2 is going to exceeds the limits of 14A. Tertiary control detects the violation of constraints and readjusts the *TCG* values so as to keep *VUF* on LB2 less than 1. Around 50s, *TCG*1 and *TCG*2 are changed to *0.98* and *1.02* respectively and the system enters steady state. During steady state, the DG phase currents, *VUF* values at DG sides and LBs are all within limitations. *VUF* at CB is kept at 0.25.

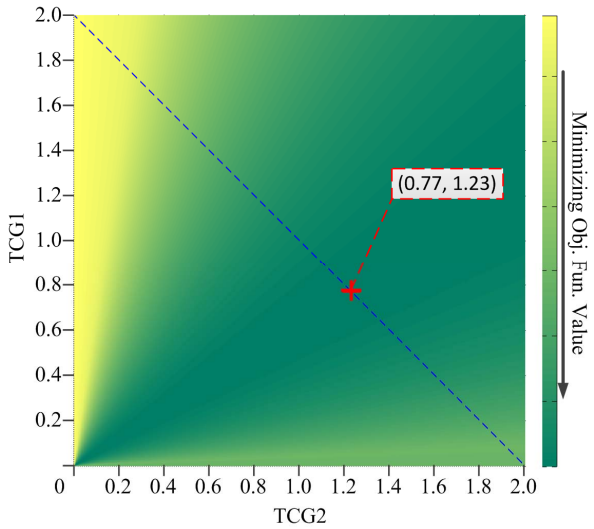


Fig. 6. Optimization results in stage 4.

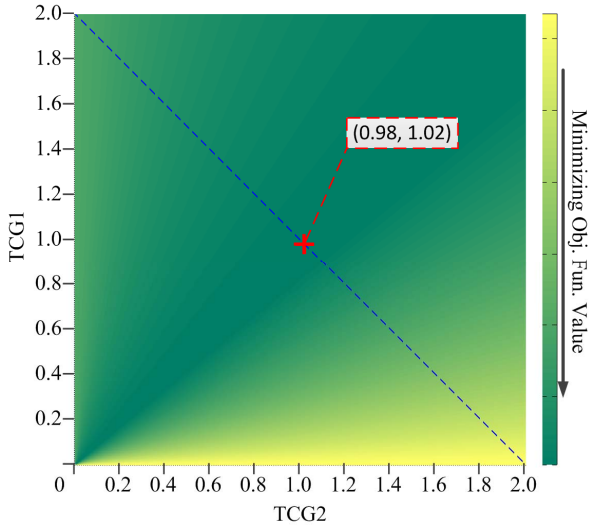


Fig. 7. Optimization results in stage 5.

In Fig. 7, the objective function is plotted under this load condition, the solution given by the algorithm (*0.98, 1.02*) is demonstrated to be located at the global minimum point.

VI. Conclusion

This paper proposes a hierarchical control to realize MPQL control for unbalance compensation in microgrids. The proposed hierarchy includes three levels: primary level for negative sequence power sharing control, secondary level for unbalance compensation control and tertiary level for global power quality optimization. HIL simulation results are presented to demonstrate that the proposed method is capable of controlling the unbalance level on each bus according to their limits and power quality requirements. This method realizes accurate unbalance control among buses in an islanded system considering different power quality requirements of the buses and compensation limits of DGs. This method also enables the possibility of higher level scheduling and management for power quality control in microgrids so as to realize economic and technical objectives.

VII. Appendix

The detailed matrices used in (2) are described as follows:

$$Y_p = \begin{bmatrix} Y+Y_u & -Y_u & 0 \\ -Y_u & Y+Y_u & 0 \\ 0 & 0 & Y \end{bmatrix}, V_p = \begin{bmatrix} V_a - V_{nn} \\ V_b - V_{nn} \\ V_c - V_{nn} \end{bmatrix}, A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}$$

The detailed parameters used in (6) are described as follows:

$$K_1 = \frac{Y_1^N}{Y_1^N + Y_{o1}^N},\ K_2 = \frac{Y_2^N}{Y_2^N + Y_{o2}^N},\ K_3 = K_1 \cdot Y_{o1}^N,\ K_4 = K_2 \cdot Y_{o2}^N$$

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