

Hybrid-Source Impedance Network and Its Generalized Cascading Concepts

Ding Li¹, Feng Gao¹, Poh Chiang Loh¹, Frede Blaabjerg², and Kuan Khoo Tan¹

¹School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore

²Institute of Energy Technology, Aalborg University, Denmark

Abstract—Hybrid-source impedance networks have attracted attention among researchers because of their flexibility in performing buck-boost energy conversion. To date, three distinct types of impedance networks can be summarized for implementing voltage-type inverters, with another three types summarized for current-type inverters. These impedance networks can in principle be combined into a single generic network entity, before generalized cascading concepts are proposed for connecting multiple of them together to form energy converters with a higher output voltage gain and other unique advantages. It is anticipated that these concepts and their formed inverters can find applications in photovoltaic and other renewable systems, which in turn motivate the investigation initiated here on two-level and three-level generalized cascading concepts. In addition to their theoretical performance merits, practical shortcomings and relevant transient phenomena exhibited by the generalized concepts are discussed to provide a comprehensive knowledge base needed for weighing relevant tradeoffs before deciding on a particular application.

Index Terms—Cascading concepts; Hybrid-Source inverter; Z-source inverter

I. INTRODUCTION

Voltage-type Z-source inverter shown in Fig. 1 is first proposed in [1], where unlike traditional voltage-source inverter (VSI) and current-source inverter (CSI), it supports both voltage-buck and boost operating modes by including a unique X-shaped LC impedance network between the dc input source and rear-end inverter circuitry. Unlike traditional two-stage buck-boost inverter where a dc-dc boost converter and a dc-ac inverter can clearly be identified, the Z-source inverter can be viewed as an integrated single-stage solution, where some semiconductor switching actions needed for dc-dc energy conversion are neatly integrated into the dc-ac inverter. Considering voltage-boost operation for example where an inductive element must either be shorted across a voltage source or a capacitive element, the necessary shorting action for the two-stage converter can be effected by turning ON the relevant switch found in the front-end dc-dc converter with the rear-end inverter switches less untouched. In contrast, this necessary short-circuiting action for a Z-source inverter can only be effected within the dc-ac inverter bridge by turning ON any two switches from the same phase (e.g. SA and SA' in Fig. 1), since no front-end switch can be explicitly found in the circuitry. This inserted shoot-through state, together with the eight traditional active and null states commonly assumed by a VSI, allows the Z-source inverter to boost its output voltage without causing damagingly large current to flow as long as the shoot-through duration is not considerably

long. It therefore is a safer circuitry than the traditional VSI, and does not require dead-time delay for protection.

As an extension, Z-source current-type inverter, representing the dual of the voltage-type Z-source inverter, is proposed in [2], and shown in Fig. 2. In addition to the traditional nine active and null states, the added impedance network allows current following into the dc-link of the inverter bridge to be broken to create an open-circuit state without causing severe overvoltage (e.g. by turning OFF all switches of the CSI bridge). This open-circuit state is in fact responsible for introducing voltage-buck (or current-boost) functionality to the otherwise only voltage-boost (or current-buck) CSI. So far, the current-type Z-source inverter has not been as popular as its voltage-type counterpart, which so far has already been applied to motor drives, photovoltaic and fuel cell powered systems [3-5] requiring either a wide input or output variation range. To provide more options for these applications, alternative embedded [6] or quasi [7] Z-source inverters have also been proposed, whose similarities and differences when compared with the traditional Z-source inverter are discussed in the next section, before generalizing them to develop an elementary network entity. This attempt has not been pursued by past researchers, and has the advantage of creating a new family of buck-boost hybrid-source inverters (hybrid-source in the sense that both L and C elements are present) with a higher voltage gain, by simply cascading multiple of the identified network

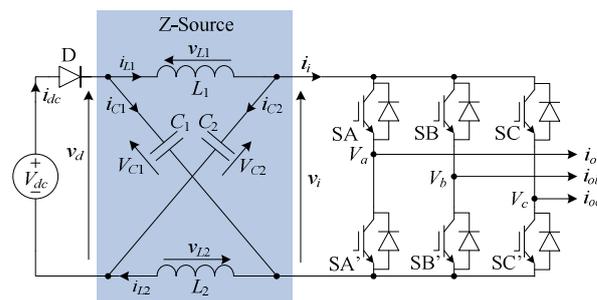


Fig. 1. Voltage-type Z-source inverter.

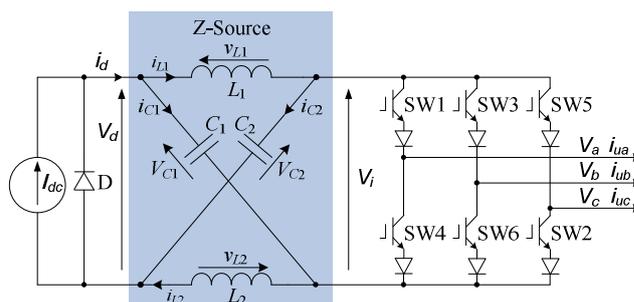


Fig. 2. Current-type Z-source inverter.

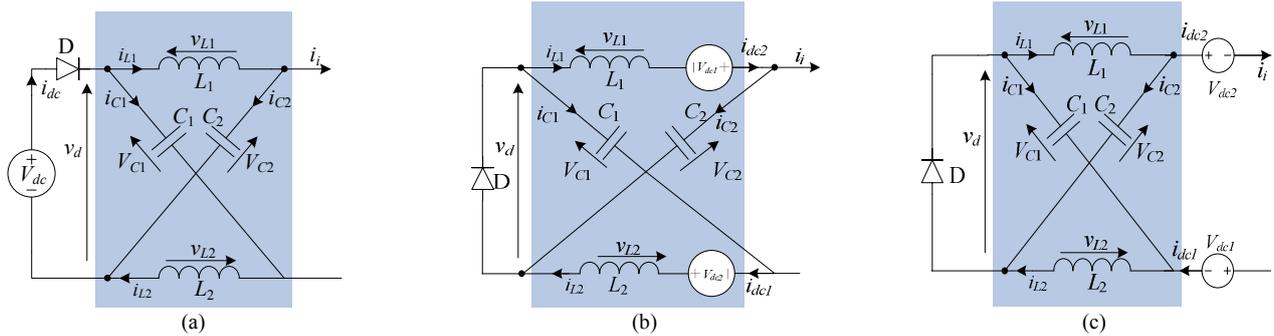


Fig. 5. Impedance networks used in (a) traditional Z-source inverter, (b) embedded Z-source inverter and (c) dc-link embedded Z-source inverter.

entities. Needless to say, cascading of more passive elements introduces more parasitic components to the inverters, and affects its dynamic response when subject to a transient step event. These effects are also discussed in the paper for comprehensiveness, and to provide a better informed guide to readers on the generalized concepts of cascading hybrid-source network entities to implement inverters with higher gain. For verifying the presented concepts, experimental testing was performed with some captured results presented in the paper.

II. HYBRID-SOURCE NETWORK ENTITY

Fig. 5 shows three impedance networks that have so far been proposed for realizing traditional, embedded and dc-link embedded voltage-type Z-source inverters. (Rear-end inverter bridges of all the impedance networks are not shown since they simply represent a traditional VSI circuitry). Viewing them side by side, the single obvious difference noted between them is the placement of their input dc sources, where for the network shown in Fig. 5(a) representing the first variant reported in [1], it is located at the far-left before the input diode D . Since the input source is in series with D , current drawn from it is expected to be chopping by nature, which in practice needs to be smoothed by using an external LC filter, especially for cases where clean sources like photovoltaic and fuel cells are used. Adding the filter would however raise the overall cost of the system, and might at times introduce additional LC resonant complication to the system.

That then motivates the development of the embedded impedance network drawn in Fig. 5(b), where the sources are drawn in series with inductors L_1 and L_2 . The resulting series connection causes currents drawn from the sources

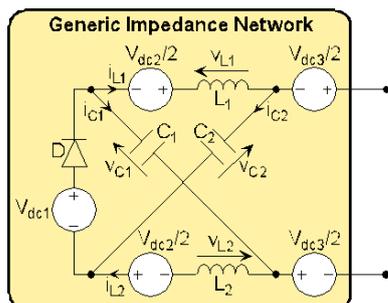


Fig. 4. Generic network entity for implementing hybrid-source inverter.

to be smoothed implicitly without deteriorating the overall inverter voltage gain, even with no external LC filter added [6]. Although not obvious at first sight, a second advantage exhibited by the embedded network is its lower voltage stress experienced by capacitors C_1 and C_2 , as compared with the original network shown in Fig. 5(a). Yet a third advantage to note for the embedded network is its minimal requirement of only a single dc source, even though two sources are explicitly shown in the figure. The only difference likely to be observed when a single source is used is its asymmetrical distribution of electrical quantities within the network, whose overall capacitive voltage stress is still lower than that experienced by the traditional network drawn in Fig. 5(a).

In addition to the earlier two networks, a third dc-link embedded network can be realized by shifting the dc sources to the far-right dc-link where connection to the rear-end inverter bridge is made [6, 7]. The resulting circuit is shown in Fig. 5(c), where an observation noted is that the dc sources are now in series with the inverter bridge, inferring that currents drawn from them are again chopping. This indeed is unfavorable, but when compared with the earlier two networks, it does have an advantage in

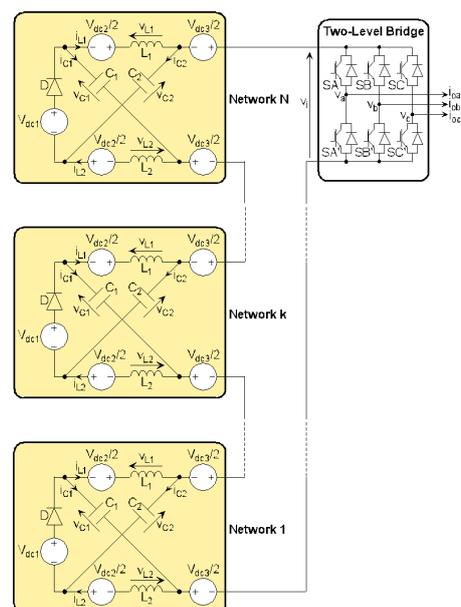


Fig. 3. Two-level hybrid-source inverter formed by direct cascading of impedance networks.

the sense that it experiences the lowest voltage stress across C_1 and C_2 , while producing the same voltage gain. Also, unlike the embedded circuit shown in Fig. 5(b), the dc-link embedded network experiences symmetrical voltage and current distribution, even when only one dc source is used for powering it. This unarguably is a favorable advantage since single point of failure at component experiencing a higher stress is less likely (two sources are mainly added to create a symmetrical network for reducing common and differential mode noises, where appropriate).

Upon summarizing the characteristic features of the three impedance networks, a generic network entity can be deduced, and is drawn in Fig. 4. At present, only the final expressions governing the network capacitive V_C , peak dc-link \hat{v}_i and peak ac output \hat{v}_{ac} voltages are stated in (1) for analysis purposes:

$$\begin{aligned}
 V_C &= \frac{1-T_0/T}{1-2T_0/T} V_{dc1} + \frac{0.5}{1-2T_0/T} V_{dc2} + \frac{T_0/T}{1-2T_0/T} V_{dc3} \\
 \hat{v}_i &= \frac{1}{1-2T_0/T} (V_{dc1} + V_{dc2} + V_{dc3}) \\
 \hat{v}_{ac} &= \frac{M}{1-2T_0/T} (V_{dc1} + V_{dc2} + V_{dc3}) \quad (1)
 \end{aligned}$$

where $M \leq 1.15$ (with triplen offset added), T_0 / T and $B \geq 1$ represent the inverter modulation ratio, normalized shoot-through duration and boost factor respectively. Clearly, (1) conveys that voltage-buck operation can be produced by setting $T_0 / T = 0$ ($\Rightarrow B = 1$), and decreasing M accordingly, while voltage-boost operation can be commanded by setting a finite value for T_0 / T ($\Rightarrow B > 1$) with M decreased according to $M \leq 1.15 \times (1 - T_0 / T)$ [1, 2]. It also shows that the same ac voltage gain can be produced by the traditional, embedded and dc-link embedded Z-source inverters, obtained when (V_{dc2}, V_{dc3}) , (V_{dc1}, V_{dc3}) and (V_{dc1}, V_{dc2}) are set to zero respectively.

III. GENERALIZED CONCEPTS OF CASCADING HYBRID-SOURCE ENTITIES

Two methods of cascading multiple hybrid-source network entities are now discussed with their relevant ac voltage gain expressions derived, and advantages and disadvantages stated.

A. Alternate Cascading

The simplest way of raising the output voltage might appear to be the series connection of impedance networks, as shown in Fig. 3. Although the output voltages of the impedance networks do add up to give an overall higher dc-link voltage, the ac voltage gain expression remains unchanged when compared with that exhibited by a single impedance network. The direct series cascading technique is therefore not a favorably recommended approach, even though it might appear to be the simplest and most promising.

Instead, the conceptually less obvious alternate cascading approach is recommended, whose operating concepts are better understood by first considering networks 1 and 2 ($k = 2$) in Fig. 3. By keeping network 1 unchanged and flipping network 2 horizontally, the upper

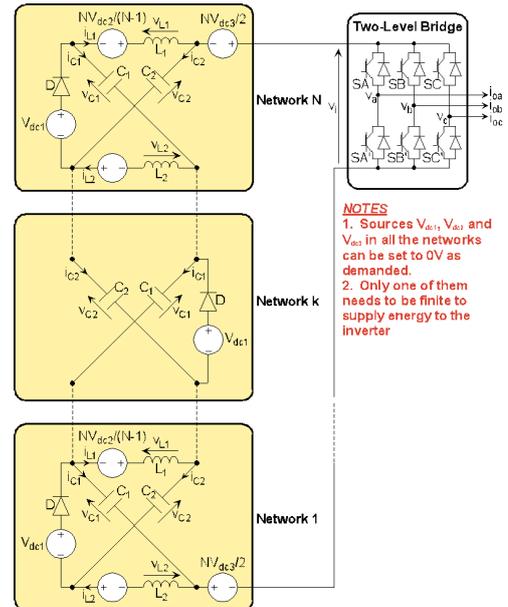


Fig. 5. Two-level hybrid-source inverter formed by alternate cascading of impedance networks.

inductive branch of network 1 and the lower inductive branch of network 2 are observed to have the same voltage and current polarities. They can then be combined as demonstrated in Fig. 7, where the same alternating and inductive combining actions are also performed on the other impedance networks to cascade N of them neatly together using $N - 1$ lesser inductors. Also, as per discussed earlier, any of the sources in the cascaded networks can be set to zero depending on the particular application in consideration, but surely at least one of them must remain to power the overall inverter. The upper and lower dc-link terminals of the cascaded network are then connected to a two-level inverter bridge, whose

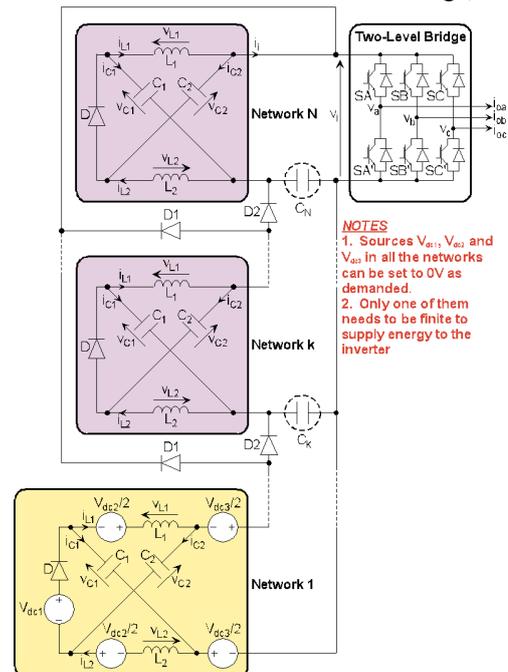


Fig. 6. Two-level hybrid-source inverter formed by capacitive cascading of impedance networks.

NOTES
 1. Sources V_{dc1} , V_{dc2} and V_{dc3} in all the networks can be set to 0V as demanded.
 2. Only one of them needs to be finite to supply energy to the inverter

NOTES
 1. Sources V_{dc1} , V_{dc2} and V_{dc3} in all the networks can be set to 0V as demanded.
 2. Only one of them needs to be finite to supply energy to the inverter

functionality is again to commutate the inverter between shoot-through and non-shoot-through (active or null) states. Analyzing these states eventually leads to the following ac voltage gain expression \hat{v}_{ac} :

$$\hat{v}_{ac} = \frac{M}{1-(N+1)T_0/T} (V_{dc1} + V_{dc2} + V_{dc3}) \quad (2)$$

By comparing the denominators of (2) and (1), an advantage exhibited by the inverter in Fig. 7 is that it reaches its maximum gain limit (theoretically infinite) earlier when T_0 / T increases from 0 to $1 / (N + 1)$, rather than to 0.5 for inverters with only a single impedance network. A smaller T_0 / T would then mean that $M \leq 1.15 \times (1 - T_0 / T)$ can be larger, hence giving rise to both a higher gain and an improved waveform quality (harmonic distortion is known to be lower at high M [2]). This advantage, together with the lesser inductive elements needed, definitely places the alternate cascading method ahead of the direct cascading method in terms of attractiveness.

B. Capacitive Cascading

A second cascading concept is illustrated in Fig. 6, where $N - 1$ additional capacitors and $2(N - 1)$ additional diodes are used for connecting N impedance networks together. Of the N networks considered, only network 1 can assume any of the three possible network types discussed in Section 2. For the remaining $N - 1$ networks, they must strictly be of the dc-link embedded type with V_{dc1} and V_{dc2} set to zero, because of reasons that would become obvious shortly. For V_{dc3} in the $N - 1$ dc-link embedded networks, they are replaced by capacitive elements C_k ($k = 2$ to N), whose voltage values are shown later to depend on the shoot-through duration, and increase as the index of the network increases from 2 to N . These N networks are then cascaded together by the $2(N - 1)$ diodes, which can be divided into two groups, labeled as $D1$ and $D2$ respectively. When the inverter bridge is commanded to enter a shoot-through state, besides diodes D turning OFF naturally, diodes $D2$ also block naturally to isolate the N impedance networks. At the same time, diodes $D1$ conduct to short all the positive terminals of the

N networks to the common negative terminal of the rear-end inverter bridge. This obviously is possible only when the upper $N - 1$ networks are all implemented by the dc-link embedded type, whose characteristic feature is the creation of a common negative inverter dc rail for tying all the negative potentials of the capacitors C_k together. The resulting negative terminal, together with the placement of diodes $D1$, then allows the simultaneous shorting of all networks by simply turning ON at least two switches from the same phase of the inverter bridge.

Upon reverting the inverter bridge back to its non-shoot-through state, diodes $D2$ and D start to conduct, while diodes $D1$ become reverse-biased. But in brief, it resembles the parallel connection of multiple capacitors C_k with one impedance network inserted in series between two adjacent capacitors. Performing state space analysis on the distinct states then gives rise to the following mathematical expressions for the voltage V_{C_k} across C_k and peak ac output voltage \hat{v}_{ac} :

$$V_{C_k} = \frac{1}{(1-2T_0/T)^{k-1}} (V_{dc1} + V_{dc2} + V_{dc3})$$

$$\hat{v}_{ac} = \frac{M}{(1-2T_0/T)^N} (V_{dc1} + V_{dc2} + V_{dc3}) \quad (3)$$

As noted in (3), the denominator of the ac gain expression is raised to the power of N , which will give a much smaller fractional number. Inverting it would then give rise to a much higher gain than that obtained by using only a single impedance network. Another point to note is that unlike the alternate cascading approach whose maximum gain limit is reached when T_0 / T increases to $1 / (N + 1)$, the capacitive cascading method produces its maximum gain when T_0 / T reaches 0.5 ($\Rightarrow M \leq 0.5 \times 1.15$), similar to the case where only one impedance network is used.

IV. EXTENSION TO THREE-LEVEL NEUTRAL-POINT-CLAMPED INVERTERS

As noted from past literature, three-level traditional, embedded and dc-link embedded Z-source inverters with better waveform quality and lower semiconductor stress can be derived [6, 8]. The same three-level extension can indeed be adopted for the two cascading approaches described in Section 3, but it is not as straightforward with a few conceptual issues to note when designing them. As an illustration, Fig. 8 shows a NPC inverter constructed by using the alternate cascading concept to cascade an odd number of impedance networks at its dc front end. Unlike its two-level counterpart, connecting even number of impedance networks is viewed as not possible because of the need to create a neutral dc potential, which together with the positive and negative dc rails, form the three terminals needed for feeding energy to the rear-end NPC bridge. To demonstrate how the neutral potential can be created, network k in Fig. 8 is assumed to be the middle network, whose source voltage V_{dc1} and diode D are

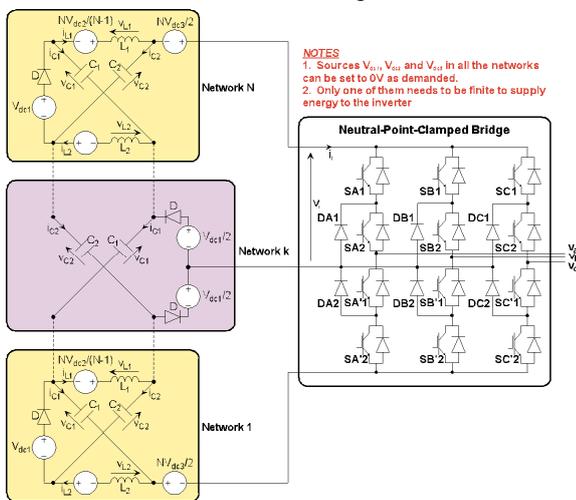


Fig. 8. Three-level hybrid-source inverter formed by alternate cascading of impedance networks.

explicitly split into two. Between the two split sets, a neutral potential can then be drawn out for direct connection to the three-phase clamping diodes of the NPC bridge. Dividing in this way ensures that two symmetrical LC groups are placed above and below the neutral potential to create two approximately balanced supplies, as demanded by the rear-end NPC bridge..

V. OTHER OPERATING ISSUES

As faced by all inverters, practical operating issues, mainly linked to parasitic imperfections found in passive and active components, always cause their performance to degrade by some measureable extent. For the inverters implemented using the presented cascading concepts, parasitic influences are mainly from resistances found in the LC elements, which then need to be analyzed in order to examine how the inverter gain deteriorates as the load power and shoot-through duty ratio increase.

VI. EXPERIMENTAL RESULTS

For the initial testing of the generalized cascading concepts, a hybrid-source two-level inverter was constructed by connecting three impedance networks in series using the alternate cascading technique, as illustrated in Fig. 7. Parametric values chosen for each network ($L = 5$ mH and $C = 2200$ μ F) were currently not optimized, and were mainly obtained from components found in the laboratory. The cascaded impedance network was then powered by a single input dc source set at 100 V and placed at the dc-link of network 1 ($\Rightarrow V_{dc3} = 100$ V) with the rest of the indicated sources set to zero ($\Rightarrow V_{dc2} = V_{dc3} = 0$ V in networks 1 to 3 and $V_{dc1} = 0$ V in networks 2 and 3). Using this circuit configuration, and with the control parameters set to $M = 0.8 \times 1.15$ and $T_0 / T = 0$, Fig. 9 shows the produced experimental waveforms under voltage-buck operation. As seen, the dc-link voltage, reflected by the phase voltage (measured with respect to the negative dc rail) and line voltage pulse heights, is measured at 100 V, which is the same as the input voltage since no voltage boosting is introduced here. The ac current amplitude measured in the figure is about 2 A, which can be boosted by tuning T_0 / T to a finite value. To illustrate that, Fig. 10 shows the recaptured waveforms with the control parameters returned to $M = 0.8 \times 1.15$ and $T_0 / T = 0.2$ to initiate voltage-boost operation. With a boosted dc-link voltage of about 300 V available for powering the rear-end inverter bridge, its ac current amplitude can now be raised to around 5 A, representing an ac gain of around 2.5. This measured gain is however lower than that calculated theoretically because of parasitic imperfections found in the preliminary experimental setup.

With the two-level bridge now replaced by a NPC bridge, and with two 50 V sources placed at V_{dc1} of networks 1 and 3 ($V_{dc2} = V_{dc3} = 0$ V in networks 1 to 3 and $V_{dc1} = 0$ V in network 2), Fig. 11 and Fig. 12 show the

three-level switching waveforms obtained when subject to the same voltage-buck and boost operating conditions, as described earlier for the two-level case. These results clearly spell out the same voltage and current gain information, but of course with better conditioned three-level phase and five-level line voltage waveforms observed, together with a narrower current ripple band. To demonstrate its front-end dc behavior, Fig. 13 shows the voltages measured across one capacitor in each network, and the dc-link voltage under voltage-buck operation. As anticipated, the capacitive voltages in networks 1 and 3 remain the same as their input voltages, while that in network 2 stays at zero since no source is tied to it. The dc-link voltage is noted at 100 V without switching, which again is expected since no shoot-through state is inserted during voltage-buck operating mode. When commanded to enter the voltage-boost mode, Fig. 14 shows the recaptured waveforms at the dc front-end, which again reflects the unequal capacitive voltage distribution among the networks. Also shown in the figure is a chopping dc-link voltage, which in principle is caused by the insertion of shoot-through states to the inverter state sequence.

VII. CONCLUSION

From analyzing the three existing impedance networks, a generic network entity is identified, before multiple of them are configured according to two generalized cascading concepts, to form an alternative family of hybrid-source inverters with a higher ac output gain. Dynamic responses of the cascaded inverters and their extensions to the NPC variants are also discussed. Presented experimental results clearly show that the hybrid-source inverters can indeed produce a higher gain, limited mainly by parasitic components found in the generic network entity.

REFERENCES

- [1] F. Z. Peng, "Z-source inverter", *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504-510, Mar/Apr. 2003.
- [2] P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, L. T. Wong and C. P. Ang, "Z-source current-type inverters: digital modulation and logic implementation", *IEEE Trans. Power Electron.*, vol. 22, pp. 169-177, Jan. 2007.
- [3] Y. H. Kim, H. W. Moon, S. H. Kim, E. J. Cheong and C. Y. Won, "A fuel cell system with Z-source inverters and ultracapacitors", in *Proc. IPEMC'04*, 2004, pp. 1587-1591.
- [4] J. W. Jung and A. Keyhani, "Control of a fuel cell based Z-source converter", *IEEE Trans. Energy Conversion*, vol. 22, pp. 467-476, Jun. 2007.
- [5] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress", *IEEE Trans. Ind. Applicat.*, vol. 42, pp. 770-778, May/June. 2006.
- [6] P. C. Loh, F. Gao and F. Blaabjerg, "Embedded EZ-Source Inverters", in *Proc. IEEE-IAS'08*, 2008, pp. 1-8.
- [7] J. Anderson and F. Z. Peng, "A class of quasi-Z-source inverters", in *Proc. IEEE-IAS'08*, 2008, pp. 1-7.
- [8] P. C. Loh, F. Gao, F. Blaabjerg and S. W. Lim, "Operational analysis and modulation control of three-level Z-source inverters with enhanced output waveform quality", in *Proc. EPE'07*, 2007, pp. 1-10.

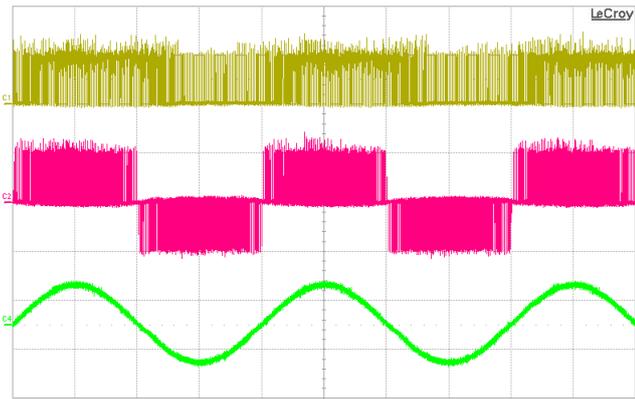


Fig. 9. Experimental phase voltage (100V/div), line voltage (100V/div), and line current (2A/div) of a two-level hybrid-source inverter with three cascaded impedance networks, $M = 0.8 \times 1.15$, $T_0/T = 0$ and a time scale of 5ms/div.

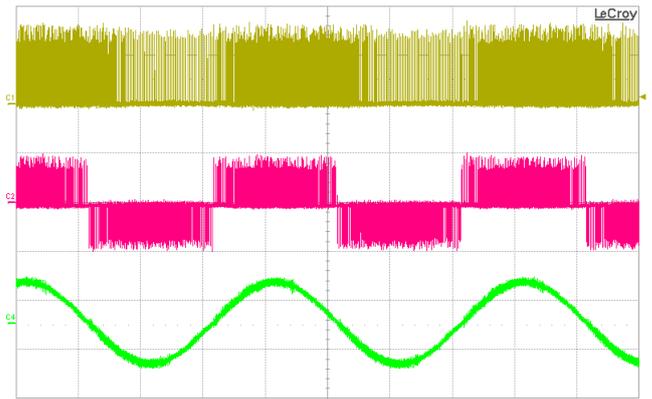


Fig. 10. Experimental phase voltage (200V/div), line voltage (350V/div), and line current (5A/div) of a two-level hybrid-source inverter with three cascaded impedance networks, $M = 0.8 \times 1.15$, $T_0/T = 0.2$ and a time scale of 5ms/div.

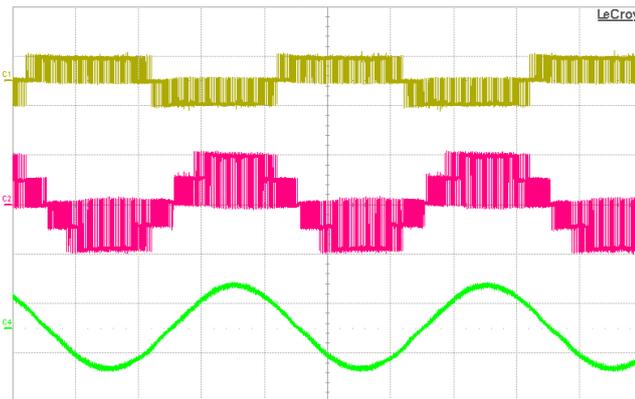


Fig. 11. Experimental phase voltage (100V/div), line voltage (100V/div), and line current (2A/div) of an NPC hybrid-source inverter with three cascaded impedance networks, $M = 0.8 \times 1.15$, $T_0/T = 0$ and a time scale of 5ms/div.

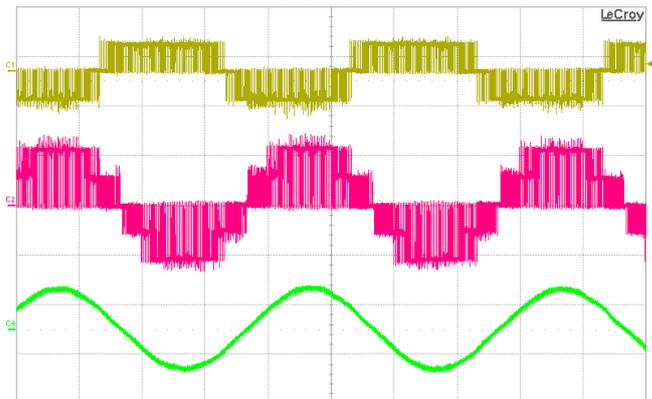


Fig. 12. Experimental phase voltage (200V/div), line voltage (200V/div), and line current (5A/div) of an NPC hybrid-source inverter with three cascaded impedance networks, $M = 0.8 \times 1.15$, $T_0/T = 0.2$ and a time scale of 5ms/div.

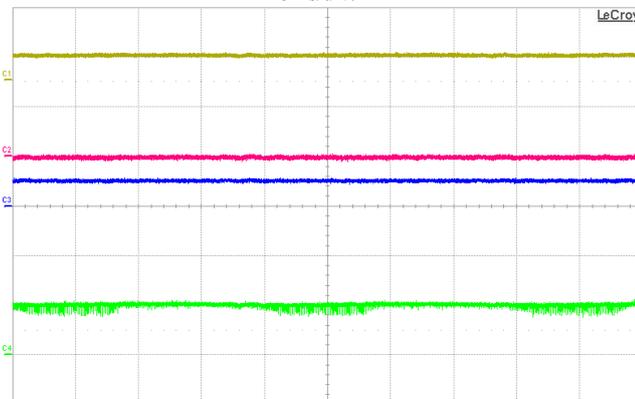


Fig. 13. Experimental capacitor voltages across network 1 (100V/div), network 2 (50V/div), network 3 (100V/div), and dc-link voltage (100V/div) of an NPC Z-source inverter with three cascaded impedance networks, $M = 0.8 \times 1.15$, $T_0/T = 0$ and a time scale of 5ms/div.

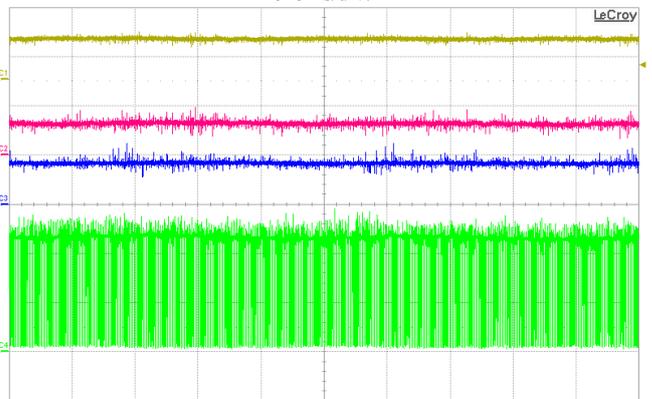


Fig. 14. Experimental capacitor voltages across network 1 (100V/div), network 2 (50V/div), network 3 (100V/div), and dc-link voltage (100V/div) of an NPC Z-source inverter with three cascaded impedance networks, $M = 0.8 \times 1.15$, $T_0/T = 0.2$ and a time scale of 5ms/div.