Design Tools for Submersible Converter

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Introduction

The DeepWind project is a study of a Darreius type VAWT system. The blades cannot be pitch controlled to suit the wind and other operational requirements such as braking. This means that the wind turbine is stall regulated and the generator and its control system together provide the means of controlling the power supplied to the grid. They must also provide the braking force for normal and some of the emergency braking. An additional requirement is that the Darreius Wind Turbine is not self-starting meaning that the converter must be able to start the generator as a motor and drive the Turbine up to normal operating speed, when the function may revert to generating mode.

Deliverable Description from DOW

D3.32) Design tools for submersible converter: Report on a four quadrant, submersible electrical power converter developed and designed for the 5MW and the 20 MW wind turbines. The converter is to provide controllability and facilitate starting the turbine. A submersible power converter is necessary for the 5 MW and 20 MW machines. Electrical power regulation and electrical grid connection will be determined and a control strategy proposed to enable direct wind turbine rotor control. The power controller will be provided with appropriate protection systems, e.g. for overvoltage and overcurrent. The wind energy controller will be provided by the control system work package (WP4). Because of the complex arrangement of proprietary components in a power electronic converter, and the continuing development of these components, necessitating new component models, it is not practical to produce a software design tool. Therefore a report will be provided detailing the design strategy and design rules. [month 43]

Converter functional modes

The converter for the 5 MW and 20 MW DeepWind wind turbines is required to operate in several different modes.

1. Start the wind turbine from standstill and run up to speed. In this mode of operation the converter will take power from the grid and use it to operate the generator as a motor that will drive the wind turbine shaft up to speed as shown in Fig. 2. As the shaft speed approaches normal operating speed, the wind power will take over the shaft drive and the motor load on the generator will be reduced.
2. Operate as a generator. In this mode, power is supplied to the grid at the frequency and voltage of the grid. Power comes from the generator at a frequency and voltage that are determined by the shaft speed. The shaft speed is controlled by the Turbine Controller to give the best power yield corresponding to the actual wind speed. The required torque will vary correspondingly. Fig. 3 show a diagram of the power flow when operating in this mode.

3. Normal Braking Mode. If braking is required, to change speed or to stop the turbine rotor, the generating torque will be increased beyond the torque available from the turbine. This will be possible only if the grid is connected and is able to absorb the power. Energy will continue to be
supplied to the grid, by reducing the kinetic energy of rotation. Fig. 3 shows the power flow in this mode of operation. The power flow is the same as for the normal generating mode.

4. Emergency braking mode #1. If braking is required, and the grid connection has been lost, the generator will continue to generate voltage so long as the generator rotor is rotating. In this case the generator side of the power electronics may be used to divert the output power into a dump resistor in a controlled manner to ensure current and torque limits are not exceeded. Fig. 4 illustrates the power flow diagrammatically.

![Power Flow Diagram](image)

Fig. 4 Diagram of power flow in DeepWind system for emergency braking #1 operation. The generator is acting as a generator. The kinetic energy and converted wind energy is dissipated as heat in a controlled manner, in the dump resistor.

5. Emergency braking mode #2. If braking is required, and the grid connection has been lost, the generator will continue to generate voltage so long as the generator rotor is rotating. If the normal duty power electronics is damaged, an emergency contactor may be provided to divert the output power into a dump resistor in an uncontrolled manner to ensure that the turbine rotor speed is reduced to an acceptable level. As the available control is negligible, this method may be expected to damage essential components, such as the turbine blades, the permanent magnets, or the generator windings. This method is to be used in extreme emergency only. Fig. 5 illustrates the power flow diagrammatically.
Fig. 5 Diagram of power flow in DeepWind system for emergency braking #1 operation. The generator is acting as a generator. The kinetic energy and converted wind energy is dissipated as heat in a controlled manner, in the dump resistor.

6. Standstill mode. From time to time it will be necessary to ensure that the wind turbine rotor is stationary and does not turn. This can be achieved by controlling the generator so that the generator rotor does not rotate relative to the generator stator. Fig. 2 illustrates the power flow in this this mode. The difference here in relation to mode 1 is that the control objective here, is to hold the speed at zero.

7. Compliance with grid connection code. A major requirement is to provide voltage ride-through so that the DeepWind electro-mechanical system will need to use energy stored in the system to provide voltage ride-through power for the specified time. As a permanent magnet generator is employed in DeepWind, the rotation of the turbine will always generate voltage enabling the kinetic energy of rotating to be utilised for this purpose. Any shortfall in energy required for voltage ride-through will have to be compensated by using energy stored in the DC link capacitors. This means that voltage ride-through must be considered as a part of simultaneous engineering of the DeepWind drive chain.

**Four quadrant two level converter for the DeepWind demonstrator**

For the demonstrator, a commercial pulse width modulated two level converter was selected as a solution that fulfilled most of the modes of operation cheaply and quickly. Modes 4 and 5 for emergency braking were not fulfilled, but this was compensated by the fitting of a fail-safe brake on the generator shaft. Fig. 6 shows a diagram illustrating the 4 quadrant, 2 level converter applied here.
Fig. 6 Diagram showing 2 level, 4 quadrant converter for 1 kW VAWT DeepWind demonstrator generator system. The converter was bench tested with the induction generator and found to exhibit suitable performance for the DeepWind VAWT demonstrator system. Designs and results are reported in detail in Appendix 1

**Design proposal: Multi level four quadrant converter for the 5MW and 20MW versions**

For the 5 MW and 20MW a multi-level, four quadrant converter was proposed. The selection process and design criteria are described in Appendix 2. The four quadrant converter comprises two multi-level inverters arranged back to back with a DC link. Inverter number 1, described in Appendix 3 converts the DC to grid frequency and voltage and controls the power flow in all situations. Inverter number 2 converts the frequency and voltage of the generator to DC. For both inverters, the power flow may be in either direction, so that the generator can operate either as a generator or as a motor. This operation and the change-over from one to the other are described in Appendix 4. In both inverters, as the DC link circuit is common to them, the neutral point is clamped (NPC). This ensures an even voltage stress distribution throughout. For design consideration, it was assumed that the grid voltage and frequency at the point of connection was 13.5 kV and 50 Hz.

The selection of semiconductor ratings for the output devices will depend on the voltage and current required and the cooling arrangement selected. As Power semiconductors are currently in a rapid state of development, it is not possible to make an actual choice at this time, but silicon carbide field effect transistors are a strong candidate (SiC).

It is unlikely that the energy storage capacitors of the DC link circuit will be dimensioned according to the normal operational needs of DeepWind. It is more likely that the dimension of these will be decided by the needs of the grid code for connection, and the kinetic energy in the DeepWind system available to satisfy these needs.

**Subsea requirements for the converter**

In the subsea environment, the housing of the converter is the deciding factor that drives the chosen basic components and materials. This can be classified in two categories: housing with pressure compensation, or housing without pressure compensation. Due to the given timeline, the first solution is considered where the housing will ensure the pressure compensation in order to be able to make use of standard components.

Considering the installation of the power converter subsea, the following requirements must be met:

- Ensure housing to handle the pressure under the seawater at the site
- Ensure proper air conditioning in the converter location
- Reduced humidity in the ambient air to avoid condensation
- Cooling system with liquid preheating - to avoid condensation
- Protect against corrosion - suitable surface treatment, cathodic protection
- Ensure proper cooling - water to water heat exchangers with pressure compensators
- Reinforced insulation

**Prototype small scale three level four quadrant converter**

To validate the proposal that a three level four quadrant converter is suitable for the DeepWind system, two small scale inverters were designed, built and tested. One was to test the operation of the grid side inverter, and the other was to test the operation of the generator side converter, given the DC link voltage. These are described in detail in Appendix 3 and Appendix 4 respectively. The generator side converter was tested in conjunction with the prototype small scale permanent magnet generator designed and built in the DeepWind project.

![Photo of one of the small scale laboratory model inverters made for the DeepWind project tests ( Appendix 3)](image)

The three level inverters also clamp the neutral point voltage to ensure balance of the voltage stress on the high power components.

For the grid side inverter of Appendix 3 an important feature is the control of common mode voltage and total harmonic distortion. To this end a study of the effects of the different possible modulation strategies was carried out. The results were published in [1], and Fig. 8 shows a table summarising the results. The best all-round strategy tested was the Zero Small Medium Large vector (ZSML) strategy. The grid side inverter was successfully tested thermally to 6 [kW] load.

For the machine side inverter of Appendix 4, it was considered important to obtain the highest possible efficiency of energy conversion. This was obtained experimentally using a vector control strategy with an added maximum torque per ampere (MTPA) strategy. The inverter was able to start the permanent magnet generator reliably and the control was able to hold the speed steady within about 1.3% despite changes in shaft torque in the ratio 20:1. The control is able to regulate the speed during a transition of load torque.
from motoring to generating. Tests were also carried out to check that emergency braking was possible using the methods proposed. A dedicated position estimator was required to enable holding the shaft at zero speed.

Conclusion

A standard two level four quadrant converter was used for the 1 kW DeepWind demonstrator system. This worked very well. For the 5 MW and 20 MW versions a three level, NPC four quadrant converter was proposed, comprising two back to back inverters. This was partly because of the medium voltage of the grid, higher than the industrial voltage usually encountered on smaller wind energy generators.

Two identical demonstrator inverters were made and tested. Detailed design calculations were performed prior to fabricating the inverters. One was tested as the grid side inverter and the other was tested as the generator side inverter, using the DeepWind prototype generator as generator. Simulations of the inverter performance in steady state and dynamic events were performed and the results were compared favourably with the test results. In this way the design process has been mapped out. In case 5 MW and 20 MW versions are required to be made, the design process is unchanged, however, the characteristics of the devices used and the mounting and cooling techniques used will be suited to the rating of the inverter to be designed. The terms of the description of the deliverable are satisfied.

Further Work

A number of facilities remain to be tested.
- Test the two inverters back to back.
- Add a dump resistor to the DC link, with activation circuit.
- Add dump resistors to the generator terminals with an activation circuit.
- Investigate encapsulation of the power electronics. Will it make the circuits withstand condensation? Will it make the circuits withstand immersion?
- Test encapsulated inverters in a suitable ambient.

References

Appendix 1 Report – Power Electronics for WP3 DeepWind Project – September 2012

This report addresses work on the four quadrant converter supplied for the DeepWind 1 kW demonstrator and tests with the corresponding generator. Supplementary work reported covers the initial consideration of the converter required for the 5 MW and 20 MW versions.

Author: Ionut Trintis
Synopsis
This report addresses work on the four quadrant converter supplied for the DeepWind 1 kW demonstrator and tests with the corresponding generator. Supplementary work reported covers the initial consideration of the converter required for the 5 MW and 20 MW versions.
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1. Introduction
This progress report presents a brief status and summary on the work related to the power electronic converters used in the DeepWind project. The report is divided in two parts. The first part is related to the test bench used for the small scale project demonstrator, where a wind power converter system was realized to drive the generator. The second part presents the design of the wind power converter system, to be used in the full scale offshore floating vertical axes wind turbine (VAWT).

2. Test Bench Converter for the 1 kW Floating VAWT Demonstrator
The wind power converter system used in the test bench is shown in Figure 2.1. It is based on the full scale conversion, meaning that the whole electrical power generated by the squirrel-cage induction generator (SCIG) is converted to be delivered to the power grid. The electrical generator speed is controlled by the AC-DC generator converter and the resulting electrical energy is rectified to a common DC level with the DC-AC grid converter. The DC-AC grid converter is synchronized with the power grid, and delivers the generated power at unity power factor.

![Figure 2.1. Wind turbine system with full scale power converter](image1)

Figure 2.1. Wind turbine system with full scale power converter
The detailed schematic of the wind power conversion system is shown in Figure 2.2. The wind turbine is located offshore and floating, and the SCIG is installed subsea at the bottom of the wind turbine in a sealed case. The power converter is located onshore, and therefore there will be a long cable between the generator and converter. For this reason, a generator filter (du/dt filter) is required to reduce the overvoltage on the generator windings created by the long cable.

![Figure 2.2. Two-level back-to-back full scale voltage source converter system](image2)

Figure 2.2. Two-level back-to-back full scale voltage source converter system
The power converter consists of two back-to-back two-level DC-AC converters with a common DC-bus. The AC voltage levels for both converters is 400V line-to-line RMS, and therefore the transistors used are 1200V insulated gate bipolar transistors (IGBTs) and 1200V diodes. The grid converter controls the grid current in phase with the grid voltage and the common DC-bus voltage level. A grid filter is installed on the grid side to reduce the harmonics of the current injected into the grid.
2.1. **Test on Electrical Generator**

Tests on the SCIG have been done to verify the functionality and to determine the electrical parameters. A test setup was realized with the generator coupled mechanically with a DC motor, see Figure 2.3. A torque transducer was installed in the mechanical assembly to measure the mechanical torque, speed and power.

![Image of electrical generator test setup](image)

To determine the electrical parameters, the no-load and blocked rotor tests have been done. The machine parameters are given in Table 2.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Number of phases</td>
<td>3</td>
</tr>
<tr>
<td>HS rated power (kW)</td>
<td>1.100</td>
</tr>
<tr>
<td>Rated current (A)</td>
<td>2.5</td>
</tr>
<tr>
<td>No-load current (A)</td>
<td>1.4</td>
</tr>
<tr>
<td>Rated torque (N.m)</td>
<td>7.35</td>
</tr>
<tr>
<td>Starting torque (N.m)</td>
<td>12.00</td>
</tr>
<tr>
<td>Maximum torque (N.m)</td>
<td>15.00</td>
</tr>
<tr>
<td>Rated speed (min-1)</td>
<td>1429</td>
</tr>
<tr>
<td>FCR J02 Brake torque (N.m)</td>
<td>20.00</td>
</tr>
<tr>
<td>Main voltage (V)</td>
<td>400</td>
</tr>
<tr>
<td>Connection</td>
<td>DY</td>
</tr>
<tr>
<td>Starting type</td>
<td>DOL</td>
</tr>
<tr>
<td>Motor winding (V)</td>
<td>230VD/400VY</td>
</tr>
<tr>
<td>Rated Frequency (Hz)</td>
<td>50</td>
</tr>
<tr>
<td>Operation position</td>
<td>IM3601(IMB14)</td>
</tr>
<tr>
<td>Index of protection</td>
<td>IP55</td>
</tr>
<tr>
<td>Index of cooling</td>
<td>IC411</td>
</tr>
<tr>
<td>Insulation class</td>
<td>F</td>
</tr>
</tbody>
</table>

**Table 2.1. SCIG parameters (integrated mechanical brake)**

2.1.1. **No-Load Test**

Balanced voltages at the rated frequency (50Hz) are applied to the machine stator varying the line-to-line voltage from 0 to 400V. The characteristics of current and power as a function of the applied voltage are shown in Figure 2.4.
2.1.2. Blocked Rotor Test
Balanced voltages are applied to the machine stator, while the rotor is mechanically blocked to prevent rotation. The current and power characteristics as a function of the applied voltage are shown in Figure 2.5.

2.1.3. Calculated Machine Parameters
Based on the above test results, the machine equivalent circuit parameters can be calculated. In Figure 2.6, and equivalent circuit with the calculated values is shown. The parameters are calculated in Ohms at the rated frequency (50 Hz).

\[
\begin{align*}
R_s &= 12.8 \, \Omega \\
X_s &= 7.5 \, \Omega \\
l &= j\omega \phi_t \\
j(\omega - \omega_r)\phi_r &= X_s = 7.5 \, \Omega \\
R_r &= 2.7 \, \Omega \\
X_m &= 148.9 \, \Omega 
\end{align*}
\]

2.1.4. Mechanical Brake Test
In order to break the generator and therefore the wind turbine in case of too high wind speed, or in case of loss of the power supply, a mechanical brake is installed at the generator axe. The mechanical brake it is normally coupled if the built-in DC coil is not supplied. Having the generator brake supplied from the same electrical grid, in Figure 2.7 the mechanical torque given by the brake in case of the power supply for the DC coil, while the machine operates at nominal speed with no load.
2.2. Test of the Power Converter with the SCIG

The back-to-back power converter test setup is shown in Figure 2.8. The grid converter is controlling the grid current at unity power factor, and maintains the total harmonic distortion below 5% as imposed by the standards and controls the DC-link voltage level to around 570 V (with 2% more than the peak line-to-line voltage).

The measured grid voltage and grid current during the operation of the electrical generator is shown in Figure 2.9. It can be noticed the unity power factor operation, and low distortion level.
3. Design of the Full Scale Wind Turbine Converter

A design of 5 MW wind power converter will be considered for the full scale turbine. Considering the choices on the generator side, such as squirrel-cage induction generator or permanent magnet synchronous generator the full scale power converter will be considered (total electrical power is processed). During the design process, the possibility to upscale in power up to 20 MW is taken as a background requirement.

The considered general structure of the wind turbine with full scale converter is shown in Figure 3.1. As main components, the followings can be enumerated: rotor, optional gear-box depending on the generator design, electrical generator, AC-DC generator converter, DC-AC grid converter, common DC-bus, and boost transformer.
3.1. **Design Requirements**

The requirements of the converter design are directly linked to the desired location of the installation, and the configuration. It is clear that the converter must be designed for the offshore application, the same as for the generator. The electrical generator must be located subsea, considering the floating structure of the VAWT. However, regarding the electrical configuration, the following aspects can be distinguished with regard to the power converters location in the wind turbine:

1. **Converter located above sea level**: Generator connected with long cables to the AC-DC generator converter. This case will require a dV/dt filter between the generator and the generator converter to reduce the overvoltage on the generator’s windings.
2. **Generator converter located close to the generator, subsea, and grid converter located above sea level** having the DC-links of the two converters connected with a DC cable
3. **Converter located subsea with boost transformer located above sea level**
4. **Converter located subsea with boost transformer located subsea**

3.1.1. **General Requirements**

As a state of the art wind turbine converter, the following requirements have to be met:

- Operation with wind speeds on a broad range
- Ability to operate under weak grid conditions
- Ensure low harmonic content on the generator and grid
- Grid compatibility → Comply with the grid codes at the turbine/farm point of common coupling
- Low voltage ride through capability
- Grid support with reactive power on demand

3.1.2. **Offshore Requirements**

Considering the location of the wind turbine in the harsh conditions created by the sea, the following requirements have to be met:

- High reliability → Maintenance and Service are difficult and costly → must be reduced
  - Remote Operated Vehicles or Robots for maintenance and monitoring?
- High availability → Low downtime → increase energy production
  - Redundancy of some components is justified
- Safety → Overspeed, overvoltage and overcurrent protections
- Remote monitoring and sensing

3.1.3. **Subsea Requirements**

In the subsea environment, the housing of the converter is the deciding factor that drives the chosen basic components and materials. This can be classified in two categories: housing with pressure compensation, or housing without pressure compensation. Due to the given timeline, the first solution is considered where the housing will ensure the pressure compensation in order to be able to make use of standard components.

Considering the installation of the power converter subsea, the following requirements must be met:

- Ensure housing to handle the pressure under the seawater at the site
- Ensure proper air conditioning in the converter location
  - Reduced humidity in the ambient to avoid condensation
- Cooling system with liquid preheating → to avoid condensation
- Protect against corrosion → proper paint, cathodic protection
• Ensure proper cooling → water to water heat exchangers with pressure compensators
• Reinforced insulation

3.1.4. Special Requirements
In the new turbine concept based on Darrieus VAWT, due to the mechanical construction and functionality, the following aspects need to be considered:
• Suitable for the required wind turbine speed control to increase the harvesting energy
• Braking using the electrical generator capabilities → Reduce the braking torque on the additional installed mechanical brake
• Overspeed protection and handling
• Handling of fault situations
  o Grid loss → auxiliary power supply with enough installed power and energy capacity
  o Safe/Soft Shutdown Sequence

3.2. Converter Topologies
Considering the defined design requirements, a survey on the suitable converter topologies is in progress. The topology must allow a reliable construction of the 5 MW converter system and scalability up to 20 MW. The state of the art power converters for wind turbines up to 5 MW make use of the low voltage technologies. However, the 5MW power range is the border between low voltage and medium voltage power electronics.
The shift to medium voltage technologies becomes relevant in order to reduce the current levels and therefore reduce the amount of copper and copper losses in the connections. Moreover, having the perspective of the 20 MW power range the medium voltage becomes very relevant. However, the reliability and availability of such a converter must be very high and this is a well-known design challenge.

3.3. Internal and External Grid Connections of the Wind Farm
In the design of the full scale wind turbine, the connections in a future wind farm and the wind farm connection to the shore must be considered. When considering the internal connections in the farm, the state of the art is the medium voltage AC bus. Proposals to replace the AC with DC distribution inside the wind farm have been done. However, a DC-DC converter to convert the power bidirectional from HVDC to MVDC with high power and high reliability does not exist yet in industry. Therefore, the most easy and industry available solution to boost the voltage up to the highest levels is done in AC. The typical configurations for the offshore wind farms depending on the distance to shore are shown in Figure 3.2. For short distances to shore, the investment and the conversion to HVDC is not justified and therefore the HVAC connection like in Figure 3.2.(a) is chosen. For long distances to shore, the investment in a HVDC transmission line starts to be justified. The typical wind farm connection via HVDC can be seen in Figure 3.2.(b).
Conclusions and Future work
The power converter and generator systems, for the 1 kW demonstrator, were tested at Aalborg University, Department of Energy Technology. The operation is according to expectations, and expected to be similar on the field test with the wind turbine system. The generator system was delivered in July to our project partners in Risø, and the expected commissioning is scheduled to be in October 2012.
The design of the full scale wind turbine converter was started by setting up the requirements for the present application. The reliability and availability of the system are key points for the converter system in the offshore application. Therefore, the next step is to identify the suitable converter topologies that comply with the given requirements. The converter system design will take into account also the grid connection inside the future wind farms, and the external connection to shore.
Appendix 2 Report - Control of a 5MW multilevel converter for direct drive wind turbine application

This report proposes a multi-level, four quadrant converter as a possible solution for the control of a 5 MW wind turbine generator. A method to design multilevel neutral point clamped (NPC) converters according to different power ratings is also proposed.

The system comprises a wind turbine, a permanent magnet synchronous generator, a back to back three level NPC converter and the grid. A mathematical model of each element of the system was built and control strategies were implemented.

The generator side converter is controlled in such a way that a field oriented control (FOC) technique is applied to the generator. A current control is applied to the grid side converter and a PLL control technique is used for grid synchronization and active and reactive power control.

The different simulations and results presented in the project were carried out considering different wind speeds. Results are presented under different working conditions, such as normal working conditions and grid fault working conditions.

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Control of a 5MW multilevel converter for direct drive wind turbine application

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Control of 5MW multilevel converter for direct drive wind turbine application

Project period:
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Synopsis
A possible solution for the control of a 5 MW wind turbine generator system is studied in this report. A method about how to design multilevel neutral point clamped (NPC) converters according to different power ratings is also proposed. The system is composed of a wind turbine, a permanent magnet synchronous generator, a back to back three level NPC converter and the grid. A mathematical model of each element of the system was built and control strategies were implemented. The generator side converter is controlled in such a way that a field oriented control (FOC) technique is applied to the generator. A current control is applied to the grid side converter and a PLL control technique is used for grid synchronization and active and reactive power control. The different simulations and results presented in the project were carried out considering different wind speeds. Results are presented under different working conditions, such as normal working conditions and grid fault working conditions.
Preface

This 8th semester report was conducted by power electronics and drives and wind power systems students at the Department of Energy Technology, Aalborg University. The project started on 1st of February and finished on 30th May 2012. The project theme is “Control of Converter-fed AC Drives”.

The project, named “Control of a 5MW multilevel converter for direct drive wind turbine application”, was chosen from the different project proposal presented at the beginning of the semesters. It has as a main purpose to enhance the student’s knowledge in designing, modelling, analysis and simulation of the power electronics control systems.

The authors have different cultural backgrounds, each of them coming from different countries.

The text is divided into seven chapters plus 2 appendixes.

We will like to show our gratitude to our supervisors for their support during the entire project work.

We will like also to thank the Aalborg Department of Energy Engineering for the possibility that they offered us to develop in the field that we have chosen.

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Chapter 1

Introduction

In the present chapter introductory concepts and background of wind energy are presented. This sets the scenario where the DeepWind project is born. Project formulations, project limitations and project objectives are presented at the end.

1.1 Background and evolution of wind power systems.

The conventional energy sources as coal, oil or natural gases are finite and generate a high amount of pollution. Because of these reasons research in alternative energy sources has been rapidly increasing in the last few years. Alternative renewable energy sources like wind, solar, biomass or geothermal are clean and widely available in the nature [1], [2].

Wind energy is one of the major sources of renewable energy in the world. The energy obtained from the wind is clean and emission free. It has none of the polluting effects associated with the conventional energy sources. The energy of the wind is converted into electrical energy by the wind turbines, which cause virtually no emissions during their operation and a small amount during their manufacturing, installation, maintenance and removal [1], [2].

For the last 10 years wind energy has been one of the fastest growing energy technologies worldwide [1], [2]. Some of the factors that contributed to this rapid growth include falling cost of wind energy, state legislative requirements for greater use of renewable energy and the benefits of the wind energy in competitive renewable energy markets [1], [2].

From Figure 1 and Figure 2 it can be seen how wind power installed worldwide has been steadily increasing over the last years. Nowadays there are over 300.000 MW of wind power energy installed over the world and the trend is to keep increasing the amount of wind farms and the electrical power generated form wind energy even more [1].

As a consequence of this general growth in the wind power market new ideas in the field are studied and subjected to research. The DeepWind project is one of these ideas and it studies a new concept of off-shore large power wind turbines.
Figure 1. Global annual installed wind capacity 1996-2012 [3].

Figure 2. Global cumulative installed wind capacity 1996-2012 [3].
1.2. DeepWind project.

The DeepWind project consists of designing an offshore wind turbine with a power ranging from 5 to 20 MW which can operate in water depths of more than 150 meters.

The type of wind turbine selected to be used in this project is a floating vertical axis wind turbine, also known as Darrieus wind turbine. The wind turbine will be anchored to the bottom of the sea while the entire structure will be floating like a buoy. The concept can be seen in Figure 3. The generator will be directly connected to the axis of the turbine. Because of this topology, the generator will have to be placed under the water, at the bottom of the structure.

The placement of the wind turbine in the water raises a number of problems for the generator, which have to be taken into account in the design process. Some of the problems encountered are:

- the enclosure of the generator (totally enclosed and tight or totally open and filled with sea water);
- the maintenance, because of the depth at which the generator is operating any maintenance operation will demand a large economical and technical effort;
- the control, no pitch control can be applied for this type of turbine because of its geometry and also different problems with the mechanical brake appear because the structure is placed under the water, etc;

In order to capture sufficient amount of wind to produce the electrical power requested by the project, the scale of the entire wind turbine has to be very large. To get a sense of the entire size a schematic with the dimensions of the wind turbine is presented in Figure 4. The dimensions according to the drawing are placed in Table 1.

It should be noted that this is only an initial design of the wind turbine and the dimensions could differ for the final design. As it can be seen the total length of the wind turbine is 253 meters. Constructing and putting together the entire structure will represent a magnificent task.
This topology of the wind turbine carries the following technical problems which need to be solved by controlling the generator:

- the Darrieus turbine type is not self-starting, even when the wind is powerful enough to maintain the rotational speed. The generator has to accelerate the turbine until certain speed is reached. During the starting procedure, the machine will be working as a motor and power will be consumed from the grid [4];
- after the proper rotating speed is reached, which depends on the wind speed, the turbine will produce a torque in opposite direction and the machine will act as a generator;
- pitch control cannot be applied for this geometry, the entire structure will have to be controlled using the generator;
- the size and weight of the entire structure creates a very large moment of inertia which will affect the way the generator has to be controlled;
- the stopping of the turbine cannot be made using traditional mechanical brakes, the generator has to be able to stop the entire structure from rotating;

![Figure 4. Darrieus wind turbine (placement in the water and dimensions).](image)

<table>
<thead>
<tr>
<th>Geometry of the tower above sea level [m]</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Total length above sea level ( (H_0 + H_R) )</td>
<td>145</td>
</tr>
<tr>
<td>Clearance from mean water level ( H_0 )</td>
<td>15</td>
</tr>
<tr>
<td>Diameter of the tower ( D_1 )</td>
<td>3.15</td>
</tr>
<tr>
<td>Thickness of the tower</td>
<td>0.02</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Geometry of the tower below sea level [m]</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Total length below sea level</td>
<td>108</td>
</tr>
<tr>
<td>Length of the slender part ( H_1 )</td>
<td>5</td>
</tr>
<tr>
<td>Thickness of the slender part</td>
<td>0.02</td>
</tr>
<tr>
<td>Length of the tapered part ( H_2 )</td>
<td>10</td>
</tr>
<tr>
<td>Length of the bottom part ( H_3 )</td>
<td>93</td>
</tr>
<tr>
<td>Diameter of the bottom part ( D_2 )</td>
<td>4.15</td>
</tr>
<tr>
<td>Thickness of the bottom part</td>
<td>0.05</td>
</tr>
</tbody>
</table>

Table 1. Dimensions of Darrieus Wind Turbine
1.1. Project statement and objectives.

This master project is developed based on the DeepWind Project. The study of a design method of a back to back power electronic converter needs to be carried out and the control strategies for it implemented. One side of the converter will be connected to a synchronous permanent magnet generator and the other side will be connected to the grid.

The main objectives for this project are:

- **propose a power converter topology** capable to ensure a full four quadrant control of the generator;

- **for the selected topology a design process** has to be created (general recipe) which can be used to build the converter for different power levels and will enables the user to get a feeling about how to approach a converter design;

- **propose control strategies** in order to operate the converter in normal and abnormal working conditions for the wind turbine;

- The **control strategies will be implemented for only four situations**:
  
  - Normal conditions (the turbine works in nominal condition and it is connected to the grid);
  
  - Abnormal conditions:
    
    - starting the turbine;
    
    - stopping the turbine while a connection to the grid exists;
    
    - fault in grid voltage (voltage dip);

- **build the models of the different elements of the system** in MATLAB Simulink and implement the control strategies for them;
1.1. Project limitations.

- This project will focus only on the theoretical converter design and the control applied for the converter;
- Only one converter topology will be discussed and analysed for different power levels;
- No MPPT strategy will be implemented in the control;
- The input and output filters of the converter will not represent a part of this project;
- This project is focused on the mathematical modelling of the control system, hence, switching strategy and switching frequency selection have not been taken into account.
- The thermal study of the converter will not be covered by this project;
The two main parts of the system are the power electronic converter and the electrical machine. The first step carried out in the project was to study the different topologies of the multilevel converters and select the most suitable one for our purpose. In order to gain a deep understanding of them research and study of the fundamental working principles have been carried out.


To achieve the objectives of this project a converter topology has to be selected in order to enable the application of different control strategies for the generator.

Because the purpose of this project is not focused on presenting converter topologies, only a very brief presentation of the main topologies will be made along with their advantages and disadvantages.

After a thorough research on the literature the direction for the high power converters implemented in wind applications seems to be very clear towards the multilevel converters[5]-[8].

From the different multilevel converters presented in the literature mainly three topologies have managed to impose themselves as a viable solution to be implemented in the industry. The three topologies are the neutral point clamped (NPC), flying capacitor and cascaded H bridge which are presented below. The main advantages and disadvantages for each topology will be presented in order to decide on the most attractive option for this project.
Neutral Point Clamped (NPC)

![Neutral Point Clamped (NPC) Circuit Diagram]

Figure 5. Neutral Point Clamped (NPC).

The layout of this topology is shown in Figure 5. The advantages that make this topology appropriate are [5], [6], [8]-[20]:

- The harmonic content is reduced because the topology adds the zero level to the output of the voltage [9];
- This topology can be extended to any number of levels by inserting additional capacitors and diodes;
- Relatively small DC link capacitor;
- Simple power circuit topology;
- Low number of components compare to the other two;
- Easy to implement protection and modulation schemes leading to a smaller footprint [10];
- Highest convertor efficiency among the available solutions implemented in the industry [15];
- The back-to-back topology for regenerative applications can be implemented because all the phases share a common DC bus;
- This topology is one of the most widely used in MV applications where it has shown its capabilities [12], [14], [15], [20], [21].

The disadvantages are:

- A problem appears in balancing the capacitor voltage for high levels, which made the implementation of the converter to be mostly used for three levels [9].
- This topology features medium/high voltage devices [integrated gate-commutated thyristor (IGCT) and medium/high voltage insulated gate bipolar transistors (IGBTs)].
• Flying Capacitor (FLC)

![FLC Diagram]

Figure 6. Flying Capacitor (FLC)

The advantages that make this topology appropriate for this project are:

- Symmetric switching loss distribution;
- Reduced cost of flying capacitors.

The disadvantages are:

- The capacitors must be pre-charge at the start time and the capacitors voltage must be balanced.
- This topology is impractical at very low switching frequencies because the required capacitance increases with inverse proportion to the switching frequency [22].

• Cascaded H Bridge (CHB)

![CHB Diagram]

Figure 7. Cascaded H-Bridge (CHB)

The advantages that make this topology appropriate for this project are:

- The output voltage $v_{an}$ has three states: $-V_d$, 0 and $V_d$. Compared to the other two it can deliver at the output the entire input voltage;
- It uses exclusively low voltage IGBTs;
- It reaches higher voltage and higher power levels;
- The switch power rating and the stored energy in the LC filter are reduced compared to the other typologies [15];
- Due to its modular construction it can be used in high-power and high-quality applications.

The disadvantages are:

- In order to achieve a regenerative option it needs a higher number of devices [14].
- It requires a large number of isolated power supplies, the only alternative being a phase shifting transformer, which increases significantly the price of the entire structure [9], [14].
- For the grid part a complicated grid transformer is needed, which increases the DC-link capacitance [9];
- Complex control strategies.

Based on the analysis made for every topology the conclusion was to use the neutral point clamped converter. After deciding on this matter the entire structure of the converter is displayed in Figure 8 for a better understanding of the system.

![Multilevel back-to-back converter](image)

**Figure 8.** Multilevel back-to-back converter for a direct connection of a wind turbine to the utility grid.
2.2 Multilevel NPC converters.

Multilevel converters are finding increased usage in the industry as one of the preferred choices of power electronic conversion for high power applications. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage systems. The basic concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to obtain the required power conversion by combining a staircase voltage waveform. The commutation of the switching devices combine the output of this multiple DC sources in order to achieve higher voltage levels at the output terminal, however the rated voltage of the power semiconductors that they should be able to withstand depends only on the rating of the DC voltage source which they are connected to and not the output voltage level of the converter [23]-[25].

2.2.1 Three level neutral point clamped converter.

![Three-Level Neutral Point Clamped Converter Diagram](image-url)

Figure 9. Three-Phase Three-Level Neutral Point Clamped Converter.
A three level NPC converter consists of 2 capacitors on the DC bus, 12 unidirectional active switches each with its own free-wheeling diode and 6 neutral point clamped diodes [26].

The main benefit of this configuration is that while there are twice as many switching devices as in the two level converter topology each of the switches must block only half of the DC link voltage $U_{dc}$ [26].

In the NPC converter in order to produce three voltage levels, the switching devices are controlled in such a way that only 2 of the 4 switches in each phase leg are conducting at any given time. Basically each of the phase nodes a, b and c can be connected to any node in the capacitor bank M0, M1 and M2 thus the number of the different switching states is:

$$n_{sw} = N^{p_h} = 3^3 = 27$$

Eq. 1

where “N” is the number of voltage levels in the DC link and “p_h” the number of phases.

Connection of phase “a” to point M0 and M2 can be accomplished by switching both switches $T_{1a}$ and $T_{2a}$ on or off. This will yield a phase voltage of $U_a = \frac{U_{dc}}{2}$ or $U_a = -\frac{U_{dc}}{2}$ considering $U_{c1}=U_{c2} = \frac{U_{dc}}{2}$. The connection to the junction point M1 is done by switching on $T_{1a}$ and switching off $T_{2a}$. Since the switching devices are always turned in pairs the complement switches are named accordingly $T'_{1a}$ and $T'_{2a}$ [26].

From Figure 9 it can be seen that with this particular switching in the circuit the phase a current $i_{pha}$ will flow into the junction point through the diode $D_{1a}$ if it is negative and out of it through $D_{2a}$ if it is positive. The switching positions for the three possible voltages are given in Table 2.

<table>
<thead>
<tr>
<th>state</th>
<th>$T_{1x}$</th>
<th>$T_{2x}$</th>
<th>$T'_{1x}$</th>
<th>$T'_{2x}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>+</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>0</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>-</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
</tr>
</tbody>
</table>

Table 2. Switching positions for one phase of the three level NPC.

The current paths for the positive, negative and zero states are shown in Figure 10. In zero state the direction of the phase current dictates whether the upper or lower path of the neutral tap is utilized. Thus both switches $T_{1x}$ and $T'_{2x}$ have to be turned on in zero state “0” to provide an open path in case the phase current reverses. In any state 2 active switches or 2 diodes lie in series within the current path depending if it is a positive “+” or negative “-” state [26].

Figure 10. Different conduction paths of the Three level NPC.

It should be considered that each of the switching devices must block only one-half of the DC link voltage assuming sinusoidal currents. The maximum semiconductor current is the maximum phase current. These parameters ratings are considered when choosing the components for the converter [26].

<table>
<thead>
<tr>
<th>state</th>
<th>T1x</th>
<th>D1x</th>
<th>T2x</th>
<th>D2x</th>
<th>T'1x</th>
<th>D'1x</th>
<th>T'2x</th>
<th>D'2x</th>
<th>D1x</th>
<th>D2x</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;+&quot;</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;0&quot;</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;-&quot;</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Positive phase current

<table>
<thead>
<tr>
<th>state</th>
<th>T1x</th>
<th>D1x</th>
<th>T2x</th>
<th>D2x</th>
<th>T'1x</th>
<th>D'1x</th>
<th>T'2x</th>
<th>D'2x</th>
<th>D1x</th>
<th>D2x</th>
</tr>
</thead>
<tbody>
<tr>
<td>&quot;+&quot;</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;0&quot;</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;-&quot;</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Negative phase current

Table 3. Conduction losses in a three level NPC.

2.2.2 n level topologies for NPC.

As the number of levels for the converter increases the compiled output waveform adds more and more steps producing a staircase waveform which approaches the sinusoidal
wave with less harmonic distortion. Theoretically a zero harmonic distortion at the output
wave signal can be obtained by using an infinite number of levels for the converter [27].

The basic principle for the multilevel Neutral Point Clamped converter topology can
be summarized as follows. An m-level NPC converter consists of m-1 DC link capacitors and is
able to produce m number of levels for the phase voltage [27], [28].

Three different multilevel NPC converters are presented in Figure 9, Figure 11 and
Figure 12 to show the basic difference between the circuits.

![Figure 11. Four level NPC converter.](image)

Figure 12 shows the basic circuit of a five level diode clamped multilevel converter.
The total DC link voltage is divided into four voltage levels by connecting the four DC bus
capacitors in series. The voltage rating over each capacitor is $\frac{U_{dc}}{4}$. The midpoint node of the
DC link is considerate as the neutral point and the possible converter AC output voltage levels
are $-\frac{U_{dc}}{2}$, $-\frac{U_{dc}}{4}$, 0, $\frac{U_{dc}}{4}$ and $\frac{U_{dc}}{2}$ [27], [28].

The three middle nodes of the DC link are connected to the phase legs by means of
clamping diodes to limit the collector-emitter voltages of the switching devices to the voltage
level across only one of the DC link capacitors. The converter consists of 24 switching devices
and each of the phase legs includes 8 switches. The switches in one phase leg are commutated
in such way that at any given time four consecutive switches are conducting. It should be
noted that the clamping diodes must block different voltage levels than the switching devices
in the converter. The voltage levels for the clamping diodes can go as high as $\frac{3U_{dc}}{4}$ of the
total voltage. This requires diodes with different voltage ratings to be used or to implement
series connected clamping diodes in the circuit which will increase the complexity of the
system [27], [28].
Assuming that each blocking diode voltage rating is the same as the switching device voltage rating the number of diodes needed for each phase will be \((m-1)(m-2)\). When the level of the converter is subsequently high the number of diodes required for the topology will make the converter impractical to be implemented [27], [28].

The staircase voltage in the five level NPC converter is obtained using 5 different switch combinations to synthesize the five voltage levels [27]

- For \(U_{a0} = \frac{U_{dc}}{2}\) all upper switches \(Sa1\) through \(Sa4\) are turned on
- For voltage level \(U_{a0} = \frac{3U_{dc}}{8}\) switches \(Sa2\) through \(Sa4\) and \(S'a1\) are turned on
- For \(U_{a0} = \frac{U_{dc}}{2}\) \(Sa3\) and \(Sa4\) are turned on, also \(S'a1\) and \(S'a2\) are also turned on
- For voltage level \(U_{a0} = \frac{U_{dc}}{8}\) \(Sa4\) is turned on and \(S'a1, S'a2\) are turned on
- For voltage level \(U_{a0} = 0\) all lower switches \(S'a1\) through \(S'a4\) are turned on

Figure 12. Five level NPC converter.
Figure 13. Phase and line voltage waveforms of a 5-level NPC converter.

Table 4 shows the voltage levels and the corresponding switch states. It should be noted that each switch is switched only once per cycle. There are four complimentary switch pairs in each phase leg. The complimentary switches are defined such that when turning one of the switches on automatically excludes the other one from being turned on. In phase “a” the complimentary switches are $S_a1 - S'_a1$, $S_a2 - S'_a2$, $S_a3 - S'_a3$ and $S_a4 - S'_a4$ [27].

<table>
<thead>
<tr>
<th>Output $V_{ao}$</th>
<th>Switch state</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V5=V_{DC}/2$</td>
<td></td>
</tr>
<tr>
<td>on</td>
<td>on</td>
</tr>
<tr>
<td>$V4=3V_{DC}/8$</td>
<td></td>
</tr>
<tr>
<td>off</td>
<td>on</td>
</tr>
<tr>
<td>$V3=V_{DC}/4$</td>
<td></td>
</tr>
<tr>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>$V2=V_{DC}/8$</td>
<td></td>
</tr>
<tr>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>$V1=0$</td>
<td></td>
</tr>
<tr>
<td>off</td>
<td>off</td>
</tr>
</tbody>
</table>

Table 4. Voltage levels and their corresponding switch states in five level NPC.
2.3. PMSG parameters estimation.

In order to carry out the modelling and simulation of the system the parameters of the machine are needed. Given that the real machine that will be used in the application is not designed yet, the parameters are determined here. In order to determine the model parameters of the permanent magnet generator the power flow diagram of an ac generator shown in Figure 14 is used [29].

\[
P_{\text{conv}} = T_{\text{conv}} \cdot \omega_{\text{el}} = \frac{3}{2} \cdot E_o \cdot I_{\text{ph}} \cdot \cos \psi
\]
\[
P_{\text{in}} = T_{\text{app}} \cdot \omega_{\text{el}}
\]
\[
P_{\text{out}} = \frac{3}{2} \cdot V_{\text{ph}} \cdot I_{\text{ph}} \cdot \cos \theta
\]

Figure 14. Power flow of an ac generator[29].

Along with the diagram shown above, the following per phase equivalent circuit of the inverter – PMSG system is also necessary for the determination of the machine parameters. The parameters are determined considering that the machine is in steady state working as a generator and a FOC is performed during its operation.

Figure 15. Per phase equivalent circuit of an ac machine.
The parameters of the PMSM used for our simulations are determined below. For it, the following assumptions are taken into account:

- Line to line rms voltage is:

\[ v_{ll_{rms}} = 13 \text{ kV rms} \]  \hspace{1cm} \text{Eq. 2}

The phase rms voltage of the machine is:

\[ v_{ph_{rms}} = \frac{v_{ll_{rms}}}{\sqrt{3}} = \frac{13000}{\sqrt{3}} = 7505.553499 \text{ V rms} \]  \hspace{1cm} \text{Eq. 3}

The peak phase voltage of the machine will be then:

\[ v_{ph_{pk}} = v_{ph_{rms}} \times \sqrt{2} = 10614.45555 \text{ V} \]  \hspace{1cm} \text{Eq. 4}

The PMSG will be controlled using a FOC technique, which means that the back e.m.f. and the phase current are in phase all the time.

\[ \cos (\psi) = 1 \]  \hspace{1cm} \text{Eq. 5}

The efficiency of the machine is considered to be 95%.

\[ \eta = 0.95 \]  \hspace{1cm} \text{Eq. 6}

The nominal rotational speed of the shaft is 5.68 r.p.m.

\[ N_{mec} = 5.68 \text{ rpm} \]  \hspace{1cm} \text{Eq. 7}

Which expressed in rad/s is equal to:

\[ \omega_{mec} = 5.68 \times \frac{2 \times \pi}{60} = 0.594808209 \text{ rad/s} \]  \hspace{1cm} \text{Eq. 8}

The number of pair poles of the machine is considered to be:
The nominal electrical frequency will be then:

\[ \omega_{el} = \omega_{mec} \times n_{pp} \quad \text{Eq. 10} \]

\[ \omega_{el} = 0.594808209 \times 128 = 76.13545076 \frac{\text{rad}}{s} = 2 \pi \times f \quad \text{Eq. 11} \]

\[ f = \frac{\omega_{el}}{2 \pi} = \frac{76.13545076}{2 \pi} = 12.11733333 \text{ Hz} \quad \text{Eq. 12} \]

The active power at the terminals of the generator must be 5MW.

\[ P_{out} = 5\text{MW} \quad \text{Eq. 13} \]

\[ P_{out} = 3 \times P_{ph_{out}} \quad \text{Eq. 14} \]

Taking into account the efficiency of the machine, the power at the input will be:

\[ P_{in} = 5000000 \times \frac{100}{95} = 5263157.895 \text{ W} \quad \text{Eq. 15} \]

The torque in nominal conditions will be then:

\[ T_{app} = \frac{P_{in}}{\omega_{mec}} = \frac{5263157.895 \text{ (W)}}{0.594808209 \text{ (rad/s)}} = 8848495.724 \text{ Nw} \times \text{m} \quad \text{Eq. 16} \]

As the performance of the machine is 95%, 5% of the input power of the generator are losses. The stray losses, mechanical losses and core losses are considered to introduce 4.9% of the total losses. The remaining 0.1% will be considered as copper losses. Hence, it will be considered that only 95.1% of the input power is converted into electrical power.

\[ P_{\text{conv}} = 0.951 \times P_{in} = 0.96 \times 5263157.895 = 5005263.158 \text{ W} \quad \text{Eq. 17} \]
This is the same as considering that only 0.951 of the applied torque, $T_{app}$ will be converted into electrical power:

$$T_{conv} = 0.951 \times T_{app} = 8414919.434 \text{ Nm} \times \text{m} \quad \text{Eq. 18}$$

$$P_{conv} = T_{conv} \times \omega_{mec} \quad \text{Eq. 19}$$

$$P_{conv} = 8494555.895 \times 0.594808209 = 5005263.158 \text{ W} \quad \text{Eq. 20}$$

As the current will be in phase with the back e.m.f:

$$P_{conv} = S_{conv} = 3 \times P_{ph_{conv}} = 3 \times S_{ph_{conv}} \quad \text{Eq. 21}$$

$$Q_{conv} = 3 \times Q_{ph_{conv}} = 0 \quad \text{Eq. 22}$$

The cosine of theta is estimated as:

$$\cos \theta = 0.9 \quad \text{Eq. 23}$$

The angle theta is then:

$$\theta = \cos^{-1} 0.9 = 0.451026811 \text{ rad} = 25.84193276^\circ \quad \text{Eq. 24}$$

The peak value of the current is calculated then:

$$P_{out} = \frac{3}{2} \times v_{ph_{pk}} \times i_{ph_{pk}} \times \cos \theta = 5 \text{ MW} \quad \text{Eq. 25}$$

$$i_{ph_{pk}} = \frac{2 \times P_{out}}{3 \times v_{ph_{pk}} \times \cos \theta} \quad \text{Eq. 26}$$
CONTROL OF 5MW MULTILEVEL CONVERTER FOR DIRECT DRIVE WIND TURBINE APPLICATION

\[
\text{Eq. 27}
\]
\[
\text{Eq. 28}
\]

Given that the phase current and the back e.m.f. are in phase all the time:

\[
P_{\text{conv}} = \frac{3}{2} \times E_{\text{opk}} \times i_{\text{ph pk}} = 5005263.158 \text{ W} \quad \text{Eq. 29}
\]

The peak value of the back e.m.f. is calculated then:

\[
E_{\text{opk}} = \frac{2 \times P_{\text{conv}}}{3 \times i_{\text{ph pk}}} = \frac{2 \times 5005263.158}{3 \times 348.9301629} = 9563.065792 \text{ V} \quad \text{Eq. 30}
\]

As FOC technique will be used, in the synchronous dq reference frame the torque is given by the following expression:

\[
T_e = T_{\text{conv}} = \frac{3}{2} \times \frac{p \times \lambda_{\text{mpm}} \times iq}{i_{\text{ph pk}}} \quad \text{Eq. 31}
\]

Taking into account that when using the FOC technique id = 0 and iq = iphpk, the peak values of the permanent magnet flux linkage is:

\[
\lambda_{\text{mpm}} = \frac{T_{\text{conv}}}{\left(\frac{3}{2}\right) \times p \times i_{\text{ph pk}}} \quad \text{Eq. 32}
\]

\[
\lambda_{\text{mpm}} = \frac{8414919.434}{\left(\frac{3}{2}\right) \times 128 \times 348.9301629} = 125.6059523 \text{ Webers} \quad \text{Eq. 33}
\]

At the terminals of the generator it is known that the active power is 5e6 W and this is equal to:

\[
P_{\text{out}} = \frac{3}{2} \times v_{\text{ph pk}} \times i_{\text{ph pk}} \times \cos \theta = 5e6 \text{ W} \quad \text{Eq. 34}
\]

The reactive power at the output will be:
The output apparent power will be:

\[ Q_{out} = \frac{3}{2} \times v_{ph_{pk}} \times i_{ph_{pk}} \times \sin \theta \]  
\[ \text{Eq. 35} \]

\[ Q_{out} = \frac{3}{2} \times 10614.45555 \times 348.9301629 \times 0.435889894 \]  
\[ \text{Eq. 36} \]

\[ Q_{out} = 2421610.523 \text{ VAR} \]  
\[ \text{Eq. 37} \]

The output apparent power will be:

\[ S_{out} = \frac{3}{2} \times v_{ph_{pk}} \times i_{ph_{pk}} = \sqrt{P_{out}^2 + Q_{out}^2} \]  
\[ \text{Eq. 38} \]

\[ S_{out} = \sqrt{5e6^2 + 2421610.523^2} = 5555555.555 \text{ VA} \]  
\[ \text{Eq. 39} \]

The copper losses are the power dissipated into the phase resistors:

\[ P_R = P_{conv} - P_{out} = 5005263.158 - 5000000 = 5263.158 \text{ W} \]  
\[ \text{Eq. 40} \]

The phase copper loss is also equal to:

\[ P_{phR} = \frac{P_R}{3} = \frac{5263.158}{3} = 1754.385967 \text{ W} \]  
\[ \text{Eq. 41} \]

\[ P_{phR} = \frac{1}{2} \times R \times i_{ph_{pk}}^2 = 1754.385967 \text{ W} \]  
\[ \text{Eq. 42} \]

The phase winding resistance is then:

\[ R = \frac{2 \times P_{phR}}{i_{ph_{pk}}^2} = \frac{2 \times 1754.385967}{348.9301629^2} = 0.028818947 \Omega \]  
\[ \text{Eq. 43} \]

As can be observed the apparent power at the terminals of the generator, \( S_{out} \), is greater than the converted apparent power, \( S_{conv} \). This is due to the phase inductance, which consume reactive power. As the back emf is in phase with the phase current, the reactive power needed is provided by the inverter. The phase reactive power is then:
Because of the signs convention adopted this reactive power will have a negative sign at the inverter generator, indicating that it is actually provided by the inverter and not consumed.

The value of the phase synchronous reactance is then:

\[ X_l = \frac{2 \times Q_{ph_{out}}}{i_{ph_{pk}}^2} \]

Given that the electrical frequency is 12.5 Hz, the values of the phase synchronous inductance can be calculated as following:

\[ L_s = \frac{X_l}{\omega_{el}} = \frac{X_l}{\frac{2 \times \pi \times 12.5}{348.9301629^2}} = 0.168828642 \, \text{H} \]

The calculated value of the inductance is equal to the leakage inductance plus the magnetization inductance, and as the machine is considered to be a surface mounted PM machine:

\[ L_s = L_{ls} + L_m = L_{q} = L_{d} = 0.168828642 \, \text{H} \]

The calculations carried above are resumed in the following table where the main parameters are presented:

<table>
<thead>
<tr>
<th>Nominal Output Power</th>
<th>5 MW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Line-to-line voltage</td>
<td>13 kV rms</td>
</tr>
<tr>
<td>Nominal Current</td>
<td>246.7308843 A rms</td>
</tr>
<tr>
<td>Nominal Torque</td>
<td>8848495.724 Nw * m</td>
</tr>
<tr>
<td>Nominal Speed</td>
<td>5.68 rpm</td>
</tr>
<tr>
<td>Stator Winding Resistance</td>
<td>0.028818947 Ω</td>
</tr>
<tr>
<td>Synchronous inductance</td>
<td>0.168828642 H</td>
</tr>
<tr>
<td>Permanent magnet peak flux linkage</td>
<td>125.6059523 Webers</td>
</tr>
<tr>
<td>Moment of inertia</td>
<td>55e7 kg * m²</td>
</tr>
<tr>
<td>Number of pole pairs</td>
<td>128</td>
</tr>
</tbody>
</table>

Table 5. Machine parameters.
Chapter 3

System description and modelling

The system discussed in the project is composed by a wind turbine, a permanent magnet synchronous generator, a back to back three level NPC converter and the grid. A mathematical model of each element of the system was built and control strategies were implemented. A graph showing the different parts of the system and how they are interconnected is shown in Figure 16.

![Figure 16. Block diagram of the system.](image)

The grid, the converter, the permanent magnet synchronous generator and the turbine are described in this chapter.

3.1 Grid Model

The grid presented in Figure 17 can be modelled in abc reference frame using the following equation:

\[ e_k = R_{\text{grid}} i_k + L_{\text{grid}} \frac{di_k}{dt} + v_{kn} \]

Eq. 49

where:
- \( k \) - represents phase a, b and c,
- \( e_k \) - represents the grid voltage,
- \( R_{\text{grid}} \) - represents the grid resistance,
- \( L_{\text{grid}} \) - represents the grid inductance,
$i_k$ represents the phase current and $v_{kn}$ represents the phase voltage which will be applied at the rectifier terminals.

![Grid model](image)

Figure 17. Grid model (abc reference frame).

For an ease of implementation in the Simulink model the equations will be transferred in dq reference frame. After the transformation the equations will be:

\[
e_d = R_{\text{grid}}i_d + L_{\text{grid}}\frac{di_d}{dt} + v_{dn} - \omega L_{\text{grid}}i_q \quad \text{Eq. 50}
\]

\[
e_q = R_{\text{grid}}i_q + L_{\text{grid}}\frac{di_q}{dt} + v_{qn} + \omega L_{\text{grid}}i_d \quad \text{Eq. 51}
\]

where:

$\omega L_{\text{grid}}i_{d,q}$ are cross-coupling terms introduced by the dq transformation.

From Eq. 50 and Eq. 51 the equations for the rectifier input current can be obtained.

\[
i_d = \frac{1}{L_{\text{grid}}} \int (e_d - R_{\text{grid}}i_d - v_{dn} + \omega L_{\text{grid}}i_q) \quad \text{Eq. 52}
\]

\[
i_q = \frac{1}{L_{\text{grid}}} \int (e_q - R_{\text{grid}}i_q - v_{qn} - \omega L_{\text{grid}}i_d) \quad \text{Eq. 53}
\]

Equations Eq. 52 and Eq. 53 are implemented in Simulink to model the behavior of the grid.
3.2 Level NPC Convertor Model

To construct the mathematical model for the 3 level back to back neutral point clamped convertor a transfer from the physical to an ideal system has to be made. Starting from the model presented in Figure 8 the ideal model is produced as in [18] and displayed in Figure 18. The ideal switches have three positions as explained earlier.

![Figure 18. Back to back equivalent circuit based on ideal switches.](image)

From the current directions it can be seen that the machine part of the convertor acts as an inverter, all these values have the letter i as an index and the grid side of the convertor acts as a rectifier, the letter r is presented as the index for these values. The inverter side of the convertor can be modelled using the following equations:

\[
\begin{align*}
    v_{AN} &= v_{i1} + v_{ON} \\
    v_{BN} &= v_{i2} + v_{ON} \\
    v_{CN} &= v_{i3} + v_{ON}
\end{align*}
\]  

where:

- \(v_{kN}\) – phase to neutral voltage (k= A, B, C)
- \(v_{ij}\) – switch voltage (j= 1, 2, 3)
- \(v_{ON}\) – the voltage from the DC link point to neutral

Taking into consideration that the sum of the phase currents \((i_{i1}, i_{i2}, i_{i3})\) is supposed to be zero, by adding all three equations the voltage \(v_{ON}\) becomes:

\[
v_{ON} = -\frac{1}{3}(v_{i1} + v_{i2} + v_{i3})
\]

Direct substitution of \(v_{ON}\) in Eq. 54 yields the equation written in matrix form:
The similar result is obtained for the rectifier part of the converter as it can be seen in the following equation:

\[
\begin{bmatrix}
V_{AN} \\
V_{BN} \\
V_{CN}
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
2 & 1 & -1 \\
-1 & 2 & -1 \\
-1 & -1 & 2
\end{bmatrix} \begin{bmatrix}
V_{i1} \\
V_{i2} \\
V_{i3}
\end{bmatrix}
\]  

Eq. 56

Because in a 3-level NPC converter, the most important task is to ensure a constant DC voltage and the balance of the two capacitors voltages, two new variables are defined [18]:

\[x_1 = \frac{V_{c1} + V_{c2}}{2}; \quad x_2 = \frac{V_{c1} - V_{c2}}{2}\]  

Eq. 58

where:

\(x_1\) – represents the DC voltage divided by two (the maximum or minimum value of voltage at the output of the converter);

\(x_2\) – represents the difference of capacitors voltages divided by two (this value characterises the balance between the capacitors voltages);

The next step is to define the voltages in the switches as a function of the duty cycle, \(x_1\) and \(x_2\). This is done using a quadratic function with a characteristic as the one presented in the following figure:

![Figure 19. Description of voltage quadratic function \(v_{ij}\)](image)

Analytically, the function presented in Figure 19 can be expressed using the following equations:

\[v_{ij} = x_1 \delta_{ij} + x_2 \delta_{ij}^2 = \delta_{ij} (x_1 + x_2 \delta_{ij})\]  

Eq. 59
In order to obtain the capacitors voltage equations Kirchhoff’s current law is applied to the circuit, as in [ref1], and the result is:

\[ v_{rj} = x_1 \delta_{rj} + x_2 \delta_{rj}^2 = \delta_{rj} (x_1 + x_2 \delta_{rj}) \]

where:

- \( i_{dcr} \) – the capacitance of each DC link capacitor;
- \( i_{dt} \) – the current in the inverter/rectifier part of the DC link (j=1, 2, 3);
- \( \delta \) – the variables used in the quadratic functions.

\[ i_{dcr1} = i_{C1} + i_{dc1} \]
\[ i_{dcr2} = i_{C2} + i_{dc2} \]
\[ i_{dcr3} = i_{C2} + i_{dc3} \]

Equation 60

\[ C \frac{dx_1}{dt} = i_{C1} + i_{C2} \]
\[ C \frac{dx_2}{dt} = i_{C1} - i_{C2} \]

Equation 61

The \( i_{dcj} \) and \( i_{dcj} \) currents are obtained from the phase currents and duty cycle, using a quadratic function, as in [ref].

Figure 20. Description of current function \( i_{dc1} \)

Figure 21. Description of current function \( i_{dc2} \)

Figure 22. Description of current function \( i_{dc3} \)
The currents have the same expressions for the inverter and rectifier part of the convertor and are obtained from the quadratic function presented earlier, as in [2]:

\[
\begin{align*}
    i_{dci1} &= \frac{(\delta_{i1} + 1)\delta_{i1}}{2}i_{i1} + \frac{(\delta_{i1} + 1)\delta_{i2}}{2}i_{i2} + \frac{(\delta_{i3} + 1)\delta_{i3}}{2}i_{i3} \\
    i_{dci2} &= (1 - \delta_{i1}^2)i_{i1} + (1 - \delta_{i2}^2)i_{i2} + (1 - \delta_{i3}^2)i_{i3} \\
    i_{dci3} &= \frac{(\delta_{i1} - 1)\delta_{i1}}{2}i_{i1} + \frac{(\delta_{i1} - 1)\delta_{i2}}{2}i_{i2} + \frac{(\delta_{i3} - 1)\delta_{i3}}{2}i_{i3}
\end{align*}
\]
Eq. 62

By substituting the currents from Eq. 62 in Eq. 61 we obtain the expressions for the capacitors voltages:

\[
\begin{align*}
    C \frac{dx_1}{dt} &= (\delta_{r1}i_{r1} + \delta_{r2}i_{r2} + \delta_{r3}i_{r3}) - (\delta_{i1}i_{i1} + \delta_{i2}i_{i2} + \delta_{i3}i_{i3}) \\
    C \frac{dx_2}{dt} &= (\delta_{r1}^2i_{r1} + \delta_{r2}^2i_{r2} + \delta_{r3}^2i_{r3}) - (\delta_{i1}^2i_{i1} + \delta_{i2}^2i_{i2} + \delta_{i3}^2i_{i3})
\end{align*}
\]
Eq. 63

3.3 Dynamic Model of a Synchronous Permanent Magnet Machine

The voltage and flux linkage equations that describe the electrical behavior of the surface permanent magnet synchronous machine in the abc system are presented below[30]. The complexity and difficulty of these equations is obvious because of the large number of variables which are time and position dependent[30]. A simpler model of the machine is obtained when using a synchronous reference frame.

\[
\begin{align*}
    v_a(t) &= R_i * i_{ph_a}(t) + \frac{d\lambda_a(t)}{dt} \\
    v_b(t) &= R_i * i_{ph_b}(t) + \frac{d\lambda_b(t)}{dt} \\
    v_c(t) &= R_i * i_{ph_c}(t) + \frac{d\lambda_c(t)}{dt}
\end{align*}
\]
Eq. 64
Eq. 65
Eq. 66

\[
\begin{align*}
    \lambda_a(t) &= L_{as} * i_{ph_a}(t) + L_{abs} * i_{ph_b}(t) + L_{acs} * i_{ph_c}(t) + \lambda_{apmp}(t) \\
    \lambda_b(t) &= L_{abs} * i_{ph_a}(t) + L_{bs} * i_{ph_b}(t) + L_{abc} * i_{ph_c}(t) + \lambda_{bpm}(t) \\
    \lambda_c(t) &= L_{acs} * i_{ph_a}(t) + L_{bcs} * i_{ph_b}(t) + L_{cs} * i_{ph_c}(t) + \lambda_{cpm}(t)
\end{align*}
\]
Eq. 67
Eq. 68
Eq. 69

3.3.1. dq model of the PMSM

A permanent magnet synchronous machine which has \( n_{pp} \) pair of poles and rotates at a mechanical speed \( \omega_{mech} \) can be regarded as a one pair pole machine rotating at electrical speed \( \omega_{el} \) due to magnetic symmetry. In order to obtain the model of the machine in the
synchronous reference frame dq, the Park Transformation must be applied. Two of the main advantages of applying the transformation is that the number of equations is reduced and the values of the different inductances of the machine are not position dependent any more simplifying the control of the machine\cite{30}, \cite{31}.

The dq reference axes are placed on the rotor of the machine and will rotate the with the same angular speed $\omega_{el}$. The consequence of this is that the three phase stationary windings are transformed in two rotating windings and hence in steady state all machine parameters will be constants.

The d axis has to be placed along the magnetic axis of the rotor and the q axis perpendicular to it. Both axes form $\pi/2$ electrical radians, which correspond to $(\pi/2)/n_{pp}$ mechanical degrees \cite{31}. This is shown in Figure 23. As the type of motor considered for the project is a surface mounted permanent magnet, the $L_d$ and $L_q$ are equal \cite{32}.

![dq axes definition](image)

The voltage equations in the dq synchronous reference frame are:

\begin{align*}
v_q(t) &= R \cdot i_q(t) + p \cdot \lambda_q(t) + \omega_{el} \cdot \lambda_d(t) \quad \text{Eq. 70} \\
v_d(t) &= R \cdot i_d(t) + p \cdot \lambda_d(t) - \omega_{el} \cdot \lambda_q(t) \quad \text{Eq. 71}
\end{align*}

Where:
- $p$: is the derivative operator $d/dt$

The flux linkage equations in the dq synchronous reference frame are:

\begin{align*}
\lambda_q(t) &= (L_{qs} + L_{mq}) \cdot i_q(t) = L_q \cdot i_q(t) \quad \text{Eq. 72} \\
\lambda_d(t) &= (L_{ds} + L_{md}) \cdot i_d(t) + \lambda_{mp}(t) = L_d \cdot i_d(t) + \lambda_{mpm} \quad \text{Eq. 73}
\end{align*}

Torque equation:
\[ T_e(t) = \frac{3}{2} N_{pp} \lambda_{mpm} i_q(t) \]  
Eq. 74

Mechanical equations:

\[ T_e(t) - T_i(t) = J \frac{d\omega_{mec}(t)}{dt} \]  
Eq. 75

\[ \omega_{mec}(t) = \frac{\omega_{el}(t)}{N_{pp}} \]  
Eq. 76

3.4 Wind Turbine.

The model of the wind turbine implemented in the simulation will be a simplified one, constructed base on the Wind Turbine Block presented in Matlab Simulink [33].

The input variables for the model are the ones provided by the DeepWind Project so the maximum wind speed is considered to be 15 m/sec.

The behaviour of the wind turbine model is presented in the following figure:

![Wind turbine characteristic](image)

Figure 24. Wind turbine characteristic [33].

In order to simplify the model the values from this characteristic are used to create two functions. The first function is created in order to obtain the maximum power from the wind turbine as a function of the wind speed and the second function gives the optimal rotational speed of the turbine as a function of the wind speed. Through this approach the
wind turbine will provide for each wind speed the optimum rotational speed for the turbine in order to obtain the maximum power.

The values taken from the wind turbine characteristic were analysed using the Matlab functions *polyval* and *polifit* in order to obtain the coefficient for the function. The result of this analysis provides the two functions for the wind turbine model:

\[
\omega = f(u) = 15 \times u \quad \text{Eq. 77}
\]

\[
P = f(u) = -2.9583 \times 10^{-8}u^4 + 2.9732 \times 10^{-4}u^3 - 1.0602 \times 10^{-5}u^2 + 2.9278 \times 10^{-5}u \quad \text{Eq. 78}
\]

The characteristic of the two functions are displayed in the following figure along with the torque characteristics.

![Wind turbine behaviour](image)

**Figure 25. Functions results.**

It can be observed that the rotational speed of the generator has a linear dependency of the wind speed, while the power and the load increase more slowly in the first part.

The torque function is determined from the other two functions, dividing power by the speed. The output values are given in per-unit so a multiplication with the nominal values is required.
Chapter 4

System Control

In the present chapter two control strategies are presented. One strategy is applied to the PMSG and it consists of a FOC technique. The second strategy is commonly named as current mode control and it is used in order to control the active and reactive power sent to the grid.

4.1. Rectifier control

The rectifier control method used in this report is based on voltage oriented control, as presented in [34]. The block diagram of the rectifier control is presented in Figure 26.

![Block diagram of rectifier control system with dq current control](image)

Figure 26. Block diagram of rectifier control system with dq current control.

The principle behind this control method is to control the dq current ($i_{d,q}$) using the phase voltage ($v_{d,q,n}$), the grid voltage ($e_{d,q}$), and the DC voltage ($V_{dc}$). The control can be separated in two levels. The interior level is represented by the current controllers and the external level is represented by the DC voltage controller and the reactive power controller.
A PI controller structure will be used in each case, with the structure as presented in Figure 27:

![Figure 27. Structure of PI controller.](image)

In the following of this subchapter the control strategy along with method to determine the parameters for the PI controllers will be presented step by step for each controller.

### 4.1.1. Current controllers

In order to design the current controllers for the rectifier the equations of the grid model are necessary.

\[
e_d = R_{\text{grid}} i_d + L_{\text{grid}} \frac{d i_d}{dt} + v_{dn} - \omega L_{\text{grid}} i_q \quad \text{Eq. 79}
\]

\[
e_q = R_{\text{grid}} i_q + L_{\text{grid}} \frac{d i_q}{dt} + v_{qn} + \omega L_{\text{grid}} i_d \quad \text{Eq. 80}
\]

Starting from the grid equations the reference values for the rectifier can be determined. These values are represented by the phase voltages \((v_{d,q})\). To obtain these voltages the equations will become:

\[
v_{dn} = e_d - R_{\text{grid}} i_d - L_{\text{grid}} \frac{d i_d}{dt} + \omega L_{\text{grid}} i_q \quad \text{Eq. 81}
\]

\[
v_{qn} = e_q - R_{\text{grid}} i_q - L_{\text{grid}} \frac{d i_q}{dt} - \omega L_{\text{grid}} i_d \quad \text{Eq. 82}
\]

A problem appears at this stage because the two axes are coupled by the \(\omega L_{\text{grid}} i_{d,q}\) terms. This problem will be solved by introducing the feed-forward terms in the PI controllers, procedure which is similar as for the machine control. Besides the coupling terms the feed-forward terms will also contain the voltage from the grid, as it can be seen in the following equations:
Once the feed-forward components are determined the structure of the PI controllers can be presented:

\[ v_{dn} = \left( k_{pi} + \frac{k_{ii}}{s} \right) (i_d^* - i_d) + V_{df} \] \hspace{1cm} \text{Eq. 85}

\[ v_{qn} = \left( k_{pi} + \frac{k_{ii}}{s} \right) (i_q^* - i_q) + V_{qf} \] \hspace{1cm} \text{Eq. 86}

With the structure of the PI established the transfer function of the current can be determined by joining Eq. 81 with Eq. 85 and Eq. 82 with Eq. 86, as it can be seen in the following.

\[ v_{dn} = \left( k_{pi} + \frac{k_{ii}}{s} \right) (i_d^* - i_d) + V_{df} = -R_{grid} i_d - L_{grid} \frac{di_d}{dt} + V_{dfr} \] \hspace{1cm} \text{Eq. 87}

\[ v_{qn} = \left( k_{pi} + \frac{k_{ii}}{s} \right) (i_q^* - i_q) + V_{qf} = -R_{grid} i_q - L_{grid} \frac{di_q}{dt} + V_{qfr} \] \hspace{1cm} \text{Eq. 88}

The feed-forward components are going to be eliminated from both sides of the equal and the equations in Laplace domain will become:

\[ \left( k_{pi} + \frac{k_{ii}}{s} \right) (i_d^* - i_d) = -R_{grid} i_d - sL_{grid} i_d \] \hspace{1cm} \text{Eq. 89}

\[ \left( k_{pi} + \frac{k_{ii}}{s} \right) (i_q^* - i_q) = -R_{grid} i_q - sL_{grid} i_q \] \hspace{1cm} \text{Eq. 90}

Once having these equations the axis can be combined in vectorial form again considering:

\[ i_{d}^* = i_d^* + j i_q^* \] \hspace{1cm} \text{Eq. 91}

\[ i_{d} = i_d + j i_q \] \hspace{1cm} \text{Eq. 92}

In this case the main equation will become:

\[ \left( k_{pi} + \frac{k_{ii}}{s} \right) i_{dq} - \left( k_{pi} + \frac{k_{ii}}{s} \right) i_{d} = (-R_{grid} - L_{grid} s) i_{q} \] \hspace{1cm} \text{Eq. 93}

Both sides of the equal will be multiply with s to eliminate the s in the denominator and the \( i_{dq} \) component will be transferred to the other side of the equal. By doing this the equation will be:
The transfer function of the current is:

\[
H_i(s) = \frac{i_{dq}}{i_{dq}} = \frac{k_{pi}s + k_{ii}}{-L_{grid}s^2 + (-R_{grid} + k_{pi})s + k_{ii}}
\]  
Eq. 95

Once the transfer function of the current was determined the next step is to tune the current controllers. This procedure is done by allocating the poles of the transfer function. The poles are the roots of the characteristic equation.

\[-L_{grid}s^2 + (-R_{grid} + k_{pi})s + k_{ii} = 0\]  
Eq. 96

In the following the poles will be represented by \(p_1\) and \(p_2\) and they have to fulfil the conditions:

\[
p_1 + p_2 = \frac{(-R_{grid} + k_{pi})}{L_{grid}}
\]  
Eq. 97

\[
p_1 * p_2 = -\frac{k_{ii}}{L_{grid}}
\]  
Eq. 98

In order to have a stable behaviour of the system the poles must be selected from the left half plane, which means that the real part has to be negative. In this case the PI coefficients will become:

\[k_{pi} = L_{grid}(p_1 + p_2) + R_{grid}\]  
Eq. 99

\[k_{ii} = -L_{grid}(p_1 * p_2)\]  
Eq. 100

Like in the control of the machine case the current loop has to be faster than the speed loop, by an approximation, the current loop has to be at least ten times faster than the speed loop.

The time constants of the regulator are:

\[
T_1 = -\frac{1}{p_1}
\]  
Eq. 101

\[
T_2 = -\frac{1}{p_2}
\]  
Eq. 102

Based on the parameters of the system the user has to select the time constants of the PI controller.

The first time constant of the PI controller is selected to be equal to the time constant of the electrical circuit.

\[
T_1 = \frac{R_{grid}}{L_{grid}} = \frac{1.5}{0.05} = 0.033 \text{ [seconds]}
\]
Because the first time constant of the PI controller is equal to the time constant of the electrical circuit the two poles are going to get simplified and the second order equation will become a first order equation. Because of the simplification the second time constant will control the behaviour of the system. This has to be selected faster than the previous one for the system to have an adequate response.

In order to obtain the best tuning parameters three time variables are tested with the step function to determine the behaviour of the system. As it can be seen in Figure 28 the first time variable represented by the blue line has a response which is too slow for the control that we want to implement. The red line, which represents the system with the fastest response, presents an aggressive behaviour which can affect the stability of the system. The variable presented in the middle of the range is selected to be used for the model because it provides a fast enough response which doesn’t affect the stability of the system.

![Figure 28. The step response for different time variables.](image)

In the model used in this report the time constant is selected to be one hundred times smaller than the time constant of the electrical circuit.

\[ T_2 = 0.01 \times T_1 = 0.01 \times 0.033 = 0.00033 \text{ [seconds]} \]

With these two values for the time constant the coefficients of the PI controller can be determined.

\[ k_{pi} = -150 \quad \quad \quad \quad k_{ii} = -4500 \]

Once the coefficients are determined the transfer function of the current is obtained:
To test the behaviour of the transfer function a step is applied at the input. The result is displayed in Figure 28. As it can be seen the system response is according to the second time constant selected and no steady state error appears.

In order to test the stability of the system a root locus will be constructed. The result is displayed in Figure 29. From the result it can be seen that the system is stable for every value of the gain because the characteristic remains in the left half plane.

The transfer function has to be tested also for frequency response. For this purpose the Bode diagram is constructed and displayed in Figure 30. From the results it can be seen that the gain margin is infinite and the phase margin is equal to $-180^\circ$. These results provide the information that the current transfer function is stable and it does not have steady state errors.

$$H_1(s) = \frac{150s + 4500}{0.05s^2 + 151.5s + 4500}$$

Figure 29. Root locus of the current transfer function.
4.1.2. DC voltage controller

In order to create the controller for the DC voltage the equation which models the system is required [34], [36].

In this case the DC voltage is modelled as a pure capacitor which stores energy according to the formula:

\[ E_c = \frac{1}{2} CV_{dc}^2 \]  \hspace{1cm} Eq. 103

The time derivative of this stored energy has to be equal to the sum of input power and output power, with the power direction according to Figure 31 [34], [36].

\[ \frac{1}{2} C \frac{dV_{dc}^2}{dt} = P_{in} - P_{out} \]  \hspace{1cm} Eq. 104

A problem appears when using this equation to simulate the model because, as it can be seen in Eq. 104 the equation is not linear with respect to \( V_{dc} \).

In order to solve this problem the system has to be linearized. This is done by replacing \( V_{dc}^2 \) with a new variable, \( W \), and Eq. 104 becomes linear with respect to \( W \):
To create the controller for this system the input and output power has to be defined for our system.

The input power is considered to be the power that comes from the grid to the DC link and the output power is considered to be the power that goes from the DC link to the motor.

The equation for the input active and reactive power to the converter is:

\[ P = \frac{3}{2} (v_q i_q + v_d i_d) \]  \hspace{1cm} \text{Eq. 106} \\
\[ Q = \frac{3}{2} (v_q i_d + v_d i_q) \]  \hspace{1cm} \text{Eq. 107}

The control strategy applied for the rectifier maintains the \( i_d \) current equal to zero and because \( e_d \) grid voltage is equal to zero from the Park transformation the unity power factor is achieved in the grid side. This means that the input power is equal with:

\[ P_{in} = \frac{3}{2} v_q i_q \]  \hspace{1cm} \text{Eq. 108}

Because the output of the DC voltage PI controller is the current \( i_q \) Eq. 108 will be replaced in Eq. 105 and the current will be obtained:

\[ i_q = \frac{C}{3 v_q} \frac{dW}{dt} + P_{out} \]  \hspace{1cm} \text{Eq. 109}

Once this form is obtained for the current the equation for the PI controller which provides the reference \( i_q^* \) current is introduced:

\[ i_q^* = \left( k_{pw} + \frac{k_{iw}}{s} \right) (W^* - W) = \frac{C}{3 v_q} \frac{dW}{dt} + P_{out} \]  \hspace{1cm} \text{Eq. 110}

In order to obtain the transfer function Eq. 110 is transformed into Laplace domain and the \( P_{out} \) is considered to be equal to zero.

\[ \left( k_{pw} + \frac{k_{iw}}{s} \right) W^* - \left( k_{pw} + \frac{k_{iw}}{s} \right) W = \frac{C}{3 v_q} s W \]  \hspace{1cm} \text{Eq. 111}

From Eq. 111 we can determine the transfer function:

\[ H_w(s) = \frac{W}{W^*} = \frac{k_{pw}s + k_{iw}}{C s^2 + k_{pw}s + k_{ii}} \]  \hspace{1cm} \text{Eq. 112}

The tuning of the DC voltage controller is made in the same way as for the current controller, by determining the positions of the poles in the left half plane of the system.

The poles of the system, which represent the roots of the characteristic equation \( q_1 \) and \( q_2 \) must fulfil the following equations:
As in the case of the machine control the current control loop has to be faster than the DC voltage control loop because the dynamic of the current is faster than the dynamic of the DC voltage. The same difference between the poles is applied here as for the machine controller.

The tuning condition that ensures that the current loop is faster than the DC voltage loops is:

\[ q_1 = \frac{p_1}{14} = -\frac{30}{14} = -2.1429 \quad \text{and} \quad q_1 = \frac{p_1}{14} = -\frac{3000}{14} = -214.2857 \]

With the poles determined the PI controller coefficients and the transfer function can be calculated:

\[ k_{pw} = -1.9154 \times 10^{-6} \quad \text{and} \quad k_{iw} = -4.0638 \times 10^{-5} \]

\[ H_w(s) = \frac{1.9154 \times 10^{-6} s + 4.0638 \times 10^{-5}}{8.85 \times 10^{-9} s^2 + 1.9154 \times 10^{-6} s + 4.0638 \times 10^{-5}} \]

To determine the behaviour of the system a step input is applied. The result is displayed in Figure 32 and it can be seen that no steady state errors are introduced.

![Step response of the speed transfer function Hw(s)](image)

Figure 32. The response of the DC voltage transfer function when a step is applied.
The stability of the system is tested by constructing the root locus. The result displayed in Figure 33 provides the information that the system stability is independent of the gain. The system is stable for every value of the gain applied because the characteristic is present only in the left half plane.

The last test applied to the transfer function is the frequency response test. For this the Bode diagram is constructed and displayed in Figure 34. From the results it can be seen that the gain margin is infinite and the phase margin is equal to 171.99° for $\omega=30.3$ rad/sec.

![Figure 33. Root locus of the DC voltage transfer function.](image)
4.1.3. Reactive power controller

Using Eq. 106 and Eq. 107 the active and reactive power from or to the grid can be determined. As it was explained earlier the control strategy in normal working conditions maintains the $I_d$ current equal to zero to ensure that the rectifier provides unity power factor. Because in the project presented in this report there are situations when reactive power is needed, for example in a voltage drop situation, the controller has to be able to control the amount of reactive power produced.

In order to implement the control on the real turbine it must respect a series of requirements presented in the grid codes [37]. The reactive power control becomes a priority when an abnormal event appears in the system. One of the biggest problems encountered in such a system is represented by the voltage drop [37]. The grid codes have very specific requirements for the tolerance in this kind of situation as presented in Figure 35 [37]. These requirements must be complied for symmetrical as well as for asymmetrical faults, for one, two or three phases.

It can be seen in Figure 35 that the grid codes require that the turbine must withstand voltage drops down to 20% of the voltage in the point of connection over a period of minimum 0.5 seconds without disconnecting.
The voltage drop can be separated in three areas where the behaviour has to be different:

- **Area A**: the wind power plant has to stay connected to the grid and uphold normal protection;

- **Area B**: the wind power plant has to stay connected to the grid. The wind power plant must provide voltage support by supplying reactive power. The amount of reactive power that the wind power plant has to supply is depicted in Figure 36;

- **Area C**: the wind power plant can be disconnected;

![Diagram showing voltage drop areas](image)

Figure 35. Requirements for tolerance of voltage drops for wind power plants with an output power greater than 1.5MW [37].
Figure 36. Requirements for reactive power supply, $I_Q$, during voltage drops for wind power plants with a power output greater than 1.5MW [37].

The control must behave as the characteristic in Figure 36 because the reactive power has to follow the control characteristic with a tolerance of ±20% after 100 ms. In Area B the supply of reactive power has first priority, while the supply of active power has second priority.

Another requirement is for the active power to be maintained constant during the voltage drop, but a reduction in active power is acceptable [37].

The control method, as presented in the bloc diagram in Figure 26 is an open loop control, where the normalized rms voltage of the grid is the input variable. From the input variable, using the diagram in Figure 36 the report $\frac{I_Q}{I_N}$ is determined which is multiply by the nominal current in order to obtain the reference for the reactive current.

In the simulation the diagram is implemented using the Matlab Function block which separates the entire voltage spectre in three regions:

- If $E_{Norm} \geq 0.9$, then $\frac{I_Q}{I_N} = 0$;
- If $0.9 > E_{Norm} > 0.5$, then $\frac{I_Q}{I_N} = - \frac{1}{0.4} \ast E_{Norm} + \frac{0.9}{0.4}$;
- If $E_{Norm} \leq 0.5$, then $\frac{I_Q}{I_N} = 1$;
From these three regions it can be seen that if the grid voltage is maintained above 90% of its nominal value the control will be affiliated with Area A and no reactive power will be transmitted into the grid. If the grid voltage drops within a [50, 90] per cent region a reference for the reactive power will be introduced into the system according to the equation presented earlier. In the third region, when the grid voltage drops below 50% the reference for the reactive current will become equal with one.

4.2. Machine Control

The machine control method used in this report is based on flux oriented control, as presented in [34]. Based on the advantages that the dq transformation offers for the induction machine and synchronous machine, like the possibility to control the torque by simply controlling the current, similar to the DC machine, field oriented control has the purpose to control the current in such a way that maximum torque is obtained at any moment for minimum current [31]. The block diagram of the machine control is presented in Figure 26 [30].

![Figure 26. Block diagram of a flux oriented control system](image)

The principle behind this method is to control the speed using the torque and the dq currents ($i_{d,q}$). The control can be separated in two levels. The interior level is represented by the current controllers and the external level is represented by the speed controller. For each controller the PI structure will be used, with the structure as presented in Figure 27:

![Figure 27. Structure of PI controller](image)
In the following of this subchapter the control strategy along with method to
determine the parameters for the PI controllers will be presented step by step for each
controller.

4.2.1. Current Controllers

In order to design the current controllers the equations of the machine model are
necessary. Eq. 50 and Eq. 51 represent the machine model in dq reference frame.

\[ v_d = R_s i_d + L_d \frac{d}{dt} i_d - \omega_r L_q i_q \]  \hspace{1cm} \text{Eq. 115}

\[ v_q = R_s i_q + L_d \frac{d}{dt} i_q + \omega_r (\lambda_{PM} + L_d i_d) \]  \hspace{1cm} \text{Eq. 116}

Starting from the machine equations the reference values for the converter can be
determined. These values are represented by the voltages \((v_{d,q})\).

A problem appears at this stage because of the dq transform, the two axes are coupled
by the \(\omega_r L_{d,q} i_{d,q}\) terms. This problem will be solved by introducing the feed-forward terms in
the PI controllers, as it can be seen in the following equations:

\[ V_{dff} = -\omega_r L_q i_q \]  \hspace{1cm} \text{Eq. 117}

\[ V_{qff} = \omega_r (\lambda_{PM} + L_q i_d) \]  \hspace{1cm} \text{Eq. 118}

Once the feed-forward components are determined the structure of the PI controllers
can be presented:

\[ v_d = \left(k_{pi} + \frac{k_{ii}}{s}\right) (i_d^* - i_d) + V_{dff} \]  \hspace{1cm} \text{Eq. 119}

\[ v_q = \left(k_{qi} + \frac{k_{ii}}{s}\right) (i_q^* - i_q) + V_{qff} \]  \hspace{1cm} \text{Eq. 120}

With the structure of the PI established the transfer function of the current can be
determined by joining Eq. 50 with Eq. 85 and Eq. 51 Eq. 82 with Eq. 86, as it can be seen in
the following.

\[ v_d = \left(k_{pi} + \frac{k_{ii}}{s}\right) (i_d^* - i_d) + V_{dff} = R_s i_d + L_d \frac{d}{dt} i_d + V_{dff} \]  \hspace{1cm} \text{Eq. 121}

\[ v_q = \left(k_{qi} + \frac{k_{ii}}{s}\right) (i_q^* - i_q) + V_{qff} = R_s i_q + L_q \frac{d}{dt} i_q + V_{qff} \]  \hspace{1cm} \text{Eq. 122}

The feed-forward components are going to be eliminated from both sides of the equal
and the equations in Laplace domain will become:
Once having these equations the axis can be combined in vectorial form considering:

\[ i_s^* = i_d^* + j i_q^* \quad \text{Eq. 125} \]
\[ i_s = i_d + j i_q \quad \text{Eq. 126} \]
\[ L_s = L_d + j L_q \quad \text{Eq. 127} \]

In this case the main equation will become:

\[ (k_{pi} + \frac{k_{ii}}{s}) i_d^* - \left( k_{pi} + \frac{k_{ii}}{s} \right) i_q = (R_s + s L_d) i_d \quad \text{Eq. 128} \]

Both sides of the equal will be multiply with \( s \) in order to eliminate the \( s \) in the denominator and the \( i_d q \) component will be transferred to the other side of the equal. By doing this the equation will be:

\[ (k_{pi} s + k_{ii}) i_d^* = \left[ L_s s^2 + (R_s + k_{pi}) s + k_{ii} \right] i_s \quad \text{Eq. 129} \]

The transfer function of the current is:

\[ H_i(s) = \frac{i_d}{i_s} = \frac{k_{pi} s + k_{ii}}{L_s s^2 + (R_s + k_{pi}) s + k_{ii}} \quad \text{Eq. 130} \]

Once the transfer function of the current was determined the next step is to tune the current controllers. This procedure is done by allocating the poles of the transfer function. The poles are the roots of the characteristic equation.

\[ L_s s^2 + (R_s + k_{pi}) s + k_{ii} = 0 \quad \text{Eq. 131} \]

In the following the poles will be represented by \( p_1 \) and \( p_2 \) and they have to fulfil the conditions:

\[ p_1 + p_2 = -\frac{(R_s + k_{pi})}{L_s} \quad \text{Eq. 132} \]
\[ p_1 * p_2 = \frac{k_{ii}}{L_s} \quad \text{Eq. 133} \]

In order to have a stable behaviour of the system the poles must be selected from the left half plane, which means that the real part has to be negative. In this case the PI coefficients will become:
Like in the control of the machine case the current loop has to be faster than the speed loop, by an approximation, the current loop has to be at least ten times faster than the speed loop.

The time constants of the regulator are:

\[ T_1 = -\frac{1}{p_1} \quad \text{Eq. 136} \]
\[ T_2 = -\frac{1}{p_2} \quad \text{Eq. 137} \]

Based on the parameters of the system the user has to select the time constants of the PI controller. Starting from this point the poles and the coefficients of the PI controller are determined.

The first time constant is selected to be equal with the time constant of the electrical circuit in order to simplify the transfer function from a second order equation to a first order equation. Then \( T_1 \) will become:

\[ T_1 = \frac{R_s}{L_s} = \frac{0.02882}{0.16883} = 5.8583 \text{ [seconds]} \]

The second time constant of the PI controller has to be selected smaller than the electrical time constant in order to obtain a good control of the system. The second time constant is selected to be two hundred times smaller than the time constant.

\[ T_2 = \frac{5.8583}{200} = 0.0293 \text{ [seconds]} \]

With the two time constants selected the coefficients of the PI controller can be calculated.

\[ k_{pi} = 5.7638 \]
\[ k_{ii} = 0.9839 \]

The transfer function of the system becomes:

\[ H_i(s) = \frac{5.7638 s + 0.9839}{0.1688 s^2 + 5.793 s + 0.9839} \]

In order to observe the behaviour of the system a step input is applied. The result can be observed in Figure 39. It can be observed that the system reaches steady state in approximately 0.1 seconds, which means that the time constant of the system is the second time constant selected earlier.
Figure 39. The response of the current transfer function when a step is applied.

The stability of the transfer function is tested by constructing the root locus. The result is presented in Figure 40. As it can be seen the system remains in the left half plane for every value of the gain, which means that the system is stable.

Figure 40. Root locus of the current transfer function.

The third and the last test of the transfer function is made using the Bode diagram which determines the frequency response of the system. As it can be seen from Figure 41 the
gain margin is infinite and the phase margin is -180°. The system frequency response proves that the system is stable.

Figure 41. Bode diagram of the current transfer function.

4.2.2. Speed Controller

Like in the current controller case the equation of the machine are required to develop the control. In this case the mechanical equation is used, in which the speed varies based on the torque. The mechanical equation is presented in Eq. 138.

\[
\frac{J}{npp} \frac{d\omega_r}{dt} = T_e - T_l
\]

Eq. 138

where: 
- \( J \) – moment of inertia [kg*m]
- \( npp \) – number of pole pairs
- \( \omega_r \) – rotor electrical speed [rad/sec]
- \( T_e \) – electric torque [Nm]
- \( T_l \) – load torque [Nm]

The speed controller applied in field oriented control has to provide the reference \( i^*_q \) current to the current controller. Because the output of the speed controller is the torque, it has to be transformed to current by a gain \( k_T \). The gain is determined from the torque equation of the machine obtained after dq transformation.
Because in our case the machine is a PM synchronous machine with equal inductances on the d and q axes, Eq. 139 can be simplify to the following form:

\[ T_e = \frac{3}{2} n_{pp} \lambda_{PM} (I_d - L_q i_d) i_q \]  

Eq. 139

\[ T_e = \frac{3}{2} n_{pp} \lambda_{PM} i_q \]  

Eq. 140

Eq. 140 is used to obtain the \( k_T \) coefficient, which makes the translation from torque, which will be the output of the speed controller to the \( i_q \) current which will be the reference for the current controller. The coefficient is:

\[ k_T = \frac{i_q}{T_e} = \frac{2}{3 \cdot n_{pp} \lambda_{PM}} \]  

Eq. 141

Once the transfer function from torque to current is determined the PI speed controller can be designed. The design of the controller starts from Eq. 138 which is rearranged to obtain the electrical torque from the speed. Besides this, the equation is transferred in Laplace domain and the load torque is considered to be equal to zero (\( T_l = 0 \)). After these changes the equation will become:

\[ T_e = \frac{J}{n_{pp}} s \omega_r \]  

Eq. 142

The equation of the PI speed controller is:

\[ T_e^* = (k_{p \omega} + \frac{k_{i \omega}}{s}) (\omega_r^* - \omega_r) = \frac{J}{n_{pp}} s \omega_r \]  

Eq. 143

If the equation is multiplied on both sides with \( s \) to eliminate the \( s \) in the denominator and if the speed component is transferred to the other side of the equal the equation will become:

\[ (k_{p \omega} s + k_{i \omega}) \omega_r^* = \frac{J}{n_{pp}} s^2 + k_{p \omega} s + k_{i \omega} \omega_r \]  

Eq. 144

From Eq. 144 the transfer function will become:

\[ H(s) = \frac{\omega_r}{\omega_r^*} = \frac{k_{p \omega} s + k_{i \omega}}{\frac{J}{n_{pp}} s^2 + k_{p \omega} s + k_{i \omega}} \]  

Eq. 145

Once the transfer function of the speed controller was determined the next step is to select the poles of the transfer function. The characteristic equation is:

\[ \frac{J}{n_{pp}} s^2 + k_{p \omega} s + k_{i \omega} = 0 \]  

Eq. 146

The roots of the transfer function, which in this case represent the poles of the characteristic equation, must respect the following conditions:
In order for the system to be stable the poles must be selected from the left half side, which means that the real part of the poles has to be negative. From Eq. 147 and Eq. 148 the coefficients of the PI controller can be determined:

\[ q_1 + q_2 = -\frac{npp \cdot k_{p\omega}}{J} \quad \text{Eq. 147} \]
\[ q_1 \cdot q_2 = \frac{npp \cdot k_{i\omega}}{J} \quad \text{Eq. 148} \]

Because the time constant of the mechanical system is slower from the time constant of the electrical system the poles for the speed transfer function must be selected considering this problem. This is why both poles are selected starting from the current transfer function and applying the difference coefficient. In the case presented in this report the difference coefficient will be selected to be equal to fourteen, then the poles become equal to:

\[ q_1 = \frac{p_1}{14} = -0.1707 \cdot 14 = -0.0122 \quad q_1 = \frac{p_1}{14} = -34.1399 \cdot 14 = -2.4386 \]

From these poles values the coefficients of the PI controller can be calculated.

\[ k_{p\omega} = -\frac{J}{npp} (q_1 + q_2) \quad \text{Eq. 149} \]
\[ k_{i\omega} = \frac{J}{npp} (q_1 \cdot q_2) \quad \text{Eq. 150} \]

A root locus of the transfer function is created to observe the stability of the system. The result can be observed in Figure 33. As it can be seen the system is stable for every value of the gain, because the characteristic remains in the left half plane.

The frequency response of the transfer function is determined constructing the Bode diagram. From the result displayed in Figure 34 it can be observed that the gain margin is infinite and the phase margin is equal to 174.3° at \( \omega = 0.2438 \) rad/sec.
Figure 42. The response of the speed transfer function when a step is applied.

Figure 43. Root locus of the speed transfer function.
These results provide the information that the system created with the selected time constants is stable.
Chapter 5

Simulation Results

In this chapter the results of the simulation will be presented for different working conditions like: normal operation, starting the turbine, stopping the turbine and voltage dip situation.

5.1. Normal operation

In the normal operation mode the generator is working at nominal values and it is providing power to the grid. The speed of the wind is considered to be constant, which means that the speed of the turbine is also constant and working at nominal value.

The shape of the current in both sides is presented in the following figure:

![Current in the machine side](image1)

![Current in the grid side](image2)

Figure 45. The current in both sides of the system.

The shape of the voltage in both sides is presented in the following figure:
Because the voltage and the current are constant the active power is constant and is equal with the nominal value. As it can be seen in the following figure the reactive power in the machine side of the converter is constant and positive because the inductors presented in the machine consume reactive power which comes from the converter, opposite to the power flow.

Figure 46. The voltage in both sides of the system.

Figure 47. The active and reactive power at the machine terminals.
It should be mentioned that the entire model was created to have the positive power flow from the grid to the generator. This means that the model of the machine was built using the motor equations, and if the active power is negative, as in Figure 45 it means that machine works as a generator and power is transferred to the grid.

The direction of the power can also be observed in the grid side of the converter, where the active power is negative. In this case the reactive power consumed by the inductors which model the grid is also negative because this power comes from the converter and has the same direction as the power flow.

Figure 48. The voltage in both sides of the system.

5.2. Stopping the turbine

The stopping procedure is applied when the wind speed decreases under a certain value for which the wind turbine cannot function.

In this simulation the wind speed is reduced from nominal value to zero in a time interval of 50 seconds. The normal time needed to stop the turbine has to be greater but because of the long simulation time and the amount of virtual memory required the simulation was made to last for only 52 seconds. The wind speed targets the rotation speed of the turbine to reduce linearly to zero. This strategy is implemented in the wind turbine block in order to obtain the maximum power at any given wind speed. The behaviour of the rotation speed can be seen in Figure 49 along with the reference for the electrical speed. It can be observed that the measured speed follows very close the reference speed, meaning that the control provides a good result.
The waveform of the currents on both sides of the convertor has the shape as presented in the following figure:

Figure 49. Electrical speed of the turbine ($\omega_e$)

Figure 50. The current in both sides of the system.
The behaviour of the voltages on both sides of the converter can be observed in the following figures:

To better observe the behaviour of the system the active and reactive power is displayed for both sides of the converter.

It can be observed that the power reduces from the nominal value to zero, but with an increase in the initial step. This happens because the ramp which controls the speed of the wind turbine has a slope which decreases too fast for this system. For a practical implementation the slope has to be reduced in order to maintain the current inside specific limits. This strategy could not be applied in this simulation because of the problems mentioned at the beginning of this working condition.

The rest of the behaviour, positive reactive power, is the same as for the normal working situation.
The last important parameter for this simulation is the DC voltage. The behaviour of this parameter can be observed in Figure 54. A large increase can be observed at the beginning of the simulation, when the stopping procedure is enabled. This increase is quickly
compensated by the control and the DC voltage reaches a value close to the nominal one. The reference DC voltage is achieved when the system stops.

5.3. Starting the turbine

The procedure of starting the turbine from zero to nominal speed was simulated for 60 seconds. The reference value and actual value of the speed can be observed in Figure 55. A ramp is applied at the input as a reference for the speed in order to limit the rise of the current.
During the starting procedure the load torque provided by the wind turbine varies from a positive initial value to the nominal negative value as a function of the speed. This behaviour is caused by the Darreius wind turbine, which cannot be started only by the wind. This type of turbine needs to be started by the machine until a certain value of the speed is achieved. The load torque characteristic as a function of time is presented in in the following figure:

![Load Torque from Wind Turbine](image)

Figure 56. The wind turbine torque.

The behaviour of the current in the machine and grid side is displayed:

![The current in the machine side](image)

![The current in the grid side](image)

Figure 57. The current on both sides of the convertor.

Only one phase of the current is displayed for a better visualization of the process. It can be seen in the machine part that the current increases from zero to a certain value...
necessary to produce the electromagnetic torque which starts the turbine. The current increases in frequency as the rotational speed increases. In the first region the current is positive because the machine works as a motor, but changes sign once the load torque becomes negative, the machine becomes a generator. The current reaches its nominal value once the nominal speed is achieved, and the system enters steady state.

In the grid side of the converter it can be observed a different behaviour of the current. It starts from zero and goes to a maximum value smaller than the nominal value which is achieved at the middle of the starting period. The current also changes sign when the turbine starts rotating only by the influence of the wind, and power is transmitted into the grid.

The behaviour of the voltage in both sides of the converter is:

![Voltage Graph](image)

Figure 58. The voltage on both sides of the converter.

It can be seen that the voltage on the machine side increases in magnitude and frequency as the speed of the machine increases until the nominal value is reached. This is done by the machine control.

On the grid side the voltage is almost constant on the entire period, but with a smaller magnitude in the first part of the simulation when the machine works as a motor and power is taken from the grid. When the machine enters generator mode the voltage at the convertor terminals on the grid side increases to enable the power flow to the grid.

For a better visualization of the power flow direction the active and reactive power at the machine terminals is displayed in Figure 65. It can be seen that the machine starts as a motor in order to rotate the wind turbine to a specific value and the switch to generator mode is made once the load torque changes sign. The machine provides nominal power to the grid when the speed of the turbine reaches the nominal value.
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Figure 59. The active and reactive power at the machine terminals.

Figure 60. The active and reactive power at the grid terminals.

From the grid side active and reactive power it can be seen that the active power taken from the grid in order to start the turbine is equal to the active power on the machine side. The reactive power is negative on the entire time domain because the flow of reactive power is negative compared to the flow of energy.

The DC voltage is affected by this transient process, as it can be seen in Figure 61 but the control strategy is able to provide compensation in order to maintain the voltage at the reference value.
5.4. Voltage dip situation

In this situation the voltage of the grid is falling from the nominal value to 20% and increases back to 90% of the nominal value, as in the requirement presented in the grid codes [37]. In this situation the main priority is to supply reactive power to the grid in order to help the grid recover from this abnormal situation.
Because the voltage drop has a time span of only 4 seconds and the time constant of the mechanical circuit has a very big value the voltage dip is not observed on the machine side of the converter. As it can be seen in the following figure the speed of the machine is not affected by this fault.

Figure 63. The speed of the generator.

Also the current and the voltage are not affected by this fault on the machine type, the influence can be observed only on the grid side.

Figure 64. The current on both sides of the convertor.
Figure 65. The voltage on both sides of the convertor.

The stability of the machine side convertor can be observed also from the active and reactive power characteristic.

Figure 66. The active and reactive power in the machine sides of the system.

Here it can be observed that the active and reactive power do not change during the voltage drop in the grid. This is a requirement of the grid codes [37].
The main part of the control in this situation happens in the grid side of the convertor. Here the influence of the fault can be observed better.

Figure 67. The active and reactive power at the grid side converter terminals.

It can be observed that the active power is maintained almost constant during the entire period, the increase and decrease of the power taking place for very short periods. The reactive power increases from zero to a certain value which is determined by the control using the requirements presented in the grid codes.

Figure 68. The active and reactive power at the grid side converter terminals.
The complete behavior of the system can be better observed in the power which is transferred directly to the grid. This power is presented in the following figure:

![Figure 69. The active and reactive power transferred to the grid.](image)

From these characteristics we can observe that if a voltage drop such severs appears in the grid the convertor supplies only reactive power to the grid in order to help the grid.

Although this drastic phenomenon happens in the grid side converter the value of the DC voltage is maintained between acceptable limits and after a period of time it is brought back to the reference value, as it can be seen in Figure 70.

From these characteristics it can be seen that the system is able to handle a fault presented in the grid according to the grid requirements.
5.5. Normal working condition with the converter model

The simulation was made as in the previous situation, when the system is in steady state and the power flow is from the generator to the grid.

The shape of the current in this situation is presented in the following figure:
It can be seen that the waveforms are affected by perturbation once the model of the convertor has been introduced. The same result can be seen in the voltage waveform.

![The voltage at the machine terminals](image)

![The voltage at the grid terminals](image)

**Figure 72.** The voltage waveform on both sides of the convertor.

The problem that appears once the convertor is connected is related with the balancing of the voltages in the DC link. Because no balancing control strategy was applied to this part of the convertor the waveforms and the behaviour of the system is drastically affected. The difference of capacitor voltages in the DC link is displayed in the following figure:

![The difference between the capacitors voltage](image)

**Figure 73.** The difference between the capacitors voltages.
As it can be seen from the figure the voltage increases to dangerous values. In order to test the entire model with the convertor attached the strategy to control the voltage balance has to be implemented.

Once the convertor model is implemented the entire set of values which describes the model can be visualized, as for example the DC currents in the grid side and the machine side.

![Figure 74. The DC currents in the machine side of the convertor.](image_url1)

![Figure 75. The DC currents in the grid side of the convertor.](image_url2)
Chapter 6

Converter design

The objective of this chapter is to present the general idea how to design and calculate multilevel Neutral Point Clamped Converter.

In the design process the determination of the number of levels for the topology is one of the most crucial factors affecting the number of the devices in the circuit, their ratings and even the control techniques to be used for the converter. The minimum number of levels for the converter and the voltage ratings for the active devices are inversely related to each other. Higher converter level topology will require more active devices for the circuit but the voltage levels applied on the switches will be lower compared to a topology with fewer levels. However it should be considerate that unlike the active devices additional levels do not enable a decrease in the voltage rating for the clamping diodes [24], [38].

6.1. Define the system specifications

The first step is to define the system specifications for the converter, the utility grid to which it is going to be connected and the generator in our case the wind turbine and some additional information about the converter. The required parameters for the input and the output of the design program are summarized and shown in Figure 76 [38]:
6.2. DC Bus Voltage calculation

The first parameter for the converter to be determined is the DC Bus voltage for the DC link. The value of this voltage is closely related to the selection process of the semiconductor devices, active switches and capacitors in the circuit and is one of the main basic parameters for the converter [39].

The DC bus voltage is composed of two values that have to be defined the minimum DC voltage in the DC link \( U_{dc-min} \) and the max value for the DC voltage in the DC bus link \( U_{dc-max} \). Both of them are dependent on the AC output voltage level that we want to generate. It should be mentioned that in our project the input voltage level will be the same as the output AC voltage level of the converter and the NPC have the main function of control in our system [39].

The minimum dc-bus voltage to achieve a line to line voltage of given magnitude \( U_{out} \) using the PWM strategy is
The maximum dc-bus voltage is fixed around a value of

\[ U_{dc-min} = U_{out} \times \sqrt{2} \]  

Eq. 151

Where \( k \) is a coefficient between 1.5-2 it is chosen based on what kind of voltage level are presented in our system.

There are 2 main reasons for limiting the maximum DC-bus voltage in the converter

- In order to limit the minimum value of the amplitude modulation index
- In order to have a safety margin, with consideration to the nominal voltages of the components that are used under possible oscillations in the system

### 6.3. Calculation of the switching devices and free-wheeling diodes

In this step the voltage rating and the current for the switches used in the circuit (IGBT’s MOSFET etc.) and the free-wheeling diodes will be determined.

The voltage that these devices have to withstand as mentioned before is based on the level of the Neutral Point Clamped converters topology used. The voltage rating that each switch has to be able to withstand can be summarized in the following equation [39].

\[ V_{Rswitch} \geq \frac{U_{dc-max}}{m - 1} \]  

Eq. 153

Where “\( m \)” is the level of the NPC converter used.

For the free-wheeling diodes the same equations is valid and is going to be used.

\[ V_{Rf-diode} \geq \frac{U_{dc-max}}{m - 1} \]  

Eq. 154

Hence it can be seen that in the multilevel NPC converter topology the voltage that the switching devices have to be able to withstand is reduces starting by factor of 2 for the three level NPC converter topology and keeps increasing so forth as the number of levels for the converter increases [24], [39].

The current rating for the switches and the freewheeling diodes is given in the following equation. It should be noted that the level for the Neutral Point Clamped converter topology does not affect the current that this devices have to be able to withstand [39].
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\[ I_{\text{Rswitch}} \geq \frac{I_{\text{Base}}}{\sqrt{3}} \quad \text{Eq. 155} \]

\[ I_{\text{Rf-diode}} \geq \frac{I_{\text{Base}}}{\sqrt{3}} \quad \text{Eq. 156} \]

Where \( I_{\text{Base}} \) is the line to line current of the converter so basically the devices should be able to withstand the phase to phase current for the converter.

6.4. Calculation of the clamping diodes for the converter

Although each active switching device and the freewheeling diodes in an NPC converter are required to block voltage level of

\[ V \geq \frac{U_{\text{dc-max}}}{m - 1} \quad \text{Eq. 157} \]

The clamping diodes need to have different voltage rating for the reverse voltage blocking capabilities than the other semiconducting devices [28].

For example using Figure 12 of a 5 level NPC, when all off the lower switching devices S’a1 to S’a4 are switched on the clamping diode D’a1 is required to block three capacitor voltage levels. The highest voltage level that each clamping diode in an “m” level NPC converter will have to block can be summarized in the following equation [28].

\[ V_{\text{R-clamping}} \geq \frac{(m - 2) \times U_{\text{dc-max}}}{m - 1} \quad \text{Eq. 158} \]

\( m \)- Level of the NPC topology used

If we assume that each clamping diode has a voltage rating of the same value as the switches and the freewheeling diodes in the circuit the number of diodes required for each leg is:

\[ n_{\text{clamping-d}} \geq (m - 1) \times (m - 2) \quad \text{Eq. 159} \]

6.5. Calculation of the dc-bus capacitors

A critical part of the NPC converter is the design and calculation of the DC link capacitors. The calculation of the DC bus capacitor is closely related to the different types of
ripples that the converter should be able to withstand under all type of conditions. The capacitance required for the DC link and the voltage ripple in the converter are inversely related to each other. An increase in the capacitance will decrease the amount of ripple in the DC voltage \[39\], \[40\].

It is assumed that the capacitance value of each of the capacitors in the DC link of the Neutral Point Clamped Converter is equal.

\[
C_{dc-link} = C_{dc-1} = C_{dc-2} = C_{dc-3} = C_{dc-n}
\]

Eq. 160

The ripple types and the corresponding analytical expressions can be summarized as follows \[39\], \[40\] :

- Ripple of High Frequency Due to Commutation

\[
C_{dc} \geq \frac{T_{sw} \cdot S_n}{2 \cdot U_{dc-min} \cdot \Delta U_{dc}}
\]

Eq. 161

\( \Delta U_{dc} \) – Maximum allowed ripple. The maximum allowed voltage ripple is normally chosen to be in the range between 5% - 10% of the minimum DC bus voltage \( U_{dc-min} \)

\( T_{sw} \) – Commutation Frequency

\( S_n \) – Nominal Power of the converter

- Ripple of Twice the Utility Grid Frequency (Active Filter)

The worst situation takes place when it is necessary to balance a load of negative sequence to nominal. In these circumstances the ripple is twice the utility grid frequency and the capacitance should fulfill the requirement \[39\], \[40\]:

\[
C_{dc} \geq \frac{S_n}{2 \cdot \omega_{base} \cdot U_{dc-min} \cdot \Delta U_{dc}}
\]

Eq. 162

\( \omega_{base} \) – Base frequency of the converter

- Ripple of frequency equal to three times the modulation frequency

This ripple produces an unbalance voltage between the capacitor banks in the DC link bus and should be limited.

\[
C_{dc} \geq \frac{4 \cdot \sqrt{2} \cdot I_{base} \cdot T_{base}}{3 \cdot \sqrt{3} \cdot \pi^2 \cdot \Delta U_p}
\]

Eq. 163

\( I_{base} \) - Phase current of the converter
The unbalance voltage between the capacitor banks is considerate to 5% of $U_{dc-min}$.

The capacitance of each capacitor in the DC link should fulfill this requirement and its value should be higher than the biggest one for the given conditions. If these requirements are not fulfilled some of the following negative effects that affect the normal work of the converter will be observed [39], [40]:

- Possible overvoltage's in the power electronic devices and in the DC bus capacitors
- Worsening of the quality of the current that circulate for the load
- In extreme cases an inappropriate behavior of the converter
Chapter 7

Conclusions and future work

In this chapter the main conclusions for each part of the report are going to be presented along with the main directions that can be studied and implemented in the future, starting from the work that has been done so far.

7.1. Conclusions

System Modelling

All the components of the system were implemented in Matlab Simulink to test their behaviour. Each mathematical model was developed to simulate as best as possible the real system. During the development process simplifications were made to the mathematical model in order to reduce the complexity and to make the process faster.

From the results presented in the previous chapter it can be observed that each model provides relevant information, comparable with the practical component that it models. From this information we can conclude that the models are correctly implemented and the control strategies can be applied to them.

System Control

In order to implement the control, the converter was separated in two parts, the machine side converter and the grid side converter. For each part of the converter a different control strategy was implemented.

For the part of the converter placed on the machine side a field oriented control was applied, where the current and the speed of the machine are controlled.

For the part of the converter placed on the grid side a current control was applied in order to maintain unity power factor for the power transmitted to the grid. A DC voltage control was also implemented to maintain the DC voltage level in the DC link to a constant value. The last control was made for the reactive power, which has to be controlled in fault situations as voltage dip.
The control implemented on the converter has provided acceptable results for the model as it can be observed from the results presented in the previous chapter.

The system is efficiently controlled in different working situations as starting the turbine, stopping the turbine and grid faults, as well as in normal working situation, when the entire process is in steady state operation.

**Converter design program**

The presented converter design program offers the basic concept for calculation of a multilevel NPC converter. The output results from the program include the level of the topology needed to implement the NPC converter, the quantity and the ratings for the semiconductor devices and DC link values for the capacitors based on the user input specifications. Values regarding the losses in the components and the efficiency of the converter are also calculated and presented in the output.

The results obtained are only theoretical, they have not been verified with real data in order to proof if they are correct or not.

**7.2. Future Work**

**System Modelling**

In order to obtain results closer to the practical system the mathematical models have to be made with a more increase degree of complexity that can cover a larger number of phenomenon’s present appear in the real system.

The grid model can be implemented with the connection switch in order to be able to simulate the grid connection procedure and to implement the control for this procedure.

The Darreius wind turbine presents a different behaviour from the normal wind turbines which are already modelled in the literature, which make this topology interesting for further study and modelling.

**System Control**

Because the control presented in this project has proven to work in the simulation a next step will be to implement it in a practical system in order to validate its behaviour. All the control system presented is in continuous time all the components are considered ideal. The next step regarding this is to discretize the control system and to implement PWM modulators.

More control strategies have to be implemented for the real system as: voltage balancing control and control for different fault situations.

**Converter design program**

Future work regarding the converter design should include more detailed component selection including bigger library for the semiconductors and additional components such as gate drives.
An important step to be carried out is to verify the data provided by the software with real applications in order to prove if they are correct or not.

Thermal design including transient and steady state models thermal models should be implemented and also the program should be able to propose different cooling techniques and heat sink selection based on the obtained results.
References


37. Energinet.dk. (1-30 September 2010). *Technical regulation 3.2.5 for wind power plants with a power output greater than 11 kW* [Online]. available:
http://www.energinet.dk/SiteCollectionDocuments/Engelske%20dokumenter/El/55986-10_v1_Grid%20Code%203%202%205_v%204%201-30%20%20September%202010.pdf.

38. Hang-Seok Choi. *Application Note AN4137*<br />


40. Emilio J. Bueno, Santiago Cobreces, Francisco J. Rodriguez, Felipe Espinosa, Marta Alonso, Raul Alcaraz, "Calculation of the DC-bus capacitors of the backto to back NPC converters."
Appendix A

Converter design program

%%% A help file is presented with all of the used variables as an addition

%%% Input values for the Converter
% In this part the user has to introduce the design variables for the converter;

Sinput=5e3;
% input Power of the converter

Vllinput=12000;
% input Voltage level of the converter

Iphase=Sinput/(sqrt(3)*Vllinput);
% phase current of the converter

fsw=1000;
% commutation period

Tsw=1/fsw;
% commutation frequency

fgrid=50;
% grid frequency

Wbase=2*pi*fgrid;
% base frequency of the converter

ton=0.17e-4;
% diode on time

toff=0.13e-4;
% diode off time

Tbase=1/fgrid;

%%% IGBT Selection

%IGBT 1 - Vigbt=1700 V; Iigbt=1600 A;
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% IGBT 2 - Vigbt=3300 V; Iigbt=1500 A;
% IGBT 3 - Vigbt=4500 V; Iigbt=1200 A;
% IGBT 4 - Vigbt=6500 V; Iigbt=750 A;
selectIGBT=4;

[Vigbt, Iigbt, Eon, Eoff, Rcc, Vce]=IGBT(selectIGBT);

if Iigbt<Iphase
    disp('The IGBT selected cannot withstand the current;')
end

% Diode Selection

% Diode 1 - Vdiode=275 A; Vdiode=4500V;
% Diode 2 - Vdiode=1100 A; Vdiode=4500V;
% Diode 3 - Vdiode=1650 A; Vdiode=4500V;
% Diode 4 - Vdiode=2750 A; Vdiode=4500V;
selectDiode=4;

[Vdiode, Idiode, Vfd, Ir]=Diode(selectDiode);

if Idiode<Iphase
    disp('The selected diode cannot withstand the current;')
end

% DC-bus Voltage level calculation
% The minimum and the maximum DC voltage of the converter is computed;

k=1.5; % coefficient for the DC bus max voltage 1.5 - 2
Vdcmin=Vllinput*sqrt(2); % minimum dc-bus voltage level
Vdcmax=Vllinput*k; % maximum dc-bus voltage level

% Converter Level Determination
convLevelIGBT=ceil(Vdcmax/Vigbt)+1;
convLevelDiode=ceil(Vdcmax/Vdiode)+1;

convLevel=max(convLevelIGBT,convLevelDiode);
disp(['The convertor need to have at least ',num2str(convLevel),',
levels.'])

% Number of components for the convertor determination

ClmapingDiodes=6*(convLevel-1)*(convLevel-2);
disp(['The convertor will have ',num2str(ClmapingDiodes),',
clamping diodes.'])

igbts=12*(convLevel-1);
freewhdiodes=igbts;

disp(['The convertor will have ',num2str(igbts),', IGBTs.'])
disp(['The convertor will have ',num2str(freewhdiodes),', Free-wheeling diodes.'])

% Capacitor Selection
% In this part of the program the value for the capacitor si selected;

\[ \text{deltaVdc} = 0.1 \times V_{dcmin}; \]
\[ \text{deltaVdc} = \text{maximum allowed ripple} \]
\[ \text{deltaVp} = \frac{\text{deltaVdc}}{2}; \]
\[ C_{dc1} = \frac{(T_{sw} \times S_{input})}{2 \times \text{deltaVdc} \times V_{dcmin}}; \]
\[ \text{Ripple of High frequency due to the commutation} \]
\[ C_{dc2} = \frac{S_{input}}{2 \times W_{base} \times \text{deltaVdc} \times V_{dcmin}}; \]
\[ \text{Ripple of Twice the utility grid frequency} \]
\[ C_{dc3} = \frac{4 \times \sqrt{2} \times I_{phase} \times T_{base}}{3 \times \pi^3 \times \text{deltaVp}}; \]
\[ \text{Ripple of frequency equal to three times modulation frequency} \]
\[ C_{dc} = \max(C_{dc1}, \max(C_{dc2}, C_{dc3})); \]
\[ \text{Capnumber} = \text{convLevel} - 1; \]

\[
\text{disp(['The capacitor should have at least ',num2str(Cdc),' F capacitance.'])}
\]
\[
\text{disp(['The convertor will have ',num2str(Capnumber),' Capacitors.'])}
\]

%% Power Losses Determination

% Power losses for the IGBT's

\[ V_f = V_{ce} + R_{cc} \times I_{phase}; \]
\[ P_{cond} = I_{phase} \times V_f \times 0.5; \]
\[ \text{Conduction losses} \]
\[ P_{switch} = (E_{on} + E_{off}) \times T_{sw}; \]
\[ \text{Switching losses} \]
\[ \text{ibgtlosses} = (P_{switch} + P_{cond}) \times \text{igbts}; \]
\[ \text{disp(['The losses for IGBTs are ',num2str(ibgtlosses),' watts.'])} \]

% Power losses for the Diodes

\[ P_{conddiode} = V_{fd} \times I_{phase} \times t_{on} / T_{sw}; \]
\[ \text{Diode Conduction losses} \]
\[ P_{off} = I_r \times V_{dcmax} \times t_{off} / T_{sw}; \]
\[ \text{Diode off-state losses} \]
\[ \text{Diodelosses} = (P_{conddiode} + P_{off}) \times (C_{mappingDiodes} + freewhdiodes); \]
\[ \text{disp(['The losses for the Diodes are ',num2str(Diodelosses),' watts.'])} \]

%%Converter efficiency

\[ \text{eff} = (S_{input} - (\text{ibgtlosses} + \text{Diodelosses})) \times 100 / S_{input}; \]
\[ \text{disp(['The Efficiency of the converter is ',num2str(eff),' %.'])} \]
Semiconductors used in the design program

The switching devices selected for the design program are IGBT’s from the ABB manufacture. The codes of the devices with the voltage and current rating are presented in the following table.

<table>
<thead>
<tr>
<th>IGBT’s used for the converter design program</th>
<th>Code of the device</th>
<th>Voltage rating</th>
<th>Current rating</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5SNA 1600N170100</td>
<td>1700</td>
<td>1600</td>
</tr>
<tr>
<td></td>
<td>5SNA 1500E330305</td>
<td>3300</td>
<td>1500</td>
</tr>
<tr>
<td></td>
<td>5SNA 1200G450350</td>
<td>4500</td>
<td>1200</td>
</tr>
<tr>
<td></td>
<td>5SNA 0750G650300</td>
<td>6500</td>
<td>750</td>
</tr>
</tbody>
</table>

The diodes selected for the design program are also from the ABB manufacture. The main parameters for the diodes the reverse voltage rating and the current rating of the devices are presented in the following table.

<table>
<thead>
<tr>
<th>Diodes used for the converter design program</th>
<th>Code of the device</th>
<th>Voltage rating</th>
<th>Current rating</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5SDF 03D4502</td>
<td>4500</td>
<td>275</td>
</tr>
<tr>
<td></td>
<td>5SDF 10H4503</td>
<td>4500</td>
<td>1100</td>
</tr>
<tr>
<td></td>
<td>5SDF 16L4503</td>
<td>4500</td>
<td>1650</td>
</tr>
<tr>
<td></td>
<td>5SDF 28L4520</td>
<td>4500</td>
<td>2620</td>
</tr>
</tbody>
</table>
This report addresses the development of a multi-level inverter suitable for the grid side DeepWind converter. Two level inverters are known to generate Common Mode Voltage (CMV) in the machine windings, causing machine failures due to bearing currents. Furthermore, a leakage current will flow through the stator windings and motor frame creating common mode electromagnetic interference. Taking these problems into consideration and the fact that the multilevel inverters offer better Total Harmonic Distortion (THD) as well as the possibility to reduce the CMV by selecting a suitable modulation strategy, they became a point of interest. In addition, multi-level inverters offer the possibility of developing high voltage units without placing extra voltage stress on the semiconductor switches. Compared to higher level topologies, a good ratio between complexity and performance is offered by the three-level topology. As this type of inverter synthesises the output voltage from series connected DC link capacitors, problems such as neutral point balancing might appear, causing voltage stress on the semiconductors.

The aim of this project is to develop modulation strategies that address both DC link voltage balancing and CMV reduction.

Four modulation strategies that address these problems were developed and validated through simulation. In order to experimentally validate them, a small scale Neutral Point Clamped (NPC) inverter was designed, built and tested. Analysis was performed on each developed modulation, of the CMV and Electromagnetic Interference (EMI) and neutral point balance assessment. The authors conclude that all proposed strategies offer better CMV and EMI spectrum compared with classical NTV and ZCM.

Authors: Daniela Boian, Ciprian Biris
Development of Modulation Strategies for NPC Inverter Addressing DC Link Balancing and CMV Reduction
Title: Development of Modulation Strategies for NPC Inverter Addressing DC Link Balancing and CMV Reduction

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Semester theme: Master Thesis
Project period: 01.09.2011 to 31.05.2012
ECTS: 60
Supervisors: Remus Teodorescu
            Michal Sztykiel
Project group: PED1041

SYNOPSIS:

Two level inverters generate Common Mode Voltage (CMV) in the motor windings, causing motor failures due to bearing currents. Furthermore, a leakage current will flow throughout the stator windings and motor frame creating common mode electromagnetic interference. Taking these problems into consideration and the fact that the multilevel inverters offer better Total Harmonic Distortion (THD) as well as the possibility to reduce the CMV by modulation strategy, they became a point of interest. Compared to higher level topologies, a good ratio between complexity and performance is offered by the three-level topology. As this type of inverter synthesises the output voltage from series connected DC link capacitors, problems such as neutral point balancing might appear, causing voltage stress on the semiconductors.

The aim of this project is to develop modulation strategies that address both DC link voltage balancing and CMV reduction.

Four modulation strategies that address these problems were developed and validated through simulation. Furthermore, in order to experimentally validate them, a Neutral Point Clamped (NPC) inverter was designed and built. Analysis, regarding CMV and Electromagnetic Interference (EMI) together with neutral point balance assessment, was performed on each developed modulation which concluded that all proposed strategies offer better CMV and EMI spectrum compared with classical NTV and ZCM.

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Ciprian Biris

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Appendix: [ 11 ]
Supplements: [ 1 CD ]

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.
Preface

The Master in Science thesis was carried out during 9th and 10th semester at Aalborg University in the Department of Energy Technology starting from 1st of September 2011 until 31st of May 2012. The project “Modulation of three-level inverter with common-mode voltage elimination and DC-link balancing” was chosen by the authors from the Vestas catalogue containing proposals for students from Energy Technology department.

Acknowledgments

The authors would like to thank their supervisors: Remus Teodorescu, Michal Sztykiel and Osman Selcuk Senturk for their guidance during the master thesis.

They would like to give special thanks to Stig Munk-Nielsen, Carsten Karup Nielsen and Laszlo Mathe for their help during inverter design, as well as to Adrian Hasmasan and Ram Krishan Maheshwari.

More thanks goes to Anamaria Man for her moral support as well as to Krisztina Leban.

The authors would like to give thanks to Vestas for the financial support during the two years of Master in Science.

The Master in Science Thesis was conducted by:

Daniela Boian

Ciprian Biris

_________________________  ______________________

[III]
Summary

As well known the two-level topology generates CMV in the motor windings furthermore causing motor failures due to bearing currents. As there are parasitic capacitive couplings between the stator windings and the motor frame a common mode leakage current will flow, hence there will be common mode electromagnetic interference. Taking these problems into consideration, multilevel inverters have gained interest. These types of inverters offer lower THD in the phase-to-phase voltage as well as the possibility to reduce the CMV through modulation strategy. As the phase-to-phase waveform is produced form series connected capacitors an unbalance may appear causing voltage stress on the IGBTs.

Solutions to reduce the common mode voltage and to balance the DC link through modulation strategies have been studied in this project due to their cost effectiveness.

This thesis is structured in six chapters and has ten appendixes. The background of the three-level NPC inverter together with the problem formulation regarding CMV and DC link balance is presented in the first chapter. Furthermore, the study and development of new and improved modulation strategies as well as the hardware design represent the objectives. Also, project limitations are stated.

Chapter two is focused on the NPC inverter topology and its background. Further in this chapter space vector modulation and switching states make an introduction for the classical modulation strategies studied: Nearest Three Vectors with Even Harmonic Elimination (NTV-EHE) and Zero Common Mode (ZCM). Also the DC link balancing problem and mitigation for NPC converters is studied as well as CMV and its mechanism together with its effects. The end of second chapter presents the methods for measuring the CMV and EMI.

The new proposed modulation strategies are presented in the third chapter. The theoretical basics together with the validation through simulations are part of the acknowledgement of these strategies. The chapter ends with a comparative evaluation of the developed strategies compared with the classical ones.

The fourth chapter is dedicated entirely to hardware design. A NPC inverter was built featuring reduced size, snubberless design due to newly introduced NPC leg Insulated Gate Bipolar Transistor (IGBT) modules, protections, RS-232 and CAN communications and mixed analogue and digital design. The overview of the developed platform is made after which, the sizing and implementation of the DC link is described, IGBT modules, gate drivers, microcontroller and protections. The thermal cooling solution is presented together with its validation through thermal imaging. This chapter ends with an overview of the implemented control on the Digital Signal Processor (DSP) and Complex Programmable Logic Device (CPLD) is followed by hardware validation tests.

The experimental validation and analysis of the developed modulation strategies is the main focus of chapter 5. The results and waveforms of the new strategies as well as the classical ones are presented and analysed together with the DC link balancing capability assessment and CMV evaluation. The chapter is ended with results regarding the conductive EMI produced by these strategies.

The last chapter presents conclusions regarding the results of CMV, DC link balancing and conductive EMI of the developed modulation strategies, in comparison with classical ones.
Furthermore, the appendixes are included as follows:

- Appendix 1: Project Proposal
- Appendix 2:
- Appendix 3: Experimental Setup Data
- Appendix 4: CPLD/DSP Pin Assignment
- Appendix 5: CPLD Functional Schematic
- Appendix 6: PCB Photos
- Appendix 7: PCB Layers
- Appendix 8: Electrical Schematic
- Appendix 9: Bill of Materials
- Appendix 10: Paper
- Appendix 11: Contents of the CD

Contributions

This project brings the following contributions:

- NPC inverter design with NPC leg IGBT modules
  - Reduced size
  - RS-232, RS485 and CAN communication
  - Software and hardware protections
  - Snubberless design
  - Embedded DSP
- Modulation Strategies that address both DC link balancing problem and CMV reduction

During this project a paper has been written. This paper has been accepted in the IEEE PEDG conference held in Aalborg, Denmark in June 2012. This paper can be seen in Appendix 10.

- Daniela Boian, Ciprian Biris, Remus Teodorescu, Michal Sztykiel, “Development of Modulation Strategies for NPC Converter Addressing DC Link Voltage Balancing and CMV Reduction”
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full form</th>
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<tbody>
<tr>
<td>AC</td>
<td>Alternative Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analogue to Digital Converter</td>
</tr>
<tr>
<td>ASD</td>
<td>Adjustable Speed Drive</td>
</tr>
<tr>
<td>CAL</td>
<td>Controlled Axial Lifetime</td>
</tr>
<tr>
<td>CAN</td>
<td>Controller Area Network</td>
</tr>
<tr>
<td>CM</td>
<td>Common Mode</td>
</tr>
<tr>
<td>CMC</td>
<td>Common Mode Current</td>
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<tr>
<td>CMR</td>
<td>Common Mode Rejection</td>
</tr>
<tr>
<td>CMV</td>
<td>Common Mode Voltage</td>
</tr>
<tr>
<td>CPLD</td>
<td>Complex Programmable Logic Device</td>
</tr>
<tr>
<td>CSI</td>
<td>Current Source Inverter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCB</td>
<td>Direct Copper Bonded</td>
</tr>
<tr>
<td>DMOS</td>
<td>Double Diffused Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>EDM</td>
<td>Electric Discharge Machine</td>
</tr>
<tr>
<td>EHE</td>
<td>Even Harmonic Elimination</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ePWM</td>
<td>enhanced Pulse Width Modulator</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transformation</td>
</tr>
<tr>
<td>FLC</td>
<td>Flying Capacitor</td>
</tr>
<tr>
<td>FLIR</td>
<td>Forward Looking Infra-Red</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input Output</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>HV</td>
<td>High Voltage</td>
</tr>
<tr>
<td>HVDC</td>
<td>High Voltage DC</td>
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<tr>
<td>I/O</td>
<td>Input/ Output</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>ISR</td>
<td>Interrupt Service Routine</td>
</tr>
<tr>
<td>LCI</td>
<td>Load Commutated Inverter</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
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<tr>
<td>LISN</td>
<td>Line Impedance Stabilisation Network</td>
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<tr>
<td>NP</td>
<td>Neutral Point</td>
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<tr>
<td>NPC</td>
<td>Neutral Point Clamped</td>
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<tr>
<td>NPT</td>
<td>Non Punch Through</td>
</tr>
<tr>
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<td>Negative Temperature Coefficient</td>
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<td>Nearest Three Vectors</td>
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<tr>
<td>NTV-EHE</td>
<td>NTV with Even Harmonic Elimination</td>
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<tr>
<td>OLOM</td>
<td>One Large One Medium</td>
</tr>
<tr>
<td>OSOM</td>
<td>One Small One Medium</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
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<tr>
<td>PWD</td>
<td>Pulse Width Distortion</td>
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[VII]
<table>
<thead>
<tr>
<th>Abbr</th>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RC</td>
<td>Resistive - Capacitive</td>
</tr>
<tr>
<td>RCD</td>
<td>Random Centre Distribution</td>
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<tr>
<td>RL</td>
<td>Resistive - Inductive</td>
</tr>
<tr>
<td>RLL</td>
<td>Random Lead-Lag</td>
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<tr>
<td>RMS</td>
<td>Root Mean Square</td>
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<tr>
<td>RS3N</td>
<td>Random Sequence of 3 with Neutral Balancing</td>
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<tr>
<td>RZD</td>
<td>Random Zero Distribution</td>
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<tr>
<td>SARAM</td>
<td>Single Access RAM</td>
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<tr>
<td>SHE</td>
<td>Selective Harmonic Elimination</td>
</tr>
<tr>
<td>SOIC</td>
<td>Small Outline Integrated Circuit</td>
</tr>
<tr>
<td>SVM</td>
<td>Space Vector Modulation</td>
</tr>
<tr>
<td>TBCTR</td>
<td>Time Based Counter</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>TNPC</td>
<td>Type Neutral Point Clamped</td>
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<tr>
<td>UVLO</td>
<td>Under Voltage Lock-Out</td>
</tr>
<tr>
<td>V/f</td>
<td>Volt/hertz</td>
</tr>
<tr>
<td>VSI</td>
<td>Voltage Source Inverter</td>
</tr>
<tr>
<td>ZCM</td>
<td>Zero Common Mode</td>
</tr>
<tr>
<td>ZSML</td>
<td>Zero Small Medium Large</td>
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1. Introduction

This chapter introduces the problems that appear in Adjustable Speed Drives (ASD) - which affect both the inverter and motor, as well as presenting advantages and disadvantages for the three-level NPC inverter. Furthermore, problem formulation, motivation, objectives and limitations are stated.

1.1. Background

A widely discussed subject is the one of saving energy. Electrical motors are widely used to generate motion from electrical energy [1]. Industrial and domestic applications use electric motors with a large variety of power ratings. In most countries, electric motors use approximately 70% of the produced electric energy [2]. In the past, DC machines were used due to their simplicity in speed control. Nevertheless, these types of machines compared with AC ones, have some disadvantages such as higher cost, higher rotor inertia and maintenance issues with the brushes. Due to these problems, DC machines have been progressively replaced by AC machines. These types of machines cannot be efficiently controlled with direct connection to the grid, thus ASD for control of the magnitude and frequency of the output voltage are needed. These types of drives have a large scale of utilization in industrial applications. Due to the development of adjustable drives, the reliance in three phase AC motors has increased [1]. As a consequence of the rotor simplicity, induction motors have allowed solutions with lower cost [3].

As most applications require variable speed. Its principle is to convert the constant AC voltage into a variable one with the purpose of controlling the speed of the AC motor. A typical structure can be seen in Figure 1-1.

The Pulse Width Modulation (PWM) inverter needs to synthesise the input voltage in order to obtain the desired variable output voltage with a corresponding pulse shape sinusoidal.

[1]
Chapter 1 - Introduction

When long cables are required in order to connect the inverter to the motor, a LC filter is used [3]. The variation in time has to be taken into account as it is dependent on the rise and fall time of the switching device that might lead to stress at the motor terminals.

Adjustable speed drives can be classified based on the inverter topologies according to [4]:

- Voltage Source Inverter (VSI) drives: have a constant DC link voltage. The DC link capacitors are used in order to supply reactive power to the motor and to smooth the DC link voltage.
- Multi-level Voltage Source Inverter drives: uses series connected low voltage IGBTs.
- Current Source Inverter (CSI) drives: makes use of DC link current.
- Load Commutated Inverter (LCI) drives: takes part of the CSI. This type of drive store energy in the DC link inductor in order to supply quasi-sinusoidal current.
- Cycloconverter: does not have the ability to store energy in the DC link. Each phase of the Cycloconverter modifies the fixed line AC voltage into an alternating voltage at a variable load frequency.
- Cascade drives: makes use of a three phase diode rectifier that operates at slip frequency and feeds back the power to the supply network through a reactor and line commutated inverter. The motor speed is controlled by the DC current.

Nowadays, the need to increase efficiency and reduce production cost is the most discussed subject. This can be achieved by increasing the size and power of all electrical drives and equipment. The power increase can be done in two ways [5]:

- Developing High Voltage (HV) semiconductors with increased voltage blocking capabilities
- Development of multilevel inverters

The dominant topology for low voltage is two-level VSI. At medium and high voltage there are a variety of topologies. In high voltage, it is possible to use direct converters (cyclo-converters) and indirect converters (with current or voltage in DC link). Figure 1-2 presents the structure for high power converters [5].

![Diagram of high power converters](image)

Figure 1-2 – Family of High – Power Converters [5]

[2]
Chapter 1 - Introduction

The type of inverter used in this project is NPC Converter with the schematic from Figure 1-3. As it can be seen, this inverter has the neutral point clamped to the midpoint of the DC link. This configuration uses series IGBTs, thus the stress on the devices is reduced. Furthermore, the NP is used in order to generate at the inverter output three levels of voltage: \( \frac{V_{DC}}{2}, 0, -\frac{V_{DC}}{2} \), based on commutation of the twelve switching devices. The combination of these semiconductors allows 27 switching vectors.

Figure 1-3 – Three-Level NPC Converter Schematic

A three phase inverter provides leg voltages \((V_{a0}, V_{b0}, V_{c0})\), phase voltages \((V_{an}, V_{bn}, V_{cn})\) and phase-to-phase voltages \((V_{ab}, V_{bc}, V_{ca})\). Aside from these voltages, another one appears between the neutral point of the motor and the neutral point of the inverter, acknowledged as common mode voltage (CMV). This voltage can be calculated based on the influence of each switching vector; however the general formula for calculating CMV is presented in [6] and can be seen in equation (1-1).

\[
V_{N0} = \frac{V_{a0} + V_{b0} + V_{c0}}{3}
\]  

(1-1)

Based on equation (1-1) it can be noticed that the CMV is created by the switching pattern on each device, thus this voltage can be reduced by using appropriate switching patterns.

The effect of high frequency PWM voltage is generally neglected in the electromagnetic performance of the induction motor. From the motor point of view it needs to be said that there exist small capacitive couplings, however they can be neglected in low frequency analysis. At high frequencies, a low impedance path is created and current flows through the capacitive couplings. As a consequence of high dv/dt applied to the motor, high frequency leakage currents flow through the capacitive couplings created between the stator winding and motor frame. Furthermore, as the motor frame is connected to the ground the high frequency currents may cause electromagnetic interference (EMI) [7].

As the semiconductors are improved the switching speed increases making the effect of capacitive couplings to be dominant. Considering this, two important parasitic capacitances can be observed: the one between stator winding – stator iron and stator winding – rotor iron [8]. These capacitances in interaction with CMV

[3]
and high \( \frac{dv}{dt} \) can cause shaft voltage, leading to bearing currents, and leakage currents, which further lead to noise and EMI, in the induction motor [3].

The main problems in ASD are CMV and high \( \frac{dv}{dt} \). The two problems cause issues such as [3]:

- Grounding currents – circulating between the parasitic capacitance inside the motor and ground
- Shaft voltages – that result in bearing currents
- Conductive and radiated noise
- Overvoltage at motor terminals

There have been developed multiple techniques with the purpose of reducing or eliminating the shaft voltage and CMV. The PWM techniques based can be summarised according to [3] as:

- Bearing current reduction methods
- Leakage current mitigation techniques

Three level inverters present advantages such as reduced voltage ratings for the semiconductors, good harmonic spectrum and good dynamic response, that makes them very popular. As disadvantage they have is increased control complexity over conventional VSI [9].

### 1.2. Problem Formulation and Motivation

When referring to three-level Voltage Source Inverters (VSI) it needs to be mentioned that since their invention they have been considered to be used in high capacity, high performance AC drives applications [10]. Taking this into account this thesis focuses mainly on the ASD application.

ASD are often used in industrial and household applications, like ventilation system, pumps and electric drives for machine tools. The output speed can be modified through magnitude and frequency of the output voltage by means of PWM [3].

Common Mode Voltage (CMV) is defined as the voltage between the neutral point of the inverter and neutral of the wye connected load, and it is generated by the PWM strategies. This type of voltage creates important problems in high switching frequencies. The techniques regarding attenuation of high frequency problems in AC motor drives systems have at base the reduction of CMV. This voltage has a very important influence over the shaft voltage. One important solution for reducing the shaft voltage and leakage current is the reduction of CMV. This can be achieved using two methods [3]:

- Attenuation of the shaft voltage through motor design
- CMV attenuation through PWM strategy
Further on, in low frequency analysis these capacitances can be neglected due to their small values, but their effects become important when the switching frequency of the converter is increased as the switching devices are improved. These capacitances offer a flow path for high frequency currents.

One important problem discovered in three – level NPC converter is the balancing of the DC link Neutral Point (NP). This type of inverter is exposed to problems like fluctuations in the NP due to irregular and unpredictable charging and discharging of the upper and lower DC link capacitors \[10\]. As it is defined in literature \[10\], there is an unbalance regarding the charging and discharging in each capacitor, thus the voltage across the capacitor may rise or fall and the NP voltage will not be able to maintain half of the DC link voltage. Due to this problem a high voltage may be applied to the semiconductors or DC link capacitors causing damage. This can be solved through three methods:

- Separate DC sources \[11\]
- Voltage regulators for each level using an additional small leg \[12\]
- Modified PWM pattern and voltage vector selection \[11\] \[13\]

The main focus of the thesis is to reduce the CMV and to balance the DC link voltage through appropriate PWM strategies due to their cost effectiveness.

### 1.3. Objectives

The following objectives have to be addressed according to Appendix 1: Project Proposal.

- Development of modulation strategies that address DC link balancing and CMV reduction
  - Study of classical modulation strategies
  - Study of DC link unbalance and CMV
  - Development of simulation model to test different modulation strategies before experimental implementation
  - CMV Analysis
  - Analysis of DC link unbalance
- Hardware design of the three-level NPC inverter
  - Study of NPC converter
  - DSP implementation of the modulation strategy for the three level converter
  - Comparison of the emitted common mode EMI from conventional modulations and the developed ones
  - CMV Analysis
  - Analysis of DC link unbalance
1.4. Project Limitations

During the development of this project some limitations had to be imposed, due to limited time and/or resources. The main limitations are:

- Only conducted EMI up to 20 MHz – radiated EMI requires special chamber and equipment
- Current <16 A – for analysing the developed modulation strategies this current is enough
- Application – The developed methods are tested only for induction motor adjustable speed drives
- DC link voltage, \( V_{DC} = 600 \, V \) – for analysis purposes and due to the fact that most wye connected induction motors available in the Aalborg University laboratories have the rated voltage of 380 – 420 V. Hence, the DC link has to be large enough in order to produce the rated voltage: \( V_{DC} = \sqrt{2} \times V_L = \sqrt{2} \times 420 = 593.94 \approx 600 \, V \).
2. Neutral Point Clamped Converter

This chapter begins with the general theory regarding the three-level NPC inverter, followed by an introduction into SVM and theory concerning classical modulation strategies. A general simulation structure was developed. Simulation results are presented for further comparison with the proposed modulation strategies. The problems that need to be addressed in this project, DC link balancing and CMV reduction are presented.

2.1. Background of NPC

In the last few years interest in multilevel converters has increased. Different topologies for utility grid and drives have been studied among years. The ability to synthesise waveforms with the improvement in harmonic spectrum and acquirement of higher voltages with a limited maximum device rating made three level inverters suitable for high voltage and high power applications [14].

The oldest topology of three level inverters was introduced by Nabae in 1981 [11], the neutral point clamped topology. The layout of three level diode – clamped inverter is also called three – level NPC inverter. Compared with two level voltage source inverters this topology has better spectral performance. Multilevel inverters reduce voltage stress on the devices. Bhagwat and Stefanovic improved the spectral structure of output waveforms in multilevel inverters. The original topology with the neutral point clamped has been expanded to higher number of levels. The required voltage blocking capability of the clamping diodes varies with the levels, thus multiple diodes at higher levels may be required [14].

According to [15] a general comparison between two level and three level inverter can be done. This is presented in Table 2-1.

<table>
<thead>
<tr>
<th></th>
<th>Two Level</th>
<th>Three Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver</td>
<td>Better</td>
<td>Worst</td>
</tr>
<tr>
<td>PWM Algorithms</td>
<td>Better</td>
<td>Worst</td>
</tr>
<tr>
<td>DC Link</td>
<td>No difference</td>
<td>No difference</td>
</tr>
<tr>
<td>Output Filters</td>
<td>Worst</td>
<td>Much better</td>
</tr>
<tr>
<td>THD</td>
<td>Worst</td>
<td>Much better</td>
</tr>
<tr>
<td>Current Ripple Losses</td>
<td>Worst</td>
<td>Much better</td>
</tr>
<tr>
<td>IGBT Voltage</td>
<td>$V_{DC}$</td>
<td>$\frac{V_{DC}}{2}$</td>
</tr>
<tr>
<td>Losses (switching/conduction)</td>
<td>Much worst</td>
<td>Much better</td>
</tr>
</tbody>
</table>
Multilevel converters supply ingenious methods of series connection of the switches, therefore enabling the processing of voltages that are higher than the device ratings. These converters are effective by means of reduction of harmonic distortion and dv/dt output voltage, thus making the devices useful for utility interface and drives [16]. One of the major disadvantages in multilevel inverters is the voltage unbalance between different levels. The output voltage of a three level inverter is a quasi-sinusoidal waveform [17].

Problems created by common mode voltages are encountered in conventional two level drives. These voltages are responsible for the shaft voltages and bearing failures, thus both need to be eliminated or reduced within certain bounds. Four leg inverters, passive filters, passive elements with active circuitry and dual bridge inverters have been investigated for reduction of common mode voltages [3].

Multi-level inverters can be divided into three main categories based on their topology [9]:

- Neutral Point Clamped (NPC)
- Flying Capacitor (FLC)
- H – Bridge

By means of PWM, quasi-sinusoidal waveform can be obtained at the output of the inverter. In order to have a high quality waveform, filtering and high switching frequency is required. Flexibility can be obtained by splitting the DC link voltage in two equal sources [18]. Now the output can have the voltage levels: 0 and $\pm \frac{V_{dc}}{2}$. This configuration can be seen in Figure 2-1:

![Figure 2-1 – General Inverter Leg](image)

The idea can be expanded in order to obtain a generalized three level inverter that can be seen in Figure 2-2. In order to raise the blocking capacity of conventional two level inverters the switching devices are connected in series. Fast switching devices connected in series that switch simultaneous will generate a high dv/dt at the output terminal of the inverter. The short rise time of the output of the inverter correlated with a long cable is potentially hazardous for the insulation of a motor and for the cable due to the fact that high dv/dt generates partial discharges and as a result the aging of the insulation is accelerated. This phenomenon appears in the motor as leakage current. In motor drives this current leads to electromagnetic
interference noise, thus causing trip of the inverter, problems with the protections of the supply transformer and interference with electronic equipment from the vicinity [2].

![General Three Level Inverter](image)

The switching states can be described using three variables in order to show where each phase leg is connected. The variables are: \( m_0 \) for connection to neutral point, \( m_- \) for connection to the negative bus and \( m_+ \) for connection to the positive bus. These variables are Boolean. Only one of the variables can be on high state for each leg. This property can be written as in equation (2-1):

\[
\begin{align*}
m_0 + m_+ + m_- &= 1 \\
\text{(2-1)}
\end{align*}
\]

If the voltages on the DC link capacitors are equal, \( E_1 = E_2 \) and \( x \) is one of the three phases of the load then the leg voltage of the inverter can be written as in equation (2-2):

\[
\begin{align*}
V_{x0} &= m_x^+ - m_x^- \\
\text{(2-2)}
\end{align*}
\]

This results in three possible phase voltages: \( \frac{V_{DC}}{2} \), \( -\frac{V_{DC}}{2} \) and 0. If \( x \) and \( y \) are two different phases, the phase to phase voltage can be written as in equation (2-3):

\[
\begin{align*}
V_{xy} &= V_{x0} - V_{y0} = \frac{V_{DC}}{2} (m_x^+ - m_x^- - m_y^+ + m_y^-) \\
\text{(2-3)}
\end{align*}
\]

Furthermore, five levels of line voltage can be obtained: 0, \( \frac{V_{DC}}{2} \), \( -\frac{V_{DC}}{2} \), \( V_{DC} \) and \( -V_{DC} \). The phase voltage is defined as in equation (2-4). If switching variables are introduced in this equation, another equation (2-5) will result.

\[
\begin{align*}
V_{an} &= V_{a0} - V_{a0} = V_{a0} - \frac{1}{3} (V_{a0} + V_{b0} + V_{c0}) = \frac{2}{3} V_{a0} - \frac{1}{3} V_{b0} - \frac{1}{3} V_{c0} \\
\text{(2-4)}
\end{align*}
\]

\[
\begin{align*}
V_{an} &= \frac{V_{DC}}{2} \left( \frac{2}{3} m_a - \frac{1}{3} m_b - \frac{1}{3} m_c \right) \\
\text{(2-5)}
\end{align*}
\]

If the stationary vectors are introduced into equation (2-5) it can be observed that nine voltage levels are created. Furthermore, as the DC link voltage for this project was chosen to be 600 V, those nine levels are \( \pm 400, \pm 300, \pm 200, \pm 100, 0 \).
To produce AC voltage waveforms with multiple levels, the diode – clamped multilevel inverter employs clamping diodes and cascade DC capacitors. In high power, the configuration used most often is three level neutral point clamped inverter. The most important characteristic of the NPC inverter, in comparison with two level inverters is that in AC output voltage dv/dt and THD is reduced [19].

Figure 2-3 presents the layout of a three level NPC inverter. Each inverter leg is composed of four switches with anti-parallel diodes. In real life these diodes are comprised inside the switching device module, if they are IGBTs. A zero DC voltage point is present dividing the DC link in two, which ensures the switching of each phase output to one of three level voltages. The most important benefit of this configuration is that every switching device needs to block only one half of the DC link voltage, but the main problem emphasis that DC link created by the two series capacitors needs to be balanced. A steady-state unbalance at the neutral point can appear due to non-idealities, nonlinearities and transients. For this problem there are two solutions presented [20]:

- Connect each capacitor to its own isolated DC source
- Balance of the midpoint by feedback control

![Neutral Point Clamped Inverter Topology](image)

The clamping diodes \(D_{A5}, D_{A6}, D_{B5}, D_{B6}, D_{C5}, D_{C6}\) are connected to neutral point. When the switches \(T_{A1}\) and \(T_{A3}\) are switched on, the inverter output terminal A is connected to the neutral point through one of the clamping diodes \(D_{A5}\) and \(D_{A6}\). For a better analysis, one inverter leg is presented in Figure 2-4, representing the inverter states: P, N, 0.

In the switching state P (Figure 2-4a) the upper two switching devices are on and the resulting inverter leg voltage is \(+\frac{V_{DC}}{2}\), while in N switching state (Figure 2-4c) the lower two switching devices are on and inverter leg voltage is \(-\frac{V_{DC}}{2}\). When the inner two switches \(T_2\) and \(T_3\) are on the inverter leg voltage is 0, hence the switching state 0 (Figure 2-4b). The switches \(T_1 - T_3\) and \(T_2 - T_4\) operate in a complementary mode [21].
Considering that the load current $i_A$ is constant during commutation due to inductive load, the DC link capacitors are large enough and that all the switching devices are ideal, the commutation can be analysed [19]:

- **Commutation when $i_A > 0$**

In switching state 0, switches $T_1$ and $T_3$ are off and voltage across each one is $\frac{V_{dc}}{2}$. The devices $T_2$ and $T_3$ are on and the voltage across them is 0. Furthermore, the clamping diode $D_5$ is turned on by phase A current, $i_A$. During dead time $\delta$, $T_3$ is turned off and load current path remains the same. When $T_3$ is completely off, the voltage across $T_3$ and $T_4$ becomes $\frac{V_{dc}}{4}$.

In switching state P, the first transistor $T_1$ is on and the clamping diode $D_5$ is turned off. The load current $i_A$ is commutated from $D_5$ to $T_1$. Since $T_3$ and $T_4$ were off, the voltage across each one is $\frac{V_{dc}}{2}$.
Chapter 2 – NPC Converter

- **Commutation when \( i_A < 0 \)**

In switching state 0, the transistors \( T_2 \) and \( T_3 \) are on and the clamping diode \( D_6 \) is turned on by the phase A current, \( i_A \). The voltage across \( T_1 \) and \( T_4 \) is \( \frac{V_{DC}}{2} \). Furthermore, during dead time interval \( \delta \), \( T_3 \) is turned off. Diodes \( D_1 \) and \( D_2 \) are turned on and the voltage across \( T_1 \) and \( T_2 \) is 0 because \( i_A \) cannot change direction instantly. The phase A current, \( i_A \), is then commutated from \( T_3 \) to the diodes. While \( T_3 \) is turned off, the voltage across \( T_4 \) will have a maximum of \( \frac{V_{DC}}{2} \) due to the diode \( D_5 \). Hence, the voltage across \( T_3 \) increases from 0 to \( \frac{V_{DC}}{2} \) while voltage across \( T_4 \) is \( \frac{V_{DC}}{2} \).

In switching state P, the first two transistors, \( T_1 \) and \( T_2 \), are turned on and not affect the operation of the circuit. Even if \( T_1 \) and \( T_2 \) are on, they do not carry load current due to \( D_1 \) and \( D_2 \) conduction. The conclusion is that all switching devices sustain half of the DC link voltage during switching P-0, 0-P, N-0, 0-N. Switching P-N is denied because it involves all four switches commutated and the switching losses will be doubled.

Table 2-2 describes the switching states of the NPC inverter leg presented in Figure 2-4. The positive state denotes that the two upper switches are on and the voltage across the output terminal is \( \frac{+V_{DC}}{2} \). This voltage is determined with respect to the neutral point 0. The negative state denotes that the two lower switches are turned on with respect to neutral point 0 and the output voltage is \( \frac{-V_{DC}}{2} \).

<table>
<thead>
<tr>
<th>State</th>
<th>T1</th>
<th>T2</th>
<th>T3</th>
<th>T4</th>
<th>Output phase Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>( \frac{+V_{DC}}{2} )</td>
</tr>
<tr>
<td>N</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>( \frac{-V_{DC}}{2} )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Some of the most important advantages of diode-clamped multilevel VSI can be summarised as [17]:

- If the inverter level increases, the size and weight of harmonic filter decreases and thus, the need for harmonic filter decreases
- High efficiency
- Simple control for a back-to-back system

Electrostatic couplings between the rotor and stator windings produce shaft voltages and voltages between the rotor and the motor frame. These voltages will generate flashovers when the voltage exceeds the dielectric strength of the grease in the bearing [22].

One of the most important problems in the control of multilevel converters is the determination of switching angle so that the converter produces the required fundamental voltage and does not generate lower order dominant harmonics.

The main problems in the NPC can be summarised as [23]:

[12]
• Increased switching frequency in the converters can generate EMI.
• The common mode voltage is generated between the neutral point of the load and the NP of the inverter by means of PWM in the three phase inverter.
• Due to parasitic capacitances in the machine structure, the CMV creates problems such as shaft voltage and bearing currents.

In multilevel inverters CMV can be reduced or eliminated. These types of inverters have a high number of switching states; therefore the output voltage is stepped in small increments. The switching losses are reduced by the mitigation of the harmonics at low frequencies, thus the leakage current is reduced by a lower \( \frac{dv}{dt} \). A feasible solution is to eliminate the CMV by PWM techniques.

### 2.2. Classical Modulation Strategies

#### 2.2.1. Background

In the early stages of Voltage Source Inverters (VSI), the operation mode was square wave. Using this type of operation mode the inverter phase and phase – to – phase output voltage has a square wave shape. An important drawback of this operation mode is that the output voltage of the inverter has low order harmonics, such as 5\(^{th}\) and 7\(^{th}\), with large magnitude. Regardless of this drawback this operation mode was preferred due to low number of switchings, as the switching devices used in the first inverters had long turn – on and turn – off time, thus the switching losses were high. Utilization of these switches made the switching at high frequency impossible, therefore the square wave operation was preferred [1].

Due to increasing development in the semiconductor technology faster switching devices have been developed. In VSI the most used power semiconductors are the IGBTs. These devices have low turn – on and turn – off times, thus reducing switching losses and making switching at high frequency possible. Nowadays, the PWM methods are preferred in three – phase motors due to superior characteristics. In this operation mode low current harmonics are not present, only at inverter switching frequency, and further on current damped by the motor windings [1].

In the carrier based PWM method, the power switches are turned on and off according to a carrier period in an appropriate manner in order to generate switch pulse patterns. There are three categories of modulation and control strategies for three level inverters [5]:

• Carrier based PWM – is a method based on the comparison of a fundamental sinusoidal waveform with two carrier signals
• Space Vector Modulation (SVM) – is defined by the switching states of the commutation devices
• Selective Harmonic Elimination (SHE) – in this method the commutation devices operate at a very low frequency in order to reduce the losses. The strategy is to control the fundamental frequency and to eliminate the harmonics five and seven.
Recently, more and more modulation strategies are implemented into Digital Signal Processors (DSP). PWM signals have to be calculated in real time, thus significant time is required for computation. When using SVM, the process for calculation is simplified. Therefore the computation time is reduced and better performance can be achieved.

It is known [24] that for each carrier-based there is an equivalent SVM and vice-versa. In [24] [25] [26] is concluded that by common-mode injections, an equivalent SVM of carrier-based modulation can be obtained. By selection of proper dwell times for the redundant states, the SVM can provide an equivalent for the carrier-based modulation. The authors choose for this project the Space Vector Modulation.

The SVM determines each switching state of the inverter in the complex \((a\beta)\) space. The phasor rotating at the fundamental frequency is sampled and the three inverter switching states (nearest) are selected with the duty cycles calculated so that the same volt-second average is obtained as in the sampled reference frame. There is a vast research based on modulation strategies as SVM, which became a standard in the industry for the power converters. Park and Kron were the first ones to represent three phase systems in vectorial form [27]. Active and zero space vectors represent active and zero switching states. A typical space vector diagram is formed in the SVM hexagon with six equal sectors. Each sector can be divided into four equilateral triangles. This can be seen in Figure 2-5. The centre of the hexagon is represented by the zero vector \(\bar{V}_0\) [19].

![Figure 2-5 - Space Vector Diagram - Sectors and Regions [19]](image)

A three phase system defined by \(a_x(t), a_y(t)\) and \(a_z(t)\) can be represented by a rotating vector \(\bar{a}_x\) from equation (2-6):

\[
\bar{a}_x = \frac{2}{3} [a_x(t) + aa_y(t) + a^2a_z(t)]
\]

\(a = e^{j\frac{2\pi}{3}}\) \quad (2-7)

The vectorial form can be obtained after Clarke transformation represented in equations (2-8) and (2-9):
\[
[ A_\alpha \\
A_\beta ] = T \begin{bmatrix}
A_x \\
A_y \\
A_z
\end{bmatrix}
\] (2-8)

\[
T = \frac{2}{3} \begin{bmatrix}
1 & -1 & -1 \\
-\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\
0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix}
\] (2-9)

The coefficient \( \frac{2}{3} \) is used so that the magnitude of the two phase voltages after transformation will have the same magnitude as the three phase voltages [19]. Inverse transformation can be obtained as in equation (2-10):

\[
\begin{bmatrix}
A_x \\
A_y \\
A_z
\end{bmatrix} = T^{-1} \begin{bmatrix}
A_\alpha \\
A_\beta
\end{bmatrix}
\] (2-10)

\( A_\alpha \) and \( A_\beta \) form a orthogonal two phase system. Furthermore, \( \overline{a_s} \) can be written as in equation (2-11):

\[
\overline{a_s} = a_\alpha + ja_\beta
\] (2-11)

Now there is a correspondence between the three phase system and the space vector in the three phase plane, hence some advantages appear:

- The three phase system can be analysed as a whole.
- Properties of a vectorial system can be used. When rotating with \( \omega t \) the analysis can be made in DC.

The voltage space vector in the complex \( \alpha \beta \) can be written as in equation (2-12). Furthermore, the voltage phasor is expressed like in equation (2-13).

\[
\overline{v(t)} = v_\alpha(t) + jv_\beta(t)
\] (2-12)

\[
\overline{v(t)} = \frac{2}{3} [v_{A0}(t)(1 + j0) + v_{B0}(t)(-0.5 + j\frac{\sqrt{3}}{2}) + v_{C0}(t)(-0.5 - j\frac{\sqrt{3}}{2})]
\] (2-13)

The exponential form can be written as equation (2-14).

\[
\overline{v(t)} = \frac{2}{3} [v_{A0}(t)e^{j0} + v_{B0}(t)e^{j2\pi/3} + v_{C0}(t)e^{j4\pi/3}]
\] (2-14)

From equation (2-14) the size for each type of vector can be calculated, equations (2-15) – (2-18).

- Zero vector:

\[
\overline{v_{zero}} = \overline{v_{000}} = \frac{2}{3} [0e^{j0} + 0e^{j2\pi/3} + 0e^{j4\pi/3}] = 0
\] (2-15)
Chapter 2 – NPC Converter

- Small vector:
  \[
  \underline{v}_{\text{small}} = \underline{v}_{\text{PN0}} = \frac{2}{3} \left[ \frac{V_{DC}}{2} e^{j0} + 0 e^{\frac{2\pi}{3}} + 0 e^{\frac{4\pi}{3}} \right] = \frac{1}{3} V_{DC}
  \]  
  (2-16)

- Medium vector:
  \[
  \underline{v}_{\text{medium}} = \underline{v}_{\text{P0N}} = \frac{2}{3} \left[ \frac{V_{DC}}{2} e^{j0} + 0 e^{\frac{2\pi}{3}} - \frac{V_{DC}}{2} e^{\frac{4\pi}{3}} \right] = \frac{\sqrt{3}}{3} V_{DC}
  \]  
  (2-17)

- Large vector:
  \[
  \underline{v}_{\text{large}} = \underline{v}_{\text{PPN}} = \frac{2}{3} \left[ \frac{V_{DC}}{2} e^{j0} + \frac{V_{DC}}{2} e e^{\frac{2\pi}{3}} - \frac{V_{DC}}{2} e^{\frac{4\pi}{3}} \right] = \frac{2}{3} V_{DC}
  \]  
  (2-18)

Space vector modulation is performed in real time and is used to determine the correct duty cycles for the corresponding switching sequences [18].

There is a total number of 24 active vectors which can be split in three categories: large, medium and small vectors. There are 6 large vectors, 6 medium vectors, 12 small vectors and 3 additional zero vectors. The midpoint charge is related to the switching vectors [28]. Figure 2-6 presents the vectors and their switching states.

![Figure 2-6 – NPC Vectors and Switching States](image)

Active and zero vectors are called stationary vectors due to the fact that they do not move in space. The reference vector \( \underline{V}_{\text{ref}} \) rotates with the angular speed \( \omega \) which is proportional with the fundamental frequency \( f_1 \) of the inverter, equation (2-19):

\[ [16] \]
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\[ \omega = 2\pi f_1 \] (2-19)

In \( \alpha \beta \) plane the angle between \( V_{ref} \) and \( \alpha \) axis is, equation (2-20):

\[ \theta(t) = \int_{0}^{t} \omega(t) dt + \theta(0) \] (2-20)

The twelve small vectors can be split in six sets of two types: N and P. The six sets have same direction and magnitude according to switching combination and will connected to one of the output lines through the upper or lower capacitor. Each set of vectors draw current in the opposite directions from the neutral point. By correct selection of small vectors for the reference vector, the balance can be set.

The medium vectors have one definition per current direction. One of the three output lines is permanently connected to the midpoint. When the reference vector is synthesized with the medium vector the line current flows through the midpoint. If the charge cannot be compensated with small vectors, the compensation is given to the next medium vector because it could have opposite current direction [28]. Further, the large vectors does not have direct connection to the neutral point, hence they do not influence it.

<table>
<thead>
<tr>
<th>Vector Magnitude</th>
<th>Vector Type</th>
<th>Space Vector</th>
<th>P Type</th>
<th>N Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{1}{3} V_{dc} )</td>
<td>Small Vector</td>
<td>( v_1 )</td>
<td>P00</td>
<td>ONN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_2 )</td>
<td>PPO</td>
<td>00N</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_3 )</td>
<td>0PO</td>
<td>NON</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_4 )</td>
<td>OPP</td>
<td>N00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_5 )</td>
<td>0OP</td>
<td>NNO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_6 )</td>
<td>POP</td>
<td>0NO</td>
</tr>
<tr>
<td>( \frac{\sqrt{3}}{3} V_{dc} )</td>
<td>Medium Vector</td>
<td>( v_7 )</td>
<td>PON</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_8 )</td>
<td>OPN</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_9 )</td>
<td>NPO</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{10} )</td>
<td>NOP</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{11} )</td>
<td>ONP</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{12} )</td>
<td>PNO</td>
<td></td>
</tr>
<tr>
<td>( \frac{2}{3} V_{dc} )</td>
<td>Large Vector</td>
<td>( v_{13} )</td>
<td>PNN</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{14} )</td>
<td>PPN</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{15} )</td>
<td>NPN</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{16} )</td>
<td>NPP</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{17} )</td>
<td>NNP</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( v_{18} )</td>
<td>PNP</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Zero Vector</td>
<td>( v_0 )</td>
<td>000</td>
<td>PPP</td>
</tr>
</tbody>
</table>

A switching state, for example ONP means that the inverter leg A is connected to the neutral point (0), leg B is connected to negative side (- or N) and the third leg C is connected to the positive side (+ or P).
These methods are based on load currents and the midpoint balance is kept to zero with a small variance, depending on the size of the capacitors. The efficiency of these methods is limited. This problem appears because the midpoint is used as power source. The midpoint problem increases with the level of the converter. The voltage vectors and the switching states are summarized in the Table 2-3:

The reference vector is built based on three stationary vectors. Each of the stationary vectors is applied for a specific time, the dwell time. The dwell time is defined as the duty cycle time of the switches during the modulation sampling period. The volt per second balancing principle is used in order to calculate the dwell times [19]. The principle is shown in equation (2-21):

$$\int_{0}^{T_s} \tilde{V}_{ref} dt = \int_{0}^{T_a} \tilde{V}_x dt + \int_{T_a}^{T_b} \tilde{V}_y dt + \int_{T_b}^{T_c} \tilde{V}_z dt$$

(2-21)

$$T_x = T_a + T_b + T_c$$

(2-22)

Where:

- $T_s$ is the sampling period
- $\tilde{V}_x$, $\tilde{V}_y$ and $\tilde{V}_z$ are the nearest three vectors from arbitrary sector and region
- $T_a$, $T_b$ and $T_c$ are the dwell times for the three chosen vectors.

The volt – second balancing principle states that the product of the reference vector with the sampling period equals the sum of the products between the stationary vectors and their corresponding dwell times. This is shown in equation (2-23):

$$\tilde{V}_{ref} T_s = \tilde{V}_x T_a + \tilde{V}_y T_b + \tilde{V}_z T_c$$

(2-23)

Voltage space vectors can also be expressed as:

$$\tilde{V} = kV_{DC} e^{j\theta}$$

(2-24)

Where:

- $\theta$ is the angle displacement
- $k$ a constant dependent on the vector type

The fundamental output voltage of the inverter is controlled by amplitude modulation index $m_a$ which is defined as in equation (2-25):

$$m_a = \sqrt{3} \frac{V_{ref}}{V_{DC}}$$

(2-25)

The maximum magnitude of $V_{ref}$ is the radius of the largest circle that can be inscribed in the SVM hexagon. Medium vectors have the same length as the maximum $V_{ref}$.

$$V_{ref,max} = \frac{2}{3} V_{DC} \frac{\sqrt{3}}{2} = \frac{\sqrt{3}V_{DC}}{3}$$

(2-26)
Based on equations (2-25) and (2-26), the maximum modulation index can be calculated:

\[
\alpha_{\text{max}} = \sqrt{3} \frac{V_{\text{ref, max}}}{V_{\text{DC}}} = 1
\]  

(2-27)

The range of modulation index in SVM is in interval \([0, 1]\) if over-modulation is not considered. The maximum phase-to-phase voltage obtained by means of SVM is calculated in equation (2-28):

\[
V_{\text{max, SVM}} = \sqrt{3} \left( \frac{V_{\text{ref, max}}}{\sqrt{2}} \right) = 0.707 V_{\text{DC}}
\]  

(2-28)

Where: \( \frac{V_{\text{ref, max}}}{\sqrt{2}} \) is the maximum RMS value of the fundamental phase voltage.

### 2.2.2. Nearest Three Vectors with Even Harmonic Elimination

The Nearest Three Vectors with Even Harmonic Elimination (NTV-EHE) method was introduced by D. W. Feng and B. Wu in 2004 [29] for compliance with harmonic standards, like IEEE 519-1992, when the converter is used in rectifier mode. The generation of even order harmonics is due to fact that the waveform generated by SVM is not half-wave symmetrical [29]. Alternative switching sequences: one starting with \(N\) – type vector and the other with \(P\) – type vector needs to be used in order to obtain half-wave symmetrical voltage at the output.

The reference vector is synthetized by three stationary space vectors. The stationary vectors are chosen as the nearest three vectors from the region in which the reference vector is found. An example is considered where the reference vector falls in sector I, region 4, as seen in Figure 2-7. The reference vector will be synthetized by \(\vec{V}_2\), \(\vec{V}_7\) and \(\vec{V}_{14}\).

![Figure 2-7 – NTV – Stationary and Reference Vectors with Corresponding Dwell Times for Sector I, Region 4](image)

Using volt-second principle and assuming that during \(T_s\) the reference vector \(V_{\text{ref}}\) is constant equation (2-29) can be written.
\[ V_{ref} T_s = V_{14} T_a + V_7 T_b + V_2 T_c \] (2-29)

The stationary vectors can be summarized as in equation (2-30).

\[ V_{14} = \frac{2}{3} V_{DC} e^{j\frac{\pi}{3}} \quad V_7 = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} \quad V_2 = \frac{1}{3} V_{DC} e^{j\frac{\pi}{3}} \quad V_{ref} = V_{ref} e^{j\theta} \] (2-30)

The dwell times can be calculated by introducing equation (2-30) in (2-29). The result can be seen in equation (2-31).

\[ V_{ref} e^{j\theta} T_s = \frac{2}{3} V_{DC} e^{j\frac{\pi}{3}} T_a + \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} T_b + \frac{1}{3} V_{DC} e^{j\frac{\pi}{3}} T_c \] (2-31)

Equation (2-32) is obtained by transformation of equation (2-31) in polar coordinates.

\[ V_{ref} T_s (\cos \theta + j \sin \theta) = \frac{2}{3} V_{DC} T_a \left( \cos \frac{\pi}{3} + j \sin \frac{\pi}{3} \right) + \frac{\sqrt{3}}{3} V_{DC} T_b \left( \cos \frac{\pi}{6} + j \sin \frac{\pi}{6} \right) + \] \[ + \frac{1}{3} V_{DC} T_c \left( \cos \frac{\pi}{3} + j \sin \frac{\pi}{3} \right) \] (2-32)

In order to calculate the dwell times, equation (2-32) is divided into real and imaginary part. Together with the switching period, the equation system (2-33) is obtained:

\[ \begin{cases} V_{ref} T_s \cos \theta = \frac{\sqrt{3}}{3} V_{DC} T_a + \frac{\sqrt{3}}{6} V_{DC} T_b + \frac{\sqrt{3}}{6} V_{DC} T_c \\ V_{ref} T_s \sin \theta = \frac{1}{3} V_{DC} T_a + \frac{1}{2} V_{DC} T_b + \frac{1}{6} V_{DC} T_c \\ T_s = T_a + T_b + T_c \end{cases} \] (2-33)

By solving equation system (2-33) the dwell times will result as in equation (2-34):

\[ \begin{align*}
T_a &= T_s \left( 2\sqrt{3} \frac{V_{ref}}{V_{DC}} \sin \theta - 1 \right) \\
T_b &= T_s \left( 2\sqrt{3} \frac{V_{ref}}{V_{DC}} \sin \left( \frac{\pi}{3} - \theta \right) \right) \\
T_c &= T_s \left( 2 - 2\sqrt{3} \frac{V_{ref}}{V_{DC}} \sin \left( \frac{\pi}{3} + \theta \right) \right) \end{align*} \] (2-34)

Observing equation (2-34) it can be noticed that \( \sqrt{3} \frac{V_{ref}}{V_{DC}} \) is the modulation index, \( m_a \). Using the above calculations the dwell times for the first sector are obtained in Table 2-4 [19]:

[20]
Table 2-4 – Dwell Times for Reference Voltage in Sector I [19]

<table>
<thead>
<tr>
<th>Region</th>
<th>$T_a$</th>
<th>$T_b$</th>
<th>$T_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\vec{V}_1$</td>
<td>$T_s\left(2m_a \sin \left(\frac{\pi}{3} - \theta\right)\right)$</td>
<td>$\vec{V}_0$</td>
</tr>
<tr>
<td>2</td>
<td>$\vec{V}_1$</td>
<td>$T_s(1 - 2m_a \sin \theta)$</td>
<td>$\vec{V}_7$</td>
</tr>
<tr>
<td>3</td>
<td>$\vec{V}_1$</td>
<td>$T_s\left(2 - 2m_a \sin \left(\frac{\pi}{3} + \theta\right)\right)$</td>
<td>$\vec{V}_7$</td>
</tr>
<tr>
<td>4</td>
<td>$\vec{V}_{14}$</td>
<td>$T_s(2m_a \sin \theta - 1)$</td>
<td>$\vec{V}_7$</td>
</tr>
</tbody>
</table>

The dwell times for each sector can be determined based on Table 2-4 by modifying the angular displacement $\theta$. When calculating the dwell times for other sectors, the angle has to be adjusted so that it falls in the interval $\left[0, \frac{\pi}{3}\right]$. This can be done by extracting a multiple of $\frac{\pi}{3}$ from the actual angle and it is presented in equation (2-35):

$$\theta_n = \theta - \frac{\pi}{3}(n - 1) \quad (2-35)$$

Where:
- $\theta_n$ is the angle reduced to sector I
- $\theta$ is the actual angle
- $n$ is the sector number

The overall requirements for switching sequence design of a three level inverter are [19]:
- In one inverter leg, when moving from one switching state to another, only two switches can be used in complementary mode
- When moving from one sector to another there should be a minimum number of switchings
- Neutral point voltage deviation should be minimum

The dwell time between two opposite small vectors can be equally distributed in order to minimise the neutral point voltage deviation. There are two cases that need to be investigated regarding the position of the reference vector inside a sector:
- One small vector in the nearest three vectors – case 1
- Two small vectors in the nearest three vectors – case 2

Case 1 - the reference vector in sector I can be in region 3 or 4, as shown in Figure 2-8:
In order to minimize the NP voltage deviation, the dwell time for the small vector should be equally distributed between P and N type states [19]. A typical seven segment switching sequence is shown in Figure 2-9. From the switching sequence the following conclusions can be drawn:

- The sampling period equals the sum of all dwell times
- Only two switches are used in complementary mode
- Dwell time $T_c$ for $\vec{V}_2$ is equally distributed between P and N type states, thus minimizing the NP voltage influence
- The device switching frequency is half of the sampling frequency due to the fact that in each inverter leg there are only two switchings on each sampling period.

Case 2 – the reference vector in sector I can be in region 1 or 2. The region in which the reference vector is found is split in two sub-regions. Depending on which sub-region the reference vector is found, it will be
closer to one of the two small vectors. This will be the dominant small vector as it has the highest effect in
the NP voltage. The dominant vectors dwell time is distributed equally between its N and P type states. An
example can be seen in Figure 2-10:

![Diagram](image)

Figure 2-10 – Division of Region 2 in Sector I for Minimization of NP Voltage Deviation

Based on Figure 2-10 observations can be made:

- Transition between the two sub-regions implies an extra switching
- The average switching frequency is increased because of six extra switches in each fundamental
  switching period. The extra switching requires only two devices

The seven switching sequence for region 2a and 2b are shown in Figure 2-11:

![Diagram](image)

Figure 2-11 – Seven Segment Switching Sequences for $\bar{V}_{ref}$ in Sector 1, Region 2a and 2b

[23]
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Most standards, such as IEEE 519-1992, are very restrictive regarding THD in even harmonics. The NTV switching sequences can be altered in order to cancel phase-to-phase even harmonics from the voltage waveform.

Switching sequences can be split in two categories:
- Type A – the sequence starts with N type small vector
- Type B – the sequence starts with P type small vector

In classical SVM, only A type sequences are used. In order to force the phase-to-phase even harmonics to cancel, A and B types of switching sequences have to be alternated as shown in Figure 2-12.

![Figure 2-12 – Alternation of A and B Switching Sequences for Even Harmonic Elimination][29]

The requirement for even harmonic elimination is that the phase-to-phase voltage waveform is half wave symmetrical. Consider that the reference voltage vector is situated in sector I, region 4, as in Figure 2-9. The opposite half wave is reached when the reference vectors is situated in sector IV, region 4, as seen in Figure 2-13a.

![Figure 2-13 – Switching Sequence when \( \vec{V}_{ref} \) is situated in Sector IV, Region 4.][24]
In order to gain symmetry, the switching sequence in sector IV, region 4 has to start with a P type small vector. The modified sequence can be seen in Figure 2-13b. The phase voltages appear to be different in Figure 2-13, the only difference is an offset of $\frac{T_s}{2}$ between the a) and b) variants of the switching sequence.

It can be observed that $V_{AB}(\omega t)$ from Figure 2-13a equals $-V_{AB}(\omega t + \pi)$ from Figure 2-13b, as the sequences are 180 degree apart. A minor increase in the switching frequency can be observed compared with conventional NTV method [19]. The increase is due to extra switching required to alternate between A and B type sequences.

In order to validate the theory presented here and to develop new modulation strategies a base model was built using Matlab/Simulink R2011b and Plecs. The inverter model was divided into two main parts: the electronic part, consisting in switching devices, and the control one. In order to facilitate the DSP implementation, the modulation strategy was developed in Matlab code. The switching devices were modelled using Plecs toolbox. The general structure is presented in Figure 2-14. For a better control of the modulation strategy few input parameters have been chosen:

- Reference voltage, $V_{ref}$
- Simulation time
- Output frequency, $f$
- Switching time, $T_s$
- Deadtime, $dt$

The outputs of the Control block are the gate signals. These signals are fed to the Inverter block through the dead time generator, together with the DC link voltage.

![General Structure of NPC Converter Developed in Matlab/Simulink and Plecs](image)

In order to analyse the modulation strategy the following parameters were saved:

- DC link voltage
- DC link current
- CMV
- Inverter leg voltages ($V_{a0}, V_{b0}, V_{c0}$)
- Inverter phase voltages ($V_{an}, V_{bn}, V_{cn}$)
Chapter 2 – NPC Converter

- Inverter phase – to – phase voltages \((V_{ab}, V_{bc}, V_{ca})\)
- Inverter currents \((I_a, I_b, I_c)\)

The main conditions in which the simulations were performed are:

- DC link voltage of 600 V
- Switching frequency of 4 kHz
- Fundamental frequency of 50 Hz
- Dead time of 2 µs
- Six DC link capacitors with the configuration presented in chapter 4.2
- Load of 7.5 kW modelled as in chapter 4.2

The general structure for the developed modulation strategies is presented in Figure 2-15. First the input parameters have to be set, followed by the definition of the stationary vectors and switching table. Next a decision has to be done regarding neutral point balancing. If the method has the ability to balance the neutral point, and it is needed, the switching sequence for balancing is chosen otherwise the default one. If the method does not have NP balancing and it is needed a fault will be triggered, otherwise the default is selected. After choosing the output switching sequence the dwell times are calculated and the PWM signals are generated.

![Diagram](image)

Figure 2-15 - Modulation Strategy Structure for Simulation Model

In order to validate the proposed simulation model, the results of NTV-EHE implementation are analysed. Simulations at maximum modulation index were performed. Figure 2-16 presents the output currents in steady state. The RMS value of current on a phase is 12.11 A.
The leg voltage is defined as the voltage drop between one leg and the neutral point of the inverter, Figure 2-17. This voltage can have only three levels: $V_{\text{dc}}/2$, $0$, $-V_{\text{dc}}/2$, due to the direct connection to the positive, negative or midpoint of the DC link. Hence, the limits for the leg voltage are $+300$ V, $-300$ V and 0 V.

Figure 2-18 presents two fundamental periods of phase voltage, phase-to-phase voltage, CMV and DC link voltages. The first waveform from Figure 2-18 presents the phase voltage, defined as the voltage drop between one inverter leg and neutral point of the load with wye connection, $V_{\text{fan}}$. As can be seen this voltage is quasi-sinusoidal and has nine voltage levels $\pm400, \pm300, \pm200, \pm100, 0$. The second waveform from Figure 2-18 represents the phase-to-phase voltage, which has five voltage levels $\pm600, \pm300, 0$. The total harmonic distortion in this voltage is 26.73 [%]. Furthermore, the CMV for this method is presented in the third waveform from Figure 2-18 and it is defined as the voltage drop between the neutral point of the wye connected load and the neutral point of the DC link. As can be seen there are three voltage levels $\pm200, \pm100, 0$ with a fundamental period of 150 Hz. An analysis of this voltage will be performed in subchapter 5.9.

When referring to DC link voltage there has to be mentioned that this method has the ability of natural balancing. The voltage on the upper capacitor fluctuates between approximately 294 V and 308 V as for the lower capacitor the voltage is between 291 V and 306 V at maximum modulation index.
The active switching frequency per device is different than the sampling frequency. If \( D_{sw} \) is the number of devices which perform a commutation, \( D_{Total} \) is the total number of switches, \( f_s \) is the sampling frequency, \( f_1 \) is the fundamental frequency and \( S_{on,off} \) is the number of on/off and off/on switchings. The average active device switching frequency for NTV can be calculated as:

\[
\frac{D_{sw1}}{D_{Total}} f_s + \frac{D_{sw2}}{D_{TOTAL}} \frac{S_{on,off}}{2} S_{ext} f_1 = 2.025 \text{ kHz} \tag{2-36}
\]

Only six of the twelve transistors switch on and off per sampling frequency. Ignoring extra switching, for a 4 kHz sampling frequency there would result a 2 kHz active device frequency, due to the fact that when passing from region 1a to 1b or 2a to 2b, there is an extra switching, the 2 kHz is slightly increased. Per each fundamental period, there are six extra switchings which involve four devices out of twelve. The switching involves only on/off or off/on transition, hence the number of switches is divided by 2. The resulting frequency of 2.025 kHz is the average active switching frequency per IGBT.
The Zero Common Mode Method (ZCM) was first introduced by Haoran Zhang and Annette von Jouanne in 2000 [30]. This method uses the six active middle vectors and one zero vector due to their ability to create zero common mode voltage as long as the DC link is balanced. These vectors can be seen in Figure 2-19.

As can be seen in Figure 2-19 the sectors need to be redefined compared with NTV-EHE, therefore the first sector is between $\vec{V}_7$ and $\vec{V}_{12}$. Based on this rearrangement and together with volt-second principle the dwell times for the first sector can be calculated, (2-37):

$$\vec{V}_{ref} \cdot T_s = \vec{V}_{12} \cdot T_a + \vec{V}_7 \cdot T_b + \vec{V}_0 \cdot T_c$$

(2-37)

Where:

- $T_a$ – dwell time for vector $\vec{V}_{12}$
- $T_b$ – dwell time for vector $\vec{V}_7$
- $T_c$ – dwell time for vector $\vec{V}_0$

The stationary vectors for this method can be summarised as in equation (2-38)

$$\vec{V}_{12} = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{11\pi}{6}} \quad \vec{V}_7 = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} \quad \vec{V}_0 = 0$$

(2-38)

Introducing equation (2-38) in (2-37) it will result into equation (2-39).

$$V_{ref} e^{j\theta} T_s = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{11\pi}{6}} T_a + \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} T_b$$

(2-39)

Dividing equation (2-39) into real and imaginary part and transforming it into polar coordinates the system of equations (2-40) will be obtained:
\[
\begin{align*}
V_{\text{ref}} T_s \cos \theta & = \frac{1}{2} V_{\text{DC}} T_a + \frac{1}{2} V_{\text{DC}} T_b \\
V_{\text{ref}} T_s \sin \theta & = -\frac{\sqrt{3}}{6} V_{\text{DC}} T_a + \frac{\sqrt{3}}{6} V_{\text{DC}} T_b \\
T_s & = T_a + T_b + T_c
\end{align*}
\tag{2-40}
\]

By solving (2-40) the dwell times are obtained as in (2-41):

\[
\begin{align*}
T_a & = 2T_s \frac{V_{\text{ref}} \sin \left(\frac{\pi}{3} - \theta\right)}{V_{\text{DC}}} \\
T_b & = 2T_s \frac{V_{\text{ref}} \sin \theta}{V_{\text{DC}}} \\
T_c & = T_s - T_a - T_b
\end{align*}
\tag{2-41}
\]

If the angular displacement is modified in such a manner that falls into the first sector the dwell times are valid for the other sectors. By the use of zero and medium vectors the modulation index will be decreased \[29\]. The maximum amplitude for the reference voltage is described in equation (2-42):

\[
V_{\text{ref, max}} = \frac{\sqrt{3}}{3} V_{\text{DC}} \frac{\sqrt{3}}{2} = \frac{V_{\text{DC}}}{2}
\tag{2-42}
\]

The maximum modulation index for this method is presented in (2-43):

\[
m_{\text{a, max}} = \sqrt{3} \frac{V_{\text{ref, max}}}{V_{\text{DC}}} = \sqrt{3} \frac{V_{\text{DC}}}{2} = \frac{\sqrt{3}}{2} = 0.866
\tag{2-43}
\]

Due to the fact that in this method there are no redundant states and the transition between two adjacent states involves two inverter legs, the harmonic content is increases \[31\]. This method does not follow the rule regarding the transition between two switching states. Figure 2-20 presents the switching sequences for the first sector in the ZCM method.

![Switching Sequence for the First Sector in ZCM Method](image)
In order to test this modulation strategy, simulations were performed. The simulation structure presented in Chapter 2.2.2 was used. Simulations at its maximum modulation index, \( m_a = 0.866 \), were done.

Figure 2-21 presents two fundamental periods from phase voltage, phase-to-phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, \( V_{an} \). As can be seen this voltage is very similar with the output of a two level voltage source inverter, due to the fact that this strategy does not use all the vectors. Hence, the phase voltage levels are \( \pm 300, 0 \). The second waveform from Figure 2-21 is the phase-to-phase voltage, which has five voltage levels \( \pm 600, \pm 300, 0 \) as NTV-EHE. The total harmonic distortion in this voltage is 52.23 \([\%]\). Furthermore, the CMV for this method is presented in the third waveform. As it can be seen CMV has three voltage levels \( \pm 100, 0 \) (when deadtime is introduced) with a fundamental period of 150 Hz. As at NTV-EHE, a more specific analysis will be performed in subchapter 5.9.

By the use only of medium and zero vectors this method has the ability to self-balance. In steady state the voltage on the upper capacitor varies between approximately 296 V and 309 V as for the lower capacitor the voltage is between 292 V and 304V, at maximum modulation, \( m_a = 0.866 \).

As described at NTV-EHE the active switching frequency per device can be calculated. For this method this frequency is 2 kHz, due to the fact that there are no extra switchings.
2.3. **DC Link Balancing**

The voltage deviation problem is inherent to all three level NPC converters [32]. Neutral point voltage deviation implies that any current flowing through the NP of a three level inverter would cause the charging of one of the capacitors and the discharging of the other. The effect is that the output voltage becomes asymmetric. The unbalance problem does not appear in two level inverters or in three level inverters with separate DC sources [18].

From the total of 27 vector combination, 18 produce neutral point voltage deviation [32]. The zero and the large vectors have no influence on the neutral point. Aside from this, the voltage deviation can have more causes [18]:

- The capacitors have different parameters
- DC link capacitor failure
- Switching devices have different parameters
- Non-linear and unbalanced loads

By not taking care of the DC link voltage deviation the following problems can occur [18]:

- Premature failure of the switching devices because the voltage increases above $\frac{V_{dc}}{2}$
- THD increase due to asymmetric supply
- The terminal with lower voltage will limit the modulation ratio
- The inverter will become unable of synthetizing the output voltage in case of a major DC link voltage deviation

The effect of some switching states determines the AC currents to flow in and out the NP. These currents will generate a ripple in the NP voltage and low order harmonics. Without caring about the NP balancing, the DC link capacitors and the switching devices are prone to destruction [32].

The DC current ripple is important for the size determination of the DC link capacitors as they suppress the PWM current ripple. For the analysis of the DC link current ripple performance, $K_{DC}$ factor is defined which is the squared ratio of DC link ripple RMS over the output phase current RMS [1]. This can be seen on equations (2-44) and (2-45):

$$K_{DC} = \left( \frac{I_{DCR-RMS}}{I_{PH-RMS}} \right)^2$$  \hspace{1cm} (2-44)

$$I_{DCR-RMS}^2 = I_{DC-RMS}^2 - I_{DC-MEAN}^2$$  \hspace{1cm} (2-45)

For a longer capacitor life and smaller size requirements, the $K_{DC}$ variable has to be small. When the ASD runs at full load at rated current, the $K_{DC}$ will be small. At no load and small currents the DC link current ripple, $K_{DC}$, will have higher values. The influence of each type of vector can be seen in Figure 2-22.
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Figure 2-22 – Space Vectors Influence on the NP Current
When the inverter uses the zero vector with 000 configuration, all three inverter legs are connected to the midpoint of the DC link, Figure 2-22a, thus the switching states do not affect $V_0$. Figure 2-22b describes how the medium vector influences the neutral point. For a better understanding one medium vector was chosen, $V_7$. As can be seen in Figure 2-22b each of the inverter legs are connected to one of the load terminals: the positive side of the DC link is connected to the A terminal, the neutral point is connected to B terminal and negative side of the DC link is connected to C terminal. The voltage across the lower capacitor may increase or decrease depending on the operating conditions of the inverter [19].

The small vectors have an important influence on the neutral point. The P type vector causes an increase in the voltage across one capacitor and the N type vector a decrease. This is due to the fact that for P type vectors, one of the load terminals is connected to the positive DC link, respectively negative DC link for N type vectors. As an example the $V_1$ small vector was chosen. Its influence can be seen in Figure 2-22c for P type small vector, and Figure 2-22d for N type small vector [19].

When talking about large vectors it can be noticed that each of the load terminals are connected to the positive or negative DC link, never at the neutral point. Hence, these types of vectors do not influence the neutral point. Figure 2-22e presents the $V_{13}$ large vector. As it can be seen the A terminal of the load is connected to the positive DC link and B and C terminals to the negative DC link [19].

### 2.4. Common Mode Voltage

#### 2.4.1. Common Mode Voltage in Adjustable Speed Drives

Electric machines are an important part of the industry. Most motors are controlled by variable frequency drives. These drives generate high frequency noise in current and voltage. This noise can follow the paths [33]:

- To the load
- To the supply
- Shaft through the motor bearings

When applying PWM to a three phase inverter a voltage is generated between neutral point of the wye connected load and NP of the inverter. This voltage is known as common mode voltage and acts like a source for many unwanted problems in motor drives such as shaft voltage and bearing currents due to parasitic capacitances that exists in the motor structure [23] [34].

The switching operation of the inverter generates common mode voltages. From this point of view the common mode voltages are defined as being the zero – sequence voltages overlapped with noise generated by switching. If the magnitude is not reduced the motor phase – to – ground voltage can be substantially increased, thus leading to premature failure of motor winding insulation. As a result, the life of the motor is shortened. In medium voltage, motors need to be protected against common mode voltages, if they are not,
Chapter 2 – NPC Converter

the cost of the damaged motor will increase the cost of production [19]. The CMV path can be seen in Figure 2-23.

The parasitic capacitance between the stator winding and the rotor can be changed by changing the design parameters while other capacitances cannot be changed that easily. Also, shaft voltage will be higher on an increased stator slot tooth [6].

The parasitic capacitances between the stator winding, rotor and motor frame is presented in Figure 2-24. The capacitances are:

- $C_{wf}$ – equivalent capacitance between motor windings and motor frame
- $C_{wr}$ – capacitance between the stator windings and rotor
- $C_{rf}$ – capacitance between rotor and motor frame
- $C_b$ – bearing capacitance

In Figure 2-24 $I_{cm}$ describes the overall leakage current flowing from the motor frame to ground and $i_b$ is the bearing current. In practice the bearing currents are a small part of the overall leakage currents [1].

Three phase inverters have leg voltages ($V_{a0}, V_{b0}, V_{c0}$), phase voltages ($V_{an}, V_{bn}, V_{cn}$) and phase-to-phase voltages ($V_{ab}, V_{bc}, V_{ca}$). As can be seen from Figure 2-23 the leg voltages can be calculated as in equations (2-46), (2-47) and (2-48):
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\[ V_{a0}(t) = V_{an}(t) + V_{n0}(t) \]  \hspace{1cm} (2-46)  
\[ V_{b0}(t) = V_{bn}(t) + V_{n0}(t) \]  \hspace{1cm} (2-47)  
\[ V_{c0}(t) = V_{cn}(t) + V_{n0}(t) \]  \hspace{1cm} (2-48)

If equations (2-46), (2-47) and (2-48) are summed equation (2-49) is obtained:

\[ V_{a0}(t) + V_{b0}(t) + V_{c0}(t) = V_{an}(t) + V_{bn}(t) + V_{cn}(t) + 3 * V_{n0}(t) \]  \hspace{1cm} (2-49)

As well known, the sum of a three phase voltages into a balanced system is equal to zero, thus the CMV at the motor terminals can be described as in equation (2-50) and defined as the load star point to the centre of the DC bus of the VSI [35].

\[ V_{n0}(t) = \frac{V_{a0}(t) + V_{b0}(t) + V_{c0}(t)}{3} \]  \hspace{1cm} (2-50)

The CMV magnitude depends on the switching sequence. Leakage currents (common mode currents) flow from motor to ground and from cables to ground due to high \( \frac{dv}{dt} \) and magnitude of CMV. The most important consequences of the Common Mode Current (CMC) are the bearing currents, electromagnetic interference and inverter unwanted trips [1].

A. Shaft Voltage

On rotating shafts stray voltages occur with magnitudes from micro – volts to hundreds of volts. This voltage may be produced in two ways: by rotation of the shaft (and produced into the magnetic field of the earth) and electromagnetic communication signal induction. The stray voltage induced by electromagnetic signal can be produced by shaft rotation that links to the asymmetrical magnetism of electrical machine, through the residual magnetism present in the shaft or in adjacent stationary members and by induction from power electronics devices, exciters or current – carrying brushes [36].

Shaft voltages are produced by CMV through capacitive couplings between rotor and stator windings \( (C_{rs}) \) and between rotor and frame \( (C_{rf}) \). The structure of a simplified high frequency model of motor is described in Figure 2-24. Based on this figure the shaft voltage can be calculated as:

\[ V_{shaft} = \frac{C_{rs}}{C_b + C_{rs} + C_{rf}} * V_{CMV} \]  \hspace{1cm} (2-51)

Shaft voltages can help and harm the system. They can warn about problems regarding development at an early stage, but at the same time they can generate circulating currents, reduce the efficiency of the unit, and generate flashovers that can damage the bearings, seals, gears and couplings. The potential for damage can be reduced by controlling the shaft voltages. There are two methods for controlling the shaft voltage: passive and active. The active method refers to injecting counteracting current signals in the rotor and the passive method is by simply placing grounding brushes [36].
B. Shaft Current

According to the generating mechanism there can be multiple types of bearing currents. The inverter – induced bearing currents classification can be found in Figure 2-25.

![Figure 2-25 – Inverter – Induced Bearing Currents Classification](image)

The common mode voltage can result in capacitive bearings currents, Electric Discharge Machine (EDM) and leakage currents. High frequency shaft voltage is induced by leakage ground currents originated from high \( dv/dt \), therefore resulting in a source of high frequency circulating bearing currents. From all types of currents, the capacitive currents have the smallest magnitude and do not harm the motor. The most important common mode currents are EDM and High Frequency (HF) circulating bearing currents [1]. This can be seen in Figure 2-25.

The bearing currents appear when the shaft voltage exceeds the breakdown limit of the insulating grease thin film [3].

2.4.2. Switching Sequence Influence on CMV

Stationary vectors produce CMV, thus every vector influence in different manners [31]. Based on equations (2-46), (2-47), (2-48) and (2-50) the influence of every switching state on CMV can be calculated. As an example the sector I, region 4 from NTV-EHE was chosen. Each of the leg voltages has been drawn, as well as the resultant CMV for the case in which the DC link is balanced, presented in Figure 2-26.
Furthermore the influence of each space vector on the CMV can be calculated. This can be seen in Table 2-5: first column represents the switching state, column two the vector type, column three describes the CMV when the neutral potential is zero and column four when it is different from zero.

![NTV-EHE Sector I, Region 4 - Leg Voltages and their Resultant CMV](image)

**Table 2-5 – Influence of Space Vectors on CMV [31]**

<table>
<thead>
<tr>
<th>State</th>
<th>Vector Type</th>
<th>Common Mode Voltage ($V_0 = 0$)</th>
<th>Common Mode Voltage ($V_0 \neq 0$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Zero</td>
<td>0</td>
<td>$V_0$</td>
</tr>
<tr>
<td>NNN</td>
<td>Zero</td>
<td>$-\frac{1}{2}V_{DC}$</td>
<td>$-\frac{1}{2}V_{DC}$</td>
</tr>
<tr>
<td>PPP</td>
<td>Zero</td>
<td>$\frac{1}{2}V_{DC}$</td>
<td>$\frac{1}{2}V_{DC}$</td>
</tr>
<tr>
<td>NOO</td>
<td>Small</td>
<td>$-\frac{1}{6}V_{DC}$</td>
<td>$-\frac{1}{6}V_{DC} + \frac{2}{3}V_0$</td>
</tr>
<tr>
<td>ONO</td>
<td>Small</td>
<td>$-\frac{1}{6}V_{DC}$</td>
<td>$-\frac{1}{6}V_{DC} + \frac{2}{3}V_0$</td>
</tr>
<tr>
<td>OON</td>
<td>Small</td>
<td>$-\frac{1}{6}V_{DC}$</td>
<td>$-\frac{1}{6}V_{DC} + \frac{2}{3}V_0$</td>
</tr>
<tr>
<td>POO</td>
<td>Small</td>
<td>$\frac{1}{6}V_{DC}$</td>
<td>$\frac{1}{6}V_{DC} + \frac{2}{3}V_0$</td>
</tr>
<tr>
<td>OPO</td>
<td>Small</td>
<td>$\frac{1}{6}V_{DC}$</td>
<td>$\frac{1}{6}V_{DC} + \frac{2}{3}V_0$</td>
</tr>
<tr>
<td>OOP</td>
<td>Small</td>
<td>$\frac{1}{6}V_{DC}$</td>
<td>$\frac{1}{6}V_{DC} + \frac{2}{3}V_0$</td>
</tr>
<tr>
<td>NNO</td>
<td>Small</td>
<td>$-\frac{1}{3}V_{DC}$</td>
<td>$-\frac{1}{3}V_{DC} + \frac{1}{3}V_0$</td>
</tr>
<tr>
<td>NON</td>
<td>Small</td>
<td>$-\frac{1}{3}V_{DC}$</td>
<td>$-\frac{1}{3}V_{DC} + \frac{1}{3}V_0$</td>
</tr>
<tr>
<td>ONN</td>
<td>Small</td>
<td>$-\frac{1}{3}V_{DC}$</td>
<td>$-\frac{1}{3}V_{DC} + \frac{1}{3}V_0$</td>
</tr>
</tbody>
</table>
2.5. Method of Measuring EMI and CMV

2.5.1. Method of Measuring EMI

One of the most important problems in electric motor drives is the electromagnetic interference. This phenomenon produces undesirable effects on electronic devices. The top requirements in markets are increasing power density and decreasing cost and size of a system. When designing or optimising an electric machine drive: switching losses, harmonics and electromagnetic interference should be taken into account [37].

The operation of switching in power electronics, that feed one motor, creates electromagnetic noise in the drive system. EMI is generated by electromagnetic disturbances and can be classified as noise, impulses and transients. This noise goes into close circuits by inductive and capacitive couplings. This type of disturbance can be divided into [38]:

- Conducted EMI
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- Radiated EMI

The most problematic frequency range that Electromagnetic Compatibility (EMC) standards address for conducted disturbances is 0.15 – 30 MHz [39]. There are four methods developed for mitigation of Common Mode (CM) EMI:
- Passive CM current cancellation [40]
- Active noise cancellation [41]
- CMV source reduction through modified PWM strategies [42]
- Filters [43] [44]

Conducted EMI is defined as undesired electromagnetic energy coming from an emitter or entering into a receptor through cables or wires. This type of electromagnetic energy causes interference in electronic system due to the fact that power distribution is represented as a large antenna. In order to measure it the CISPR 16 standard needs to be taken into account. This international standard specifies the tests for compliance with conducted emissions limits and utilises the Line Impedance Stabilization Network (LISN), a passive filter, for measurements. This can be seen in Figure 2-27:

![Figure 2-27 Test Setup for EMI Measurement](image)

The current created by noise has two components:

- Common mode noise current, $I_{cm}$, that flows out from line and neutral and returns through the earth wire
- Differential mode noise current, $I_{dm}$, which flows from line and returns through neutral.

The test set-up presented in Figure 2-27 measures the total common and differential mode current in the line or neutral. These are measured across the 50 Ohm LISN resistor (R2).

This thesis proposes the reduction of the CM EMI by reducing the CMV through improved PWM strategies.
2.5.2. Method of Measuring CMV

For measuring CMV and CMC the setup from Figure 2-28 can be used. The setup is isolated from the network through the isolation transformer. The motor is mounted on an insulated plate (wood) for a good galvanic separation from the ground. The CMV is measured between the neutral point of the motor and the zero point of the DC link. The CMC must be measured via a high bandwidth current transducer and the CMV via a high bandwidth voltage probe [1].

Figure 2-28 – Test Setup for Measuring the CMV and CMC
3. Improved Modulation Strategies

This chapter introduces four improved modulation strategies developed based on the space vector table and theory presented in chapter 2. Each of this modulation strategies are validated through simulation results. This chapter ends with a comparative performance evaluation consisting of comparison at maximum modulation index as well as an analysis of THD in the phase-to-phase voltage throughout entire modulation index range.

3.1. One Small One Medium Vector

Analysing Table 2-5 from Chapter 2.4.2 it can be noticed that small vectors have the ability to natural balance the neutral point by proper switching from N – type to P – type vectors. In order to create this modulation strategy the space vector diagram is divided in twelve sectors with a 30° angle between small vectors and medium vectors. The appropriate vectors for this method, regarding sector one and two, are presented in Figure 3-1.

![Figure 3-1](image)

Figure 3-1 – One Small One Medium Vector Method

Considering the first sector, the reference vector is created from the stationary vectors $\bar{V}_0$, $\bar{V}_1$, $\bar{V}_7$. In order to calculate the dwell times for this sector the volt – second principle together with the assumption that during $T_s$ the reference voltage $V_{ref}$ is constant are used. This can be seen in equation (3-1).

$$\bar{V}_{ref}T_s = \bar{V}_1T_a + \bar{V}_7T_b + \bar{V}_0T_c$$  \hspace{1cm} (3-1)

The stationary vectors that form the reference voltage as well as the reference vector are summarized in equation (3-2).
\[
\vec{V}_1 = \frac{1}{3} V_{DC} e^{j0} \quad \vec{V}_7 = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} \quad \vec{V}_0 = 0 \quad \vec{V}_{ref} = V_{ref} e^{j\theta} \tag{3-2}
\]

Introducing (3-2) in (3-1) the dwell times can be calculated. The result can be seen in equation (3-3).

\[
V_{ref} e^{j\theta} T_s = \frac{1}{3} V_{DC} e^{j0} T_a + \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} T_b \tag{3-3}
\]

Equation (3-4) is obtained by transforming equation (3-3) into polar coordinates.

\[
V_{ref} T_s (\cos \theta + j \sin \theta) = \frac{1}{3} V_{DC} T_a (\cos 0 + j \sin 0) + \frac{\sqrt{3}}{3} V_{DC} T_b \left( \cos \frac{\pi}{6} + j \sin \frac{\pi}{6} \right) \tag{3-4}
\]

In order to calculate the dwell times, equation (3-4) is divided into real and imaginary part. Equation system (3-5) is obtained for a switching period:

\[
\begin{align*}
V_{ref} T_s \cos \theta &= \frac{1}{3} V_{DC} T_a + \frac{1}{2} V_{DC} T_b \\
V_{ref} T_s \sin \theta &= \frac{\sqrt{3}}{6} V_{DC} T_b \\
T_s &= T_a + T_b + T_c
\end{align*} \tag{3-5}
\]

Solving equation (3-5), dwell times will result as in equation (3-6):

\[
\begin{align*}
T_a &= 6 T_s \frac{V_{ref}}{V_{DC}} \sin \left( \frac{\pi}{6} - \theta \right) \\
T_b &= 2 \sqrt{3} T_s \frac{V_{ref}}{V_{DC}} \sin \theta \\
T_c &= T_s - T_a - T_b
\end{align*} \tag{3-6}
\]

The dwell times for odd sectors are determined based on equation (3-6) by adjusting the angular displacement so that it can fall in the interval \([0, \frac{\pi}{6}]\). For even sectors the dwell times are determined in the same manner.

In order to cancel the phase-to-phase even harmonics from the voltage waveform the switching sequences are divided in:

- Odd sector – the sequence is predominant by P type small vector
- Even sector – the sequence is predominant by N type small vector

The requirement for even harmonic elimination is that the phase-to-phase voltage waveform is half wave symmetrical. By alternating the N and P type small vectors these harmonics are forced to cancel. This can be seen in Figure 3-2.
Chapter 3 – Improved Modulation Strategies

When referring to modulation index it is needed to be mentioned that, for this method, the magnitude for the reference vector is limited to the inscribed circle in the hexagon created by the small vectors. The maximum reference vector is presented in equation (3-7):

\[ V_{ref,max} = \frac{1}{3} V_{DC} \frac{\sqrt{3}}{2} = \frac{\sqrt{3}V_{DC}}{6} \]  

(3-7)

The maximum modulation index is presented in equation (3-8):

\[ m_{a,max} = \sqrt{3} \frac{V_{ref,max}}{V_{DC}} = \sqrt{3} \frac{6}{\sqrt{3}V_{DC}} = \frac{1}{2} = 0.5 \]  

(3-8)

It can be mentioned that in comparison with ZCM, this method has the advantages:

- Redundant states
- Transition between two adjacent states does not involve two inverter legs

In order to test this modulation strategy simulations at its maximum modulation index, \( m_a = 0.5 \), were performed. The simulation structure presented in Chapter 2.2.2 was used. Figure 3-3 presents two fundamental periods of phase voltage, phase-to-phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, \( V_{an} \). This voltage has five levels \( \pm 300, \pm 100, 0 \), due to the fact that only small, medium and zero vectors are used. The second waveform from the same figure represents the phase-to-phase voltage, which has five voltage levels \( \pm 600, \pm 300, 0 \) as the classical methods. The total harmonic distortion in this voltage is 78.52 [%]. Furthermore, the CMV is presented in

[45]
the third waveform. As it can be seen CMV has three voltage levels ±100, 0, with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in Chapter 5.8.

By the use of small, medium and zero vectors this method has the ability to self-balance, through a proper switching between P and N type small vectors. The DC link voltage is presented in last waveform from Figure 3-3. In steady state the voltage on the upper capacitor varies between approximately 299 V and 304 V as for the lower capacitor the voltage is between 296 V and 301 V at maximum modulation, \( m_\alpha = 0.5 \).

Figure 3-3 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OSOM at \( m_\alpha = 0.5 \) - Simulation

As described at NTV-EHE the active switching frequency can be calculated and results as 1.33 kHz, due to the fact that only four transistors from a total of twelve perform a full commutation on each sampling period.
3.2. One Large One Medium Vector

In order to increase the modulation index and to better use the bus bar, one large and one medium vectors are used to define the reference vector. The space vector diagram is divided into twelve sectors with 30° angle between medium and large vectors as shown in Figure 3-4.

![Space Vector Diagram](image)

**Figure 3-4 – One Large One Medium Vector Method**

In order to calculate the dwell times, for this method, the first sector is taken into account. The reference vector is created by $\vec{V}_0$, $\vec{V}_{13}$, $\vec{V}_7$. Using volt – second principle together with the assumption that during $T_s$ the reference voltage is constant, equation (3-9) is obtained.

$$\overline{V}_{ref}T_s = \overline{V}_{13}T_a + \overline{V}_7T_b + \overline{V}_0T_c \quad (3-9)$$

The stationary vectors that form the reference voltage are summarized in equation (3-10).

$$\overline{V}_{13} = \frac{2}{3}V_{DC}e^{j0} \quad \overline{V}_7 = \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}} \quad \overline{V}_0 = 0 \quad (3-10)$$

The dwell times can be calculated by introducing (3-10) in (3-9). The result can be seen in equation (3-11).

$$V_{ref}e^{j0}T_s = \frac{2}{3}V_{DC}e^{j0}T_a + \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}}T_b \quad (3-11)$$

By transforming equation (3-11) into polar coordinates equation (3-12) is obtained.

$$V_{ref}T_s(cos\theta + jsin\theta) = \frac{2}{3}V_{DC}T_a(cos\ 0 + jsin\ 0) + \frac{\sqrt{3}}{3}V_{DC}T_b \left(cos\ \frac{\pi}{6} + jsin\ \frac{\pi}{6}\right) \quad (3-12)$$

Equation (3-12) is divided into real and imaginary part, thus obtaining the system of equations (3-13) for a switching period:
\[
\begin{align*}
V_{ref} T_s \cos \theta &= \frac{2}{3} V_{DC} T_a + \frac{1}{2} V_{DC} T_b \\
V_{ref} T_s \sin \theta &= \frac{\sqrt{3}}{6} V_{DC} T_b \\
T_s &= T_a + T_b + T_c
\end{align*}
\] (3-13)

Solving equation (3-13) the dwell times will result as in equation (3-14):

\[
\begin{align*}
T_a &= 3T_s \frac{V_{ref}}{V_{DC}} \sin \left( \frac{\pi}{6} - \theta \right) \\
T_b &= 2\sqrt{3}T_s \frac{V_{ref}}{V_{DC}} \sin \theta \\
T_c &= T_s - T_a - T_b
\end{align*}
\] (3-14)

The dwell times for all odd sectors are determined based on equation (3-14) by adjusting the angular displacement in such a manner that it can fall in the interval \([0, \frac{\pi}{6}]\). Furthermore, for even sectors the dwell times are determined in the same manner.

For a better understanding of the proposed modulation strategy the switching sequence for sector I is presented in Figure 3-5.

![Figure 3-5 – Five Segment Switching Sequences for \(V_{ref}\) in Sector I](image)

The modulation index for this method is determined by the inscribed circle in the hexagon created by large vectors. The maximum reference vector is presented in equation (3-15):

\[
V_{ref, max} = \frac{2}{3} V_{DC} \frac{\sqrt{3}}{2} = \frac{\sqrt{3}}{3} V_{DC}
\] (3-15)

The maximum modulation index is calculated in (3-16):
\[ m_{a,\text{max}} = \sqrt{3} \frac{V_{\text{ref, max}}}{V_{\text{DC}}} = \sqrt{3} \frac{3}{V_{\text{DC}}} = 1 \] (3-16)

In order to test this modulation strategy simulations at maximum modulation index, \( m_a = 1 \), were performed. The simulation structure presented in subchapter 2.2.2 was used. Figure 3-6 presents two fundamental periods of phase voltage, phase-to-phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, \( V_{an} \). This voltage has seven levels \( \pm 400, \pm 300, \pm 200, 0 \), due to the fact that only large, medium and zero vectors are used. The second waveform from the same figure represents the phase-to-phase voltage, which has five voltage levels \( \pm 600, \pm 300, 0 \) as expected. The total harmonic distortion in this voltage is 31.81 [%]. Furthermore, the CMV is presented in the third waveform. As it can be seen CMV has three voltage levels \( \pm 100, 0 \), with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in subchapter 5.9.

By the use of only of large, medium and zero vectors this method has the ability to self-balance. The DC link voltage is presented in last waveform from Figure 3-6. In steady state the voltage on the upper capacitor varies between approximately 294 V and 308 V as for the lower capacitor the voltage is between 292 V and 306 V at maximum modulation index, \( m_a = 1 \).

As described for the classical modulation strategy NTV-EHE the active switching frequency on each device can be calculated. For this method the active switching frequency is 2 kHz.


3.3. Zero Small Medium Large Method

Taken into consideration Table 2-5 and theory presented at NTV, another method can be proposed. The idea behind this method is to use all four vectors in order to maintain the THD low, while choosing the small vectors in such a manner that the CMV levels are half compared to NTV. The space vector diagram is divided into six sectors each of them having two regions. This configuration can be seen in Figure 3-7. First region lasts between \([0, \frac{\pi}{6}]\) and the second one between \([\frac{\pi}{6}, \frac{\pi}{3}]\).

![Space Vector Diagram for Zero Small Medium Method in Sector I](image)

Figure 3-7 – Space Vector Diagram for Zero Small Medium Method in Sector I

In order to calculate the dwell times the volt-second principle is used, together with the assumption that during switching time the reference vector is constant. As an example the reference vector from sector I, region 1 is presented in equation (3-20) and its stationary vectors in equation (3-18).

\[
\overrightarrow{V_{ref}}T_s = \overrightarrow{V_1}T_a + \overrightarrow{V_7}T_b + \overrightarrow{V_{13}}T_c + \overrightarrow{V_0}T_d
\]  

(3-17)

\[
\overrightarrow{V_{13}} = \frac{2}{3} \overrightarrow{V_{DC}} e^{j0} \quad \overrightarrow{V_7} = \frac{\sqrt{3}}{3} \overrightarrow{V_{DC}} e^{j\frac{\pi}{6}} \quad \overrightarrow{V_1} = \frac{1}{3} \overrightarrow{V_{DC}} e^{j0} \quad \overrightarrow{V_0} = 0
\]  

(3-18)

The dwell times are calculated differently for each half-sector. A factor \(k_1\) is inserted in the equations in order to make possible the division of the dwell times between the four vectors. This factor has been defined as the ratio between the reference voltage and maximum reference voltage, equation (3-19). Furthermore, when the amplitude of the reference voltage is maximum only small, medium and large vectors will form it.

\[
k_1 = \frac{V_{ref}}{V_{ref,\text{max}}}
\]  

(3-19)

When calculating the dwell times, the displacement angle needs to be taken into account. Hence when the displacement angle is in region 1 the dwell times have the form presented in equation (3-20) and when is in region 2 they have the form presented in equation (3-21).
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\[
\begin{align*}
T_{aa} &= T_s \frac{-3 * V_{ref} * \cos \theta + 2 * k1 * V_{DC} - \sqrt{3} * V_{ref} * \sin \theta}{k1 * V_{DC}} \\
T_{bb} &= 2\sqrt{3} * T_s \frac{V_{ref} * \sin \theta}{k1 * V_{DC}} \\
T_{cc} &= T_s \frac{3 * V_{ref} * \cos \theta - 3\sqrt{3} * V_{ref} * \sin \theta - k1 * V_{DC} + 2\sqrt{3} * V_{ref} * \sin \theta}{k1 * V_{DC}}
\end{align*}
\]

\[
\begin{align*}
T_{aa} &= T_s \frac{-3 * V_{ref} * \cos \theta + 2 * k1 * V_{DC} - \sqrt{3} * V_{ref} * \sin \theta}{k1 * V_{DC}} \\
T_{bb} &= T_s \frac{3 * V_{ref} * \cos \theta - \sqrt{3} * \sin \theta}{k1 * V_{DC}} \\
T_{cc} &= T_s \frac{2\sqrt{3} * V_{ref} * \sin \theta - k1 * V_{DC}}{k1 * V_{DC}}
\end{align*}
\]

Based on equations (3-20) and (3-21), the dwell times are presented in equation (3-22):

\[
\begin{align*}
T_a &= k1 * T_{aa} \\
T_b &= k1 * T_{bb} \\
T_c &= k1 * T_{cc} \\
T_d &= (1 - k1) * T_s
\end{align*}
\]

This method is able to balance the DC link, in a case of an external event, by proper use of the small vectors. When in balancing mode, the CMV levels are same as NTV. As all the vectors are used, the largest vector that can be inscribed in the hexagon is the large vector, thus the modulation index is 1, as at the classical method, NTV-EHE. For a better understanding of this method a typical switching sequence is presented in Figure 3-8:

Figure 3-8 – Switching Sequence for ZSML in Sector I, Region 1
Chapter 3 – Improved Modulation Strategies

In order to test this modulation strategy, simulations at maximum modulation index, \( m_a = 1 \), were performed based on the simulation structure presented in subchapter 2.2.2. Figure 3-9 presents two fundamental periods of phase voltage, phase-to-phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, \( V_{am} \). This voltage has a quasi-sinusoidal shape and nine levels \( \pm 400, \pm 300, \pm 200, \pm 100, 0 \), because all the stationary vectors are used in order to form the reference voltage vector. The second waveform from this figure represents the phase-to-phase voltage, which has five voltage levels \( \pm 600, \pm 300, 0 \) as expected. The total harmonic distortion in the line voltage is 27.13 \([\%]\). Furthermore, the CMV is presented in the third waveform. As it can be seen CMV has three voltage levels \( \pm 100, 0 \), with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in subchapter 5.9.

By the use of stationary vectors this method has the ability to self-balance and balance the DC link in case of an external disturbance. The voltage on the DC link capacitors under natural balancing conditions is presented in last waveform from Figure 3-9. In steady state the voltage on the upper capacitor varies between approximately 295 V and 309 V as for the lower capacitor the voltage is between 291 V and 305 V at maximum modulation index, \( m_a = 1 \).

As presented at NTV-EHE the active switching frequency on each device can be calculated. For this method this frequency is 2 kHz as only six of the twelve transistors are commutated in each sampling period.
3.4. Random Sequence of 3 Vectors with Neutral Point Balancing Method

The idea of randomization is not new to inverters modulation, but its purpose and utilization is quite different from the idea implemented in Random Sequence of 3 Vectors with Neutral Point Balancing (RS3N). Some methods used are SVM with variable switching frequency others are deterministic [45] because of the fixed switching frequency. The methods try to maintain the average switching frequency low while reducing acoustic noise [46]. Lead-lag modulation (RLL) aligns the pulse position with the beginning or the end of the switching interval. Random displacement of pulse centre (RCD) aligns the centre of pulses from each phase. Random distribution of zero vector (RZD) is based on the idea that zero vector time is randomly divided between PPP and 000 state [46]. The RLL, RCD and RZD are fixed frequency random modulation strategies for two level inverters.

Random pulse width modulation is known to be proposed for reduction of current harmonics, torque ripple and acoustic noise [45]. Because using a variable switching frequency is microcontroller intensive, the methods based on fixed switching frequency are preferred.

The proposed method is based on the idea that each switching sequence can have the vector order changed, having an impact in the CMV due to the reduction of voltage levels at high frequencies. Eliminating the repetition of the CMV distribution between each switching sequence should have a big impact on the frequencies which are a multiple of the switching frequency. These assumptions are confirmed in both the simulation and the experimental results.

The idea behind the RS3N modulation strategy is to improve spectral performance on CMV while reducing it in the time domain to half of NTV. To obtain this, the switching sequence for each combination of nearest three vectors is done in a sequence of three vectors. Using a pseudo-random number generator, this switching sequence is randomized up to 80 times on each period of the output frequency. The maximum randomization value is obtained as in equation (3-23).

$$r = \frac{f_{sw}}{f_{out}} = \frac{4000}{50} = 80$$  \hspace{1cm} (3-23)

Where:

- \( r \) – is the randomization factor
- \( f_{sw} \) – is the switching frequency
- \( f_{out} \) – is the output frequency

By having the switching sequence randomized, the resultant CMV levels on each sequence will not be repeated anymore, thus reducing the CMV levels which are multiple of switching frequency, in the frequency domain. An example of the effect of randomization can be seen in Figure 3-10, the CMV output does not repeat from one sequence to another.
For this method, the space vector diagram is divided in 6 sectors, as the NTV-EHE. The difference between these two is that there are only four regions in each sector, and the behaviour of the modulation in these regions is different. As it is well known that some of the small vectors produce less CMV [31], these vectors are preferred in each region. By choosing these vectors, the CMV levels in the time domain are half of NTV for any modulation index. The division between sectors and regions can be seen in Figure 3-11. The THD should follow the behaviour of the NTV-EHE method due to the fact that it relies on the choice of the nearest three vectors.

As this method uses the same principle as NTV, the dwell times will have the same form as well as the modulation index.
Chapter 3 – Improved Modulation Strategies

The method is able to balance the DC link voltage, in a case of an external event, by proper use of the P and N type small vectors. During balancing mode, in case on an external event, the CMV level in time domains are same to NTV, however there is an improvement in the frequency domain due to switching sequence randomization.

In order for this method to function adequately, two filters were implemented. The first filter ensures that there is no N-P or P-N switching between two consecutive sequences and the second one that the combination P-O-P is avoided, in order to make the DSP implementation possible. These two filters follow the principle: if one of the two events is detected, another random number is chosen and the switching sequence is randomized again. If the new combination passes the two filters, is sent to the output. For the DSP implementation, this method uses asymmetrical up-count mode for the enhanced Pulse Width Modulator (ePWM) modules.

As the other methods, this one has been tested on the structure presented in subchapter 2.2.2. Figure 3-12 presents two fundamental periods of phase voltage, phase-to phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, \( V_{\alpha n} \). This voltage has a quasi – sinusoidal shape and nine levels \( \pm 400, \pm 300, \pm 200, \pm 100, 0 \), as NTV. The second waveform from this figure represents the phase-to-phase voltage, which has five voltage levels \( \pm 600, \pm 300, 0 \) as expected. The total harmonic distortion in the line voltage is 26.73 [%]. Furthermore, the CMV is presented in the third waveform. As it can be seen it has three voltage levels \( \pm 100, 0 \), with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in subchapter 5.9.

![Phase Voltage](image1.png)

![Phase-to-phase Voltage](image2.png)

![CMV](image3.png)

![DC Link Voltages](image4.png)

Figure 3-12 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for RS3N at \( m_\alpha = 1 \) - Simulation

[55]
Chapter 3 – Improved Modulation Strategies

This method has the ability to self-balance and balance the DC link in case of an external disturbance. The fourth waveform from Figure 3-12 presents the DC link voltage in natural balancing mode. The voltage on the DC link capacitors is presented in last waveform from Figure 3-9. In steady state the voltage on the upper capacitor varies between approximately 295 V and 310 V as for the lower capacitor the voltage is between 290 V and 305 V at maximum modulation index, $m_a = 1$.

The active switching frequency on each device is 2 kHz as only six transistors from a total of twelve perform a full commutation on each sampling period.

3.5. Performance Evaluation of Improved Modulation Strategies

Based on the theory and simulations results presented in this chapter, a comparative analysis has been performed between the developed modulation strategies and the classical ones.

Two of the developed modulations, ZSML and RS3N, have nine levels on the phase voltage as NTV-EHE, while OLOM has seven and OSOM five. Hence, for ZSML and RS3N the output filter requirements are as for NTV, while at OLOM and OSOM the filter needs to be increased. For a better understanding of the output filter requirements, in order to reduce the cost of the drive, the current and phase-to-phase voltage THD have been calculated. OLOM and ZSML have the current THD very similar with NTV, while ZSML present similarities with ZCM. OSOM has the largest distortion in the phase current and phase-to-phase voltage, but the modulation index is half of the other ones. ZSML and RS3N have similar harmonic distortion with NTV, at maximum modulation index, while at OLOM is slightly increased.

For a good utilization of the bus bar the modulation index needs to be taken into account as this is proportional with the DC link voltage. From this point of view OLOM, ZSML and RS3N have the best perspective, while OSOM can use only half of it.

In case of an external event that will unbalance the DC link, the modulation strategy needs to be able to counteract it as to maintain the balance. The RS3N and ZSML have this ability, while the other methods have only the ability to self-balance. Furthermore, the CMV needs to be analysed. From this point of view all the developed methods present a better performance in time domain, half of the NTV amplitude.
Table 3-1 – Comparative Analysis between Modulation Strategies

<table>
<thead>
<tr>
<th>Modulation Strategy</th>
<th>Output phase to neutral voltage levels [V]</th>
<th>Modulation Index</th>
<th>DC link balancing</th>
<th>CMV Levels [V]</th>
<th>THD&lt;sub&gt;1&lt;/sub&gt;</th>
<th>Phase to phase THD&lt;sub&gt;V&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTV</td>
<td>±400, ±300, ±200, ±100, 0</td>
<td>1</td>
<td>Natural balancing</td>
<td>±200, ±100, 0</td>
<td>0.23%</td>
<td>27.93%</td>
</tr>
<tr>
<td>ZCM</td>
<td>±300, 0</td>
<td>0.866</td>
<td>Natural balancing</td>
<td>±100, 0</td>
<td>0.56%</td>
<td>52.23%</td>
</tr>
<tr>
<td>OLOM</td>
<td>±400, ±300, ±200, 0</td>
<td>1</td>
<td>Natural balancing</td>
<td>±100, 0</td>
<td>0.30%</td>
<td>31.81%</td>
</tr>
<tr>
<td>ZSML</td>
<td>±400, ±300, ±200, ±100, 0</td>
<td>1</td>
<td>Natural balancing and balancing</td>
<td>±100, 0</td>
<td>0.28%</td>
<td>27.13%</td>
</tr>
<tr>
<td>OSOM</td>
<td>±300, ±100, 0</td>
<td>0.5</td>
<td>Natural balancing</td>
<td>±100, 0</td>
<td>0.88%</td>
<td>78.52%</td>
</tr>
<tr>
<td>RS3N</td>
<td>±400, ±300, ±200, ±100, 0</td>
<td>1</td>
<td>Natural balancing and balancing</td>
<td>±100, 0</td>
<td>0.56%</td>
<td>26.73%</td>
</tr>
</tbody>
</table>

For a better understanding of how each modulation strategy acts at different reference voltages a chart has been developed, Figure 3-13. This figure presents the THD on phase-to-phase voltage as a function of modulation index. From the developed strategies only OLOM, ZSML and RS3N have a proper utilization of the DC link.

Figure 3-13 – Modulation Index vs. Line Voltage THD of Classic and Developed Modulation Strategies based on Developed Simulation

As it can be seen from Figure 3-13 RS3N has the THD exactly the same as NTV-EHE. OSOM presents a good performance in the entire range, less than half of the distance between NTV and ZCM. At maximum modulation index ZSML and OLOM present similar performance with NTV, but when the modulation index decreases the similarity is closer to ZCM.
4. Hardware Design of three-level NPC Inverter

This chapter presents the design of the 7.5 kW NPC inverter that was built featuring newly introduced NPC leg modules from Semikron, four layer PCB for noise reduction and full protections against over temperature, overcurrent or out of range voltages on the DC link capacitors. The embedded DSP design together with a CPLD for deadtime and protection management make the inverter very customisable through software. Advanced gate drivers with extra protection add to the design performance.

4.1. System Overview

The three level NPC inverter was modelled based on the simplified hardware schematic from Figure 4-1 and has the following main features:

- Embedded TMS320F28335 DSP design.
- 4 layer Printed Circuit Board (PCB) with stacked DC link layout, ground and power planes.
- Design based on NPC leg IGBT modules.
- Adjustable over temperature, overcurrent and overvoltage protection.
- Xilinx XC9572XL CPLD based dead time and protection management.
- Real time PWM Signal analysis and protection.
- DC Link up to 1kV.
- Shielded Analog to Digital Converter (ADC) and PWM signals.
- Optocoupler galvanic isolated gate driver with active Miller clamping.
- Desaturation detection.
- JTAG interface for DSP and CPLD.
- Hall effect current sensors.
- Mixed analog and digital design.
- Reduced size.
Chapter 4 – Hardware Design

Figure 4-1 – Simplified Schematic of Hardware Platform

The developed schematic is based on two stages – control and power – which are electrically isolated from each other. In the low power, low voltage stage, the DSP supplies the six PWM signals which are a result of the implemented modulation algorithms. The PWM signals from the DSP are transmitted to the CPLD, which manages the insertion of deadtime and PWM signal multiplication. The twelve PWM signals outputs of the CPLD are used by the gate drivers in order to control the three IGBT modules that supply the three phase AC voltage to the desired load. The power input for the modules is the DC Link, a high voltage DC which is supplied with an external DC source and the bulk capacitors form the DC link.

As feedback, the three phase currents are acquired via Hall Effect sensors. Each sensor transmits the analogue signal to the DSP through the ADC. The same signals are used in order to detect an overcurrent event. The upper “OC” block, manages the phase overcurrent / short-circuit situations. The OC block consists of three window comparators that generate an active high fault signal which is transmitted to the CPLD through an AND gate (not shown).

From the DC link, using the same Hall effect sensors, two signals are acquired and used in order to detect a DC Link overcurrent or shortcircuit. The signals are processed through the lower “OC” block. The CPLD is interfaced via an AND logic gate.

The DC link voltages, corresponding to the superior and the inferior halves of the DC link, are acquired using a differential operational amplifier from Linear Technology, LT1366. The signals are fed back to the DSP via its ADC. The same signals are used in “OV” block in order to detect a DC link overvoltage or voltage out of range. The detected overvoltage is processed through an AND gate and fed to the CPLD.

Overtemperature detection is also implemented. Three thermistors are used in order to monitor the temperature on each IGBT module. For each module, the comparators detect two temperature levels. The
six resulted signals are passed thorough and AND logic gate which outputs two signals, one for each level. The two signals are passed to the CPLD. The overtemperature management is included in “OT” block.

Each gate driver outputs an active high fault signal. The twelve signals are tied on a logical AND configuration indicated by the “F” block. The resulting signal is passed to the CPLD. Another two inputs for the CPLD come from the user via two buttons, one for reset / trip and one for initialisation of modulation (not shown). The XC9572 outputs a communication signal for the DSP, marked by the letter “A”. Also, seven Light-Emitting Diodes (LED) are controlled by the CPLD in order to show current circuit state.

The DSP receives five analogue signals which are converted in numerical form by the internal ADCs. Furthermore, the six PWM signals are sent to the CPLD. The begging and ending of the modulation is controlled through the “A” pin. The RS-232 / 485 and CAN protocols for communication with other devices are also implemented.

The dotted line which passes through the gate driver block represents the electrical isolation which separates high power circuitry from the low power control stage.

### 4.2. DC Link Capacitors and Load

The DC link capacitors are used mainly to decouple the effects of the inductance from the DC voltage source. They provide a low impedance path for the ripple currents that are associated with the switching devices of the inverter. There are three main factors that influence the ripple currents: the output inductance of the load, the bus voltage and the PWM frequency of the inverter. These ripple currents are the most important in sizing the electrolytic DC link capacitors [47]. Figure 4-2 presents the structure of the DC link capacitors as developed on the experimental board.

![Figure 4-2 – DC Link Capacitors from the Developed Experimental Board](image)

These capacitors have to reduce the leakage inductance of the power bridge. The leakage inductances produces inefficiencies throughout voltage spikes when the semiconductors are switched on and off with a high $\frac{dl}{dt}$. If this inductance has a large value the switching time of the semiconductors needs to be increased in order to protect the switching devices from voltage spikes. If this solution is implemented the losses
during turn on and off increase, thus more heat is dissipated through the switching devices, hence the impedance of the DC link has to be low.

When calculating the value of the DC link capacitors the amount DC link capacitance needs to be taken into account as required for the inverter design. There are two important limitations when talking about electrolytic capacitors in the DC link: the ripple current and the voltage that these capacitors can sustain [47].

It has been highlighted that the impedance of the load influences the ripple currents in the DC link, thus for the inverter designed a 7.5 [kW] induction motor was chosen as a load. The motor has the following parameters according to [48]:

- Power: 7.5 [kW]
- Voltage: 220 V
- Poles: 6
- Type: squirrel – cage induction motor
- Stator resistance: \( R_s = 0.288 \ \Omega \) per phase
- Stator inductance: \( L_s = 0.0425 \ \frac{H}{\text{phase}} \)
- Rotor inductance: \( L_r = 0.0418 \ \frac{H}{\text{phase}} \)
- Rotor resistance: \( R_r = 0.158 \ \frac{\Omega}{\text{phase}} \)
- Mutual inductance: \( L_m = 0.0412 \ \frac{H}{\text{phase}} \)
- Inertia: \( J = 0.4 [kg \cdot m^2] \)

Taking this information into account the equivalent resistance and inductance per phase can be obtained as: \( R_e = 1.57 [\Omega] \) and \( L_e = 64.1 [mH] \). These calculations were made based on the equivalent schematic of the induction motor.

Based on equivalent impedance per phase, the peak phase current can be written as in equation (4-1).

\[
I_{\text{phase}} = \left| \frac{V_{\text{ref}}}{R_e + j\omega L_e} \right| = 17.15 [A] \tag{4-1}
\]

The three phase currents can be further modelled as in (4-2).

\[
\begin{align*}
I_a &= 17.15\sin(\theta) \\
I_b &= 17.15\sin(\theta - \frac{2\pi}{3}) \\
I_c &= 17.15\sin(\theta + \frac{2\pi}{3})
\end{align*} \tag{4-2}
\]

The only influence in the neutral point is due to small and medium vectors. For maximum modulation index, the reference vector lies in region 3 or 4. If the reference vector lies in region 3, the dwell times for chosen vectors are the one in Table 2-4. Given that only the small and medium vector influences the neutral point, and that in the region 3, the dwell times of small vectors is equally split between N and P state, the RMS value of the NP current for half sector is:
\[ I_{np} = \sqrt{\frac{6}{\pi} \int_0^{\frac{\pi}{6}} \left( \frac{T_b}{T_s} \right)^2 d\theta} = \sqrt{\frac{6}{\pi} \int_0^{\frac{\pi}{6}} \left( 17.15 \sin(\theta) - \frac{2\pi}{3} \sqrt{2m_a \sin^2 \theta} \right)^2 d\theta} = 12 [A] \quad (4-3) \]

Given the neutral point current, the capacitor current can be written as:

\[ I_c = C \frac{dU_C}{dt} \quad (4-4) \]

The total DC link capacitance results as:

\[ C_{total} = \frac{I_c dt}{dU_C} \quad (4-5) \]

For a maximum voltage change of 2 V at 4 kHz switching frequency, the needed capacitance results as 1.5 mF. Given the neutral point current ripple and the needed capacitance, the DC link was modelled using 6 capacitors of 330 µF, each supporting up to 3 A rms current ripple at 450 V. The Panasonic capacitor chosen feature reduced size and 85 °C endurance. Each half of the DC link consists of 3 parallel connected capacitors as seen in Figure 4-3. The total supported current ripple is 18 A\textsubscript{rms} and the equivalent capacitance is 1.98 mF.

![Figure 4-3 – DC Link Configuration Used](image)

### 4.3. Switching

As mentioned earlier, for switching, three NPC IGBT leg modules from Semikron were chosen. The Semitop 3 series module, Figure 4-4, SK50MLI065 features the following [49]:

[63]
- 600 V / 54 A per IGBT
- Compact design
- One screw mounting
- Snubberless design
- Heat transfer and isolation through Direct Copper Bonded aluminium oxide ceramic (DCB)
- Ultra-fast Non Punch Through (NPT) IGBT technology
- Controlled Axial Lifetime (CAL) technology for freewheeling diodes [50]

Figure 4-4 – One NPC Leg IGBT Module [49]

The advantage of using modules is that they are designed with special consideration for the commutation paths [51]. Large commutation paths would make the circuit prone to high stray inductance. The chosen Semikron modules are designed to minimise the stray inductance problem [51].

The CAL technology used for the freewheeling diodes is able to provide 30% more current compared with previous generations. The technology features high power density and high thermal stability and reliability [50]. The IGBT leg configuration is shown in Figure 4-5:

- 4 N-channel IGBTs: $T_1 - T_4$
- 4 freewheeling diodes: $D_1 - D_4$
- 2 clamping diodes: $D_5 - D_6$

Figure 4-5 – Internal NPC Module Schematic

The gate switching times as a function of gate resistor $R_G$, extracted from IGBTs datasheet, is shown in Figure 4-26. Based on this characteristic, in order to have a fall time of 20 ns and a rise time of 25 ns, the value for $R_G$ was chosen to be 20.1 Ω. The switch on delay results as 60 ns and the switch off delay as 300 ns. The switch off delay is the main reason for the chosen value.
Given a dead time of 1.5 $\mu$s, the switching frequency has to be chosen so that the dead time represents only a small fraction of the switching period (calculated in subchapter 4.7). Considering maximum 1% dead time [52], the maximum switching frequency preferred is:

$$\frac{1}{100 \cdot dt} = \frac{1}{100 \cdot 1.5 \cdot 10^{-6}} = 6.67 \text{ kHz}$$  \hspace{1cm} (4-6)

Given that the DSP main code run time for the NTV modulation is approximately 0.1 $\mu$s and considering that the whole code should run at least twice after each interrupt, the preferred frequency considering the update of the main code inside the 150 MHz DSP of 2.5 times is:

$$\frac{1}{0.1 \cdot 10^{-6} \cdot 2.5} = 4 \text{ kHz}$$  \hspace{1cm} (4-7)

Based on this, the 4 kHz frequency was used both in the simulations and experiments.

4.4. Gate Drivers and Protections

4.4.1. Gate Drivers

When choosing a gate driver, high interest was focused on a solution which would integrate both optocoupler isolation and protection on a single Integrated Circuit (IC). Avago ACPL-332j, Figure 4-7, was chosen due to its features such as [53]:

[65]
Chapter 4 – Hardware Design

- Desaturation detection
- Active Miller Clamping
- Isolated Fault feedback
- “Soft” IGBT turn-off
- Under Voltage Lock-Out
- Small package – Small Outline Integrated Circuit SOIC-16
- 50 kV/μs Common Mode Rejection (CMR) at VCM = 1500 V
- 2.5 A output current

Figure 4-7 – Avago ACPL-332j Gate Driver [54]

The gate driver has an optically isolated power stage capable of driving IGBTs with up to 150 A and 1200 V [53]. Under normal operation, the output voltage at pin 11 is controlled by the input LED PWM signals. At the same time, the $V_{CE}$ voltage is monitored. The fault output is active high.

When the voltage on the desaturation pin 14 exceeds 6.5 V while the switching devices are on, the output voltage is “softly” turned off in order to avoid large $di/dt$ voltages [53]. At the same time, the fault output is brought low. During “soft” turn-off, all input signal are ignored and the output is shut down for at least 5 $\mu$s. The output of the gate driver is a combination of LED PWM input, Under Voltage Lock-Out (UVLO) and desaturation detection.

Figure 4-8 – ACPL-332j Circuit Application

The gate driver is used based on the recommended application circuit from Avago datasheet. The implementation for driving the third transistor from leg A is shown in Figure 4-8.

The circuit is powered through the floating isolated dual DC-DC converter DCDC8 from Murata (NMK1212SC). The converter is floating with respect to IGBT emitter voltage. The input voltage is $+12 \, V_{DC}$.
between pin 1 and 2. The output voltage between pin 5 an 7 is 24 $V_{DC}$. This 2 Watt converter was chosen for the physical form, being rectangular instead of a square, as the other single output 24 $V_{DC}$ DC-DC converters were. The physical form helps in designing a reduced size inverter. Also, if features 3 kV isolation. Two Schottky diodes, B0530W from Taiwan Semiconductor are tied between pins 5-6 and 6-7. The two diodes are used in order to prevent converter damage from reverse current [55].

For obtaining the required 18 V for supplying the power part of the gate driver, the L78S18CV voltage regulator from ST Microelectronics is used. The regulator features 2 A current capability, thermal overload protection and shortcircuit protection [56]. The 0.33 $\mu F$ electrolytic capacitor is used for input filtering and the 10 $\mu F$ electrolytic capacitor is used for improving regulator transient response [56] and for supplying high currents needed during transient switching for the IGBT. The TESTR8 resistor is used for debugging purposes.

The Avago ACPL-332j gate driver is formed by two circuits optically separated. The primary input voltage is 3.3 $V_{DC}$ and the secondary input voltage is 18 $V_{DC}$. The 3.3 $V_{DC}$ is supplied to the pins 2, 6 and 7. Because the signal coming from the CPLD is passed through an inverting buffer, the PWM signal is connected to pin 5 and 8 (cathode) while the anode (pins 6-7) is kept a 3.3 $V_{DC}$ potential. The 330 $\Omega$ resistor used limits the input LED current to recommended 10 mA. The low power ground is connected to pins 1 and 4.

The fault signal is transmitted through a LED (pins 5-8). A 0.471 k$\Omega$ pull-up resistor (not shown) is used after the logical AND connection of the twelve fault signals. The 1000 pF capacitor on each fault output is used for filtering. C1_08, a 0.1 $\mu F$ capacitor is used for bypassing and circuit decouplings. The values chosen are the ones recommended by the datasheet.

In the secondary part of the gate driver circuit, 18 $V_{DC}$ is supplied to pin 13. The power ground (which is the IGBT emitter) is connected to pins 9, 12 and 16. Another 0.1 $\mu F$ capacitor is used for decoupling. CBLNK_08, D_08, 35 ns diode from Taiwan Semiconductor and the 100 $\Omega$ resistor, are required for fault detection. The 0 $\Omega$ resistor is used as a simple jumper. The parallel connection of the 10 $V_{DC}$ Zener diode and the 0.5 A Schottky (On Semiconductor) diodes to pins 14 and 16, is used for improving desaturation detection by avoiding false triggering which could happen when the gate driver substrate diode is forward biased. This can happen when the negative voltage spikes due to freewheeling IGBT diode bring the desaturation pin below ground. The Schottky prevents the substrate diode from being forward biased and the Zenner diode prevents positive transient voltage to affect the desaturation pin.

The fast recovery, 35 ns diode is used in order to deny reverse recovery spikes on forwarding the gate driver substrate diode which would lead to false fault detection. The 100 $\Omega$ resistor is used to limit the current which could appear due to a negative voltage spike on the desaturation, pin 14. The negative voltage spike can happen when the IGBT anti-parallel diode has a large instantaneous voltage transient [57].

The parallel 40.2 $\Omega$ resistors from Te Connectivity are 0.1% precision, 0.5 W power devices used as IGBT gate resistors with an equivalent resistance of 20.1 $\Omega$. The resistor limits the gate charge and collector rise and fall times. The value is chosen based on IGBTs characteristics [49] from Figure 4-6. The 47 $k\Omega$ resistor is used for pull-down in order to benefit a predictable high level output voltage.

Power dissipation in the gate resistors needs to be checked. Based on [58] the peak power dissipation in the gate resistor can be calculated using (4-8) resulting as 16.119 W.
The RMS current is the value that needs to be considered. Based on (4-8), the power dissipation in the gate resistor for a 4 kHz switching frequency is 1.07 [mW]:

\[
P_g = 2I_{RMS}^2 R_g
\]  

(4-9)

The RMS gate current is obtained considering a triangle pulse derivation during turn-on time:

\[
I_{RMS} = I_{peak} \sqrt{\frac{tp}{3}}
\]  

(4-10)

**Under Voltage Lockout** [53]

The under voltage lockout prevents the application of insufficient voltage in the gate of the IGBT by forcing the output of the gate driver to be low by clamping it. When the \( V_{CC2} \) (pin 13) goes above \( V_{UVLO+} \) (positive threshold) the UVLO clamp is released and the gate driver will respond to input PWM signals. During the increase of \( V_{CC2} \) from 0 V, the first function which becomes active is the desaturation function. UVLO has an integrated hysteresis for improved noise immunity [57].

**Active Miller Clamping** [59]

A serious problem when driving IGBTs is the parasitic turn-on. This arises due to the Miller capacitor between gate and collector. During turn-off, a high dv/dt transient could induce a parasitic turn-on which could destroy the power converter. A current flowing through the parasitic Miller capacitor, gate resistor and gate driver internal resistor can create a voltage drop on the gate resistor. If the voltage drop is higher than the IGBT threshold, the parasitic turn-on will occur. Also, gate threshold is reduced by chip temperature increase.

The Miller current can be derived as:

\[
I_{CG} = C_{CG} \frac{dV_{CE}}{dt}
\]  

(4-11)

In equation (4-11), the \( C_{CG} \) is the Miller capacitor, \( I_{CG} \) is the Miller current and \( V_{CE} \) is the IGBT collector-emitter voltage. This effect can be seen of both switching devices of a half – bridge configuration. The Miller capacitance can be seen in Figure 4-9.
The classical solution for dealing with Miller capacitor is the use of an additional gate-emitter capacitor to shunt the Miller current or the use of a negative power supply in order to increase the threshold voltage for the IGBT. First method suffers from efficiency loss and the second from the increased cost by the use of a negative power supply.

Another solution would be the shorting of gate-emitter path through the help of an additional transistor between gate and emitter. The currents across Miller capacitance are shunted by this transistor and will not flow through the output gate driver pin 11. The gate clamp is activated when, during turn-off, the gate voltage goes below 2 V.

**“Soft” Turn-off Feature [60]**

When short-circuit or overcurrent events occur, the soft turn-off feature helps by improving the designed application reliability. Soft turn-off means that the gate driver output voltage is brought low softly in order to reduce overvoltage spikes caused by lead wire inductances.

This feature is a process which occurs in two stages. The ACPL-332J features two pull-down devices, a weak one (Doubled Diffused Metal Oxide Semiconductor – DMOS) and a larger (fifty times) DMOS transistor. In the first stage, the weak pull-down device will slowly discharge the IGBT. During turn-off the large DMOS remains off until the gate voltage output goes below $V_{EE} + 2$ V. This is the time the large DMOS will clamp the gate voltage to $V_{EE}$.

**Desaturation Detection [57]**

Desaturation detection and protection are used to ensure the safety operation of IGBTs in short-circuit condition. Desaturation can also occur due to other reasons such as driver supply voltage problems or insufficient driver gate signal. Human error and supply rail short-circuits can cause high power dissipation in the switching devices which lead to device destruction by overheat. The desaturation protection works by monitoring the collector-emitter voltage, $V_{CE}$. When a high current of a short-circuit occurs, the voltage will rise. The gate driver detects and triggers a fault when the collector-emitter voltage rises above the internal gate driver desaturation voltage threshold, 6.5 V. When the fault is triggered, the IGBT is “softly” turned off and the fault output is brought low.
While the IGBT is in off state, the fault detection is disabled in order to prevent false triggering. Also, the desaturation fault detection has to be disabled for a small amount of time after the IGBT is turned on in order to allow the $V_{CE}$ voltage to fall below the internal desaturation threshold. The blanking time is controlled by the internal desaturation charge current of 250 $\mu A$, the desaturation threshold and the external blanking capacitor. The blanking time is calculated using equation (4-12):

$$t_{\text{blank}} = \frac{C_{\text{blank}} V_{\text{desat}}}{I_{\text{chg}}}$$  \hspace{1cm} (4-12)

With the recommended 100 pF capacitor, the resulting blanking time is 2.6 $\mu$s.

Gate driver fault management, as a combination of LED current $I_F$, UVLO and desaturation function is shown in Table 4-1:

<table>
<thead>
<tr>
<th>$I_F$</th>
<th>UVLO ($V_{CC2} - V_F$)</th>
<th>DESAT Function</th>
<th>FAULT Output</th>
<th>$V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>On</td>
<td>Active</td>
<td>Inactive</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>On</td>
<td>Inactive</td>
<td>Active (desaturation fault)</td>
<td>Low (fault)</td>
<td>Low</td>
</tr>
<tr>
<td>On</td>
<td>Inactive</td>
<td>Active (no fault)</td>
<td>High (no fault)</td>
<td>High</td>
</tr>
<tr>
<td>Off</td>
<td>Active</td>
<td>Inactive</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Off</td>
<td>Inactive</td>
<td>Inactive</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

### 4.4.2. Signal Acquisition

To assure that the inverter is working in its safe operating area and that in case of a fault, no hardware destruction occur, different types of hardware protection must be considered. The protections implemented for the proposed design are:

- Phase overcurrent / short-circuit protection
- DC Link overcurrent / short-circuit protection
- DC Link overvoltage / out of range protection and detection
- Over temperature protection
- Integrated gate driver protection

In order to implement these protections, essential measurements have to be made. The phase currents and the DC link currents are measured with Allegro ACS756 Hall Effect based current sensor. The DC link voltages are measured by means of Linear Technology LT1366 differential amplifier. Temperatures are measured using AVX NJ28 Negative Temperature Coefficient (NTC) thermistor.

Currents and voltages have been passed through the TLC372 voltage comparators used in a window configuration. The temperature signals are compared with two levels. All signals are passed through AND gates and then supplied to the CPLD. The CPLD will further stop the modulation in case of a fault and output the fault condition through LEDs. All fault management is performed through the CPLD.
Allegro ACS756 Hall Effect IC sensor is a precise and economical solution for current sensing in AC and DC. The low-offset linear Hall circuit converts the current flowing through the conductive path and generates proportional magnetic field which is then converted into a voltage signal. The obtained voltage is precise due to low-offset chopper stabilised IC. The Allegro ACS756, shown in Figure 4-10, benefits from the following features:

- Industry-leading noise performance
- Total output error 0.8%
- Monolithic Hall IC
- Ultra-low power loss: 130 μΩ conductor resistance
- 3 kV RMS minimum isolation
- Nearly zero magnetic hysteresis
- Small package size
- Measurement of ±50 A
- Chopper stabilisation technique

The current sensors are used in the configuration shown in Figure 4-11 for both phase current acquisition and DC link current acquisition. The shown example from Figure 4-11 is for phase A. The 0.1 μF capacitor is used for bypassing and the 100 pF capacitor is recommended for filtering. The current path is through pins 4 and 5. The 5 V\text{DC} analogue supply voltage is connected to pins 1-2. The output voltage signal is yielded at pin 3. The SNS\_CRTx (where x=1:3) signal outputs have a value of 2.5 V\text{DC} for 0 A and ±40 mV/A characteristic.

For a correct ADC interface, the 2.5 V\text{DC} for 0 A has to be brought to about 1.5 V\text{DC}. This is performed through a divider on each SNS\_CRTx signal (where x=1:3), like in Figure 4-12. The resulting signal, SNS\_CRTxA (where x=1:3) has a value of:

\[
SNS\_CRTxA = \frac{RDIVA1 \cdot SNS\_CRTx}{RDIVA1 + RDIV2} = \frac{20 \cdot 10^3 \cdot SNS\_CRTx}{30 \cdot 10^3} = 0.6666 \cdot SNS\_CRTx
\]

The SNS\_CRTxA signal could be written as a function of measured current, equation (4-15).
\[ SNS_{CRTxA} = k_{cs} I_{SNS} \]  

(4-14)

Where \( k_{cs} \) is defined as in equation (4-15).

\[ k_{cs} = \frac{RDIVA1 \cdot (40 \cdot 10^{-3} \cdot I_{meas} + 2.5)}{RDIVA1 + RDIVA2} \]  

(4-15)

For a current of 0 A through the sensor, \( SNS_{CRTxA} \) will have a value of 1.666 \( V_{DC} \). The ±40 mV/A characteristic is also changed by the divider based on equation (4-13) to ±26.666 mV/A. The \( SNS_{CRTx} \) signals are passed to the window comparators and the \( SNS_{CRTxA} \) signals are supplied to the ADC through voltage followers (buffers).

**Voltage Signal Acquisition**

An effective and economical solution for acquirement of voltage signals is the use of a differential operational amplifier connected to the DC Link through high value resistors. The resistor network used is composed of four High Voltage Direct Current (HVDC) connections through three series resistors (470k+470k+560k). The series connection of the resistors ensures that the connection to the DC link will not fail, as the current is small compared to resistors current capability.

The operational amplifier chosen is Linear Technology LT1366. The application of LT1366 is shown in Figure 4-13. The choice was made for the features that this amplifier benefits of:

- Input common mode range includes both rails
- Output swing rail-to-rail
- Low offset voltage
- High Common Mode Rejection Ratio – 90dB
- Power Supply Rejection Ration – 105 dB
- Low input bias current – 10nA
- Low supply current
- 400 kHz gain bandwidth
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The LT1366 is a dual operational amplifier supplied by a dual \( \pm 12 \, V_{DC} \) isolated DC-DC converter (NMK1212SC from Murata). A voltage of \( +12 \, V_{DC} \) is supplied at pin 8 and \( -12 \, V_{DC} \) at pin 4. Both pins are bypassed by a 0.1 \( \mu F \) capacitor. The DC-DC converter is bypassed by two 10 \( \mu F \) electrolytic capacitors, one between pins 5-6 and the other between pins 6-7. Resistors TESTVa and TESTVb are for debugging purposes.

The inputs of each comparator are protected from DC link voltage transients through a pair of antiparallel small signal diodes (TS148 from Taiwan Semiconductor). As said earlier, the high voltage signal is passed through four series of three resistors with an equivalent resistance of 1.5 \( \Omega \). The 100 \( \mu F \) capacitor on both non-inverting inputs forms with the resistors a low-pass filter. The cut-off filter frequency results as in (4-16) where \( R=1.5 \, \Omega \) and \( C=100 \, \mu F \).

\[
f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 1.5 \cdot 10^6 \cdot 100 \cdot 10^{-12}} = 1.06 \, kHz
\]  

(4-16)

The transfer function of each operational amplifier, configured as a differential amplifier, is derived as an example for first amplifier as in equation (4-17). In the normal operating condition, \( +HVDC=300 \, V \), \( 0HDVC=0 \, V \) and \( -HVDC=-300 \, V \). The second output can be calculated in the same manner, equation (4-18).

\[
V_{1out} = \frac{RSA4}{RSA1 + RSA2 + RSA3} (+HVDC - 0HVDC) = \frac{30 \cdot 10^3}{1.5 \cdot 10^6} (300 - 0) = 6 \, V_{DC}
\]  

(4-17)

\[
V_{1out} = \frac{RSC1}{RSC2 + RSC3 + RSC4} (0HVDC - -HVDC) = \frac{30 \cdot 10^3}{1.5 \cdot 10^6} (0 - -300) = 6 \, V_{DC}
\]  

(4-18)

Both 6 \( V_{DC} \) outputs are passed through a voltage divider in order to obtain \( \sim 1.5 \, V_{DC} \). The VSISO1 and VSISO2 voltages will have for 300 \( V_{DC} \) an output of:
Chapter 4 – Hardware Design

\[
VSISO_1 = VSISO_2 = \frac{RVD_1}{RVD_1 + RVD_2} \cdot 6 = \frac{RVD_3}{RVD_3 + RVD_4} \cdot 6 = \frac{6.8 \cdot 10^3}{26.8 \cdot 10^3} \cdot 6 = 1.522 V_{DC}
\] (4-19)

Combining (4-17), (4-18) and (4-19), the VSISOx (where \(x=1,2\)) could be written as:

\[
VSISOx = k_{VS} \cdot HVDC2
\] (4-20)

Where:

\[
k_{VS} = \frac{RSA4 \cdot RVD1}{(RSA1 + RSA2 + RSA3)(RVD1 + RVD2)} = 0.0050733
\] (4-21)

The VSISOx signals are passed through the window comparators and then to the ADC through operational amplifier voltage followers (buffers).

Temperature Signal Acquisition

The temperature is acquired using NJ28 high accuracy thermistors from AVX. The thermistors have a resistance of 100 \(k\Omega\) at 25 \(^\circ\)C, which decreases with the temperature increase – thus having a NTC characteristic. Temperature acquirement setup is shown in Figure 4-14:

![Figure 4-14 – NJ28 Temperature Acquisition](image)

Each thermistor, RTx (\(x=1:3\)) is connected in parallel with a 22 \(k\Omega\) resistor and the resulted value signal is passed through a voltage divider in order to modify the NJ28 characteristic. They are supplied with 5 \(V_{DC}\).

The output voltage of the thermistors becomes (example shown for RT1), equation (4-22):

\[
THERM1 = \frac{RS1 \cdot 5}{RS1 + \left(\frac{RP1 \cdot RT1}{RP1 + RT1}\right)}
\] (4-22)

THERM1 values for important temperatures are shown in Table 4-2, calculated using (4-22).

<table>
<thead>
<tr>
<th>Degree Celsius</th>
<th>RT1 Value (k\Omega) [62]</th>
<th>THERM1 Output (V_{DC})</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>100</td>
<td>1.0337</td>
</tr>
<tr>
<td>70</td>
<td>14.83</td>
<td>1.4994</td>
</tr>
<tr>
<td>75</td>
<td>12.28</td>
<td>1.6106</td>
</tr>
<tr>
<td>80</td>
<td>10.22</td>
<td>1.7332</td>
</tr>
<tr>
<td>85</td>
<td>8.537</td>
<td>1.8679</td>
</tr>
</tbody>
</table>

[74]
The THERMx signals are compared with two pre-settable values and the result is passed to the CPLD through logical AND gates.

**Signal Processing Through Windows Comparators**

The TLC372 from Texas Instruments was chose due to following features [63]:

- Fast response time: 200 ns typical
- Low supply current drain: 150 µA at 5 $V_{DC}$
- High input impedance: $10^{12} \, \Omega$

The voltage signals corresponding to phase currents, DC link currents and DC link voltages are passed through windows comparators with an active high output [64] when the signal is in the window limits. The TLC372 [63] voltage comparator from Texas Instruments features two comparator per each IC, which are connected in a window configuration as shown in Figure 4-15 (example for phase A current):

![Figure 4-15 – Window Comparator Configuration](image)

The comparator IC is supplied with 5 $V_{DC}$ at pin 8 and bypassed with a 0.1 µF capacitor. The signal to be compared is fed to pin 2 (inverting input for first comparator) and pin 5 (non-inverting input for the second comparator). The “window” is formed by the reference voltages supplied at pins 3 and 6. The high reference is supplied at the non-inverting input pin 3 and the low reference to the inverting pin 6. The high reference is always greater than the low reference voltage. Each voltage reference is obtained by means of a voltage divider between a potentiometer, configured as a variable resistor and a fixed 20 $k\Omega$ resistor. The output signal is the union of first comparator output from pin 1 and the second comparator output from pin 7. The signal is pulled up through a 10 $k\Omega$ resistor. Signals should not go above the maximum common mode input voltage of 3.5 $V_{DC}$.

When the input signal voltage is between the two references, the output will be high and low when the input signal is out of the voltage window from Figure 4-16. The output signal is the thick dashed line and the input is the thin arrow-ended line.
4.4.3. Protection Adjustment

The phase overcurrent and DC link overcurrent protection should be adjustable in ±50 $A$ range. The input signal for the window comparators is $1.666 \ V_{DC}$ for 0 $A$ and the sensitivity is ±26.666 $mV / A$. The output voltage, using (4-14), will be $2.9993 \ V_{DC}$ at +50 $A$ and $0.3327 \ V_{DC}$ at -50 $A$. Based on these values, the potentiometers for high reference voltage and the one for low reference voltage can be chosen. For the low reference value a potentiometer of 20 $k\Omega$ was chosen, and for the high reference value a potentiometer of 200 $k\Omega$. The choice is viable for both phase overcurrent protection as for DC link overcurrent protection.

The over temperature protection should have two pre-settable levels. First level should be settable up to 70°C and the second level should be settable up to 80°C. For both levels one potentiometer with the value of 100 $k\Omega$ was chosen.

The DC link voltages should be settable to deviate up to ±10% of the DC link voltage. At 300 $V_{DC}$, the output of the voltage sensing is 1.522 $V_{DC}$. For 330 $V_{DC}$, the output signal will be 1.674 $V_{DC}$ and for 270 $V_{DC}$ will be 1.37 $V_{DC}$. For the low voltage reference a 10 $k\Omega$ potentiometer is chosen and a 20 $k\Omega$ potentiometer for the high voltage reference.

For management and further fault notification, two SN75F21D AND logical gates from Texas Instruments are used. Each IC contains three AND logical gates with three input each. The choice was made due to $3.2 \ ns$ fast switching times [65]. Each gate is decoupled by a 0.1 $\mu F$ capacitor. Through these gates, the outputs of the three window comparator for phase overcurrent detection are merged into a single signal informing about a fault condition regarding the current on one of the phases. The operation is logical AND because the fault signals are active high. Furthermore, the signal is supplied to the CPLD.

The output of the six comparators used for over temperature detection are merged through the AND gates in order to have two fault signals – one representing the first temperature level threshold and another representing the second temperature threshold. These two signals are also supplied to the CPLD.

The two outputs regarding DC link overvoltage are also merged through the AND gates into a single signal. The DC link overcurrent conditions are performed in the same manner. The gate drivers fault signals are tied in a wired AND connection. The final fault signals supplied to the CPLD are:
Chapter 4 – Hardware Design

- OT_A - which will switch low when one of the temperature of the IGBT modules will go above first threshold level
- OT_B - which will switch low when IGBTs temperature goes above second threshold level
- DC_OV - will switch low when there is an overvoltage on one of the DC link halves
- DC_OC - will switch low if there is an overcurrent condition on the two DC link halves
- OCR - which switches low if a overcurrent condition occurs on any of the three phases
- FAULT_GDX - which will be low if any of the twelve gate drivers encounters a fault

The three phase currents and the two DC link voltages are transmitted to the ADC block of the DSP. The interfacing is made through five operational amplifiers configured as voltage followers. The chosen amplifier is also recommended by Texas Instruments – OPA234, the manufacturer of the DSP. These are chosen due to features such as rail-to-rail input/output, low noise and low quiescent current [66]. The voltage follower configuration is shown in Figure 4-17 for the signals corresponding to the currents on two phases. The configuration used is the same for the other signals.

Each OPA2343 IC contains two operational amplifiers. The IC is supplied with 3.3 $V_{DC}$ from the analog supply. The 0.1 $\mu F$ capacitor on pin 8 is used for bypassing. The 100 $\Omega$ resistor and the 0.1 $uF$ capacitor on the outputs of each operational amplifier are used as a low-pass filter for ADC input. Other scope of the two components is to be used as a flywheel for the currents pulses created by the ADC’s input circuitry [67]. The resulted filter cut-off frequency is 15.91 $kHz$, calculated using (4-16).

The buffer input signals and the ADC input signals are protected from going over 3.3 $V_{DC}$ or below ground potential using a pair of dual series small signal Schottky diodes (BAT54S) from ST Microelectronics, Figure 4-17. The chosen solution is made due to low conduction and reverse losses, low forward and reverse recovery times, low capacitance and extreme fast switching (8 ns) [68].

![Figure 4-17 – OPA2343 Buffer Solution](image)

4.4.4. Voltage Supply and Regulators

The developed PCB is divided in two main areas: HVDC area and low voltage – control area. The HVDC is supplied through an external power supply. For the control area, a 12 $V_{DC}$ also must be supplied externally.

The low voltage area has three parts: analog, digital and isolated communications area. For this purpose, three isolated DC-DC converters from Traco Power (TEL3-1211) are used. These converters feature high...
efficiency, 1.5 \( kV \) isolation, and short-circuit protection and regulated 5 \( V_{DC} \) output. Power supplied is up to 3 W [69]. The output of each DC-DC converter is decoupled by a 33 \( \mu F \) capacitor.

In order to obtain 3.3 \( V_{DC} \), the Texas Instruments TPS79533 regulator was chosen due to its features:

- 500 mA low dropout regulator
- Ultralow noise
- 50 \( \mu s \) start-up
- Very low dropout voltage, 110 \( mV \) at full load
- High Power Supply Rejection Ratio (PSRR)
- Internal current limiting and thermal protection

The application of TPS79533 is shown in Figure 4-18. The datasheet [70] recommends a 2.2 \( \mu F \) filtering capacitor near the input of the regulator – pins 1 and 2. The output capacitor, used to stabilize the internal control loop is chosen to be 2.2 \( \mu F \) and connected between pin 4 and 6. The 0.01 \( \mu F \) capacitor is user for bypassing the NR pin. Together with the internal 250 \( k\Omega \) resistor, a low pass filter is created for the internal voltage reference.

Three 3.3 \( V_{DC} \) regulators are used on the board design. The given example, Figure 4-18, is for obtaining desired voltage level for powering digital circuitry. The other two regulators supply 3.3 \( V_{DC} \) to analog circuitry and isolated communication circuitry. Their usage is the same as given in Figure 4-18.

In Table 4-3 the low voltage sequencing is shown. Each voltage type has its own ground and power planes. The analogue and digital grounds meet near the DSP.

<table>
<thead>
<tr>
<th>Type</th>
<th>Voltage Levels ([V_{DC}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>12</td>
</tr>
<tr>
<td>Isolated</td>
<td>3.3 5</td>
</tr>
<tr>
<td>Analog</td>
<td>-12 3.3 5 12</td>
</tr>
<tr>
<td>Digital</td>
<td>3.3 5</td>
</tr>
<tr>
<td>Floating</td>
<td>-12 12 18 24</td>
</tr>
</tbody>
</table>

---

[78]
4.4.5. Communication

The DSP can communicate with external CPUs through the CAN or RS-232 / 485 protocols. Hardware implementation for CAN and RS-232 / 485 is shown in Figure 4-26. Through the D_Isolator1, signals needed for RS-485 communication are isolated. Furthermore, the CAN signal isolation is obtained through the D_Isolator2. The digital isolator chosen is the ISO7221 from Texas Instruments, featuring up to 150 Mbps signalling rate, low Pulse Width Distortion (PWD), low jitter (1 ns), 4 kV isolation and high electromagnetic immunity [71].

The digital isolators are powered with 3.3 $V_{DC}$ from the digital supply on the PCB side and with 5 $V_{DC}$ from isolated supply for the output side. Both are decoupled by a 0.1 $\mu F$ capacitor. The 0 $\Omega$ resistor on pin 6 of the D_Isolator1 is to be soldered only if RS-485 is going to be used. The input of the D_Isolator1 is formed by RXB and TXB signals coming from the DSP. The D_isolator2 input is composed of CAN_RXA and CAN_TXA also coming from the DSP. All digital isolator input signals are pulled-up with a 10 $k\Omega$ resistor.

The signals for RS-485 communication are passed through SN75LBC176 differential bus transceiver from Texas Instruments, featuring bidirectional transmission, high speed, low skew, current limiting and thermal shutdown protection [72]. The IC is supplied with 5 $V_{DC}$ from the isolated supply and bypassed with 0.1 $\mu F$ capacitor. The driver and the receiver enable pins 2 and 3, RE and DE, connected to the 5 $V_{DC}$ supply (DE pin) and ground (RE pin). A and B are the driver outputs and R is the receiver output. The jumper J1 is used to enable or disable the 120 $\Omega$ termination resistor.

The output of the transceiver together with the RXA_ISO and TXA_ISO are received from the DSP and are interfaced through a serial DE-9 connector. RXA_ISO and TXA_ISO are connector to pins 2 and 3 of the RS-232 communication. Pins 4-8 and 5-9 are used for RS-485 communication [73].

The CAN signals are passed through SN65HVD1050 CAN transceiver from Texas Instruments. It features high electromagnetic immunity, low electromagnetic emissions and bus fault protection [74]. The IC is supplied with isolated 5 $V_{DC}$ and bypassed with 0.1 $\mu F$ capacitor. The J2 jumper is used to enable or disable the 120 $\Omega$
resistor termination. The output signals are transmitted to the outside world through another DE-9 connector, that has pins 2 and 7 used for data [75].

4.5. Power Tracks Sizing

The current carrying capability of the PCB has to be calculated prior to the board manufacture. The maximum current is proportional to the cross-sectional area of the tracks. The copper thickness is 70 µm. Given the minimum width of the DC link track as 6.73 mm and of the phase track as 10.5 mm, the maximum current [76] can be calculated as in equation (4-23).

\[
I = k \Delta T^{0.44} A^{0.725} \tag{4-23}
\]

Where \( I \) is the current in amperes, \( A \) is the cross section in square mills and \( \Delta T \) is the temperature rise in Celsius degree between ambient temperature and the safe operating temperature of the PCB [76]. The constant \( k \) is defined as \( k=0.048 \) for outer layers and \( k=0.024 \) for inner layers. Knowing that 1 mil = 0.0254 mm, the equation (4-23) can be modified to be used with the metric units, thus resulting equation (4-24).

\[
I = k \Delta T^{0.44} \left( \frac{A}{0.0254^2} \right)^{0.725} \tag{4-24}
\]

Using equation (4-24), the current carrying capability of the DC link, for a temperature rise of 55 °C, results as 33 A for outer layers and 17 A for inner layers. For the same temperature rise, the phase current for inner layers results as 23 A for inner layers and 46 A for outer layers. The above calculation is validated through thermal imaging in subchapter 4.8.

4.6. Cooling

An important role is hold by maximum electrical ratings and thermal limitations of semiconductor devices. There needs to be taken into account that the operating junction temperature of all devices does not exceed the limits under all specified conditions [77]. The Semikron modules have high thermal performance and integrate latest silicon technology, thus the result has high efficiency and cost effectiveness. These modules are used for PCB soldering, Figure 4-20. A single mounting screw and the copper baseplate are used in order to ensure thermal performance [78].
The inverter designed in this thesis has a power rating of 8 [kW] at a frequency of 4[Hz]. Semikron offers an application note for loss calculation [51]. The analytical method presented in this application note is based on [79]. The cross-sectional view of a typical Semikron IGBT package can be seen in Figure 4-21.

\[ P_{\text{cond}} = \frac{M I}{12\pi} [3 V_{ce0}((\pi - \varphi) \cos \varphi + \sin \varphi) + 2 r_{ce} I [1 + \cos \varphi]^2] \]  

Where:

- \( M \) – Modulation index
- \( I \) – Peak value of current
- \( V_{ce0} \) – IGBT forward threshold voltage
- \( \varphi \) – Conduction angle
- \( r_{ce} \) – IGBT on-state slope resistance
For a proper calculation regarding the thermal resistance of the heatsink NTV-EHE modulation strategy was taken into account. As a load, for thermal calculations, an induction motor with the power rating of 8 [kW], peak current of 19.2 [A], power factor of 0.85 and a voltage of 400 [V] was considered. Considering these informations the conduction angle was calculated and it has a value of 0.554.

The switching losses for transistors T1 and T4 are calculated as in equation (4-26).

\[
P_{sw} = f_{sw} E_{sw} \left( \frac{I}{I_{ref}} \right)^{K_1} \left( \frac{V_{cc}}{V_{ref}} \right)^{K_2} \left( \frac{1}{2\pi} \left[ 1 + \cos \varphi \right] \right)^{1-K_1} G_t
\]

(4-26)

Where:

- \(f_{sw}\) – Switching frequency
- \(E_{sw}\) – Sum of energy dissipation during turn – on and turn – off time
- \(K_1\) – Exponent for the current dependency of the switching losses
- \(I_{ref}\) – Reference current value of the switching loss measurement
- \(K_2\) – Exponent for the voltage dependency of the switching losses
- \(V_{cc}\) – Collector – emitter supply voltage
- \(V_{ref}\) – Reference voltage value of the switching loss measurement
- \(G_t\) – Adaptation factor for the non – linear semiconductor characteristics

Conduction losses for transistors T2 and T3 are calculated based on (4-27).

\[
P_{cond} = \frac{I}{12\pi} \left[ V_{ce0} \left[ 12 + 3M(\varphi\cos \varphi - \sin \varphi) \right] + r_c I \left[ 3\pi - 2M(1 - \cos \varphi)^2 \right] \right]
\]

(4-27)

In order to calculate the switching losses for transistors T2 and T3 formula (4-28) is used.

\[
P_{sw} = f_{sw} E_{sw} \left( \frac{I}{I_{ref}} \right)^{K_1} \left( \frac{V_{cc}}{V_{ref}} \right)^{K_2} \left( \frac{1}{2\pi} \left[ 1 + \cos \varphi \right] \right)^{1-K_1} G_t
\]

(4-28)

The formula for conduction losses on the clamping diodes D5 and D6 is presented in (4-29).

\[
P_{cond} = \frac{I}{12\pi} \left[ V_{f0} \left[ 12 + 3M \left[ (2\varphi - \pi)\cos \varphi - 2\sin \varphi \right] \right] + r_f I \left[ 3\pi - 4M(1 + \cos^2 \varphi) \right] \right]
\]

(4-29)

Where:

- \(V_{f0}\) – Diode collector – emitter threshold voltage
- \(r_f\) – Diode on – state slope resistance

In order to calculate the switching losses for the clamping diodes D5 and D6 formula (4-30) is used.

\[
P_{sw} = f_{sw} E_{sw} \left( \frac{I}{I_{ref}} \right)^{K_1} \left( \frac{V_{cc}}{V_{ref}} \right)^{K_2} \left( \frac{1}{2\pi} \left[ 1 + \cos \varphi \right] \right)^{1-K_1} G_t
\]

(4-30)

Conduction losses for reverse recovery diodes D1 and D4 are calculated as (4-31):
Based on equation (4-32) the switching losses for reverse recovery diodes D1 and D4 are calculated.

\[
P_{\text{sw}} = f_{\text{sw}} E_{\text{sw}} \left( \frac{i}{I_{\text{ref}}} \right)^{K_i} \left( \frac{V_{cc}}{V_{ref}} \right)^{K_v} \left( \frac{1}{2\pi} \right)^{1-K_i} G_i
\]  

(4-32)

The formula for conduction losses on reverse recovery diodes D2 and D3 are presented in (4-33).

\[
P_{\text{cond}} = \frac{M\dot{I}}{12\pi} \left( 3V_{f0}[-\varphi \cos \varphi + \sin \varphi] + 2r_f \dot{I} \left[ 1 - \cos \varphi \right]^2 \right)
\]  

(4-33)

Switching losses for reverse recovery diodes D2 and D3 are presented in (4-34).

\[P_{\text{sw}} = 0\]

(4-34)

The typical values for $K_v$, $K_i$, and $G_i$ are found on the Semikron modules datasheet for three level NPC and three level Type Neutral Point Clamped (TNPC). They are presented in Table 4-4.

| Table 4-4 – Typical $K_v$, $K_i$, and $G_i$ for Semikron Modules [51] |
|-----------------|------------------|------------------|
|                 | IGBT             | Diode            |
| $K_v$           | 1.4              | 0.6              |
| $K_i$           | 1                | 0.6              |
| $G_i$           | 1                | 1.15             |

In order to calculate the thermal resistance of the heat sink the total losses in the NPC leg need to be calculated. The absolute maximum ratings described in (NPC leg datasheet) are used. The other parameters are selected based on the NTV modulation strategy. The most important ratings are:

- $V_{cc} = 300 [V]$  
- $V_{ref} = 600 [V]$  
- $V_{ce0} = 2.2 [V]$  
- $r_{ce} = 22 [m\Omega]$  
- $f_{sw} = 4000 [Hz]$  
- $E_{sw} = 1.83 [mJ]$ – for each IGBT  
- $E_{sw} = 1[mJ]$ – for each diode  
- $V_{f0} = 0.85 [V]$  
- $r_f = 11 [m\Omega]$ – freewheeling diode  
- $r_f = 22 [m\Omega]$ – antiparallel diode  
- $T_s = 80 [{^\circ}C]$  

The ambient temperature was considered to be $T_a = 25 [{^\circ}C]$. By solving the equations presented above conduction losses on each device are obtained and presented in Figure 4-22.
Taking all the calculated losses into account the equivalent thermal model for the NPC converter can be drawn. The equivalent model of the thermal behaviour can be seen in Figure 4-23. This represents the Semikron Semitop3 Module with the structure presented in the beginning of this chapter (Figure 4-4). From the thermal point of view the NPC leg has been considered to be built of ten parallel heat sources, correspondent into electrical terms as current sources. The model presented in Figure 4-23 describes each device from the NPC converter leg. The temperature difference between each nod is considered to be a voltage drop on the equivalent thermal resistance. There are three types of thermal resistances that are generally considered: junction – to – case resistance $R_{th\,jc}$, case – to – heat sink resistance $R_{th\,cs}$, sink – to – ambient resistance $R_{th\,sa}$. The junction – to – case resistance and case – to – heat sink resistance are offered by the producer in the datasheet. Semikron gives in [49] the thermal resistance between junction and heat sink for each device:

- $R_{th\,js} = 0.85 \frac{K}{W}$ per IGBT.
- $R_{th\,js} = 1.7 \frac{K}{W}$ per antiparallel diode
- $R_{th\,js} = 1.1 \frac{K}{W}$ per freewheeling diode.
When talking about the heat sink all devices that produce heat has to be taken into account. One of the important components that need cooling is the voltage regulator that supplies the gate driver. There are 12 gate drivers, thus 12 voltage regulators need to be used. These voltage regulators are supplied with 24 [V] and have 18 [V] at the output. The power dissipation on these devices has been calculated based on [81] [82]. This is presented in equation (4-35).

\[ P_D = [(V_{in} - V_{out})I_{load}] + (V_{in}I_{gnd}) \] (4-35)

Where:

- \( P_D \) – Power dissipation
- \( V_{in} \) – Input voltage supplied to the regulator
- \( V_{out} \) – regulator output voltage
- \( I_{out} \) – regulator output current
- \( I_{gnd} \) – Regulator biasing currents

In general, when talking about thermal considerations the worst case scenario needs to be used. The output current of the voltage regulator is decided by the gate driver, thus \( I_{load} = 8.33 [mA] \) at \( 18 [V] \) output voltage. The regulator biasing current is zero. In conclusion, the power dissipated on a voltage regulator is \( P_d = 49.98 [mW] \), therefore all the voltage regulators dissipates \( 599.76 [mW] \). The base plates of the voltage regulators have different potential, thus in order to avoid short circuit the thermo – conducting insulating layers have to be used. The thermal resistance of the pads is \( R_{th cs} = 0.24 \frac{K}{W} \).

Taking into account the voltage regulators and NPC legs the total power dissipated on the inverter is \( 188.16 [W] \). The thermal resistance was calculated based on [83] and is presented in (4-36).
Chapter 4 – Hardware Design

\[ R_{th} = \frac{\Delta T}{P_d} = \frac{T_s - T_a}{P_d} = \frac{80 - 25}{188.1632} = 0.2923 \text{[°C/W]} \] (4-36)

Considering the value of the thermal resistance a heat sink with the thermal resistance of 0.29 [°C/W] from H S Marston has been chosen.

4.7. CPLD and DSP Control

The space vector modulation strategies were implemented on a TMS320F28335 DSP based Control Card from Texas Instruments. Deadtime and protection management is performed through Complex Programmable Logic Device (CPLD) XC9572XL. The use of the Control Card represents a fully embedded design solution, Figure 4-24, providing features as:

**ControlCard Features**
- Small Form Factor
- Standard 100 pin DIMM
- Analog and Digital Input/Output (I/O)
- JTAG Interface
- Isolated RS-232 Interface
- 5v Supply

**CPU Features**
- 150 mhz, 32 bit Floating Point
- 256k x 16 Flash, 34k x 16 Single Access Random Access Memory (SARAM)
- Up to 18 PWM Outputs
- 12 Bit ADC With 16 Channels
- 80 ns ADC Conversion Rate
- 88 General Purpose Input/Output (GPIO)
- CAN, RS-232

![Figure 4-24 – Control card Integration into the Designed Inverter](image)

Different modulation strategies are implemented on the DSP based on the code developed in the simulation model. The PWM is executed by six ePWM modules. Analogue signals, as three phase currents and DC link voltages are acquired on 5 ADC channels. Pin number 95 is reserved for communication with the CPLD. The ePWM modules are set to work based on modified Up-Down-Count mode with Dual Edge Asymmetric Waveform [84]. The schematic of how the ePWM module configuration works can be seen in Figure 4-25:
Chapter 4 – Hardware Design

There are two counters active for each ePWM module, CA and CB. When the Time Based Counter (TBCTR) reaches CA on Up Count, or CB on Down Count, the output is set high. When TBCTR reaches CB on Up Count, CA on Down Count, equals zero or period, the output is switched low. This mode of operation permits better use of the ePWM module, retaining 0-100% duty cycle. All modulation strategies use the symmetrical up-down count mode, except for RS3N and ZCM which use the asymmetrical up count mode.

An interrupt takes place on the beginning of each period that is acknowledged in an Interrupt Service Routine (ISR). During the ISR, the dwell times calculated on the main function are assigned to the ePWM module counters. Also, ePWM1A sends the Start-Of-Conversion signal to all ADs. The ePWM module uses the shadow registers which act as time buffers. On the beginning of each period, the values of the counters are updated on the shadow register after the register has assigned the values to the active counters.

From the ADC module [85], 5 channels are used. The sampling frequency is set to 12.5 MHz. The three phase currents and the two DC link voltages are acquired on each Start-Of-Conversion signal received from the ePWM module. In order to save time, the values are read into 5 global variables on the ISR used for PWM.

Pin 95 on the control card makes possible communication with the CPLD. The signal received from the CPLD stops the modulation or starts the V/f control when needed. One of the LEDs on the Control Card is used to show operation of the DSP and it flashes with the system frequency of 50 Hz or the frequency used to start in V/f control. The LED is off while the modulation is not running. In order to benefit from the full speed while embedded, the DSP has been programmed to load the entire code from flash memory to the Random Access Memory (RAM) memory at power-up. Then, the programs run fully from the RAM memory.

The Xilinx XC9572XL, Figure 4-26, CPLD used benefits from the following features:

- 72 Macrocells
- 100 MHz frequency
- 1600 usable logic gates
- 34 User I/O
- 3.3/5v Tolerant

Figure 4-25 – DSP Counter Modes

Figure 4-26 – CPLD used for Deadtime and Protection Management
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The tasks performed by the CPLD are:

- Deadtime management for each pair of complementary switches.
- Stop the modulation and disable the buffers in case of a fault.
- Signal fault status.
- Manages PWM procedures specific to NPC topology.

When IGBTs are used the deadtime or interlock delay time needs to be taken into account. This time is used to first turn off one IGBT and turn on another. Furthermore, bridge shoot through caused by unsymmetrical turn on and off times are avoided [86]. The dead time was calculated based on equation (4-37).

\[
t_{\text{dead}} = \left[ (t_{d_{\text{off, max}}} - t_{d_{\text{on, min}}} + (t_{pdd_{\text{max}}} - t_{pdd_{\text{min}}})) \right] \times 1.2
\]  

(4-37)

Where:

- \( t_{d_{\text{off, max}}} \) – is the maximum turn off delay time
- \( t_{d_{\text{on, min}}} \) – the minimum turn on delay time
- \( t_{pdd_{\text{max}}} \) – the maximum propagation delay of driver
- \( t_{pdd_{\text{min}}} \) - the minimum propagation delay of driver

By the use of gate driver [53] and Semikron module datasheets [49] the dead time can be calculated. The maximum turn off delay time is 300 \( ns \), the minimum turn on delay time is 60 \( ns \), the maximum propagation delay of the driver is 500 \( ns \) and the minimum propagation delay of the driver is 200 \( ns \). Hence, the dead time according to equation (4-37) is \( 6.48 \times 10^{-7} \) s. As the developed board is a test one and the dead time is generated through the CPLD, dead time can be modified through software, for safety reasons a dead time of 1.5 \( us \) was chosen. Aside from deadtime insertion, the algorithm has to assure that certain gate signal combinations are avoided. On a three level inverter using IGBT leg modules, the following switching states are possible [51], Table 4-5.

<table>
<thead>
<tr>
<th>T1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>T3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>T4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>state</th>
<th>Allowed States</th>
<th>Dangerous States</th>
<th>Destructive States</th>
</tr>
</thead>
</table>

All the destructive states are avoided by insertion of deadtime by means of shift registers because switch pairs T1-T3 and T2-T4 cannot be high at the same time. By means of a simple filter on the PWM inputs, the rest of the dangerous states are avoided.

Also, in the case of an emergency shutdown, the switches have to be turned off in a certain manner. In order to avoid voltage breakdown, outer switches (T1 and T4) have to be switched off first [51]. Also, in a desaturation event, there is a window of 10 \( us \) for complete switch-off [51]. The shutdown procedure ensures that any switching sequence is overridden with state “0” after proper deadtime. After reach of state “0” the inverter is completely shut down by disabling the external PWM buffers. The shutdown procedure is applied whenever there is a fault or the inverter is manually tripped.

[88]
Chapter 4 – Hardware Design

In case of a desaturation event, the gate drivers will latch in fault state. In order to be able to further use the inverter, a gate driver reset procedure is performed. The reset procedure disables the PWM from the DSP and sends the command sequence O-N-O-P-O to the inverter. This way each gate driver receives a short reset pulse used to release the latch (in case the fault is cleared).

The LED enable procedure sends the multiplexed LED signals to a demultiplexer through PWM. Seven LEDs, two green and five red provide information about the inverter state.

<table>
<thead>
<tr>
<th>LED1</th>
<th>LED2</th>
<th>LED3</th>
<th>LED4</th>
<th>LED5</th>
<th>LED6</th>
<th>LED7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Green</td>
<td>Green</td>
<td>Red</td>
<td>Red</td>
<td>Red</td>
<td>Red</td>
<td>Red</td>
</tr>
<tr>
<td>Power On</td>
<td>SVM On</td>
<td>Gate driver</td>
<td>DC Overcurrent</td>
<td>DC Voltage Range</td>
<td>Phase Overcurrent</td>
<td>Overtemperature</td>
</tr>
</tbody>
</table>

The start/end of PWM is transmitted to the DSP in order to stop the ePWM modules or to start the V/f control.

### 4.8. Hardware Validation

The three level NPC inverter design presented in this chapter has been built and tested in the laboratory. Furthermore, the protections together with dead time and turn on and off procedures are validated through experimental results.

**Deadtime Insertion**

Before powering up the inverter at full power a few tests have to be performed. The dead time between two complementary IGBTs has to be tested. The experimental result can be seen in Figure 4-27. The purple signal is the command for transistor T1 and the blue signal is the command for transistor T3. A proper 1.5 us dead time is inserted between any two complementary IGBTs.

![Figure 4-27 – Deadtime between Two Complementary IGBTs – Experimental Result](image)
Chapter 4 – Hardware Design

**Turn On and Off Procedures**

As stated before, in chapter 4.7, each IGBT leg of the inverter has to be turned on and off in a certain way. When the inverter is shut down, the outer transistors have to be turned off first followed by the inner transistors after proper deadtime.

![Figure 4-28 – Turn On and Off Procedures of the Semikron IGBT Module – Experimental Results](image)

The turn on and turn off procedures can be seen in Figure 4-28. The procedures are applied in parallel for all three inverter legs. Each of the inverter legs can be in a different state (0, N or P). Figure 4-28 presents one inverter leg. For all waveforms, the blue represents signal for transistor T1, light blue signal for transistor T2, purple represent signal for transistor T3 and the green signal represents transistor T4. As seen in the first waveform, the inverter is in N state. After deadtime, the inverter is switched to state 0 and after 1.5 us, the octal buffers are disabled, switching the inverter off completely. Second waveform represents the shut down from an N state and the third waveform shows turn off from a 0 state. The fourth waveform represents the turn on procedure. Every time, every leg starts in the 0 state, after which the modulation is started.

**Reset Procedure**

In the case that one of the gate drivers encounters a fault, a reset procedure has to be followed in order to release all gate drivers latch and restart modulation. Signal colours are the same as in Figure 4-28. The reset procedure can be seen in Figure 4-29.
The reset procedure works together with the turn on and the turn off procedures. Hence, the start and end of the reset procedure is the state “0” (0110), meaning that the inner transistors are switch first at the beginning and end of procedure. As each gate driver has to receive a short pulse in order to release the latch, the gate driver reset procedure ensures that the entire inverter is reset using zero states. As it can be seen in Figure 4-29, each inverter leg goes through states O-N-O-P-0. Because the procedure is applied at the same time for all legs, the inverter will switch through all zero vectors: 000, NNN and PPP thus ensuring that each gate driver receives a short signal in order to release the fault latch, while the voltage applied to the load is 0 V.

**DC Link Voltage Range Protection**

The DC link voltage has to be maintained between certain limits. The protection is set to shut down the inverter if each capacitor voltages voltage drops or increases with 10%. This means a ±30 V band for each of the capacitors. For this test, the DC link was connected to a three phase power switch in order to be able to connect a 5 kΩ resistor to upper or lower side. In Figure 4-30, the green signals serves as overvoltage reference, set at 330V. The light blue signal serves as undervoltage reference equal to 270 V. The blue signal is the capacitor bank voltage for upper half of the DC link (left) and lower half (right). The purple signal represents the protection response. As it can be seen in Figure 4-30, when the capacitor voltage is outside the two references, the protection triggers a fault, shutting down the inverter. The capacitor voltage in each case was raised from below the lower reference to above the upper reference and back.

![Figure 4-29 – Reset Procedure for Restarting the Modulation – Experimental Result](image)

![Figure 4-30 – DC Link Voltage Range Protection – Experimental Results](image)
DC Link and Phase Overcurrent Protection

An overcurrent event on the DC link or one of the phases also triggers the inverter. The phase overcurrent response can be seen in Figure 4-31. For this test the DC link was set at 15V and two of the output phases have been connected together. The pink signals serves as the reference and it is set to 25 A. The green signal is the short circuit current for phase overcurrent protection (left) and for DC link overcurrent protection (right). The blue signal is the protection response in each case. At the encounter of a high current the inverter trips in both cases.

![Figure 4-31 – Overcurrent Protection – Experimental Result](image)

Overtemperature Protection

The overtemperature protection has to trip the inverter if any of the three modules surface reaches 80°C. The protection response can be seen in Figure 4-32. For this test, the thermistors were removed from their sockets and external resistors were used to trigger the protection. Each of the signals represents one of the IGBT thermal protection responses.

![Figure 4-32 – Overtemperature Protection – Experimental Result](image)

Three 9.09 kΩ resistors corresponding to a temperature of 82 degree Celsius has been inserted at different times in the socket of each thermistor in order to trigger the protection. The protection triggers a fault immediately as the resistors are inserted.
**Thermal Design Validation**

Furthermore, the thermal design needs to be validated through experimental results. The setup from Figure 4-33 was used. The inverter had an R-L load with equivalent of 6 kVA. Temperature was verified each ten minutes using a thermal camera. The inverter reached thermal steady state after 40 minutes. In order to have a confidence in the measurement the test was carried another 20 minutes. The temperature did not increase in this interval.

![Experimental Setup for Thermal Validation](image1)

The infrared picture from Figure 4-34 was taken after one hour. As it can be seen the temperature in the DC link capacitors was approximately 30°C, which is below the 85°C limit of the Panasonic capacitor chosen. The temperature from the modules area was 50°C, which is below the maximum surface temperature of 80°C allowed for the IGBT modules. The hottest part of the inverter was at 56°C on the gate drivers and their DC-DC converters. The board shows thermal symmetry with the hot area in the middle being surrounded by colder areas, presenting good heat dissipation. Hence, the thermal design was validated.

![Thermal Picture of the Inverter at 6 [kW] After One Hour](image2)
5. Experimental Validation and Analysis of the Developed Modulation Strategies

Four modulation strategies were developed and rigorously tested through simulation before implemented on the designed inverter. The comparison between the four new strategies was made against classical NTV and ZCM. All offer reduced spectra for CMV compared to NTV. Although all offer natural NP balancing, only two provide extra balancing capability of up to 35%. One of the strategies developed, RS3N exhibits very strong advantages: the CMV is similar to ZCM method while maintaining the maximum modulation index of the NTV modulation. It also offers better EMI performance in high frequency range and the ability to balance the DC link in the event of external factors.

5.1. Experimental Setup

For validation of the theory and simulations, regarding the developed modulation strategies, experiments have been performed on the developed board described in Chapter 4. All experiments were performed in the same manner and with the same settings at its maximum modulation index. The control of the inverter was supplied from an external source, GwIntek GPS-4303. The DC link voltage was provided by 2 power supplies of 300 V each, SM 300-5. A 1.5 kW three phase induction motor was used as a load connected to a DC motor and power resistor. In order to see how the modulation strategy influences the CMV and EMI, no output filters were used. All voltage measurements were acquired using differential probes and visualised on the Tektronix oscilloscope. The experimental setup used to validate the developed modulation strategies is presented in Figure 5-1.

![Figure 5-1 – Experimental Setup for Testing the Developed Modulation Strategies](image-url)
5.2. Nearest Three Vectors with Even Harmonic Elimination Method

Figure 5-2 presents the experimental results regarding the phase, phase-to-phase, common mode and DC link voltages for NTV-EHE. The experiment was performed at maximum modulation index, $m_a = 1$. As expected, this voltage has a quasi-sinusoidal shape and nine voltage levels. The line voltage features five levels and the CMV has the maximum amplitude of $+\pm 200\,\text{V}$. The DC link maintains balance proving the natural balancing mode. The voltage variation on the DC link capacitors is under 5V. The results are in concordance with the theoretical basics and with the simulations. The results regarding the performance of the following methods will be compared to this method.

5.3. Zero Common Mode Method

The waveforms for ZCM are also in concordance with theory and the results from simulation. The level on the phase and on the line voltages are the same with the simulation. The effect of dead time is seen in the presence of CMV, Figure 5-3. The amount is to be analysed on chapter 5.9. Considering that the reference vector lies in sector 1 the switching sequence is $[V_0, V_7, V_{12}, V_0]$. The IGBT modules will receive the command from Table 5-1. In the ideal case, the switching between vectors does not have any dead time inserted, thus resulting in no CMV. This can be seen in the first line of Table 5-1. In the presence of dead time, the intermediate states appear when switching between certain vectors, as seen in the second line of Table 5-1. For example, the crossing between PON and PNO vectors has an intermediate state for which both second
Chapter 5 – Experimental Validation

leg and third leg are in zero state, hence P00. The length of this state is the dead time interval. Known from Table 2-5 in chapter 2.4.2, the POO intermediate state generates a CMV of $\pm \frac{1}{6} V_{DC}$. Similarly happens in the rest of the sectors, resulting in a CMV of $\pm \frac{1}{6} V_{DC}$, but on a very short period of time, compared to the applied vectors.

The performance of the proposed modulation strategies is going to be analysed in comparison with the ZCM and NTV.

<table>
<thead>
<tr>
<th>Table 5-1 – Influence of dead time on the switching sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>000</td>
</tr>
</tbody>
</table>

![Figure 5-3](image1)  
![Figure 5-3](image2)  
![Figure 5-3](image3)

Figure 5-3 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for ZCM - Experimental Results

5.4. One Large One Medium Method

Experimental results for OLOM validate the simulation model proposed before. The experiment, Figure 5-4, shows the same number levels in the phase voltage, phase-to-phase voltage and CMV. The DC link benefits the natural balancing mode, with the capacitor voltage having a ripple under 5V. The CMV has a fundamental of 150 Hz, easily visible. The performance regarding CMV is going to be analysed in chapter 5.9.
5.5. Zero Small Medium Large Method

The results of the ZSML, Figure 5-5, seem to be similar with NTV modulation. This occurs only at maximum modulation index, due to the fact that the zero vector is not applied. This can be seen from equation (5-1).

\[ T_{zero} = \left(1 - \frac{V_{ref}}{V_{ref,max}}\right)T_s \]  \hspace{1cm} (5-1)

As the reference voltage is increased, the time for zero vector is decreased. Hence, the dwell time for the zero vector becomes zero when \( V_{ref} = V_{ref,max} \). This particularity makes the phase and phase-to-phase voltages to look identical with NTV-EHE. The difference can be clearly seen in the CMV levels, which are maxim \( \pm 100 \text{ V} \) compared with \( \pm 200 \text{ V} \) for NTV. The method is tested in natural balancing mode, but there is the possibility of balancing in the case of an external neutral point unbalance. The balancing capability curve is presented in chapter 5.8.

Figure 5-4 –Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OLOM - Experimental Results
Figure 5-5 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltage for ZSML - Experimental Results
5.6. One Small One Medium Method

The good concordance between theory, simulation and experiment is also maintained for OSOM, Figure 5-6. The ripple on the capacitor voltages is smaller when compared with the rest of the modulations, being under 2.5 V. As in the OLOM modulation, the CMV fundamental frequency of 150 Hz can also be clearly seen.

![Figure 5-6](image)

Figure 5-6 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OSOM - Experimental Results

5.7. Random Sequence of 3 with Neutral Point Balancing Method

RS3N modulation follows the same pattern of good concordance between simulation, theory and experimental results as seen in Figure 5-7. Although the similarity with the NTV modulation is very high, this method has some clear differences compared to NTV. The line voltage and phase voltage are similar to NTV but the randomization of the vectors inside each switching sequence can be clearly seen. Another difference is the level of ± 100 V in the CMV voltage, which is half of NTV. Again, the random component can also be seen clearly in the CMV which is expected to reduce the amplitudes at high frequencies.

The voltage on the capacitors features a variation under 5 V. The waveforms were acquired for natural balancing mode. Another method of differentiating it from NTV is by the fact that this modulation will recover natural point balance if the neutral point potential slides towards negative or positive voltages. The balancing capability curve is presented in chapter 5.8.
5.8. DC Link Balancing Capability

All developed modulation strategies have the ability to self-balance, but only ZSML and RS3N can balance the DC link in case of an external event. The balancing capability can be determined based on theory presented at DC link capacitors, chapter 4.2 – equation (4-3). According to [32] it can be determined which phase is connected to the neutral point. Furthermore, the balancing capability is calculated as a function of phase current, equation (4-15).

\[ B_c = \frac{I_{bal}}{I_{ph}} \times 100 \% \]  \hspace{1cm} (5-2)

When the modulation index is maxim and the displacement angle is between 0 and \( \frac{\pi}{6} \) the balancing current can be calculated as in equation (5-3) for both ZSML and RS3N.

\[ I_{bal} = \sqrt{\frac{6}{\pi}} \int_0^{\frac{\pi}{6}} -I_a \left( \frac{T_a}{T_s} \right)^2 \, d\theta \]  \hspace{1cm} (5-3)

Starting from minimum modulation index until at half of it, both modulation use two small vectors for balancing. Hence, their balancing capability can be calculated. As an example, the equation for balancing capability at \( m_a = 0.5 \) is presented in (5-4).
In order to validate this theory experiments at different modulation indexes have been performed on the two methods, ZSML and RS3N. The setup shown in Figure 5-8 was used. A variable power resistor was connected through a three position switch to the neutral point of the inverter, enabling the connection to the upper or lower halves of the DC link. When the switch is in neutral position the resistor has no effect (natural balancing mode).

\[
I_{bal} = \left(3 \int_0^{\frac{\pi}{3}} \left| -I_a \frac{T_a}{T_s} + I_c \frac{T_c}{T_s} \right|^2 \, d\theta \right)^{\frac{1}{2}}
\]

(5-4)

Based on the performed experiments Figure 5-9 was obtained. As it can be observed RS3N has better capabilities of balancing than ZSML. The RS3N has the maximum balancing capability at \( m_a = 0.6 \), while ZSML at \( m_a = 1 \). The ability to balance the DC link at maximum modulation index is similar.
Chapter 5 – Experimental Validation

5.9. CMV Analysis

The general theory regarding CMV has been presented in subchapter 2.4 and the theory of developed modulation strategies chapter in 3. For a better understanding, experiments have been performed with the measurement setup described in chapter 2.5.2. The CMV has been measured at the maximum modulation index of each modulation strategy and performed the Fast Fourier Transformation (FFT) on it, Figure 5-10. As it can be seen, all modulation strategies decrease in amplitude while increasing in frequency. As the parasitic coupling inside the motor are mainly capacitive, this characteristic is preferred. The amplitude at very low frequency, as 150 Hz has little effect as the current generated is small. This can be observed from the formula (5-5). As the frequency of the capacitance decreases, the current decreases.

\[
I_p = \left| \frac{U}{R + j \frac{1}{2\pi f C}} \right| \tag{5-5}
\]

The fundamental frequency for all modulation strategies is 150 Hz. The NTV-EHE modulation has 53.7 V on the fundamental frequency. Around the switching frequency, 4 kHz, the CMV amplitude is 44.3 V. At the rest of the frequency range, the NTV-EHE modulation has amplitudes under 14.8 V. The CMV is present up to 100 kHz. The ZCM modulation should have zero CMV, if it was ideal, but in real life applications deadtime has an influence resulting in the low CMV, Figure 5-10. The fundamental for ZCM is at 8.24 V; while at switching frequency is 16.5 V. The CMV vanishes before reaching 50 kHz.

Figure 5-10 – FFT on CMV for Classic and Developed Modulation Strategies – Experimental Results
Further on, the proposed modulation strategies are to be compared with the classical ones. OLOM shares the same 100 kHz frequency range as NTV while having only 27 V CMV around the switching frequency. The rest of the spectrum remains below 11.8V. OSOM has higher amplitude on fundamental frequency 74.7 V, and low amplitude, 12.3 V, around the switching frequency. The disadvantage would be the 32.7 V at the double of the switching frequency. The spectrum remains below 100 kHz with amplitudes below 14.7V.

ZSML has 43 V on CMV around the switching frequency, but the spectrum is only until 50 kHz with amplitudes under 17.7V. An interesting result is provided by the RS3N modulation strategy. By randomizing its vectors inside the switching sequence, the CMV frequencies are moved towards lower frequency range. The CMV around the switching frequency for RS3N is 19.1 V. The rest of the spectrum, which is until 50 kHz, features amplitudes below 7.5 V.

In an overall comparison, ZSML maintains the level of CMV around the switching frequency, compared with NTV, while having half its spectrum. OLOM has almost twice as low CMV at switching, retaining amplitudes under NTV throughout the entire spectrum. OSOM seems to move the amplitudes, seen at other strategies, to double of switching frequency, while the rest of the spectrum is comparable with NTV-EHE. The RS3N modulation has superior results to NTV-EHE for entire spectrum. Around switching frequency, it features half of the CMV, compared to NTV-EHE, and almost the same level compared to ZCM. The performance of RS3N is comparable with ZCM modulation in terms of spectrum length and CMV levels throughout the entire frequency range.

5.10. Comparison of Conductive EMI produced by Modulation Strategies

The theoretical part regarding EMI is described in chapter 2.5.1. An experimental setup has been built in order to observe the influence of modulation strategy over the EMI. Due to limited resources an alternative solution has been adopted. This solution is based on [87] and uses a clamp-on current probe for measuring the common mode current. The current probe used can measure currents with frequencies up to 20 MHz. Figure 5-11 presents the adopted solution. The probe will add the currents in the same direction and subtract the one with opposite directions, hence only the common mode current will be measured.
Based on this solution experiments were performed on each modulation strategy at its maximum modulation index. Figure 5-12 presents the conducted EMI, between the inverter and load, in decibels on a logarithmic scale. All six modulation strategies seem to develop the same EMI, but at a closer look, there are some differences. The four developed modulation strategies are compared against the classical ones, ZCM and NTV. The ZCM method has 7 dB less at lower frequencies, compared to NTV, which is constant at 60 dB up to 1 MHz. After this frequency the difference between these two decreases to 2 dB. The peak for all strategies is at 2 MHz. NTV has a peak of 79 dB, while ZCM has 70 dB. Both strategies remain at 50 dB on the high frequency range, between 3 MHz and 20 MHz.

The proposed strategies have similar results in the low frequency range, amplitude of 57 dB. The peak for all strategies is around 75-77 dB at 2 MHz, being situated between ZCM and NTV. In the high frequency range, OLOM, OSOM and ZSML remain at 50 dB. RS3N has lower amplitude between 3 MHz and 20 MHz, 43 dB, being 7 dB lower than the rest of the modulation strategies.

Comparing all the EMI results it can be seen that OSOM, OLOM and ZSML seem to be situated between ZCM and NTV. RS3N is situated between ZCM and NTV at low frequency range, while at high frequency range seem to offer improvements over both.

![Graphs of Conductive EMI Currents Produced by Modulation Strategies](image-url)

Figure 5-12 – Conductive EMI Currents Produced by Modulation Strategies
Chapter 6 – Conclusions

6. Conclusions and Future Work

This chapter presents the conclusions regarding the two main objectives: development of modulation strategies that address DC link balancing and CMV reduction and the hardware design of the three-level NPC inverter. Further on, future work is stated.

6.1. Conclusions Regarding the Development of Modulation Strategies that Address DC Link Balancing and CMV Reduction

Solutions to reduce the common mode voltage and to balance the DC link through modulation strategies regarding three-level NPC inverter were studied. Throughout the master thesis four modulation strategies have been developed that address these problems:

- OLOM – uses one large, one medium and one zero vector in order to create the reference voltage vector over each 30° displacement angle.
- ZSML – the reference vector comprises all types of stationary vectors. At maximum modulation index only small, medium and large vectors are used. The zero vector is applied at smaller modulation indexes and its time is dependent on the amplitude of the reference voltage.
- OSOM – on each 30° displacement angle one small, one medium and one zero vector are used to build the reference vector.
- RS3N – uses the nearest three vectors to create the reference vector. The difference from NTV is that has the switching sequence of three and it is randomized.

All of the developed modulations have the ability to self-balance, but only two can balance the DC link voltage in case of external event. The balancing capability has been determined as a function of phase current. At maximum modulation index both ZSML and RS3N have similar capabilities for balancing the neutral point, but RS3N offers more at smaller modulation indexes than ZSML.

The methods were developed targeting an improved CMV response over the classical modulation strategies. All methods offer reduced CMV spectrum. Their performance is between ZCM and NTV. Good results are obtained by RS3N, which offers performance similar to ZCM while preserving the modulation index of NTV and offering up to 35% balancing capability.

Furthermore, each of these methods was analysed regarding electromagnetic interference. Conductive EMI has been measured and the results show that OSOM, OLOM and ZSML are situated between NTV and ZCM. RS3N is as well situated between NTV and ZCM at low frequencies, until 3 MHz, while at high frequency, over 3 MHz, offers better performance.
By the use of small and medium vectors OSOM can only go at half of the maximum modulation index. The other three methods have a better utilisation of the bus bar, modulation index equal to one.

All of the developed modulations were validated through simulations and experimental results. All experimental analysis has been performed on the designed three-level NPC prototype. Based on the analysis performed on each of them it can be affirmed that all of them offers reduction of the CMV. From the spectral and CMV analysis it can be affirmed that the best performance is offered by RS3N.

6.2. Conclusions Regarding Hardware Design of the Three-Level NPC Inverter

The three-level NPC inverter PCB was design in Altium. The PCB manufacturing had to be done by an external company based on the source files provided due to the fact that it has four layers and only PCBs with two layers can be done in AAU laboratories. The assembly, test and all experiments were performed in AAU laboratories. The PCB features integrated DC link and galvanic isolation between power and control stage together with mixed analog and digital design. All ADC and PWM signals are shielded against noise by being buried into the PCB and having ground layers on top and bottom.

The new specialized NPC leg IGBT modules reduce the commutation paths; therefore the high voltage spikes and noise are reduced. By using these modules the inverter has no overvoltage snubbers and permits an overall enhanced design.

Furthermore, special attention was paid when sizing the DC link capacitors. They have reduced size, 30%, and are configured in a bank having a thermally optimal position.

The use of optocoupler based gate drivers with advanced features such as undervoltage lock-out, desaturation detection and active Miller clamping contribute even more to the reduced size, featuring the need only for single power supply because the turn-off is performed by the gate driver through the active Miller clamping. The possibility of current up to 2.5 A together with soft turn-off and isolated fault feedback make these drivers well suited for this application.

The inverter reduced size is also a consequence of the embedded DSP design in combination with the CPLD used for management of dead-time and protections. This combination offers flexibility and safety. The chosen DSP benefits of small form factor, DIMM100 connector, as well as integrated FLASH and RAM memory with CPU speed up to 150 MHz. The ADC modules have fast sampling, 80ns, and run independently of the CPU as the ePWM units. Having this property the ePWM gain extra degrees of freedom. Furthermore, the CPLD features a 100 MHz running frequency and full flexibility in configuring the I/O and extra clocks. The 3.3V/5V tolerance makes the CPLD a very good choice as it permits a mixed voltage design.

Protections regarding DC link overcurrent, phase overcurrent, DC link voltage out of range, overtemperature and protection against desaturation events make the design bullet proof. The protections are all fully
adjustable thus providing a flexible hardware platform. The protections were tested and resulted in full validation of the design. As a feature this protections have an optical fault feedback system through LEDs.

Furthermore, special attention was given to the specifics of the three-level topology such as semiconductor turn-on and turn-off order. For this concern, turn-off, turn-on and reset procedures are implemented on the CPLD and validated though experiments as well as the PWM filters. These filters prevent the shoot-through of the entire inverter and N-P or P-N switching sequence combinations. The start-up behavior of the inverter was also carefully managing ensuring no destructive device states occur.

Other features such as use of Hall-effect current sensors and RS-232 and CAN communications provide an enhanced design. The JTAG interfaces for both CPLD and DSP were implemented, thus making the debugging and onboard programming processes easy.

The code inside the DSP is designed to automatically transfer itself from flash memory into RAM at each power-up, and run from there in order to optimize the computing speed and algorithm performance.

Conduction losses as well as the switching ones were calculated using a methodology offered by Semikron. Furthermore, the thermal influence of the voltage regulators, need for gate drivers, were taken into account. Based on these calculations the thermal resistance was calculated. This design was experimentally validated through thermal imaging.

### 6.3. Future Work

Future work might include:

- Standard measurement of Conducted EMI
- Measurements and Analysis of Radiated EMI
Bibliography


[33] Environmental Potentials Research and Development Department, "Reducing Motor Shaft Voltages," 800.500.7436.


[36] Elizabeth S. Galano Paul I. Nippes, "Understanding Shaft Voltage and Grounding Currents of Turbine Generators".


[43] S. Guttowski, and K. Heumann H. Jorgensen, "Reduction of conducted line emissions in voltage fed


[61] Allegro, "Fully integrated, Hall Effect-Based Linear Current Sensor IC with 3 kV RMS Voltage Isolation [IV]
and a Low-Resistance Current Conductor, "ACS756 Datasheet.


[63] Texas Instruments, "TLC372, LinCMOS Dual Differential Comparators," Dallas, Texas, USA.


[86] Zhang Xi, "How to calculate and minimize the dead time requirement for IGBTs properly," Infineon Technologies AG, Munchen, Germany, Application note 2007.

Appendix 1: Project Proposal

#16 Student Project

Project Title
Modulation of three-level inverter with common-mode voltage elimination and DC-link balancing

Target Group
M.Sc.E.E. or B.Sc.E.E. graduate students

Background
Conventional two-level voltage source inverters (VSI) generate common-mode voltage within the motor windings, which may cause motor failures due to bearing currents. Further, due to the capacitive coupling between the stator winding and the grounded motor frame, a common mode leakage current will flow, resulting in significant common-mode EMI. By use of a three-level inverter, c.f. Fig 1, and by use of only six of the active switch vectors, the common-mode voltage can be eliminated. (The common-mode voltage elimination is achieved at the expense of a reduction in the voltage transfer ratio, which becomes 0.866.) This modulation scheme was proposed by [1] where the voltage levels within the three-level inverter were achieved from independent DC-sources. However, in three-level converter structures, where the voltage levels are obtained by series connected capacitors, a DC-link voltage problem might occur by which an excessive high voltage might be applied to the switching devices (only for the topology in Fig. 1a). Further, the three-level converter might be unable to synthesize the reference voltage if too large voltage unbalance occurs. Hence, besides avoiding the common mode voltage, the modulation of the three-level converter also has to address the voltage unbalance between the upper and the lower switches.

![Diagram of a three-level neutral point clamped inverter](image)

*Fig. 1. Three-level neutral point clamped inverters. a) Conventional topology. b) Modified topology.*

[1] Haoran Zhang and Annette von Jouanne and Alan Vallace, Multilevel inverter modulation schemes to eliminate common-mode voltages, Transaction on Industry
Problem Statement:

Based on the problems listed above, the problem statement for this project becomes:

Development of a modulation scheme that addresses both common-mode voltage elimination and DC-link balancing.

Project Content

Besides paying attention to the stated problem, the project could/should include the following issues:

- Hardware design of the three-level inverter
- Development of a simulation model to test different modulation strategies before implementation.
- d-SPACE or DSP implementation of the modulation/control of the three-level converter.
- Comparison of the emitted common-mode EMI from conventional modulation schemes and the developed modulation scheme.

Analysis of the DC-link unbalance problem.
## Appendix 2: Switching Tables for All Methods

In this appendix the switching table from each modulation strategy is presented. The first implemented method was the classical NTV–EHE for comparison with the developed ones. The switching table for NTV-EHE is presented below.

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### Sector IV

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### Appendix 2 – Switching Tables

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<td>$\bar{V}<em>{6N}$ ONO $\bar{V}</em>{5P}$ OOP $\bar{V}<em>{6N}$ ONO $\bar{V}</em>{5P}$ OOP $\bar{V}<em>{17}$ NNP $\bar{V}</em>{18}$ PNP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{5N}$ NNO $\bar{V}</em>{6P}$ POP $\bar{V}<em>{5N}$ NNO $\bar{V}</em>{6P}$ POP $\bar{V}<em>{5N}$ NNO $\bar{V}</em>{6P}$ POP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{1N}$ OOO $\bar{V}</em>{1N}$ OOO $\bar{V}<em>{11}$ ONP $\bar{V}</em>{11}$ ONP $\bar{V}<em>{11}$ ONP $\bar{V}</em>{11}$ ONP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{5P}$ OPP $\bar{V}</em>{6N}$ ONO $\bar{V}<em>{5P}$ OOP $\bar{V}</em>{6N}$ ONO $\bar{V}<em>{5P}$ OOP $\bar{V}</em>{6N}$ ONO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Sector VI

<table>
<thead>
<tr>
<th>Region 1a</th>
<th>Region 1b</th>
<th>Region 2a</th>
<th>Region 2b</th>
<th>Region 3</th>
<th>Region 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\bar{V}<em>{6N}$ ONO $\bar{V}</em>{1P}$ POO $\bar{V}<em>{6N}$ ONO $\bar{V}</em>{1P}$ POO $\bar{V}<em>{6N}$ ONO $\bar{V}</em>{1P}$ POO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{1N}$ OOO $\bar{V}</em>{1N}$ OOO $\bar{V}<em>{12}$ PNO $\bar{V}</em>{12}$ PNO $\bar{V}<em>{12}$ PNO $\bar{V}</em>{12}$ PNO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{6P}$ POP $\bar{V}</em>{6P}$ ONN $\bar{V}<em>{6P}$ POP $\bar{V}</em>{6P}$ ONN $\bar{V}<em>{6P}$ POP $\bar{V}</em>{6P}$ ONN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{1P}$ POO $\bar{V}</em>{6N}$ ONO $\bar{V}<em>{1P}$ POO $\bar{V}</em>{6N}$ ONO $\bar{V}<em>{18}$ PNP $\bar{V}</em>{13}$ PNN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\bar{V}<em>{1N}$ ONO $\bar{V}</em>{6N}$ ONO $\bar{V}<em>{1P}$ POO $\bar{V}</em>{6N}$ ONO $\bar{V}<em>{18}$ PNP $\bar{V}</em>{13}$ PNN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Furthermore, another classical method was implemented for its ability to reduce the CMV. The switching table is presented below.

### ZCM switching sequence

<table>
<thead>
<tr>
<th>Sector 1</th>
<th>Sector 2</th>
<th>Sector 3</th>
<th>Sector 4</th>
<th>Sector 5</th>
<th>Sector 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_0$ $V_7$ $V_{12}$ $V_0$</td>
<td>$V_0$ $V_8$ $V_7$ $V_0$</td>
<td>$V_0$ $V_9$ $V_8$ $V_0$</td>
<td>$V_0$ $V_{10}$ $V_9$ $V_0$</td>
<td>$V_0$ $V_{11}$ $V_{10}$ $V_0$</td>
<td>$V_0$ $V_{12}$ $V_{11}$ $V_0$</td>
</tr>
</tbody>
</table>
The first method developed modulation strategy is OLOM. This method is divided into 12 sectors with a displacement angle of 30°. The switching table is presented below.

<table>
<thead>
<tr>
<th>OLOM Switching table</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sector 1</td>
</tr>
<tr>
<td>Sector 2</td>
</tr>
<tr>
<td>Sector 3</td>
</tr>
<tr>
<td>Sector 4</td>
</tr>
<tr>
<td>Sector 5</td>
</tr>
<tr>
<td>Sector 6</td>
</tr>
<tr>
<td>Sector 7</td>
</tr>
<tr>
<td>Sector 8</td>
</tr>
<tr>
<td>Sector 9</td>
</tr>
<tr>
<td>Sector 10</td>
</tr>
<tr>
<td>Sector 11</td>
</tr>
<tr>
<td>Sector 12</td>
</tr>
</tbody>
</table>

Next, another method arises, OSOM. This method is divided into 12 sectors as well as OLOM, but uses small, medium and zero vectors in order to create the reference vector. Its table can be seen below.

<table>
<thead>
<tr>
<th>OSOM switching sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sector 1</td>
</tr>
<tr>
<td>Sector 2</td>
</tr>
<tr>
<td>Sector 3</td>
</tr>
<tr>
<td>Sector 4</td>
</tr>
<tr>
<td>Sector 5</td>
</tr>
<tr>
<td>Sector 6</td>
</tr>
<tr>
<td>Sector 7</td>
</tr>
<tr>
<td>Sector 8</td>
</tr>
<tr>
<td>Sector 9</td>
</tr>
<tr>
<td>Sector 10</td>
</tr>
<tr>
<td>Sector 11</td>
</tr>
<tr>
<td>Sector 12</td>
</tr>
</tbody>
</table>

Theory states that if all stationary vectors are used the number of levels, in the phase voltage, is maximum. The switching table for ZSML, when in natural balancing, is presented below.

<table>
<thead>
<tr>
<th>ZSML switching sequence for natural balancing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Region 1</td>
</tr>
<tr>
<td>Sector 1</td>
</tr>
<tr>
<td>Sector 2</td>
</tr>
<tr>
<td>Sector 3</td>
</tr>
</tbody>
</table>
Furthermore, if the DC link is unbalanced due to an external event the next switching tables are going to be used until the perturbation is eliminated.

ZSML switching sequence in balancing mode – P and N type tables

<table>
<thead>
<tr>
<th>Region 1 – P type</th>
<th>Region 2 – P type</th>
<th>Region 1 – N type</th>
<th>Region 2 – N type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sector 1</td>
<td>$V_0 V_{1p} V_7 V_{13} V_{1p} V_6$</td>
<td>$V_0 V_{2p} V_{14} V_{14} V_{2p} V_6$</td>
<td>$V_0 V_{1n} V_{13} V_{13} V_{1n} V_0$</td>
</tr>
<tr>
<td>Sector 2</td>
<td>$V_0 V_{2p} V_9 V_{16} V_{16} V_{2p} V_0$</td>
<td>$V_0 V_{3p} V_{15} V_{15} V_{3p} V_0$</td>
<td>$V_0 V_{2n} V_{14} V_{14} V_{2n} V_0$</td>
</tr>
<tr>
<td>Sector 3</td>
<td>$V_0 V_{3p} V_{14} V_{17} V_{17} V_{3p} V_0$</td>
<td>$V_0 V_{4p} V_{18} V_{18} V_{4p} V_0$</td>
<td>$V_0 V_{3n} V_{15} V_{15} V_{3n} V_0$</td>
</tr>
<tr>
<td>Sector 4</td>
<td>$V_0 V_{4p} V_9 V_{12} V_{12} V_{4p} V_0$</td>
<td>$V_0 V_{5p} V_{16} V_{16} V_{5p} V_0$</td>
<td>$V_0 V_{4n} V_{17} V_{17} V_{4n} V_0$</td>
</tr>
<tr>
<td>Sector 5</td>
<td>$V_0 V_{5p} V_{11} V_{11} V_{5p} V_0$</td>
<td>$V_0 V_{6p} V_{18} V_{18} V_{6p} V_0$</td>
<td>$V_0 V_{5n} V_{17} V_{17} V_{5n} V_0$</td>
</tr>
<tr>
<td>Sector 6</td>
<td>$V_0 V_{6p} V_{14} V_{14} V_{6p} V_0$</td>
<td>$V_0 V_{1p} V_{12} V_{12} V_{1p} V_0$</td>
<td>$V_0 V_{6n} V_{18} V_{18} V_{6n} V_0$</td>
</tr>
</tbody>
</table>

Based on nearest three vectors idea, another method was developed. This method randomises the switching table in order to reduce the CMV. The switching sequence can be seen below. As ZSML, this method has the ability to balance the DC link in case of an external event.

RS3N switching sequence when in natural balancing mode

<table>
<thead>
<tr>
<th>Region 1</th>
<th>Region 2</th>
<th>Region 3</th>
<th>Region 4</th>
<th>Region 5</th>
<th>Region 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sector 1</td>
<td>$V_0 V_1 V_0 V_{2n}$</td>
<td>$V_0 V_2 V_0 V_{1n}$</td>
<td>$V_0 V_3 V_0 V_{1n}$</td>
<td>$V_0 V_4 V_0 V_{1n}$</td>
<td>$V_0 V_5 V_0 V_{1n}$</td>
</tr>
<tr>
<td>Sector 2</td>
<td>$V_0 V_1 V_2 V_{2n}$</td>
<td>$V_0 V_2 V_2 V_{1n}$</td>
<td>$V_0 V_3 V_2 V_{1n}$</td>
<td>$V_0 V_4 V_2 V_{1n}$</td>
<td>$V_0 V_5 V_2 V_{1n}$</td>
</tr>
<tr>
<td>Sector 3</td>
<td>$V_0 V_1 V_3 V_{3n}$</td>
<td>$V_0 V_2 V_3 V_{2n}$</td>
<td>$V_0 V_3 V_3 V_{2n}$</td>
<td>$V_0 V_4 V_3 V_{2n}$</td>
<td>$V_0 V_5 V_3 V_{2n}$</td>
</tr>
<tr>
<td>Sector 4</td>
<td>$V_0 V_1 V_4 V_{4n}$</td>
<td>$V_0 V_2 V_4 V_{3n}$</td>
<td>$V_0 V_3 V_4 V_{3n}$</td>
<td>$V_0 V_4 V_4 V_{3n}$</td>
<td>$V_0 V_5 V_4 V_{3n}$</td>
</tr>
<tr>
<td>Sector 5</td>
<td>$V_0 V_1 V_5 V_{5n}$</td>
<td>$V_0 V_2 V_5 V_{4n}$</td>
<td>$V_0 V_3 V_5 V_{4n}$</td>
<td>$V_0 V_4 V_5 V_{4n}$</td>
<td>$V_0 V_5 V_5 V_{4n}$</td>
</tr>
<tr>
<td>Sector 6</td>
<td>$V_0 V_1 V_6 V_{6n}$</td>
<td>$V_0 V_2 V_6 V_{5n}$</td>
<td>$V_0 V_3 V_6 V_{5n}$</td>
<td>$V_0 V_4 V_6 V_{5n}$</td>
<td>$V_0 V_5 V_6 V_{5n}$</td>
</tr>
</tbody>
</table>

RS3N switching sequence when in balancing mode

<table>
<thead>
<tr>
<th>Region 1 – P Type</th>
<th>Region 2 – P Type</th>
<th>Region 3 – P Type</th>
<th>Region 4 – P Type</th>
<th>Region 1 – N Type</th>
<th>Region 2 – N Type</th>
<th>Region 3 – N Type</th>
<th>Region 4 – N Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sector 1</td>
<td>$V_{1p} V_0 V_{2p}$</td>
<td>$V_{2p} V_0 V_{3p}$</td>
<td>$V_{3p} V_0 V_{4p}$</td>
<td>$V_{1n} V_0 V_{2n}$</td>
<td>$V_{2n} V_0 V_{3n}$</td>
<td>$V_{3n} V_0 V_{4n}$</td>
<td>$V_{1n} V_2 V_{1n}$</td>
</tr>
<tr>
<td>Sector 2</td>
<td>$V_{1p} V_1 V_{2p}$</td>
<td>$V_{2p} V_1 V_{3p}$</td>
<td>$V_{3p} V_1 V_{4p}$</td>
<td>$V_{1n} V_1 V_{2n}$</td>
<td>$V_{2n} V_1 V_{3n}$</td>
<td>$V_{3n} V_1 V_{4n}$</td>
<td>$V_{1n} V_2 V_{1n}$</td>
</tr>
<tr>
<td>Sector 3</td>
<td>$V_{1p} V_2 V_{2p}$</td>
<td>$V_{2p} V_2 V_{3p}$</td>
<td>$V_{3p} V_2 V_{4p}$</td>
<td>$V_{1n} V_2 V_{2n}$</td>
<td>$V_{2n} V_2 V_{3n}$</td>
<td>$V_{3n} V_2 V_{4n}$</td>
<td>$V_{1n} V_2 V_{1n}$</td>
</tr>
<tr>
<td>Sector 4</td>
<td>$V_{1p} V_3 V_{2p}$</td>
<td>$V_{2p} V_3 V_{3p}$</td>
<td>$V_{3p} V_3 V_{4p}$</td>
<td>$V_{1n} V_3 V_{2n}$</td>
<td>$V_{2n} V_3 V_{3n}$</td>
<td>$V_{3n} V_3 V_{4n}$</td>
<td>$V_{1n} V_2 V_{1n}$</td>
</tr>
<tr>
<td>Sector 5</td>
<td>$V_{1p} V_4 V_{2p}$</td>
<td>$V_{2p} V_4 V_{3p}$</td>
<td>$V_{3p} V_4 V_{4p}$</td>
<td>$V_{1n} V_4 V_{2n}$</td>
<td>$V_{2n} V_4 V_{3n}$</td>
<td>$V_{3n} V_4 V_{4n}$</td>
<td>$V_{1n} V_2 V_{1n}$</td>
</tr>
<tr>
<td>Sector 6</td>
<td>$V_{1p} V_5 V_{2p}$</td>
<td>$V_{2p} V_5 V_{3p}$</td>
<td>$V_{3p} V_5 V_{4p}$</td>
<td>$V_{1n} V_5 V_{2n}$</td>
<td>$V_{2n} V_5 V_{3n}$</td>
<td>$V_{3n} V_5 V_{4n}$</td>
<td>$V_{1n} V_2 V_{1n}$</td>
</tr>
</tbody>
</table>
Appendix 3: Experimental Setup Data

When the experiments were performed the following devices were used as a part of the setup:

- 2x SM 300-5, 300V, 5A Power Supplies
- 1x SM 600-10, 600V, 10A Power Supply
- 1x GwInstek GPS-4303, 12v Power Supply
- 1x Tektronix DPO 2014 Digital Phosphor Oscilloscope
- 3x Tektronix P5200 High Voltage Differential Probe 130v / 1300v
- 1x Tektronix TCP0150 Current Probe, 150A, 20 MHz
- 1x Fluke 179 True RMS Multimeter
- 4x Tektronix P2221 Voltage Probe
- 1x Digilent HS1 JTAG Emulator for CPLD
- 1x Signum JTAGJET-C2000 JTAG Emulator for DSP
- 1x National Instruments NI cDAQ-9172 Acquisition System Chasis
- 1x NI 9227 Quad Current Sensor Module
- 2x ASEA Load Inductor, 3 kVar
- 2x ASEA 5514 152-8, 220/95 V, 4000 ohm, Load Resistor, 4.5 / 2 kW,
- 1x Zentro Elektric Electronic Load, EL1000/800/20, Vi=230v, 50hz, 0.2A, V0=800v, 20A, 1000W.
- 2x Danotherm 23 E, 12.5 ohm, 13.6 A Variable Resistors
- 1x Danotherm 23 E, 2.5 ohm, 13.6 A Variable Resistor
- 1x Danotherm 23 E, 5000 ohm, 0.33 A Variable Resistor
- 1x Danotherm 23 D, 500 ohm, 0.96 A Variable Resistor
- 1x ABB Induction Motor, M2VA80C-2 3GVA081003-ASB, Wye Connection, 380-420V, 50hz, 2840 rpm, 1.5 kW, 3.4/5.7 A, cos(ϕ)=0.83
- 1x Transtecno DC Motor, EC350.240, 24V, 29.4A, 3000 rpm, 1.57 Nm, 0.5 kW
- 1x Forward Looking Infra-Red (FLIR) Camera – Thermal Camera
- Three Phase Switch, 72502E, AAU
Appendix 4: CPLD/DSP Pin Assignment

When the modulation strategies have been developed on the DSP, the pin assignment had to be performed. This was done accordingly to the DSP hardware design guidelines [67].

### DSP Pin Assignment

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3V3 ISO</td>
<td>21</td>
<td>GND A</td>
<td>41</td>
<td>NC</td>
<td>61</td>
<td>GND A</td>
<td>81</td>
</tr>
<tr>
<td>2</td>
<td>RXA_ISO</td>
<td>22</td>
<td>NC</td>
<td>42</td>
<td>GPIO 87</td>
<td>62</td>
<td>GND A</td>
<td>82</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>23</td>
<td>EPWM 1A</td>
<td>43</td>
<td>NC</td>
<td>63</td>
<td>GND A</td>
<td>83</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>24</td>
<td>EPWM 2A</td>
<td>44</td>
<td>CAN RXA</td>
<td>64</td>
<td>GND A</td>
<td>84</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>25</td>
<td>EPWM 3A</td>
<td>45</td>
<td>NC</td>
<td>65</td>
<td>GND A</td>
<td>85</td>
</tr>
<tr>
<td>6</td>
<td>GND ISO</td>
<td>26</td>
<td>EPWM 4A</td>
<td>46</td>
<td>NC</td>
<td>66</td>
<td>GND A</td>
<td>86</td>
</tr>
<tr>
<td>7</td>
<td>ADC PHASE A</td>
<td>27</td>
<td>GND D</td>
<td>47</td>
<td>GND D</td>
<td>67</td>
<td>GND A</td>
<td>87</td>
</tr>
<tr>
<td>8</td>
<td>GND A</td>
<td>28</td>
<td>EPWM 5A</td>
<td>48</td>
<td>TCK</td>
<td>68</td>
<td>NC</td>
<td>88</td>
</tr>
<tr>
<td>9</td>
<td>ADC PHASE B</td>
<td>29</td>
<td>EPWM 6A</td>
<td>49</td>
<td>TMS</td>
<td>69</td>
<td>GND A</td>
<td>89</td>
</tr>
<tr>
<td>10</td>
<td>GND A</td>
<td>30</td>
<td>NC</td>
<td>50</td>
<td>EMU1</td>
<td>70</td>
<td>NC</td>
<td>90</td>
</tr>
<tr>
<td>11</td>
<td>ADC PHASE C</td>
<td>31</td>
<td>GPIO 84</td>
<td>51</td>
<td>3V3 ISO</td>
<td>71</td>
<td>GND A</td>
<td>91</td>
</tr>
<tr>
<td>12</td>
<td>GND A</td>
<td>32</td>
<td>GPIO 86</td>
<td>52</td>
<td>TXA ISO</td>
<td>72</td>
<td>NC</td>
<td>92</td>
</tr>
<tr>
<td>13</td>
<td>ADC DC+</td>
<td>33</td>
<td>NC</td>
<td>53</td>
<td>NC</td>
<td>73</td>
<td>NC</td>
<td>93</td>
</tr>
<tr>
<td>14</td>
<td>GND A</td>
<td>34</td>
<td>NC</td>
<td>54</td>
<td>NC</td>
<td>74</td>
<td>NC</td>
<td>94</td>
</tr>
<tr>
<td>15</td>
<td>ADC DC-</td>
<td>35</td>
<td>NC</td>
<td>55</td>
<td>NC</td>
<td>75</td>
<td>NC</td>
<td>95</td>
</tr>
<tr>
<td>16</td>
<td>GND A</td>
<td>36</td>
<td>NC</td>
<td>56</td>
<td>GND ISO</td>
<td>76</td>
<td>NC</td>
<td>96</td>
</tr>
<tr>
<td>17</td>
<td>GND A</td>
<td>37</td>
<td>GND D</td>
<td>57</td>
<td>GND A</td>
<td>77</td>
<td>5V D</td>
<td>97</td>
</tr>
<tr>
<td>18</td>
<td>NC</td>
<td>38</td>
<td>NC</td>
<td>58</td>
<td>GND A</td>
<td>78</td>
<td>TXB</td>
<td>98</td>
</tr>
<tr>
<td>19</td>
<td>GND A</td>
<td>39</td>
<td>NC</td>
<td>59</td>
<td>GND A</td>
<td>79</td>
<td>RXB</td>
<td>99</td>
</tr>
<tr>
<td>20</td>
<td>NC</td>
<td>40</td>
<td>NC</td>
<td>60</td>
<td>GND A</td>
<td>80</td>
<td>NC</td>
<td>100</td>
</tr>
</tbody>
</table>

The CPLD pin configuration can be seen in the following table.

### CPLD Pin Assignment

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
<th>Function</th>
</tr>
</thead>
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Signal Path from DSP to gate drives

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Appendix 5: CPLD
Functional Schematic
Appendix 6: PCB Photos
Appendix 7: PCB Layers

Layer 1
Appendix 7: PCB Layers

Layer 1
Appendix 7: PCB Layers

Layer 2
Appendix 7: PCB Layers

Layer 3
Layer 4
Appendix 7: PCB Layers
Layer 4
Appendix 8: Electrical Schematic
### Appendix 9: Bill of Materials

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## Appendix 9 – Bill Of Materials

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<td>148121</td>
<td>farnell</td>
<td>H S MARSTON 96CN-02500-A-200</td>
<td>1</td>
</tr>
<tr>
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<td>PCB</td>
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</table>
Appendix 10: Paper

Development of Modulation Strategies for NPC Converter Addressing DC Link Voltage Balancing and CMV Reduction

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Abstract—Multilevel inverters are more popular due to their superior performance compared with two level inverters. One of the most optimal applications for multilevel inverter is the Adjustable Speed Drives (ASD). The industry reported numerous ASD failures due to high frequency PWM. Those failures consist in insulation breakdown and bearing failures. By the use of this type of converters, both Electromagnetic Interference (EMI) and harmonic distortions are improved.

This paper proposes two modulation strategies for Three Level Neutral Point Clamped Converter (3L-NPC). The main focus of these modulation strategies is to reduce the Common Mode Voltage (CMV) and balance the DC Link Voltage.

Keywords: 3L-NPC Converter, Modulation Strategies, DC Link Balancing, CMV Reduction, Multilevel, SVM

I. INTRODUCTION

An important issue nowadays is saving energy. Electrical motors are widely used to generate motion from electrical energy [1]. Industrial and domestic applications use electric motors with a large variety of power ratings. In industrialized countries, electric motors use approximately 70% of the produced electric energy [2]. In the past, DC machines were used for their simplicity in speed control. Nevertheless, these types of machines have some disadvantages compared with AC machines. AC machines cannot be efficiently controlled with direct connection to the grid, thus adjustable speed drives (ASD) for control of the magnitude and frequency of the output voltage are required. These types of drives have a large scale of utilization in industrial applications. Due to the development of adjustable drives, the reliance in three phase AC motors has increased [1]. ASD are often used in industrial and household applications, like ventilation system, pumps and electric drives for machine tools. By the use of the ASD the output speed can be modified through magnitude and frequency of the output voltage by means of PWM [2].

When talking about three level Voltage Source Inverters (VSI), there has to be mentioned that since their invention they have been considered to be used in high capacity, high performance AC drives applications [3]. Common Mode Voltage (CMV) is defined as the voltage between the neutral point and ground and it is generated by the PWM strategies. This type of voltage creates important problems when talking of high switching frequencies. The techniques regarding attenuation of high frequency problems in AC motor drives systems have at base the reduction of CMV. This voltage has a very important influence over the shaft voltage [2]. One important solution for reducing the shaft voltage and leakage current is the reduction of CMV. This can be done by two methods:

- Attenuation of the shaft voltage through motor design
- CMV attenuation through PWM strategy

It has to be mentioned that there exists different capacitive couplings between the ASD system and motor. When talking about low frequency analysis in drives systems these capacitances can be neglected due to their small values, but their effects become important when the switching frequency of the converter is increased as the switching devices are improved. These capacitances offer a flow path for high frequency currents.

One important problem discovered in 3L-NPC converter is the balancing of the DC link Neutral Point (NP). This type of inverter is exposed to problems like fluctuations in the NP due to irregular and unpredictable charging and discharging of the upper and lower DC link capacitors. As it is defined in [3], there exists an unbalance regarding the charging and discharging in each capacitor, thus the voltage across the capacitor may rise or fall and the NP voltage will not be able to keep half of the DC link voltage. Due to this problem, a high voltage may be applied to the semiconductors or DC link capacitors causing damage. This can be solved through three methods:

- Separate DC sources [4].
- Voltage regulators for each level using an additional small leg [5].
• Modified PWM pattern and voltage vector selection

This paper presents improved modulation strategies that reduces CMV and/or balances the DC link voltage.

II. NPC CONVERTER AND CLASSICAL MODULATION STRATEGIES

Two classical modulation strategies will be shortly presented. These methods are presented for comparison with the developed modulation strategies.

A. NPC Converter Theory

In order to produce AC voltage waveforms with multiple levels, the diode-–clamped multilevel inverter employs clamping diodes and cascade DC capacitors. This topology can have three, four or five levels. In high power, the configuration that is used most often is three level neutral point clamped inverter. The most important characteristic of the NPC inverter, in comparison with two level inverters is that in AC output voltage dv/dt and THD is reduced [7].

Figure II-1 presents a layout of a NPC inverter leg. This leg is composed of four switches (T1 to T4) with anti-parallel diodes (D1 to D4) and two clamping diodes (D5 and D6). In real life, forward diodes are comprised in the switching device module if they are IGBTs. A zero DC voltage point is present, which ensures the switching of each output phase to one of the three level voltages. The most important benefit of this configuration is that every switching device needs to block only half of the DC link voltage. But new problem is emphasized that DC link created by the two series capacitors needs to be balanced. For this problem there are two solutions [8]:

• Connect each capacitor to its own isolated DC source.
• Balance of the midpoint by feedback control.

The midpoint charge is related to the switching vectors. There are a total number of 24 active vectors which can be split in three categories: large, medium, and small vectors. There are 6 large vectors, 6 medium vectors and 12 small vectors. There are 3 additional zero vectors. The large vectors do not have connection to the midpoint so they are free from charge balance [9].

The influence of these vectors has been studied in [10] and can be seen in Table II-1.

<table>
<thead>
<tr>
<th>State</th>
<th>Vector Type</th>
<th>CMV (V0=0)</th>
<th>CMV (V0≠0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Zero</td>
<td>0</td>
<td>VDC</td>
</tr>
<tr>
<td>NIN</td>
<td>Zero</td>
<td>-1/2 VDC</td>
<td>-1/2 VDC</td>
</tr>
<tr>
<td>PPP</td>
<td>Zero</td>
<td>1/2 VDC</td>
<td>1/2 VDC</td>
</tr>
<tr>
<td>N00</td>
<td>Small</td>
<td>-1/6 VDC</td>
<td>-1/6 VDC</td>
</tr>
<tr>
<td>ON0</td>
<td>Small</td>
<td>1/6 VDC</td>
<td>1/6 VDC</td>
</tr>
<tr>
<td>OON</td>
<td>Small</td>
<td>-1/6 VDC</td>
<td>-1/6 VDC</td>
</tr>
<tr>
<td>POP</td>
<td>Small</td>
<td>1/6 VDC</td>
<td>1/6 VDC</td>
</tr>
<tr>
<td>OPP</td>
<td>Small</td>
<td>-1/3 VDC</td>
<td>-1/3 VDC</td>
</tr>
<tr>
<td>ONP</td>
<td>Medium</td>
<td>0</td>
<td>1/3 VDC</td>
</tr>
<tr>
<td>PPN</td>
<td>Large</td>
<td>1/6 VDC</td>
<td>1/6 VDC</td>
</tr>
<tr>
<td>PNN</td>
<td>Large</td>
<td>-1/6 VDC</td>
<td>-1/6 VDC</td>
</tr>
<tr>
<td>PPN</td>
<td>Large</td>
<td>1/6 VDC</td>
<td>1/6 VDC</td>
</tr>
<tr>
<td>PNP</td>
<td>Large</td>
<td>-1/6 VDC</td>
<td>-1/6 VDC</td>
</tr>
<tr>
<td>PNP</td>
<td>Large</td>
<td>1/6 VDC</td>
<td>1/6 VDC</td>
</tr>
</tbody>
</table>

The 12 small vectors can be split in 6 sets of 2 vectors. The 6 sets have same direction and magnitude according to switching combination and will connect one or two output lines to the upper or lower capacitor. The vectors in each set draw currents opposite in direction from the capacitor bank. By correct selection of small vectors for the reference vector, the balance can be set.

The medium vectors have one vector per current direction. One of the three output lines is permanently connected to the
midpoint. When the reference vector is synthetized with the medium vector the line current flows through the midpoint. If the charge balance cannot be compensated with small vectors, the compensation is given to the next medium vector because it could have opposite current direction [9].

B. Nearest Three Vectors with Even Harmonic Elimination – NTV-EHE

The oldest topology of three level inverters was introduced by Nabae in 1981 [4]. The layout that he proposed is neutral point clamped topology. Compared with conventional voltage source inverters this topology has better spectral performance. The original topology with the neutral point clamped has been expanded to higher number of levels. Multilevel inverters reduce voltage stress on the devices. The required voltage blocking capability of the clamping diodes varies with the levels, thus multiple diodes at higher levels may be required [7].

NTV-EHE was introduced by D. W. Feng and B. Wu in 2004 [11] for compliance with harmonic standards, like IEEE 519-1992, when the converter is used in rectifier mode. The generation of these even order harmonics is due to fact that the waveform generated by SVM is not half – wave symmetrical [11]. In order to obtain half – wave symmetrical voltage at the output and to cancel the line-line even harmonics alternative switching sequences: one starting with N – type vector (A type) and the other with P – type vector (B type) need to be used. This can be seen in Figure II-2.

Figure II-2 Alternation of N and P type sequences in NTV

This method provides low harmonic distortion. The reference vector is synthetized by three stationary space vectors. The stationary vectors are chosen as the nearest three vectors from the region in which the reference vector is found.

C. ZeroCommon Mode - ZCM

The Zero Common Mode Method (ZCM) was first introduced by Haoran Zhang and Annette von Jouanne in 2000 [12]. This method uses the six active middle vectors and one zero vector due to their ability to create zero common mode voltage as long as the DC link is balanced. This can be seen in Figure II-3.

Figure II-3 Switching Vectors for ZCM

This method uses only medium vectors, thus the other type of vectors are going to be neglected. Taking this into account, it can be observed that the maximum vector that can be inscribed in the hexagon of space vectors is given by the medium vector, therefore the maximum utilization of the bus is 86.6% of the utilization the NTV-EHE modulation strategy [10]. Due to the fact that in this method there are no redundant states, the transition between two adjacent states involves two inverter legs that double the switching frequency and increase the harmonic content.

III. PROPOSED MODULATION STRATEGIES

The voltage deviation problem is inherent to all 3L-NPC converters [13]. Neutral point voltage deviation means that any current flowing through the neutral point of a three level inverter would cause the charging of one of the capacitors and the discharging of the other. The effect is that the output becomes asymmetric. The unbalance problem does not appear in two level inverters or in three level inverters with separate DC sources [14].

When applying PWM to a three phase inverter, a voltage between neutral point of the load and ground is generated. This voltage is known as common mode voltage and acts like a source for many unwanted problems in motor drives such as shaft voltage and bearing currents (due to parasitic capacitances that exists in the motor structure) [15].

Based on the influence of the space vectors described in Table II-1 the improved modulation strategies have been developed.

A. One Large One Medium Vector - OLOM

For a proper utilisation of the bus bar, three vectors were chosen: one medium, one large and the zero vector. This method divides the space vector hexagon in 12 sectors with a displacement angle of 30°. Switching vectors for this method are presented in Figure III-1. As ZCM this method does not have the ability to balance the DC link voltage when a voltage drop occurs on one of the capacitors, but it has the ability of natural balancing.

As this method uses medium, large and the zero vectors the largest vector that can be inscribed in the space vector hexagon is the large vector, thus the modulation index is maximum as in NTV-EHE.
Figure III-1 Switching Vectors for OLOM Method in first sector

The reference vector for each sector is comprised by one large, one medium and the zero vector. Dwell times for each device are calculated using the volt-second principle together with the assumption that during switching time the reference voltage vector is constant.

Considering these space vectors and their influence, it can be stated that the influence of NP current is only given by medium vectors, as CMV is produced only by large vectors.

B. Zero Small Medium Large Vector - ZSML

The idea behind this method is to use all available levels of voltage in order to keep THD low while having the possibility to balance the DC link. In natural balancing mode the CMV levels are half of NTV-EHE. The switching vectors for first sector can be seen in Figure IV-1.

Figure III-2 Switching vectors for ZSML Method for first sector

The dwell times are calculated based on volt-second principle. Distinctive for this method is that the dwell time for zero vector is equal to $1 - \frac{v_{ref}}{v_{ref,max}}$.

In order to have natural balancing in odd sectors the N type small vector is used and P type small vector in even sectors.

IV. PROPOSED MODULATION STRATEGIES VALIDATION THROUGH SIMULATION AND EXPERIMENTAL RESULTS

For a proper validation of the two proposed modulation strategies simulations and an experimental PCB were developed. The simulations were performed in Matlab/Simulink and Plecs.

The 3L-NPC inverter was modelled based on the simplified hardware schematic from Figure IV-1:

Figure IV-1 Simplified schematic of the designed NPC converter

This inverter has the following main features:
- Embedded TMS320F28335 DSP design.
- 4 layer PCB with stacked DC link layout, ground and power planes.
- Design based on NPC leg IGBT modules (Semikron SK50M60H065).
- Adjustable over temperature, overcurrent and overvoltage protection.
- Xilinx XC9572XL CPLD based dead time and protection management.
- Real time PWM signal analysis and protection.
- DC link up to 1kV.
- Shielded ADC and PWM signals.
- RS-232, RS-485 and CAN communication.
- Optocoupler galvanic isolated gate driver with active Miller clamping.
- Desaturation detection.
- JTAG interface for DSP and CPLD.
- Hall effect current sensors.
- Mixed analogue and digital design.
- Reduced size.

This inverter can be seen in Figure IV-2.

Figure IV-2 NPC Converter developed for experimental validation of proposed modulation strategies
A. Validation through simulations

Extensive simulations have been developed in order to validate the proposed modulation strategies. Figure IV-3 presents the simulation results regarding phase-to-phase voltage of the two classical methods and the two proposed methods.

The modulations were performed using the equivalent model of a 7.5 kW IM with star – neutral connection. The DC link is set at 600 V and equivalent capacitance of upper and lower capacitor is 0.99 µF. The waveforms are obtained when the motor reaches steady state. Switching frequency is set a 4 kHz with a 2µs deadtime.

Industry standard modulation strategy is NTV. A newer method, ZCM, benefits in a great reduction in the CMV with the disadvantage of THD increase. Using only the medium vectors, ZCM manages to keep the CMV very low in comparison with NTV while this benefits of lower THD due to use of 3 vector sizes. This is reflected in the number of voltage levels, which is 9 for NTV and 3 for ZCM. Also, the modulation index is lower for ZCM. The line voltages for NTV and ZCM are found in Figure IV-3.

The first proposed method, OLOM retains the maximum modulation of NTV while using only large, medium and zero vectors. The line voltage can be seen in Figure IV-3. The second proposed method, ZSML has the distinctive feature of using 4 vectors: zero, small, medium and large. The line voltage is comparable to the waveform for OLOM. Using 4 vectors sizes comes with a THD decrease of 1.38% over NTV and 24.96% lower than ZCM.

The CMV for NTV has a range of ±200 V. The ZCM has very low CMV, under 5V on all frequencies. The CMV present is due to the influence of dead time.

The CMV range for OLOM is little over half of NTV for a THD increase in the line voltage of 6.34% compared to NTV and 17.24% lower than ZCM. The increase is also for using 7 voltage levels compared with NTVs 9 levels. The CMV can be seen in Figure IV-4. As it can be seen in the FFT in Figure IV-5, OLOM has 60% lower amplitude at the switching frequency, compared to NTV. The CMV is lower on all frequency ranges.
The CMV range for ZSML is also lower than half of the NTV as seen in Figure IV-4. The specific of this method is the extra ability to balance the DC link in the case of an external influence. The values shown are for steady state when in natural balancing mode.

B. Validation through experimental work

The hardware presented at the beginning of this chapter was built in order to validate the proposed modulations strategies. As a load to this inverter a 1.5 kW IM has been used.

The experimental results of the phase-to-phase voltage in time domain regarding classical and proposed modulation strategies can be seen in Figure IV-6. It can be observed that the modulation strategies maintain the same characteristics as in simulations.

The CMV in time domain of these modulation strategies can be seen in Figure IV-7. Voltage levels discussed on simulation results are maintained, as well as spectral analysis. This can be seen in Figure IV-8.
THD in the line voltage for each method shows a good correspondence between simulation and experiments. In the experimental setup, the THD is higher with only 2-3%. The effect of this can be seen as a lower fundamental frequency in the CMV spectral analysis. The results confirm the feasibility of the proposed methods.
V. ASSESSMENT OF THE PROPOSED MODULATION STRATEGIES

For a better view on the proposed modulation strategies, a comparative analysis has been done. This can be seen in Table V-1 — Comparative Analysis between Modulation Strategies Table V-1.

The two new proposed strategies seem prospective as they offer performance improvements. OLOM reduces the CMV on all frequencies while preserving modulation index compared to NTV. While having same amplitude of CMV at the low fundamental frequency of 150 hz, it has 40% lower amplitude at the switching frequency of 4 khz. It is also comparable with ZCM because it makes better use of the three level topology, preserving the maximum modulation index and lower THD.

Also, ZSML seems promising. The THD is lower than NTV and ZCM while the CMV distribution is more than half lower on all switching frequencies compared to NTV. While preserving the maximum modulation index, the method is able to balance the dc-link in the case of an external event, which is a great advantage. Both methods are comparable with ZCM in the high frequency range, where the effects of CMV are highest.

<table>
<thead>
<tr>
<th>Table V-1 – Comparative Analysis between Modulation Strategies</th>
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<tr>
<td></td>
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<tr>
<td>Phase / Line Voltage Levels</td>
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<tr>
<td>Modulation Index</td>
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<tr>
<td>DC link balancing</td>
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<tr>
<td>CMV Levels [V]</td>
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<tr>
<td>Simulation ph-ph THD&lt;sub&gt;s&lt;/sub&gt;</td>
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<tr>
<td>Experiment ph-ph THD&lt;sub&gt;s&lt;/sub&gt;</td>
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Special thanks go to their friends and family for their moral support during this project.

REFERENCES


Appendix 11: Contents of the CD

The CD will contain the following folders and documents:

- Report.
- CPLD Program ISE Design Suite: this folder contains the CPLD program that has integrated deadtime programming and protections.
- Developed Modulation Strategies – Matlab Simulation: this folder contains the simulations regarding classical and developed modulation strategies.
- Modulation Strategies – DSP Code Composer C++: this folder contains the C++ code implemented into DSP regarding the classical and developed modulation strategies,
- NPC Inverter Design – Altium: the PCB layout of the three level NPC converter designed in Altium.
Appendix 4 Report - Sensor less Control of PMSM Using Three Level NPC Converter

This report continues the work of Appendix 3, but addressing the operation of the DeepWind generator (referred to as Permanent Magnet Synchronous Machine in the report). A second small scale inverter was built for testing with the small scale generator prototype previously built in the DeepWind project to validate the equations used in the generator design tool.

As the converter has to control the generator in various modes of operation, many of these are simulated and tested in the laboratory.

It was assumed that the wind turbine control system issues a speed reference to the converter control, as this is the only way to control the Darreius wind turbine that has no equipment to change the pitch of the blades. The converter controller then determines the corresponding response of the converter and controls the converter accordingly.

Author: Florin Valentin Traian Nica
SENSORLESS CONTROL OF PMSM USING THREE LEVEL NPC CONVERTER
Title: Sensorless control of PMSM using three level NPC converter
Semester: 10th
Semester theme: Optimisation, Diagnostics and Control of Power Electronic Drives of Converters
Project period: 01.09.2013 – 27.05.2014
ECTS: 50
Supervisor: Ramkrishan Maheshwari; Ewen Ritchie; Krisztina Leban;
Project group: PED4-1045

SYNOPSIS:
This project is focused on the construction of a three level neutral point clamped prototype converter, for a wind turbine application. The converter has to ensure the control for a vertical axis Darreius wind turbine, which has special requirements for the system. Two sensorless control strategies are implemented and tested in laboratory experiments, to determine the best method. The conclusion of the experiments is that sensorless field oriented control is the most adequate control to be implemented for this type of application.

Florin Valentin Traian Nica

Copies: 3
Pages, total: 83
Appendix: 3
Supplements: CD

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.
Preface

The current report, entitled “Sensorless control of PMSM using three level NPC converter” was written by Florin Valentin Traian Nica, master student of Power Electronics and Drives, at the Department of Energy Technology, Aalborg University, Denmark.

The project was proposed by Ewen Ritchie, associate professor, and Krisztina Leban, Ph.D. student, as part of a European Programme contracted by Aalborg University, called DeepWind. The span of the project was one school year, started on 1st of September 2013 and finished on 27th May 2014, thus being the master thesis project of the author.

Reading Instructions

The text is divided into seven chapters plus two appendixes. The chapters are consecutive numbers, whereas the appendixes are labelled with capital letters.

The references are shown in form of number placed into square brackets. Additional information about each reference is presented in Bibliography.

The format of equations is (X.Y), where X is the chapter number and Y is the equation number.

The format of figures is Fig. X.Y, where X is the chapter number and Y is the figure number.

The format of tables is TABLE X.Y, where X is the chapter number and Y is the table number.

The enclosed CD-ROM contains the report in Word and PDF format, two Matlab Simulink models, which present different approaches of constructing the model, an extra Matlab Simulink Library, constructed by the author and images with laboratory results.

Acknowledgments

The author will like show its gratitude to the supervisors, for their extensive support during the entire project period. Special thanks are made to Krisztina Leban and Ewen Ritchie, for their financial and moral support during the two year master programme.
Summary

In order to help the reader understand the structure of the report, a summary of all the chapters is made in the following.

1. Introduction

This chapter presents at the beginning a short retrospective of wind energy evolution during the last years. This retrospective is necessary to understand the way the European Union has proposed the DeepWind Programme.

A short description of the DeepWind Programme is presented afterwards, along with the tasks that Aalborg University has to fulfil.

Because one of these tasks represents the starting point for the current master thesis, a more detailed description is made about this task.

The last part of the chapter presents the objectives along with the limitations.

2. Theoretical Background

The most important theoretical concepts used during the project are presented in this chapter.

The chapter starts by presenting the three level neutral point clamped (NPC) converter, because this topology is used for the prototype. Only the most important information about the converter is presented here, along with a selection of references.

The problem and solution for the neutral point voltage balance is presented, because this topic is very important for the NPC, and it is part of the practical implementation.

The chapter continues by presenting the permanent magnet synchronous machine (PMSM) model, in a short section.

The state of the art for scalar and vector control is presented in the last part of the chapter, along with the control theory specific for PMSM.

3. Control Description and Implementation

This chapter presents which control methods are selected for the project. Because a decision was made to use both scalar and vector control, these two are presented separately.

Scalar control is presented first, followed by vector control. As it can be seen from the report, these two control methods have a similar structure with similar components. All these similar components will be presented, in the vector control subchapter, to avoid repeating the same theory twice.

After each control method is described, the implementation process is presented. This implementation process provides the PI controller parameters.
The last part of the chapter presents the speed and position estimator. Although the estimator is used for vector control, it is presented in a separate subchapter, because it represents the most important component of the control.

4. Simulations

Using the information from chapter two and three, a Simulink model of the entire system is created. These simulations were selected based on the second objective. The results are presented for each simulation, along with necessary explanation.

5. Hardware Design of Converter

The main circuits of the three level NPC prototype are presented in this chapter. Only general block diagrams are used to highlight the main circuits, because the design was not made during this project. For a more detailed description of the prototype and the components, references are provided.

6. Laboratory Experiments

During this chapter, all the laboratory experiments are presented with measurements and explanations. In order to have a comparison between the Simulink model and the real system, the tests are made under similar conditions as the simulations.

7. Conclusions

This chapter presents the main conclusions of the project.

Appendix A. Reference Frame Transformation

The reference frame transformations used in the report are presented.

Appendix B. Neutral Point Voltage Balance Results

The voltage measurements obtained, using space vector modulation, are presented at the beginning. The rest of the appendix presents the DC link voltages for all the experiments, obtained using sinusoidal pulse width modulation.

Appendix C. Numeric Parameters

All the numeric values used during the project are presented in this appendix. These numeric values represent the machine parameters, the control parameters and the convertor parameters.
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7 Conclusions

Appendix A. Reference Frame Transformation
Appendix B. Neutral Point Voltage Balance Results
Appendix C. Numeric Parameters
Chapter 1. Introduction

1 Introduction

This chapter presents the wind energy evolution in the last years at a global level. The focus will be then changed to the European Union and its programmes, which support the development of renewable energies. A short presentation of one of these programmes, contracted by Aalborg University, called DeepWind, will be made, to relate the requirements of the programme with the project at hand. The objectives of this project will be presented in the second part, along with necessary information for each objective. The final part of the chapter will present the limitations imposed for the project.

1.1 Wind Energy Evolution

Political and economical conditions have lead to a significant increase in research and development of renewable energies in the last decade [1, 2]. Because of this, wind energy has become one of the mainstream renewable technologies with more than 300,000MW installed globally until 2013 [2], as it can be seen from Fig. 1.1.

![Fig. 1.1. Global cumulative installed wind capacity 1996-2013 [2].](image)

From the total amount of wind power installed globally until 2013, Europe is the leading region, with 38% of the total installed renewable power [2], which covers approximately 7% of the electricity demand.

Europe is the leader in installed wind power due to the policies implemented, and due to the long term objectives imposed by the European Union [3]. These targets, presented in [3], require that by 2050, 50% of the energy consumed in Europe to be produced by wind turbines.

In order to achieve this goal, massive investments are made in research and development, to increase the energy capacity of each generator, and to provide better solutions for the structure [3]. As a result, the average generator capacity installed each year has increased from 200kW for onshore and 450kW for offshore in 1991, to 1,700kW for onshore and 2,800kW for offshore in
2010 [3]. This trend is expected to be maintained in the future, allowing for an increase above 3,000kW.

<table>
<thead>
<tr>
<th>Year</th>
<th>Onshore wind (GW)</th>
<th>Offshore wind (GW)</th>
<th>Total wind energy capacity (GW)</th>
<th>Averag e capacity factor onshore</th>
<th>Averag e capacity factor offshore</th>
<th>(TWh) onshore</th>
<th>(TWh) offshore</th>
<th>(TWh) total</th>
<th>EU-27 gross electricity consumption</th>
<th>Wind power’s share of electricity demand</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020</td>
<td>190</td>
<td>40</td>
<td>230</td>
<td>26%</td>
<td>42.3%</td>
<td>433</td>
<td>148</td>
<td>581</td>
<td>3,690</td>
<td>16%</td>
</tr>
<tr>
<td>2030</td>
<td>250</td>
<td>150</td>
<td>400</td>
<td>27%</td>
<td>42.8%</td>
<td>591</td>
<td>562</td>
<td>1,154</td>
<td>4,051</td>
<td>29%</td>
</tr>
<tr>
<td>2050</td>
<td>275</td>
<td>460</td>
<td>735</td>
<td>29%</td>
<td>45%</td>
<td>699</td>
<td>1,813</td>
<td>2,512</td>
<td>5,000</td>
<td>50%</td>
</tr>
</tbody>
</table>

The European Union is supporting this development thought Framework Programmes since 1984 and plans to continue at least until 2020 [4]. Aalborg University is one of the participants engaged in one of these programmes called DeepWind [5]. A short description of the programme is presented in the following section.

1.2 DeepWind Programme

The DeepWind programme was proposed on the hypothesis that a new wind turbine concept, developed specifically for offshore, has potential for better cost efficiency than existing offshore technology [5].

Considering this hypothesis a series of objectives have been set [5]:

- To explore the technologies needed for development of a new, simple, floating offshore concept, with a vertical axis rotor, and a floating and rotating foundation;
- To develop calculation and design tools for development and evaluation of very large wind turbines, based on this concept;
- Evaluation of the overall concept with floating offshore horizontal axis wind turbines;

As part of the DeepWind programme Aalborg University is responsible for a series of tasks:

- Design the bearings of the wind turbine;
- Construct a design tool which is able to design a wind turbine generator in the range of 5 to 20MW, specific for an offshore application;
- Propose a converter topology adequate for this application;

As an integrated part in the DeepWind Programme, the current master thesis focuses on the converter topology for the wind turbine.
1.3 Converter and Control for DeepWind Programme

In order to identify the best converter topology for the current application, a student project was proposed at Aalborg University [6]. The project concluded that the best topology to be used in this situation is the three level neutral point clamped (NPC) converter [6].

This converter topology is preferred, instead of the two level converter, which is most widely used, because of its advantages as: reduced voltage across each switch (only half of the DC link voltage per each switch, compared to the entire DC link voltage per each switch, for the two level), reduced current ripple losses, reduced switching/conduction losses and reduced total harmonic distortion.

The decision was made to use the three level NPC converter. A small scale prototype of the converter is built. This step is considered to be the first objective of the current master thesis, which will be presented in more detail in the following subchapter.

Although the control of the converter is not a task required for Aalborg University, by the DeepWind Programme, it will be considered as an objective for the current master thesis.

When the control strategy is developed, the particularities specific to this application must be taken into consideration. As a start, it should be noted that the participants engaged in this project, responsible with the structure of the wind turbine, have proposed a vertical axis Darrieus type turbine.

This turbine has to be anchored to the bottom of the sea, leaving the entire structure to float. Because of the uniqueness of the construction, the generator along with the converter will be located underwater, at the bottom of the wind turbine.

The Darrieus wind turbine imposes special requirements for the control strategy, requirements which must be taken into consideration when the control is elaborated. These special requirements, specific to the Darrieus wind turbine, are presented in the following:

- The unique structure restricts it from self-starting even with high levels of wind speed. Hence, the generator will have to work as a motor in the starting phase and accelerate the turbine until a certain rotating speed is reached. During the start procedure, since the machine will be working as a motor, power will be consumed from the grid;
- Stopping the turbine. The size and weight of the entire structure creates a very large moment of inertia, and because the turbine cannot be stopped using traditional mechanical breaks, the generator has to be able to stop the entire structure;
- Pitch control cannot be implemented for this system, since the blades of the turbine are fixed. Hence the entire structure will have to be controlled by the generator via the converter.

Based on the information presented and the requirements imposed by the DeepWind Programme, the objectives for the current master thesis can be elaborated.
1.4 Project Objectives

To have a clear understanding of why the following objectives are selected for this project, each objective will be presented in a separated section, along with all the necessary information.

**Objective 1:**
A three level NPC prototype converter has to be constructed.

The prototype is constructed as a requirement of the DeepWind Programme, to test the topology proposed for the main converter. A secondary reason is that the converter has to drive a small scale generator prototype, which was constructed to test the analytical design program.

The main beneficiaries of this objective are the people involved in the DeepWind project and the author of this thesis, because of the experience gained while constructing a converter and working in a laboratory.

The PCB schematics used in the current project are taken from a previous AAU project [7], in order to save time with converter design. All the components are ordered according to the bill of materials, provided in the project, and the soldering and testing part is made by the author, in the laboratory.

**Objective 2:**
Propose suitable control strategies for the converter, in different working situations as:

- starting the turbine as motor;
- working as a motor;
- working as a generator;
- emergency breaking;
- holding the turbine at zero speed;

The Darreius wind turbine imposes special requirements for the converter, like the ones presented in the Converter and Control for DeepWind Programme subchapter presented earlier. The control implemented on the converter has to be able to handle all these situations;

The main beneficiary of this objective is the author conducting this report, because it has to study the state of the art methods in control strategies, and propose suitable ones for this project. Also the DeepWind Programme will benefit from this objective, ensuring that tests can be made in different situations.

To complete this objective, a review of the state of the art methods in control is made. Using the information gained, the most suitable method that can be applied on this system is selected.

**Objective 3:**
Construct a mathematical model of the system and simulate the proposed control strategies.

The simulations are made to: test the functionality of the system, test the control strategies selected during the previous objective and to improve the control by tuning the system. Also, the
simulation provides important information before the real system is tested, information which can be used to improve the system and to reduce the implementation time.

After the model is constructed in Matlab Simulink, the control is implemented to drive the system. In order to validate the control, numerous simulations are made using the conditions imposed at objective two.

**Objective 4:**
Test the converter in the laboratory for all the situations simulated.

On the constructed converter, the proposed control strategies are tested to validate the behaviour of the system and to verify its functionality.

The author of this report is the main beneficiary of this objective because it has the chance to learn how to build a setup in the laboratory, study, develop and implement DSP programming on the convertor and test the overall system;

With the constructed converter, and the available machine prototype, provided by the DeepWind project, the setup is made. The control is implemented on a DSP, thus providing the control for the converter.

### 1.5 Project Limitations

Because of limited time and/or resources some limitations have to be imposed to the project:

- The design of the converter is not an objective for this project. The design presented in [7] will be used to construct the converter.
- Sinusoidal pulse width modulation, without DC balance capabilities, is used in laboratory experiments;
- Because field weakening control is not an objective for this project, it was only presented as a theoretical concept. Experimental tests were made in the laboratory, using this control, but are not presented in the report.
Chapter 2. Theoretical Background

This chapter presents the main theoretical topics that will be required to handle the objectives. The focus is placed on the most important components of the system: converter, machine and control. In the first section, a short description of the three level NPC converter is made, information which is required to understand its structure and functionality. The model of the permanent magnet synchronous machine in rotating “dq” reference frame is presented afterwards. The state of the art control methods that can be applied for this type of machine are presented in the last section.

2.1 Three Level NPC Converter

The circuit diagram of a three level neutral point clamped (NPC) converter is presented in Fig. 2.1. [8]. It can be observed that two capacitors ($C_{d1}, C_{d2}$) are placed on the DC link, creating a neutral point 0. The two diodes connected to the neutral point ($D_{c1}, D_{c2}$) are called clamping diodes. $E$ is the voltage across the DC capacitors and it is normally half of the DC voltage $V_{dc}$, but neutral point voltage deviation can appear because the capacitors are charged and discharged by the neutral current $i_0$ [8].
The working procedure of the convertor is represented by the switching states of each phase. Since the procedure is similar for each phase, only the switching states for phase A are presented in TABLE 2.1.

<table>
<thead>
<tr>
<th>Switching State</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>Phase Voltage ((V_{A0}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>E</td>
</tr>
<tr>
<td>0</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>0</td>
</tr>
<tr>
<td>N</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>-E</td>
</tr>
</tbody>
</table>

As it can be seen from the table, in order to obtain at the output of the convertor a positive voltage equal with the voltage across the capacitor \(E\), the upper two switches \(S_1\) and \(S_2\) have to be on and the lower two switches \(S_3\) and \(S_4\) have to be off. This is also called the \(P\) switching state because it produces a positive voltage at the output.

To obtain a negative voltage at the output, with the same magnitude, the status of the switches has to be opposite to the \(P\) state, and this is called \(N\) switching state.

The three level NPC converter is also able to produce a zero voltage level at the output, which is determined by the switching state \(0\), when the interior switches \((S_2\) and \(S_3\)) are on, and the exterior switches are off \((S_1\) and \(S_4\)).

From these three switching states \((P, N\) and \(0\)) it should be noted that switch one and switch three always work in opposition \((S_1 = \bar{S}_3\)), same as switch two and four \((S_2 = \bar{S}_4\)).

By properly controlling these switching states, on all three phases, the neutral point voltage unbalance can be eliminated. The reasons why this phenomenon can appear are presented in the following section.

2.2 Neutral Point Voltage Balance

The neutral point voltage balance can be influenced by numerous parameters [8], as: different parameters for the DC link capacitors, DC capacitor failure, different parameters for the switching devices and unbalanced loads.

If the neutral point voltage balance problem is not considered and corrected, problems can appear in the system [8], as: premature failure of the switching devices, increased total harmonic distortion, modulation ratio limited by the terminal with the lower voltage.

This problem can be solved by applying the adequate switching state on each of the three phases. To have a unified notation of the switching state on all three phases, the space vector term was introduced [8]. The space vector considers the switching state on each phase, by using the output phase voltage, and it can be expressed using the following equation:
\[ \bar{V}_s = \frac{2}{3} [V_{A0} + aV_{B0} + a^2V_{C0}] \]  

(2.1)

, where: \( \bar{V}_s \) - space vector;

\( V_{A0} \) - voltage on phase A (considering the neutral point 0 as reference);

\( a = e^{j(2\pi/3)} \);

A more detailed explanation regarding the space vector term will be made in the following sections. At this point it is sufficient to know that the three level NPC converter has the ability to generate four groups of space vectors based on their magnitude, each corresponding to different switching states (TABLE 2.3).

Each of these space vectors has a different influence on the neutral point voltage [8], influence that will be analyzed in the following, using the switching states presented in Fig. 2.2.

**Zero space vectors** (Fig. 2.2.a.) have no influence on the neutral point voltage balance, because they ensures the connection of the converter terminals (A, B and C) with only one of the DC states at a time (positive, zero or negative DC voltage) [8].

**Small space vectors** have a powerful influence over the voltage balance. This is because when a P switching state is active (Fig. 2.2.b.), the load is connected between the positive DC voltage and neutral point, causing the current \( i_0 \) to flow towards the neutral point 0, which increases \( V_0 \). In the opposite situation, when an N switching state is active (Fig. 2.2.c.), the current \( i_0 \) flows from the neutral point 0 towards the negative point N, causing a decrease in \( V_0 \) [8].

**Medium space vectors** (Fig. 2.2.d.) also have an influence over the neutral point voltage balance. Even thought at each moment one converter terminal is connected to a different DC point, the voltage \( V_0 \) can increase or decrease depending on the operating condition [8].

**Large space vectors** (Fig. 2.2.e.) do not affect the voltage balance of the neutral point [8]. This is because the load terminals are connected between the positive and negative DC terminals, while the neutral point is left unconnected [8].
Chapter 2. Theoretical Background

1. Zero space vector [000].
2. Small space vector (P type) [PP0].
3. Small space vector (N type) [00N].
4. Medium space vector [P0N].
5. Large space vector [PPN].

Fig. 2.2. Effect of space vectors on neutral point voltage balance [8].

By adequately controlling the space vectors during the modulation, neutral point voltage balance can be achieved. Two of the most widely used modulation strategies will be presented in the following.

2.3 Modulation Strategies

Numerous modulation strategies have been proposed for the three level NPC converter [9]. The most common known and used are:

- Sinusoidal pulse width modulation (SPWM);
- Space vector modulation (SVM);

2.3.1 Sinusoidal PWM

This method is based on the comparison between a sinusoidal reference signal and two carrier signals ($V_{c1}, V_{c2}$).
Because the first carrier signal $V_{c1}$ is always bigger than the second carrier signal $V_{c2}$, and because the switches work in opposition ($S_1 = \overline{S}_3$ and $S_2 = \overline{S}_4$), it is sufficient to define two states for the PWM logic (TABLE 2.2).

<table>
<thead>
<tr>
<th>Cases</th>
<th>Switch State</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{sin}} &gt; V_{c1}$</td>
<td>$S_1 = \overline{S}_3 = ON$</td>
</tr>
<tr>
<td>$V_{\text{sin}} &lt; V_{c2}$</td>
<td>$S_2 = \overline{S}_4 = ON$</td>
</tr>
</tbody>
</table>

Besides the classical method presented here, were the modulation signal is sinusoidal with only one frequency component, there are numerous others sinusoidal PWM strategies developed to improve the quality of the result [9].

SPWM can be used as a modulation strategy because it ensures a natural balance in the DC link, when no external factors affect the system. The disadvantage of this method appears when an external factor influences the DC neutral point voltage. In this situation the balance cannot be ensured, which can cause a fault to appear in the system.

In order to provide a safe operation, even when external factors affect the DC link voltage, a different modulation strategy has to be used. This strategy is presented in the following.
2.3.2 Space Vector Modulation

The three level NPC converter has $3^3=27$ switching states combinations, which can generate different space vectors. A classification of all the space vectors obtained using (2.1) is made based on magnitude and type, in TABLE 2.3.

**TABLE 2.3**

<table>
<thead>
<tr>
<th>Vector Classification</th>
<th>Vector Magnitude</th>
<th>Space Vector</th>
<th>Switching State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_0}$</td>
<td>P type</td>
</tr>
<tr>
<td>Zero Vector</td>
<td>0</td>
<td>$\overrightarrow{V_1}$</td>
<td>P00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_2}$</td>
<td>PP0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_3}$</td>
<td>0P0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_4}$</td>
<td>0PP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_5}$</td>
<td>00P</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_6}$</td>
<td>P0P</td>
</tr>
<tr>
<td>Small Vector</td>
<td>$\frac{1}{3}V_{dc}$</td>
<td>$\overrightarrow{V_7}$</td>
<td>P0N</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_8}$</td>
<td>0PN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_9}$</td>
<td>NP0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_10}$</td>
<td>N0P</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_11}$</td>
<td>0NP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_12}$</td>
<td>PN0</td>
</tr>
<tr>
<td>Medium Vector</td>
<td>$\frac{\sqrt{3}}{3}V_{dc}$</td>
<td>$\overrightarrow{V_{13}}$</td>
<td>PNN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_{14}}$</td>
<td>PPN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_{15}}$</td>
<td>NPN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_{16}}$</td>
<td>NPP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_{17}}$</td>
<td>NNP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\overrightarrow{V_{18}}$</td>
<td>PNP</td>
</tr>
</tbody>
</table>

As it can be observed from TABLE 2.3 and from Fig. 2.2, only the small space vector has two switching state types, positive and negative. These two types produce a space vector with the same magnitude and angle. The difference between the two switching states is the direction of the neutral current $i_0$. For the positive type the current enters the DC link, while for the negative type the current is taken out of the DC link.
Using the space vectors presented in TABLE 2.3 in the correct manner, the neutral point voltage balance can be maintained, even when external influences affect the DC voltage [8]. A modulation technique which has this capability is presented in the following [7].

In order to understand which space vectors must be for each situation, all the space vectors are arranged in a diagram made out of six sectors, each sector having two regions, as it can be seen in Fig. 2.4 and Fig. 2.5.

From Fig. 2.5, it can be seen that the first region is situated between [0, 30] and the second region is situated between [30, 60]. Another important information that has to be considered is that each region contains four space vectors. For example, sector one, region one contains: \( \overrightarrow{V_0}, \overrightarrow{V_1}, \overrightarrow{V_7} \) and \( \overrightarrow{V_{13}} \).

The neutral point voltage balance is maintained by alternating the small space vector from positive type to negative type, when there is no fault in the system. When the voltage on the lower capacitor\( (V_0) \) increases above a predefined value, the negative type small space vector is used in the modulation, to draw the current out of the DC link. In the opposite situation, when the voltage on the lower capacitor\( (V_0) \) decreases below a predefined value, the positive type small space vector is used, to send current to the DC link.

In order to use all four space vectors the modulation index has to be considered. The modulation index is defined as:

\[
m_i = \sqrt{3} \frac{V_{ref}}{V_{dc}}
\]

, where: \( V_{ref} \) - magnitude of the reference voltage;
The modulation index is in the [0, 1] range because the maximum magnitude of the reference vector \( V_{\text{ref}} \) corresponds to the radius of the largest circle that can be inscribed within the hexagon in Fig. 2.4, which is equal to the medium space vectors.

The modulation index will determine the dwell time for the zero space vector \( V_0 \) according to:

\[
T_d = (1 - m_i) \cdot T_s
\]

(2.3)

where: 
- \( T_d \) - dwell time for the zero space vector;
- \( T_s \) - sampling time;

As it can be seen from (2.3), if the modulation index is equal to one, the zero space vector is not used.

In order to calculate the required dwell time for the other three space vectors, the volt-second balance principle is applied.

This principle states that the product between the reference voltage \( V_{\text{ref}} \) and the sampling time \( T_s \) is equal to the sum of voltage multiplied by the time of the chosen space vectors [8].

To better explain this principle it will be consider that the voltage reference vector \( V_{\text{ref}} \) is situated in sector one, region one. This means that the nearest three vectors are \( V_1, V_7 \) and \( V_{13} \).

Based on the volt-second balance principle the equations can be written:

\[
V_1 t_a + V_7 t_b + V_{13} t_c = V_{\text{ref}} T_s
\]

(2.4)

\[
t_a + t_b + t_c = T_s
\]

(2.5)

where: \( t_a, t_b, \) and \( t_c \) are the calculated dwell times for \( V_1, V_7 \) and \( V_{13} \), not the final dwell times.

The space vectors are expressed in the following form:

\[
V_{\text{ref}} = V_{\text{ref}} e^{j\theta}
\]

\[
V_1 = \frac{1}{3} V_{dc}
\]

\[
V_{13} = \frac{2}{3} V_{dc}
\]

\[
V_7 = \frac{\sqrt{3}}{3} V_{dc} e^{j\pi/6}
\]

(2.6)

Substituting (2.6) in (2.4) yields:

\[
\frac{1}{3} V_{dc} t_a + \frac{\sqrt{3}}{3} V_{dc} e^{j\pi/6} t_b + \frac{2}{3} V_{dc} t_c = V_{\text{ref}} e^{j\theta} T_s
\]

(2.7)

From (2.7), if Euler’s formula is applied and the real part is separated from the imaginary part the following two equations can be obtained [8]:

\[
\text{Re: } t_a + \frac{3}{2} t_b + 2 \cdot t_c = \sqrt{3} m_i T_s \cos \theta
\]

(2.8)

\[
\text{Im: } \frac{1}{2} t_b = m_i T_s \sin \theta
\]

(2.9)
Because there are three unknowns \( t_a, t_b, \) and \( t_c \) and only two equations (2.8) and (2.9), equation (2.5) is added to the system. Solving the system of equations and extracting the modulation index from each equation will result in:

\[
\begin{align*}
t_a &= 2T_s - T_s(\sqrt{3}\cdot \cos \theta + \sin \theta) \\
t_b &= 2T_s \sin \theta \quad \text{for } \theta \in \left[0, \frac{\pi}{6}\right] \\
t_c &= -T_s + T_s(\sqrt{3}\cdot \cos \theta - \sin \theta)
\end{align*}
\]

Because there are four space vectors used for modulation, the calculated dwell times \( t_a, t_b, \) and \( t_c \) must be divided by the modulation index. The division creates the required time for the zero space vector. The four dwell times used in the modulation are:

\[
\begin{align*}
T_a &= \frac{t_a}{m_i} \\
T_b &= \frac{t_b}{m_i} \\
T_c &= \frac{t_c}{m_i} \\
T_d &= (1 - m_i) \cdot T_s
\end{align*}
\]

The same procedure is applied for the second region and the calculated dwell times are:

\[
\begin{align*}
t_a &= 2T_s - T_s(\sqrt{3}\cdot \cos \theta + \sin \theta) \\
t_b &= T_s(\sqrt{3}\cdot \cos \theta - \sin \theta) \quad \text{for } \theta \in \left[\frac{\pi}{6}, \frac{\pi}{3}\right] \\
t_c &= -T_s + 2T_s \sin \theta
\end{align*}
\]

If the reference vector is placed in another sector (II to VI) the same equations as for the first sector can be used, keeping into consideration the difference between region one and two. Before the dwell time calculations, the angle has to be reduced to the first sector, as in (2.17).

\[
\theta_n = \theta - \frac{\pi}{3}(n - 1)
\]

, where: \( \theta_n \) – the angle reduced to sector one;

\( \theta \) – reference vector position (angle of \( \overrightarrow{V_{ref}} \));

\( n \) – the sector number.

**2.4 Permanent Magnet Synchronous Machine Model**

In order to construct the mathematical model of a permanent magnet synchronous machine (PMSM) the following assumptions are made [10]:

- Saturation is neglected;
- The induced electromagnetic force (EMF) is sinusoidal;
- Eddy currents and hysteresis losses are negligible;
- There are no field current dynamics;
- The “d” axis is aligned with the permanent magnet flux linkage \( \lambda_{pm} \).
Chapter 2. Theoretical Background

The voltage equations in rotating “dq” reference frame are:

\[ v_d = R_s i_d + \frac{d\lambda_d}{dt} - \omega_r \lambda_q \]  
\[ v_q = R_s i_q + \frac{d\lambda_q}{dt} + \omega_r \lambda_d \]  

(2.18)  
(2.19)

, where:  
\( v_{d,q} \) - voltage on d, q axis [V];  
\( i_{d,q} \) - current on d, q axis [A];  
\( R_s \) - stator resistance [Ω];  
\( \lambda_{d,q} \) - flux linkage on d, q axis [Wb];  
\( \omega_r \) - rotor electrical speed [rad/sec];

The flux equations are:

\[ \lambda_d = L_d i_d + \lambda_{pm} \]  
\[ \lambda_q = L_q i_q \]  

(2.20)  
(2.21)

, where:  
\( L_{d,q} \) – inductance on d, q axis [H];  
\( \lambda_{pm} \) - flux linkage due to magnets placed on the rotor, which links the stator [Wb];

The electromagnetic torque equation is:

\[ T_e = \frac{3}{2} p [(L_d - L_q) i_d + \lambda_{pm}] i_q \]  

(2.22)

, where:  
\( T_e \) – electromagnetic torque [N · m];  
\( p \) - number of pole pairs;

For the special case presented by the PMSM, where the inductances along the d and q axes are equal \((L_d = L_q)\), equation (2.22) can be simplified to:

\[ T_e = \frac{3}{2} p \lambda_{pm} i_q \]  

(2.23)

The dynamic equation for the speed of the machine is:

\[ J \frac{d\omega_m}{dt} = T_e - T_L - B \omega_m \]  

(2.24)

, where:  
\( J \) - moment of inertia [kg · m²];  
\( \omega_m \) - rotor mechanical speed [rad/sec];  
\( T_L \) - load torque [N · m];  
\( B \) – viscous friction constant [−].
2.5 Control of PMSM

Depending on the multitude of application where drives are being used, numerous types of control strategies have been developed during the time, starting from the most basic ones, as using a variable resistor to manipulate the voltage, to the most advance ones as servo-drive control [11]. The difference between all these control strategies is in the ease of implementation, performance and cost. In order to have an idea of the difference between different control strategies a comparison from [11] is presented in the following.

### TABLE 2.4

<table>
<thead>
<tr>
<th>Performance Comparison Between Different Control Strategies and Possible Applications [11]</th>
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<td>Simple Scalar Control</td>
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<td>Speed Range</td>
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<td>Static Speed Accuracy</td>
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<td>Torque Rise Time</td>
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<td>Possible Applications</td>
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</table>

As it can be seen from TABLE 2.4, only control strategies that can be implemented on converters are presented. These control strategies can be separated in two classes, scalar control and vector control. Both scalar and vector control strategies are implemented in the current project to test the theoretical concept on a real system and to get a better knowledge of how the methods behave. To do so, first, the state of the art of each control strategy is presented in the following of this chapter. After the state of the art, the control methods selected for this project are presented in more detail in the following chapter, along with the implementation method.

2.5.1 Scalar Control

Being initially developed for the induction machine, this motor drive control strategy is used in systems which do not require high dynamic performances because of its simplicity and low cost [11, 12].
As a speed control strategy it takes into consideration two of the properties specific for the induction machine [12]:

- The torque-speed characteristic is predominantly steep in the region of synchronous speed, which means that the electrical rotor speed is close to the electrical frequency. By controlling the frequency, the speed of the machine can be controlled;
- The voltage equation (2.25), expressed in steady state, highlights the fact that the flux linkage term has a much higher influence than the resistive term in the voltage equation for medium to high speed situation.

\[
\bar{v}_s = R_s \bar{i}_s + j\omega_r \bar{\lambda}_s
\]

\[
\Lambda_s = \frac{V_s}{\omega_r} = \frac{V_s}{2\pi f}
\]

, where: \(\Lambda_s\) - magnitude of the stator flux linkage;
\(V_s\) - magnitude of the applied voltage;

As it can be seen in equation (2.26), the magnitude of the flux linkage is in fact the ratio between the magnitude of the applied voltage, and rotor electrical speed. This helps us understand that in order to maintain a constant flux linkage, to avoid saturation, the ratio should be kept constant [12]. This ratio also gives the name of this method, being widely known as V/f control.

The phasor diagrams of the PMSM presented in Fig. 2.6 are used to better understand the main disadvantage of this control strategy. By only controlling the voltage and the frequency, and not the current on the direct and quadrature axis, the magnetisation of the machine cannot be control properly [12, 13].

![Phasor diagram of PMSM](image)
As stated in [12, 13], high values of V/f cause an increase in the direct axis component of the current $i_d$, which produces an over-excitation in the machine Fig. 2.6 a). On the other hand, for low V/f values the direct axis component of the current $i_d$, becomes negative and the machine experiences under-excitation Fig. 2.6 b).

Using this method, problems are experienced at low speeds, where the frequency has a small value and the resistive term cannot be neglected. To handle this problem, various compensation methods have been proposed, as it can be found in [12, 14-17].

When this control method is applied to PMSM, stability problems will appear because of desynchronization between the rotor speed and the applied frequency [14-18]. This desynchronization between the two frequencies will make the operation impossible.

The classical solution which can be implemented during the manufacturing process is to provide the rotor with damper windings [18]. These damper windings will ensure the synchronization between the two frequencies. However, this solution increases the cost significantly and it is proven to be problematic when it comes to the design of surface mounted PMSM [18].

Different other solutions have been proposed in the literature to deal with this problem by employing a close loop control, such as in [15-17] where the perturbation of the current in the DC link was used to modulate the frequency. The power efficiency was the main objective presented in all three references, with similar approach in [15] and [16], where the voltage was controlled using a search algorithm which ensures a minimum input power to the PMSM. In [17] the objective was to control the voltage in order to obtain unity power factor.

In [14] a voltage control method is used to improve the low speed performance, along with a small signal model which modulates the applied frequency proportional to the input power perturbation.

The cited methods conclude that a better stability is achieved, without the need of damper windings in the rotor, although in [15-17] poor performance was obtained for low speed operation.

A different scalar control method, called I-f control, is presented in [19], for start up without the need of initial rotor position estimation and ultra low speed sensorless control. This method also ensures over-current protection by controlling separately the $i_d$ and $i_q$ currents. The disadvantage presented by this method is the absence of an analytical method to design the I-f controller.

### 2.5.2 Vector Control

By comparison with the scalar control, vector control allows separate close loop control of both flux and torque [13], by separately controlling the direct and quadrature axis currents $i_d$ and $i_q$. These two currents are controlled through the voltage $v_d$ and $v_q$, according to the following equations, derived from (2.18) and (2.19).
Vector control can ensure optimum control of the machine under different working conditions, such as: maximum torque per ampere ratio (MTPA), maximum torque per flux ratio, unity power factor.

In the current project the MTPA strategy is implemented. Using this strategy, the control ensures minimum current is used to achieve the required torque, which maximizes the machine efficiency [20]. To achieve MTPA ratio the torque angle $\theta_T$, between the PM flux linkage phasor and the current phasor, has to be maintained at 90° (Fig. 2.8). By doing this the direct axis current $i_d$, which does not contribute to the production of torque (2.23) is cancelled, and the quadrature axis current $i_q$ becomes equal with the current magnitude ($i_q = \hat{l}_s$).

This situation can be observed in the phasor diagram Fig. 2.7. Here it can be seen that the stator flux linkage is produced by the permanent magnet flux and the flux on the q axis.

\[
\frac{di_d}{dt} = -\frac{R_s}{L_d}i_d + \frac{L_q}{L_d} \omega_r i_q + \frac{1}{L_d} v_d \tag{2.27}
\]

\[
\frac{di_q}{dt} = -\frac{R_s}{L_q}i_q - \frac{L_d}{L_q} \omega_r i_d - \frac{\omega_r}{L_q} \lambda_{pm} - \frac{1}{L_q} v_q \tag{2.28}
\]

Fig. 2.7. Phasor diagram of vector controlled PMSM for MTPA [13].

To obtain this behaviour a technique best known as field oriented control (FOC) is used. This technique employs cascaded close loop systems to control the speed and torque, by means of speed controller and current controller. A more in depth description of FOC will be made in the following chapters.
Control Description and Implementation

This chapter presents the control strategies that are selected for this project. After the selected scalar and vector control is presented, the implementation method is made. Because scalar and vector control use relatively the same structure, the common components are presented in the vector control part. The last part of the chapter presents the rotor position estimator.

3.1 Scalar Control (I-f Control)

Although V/f control is the most popular scalar control method, it was not selected for this project because of its disadvantages related to PMSM, presented in the previous chapter. Instead, I-f control was preferred because of its advantages, as [19]:

- ability to protect the system by directly controlling the current;
- similar structure and components as FOC;
- the variation in machine parameters has a limited influence over the control;
- capability to start at full load independent of the rotor position;
- in wind turbine applications it is recommended for maintenance situations, when the rotor has to be moved only slightly;

To observe the similarities with FOC, which is presented in more detail in the following subchapter, a block diagram of the scalar control is presented in Fig. 3.3.

The main difference is that a current reference is given directly to the “q” axis, eliminating the speed control loop. The “d” axis is kept at zero for the same reason as for FOC, to ensure better efficiency for the machine.

If the quadrature axis current is maintained constant during the entire operating procedure, the active power will decrease when the speed reaches nominal value, providing only the necessary power to drive the machine. The rest of the electric power sent to the machine will be transformed to reactive power, which reduces the efficiency and demagnetizes the permanent magnets (Fig. 3.1).

Fig. 3.1. Active and reactive power variation during the starting procedure ($i_q$ = constant).
To ensure the best efficiency possible using scalar control, the reference quadrature axis current $i_{q}^{*}$ has to be controlled as a function of reference frequency $f^{*}$.

If the reference quadrature axis current $i_{q}^{*}$ is decreased, after the nominal speed is achieved, the active power is maintained at the same level, while the magnitude of the reactive power is reduced (Fig. 3.2). It has to be noted here that because the imposed rotor position is not equal with the real rotor position, unity power factor cannot be achieved. The quadrature axis current $i_{q}^{*}$ has to be maintained at an adequate value, to ensure stable operation.

An important disadvantage, that makes this control unusable for a wind turbine application, must be stated here. Because there is no outer speed loop to provide at any moment the adequate reference quadrature axis current $i_{q}^{*}$, this control cannot be used in all situations required by the system. For example, when the transition from motor to generator is made, the sign of the current reference has to be modified manually by the user, at the same time, or else the control becomes unstable. Also, if a considerable load torque is applied, the current is not able to produce sufficient electromagnetic torque, causing the drive to lose stability.

Fig. 3.2. Active and reactive power variation during the starting procedure ($i_{q}^{*}(f^{*})$).

Fig. 3.3. Block diagram of closed loop I-f scalar control [19].
Because of these factors, this control cannot be applied to drive a wind turbine. However, this control is recommended for maintenance situations, when the turbine has to be moved only for short periods of time, at a small speed [19].

This control does not use any position or speed information from an encoder or estimator; instead the position is derived from the frequency command given to the machine. By imposing the position, the reference frequency controls the speed of the machine.

As for FOC two proportional integrators (PI) controllers are used to control the current. Because these two PI controllers have the same structure as for FOC, the implementation method is presented in the following subchapter, where FOC is explained.

The “dq” voltage obtained after the PI controllers, which is considered in this case to be the reference voltage, is transferred to “abc” reference frame in order to create the command for the switches.

As for vector control, the measured current of the machine is used as a feedback, making it a closed loop control.

### 3.2 Vector Control (Field Oriented Control)

As stated in the previous chapter the vector control method selected for this project is sensorless field oriented control, working in a MTPA strategy. The implemented block diagram of the control is presented in the following:

![Block diagram of the sensorless FOC.](image)

To ensure safe operation inside the speed range and above it, three types of controllers will be implemented: flux controller, which has as input the flux on the “d” axis and produces as output
the reference current on the “d” axis, speed controller, which has as input the speed error and produces at the output the reference current on the “q” axis, and current controller, which has as input the current error and produces at the output the reference voltage.

The reference current generator block, where the PI controllers for speed and flux are implemented, is presented in more detail in the following figure.

Using field weakening the speed of the machine is increased above nominal speed by decreasing the flux and controlling the torque limits [21].

On the “d” axis the current reference is given as a function of the speed magnitude. This behaviour is summarising in the following:

$$\omega_r \leq \omega_{rN} \implies \lambda_d^* = \lambda_{PM} \implies i_d^* = 0$$ \hspace{1cm} (3.1)

$$\omega_r > \omega_{rN} \implies \lambda_d^* = \frac{\omega_{rN}}{\omega_r} \lambda_{PM} \implies i_d^* = \frac{\lambda_d^* - \lambda_{PM}}{L_d} < 0$$ \hspace{1cm} (3.2)

The direct current has to be reduced ($i_d < 0$) in order to reduce the back-EMF component along the q axis (2.19). Because the direct axis current ($i_d$) affects the magnetisation it should be limited to a minimum value, at which $\lambda_d^* = 0$.

$$i_{d,min}^* = -\frac{\lambda_{PM}}{L_d} < 0$$ \hspace{1cm} (3.3)

During field weakening control the magnitude of the direct axis current increases ($|i_d| > 0$). This increase has to be taken into consideration in order to limit the current.

When $i_d^*$ current is modified, the maximum $i_{d,\text{max}}^*$ current is calculated, in order to limit the torque, using the following equation.
\[ i_{q,max}^* = \sqrt{I_{max}^2 - i_{d}^2} \] (3.4)

where: \( I_{max} \) - peak value of the maximum allowed current;

Using this approach the control ensures that the machine always runs inside the safety limits.

With the reference currents determined, the error can be calculated. This error is fed to the PI current controllers to provide the voltage command. The decoupling terms, presented in (3.5) and (3.6) are added to the voltage signal, to ensure the decoupling present in the machine equations (2.18) and (2.19).

\[ V_{d,decoup} = -\omega_r L_q i_q \] (3.5)

\[ V_{q,decoup} = \omega_r (L_{PM} + L_d i_d) \] (3.6)

With the decoupling done, the reference “dq” voltage is transferred to “abc” reference frame, using [4], before the switch modulation is generated.

Because the position and speed estimator represents an important part of the control, it is presented as a separate subchapter, after all FOC components are depicted.

The implementation methods for the current, flux and speed PI controllers are made in the following, starting with the design requirements.

It has to be noted here that in certain situations, the variables will be replaced with their numerical values. These numerical values are presented in Appendix C.

### 3.2.1 Controller Design Requirements

In the process of designing the current, flux and speed controllers the following design requirements have been taken into consideration:

- Steady state error less than 1%;
- Overshoot less than 5%;
- Rise time for the current controller less than 40 sampling periods \( (40 \cdot T_s = 10 [ms]) \);
- Rise time for the speed controller less than 400 sampling periods \( (400 \cdot T_s = 100 [ms]) \);
- Bandwidth of the speed controller has to be at least 10 times slower than the bandwidth of the current controller;

With the requirements imposed for all controllers, the implementation process is presented separately in the following.

### 3.2.2 Current Controller

To design the current controllers the machine equations (2.18) and (2.19) must be used to create the plant of the system \( (G_p(s)) \). The plant constitutes a first order transfer function (3.10), which has the voltage as input, and the current as output.
The hardware configuration of the current control is given in Fig. 3.6 a), where the digital controller (PI controller) is implemented, along with the digital to analogue converter (PWM) and the analogue to digital converter (sampler and data hold).

The block diagram, in part b), presents all the signals and transfer functions existent in the current loop. The transfer functions are:

**PI controller:**

\[ C(z) = k_{pl} + \frac{k_{il}T_s z}{z - 1} \]  

, where:  
- \( k_{pl} \) - current proportional gain;  
- \( k_{il} \) – current integral gain;  
- \( T_s \) - sampling time [s];  
- \( z \) - discrete time variable;  

**D/A converter**, represents the PWM modulation. To represent the delay introduces by the PWM process, a unity time delay is used.
A/D converter, represents the zero order hold block. This is always required after the ideal sampler [22]. The transfer function of the zero order hold is [22]:

\[
H(s) = \frac{1 - e^{-sT_s}}{s}
\]  

(3.9)

**Plant**, represented by the electrical equations (2.18) and (2.19) of the machine, after the decoupling terms have been eliminated. The remaining components, inductance and resistance, form a first order transfer function.

\[
G_p(s) = \frac{1}{L_q \cdot s + R_s}
\]  

(3.10)

A simplification in the system is made by combining the zero order hold block \(H(s)\), with the plant \(G_p(s)\), to create only one transfer function.

\[
G(s) = H(s) \cdot G_p(s) = \frac{1 - e^{-sT_s}}{s} \cdot \frac{1}{L_q \cdot s + R_s} = \frac{1 - e^{-sT_s}}{s \cdot (L_q \cdot s + R_s)}
\]  

(3.11)

To determine the system expression, a flow graph (Fig. 3.6 part c)) of the system has to be created. The flow graph is created to represent the sampler influence, using dashed line. The sampler imposes a problem in the system because it does not have a transfer function [22].

Once the flow graph is created, the signals are attributed to the correct position. A note has to be made here regarding the starred variables \(E^*, V_{dq}^*, S_{dq}^*\) and transfer functions. \((C^*(s), D^*(s))\). These starred variables and transfer functions appear in the system because of the ideal sampler and have a direct link to the \(z\) domain [22].

\[
E^*(s) = E(z)\big|_{z=e^{sT}}
\]  

(3.12)

To determine the system output, it has to be expressed like the sampler input, in terms of the system input and sampler output [22].

\[
E(s) = I_{dq\,ref}(s) - G(s) \cdot D^*(s) \cdot C^*(s) \cdot E^*(s)
\]  

(3.13)

\[
I_{dq}(s) = G(s) \cdot D^*(s) \cdot C^*(s) \cdot E^*(s)
\]  

(3.14)

Starring (3.13), and solving for \(E^*(s)\) yields:

\[
E^*(s) = \frac{I_{dq\,ref}^*(s)}{1 + G^*(s) \cdot D^*(s) \cdot C^*(s)}
\]  

(3.15)

Transferring (3.14) in the \(z\) domain and replacing \(E(z)\) using (3.15) yields:

\[
I_{dq}(z) = \frac{G(z) \cdot D(z) \cdot C(z)}{1 + G(z) \cdot D(z) \cdot C(z)} I_{dq\,ref}(z)
\]  

(3.16)
Chapter 3. Control Description and Implementation

Equation (3.16) represents the closed loop transfer function of the current controller. To determine the PI parameters, all transfer functions have to be replaced in (3.16). Because the plant transfer function (3.11) is in the \( s \) domain, it has to be transferred to the \( z \) domain first.

\[
G(s) = A(s) \cdot B^*(s) = \frac{1}{s \cdot (L_q \cdot s + R_s)} \cdot (1 - e^{-sT_s})
\]  
(3.17)

The transfer function \( G(s) \) is separated in two transfer functions, continuous transfer function \( A(s) \) and starred transfer function \( B^*(s) \), to simplify the procedure. These two transfer functions are then transferred to \( z \) domain separately.

\[
A(s) = \frac{1}{s \cdot (L_q \cdot s + R_s)} = \frac{1}{R_s} \cdot \frac{\frac{R_s}{L_q}}{s \cdot \left(s + \frac{R_s}{L_q}\right)}
\]  
(3.18)

By defining \( \tau = \frac{R_s}{L_q} \), and using the \( z \) transform tables,

\[
A(z) = \frac{1}{R_s} \cdot Z \left[ \frac{\tau}{s \cdot (s + \tau)} \right] = \frac{1}{R_s} \cdot \frac{z(1 - e^{-\tau T_s})}{(z - 1)(z - e^{-\tau T_s})}
\]  
(3.19)

The starred transfer function is transferred to the \( z \) domain using (3.12).

\[
B(z) = B^*(s)|_{e^{sT_s} = z} = 1 - z^{-1} = \frac{z - 1}{z}
\]  
(3.20)

Replacing (3.19) and (3.20) in (3.17) yields:

\[
G(z) = A(z) \cdot B(z) = \frac{1}{R_s} \cdot \frac{z(1 - e^{-\tau T_s})}{(z - 1)(z - e^{-\tau T_s})} \cdot \frac{z - 1}{z} = \frac{1}{R_s} \cdot \frac{1 - e^{-\tau T_s}}{z - e^{-\tau T_s}} = \frac{0.0159}{z - 0.9887}
\]  
(3.21)

A bode diagram is plotted in Fig. 3.7 to present the difference between the continuous plant transfer function (3.10), and the discrete transfer function (3.21). From the response it can be seen that the influence of the zero order hold block (3.9) is very limited.

![Bode Diagram](image)

Fig. 3.7. Bode diagram of continuous transfer function (3.10) and discrete transfer function (3.21)
Replacing (3.7), (3.8) and (3.21) in (3.16), yields:

\[
H_{cl}(z) = \frac{I_{dq}(z)}{I_{dq,ref}(z)} = \frac{0.0159 \cdot (k_{pi} + k_{ii}T_s)z - 0.0159 \cdot k_{pi}}{z^3 - 1.9887 \cdot z^2 + \left[0.0159 \cdot (k_{pi} + k_{ii}T_s) + 0.9887\right]z - 0.0159 \cdot k_{pi}}
\]  

(3.22)

Using all transfer functions obtained, and the design requirements imposed at the beginning, the PI parameters are determined using Matlab’s application, Control System Tuning.

The determined PI controller is:

\[
C(z) = k_{pi} + \frac{k_{ii}T_s z}{z - 1} = 4.03 + \frac{158 \cdot T_s z}{z - 1} = \frac{4.04 \cdot z - 3.99}{z - 1}
\]  

(3.23)

From

Fig. 3.8 it can be seen that for the selected PI parameters, the steady state error is below 1%, no overshoot appears, the rise time is 8.2 [ms] and the settling time is 18.4 [ms]. All these parameters correspond to the requirements imposed for the controller.

![Step Response](image)

**Fig. 3.8.** Step response of the current closed loop transfer function (3.22).

From Fig. 3.9 it can be seen that the system is stable because all the poles are situated inside the unity circle. Furthermore, a gain margin of 23.9 [dB] and a phase margin of 85.8 [deg] can be observed in the open loop Bode plot, which ensures the loop to be stable.

From the last plot, where the closed loop Bode diagram is presented, the bandwidth of the controller can be obtained. For the current control loop the bandwidth is 277 [rad/sec].
3.2.3 Flux control loop

Because the flux control loop is part of the electrical system, like the current control loop, it has to have similar response time and bandwidth. In order to simplify the control, the same PI parameters are adopted for the flux control loop, as for the current control loop.

This simplification is made, because field weakening was not considered to be an objective for the project, thus a lower importance is given to this procedure.

3.2.4 Speed Controller

The speed controller applied in FOC has to provide the reference $i_q^*$ current to the current controller. Because the output of the speed controller is the torque, it has to be converted to current by a coefficient $k_t$, which is determined using (2.24).

$$k_t = \frac{i_q}{T_e} = \frac{2}{3 \cdot p \cdot \lambda_{pm}}$$ (3.24)
As for the current controller, the machine equation is required to develop the control. In this case the mechanical equation is used (2.24), in which the speed is a function of the torque.

To better understand the structure of the system a block diagram is presented in Fig. 3.10. Here it can be observed that the current control loop is situated inside the speed control loop.

![Block diagram of the speed control loop.](image)

The transfer functions are:

**PI controller:**

\[
C_w(z) = k_{pw} + \frac{k_{iw}T_z z}{z - 1}
\]  
(3.25)

, where: \(k_{pw}\) - speed proportional gain;

\(k_{iw}\) - speed integral gain;

**Current loop**, represents the close loop transfer function of the current, determined earlier after the PI was selected. The transfer function is presented in (3.22).

**Plant**, represented by the mechanical equation (2.24) of the machine;

\[
W(s) = \frac{1}{f \cdot s + B}
\]

Because the plant is in \(s\) domain, it has to be transferred to \(z\) domain before the closed loop transfer function is determined. To diversify the procedure, Matlab is used this time to obtain the discreet time transfer function.

\[
W(z) = \frac{0.002629}{z - 1}
\]

(3.27)

As for the current control loop, Matlab’s Control System Tuning application was used to determine the PI coefficients.

\[
C_w(z) = k_{pw} + \frac{k_{iw}T_z z}{z - 1} = 2.1 + \frac{0.844 \cdot T_z z}{z - 1} = \frac{2.1 \cdot z - 2.1}{z - 1}
\]

(3.28)

From Fig. 3.11 it can be seen that for the selected PI parameters, the steady state error below 1%, the overshoot is 2.1 [%], the rise time is 86.7 [ms] and the settling time is 144 [ms]. All these parameters correspond to the requirements imposed for the controller.

From Fig. 3.12 it can be seen that the system is stable because all the poles are situated inside the unity circle. Furthermore, a gain margin of 39.2[dB] and a phase margin of 83.6 [deg] can be observed in the open loop Bode plot, which ensures the loop to be stable.
Fig. 3.11. Speed control step response (continuous).

The last plot presents the bandwidth of the controller, which is 24.27 [rad/s]. The ratio between the bandwidths of the two controllers is $277/24.27 = 11.27$. Because the ratio between the two controllers is greater than 10, the last requirement is fulfilled.

Fig. 3.12. Plots of the speed control system: a) Root locus, b) Open loop Bode and c) Closed loop Bode.
The last components of the control that have to be implemented are the limitations. These limitations maintain the output of the PI controller in a safety region. However, when the output of the PI exits the safety limit, a phenomenon called integrator windup appears [23]. Because this phenomenon can affect the performance of the control, it is analysed in the following.

### 3.2.5 Anti-Windup

The windup phenomenon appears mainly when a large error is sent to the PI, error which determines the output to vary outside the safety limit. Because the output is limited, the input error cannot be reduced as fast as the controller requires. This behaviour, determines the integrator term to increases significantly in order to correct the input error, phenomenon also called windup [23]. The windup effect has to be eliminated from the system because it produces a large overshoot and a high settling time [23].

In order to deal with this problem a tracking anti-windup solution is used, Fig. 3.13 [23, 24].

![Fig. 3.13. PI controller with anti-windup.](image)

This solution is explained starting with the classical PI controller, without anti-windup, which is created using the following equations:

\[
\frac{dI(t)}{dt} = e(t) \tag{3.29}
\]

\[
y(t) = k_p e(t) + k_i I(t) \tag{3.30}
\]

\[
y_{lim}(t) = [y(t)]_{\text{max}}_{\text{min}} \tag{3.31}
\]

To avoid integrator windup the input error \( e(t) \) has to be reduced for the integrator sum \( I(t) \), when the system enters saturation mode. The new input error \( e_{lim}(t) \) has to ensure that the output is identical with limited output \( y(t) = y_{lim}(t) \) [24].

\[
y_{lim}(t) = k_p e_{lim}(t) + k_i I(t) \tag{3.32}
\]

From (3.30) and (3.32) the new error can be determined.
Using the new error to determine the integrator sum, the new controller equations can be written.

\[
\frac{dI(t)}{dt} = e_{lim}(t) \tag{3.34}
\]

\[
y(t) = k_p e(t) + k_i I(t) \tag{3.35}
\]

\[
y_{lim}(t) = \left[y(t)\right]_{\text{max}}^{\text{min}} \tag{3.36}
\]

From (3.38) it can be observed that the new error is used only to calculate the integrator sum, the proportional part of the control uses the original error \(e(t)\).

Once the PI controllers are implemented with anti-windup, the only remaining problem is to determine the rotor position. Because a sensorless method was selected to determine the rotor position, this method will be presented in the following.

### 3.3 Rotor Position Estimation

The method used to determine the rotor position and speed is generally known as the back-EMF method \([11, 25, 26]\). In order to estimate the position, the mathematical model of the machine, in \(dq\) reference frame is used (2.18) and (2.19).

The two equations can be written in vectorial form as:

\[
\vec{v}_{dq} = R\vec{i}_{dq} + \frac{d\vec{\lambda}_{dq}}{dt} + j\omega_r \vec{\lambda}_{dq} \tag{3.37}
\]

\[
\vec{\lambda}_{dq} = L_d i_d + \lambda_{mpm} + j L_q i_q \tag{3.38}
\]

The method requires that the equations should be transferred to \(\alpha\beta\) reference frame:

\[
\vec{v}_{\alpha\beta} = R\vec{i}_{\alpha\beta} + \frac{d\vec{\lambda}_{\alpha\beta}}{dt} \tag{3.39}
\]

\[
\vec{\lambda}_{\alpha\beta} = (L_d i_d + \lambda_{mpm} + j L_q i_q)e^{j\theta_r} \tag{3.40}
\]

Since the position term \((\theta_r)\) appears only in the flux linkage equation (3.40), this will be the equation from where the position will be computed. An important transformation must be made in order to extract the position.

\[
\vec{\lambda}_{\alpha\beta} = (L_d i_d + \lambda_{mpm} - L_q i_d + L_q i_q)e^{j\theta_r} \tag{3.41}
\]

In order to better understand the meaning of each term in the equation it is written in the following form:

\[
\vec{\lambda}_{\alpha\beta} = L_q \vec{i}_{\alpha\beta} + [L_d - L_q] i_d + \lambda_{mpm} e^{j\theta_r} \tag{3.42}
\]
From (3.42) it can be seen that the direct current component $i_d$ affects only the amplitude, of the vector that contains the rotor position information. Knowing this, the rotor position (angle), can be expressed.

$$\angle[(L_d - L_q)i_d + \lambda_{mpm}]e^{j\theta_r} = \angle e^{j\theta_r} = \angle(\lambda_{a\beta} - L_q\bar{\lambda}_{a\beta})$$  \hspace{1cm} (3.43)

The estimated rotor position can be obtained using the following equation:

$$\hat{\theta}_r = \tan^{-1}\frac{\lambda_\beta - L_q i_\beta}{\lambda_\alpha - L_q i_\alpha}, \quad \begin{align*}
\lambda_\alpha &= \int (v_\alpha - R i_\alpha)dt \\
\lambda_\beta &= \int (v_\beta - R i_\beta)dt
\end{align*}$$  \hspace{1cm} (3.44)

Some problems must be considered when using this method, as: integration requires an initial value and a small drift in current value will cause increasing error after integration [21]. Because these influences can affect the computation, rendering the method unviable, an adaptive correction has to be implemented.

The correction method that was selected to be implemented in this project uses two elements: a drift compensation loop and a phase lock loop (PLL) [21, 26]. In the following, both methods will be explained along with the implementation method.

### Drift Compensation Loop

This subsystem is implemented to eliminate the error before integration, by comparing two flux values in stationary reference frame ($a\beta$). The first $a\beta$ flux value is obtained using (3.44). The second flux value is determined in $dq$ reference frame, using (2.20) and (2.21), result which is transferred to $a\beta$ reference frame.

The difference between the two fluxes represents the error sent to the PI controller. As output, the PI controller produces a voltage component $V_{comp}$, which is used to eliminate the drift.
The PLL implemented in the system is placed after the back-EMF method. It is used to eliminate the error in the estimated position, by taking as an input the estimated position \((3.44)\) and comparing it to the output of the PLL, which will represent the actual estimated rotor position.

The main disadvantage of the back-EMF method comes from its name. The method is unable to provide the correct information at very low speeds. This is because the back-EMF term contains the speed variable. When the speed is close to zero, the back-EMF term is very small, and the estimated position is not precisely estimated.

Because of this problem, during the start up procedure, the rotor will produce an initial vibration, until the alignment is achieved, followed by a smooth transition, until the reference speed is reached. This problem was observed in simulations and in laboratory experiments.
4 Simulations

The model created, along with the control, is tested during a series of simulations to observe the performance. The simulation conditions are selected considering the objectives imposed in the first chapter. This chapter will present the result of each simulation, along with necessary explanation. All simulation are made using Matlab Simulink. To get familiarized with the Matlab Simulink model, an overview is presented at the beginning.

4.1 Model Overview

As it could be seen in Fig. 4.1 the model consists out of three main blocks: permanent magnet synchronous machine, field oriented control, and speed and position estimator.

Besides the main blocks, three selectors are employed to allow the user a fast change between different load types and different working conditions.

A more complex model, containing more components, like the three level NPC converter, AC voltage source, diode bridge rectifier and SPWM, was also created. Because both models provide similar results, the simplified model is used for the report.

Using this model, a series of simulations are made. These simulations are developed to test the control for all the requirements imposed in the objectives.
4.2 Scalar Control Simulations

According to the description provided in previous chapters, scalar control is unable to operate in all situations required by the objectives. Because of this factor, and because the dynamic performance is reduced, compared to vector control, this is considered to be an alternative control strategy, not the main control. Only two simulations are made using scalar control, to verify how the control reacts during speed variation and during load torque disturbance.

4.2.1 Speed reference variation

The first simulation is made to test how the control behaves when the reference speed is modified. From Fig. 4.2, it can be seen that during the starting procedure small oscillations in speed appear. These oscillations appear because the position imposed from the reference frequency is not aligned with the rotor position.

As it could be seen from Fig. 4.2 and Fig. 4.3, the current is sinusoidal with a constant magnitude during the entire simulation time. Small changes in current magnitude appear only during the transient regime.

For a better view of voltage and current in steady state, Fig. 4.3 presents a closer perspective. Here we can observe that the current and the voltage are sinusoidal, with a phase shift of approximately 90°.

The large phase shift, which determines a small power factor, appears because the simulation is done without adding a load to the system. Without a load, the active power required by the machine is very small. Because the control maintains the current at a high value, even during no
load situation, a significant amount of apparent power is provided at the terminals, power which becomes reactive power, as it was explained in Scalar Control (I-f Control).

This large phase shift, combined with the current magnitude, determines an inefficient operation.

Fig. 4.3. Voltage and current in steady state situation.

To increase the efficiency, a modified method is proposed in Scalar Control (I-f Control) subchapter. This method requires that the reference quadrature axis current \( (i_q^*) \) is modified as a function of frequency, according to Fig. 4.4.

Fig. 4.4. Reference quadrature axis current \( (i_q^*) \) as a function of frequency.

The maximum current is applied only at the beginning, to provide sufficient torque during the starting procedure. The reference quadrature axis current \( (i_q^*) \) is reduced to 50% of the maximum value \( (i_{q,\text{max}}^*) \), when the frequency reaches nominal value.

The result of the simulation, presented in Fig. 4.5, shows that speed and the torque characteristics are not affected by this modification.
An important difference can be observed in the current waveform. In this situation the current has smaller amplitude, when the system enters steady state. However, from the result it can be seen that the oscillations have increased.

![Graph showing speed, reference, torque, and current over time](image)

Fig. 4.5. Speed reference variation using scalar control (modified version).

To analyze the phenomenon, several simulations are done at different reference currents. From the results it was observed that the oscillations increase as the current is decreased. The reference current has to be maintained above a minimum value, to ensure system stability.

The disadvantage is that the minimum current value cannot be determined analytically because it is affected by numerous other parameters as, load torque, reference speed variation and PI parameters.

### 4.2.2 Load torque variation

The second simulation is made to determine how the control behaves when an external mechanical load is applied.

From Fig. 4.6, it can be seen that the control is able to maintain the speed within ±2.4% of the nominal speed.

This fast response is due to the fact that the electromagnetic torque has a fast response time, to counteract the load torque applied at the shaft.

From both the current and electromagnetic torque waveform, it can be seen that oscillations appear in the system before it enters steady state. These oscillations are caused by the fast response of the PI controllers.

As for the previous situation, the current and voltage variation is sinusoidal.
From the simulation, an increase in power factor is observed, when the load torque is applied. This is due to the fact that a higher amount of apparent power, supplied at the machine terminals, is used as active power.

4.3 Vector Control Simulations

Because this control is considered to be the primary control strategy for the drive, it will be tested in five different situations, according to the objectives.

The first two tests are made in similar conditions as the test made for scalar control. The difference is that for vector control, the reference speed is given using the step command, not the ramp command.

4.3.1 Speed reference variation

As for the previous case, the main objective of this simulation is to observe how the control behaves when the reference speed is modified.

Because the control is implemented using speed and position estimator, the performance of the estimator is also of main interest.

From Fig. 4.7, it can be seen that the control is able to provide a fast response, when the reference speed is modified.
Compared to scalar control, a higher efficiency is achieved, because the current reference is provided by the outer speed loop.

From Fig. 4.8, it can be seen that the speed and position estimator is able to produce an accurate estimation, in less than a second. The fast response of the estimator enables the control to start the machine without the use of an encoder.
4.3.2 Load torque variation

In the second simulation, the capability of the control to react in case of a load torque disturbance is tested. From the results presented in Fig. 4.9, it can be seen that the control manages to withstand the torque step. The speed of the machine decreases with approximately 18% of the nominal speed, when the load torque is applied. The maximum speed achieved, when the load torque is removed, is 12.5% the nominal speed.

![Fig. 4.9. Result of load torque variation using vector control.](image)

From the current waveform it can be seen that compared to scalar control, no oscillations appear. The current is maintained inside the safety boundaries during the entire period.

4.3.3 Transition from motor to generator

As stated in the Converter and Control for DeepWind Programme subchapter, the Darreius wind turbine is unable to start without the help of the machine. Because of this factor, the machine has to be controlled in motor mode, until the required speed is achieved. Once the turbine is able to capture the wind power, the control must ensure a safe transition from motor to generator.

In order to test the transition from motor to generator and back, a load torque is applied at the shaft, having the same direction as the speed (Fig. 4.10).

From Fig. 4.11, it can be seen that the simulation result is very similar with the previous case. When the load torque, having the same direction as the speed, is applied, the speed of the drive increases too approximately 19% of the nominal speed. To maintain stability, the control counteracts the load torque by changing the direction of the electromagnetic torque.
Once the direction of the electromagnetic torque is opposite to the speed direction the machine enters generator mode. This operation mode continues until the load torque is removed.

![Diagram](image-url)

**Fig. 4.10.** Speed and torque direction for motor and generator mode.

As it can be seen from the current waveform, the amplitude is maintained constant, inside the safety boundaries, during the entire procedure.

![Graphs](image-url)

**Fig. 4.11.** Result of transition from motor to generator and back.

### 4.3.4 Emergency breaking

As it was explained in the Converter and Control for DeepWind Programme subchapter, mechanical breaks cannot be fitted to the turbine. The control must be capable to stop the turbine in case of an emergency, as high wind or high waves.

To emulate such a situation, the load torque was maintained constant during the breaking procedure, while the speed was brought down to zero in two seconds.

The speed was decreased using a ramp variation because of the following reasons:
- In case of a large structure, as the wind turbine is presumed to be, the transition from nominal to zero speed has to be smooth;
- To observe how the control behaves when the reference is given as a ramp command.

From the result presented in Fig. 4.12, it can be seen that between the reference and the actual speed there is a constant steady state error. This error is removed after the reference speed reaches zero.

![Fig. 4.12. Result of emergency breaking.](image)

When the speed reaches zero, the estimator cannot provide the correct position and speed information, as it can be seen in Fig. 4.13. Because the simulation uses a simplified model, the speed of the machine is maintained constant at zero, while a load torque is applied, even though the estimated position is not similar with the actual position.

In a practical experiment, there are many other parameters that influence the control, which have to be considered, in order to ensure stability. The discussion regarding stability at very low speeds, in a practical system, is presented in Laboratory Experiments.

After the speed has reached zero and the load torque is removed, the control has to reduce the electromagnetic torque, in order for the speed to remain constant at zero.
4.3.5 Holding the machine at zero speed

The last test required by the objectives is to maintain the speed of the machine at zero, while a load torque is applied.

Because the speed and position estimator cannot provide information about the position when the speed is zero, the control has difficulties to maintain the speed in a small interval, when a load torque is applied.

The control can react to torque disturbance, only after the estimator provides the proper position. Until the position is determine, the speed of the machine can increase to a high value.

From the simulation result (Fig. 4.14), it can be seen that the speed reaches a maximum value of 30% of the nominal speed.

After approximately half a second, the position estimator is able to determine the actual position (Fig. 4.15), causing the control to ensure a smooth transition to zero speed.

When the load torque is removed, the control produces an oscillatory response, until the speed becomes zero.
As for the previous case, the simplified model cannot recreate very accurate the practical situation. To have a better understanding of how the real system behaves during this experiment, please refer to Laboratory Experiments.
Chapter 5. Hardware Design of Converter

5

Hardware Design of Converter

In this chapter the design and the main circuits of the three level NPC converter are presented. Because the design was not an objective for this project, only the main parts of the converter will be presented here, with sufficient explanation in order for the reader to understand the hardware used. For more information about the design and the components, please refer to [7].

5.1 General Structure

Based on [7] and Fig. 5.1 it can be seen that the design is made in such a way as to separate the hardware into two isolated regions: the power side and the control side.

Fig. 5.1. Simplified schematic of constructed converter [7].
To facilitate the communication between these two regions, gate drivers, current sensors, voltage sensors and temperature sensors are used, which ensure that the two regions are decoupled. Also, it should be mentioned that the converter is constructed on a four layer printed circuit board (PCB), with stacked DC link layout, ground and power planes, in order to reduce the interference between different circuits [7].

In the following of this chapter, the main circuits from these two regions are presented.

5.2 Power Side

Besides the power components (IGBT modules and capacitors), the power side of the converter is made out of a series of measurements circuits. These measurement circuits represent the main advantage of this design, because using the signal acquired, a series of protections are implemented, as it can be mentioned: three phase AC over-current protection, DC over-current protection, DC over-voltage protection, over-temperature protection and gate driver protection.

All these main circuits will be shortly presented in the following, in order to highlight the components used and their functionality:

b) **Capacitor bank**, made out of six 330 μF Panasonic capacitors, arranged in three parallel arms between the +HVDC and 0HVDC and three parallel arms between –HVDC and 0HVDC.

c) **Three IGBT modules**, each representing one leg of the three level NPC converter;

The IGBT modules are produced by Semikron (SK50MLI065), and have the following properties, according to the datasheet [27]: compact design, 600V/50A per IGBT, direct copper bounded aluminium oxide ceramic (heat transfer and isolation), snubber-less design, improved commutation paths, controlled axial lifetime technology for freewheeling diodes.

d) **Voltage dividers**, each constructed out of four high value resistors, used in the DC voltage measurement circuit to ensure a permanent connection to the DC link by reducing the current below the resistor current capability and to provide DC link voltage measurement;

e) **Three NJ28 high accuracy thermistors**, used in the over-temperature protection circuit to detect the temperature of the IGBT modules. The thermistors have a negative temperature coefficient (NTC), meaning that the resistance decreases, while the temperature increases. At 25°C the resistance is 100 [kΩ].

f) **Five Hall current sensors**, two for the DC side and three for the AC side, used to measure the high currents in the power region and output a reference voltage value which will be used in the control region for over-current protection and as measurement for the DSP;

The current sensors used in this design are Allegro ACS756 Hall Effect IC Sensors, which have the following properties [28]: total output error of 0.8%, very low power loss (130μΩ resistance),
3kV isolation, small magnetic hysteresis, measurement of ±50A, and 2.5V output for 0A with ±40mV/A characteristic.

For each measurement circuit, only the components situated in the power side have been presented here, while the rest of the circuits, which are situated in the control side, are presented in the following section.

### 5.3 Control Side

The control side of the converter is comprised of circuits which ensure the command, protection, signal acquisition and communication. Because all these circuits are explained in [7] only the main features of each circuit will be presented in the following, to help the reader understand the principle of operation.

1) **Gate Driver Circuit**

The gate driver Avago ACPL-332j was selected for this design to ensure the interface, protection and isolation between the power side and the control side.

The Avago ACPL-332j gate driver has the following features: optically isolated power stage capable of driving IGBTs up to 150A and 1200V, desaturation detection, isolated fault feedback, active Miller clamping, “soft” IGBT turn off, 2.5A output current, small package.

The PWM signal, sent from the command circuit to the gate driver, is applied to the anode and cathode of the LED situated inside the gate driver. The LED is used in the gate driver to ensure galvanic isolation between the power side and the command side.

To ensure desaturation protection, the collector-emitter voltage ($V_{ce}$) is monitored during the conduction. If this voltage rises above 6.5V the IGBT is turned off and a fault signal is generated. To avoid false triggering the desaturation detection is disabled when the IGBT is not conducting.

2) **Command Circuit**

The modulation PWM signals provided to the gate drivers are generated by the digital signal processor (DSP). In the current configuration, the DSP only provides the signals for the upper two switches, of each leg. These six PWM signals are transmitted to the complex programmable logic device (CPLD), as it can be seen in Fig. 5.2.

Using the six PWM signals, the CPLD will generate the complementary PWM signals for the lower two switches of each leg, while introducing the dead time between the complementary signals.

All twelve PWM signals, from the CPLD, are transferred to a pair of octal buffers (SN74LVC540A), six PWM signals for each octal buffer. The octal buffer used in this design acts as a NOT logic circuit. This is because the anode of the LED, situated inside the gate driver, is connected to a 3.3V DC source, and the cathode is connected at the output of the octal buffer.
In this configuration, when a signal is transmitted from the CPLD, 3.3V or logic 1, the octal buffer inverts the signal to 0V or logic 0. The 0V state is transferred to the cathode and a potential difference appears at the LED terminals, enabling the current to pass through the LED, which commands the IGBT to conduct.

In the opposite situation, when the CPLD gives the 0V, or logic 0 command, the octal buffer inverts the signal to 3.3V, or logic 1. In this situation, because the cathode has the same potential as the anode, the current will not flow through the LED, which commands the IGBT not to conduct.

The octal buffers presented in the circuit are also used as a safety feature. When a fault is detected in the converter the octal buffers are disabled and the command to the gate drivers is blocked.

The user has the possibility to control the command circuit through two external buttons. The first button (pwm E) is used to trigger the PWM modulation, while the second button (D) is used to disable the modulation and to reset the protections.

3) **Current Measurement Circuit**

As stated earlier, five Hall current sensors are used in the converter. Two sensors are used for the DC link current and three sensors are used for the AC phase current. The current measurement circuit is implemented only for the AC phase current sensors. The circuit is comprised of the following components:

- Hall current sensor, presented earlier, which gives a reference of 2.5[V] at 0[A], and has a ±40 [mV/A] characteristic.
- Voltage divider, is used to reduce the voltage level at 1.6667[V] for 0[A], with a characteristic of ±26.6667 [mV/A]. This is done because the input signal to the DSP has to be in the 0-3[V] range.
- ADC buffer, constructed from an operational amplifier which is configured as a voltage follower, to isolate the ADC input of the DSP from the signal source;
- Two pairs of dual series small signal Schottky diodes, one before the ADC buffer, and the other after the ADC buffer; used to limit the voltage signal in the 0-3[V] range;
- ADC input port of the DSP;

To have a better understanding of how these components are connected to form the current measurement circuit, a block diagram of the circuit is presented in Fig. 5.3.

4) Over-Current Protection

The over-current protection circuit is implemented for all five current sensors. By doing this, protection is ensured for the DC side and for the AC side of the converter.

The over-current protection circuit is comprised out of (Fig. 5.4):

- Hall current sensor, same as for the current measurement circuit;
- Window comparator; for each measured signal a window comparator is used, to compare the signal with two reference signals, maximum and minimum reference. These two references can be set by the user through variable resistors. When the measured signal is between the two boundaries the window comparator has a high output state, which signals correct operation.
- Logic AND circuit. The signals from the window comparators are entered a logic AND circuit, and the result is sent to the CPLD.
- CPLD, receives the signals from the AND circuit and takes the appropriate action.
5) **Voltage Measurement Circuit**

In order to protect and control the converter, a voltage measurement circuit, for the DC voltage, is implemented on the converter. The circuit is comprised of (Fig. 5.5):

- Voltage dividers; as mention earlier, four voltage dividers are used to acquire the voltage signal from the DC link.
- Differential amplifier; Two differential amplifiers are used to manipulate the signal received from the voltage dividers.
- Voltage dividers; at the output of each differential amplifier a new voltage divider is placed to reduce the voltage level which goes to the ADC buffer;
- Schottky diodes and ADC Buffer with the same structure as for the current measurement circuit.

![Fig. 5.5. Block diagram of the voltage measurement circuit.](image)

Using this signal and the current signals a closed loop control can be implemented on the convertor, in order to increase the dynamic performance of the drive.

6) **Over-Voltage Protection**

In order to ensure the DC over-voltage protection and to simplify the hardware structure the circuit is comprised of components similar with the voltage measurement circuit and over-current protection circuit:

- Voltage dividers, differential amplifier and voltage dividers (components presented in the voltage measurement circuit);
- Window comparator; for each measured signal a window comparator is used, to compare the signal with two reference signals, maximum and minimum reference. These two references can be set by the user through variable resistors. When the measured signal is between the two boundaries the window comparator has a high output state, which signals correct operation.
- Logic AND circuit. The signals from the window comparators are entered a logic AND circuit, and the result is sent to the CPLD. In this way the CPLD is announced if an over-voltage situation appears in the converter.
- CPLD, which receives the signal from the fail gate and takes the appropriate action.

The circuit structure, in block diagram form, is presented in Fig. 5.6.
7) **Over-Temperature Protection**

The over-temperature protection circuit is used as a safety feature for long time operation. If the module temperature increases over a specified limit, the circuit is disabled and the fault is signalled to the user. The circuit is made out of the following components:

- Signal conditioning circuit; the thermistors are connected in a resistive circuit in order to modify the NJ28 characteristics.
- Window comparators; In this case the window comparator works different. The output of the acquisition circuit is inverted for both comparators, so that the comparators output is high (healthy situation) if the temperature is below the preset limits.
- Two logic AND gates are used to deal with the temperature measurement circuit, because there are two preset limits of temperature.
- CPLD receives the signal from the fail gate and takes the appropriate action.

8) **Communication Circuit**

The converter has also implemented two communication circuits, CAN and RS-232/485, in order to facilitate the communication between the converter and an external program. Because this feature is not used in the current project it is not presented here. To get some knowledge about these two circuits please refer to [7].
Chapter 6. Laboratory Experiments

6 Laboratory Experiments

This chapter presents the practical work done in the laboratory. At the beginning, the laboratory setup used to do all the experiments is presented. The experimental results are separated in two parts, based on the type of control implemented. The first part presents the tests done using scalar control, while the second part presents the tests done using vector control. The tests done on the drive are selected to be similar with the simulations.

6.1 Laboratory Setup

The laboratory setup used to do all the tests is presented in Fig. 6.1. The components that comprise the setup are: voltage source (grid), autotransformer, three phase diode bridge rectifier, resistor, three level NPC converter, PMSM, load machine, converter for the load machine and voltage source for the converter (grid). Also, two personal computers (PC) are used to independently control the two converters.

In order to drive the PMSM, power is taken from the grid through an autotransformer and a three phase diode bridge rectifier. The autotransformer is used to adjust the DC link voltage at the output of the three phase diode bridge rectifier.

The configuration with autotransformer, diode bridge rectifier and resistor is used, instead of a simple DC voltage source, because the machine has to be controlled in generator mode. When the machine is working in generator mode, the three level NPC converter will behave as a rectifier, sending the AC power from the PMSM to the DC link. In this situation the power will be dissipated on the resistor, because the three phase diode bridge rectifier will block the power flowing to the grid.

A second synchronous machine is connected to the shaft of the PMSM, to act as a mechanical load. Torque control is implemented as a control strategy on the load machine.
A more in depth presentation of the laboratory setup is made in the videos written on the CD, which is attached to this report.

Because the DC link voltages are very similar for all the experiments, these results are presented in Appendix B, to avoid presenting very similar oscilloscope captures and repeating the same conclusion for each situation.

As stated in the chapter description, the following section will be divided in two parts. The first part presents the tests done using sensorless scalar control, while the second part presents the tests done using sensorless vector control.

### 6.2 Scalar Control Experiments

#### 6.2.1 Speed reference variation

The speed control capability is tested in the first experiment. Because the dynamic response of the control is slower, the speed reference is modified using a ramp variation.

At the beginning the machine is started from zero to nominal speed in two seconds. As it could be seen in Fig. 6.2, no initial vibration occurs in the rotor during the starting procedure.

It has to be noted here that after numerous test made in the laboratory, it was observed that for different initial rotor positions, rotor vibrations can occur during the start up. To examine this behaviour the starting procedure was repeated at different initial rotor positions. From the results, it was observed that the rotor vibration depends on the initial position, and the control is able start the machine independent of the rotor position.

![Fig. 6.2. Machine speed during speed reference variation (scalar control).](image)

The speed of the machine is maintained at the same level for another two seconds, before is reduced to 50% of the nominal speed, in two seconds. After another two seconds, the speed is increased to nominal speed. The last part of the control focuses on stopping the machine. The speed of the machine is brought down to zero with a ramp variation, in two seconds.
The waveform of the phase current, during the entire test procedure is presented in Fig. 6.3. From this figure it can be seen that variations in current magnitude appear only during the transition period. In steady state, the control is able to maintain the amplitude of the current at the reference value during the entire testing procedure.

![Fig. 6.3. Current waveform during scalar speed control ($i_q^* = \text{const.}$).](image)

Similar to the simulation, a second experiment is done, where the reference quadrature axis current ($i_q^*$) varied as a function of frequency (Fig. 4.4). The current waveform for the second situation is presented in Fig. 6.4.

![Fig. 6.4. Current waveform during scalar speed control ($i_q^*(f^*)$).](image)

The decrease in current magnitude can be observed in the first region of Fig. 6.4. Compared to the initial situation, more powerful oscillations appear in the system. Because the result obtained here is similar with the simulation, the same conclusions are valid.

### 6.2.2 Load torque variation

As a second test, the load torque is modified in steps, to test the response of scalar control, when a load disturbance appears in the system. The result presented in Fig. 6.5 shows that the control...
is capable to maintain the stability of the system. When the load torque is applied, the speed decreases only 1.4% from the nominal speed. System stability is achieved again, after one second of transitory regime.

When the load torque is removed, the speed increases with the same magnitude as for the previous case. A decreasing oscillatory regime is encountered in this situation, compared to the previous one. These oscillations can also be observed in the current waveform Fig. 6.6.

This test is done with the reference quadrature axis current \(i_q^*\) constant, to better highlight the disadvantage of this method. Although the control is able to maintain the current at a constant value, as it is required, this operating procedure is not efficient.

### 6.3 Vector Control Experiments

#### 6.3.1 Speed reference variation

All the conditions used to do the simulation are applied for this laboratory experiment.
From Fig. 6.7, it can be seen that the control is able to start the machine in 0.5 seconds, with no initial rotor vibrations. It has to be noted here, that similar to scalar control, the vibration is dependent on the rotor initial position.

![Fig. 6.7. Machine speed during speed reference variation (vector control).](image)

The reduced transition time between steady state situations, highlights the superior dynamic performance of vector control, compared to scalar control.

From the current waveform, presented in Fig. 6.8, it can be seen that the current is maintained between the safety boundaries, during the transient regime. Also, a far better efficiency is achieved, compared to scalar control, through MTPA strategy.

![Fig. 6.8. Current waveform during vector speed control.](image)

### 6.3.2 Load torque variation

In the second test, the stability of the control, during load torque variation, is tested. The load torque is applied at the shaft, using the secondary machine. The result of the test is presented in Fig. 6.9. As it can be seen, when the load torque is applied, the control is capable to correct the 3.6% speed decrease, in approximately three seconds.
When the load torque is removed, the speed reaches a maximum value of 6%, above the nominal speed. As for the previous situation, the control is capable to ensure stability, by reducing the speed at nominal value, in approximately four seconds.

Fig. 6.9. Machine speed (red) and load torque (blue), during load torque variation (vector control).

The current waveform, presented in Fig. 6.10, displays the current transition during the entire experiment. As it can be seen, during the load torque transition, the current is maintained inside predefined limits to ensure safe operation.

Fig. 6.10. Current waveform during load torque variation.

### 6.3.3 Transition from motor to generator

From Fig. 6.11 it can be seen that the transitory regime is very similar to the previous case. The speed increases at the moment when the torque is applied with approximately 1.6%. The control is able to limit the speed increase and to stabilise the system.

When the load torque is removed, the machine changes to motor mode and the speed decreases. As for the previous case, the control is able to stabilise the system, and to ensure nominal speed.
The current waveform (Fig. 6.12), during the entire process, is very similar with the previous case. The control ensures that the current is maintained between the safety margins during the transition from motor to generator and back.

To observe the current direction during generator mode, the DC link current that enters the converter was measured with the oscilloscope.
As it can be seen from Fig. 6.13, the DC link current that enters the converter (red line), has a negative sign, meaning that the current flows from the converter to the resistor.

### 6.3.4 Emergency breaking

To observe the difference between simulation and experiment, the same test conditions were used. From Fig. 6.14, it can be seen that the transition from nominal to zero speed is linear. The control is capable to follow the ramp reference given.

When the speed is reduced close to zero, the control encounters stability problems, because the speed and position estimator cannot provide very accurate information.

Although the speed of the machine will not be kept constant at zero, the sensorless control can maintain the speed in a low range, characterised by rotor vibrations.
The difference between the simulation and experiment is consistent during the low speed operation. This is because the experiment requires accurate position information to maintain stability. Because the position cannot be estimated at zero speed, the speed cannot be maintained zero. In order to obtain better control at very small speed, a dedicated position estimator has to be implemented in the control.

The current waveform is presented for the entire test in Fig. 6.15. As it can be seen, the current increases slightly in magnitude, as the speed decreases. When the speed of the machine reaches values closed to zero, the current maintains a high magnitude to produce sufficient torque.

6.3.5 Holding the machine at zero speed

The result of the test is presented in Fig. 6.16. From the result it can be seen that when a load torque is applied at the shaft, the control encounters problems to maintain the stability.

Similar with the emergency breaking case, at low speed the control is unable to maintain the speed at a constant zero value. The reason for this problem is the same as for the previous case.
Another observation has to be made here. If a considerable torque step is applied at the shaft, the control is not able to counteract, causing instability.

The current waveform from Fig. 6.17, presents a similar behaviour to the previous case (Fig. 6.15). During low speed operation the current is situated inside the safety margins, and has an irregular form, caused by the poor stability.
7

Conclusions

From the current project a series of conclusions can be drawn. These conclusions are separated based on the topic they address.

- **Conclusions regarding the converter:**

  The three level NPC converter is a viable solution for this wind turbine application, because it provides numerous advantages compared to the two level converter, while the disadvantages are not so significant.

  The prototype constructed in the laboratory was able to fulfill all the requirements imposed during the experiments.

- **Conclusions regarding the control:**

  The scalar control strategy implemented in the current project cannot be implemented as the main control for the wind turbine, because it cannot provide stability in all situations.

  Scalar control can be recommended for certain situations, as maintenance situations, when the speed of the turbine is small [19].

  The speed and position estimator provided fast and accurate information, for the medium and high speed range, as it was observed in simulations and experiments.

  Problems were encountered at speeds closed to zero, as it could be seen in the experiments, because the estimator determines the position from the back-EMF term, which is proportional with the speed.

  The sensorless vector control was able to maintain the stability, and to provide good dynamic response during the starting procedure.

  For a more stable operation at zero and very low speeds, a dedicated estimator has to be implemented.
Appendix A. Reference Frame Transformation

To create the mathematical model of an electrical machine the three phase “abc” system was initially used, because it relates to the physical machine [30, 31]. Because this system comes with disadvantages like time varying components and complex differential equations, new reference frame transformations were developed to deal with these problems. The new variables obtained, after reference frame transformation, do not have a physical correlation to the real variables, which are encountered in the three phase ‘abc’ system.

a) Reference frame transformation from “abc” to “αβ0”

If we consider the three phase system “abc” and the complex domain, in which “a” axis is along the real axis, the ”αβ0” system can be developed, where α is along the real axis, β is along the imaginary axis and 0 is the zero component of the three phase system, perpendicular to the plan of the paper. It should be noted that the αβ0 reference frame is fixed to the stator. The transformations from “abc” to “αβ0” reference frame and vice versa are made using the transformation matrix presented in [1] and [2] [30, 31].

This new reference frame presents advantages in the study of transient regimes for unbalanced three-phase circuits [30, 31].

\[
[T_{αβ0}] = \begin{bmatrix}
\frac{2}{3} & -\frac{1}{2} & -\frac{1}{2} \\
0 & \sqrt{3}/2 & -\sqrt{3}/2 \\
\frac{1}{2} & 1 & 1
\end{bmatrix} \quad [1]
\]

\[
[T_{αβ0}]^{-1} = \begin{bmatrix}
1 & 0 & 1 \\
\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\
-\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1
\end{bmatrix} \quad [2]
\]

Figure 1. Reference frame transformation from “abc” to “αβ0”.

b) Reference frame transformation from “abc” to “dq0”

As in the ”αβ0” reference frame the “dq0” reference frame is represented in the complex domain, where the “d” axis is along the real axis, the “q” axis is along the imaginary axis and the zero component is the same [30, 31]. The difference between these two reference frames is that the “dq0” is fixed to the rotor and it is rotating with the same speed \(ω_r\) compared to the stator.
The transformation from “abc” to “dq0” reference frame is made using the transformation matrix presented in, also called Park matrix [30, 31]. To make the transformation from “dq0” back to “abc” the inverse of the matrix is required. This matrix is presented in [4].

\[
[T_{dq0}]
\begin{bmatrix}
\cos \theta & \cos \left( \theta - \frac{2\pi}{3} \right) & \cos \left( \theta + \frac{2\pi}{3} \right) \\
\frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\
-\sin \theta & -\sin \left( \theta - \frac{2\pi}{3} \right) & -\sin \left( \theta + \frac{2\pi}{3} \right)
\end{bmatrix}
\]

\[
[T_{dq0}]^{-1} = \begin{bmatrix}
\cos \theta & -\sin \theta & 1 \\
\cos \left( \theta - \frac{2\pi}{3} \right) & -\sin \left( \theta - \frac{2\pi}{3} \right) & 1 \\
\cos \left( \theta + \frac{2\pi}{3} \right) & -\sin \left( \theta + \frac{2\pi}{3} \right) & 1
\end{bmatrix}
\]

For this transformation the equivalence between the number of turns in the real machine and in the equivalent machine is:

\[
n_d = n_q = n_a
\]

, where \( n_{d,q,a} \) - number of turns on d, q or a axis;

The balance of powers between the “abc” and the “dq0” reference frame is affected by the \( 3/2 \) coefficient [30, 31]:

\[
p = u_a i_a + u_b i_b + u_c i_c = \frac{3}{2} (u_d i_d + u_q i_q + u_0 i_0)
\]

c) Reference frame transformation from “aβ0” to “dq0”

In many applications it is also required to perform the transformation from “aβ0” to “dq0”. As stated before the difference between the two is that “aβ0” reference frames is fixed to the stator and “dq0” reference frames is fixed to the rotor and is rotating with the same speed.

The transformation from “aβ0” to “dq0” reference frame is made using the transformation matrix given in [7], and inverse transformation from “dq0” to “aβ0” is also presented in [8].

Reference source not found.
Figure 3. Reference frame transformation from "αβ0" to "dq0".

\[
[T_\theta] = \begin{bmatrix}
\cos \theta & \sin \theta & 0 \\
-\sin \theta & \cos \theta & 0 \\
0 & 0 & 1
\end{bmatrix} \quad [7]
\]

\[
[T_\theta]^{-1} = \begin{bmatrix}
\cos \theta & -\sin \theta & 0 \\
\sin \theta & \cos \theta & 0 \\
0 & 0 & 1
\end{bmatrix} \quad [8]
\]
Appendix B. Neutral Point Voltage Balance Results

To ensure neutral point voltage balance, the SVM method presented in Modulation Strategies subchapter was implemented on the DSP. An RL load was used to test the modulation.

From Figure 4, it can be seen that the modulation produces nine voltage levels (±400V, ±300V, ±200V, ±100V, 0V), as it was expected. All these voltage levels appear because the modulation index is set to one.

From Figure 5, the phase to phase voltage is observed. In this situation, five voltage levels appear (±600V, ±300V, 0V).

For all the experiments done in the laboratory, sinusoidal pulse width modulation is used. This control does not have the capability to maintain the neutral point voltage balance, when an external influence appears. However, if no such influence appears, the balance is maintained naturally by the modulation, as it can be seen from the following oscilloscope captures.
Figure 6. Speed reference variation (scalar control).

Figure 7. Load torque variation (scalar control).

Figure 8. Speed reference variation (vector control).
Figure 9. Load torque variation (vector control).

Figure 10. Transition from motor to generator (vector control).

Figure 11. Emergency breaking (vector control).
As it could be seen from all the oscilloscope captures, the natural balance of the DC link is maintained during the test procedure.

It has to be noted here though, that it is recommended to implement a balance control algorithm, to ensure safe operation, in all situations.
### Appendix C. Numeric Parameters

The parameters used to construct the Simulink model and to implement the control are presented in the following table.

<table>
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<th>Name</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Speed</td>
<td>$N_r$</td>
<td>500</td>
<td>[rpm]</td>
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<tr>
<td>Stator Resistance</td>
<td>$R_s$</td>
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<td>[Ω]</td>
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<td>[H]</td>
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<tr>
<td>Synchronous Inductance</td>
<td>$L_q$</td>
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<td>[H]</td>
</tr>
<tr>
<td>PM Flux Linkage</td>
<td>$\lambda_{mpm}$</td>
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<td>[Wb]</td>
</tr>
<tr>
<td>No. of pole pairs</td>
<td>$p$</td>
<td>6</td>
<td>[-]</td>
</tr>
<tr>
<td>Viscuous Damping</td>
<td>$B$</td>
<td>1e-3</td>
<td>[-]</td>
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<td>[Nm]</td>
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<td>Rotor Moment of Inertia</td>
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<td>[kg*m²]</td>
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<td>[s]</td>
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Bibliography


[29] J. N. Khan, "Design Considerations in Using the Inverter Gate Driver Optocouplers for Variable Speed Motor Drives,"
