New Synthetic Test Circuit for the Operational Test of HVDC Thyristor Valve

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SUMMARY

In general, the power handling capability of thyristors in the classical HVDC systems has seen significant progress in the past thirty years. It was known that five or more thyristor levels in a valve section should be tested for the adequate representation in case of valve section composed of twelve or more levels in series. This means that if we adopt the direct testing for the valve section or valve, we need very large testing power, which is not the practical solution. As a result, all HVDC valve manufactures are using synthetic testing method recommended by CIGRE as an alternative to the direct testing.

Synthetic testing methods are based on the fact that the HVDC thyristor valve is stressed by current and voltage at different time intervals. The current stress occurs during the conduction interval followed by the voltage stress during the blocking interval of the valve. If we use two separate power sources, one voltage source and one current source, at different time intervals, it is possible to apply the voltage stress and the current stress to the test valve independently. This means that we can minimize the power required for valve test. Voltage and current stresses on a test thyristor valve can be analysed separately in four operation states: off-state and reverse voltage, turn-on, on-state and turn-off state. Key points of synthetic test circuit are how to control the transition intervals from one operation state to another operation state, critically from on-state to off-state or the opposite direction.

This paper proposes a new STC (Synthetic Test Circuit) by adopting two-phase chopper with an auxiliary switching circuit for the turn-off of the “so-called isolation thyristor”. Also the proposed STC can minimize the power ratings of the current source equipment by supplying “the gate power of the test thyristors” through the resonant circuit side, not from the current source side. And the gate power of the thyristors in the resonant circuit is supplied through the independent high frequency power source. The proposed STC was tested under the requirement of IEC 9.3.1~9.3.3.

KEYWORDS

Classical HVDC, Synthetic Test Circuit, Thyristor Valve Test, Operation Test, IEC 60700-1

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1. INTRODUCTION

The HVDC power converter operates in extremely high-voltage and high power condition. So, many thyristors are connected in series to comprise one valve in the power converter. The normal or abnormal operations of power converter should be tested before it is commissioned on site. A huge test facility is required if the power converter is tested under full power and voltage, which consumes a huge amount of power and expense. According to IEC 60700-1, HVDC valve type test is composed of dielectric test and the operational tests. Main purpose of the dielectric test is ac withstanding test, DC withstanding test and impulse voltage test. However, the operational tests are more complicated than dielectric tests for the simulating various operation conditions of valve. They involve not only voltage, but also a high current, simultaneously with di/dt, dv/dt and thermal capability and so on. For the operation test, STC (Synthetic Test Circuit) was usually adopted. Several STC were proposed and implemented by HVDC manufactures [1]-[4].

As shown in Fig.1, STC is typically consisted of a low voltage and high current source, a high voltage and low current source and a resonant circuit [2]. The main purpose of resonant circuit is for the voltage waveform generation across the test thyristor during the turn-off operation. Between the current source and the resonant circuit, there is “so-called isolation thyristor (V_{a1})” which connects or disconnects the test thyristor (V_T) from the low voltage and high current source.

The initial charging of capacitor (C_s) is done by turning on thyristor (V_{a2}). By using the Fig 1(b) waveforms, the basic operations can be explained [2]. It is assumed that the capacitor (C_s) is charged. When the thyristors (V_{a1} and V_T) are turned on, the low voltage high current source provides the current (I_0) through these two thyristors. When the thyristor (V_{a1}) is turned on at time t_1, thyristor (V_{a1}) is turned-off. Resonant circuit (C_s – V_{a3} – L_1 – V_T) begin to inject the resonant current through thyristor (V_T), and thyristors (V_{a3} and V_T) are turned-off at t_3. When thyristor (V_{a4}) is turned on at t_3, the reverse voltage across the capacitor (C_s) is applied to thyristor (V_T) through the resonant circuit path (C_s-V_T-L_1-V_{a4}). When thyristor (V_{a5}) is turned on at t_4, the current path (C_s-V_T-L_1-V_{a4}) forms another resonant circuit. The capacitor (C_s) voltage is reversed and thyristors (V_{a5} and V_{a4}) are turned-off at t_5. When V_{a3} is turned on at t_5, a forward voltage is applied to thyristor (V_T). When V_{a2} is turned on at t_7, the high voltage source charges the capacitor (C_s) to compensate the voltage reduction due to the resonant losses. If the C_s is fully charged, V_{a2} is turned off automatically. When thyristor (V_T) is turned on at t_9, the thyristor (V_T) goes down to zero and the turn-on current begin to increase up to I_{th}.

In general, HVDC valve thyristor gets the gate control power from the snubber capacitor circuit across the valve thyristor. This means we need several hundred voltages for each thyristor, depending on the gate driver circuit design. Typically thyristor (V_{a1} and V_T) in Fig. 1 is composed of more than five thyristors in minimum, respectively. This means that the output voltage of current source should have enough voltage level to conduct at least ten thyristor in series. For example, if each thyristor level needs 500V, the output voltage of the current source should be greater than 5000V. If the test current is 2000A (typical values), then the required power ratings of the current source will be MW level.

In this paper, we proposed a new STC to minimize the power ratings of the current source by modifying the resonant circuit to supply the gate driver power from the resonant circuit and supplying the gate power of the thyristors in resonant circuit from the independent high frequency power source. The proposed STC was tested under the requirement of IEC 9.3.1–9.3.3.

![Conventional STC circuit and its operation waveforms.](image)

(a) Circuit diagram. (b) Operation waveforms of STC
2. Proposed Synthetic Test Circuit: Part of Resonant Circuit

Fig. 2 shows the part of resonant circuit in the proposed STC. Compared to the conventional STC in Fig. 1, the proposed STC adopted an additional thyristor ($V_{aux}$) in parallel with test thyristor ($V_T$). Additional modification is that all thyristors except for test thyristor ($V_T$) in Fig. 2 get gate drive power from the independent power supply as shown in Fig. 3. Without the help of thyristor ($V_{aux}$), we can’t turn on the test thyristor ($V_T$) since we can’t obtain enough voltage from the current source if we want to minimize the power rating of the current source by adopting low voltage current source.

The principle of operation is as follows. When $V_{a2}$ is turn-on, capacitor ($C_s$) is charged to the level of voltage source. Before turning test thyristor ($V_T$) on, we need to charge the snubber capacitor of thyristor ($V_T$) to the appropriate voltage level and polarity. If $V_3$ is turn-on, then equivalent $C_t$ is charged to initial DC voltage. However, we can’t turn $V_{a4}$ on because $V_{a4}$ is reverse-biased before we could discharge the voltage of the $C_t$. Under this condition, the gate control power of the test thyristor ($V_T$) is not supplied. This means we can’t turn the test thyristor ($V_T$) on. On the other hand, if the auxiliary thyristor ($V_{aux}$) and thyristor ($V_{a3}$) are turned-on simultaneously, thyristor ($V_{a4}$) is forwardly biased and provides a path to supply alternative high ac voltage across the test thyristor ($V_T$). During normal test operation, auxiliary thyristor ($V_{aux}$) is turned off and no effect on the main operation. Auxiliary thyristor ($V_{aux}$) is only used for the initial charging the snubber capacitor before turning on the test thyristor ($V_T$).

![Fig. 2 Configuration of proposed synthetic test circuit](image)

![Fig. 3 Power supply of the thyristor gate driver using high frequency ac power supply with high voltage insulation.](image)
3. Proposed Synthetic Test Circuit: Part of Current Source

Fig. 4 shows the part of current source in the proposed STC. The proposed STC is consisted of a two phase chopper with thyristor (Vₘ1) turn-off circuit, and a six pulse thyristor rectifier for the low voltage current source. The operation of the proposed STC can be explained with the help of Fig. 5. Detailed operation was explained in [5]. Six pulse thyristor rectifier converts AC voltage waveform to controlled low DC voltage. And two-phase chopper (IGBT1, UGBT2, Lₐ, Lₜ, Diode1 and Diode2) convert the DC voltage to the controlled current source. The output waveform of the current source is controlled by the two-phase chopper by adopting high frequency PWM control. The resonant circuit is same to the Fig.2. The purpose of IGBT3, IGBT4, diode rectifier and capacitor (C) is to turn-off isolation thyristor (Vₘ1). Namely, it is for forced commutation circuit. The power rating of turn-off circuit for thyristor (Vₘ1) is very small. Instead of the proposed two phase chopper, we can adopt the conventional 6-pulse back to back thyristor converter.

![Fig. 4 Configuration of the proposed synthetic test circuit: part of current source](image)

![Fig. 5 Operation waveforms and the gating signal diagram.](image)
4. Experimental Results

Fig. 6 shows the block diagram and the photograph of the gate driver power in the resonant circuit. Single high frequency ac power supply is connected to each gate driver card in series through the high voltage insulation transformer. Fig. 7 to Fig. 10 shows a simulation and experimental result defined in the IEC 9.3.1 to IEC 9.3.3.2 items. In this experiment, we adopted the conventional 6-pulse back to back thyristor converter. Table-1 shows the several key specifications for the STC.

Fig. 6 Photograph of the gate driver power in the resonant circuit.

Fig. 7 shows the maximum continuous operating duty test. The current value is $456A_{\text{rms}}$, and the reverse and blocking voltage of $V_T$ is $12.4kV$. It is shown that the simulation and experimental results are almost the same. A small ringing at the flat top in experiment can be reduced with improved current control. Fig. 8 shows a simulation and experimental result for the maximum temporary operating duty test ($\alpha=90^\circ$). In this test the applied voltage to the test valve $V_T$ should be the peak value of the AC source voltage of HVDC converter. The voltage and current waveforms in Fig. 8 show peak voltage of $10.2kV$ and $427A_{\text{rms}}$, respectively.

Fig. 9 shows a simulation and experimental result for the minimum AC voltage test with minimum delay angle. The applied blocking voltage to $V_T$ at minimum delay angle corresponds to around $2.4kV$. It is shown that the circuit operates well under the condition of $2.4kV$ and $414A$. Fig. 10 shows a simulation and experimental result for the minimum AC voltage test with minimum extinction angle. The operation of this test is similar to that in Fig. 9 except the firing angle position.

<table>
<thead>
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<th>Test items</th>
<th>Time</th>
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<th>Voltage</th>
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<tr>
<td>Heat Run Test</td>
<td>60 Min</td>
<td>$396A_{\text{peak}}$</td>
<td>$9.6kV$</td>
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<tr>
<td>Max. Temporary Operating Duty ($\alpha=90^\circ$) Test</td>
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<td>$&gt;100A$</td>
<td>$19kV$</td>
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<td>Min. Delay Angle Test</td>
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<td>$396A_{\text{peak}}$</td>
<td>$2.5kV$</td>
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<tr>
<td>Min. Extinction Angle Test</td>
<td>15 Min</td>
<td>$396A_{\text{peak}}$</td>
<td>$2.9kV$</td>
</tr>
<tr>
<td>Intermittent DC test</td>
<td>10 Min</td>
<td>$396A_{\text{peak}}$</td>
<td>$8.0kV$</td>
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<tr>
<td>Test with transient forward voltage during recovery</td>
<td>10 $\mu$s</td>
<td>$396A_{\text{peak}}$</td>
<td>$24kV$</td>
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<td></td>
<td>1.2 $\mu$s</td>
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<tr>
<td></td>
<td>100 $\mu$s</td>
<td>$396A_{\text{peak}}$</td>
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Fig. 7 HV Circuit Control: Maximum continuous operating duty tests (IEC 9.3.1)

Fig. 8 HV Circuit Control: Maximum temporary operating duty test ($\alpha=90^\circ$, IEC 9.3.2)

Fig. 9 Minimum delay angle test (IEC 9.3.3.1)

Fig. 10 Minimum extinction angle test (IEC 9.3.3.2)
5. CONCLUSION

In this paper, a new STC for HVDC valve was proposed. The operation of the proposed STC was verified through the simulation and experiment. It was verified that the proposed STC is satisfying the requirement of IEC 9.3.1~9.3.3 standard for the HVDC valve test. Even though the power rating of current source is very low, but it can be applicable to the operation test of the very high power HVDC valve. Now we are going to increase the maximum test current of the thyristor valve up to several kA levels, or GW system power level.

BIBLIOGRAPHY


