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Modeling and Grid impedance Variation Analysis of Parallel Connected Grid Connected Inverter based on Impedance Based Harmonic Analysis

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Abstract - This paper addresses the harmonic compensation error problem existing with parallel connected inverter in the same grid interface conditions by means of impedance-based analysis and modeling. Unlike the single grid connected inverter, it is found that multiple parallel connected inverters and grid impedance can make influence to each other if they each have a harmonic compensation function. The analysis method proposed in this paper is based on the relationship between the overall output impedance and input impedance of parallel connected inverter, where controller gain design method, which can minimize the compensation error under various conditions, is also proposed.

Keywords – P+Resonant current controller, Power quality, Parallel-connected inverters, Harmonic compensation

I. Introduction

The demand in the power electronic based energy conversion technology and the development of improving the reliability and efficiency of power converter are important issues todays as the grid is becoming much more power electronics interfaced [1, 2]. Recently, parallel connected Distributed Generation (DG) systems have been emerging with the requirement of renewable energy source and energy storage system [3]. Besides, the harmonic current limitation in the grid network composed by various inverters, passive and active loads are strictly required to minimize the current distortion in the present grid network.

To restrict the harmonics, which can come from each grid connected inverter, harmonic compensation according to the standards like *IEEE 519*, *VDEW*[4] and their performance on the overall operation are very important. Especially, German Electricity Association standard for generators connected to a medium-voltage network, *VDEW* uses the SCR(Short Circuit Ratio) component in the calculation of the harmonic current limitation because the harmonic limitation value is changed according to the grid status [5]. For medium-low voltage grids, the maximum values must not be exceeded as shown in TABLE I, where I_{hlim} is the relative maximum current for 10 kV and 20 kV line voltage.

Recently, for single and parallel grid connected inverters used in DG applications, various harmonic compensation solutions are studied [6-8] to reduce the harmonic components according to the standards. Harmonic current filtering and resonance damping methods are studied in islanded micro-grid application to reduce the voltage and current harmonic components by adjusting a variable fundamental impedance and also a variable harmonic impedance [8, 9]. To avoid voltage disturbance caused by power electronics based system and non-linear load, the voltage and current controlled harmonic compensation method also have been demonstrated [10].

TABLE I
VDEW Harmonic Current Limit ($h \leq 25^{th}$) for medium voltage level [4] as a limitation of the Short Circuit Ratio(SCR)

Ordinal number [v]	I_{hlim}/SCR [A/MVA]	
-	10kV	20kV
3, 5	0.115	0.058
7	0.082	0.041
9, 11	0.052	0.026
13	0.038	0.019
15, 17	0.022	0.011
19	0.018	0.009
21, 23	0.012	0.006
25	0.01	0.005
>25 or even	0.06/v	0.03/v

Furthermore, various research have also been conducted to address the interaction of the inverter controllers [11-13]. To analyze harmonic instability in the power electronics AC system, control loop interaction between two current controlled inverters and voltage controlled inverter are studied based on impedance analysis method [11]. Impedance and admittance based analysis methods have also been used to reveal the interaction between the converter current control and grid impedance. The impedance regions have also been developed to reduce the sensitivity of the converter and to obtain a good gain and phase margin [14-16]. However, the harmonic compensation error in the parallel connected inverter is overlooked.

In this paper, a comprehensive analysis of the harmonic compensation error and instability problem in a parallel connected inverter is achieved by various combinations of parallel connected inverters. It is well understood that harmonic cancelation is an essential function to the devices connected to the DG network. But most research [6-8, 11] are performed in the same conditions like same power rating and

same controller performance. Hence, studies on the harmonic compensation error derived from unknown parallel connected inverters are urgently required. To demonstrate this problem, parallel connected inverters considering grid impedance are modeled based on impedance based analysis. Next, theoretical analysis of the sensitivity and dynamic performance of harmonic compensator of specific inverter is performed in the various DG network conditions. Additionally, a controller gain design method considering n-paralleled inverters, which can minimize the harmonic compensation error, is proposed. The analyzed result is verified by means of Simulink-PLECS Block-set simulations.

II. Modeling of Grid Connected Inverter

A. Single Grid Connected Inverter

The well-known three-phase grid connected converter topology with *L*-filter is used to do a generalized analysis. Even though the widely used *LCL*-filter also can be considered as another case, this can also be modeled as an *L*-filter in the frequency range below the *LCL*-resonance frequency [17, 18]. Hence, analysis based on the *L*-filter topology is adaptable in low frequency harmonic analysis. Further p.u systems are adopted to define the output filter and controller gain to compare the system according to the power rating for the harmonic compensation. Grid impedance values are regarded as the %Z (percent Impedance), which can be calculated from the grid Short Circuit Ratio (SCR=(1/(%Z)), are also derived from a system p.u value.

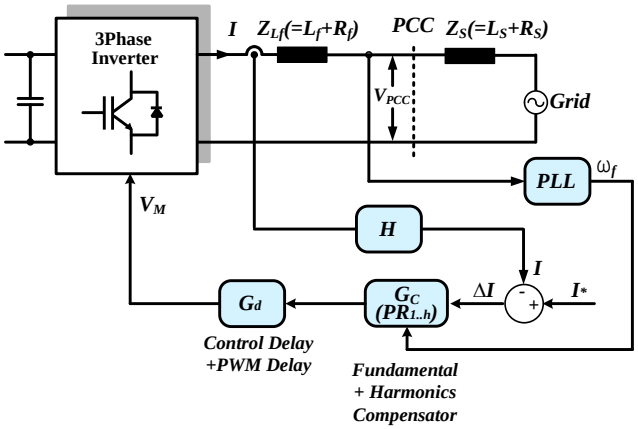


Fig. 1. Three-phase grid connected converter topology and basic control block diagram of single grid connected inverter.

Fig. 1 shows the controller and the circuit diagram of the converter, where the Proportional Resonant (PR) controller for current harmonic compensation G_c, the control delay G_d, inverter side filter inductor L_f, inductor parasitic resistance R_f, current sensor gain H, and $Z_s(=L_s + R_s)$ is describing the grid impedance. Each component of the block diagram can be expressed in the s-domain as :

$$Y_{Mf} = \left.\frac{I}{V_M}\right|_{V_{PCC}=0} = \frac{1}{Z_{Lf}} \tag{3}$$

$$Y_{of} = \left.\frac{-I}{V_{PCC}}\right|_{V_M=0} = \frac{1}{Z_{Lf}} \tag{4}$$

where the *L*-filter output admittance Y_{Mf} is the converter loop gain term, and the minor loop gain Y_{of} is describing the admittance obtained between the grid current and the PCC (Point of Common Coupling) side grid voltage.

$$G_c = K_p + \frac{K_{i(f)}\cdot s}{s^2+\omega_f^2} + \sum_{h=3,5,7,11,13} \frac{K_{i(h)}\cdot s}{s^2+(h\cdot\omega_f)^2} \tag{5}$$

$$G_d = e^{-1.5\cdot s\cdot T_s} \tag{6}$$

$$T_{cf} = G_c \cdot G_d \cdot Y_{Mf} \tag{7}$$

$$Y_{ocf} = \frac{Y_{of}}{1+T_{cf}} \tag{8}$$

$$G_{clf} = \frac{T_{cf}}{1+T_{cf}} \tag{9}$$

$$I = G_{clf} \cdot I^* - Y_{ocf} \cdot V_{PCC} \tag{10}$$

where the harmonic PR controller G_c, delay term including computation delay and PWM delay G_d considering the sampling frequency, the open loop gain of the control loop T_{cf}, the closed loop input admittance $Y_{ocf,}$ the closed loop gain $G_{clf,}$ and the current sensing feedback gain H, which is assumed as a constant gain '1' [19].

To mitigate the current harmonics in the inverter, various kind of harmonic compensation methods have been used in the different topologies [6, 20, 21]. In particular, the most reliable method for harmonic compensation is to increase the gain of the current controller at each harmonic frequency. Hence, only the proportional resonant controller will be considered in the analysis. At this point, the *PLL* also can be a component, which can affect the harmonic compensation performance due to a phase angle tracking error in the distorted grid voltage. However, this is not considered in this paper in order just to focus on the relationship between input and output impedance based analysis in the parallel connected grid inverters.

The system parameters derived from the p.u based design method are described in TABLE II. The parasitic resistance of the filter inductance and resistance in the grid impedance are regarded as 10 % of the base inductance value, which is calculated based on Fig. 3. Also a 5 kHz switching frequency is used as the nominal value for high power rated converters higher than100 kW because it depends on the current rating of filter inductor and control system bandwidth. In the case of harmonic compensation controller, PR controller gains are determined according to the system parameter considering the relationship ($f_{sw}/10 < f_g < f_{sw}/3$) between the gain cross over frequency (f_g) and the switching frequency (f_{sw}) [21]. To implement the PR controller in practical non-linear simulation, two methods are adopted [18, 21, 22] instead of a classical PR controller – see (5).

TABLE II. p.u based system parameter - examples
(a) Inverter parameter and controller gain, (b) Grid impedance calculation result according to the SCR

(a)

Inverter Type	Power Rating (kW)	Vrms (V)	freq (Hz)	Lf mH	Rf Ohm
#1	10.0	380.0	50.0	1.84	0.058
#2	100.0	380.0	50.0	0.184	0.0058

Inverter Type	Switching Frequency (Hz)	$\omega_{c(max)}$ (Hz)	Lf (mH)	Kp	Ki(f,h)
#1	10000	1000	1.84	11.6	7260
#2	5000	500	0.184	0.578	181

(b)

Z (%)	SCR (1/(%Z))	Ls(#1) mH	Ls(#2) mH	Rs(#1) Ohm	Rs(#2) Ohm
1	100	0.46	0.046	0.014	0.0014
5	20	2.3	0.23	0.07	0.0072
33	3	15.33	1.533	0.48	0.048

In [21], equation (11), where K_p and K_i values design guide was proposed considering the gain cross over frequency ω_c, filter inductance L_f and disturbance tracking error in the *S*-domain. Additionally, the PR controller which has a delay compensation function ϕ_h^* is studied in [18, 22], where the sampling frequency is T_s, and the harmonic order number h, fundamental frequency ω_f are described in (12). Even though a K_{P_sen} design guide is also studied in [18] according to the minimization method of sensitivity error in *Z*-domain, the calculated K_{p_sen} result is same with the equation (11). Hence, a more simple equation (11) is used in the simulation study. The p.u based design is also used in the determination of the gain value in order to increase the generalization of the analysis.

$$K_p = \frac{\omega_{c(\max)} \cdot L_f}{V_{dc}} \quad , \quad K_{i(f,h)} = \frac{K_p \cdot V_{dc} \cdot \omega_{c(\max)}}{10} \tag{11}$$

$$G_c = K_{p\_sen} + K_{i(f,h)} \frac{s \cdot \cos(\phi_h^*) - h \cdot \omega_f \cdot \sin(\phi_h^*)}{s^2 + h^2 \omega_f^2} \left(where, \phi_h^* = \frac{\pi}{2} + \frac{3}{2} h \omega_f T_s\right)$$

$$K_{p\_sen} = \frac{R_f}{(1-\rho^{-1})\sqrt{2}} \sqrt{2+2\rho^{-2}-(1+\sqrt{5})\rho^{-1}}, \left(where, \rho = e^{R_f T_s / L_f}\right) \tag{12}$$

B. Multi-Grid Connected Inverter

The impedance based models for 2 paralleled inverter and loads are described in equation (13)~(15), where the load or power factor correction capacitor (PFC) Y_c, connected to the grid network, admittance seen by grid connected inverter at the PCC point $Y_{to,i.}$ the minor feedback loop gain $T_{m,i}$, each current controlled DG inverter injecting current $G_{cl} \cdot i^*$, the grid impedance is assumed as an inductor and resistance components and decided according to the SCR value of the main grid Z_s and $Y_{ocf,i}$ is describing the admittance obtained between the grid current and the PCC side grid voltage. (where 'i' means the number of i-th inverter and 'j' denotes other inverter.)

$$Y_{to,i} = \frac{1}{Z_s} + Y_c + Y_{ocf,j} \tag{13}$$

$$T_{m,i} = \frac{Y_{ocf,i}}{Y_{to,i}} \tag{14}$$

$$I_i = \frac{1}{1+T_{m,i}} \cdot G_{clf,i} \cdot I_i^* - \frac{T_{m,i}}{1+T_{m,i}} \cdot G_{clf,j} \cdot I_j^* - \frac{T_{m,i}}{1+T_{m,i}} \cdot \frac{V_{PCC}}{Z_s} \tag{15}$$

These two-multi connected inverters closed loop impedance model can be generalized in the format of sigma expression as described in equation (16)-(18), when *N*-paralleled connected inverter and loads are considered, where $Y_{to(K,M),i}$, $T_{mKM,i}$, have the same meaning with (13)~(15) respectively. K,M and H are the number of other parallel connected loads, inverter output admittance and the current controlled DG inverter injecting current .

$$Y_{to(K,M),i} = \frac{1}{Z_s} + \sum_{K=0}^{l} Y_{c(K)} + \sum_{M=0}^{n} Y_{oc(M)} \tag{16}$$

$$T_{mKM,i} = \frac{Y_{ocf,i}}{Y_{to(K,M)}} \tag{17}$$

$$I_i = \frac{1}{1+T_{mKM,i}} \cdot G_{clf,i} \cdot I_i^* - \frac{T_{mKM,i}}{1+T_{mKM,i}} \cdot \left(\sum_{H=0}^{n} G_{clf,H} \cdot I_H^*\right) - \frac{T_{mKM,i}}{1+T_{mKM,i}} \cdot \frac{V_S}{Z_s} \tag{18}$$

In Fig. 2, even if these loads($Y_{c(k)}$) are connected to the each inverter, they can be regarded as a combination of parallel impedance because the network is composed of parallel connection and lumped impedance among the inverters and loads are neglected according to the previous study [23].

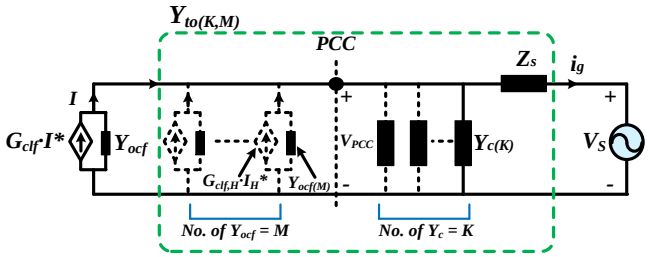


Fig. 2. Multiple inverter system - Closed loop model of multi-parallel connected current controlled inverter and various loads.

III. Impedance Based Analysis of Compensation Error

A. Analysis of impedance variations

To see the effect of the grid impedance variation and the other parallel connected converter, the grid impedance is changed based on the values in TABLE II. In this case, the PFC capacitor or other load components are not considered in the simulations. Impedance related with cable can also be considered in the simulation by changing the percent value of L_f because the lumped cable capacitance can be neglected in the cable model if inter-harmonic or sub-harmonic analysis is not included [23].

According to equation (13)-(15), in order to avoid the disturbance from grid impedance, the closed loop input admittance ($Y_{ocf,i}$) should be lower than the admittance seen

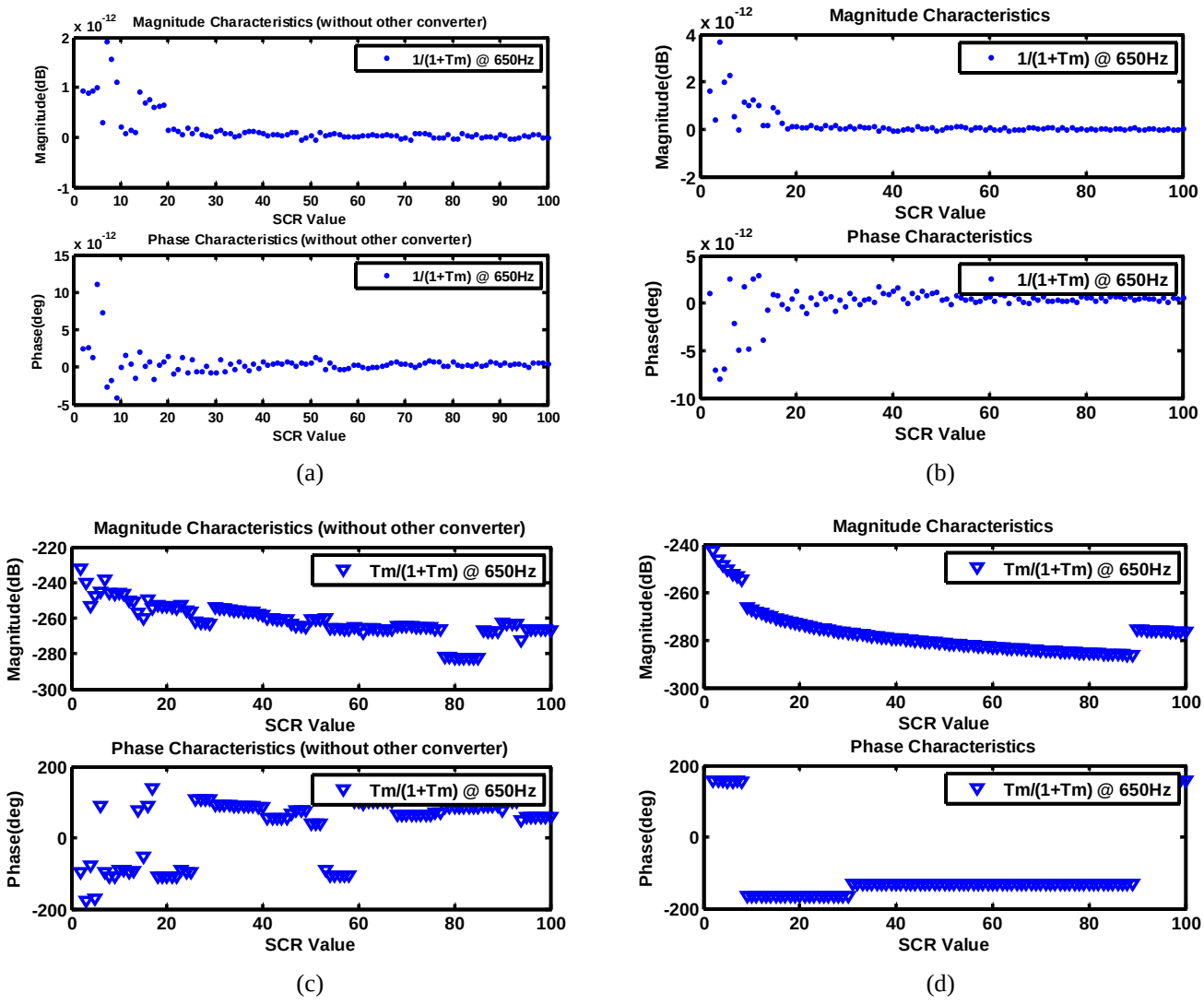


Fig. 3. Grid connected inverter minor loop (T_m) characteristic variation according to the SCR variation.(When, ω_h=2*pi*50*13 in Eq (19)-(20)) (a) Magnitude and Phase ($1/(1+T_m)$) at 13th order frequency considering the grid impedance (b) Magnitude and Phase ($1/(1+T_m)$) at 13th order frequency considering grid impedance and the other parallel connected same rating converter (c) Magnitude and Phase ($T_m/(1+T_m)$) at 13th order frequency considering grid impedance (d) Magnitude and Phase ($T_m/(1+T_m)$) at 13th order frequency considering grid impedance and the other parallel connected same rating converter

by grid ($Y_{to,i}$) to minimize the steady state error with the reference. If the closed loop input admittance ($Y_{ocf,i}$) has the same power rating and topology, the other converter closed loop input admittance ($Y_{ocf,j}$) can also be regarded as a passive element. But if the other converter closed loop input admittance ($Y_{ocf,j}$) has a different rating and a negative admittance component in the system, it can also affect the admittance seen by the grid ($Y_{to,i}$) gain value at each frequency.

It can also be found in equation (13)-(15) that the load admittance (Y_c) can affect the admittance seen by the grid ($Y_{to,i}$) gain value, if Y_c is regarded as the load components which can generate the same harmonic components with the closed loop input admittance ($Y_{ocf,i}$). Otherwise, the load admittance (Y_c) has a negative impedance like a constant power load. However, if the load is not considered and two inverters have the same conditions in the analysis, the minor feedback loop gain ($T_{m,i}$), the admittance seen by grid ($Y_{to,i}$), and the closed loop gain ($T_{cf,i,j}$) can be re-writtten like (19)-(20) at each specific harmonic frequencies (ω_h).

$$I_i(j\omega_h) = \frac{1}{1+T_{m,i}(j\omega_h)} \cdot G_{clf,i}(j\omega_h) \cdot I_i^*(j\omega_h) - \frac{T_{m,i}(j\omega_h)}{1+T_{m,i}(j\omega_h)} \cdot G_{clf,j}(j\omega_h) \cdot I_j^*(j\omega_h) - \frac{T_{m,i}(j\omega_h)}{1+T_{m,i}(j\omega_h)} \cdot \frac{V_s}{Z_s(j\omega_h)} \quad (19)$$

$$T_{m,i}(j\omega_h) = \frac{\frac{Y_{of,i}(j\omega_h)}{1+T_{cf,i}(j\omega_h)}}{\frac{1}{Z_s(j\omega_h)} + \frac{Y_{of,j}(j\omega_h)}{1+T_{cf,j}(j\omega_h)}} = \frac{Y_{ocf,i}(j\omega_h)}{\frac{1}{Z_s(j\omega_h)} + Y_{ocf,j}(j\omega_h)} \quad (20)$$

According to equation (19), if Z_S is '0', $T_{m,i}$ will be '0' in the ideal case. But, if two inverters have different specifications like $Y_{ocf,j} << Y_{ocf,i}$ or $Y_{ocf,j} >> Y_{ocf,i}$ at a specific harmonic frequency, a disturbance related with the sensitivity

can be generated. Similarly, a loop gain error and a minor loop gain error derived from the grid impedance difference is described as shown in Fig 3. The loop gain $T_m/(1+T_m)$ and minor loop gain $1/(1+T_m)$ should be unity `1` value to minimize the error in all grid conditions.

It can also be found that the frequency component near the gain cross over frequency has a different magnitude and phase characteristics according to the grid impedance and the other converter variation as shown in Fig 3. Even though the minor loop gain $1/(1+T_m)$ has a minor effect in the steady state analysis as shown in Fig 3.-(a),(b), the loop gain $T_m/(1+T_m)$ can affect the disturbance from the other parallel connected converter and grid impedance as shown in Fig 3.-(c),(d) and equation (19).

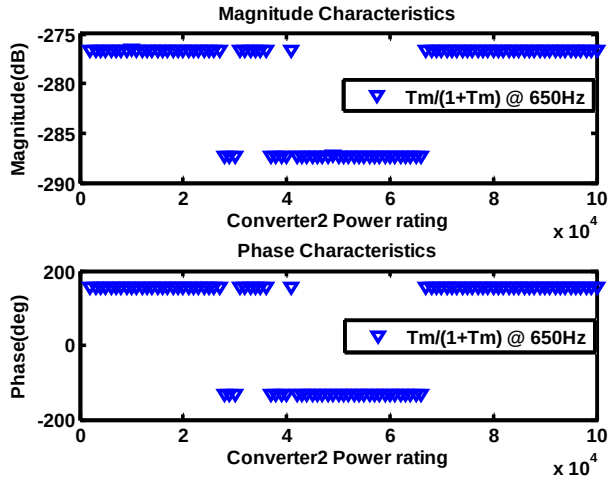


Fig. 4. Grid connected inverter minor loop (T_m) characteristic variation near the gain cross-over frequency (13^{th}) according to the Converter 2 power variation (TABLE II). (When, ω_h=2*pi*50*13 and SCR=100 in Eq(19)-(20))

In the case of the parallel connected converter power rating variation as shown in Fig. 4, the loop gain and the minor loop gain also show a similar variation with the grid impedance variation respectively. Hence, it is needed to design the controller gain through the reflection of grid impedance and parallel connected converter admittance. However, in terms of analyzed converter, the admittance seen from analyzed converter can be regarded as combined grid impedance. According to this assumption, the grid impedance considered only in controller gain design to reduce the compensation error. To implement harmonic compensator in a single converter by considering sensitivity in the design, sensitivity error analysis is also needed to be studied by using system open-loop gain T_c and phase margin respectively [18]. In that study, the sensitivity error is dependent on the $1+T_c$ gain, and not on the phase margin. Hence, the analysis based on the relative impedance amplitude is enough to analyze multi parallel connected inverter in a view of low-order harmonic compensation errors.

B. Proposed gain design method

According to the relation between (19) and (20), the steady state error and harmonic instability status can occur if the grid impedance is not considered in the K_p gain design. Hence, it is needed to improve equations (11), (12) by considering the SCR. Therefore, equation (21) is proposed to increase the gain cross over frequency considering the filter characteristic and grid impedances, where R_s, L_s, the grid impedance components, R_f, L_f, the filter components and Ts, the sampling frequency are introduced. K_{prev} compensates the DC gain at the gain cross over frequency and low frequency range (~13^{th} harmonics).

$$K_{prev} = \frac{R_S C - R_S C^2 - R_S CA + R_S C^2 A}{(A-1)\cdot(B-1)} - \frac{R_f D + R_S C^2 - R_f D^2 A + R_S C^2 A}{(A-1)} \quad (21)$$

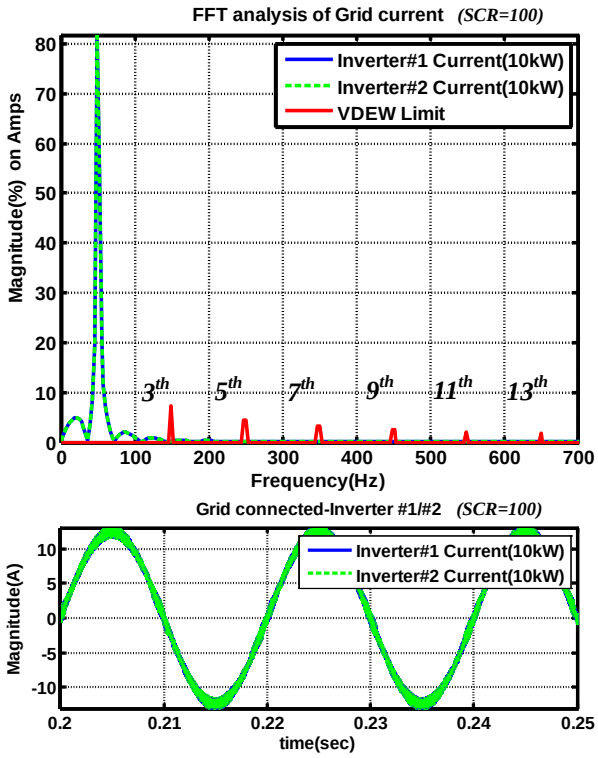
(where, $A = e^{R_f T_s/L_f}$, $B = e^{R_s T_s/L_s}$, $C = e^{\frac{i\omega_f}{10T_s}}$, $D = e^{\frac{i\omega_f}{10T_s}}$)

If the SCR or grid impedance variation range information is known before the installation of a new unit in the present grid network, an adaptable K_p gain design is possible [24].

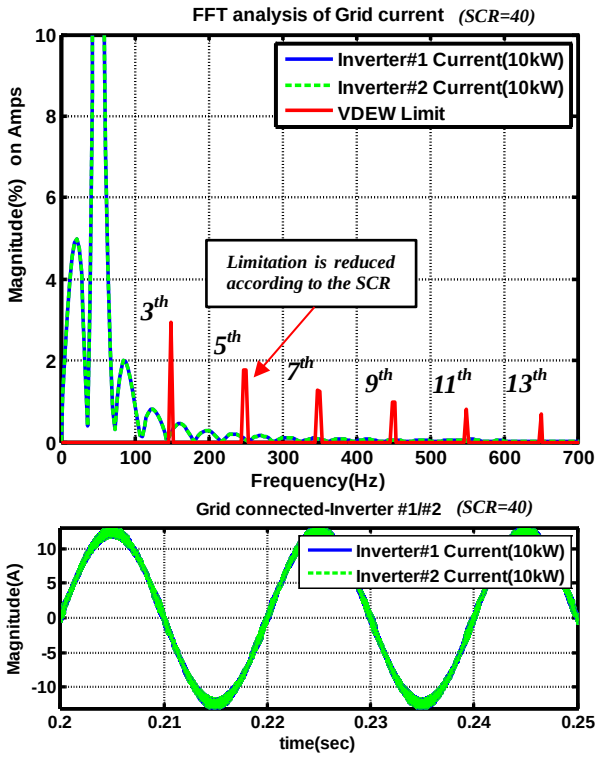
IV. Simulation Results

Simulink PLECS Block-set is used to simulate various case studies. Case studies for the analysis of PR controller disturbance are performed in the 2 paralleled inverters with the following assumptions. The *PLL* settling time is set to be 0.15 sec to avoid negative impedance effect in the operation [9]. Two identical inverter simulation results according to the SCR (grid impedance) variation are depicted in Fig. 5 and Fig. 6. It can be found that the two identical inverters are operating under the VDEW harmonic limitation in Fig. 5-(a). However, in the case of Fig. 5-(b), a harmonic steady state error is generated according to the relationship among the impedance based analysis. Even though the error is small when the result is compared with Fig. 5-(a), it is important to focus on the changed harmonic limitation according to the SCR variation. For low SCR cases, this small error should also be considered in a view of whole system power quality.

It is quite noticeable that if the grid is weak (=large grid impedance), the harmonic compensation error is larger than other conditions and harmonic instability problem can be generated as shown in Fig. 6-(a). Hence, equation (21), which considers the grid impedance, should be used to mitigate harmonics and to make the system in the stability area properly. The simulation result when two identical inverters are connected in the weak grid condition with the proposed gain is depicted in the Fig. 6-(b). It can be found that harmonic frequency component near the gain cross-over frequency (11^{th}, 13^{th}) is well compensated by using the proposed proportional gain design method in the simulation. Also, the theoretical meaning of proposed method is to increase the loop gain at the gain cross over frequency based on the impedance modeling equation and analysis. FFT (Fast Fourier transformation) results and non-linear time domain simulation results are not only well matched with the impedance based analysis results but also demonstrate a performance under the VDEW harmonic limitation.

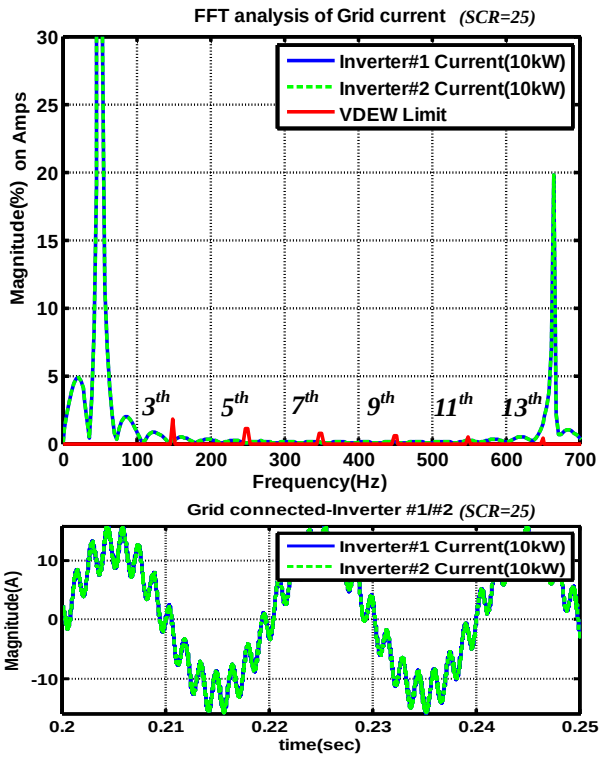


(a)

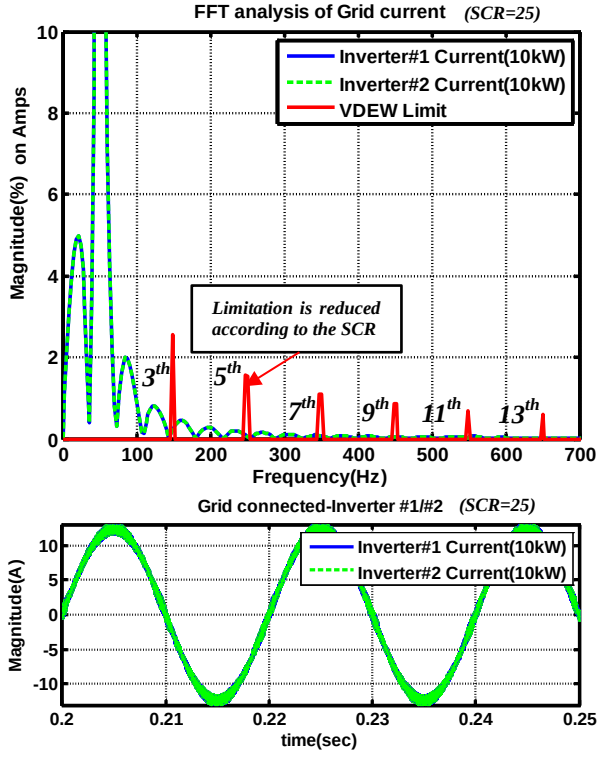


(b)

Fig. 5. FFT and time domain simulation waveform results of grid inductor side current of two identical inverter
(a) SCR = 100 (K_p=1 pu,Ki=1 pu(h=3,5,7),Ki=0.5 pu(h=11,13)
(b) SCR = 40(K_p=1 pu,Ki=1 pu(h=3,5,7),Ki=0.5 pu(h=11,13)



(a)



(b)

Fig. 6. FFT and time domain simulation waveform results of grid inductor side current of two identical inverter
(a) SCR = 25 (K_p=1 pu,Ki=1 pu(h=3,5,7),Ki=0.5 pu(h=11,13)
(b) SCR = 25 (K_p=K_{prev},Ki=1 pu(h=3,5,7),Ki=0.5 pu(h=11,13)

V. Conclusion

This paper has modeled the single grid connected inverter and the n-parallel connected inverter considering grid impedance variations. All models are analyzed based on the impedance basis analysis methods. Also, the low-order harmonic compensation error is analyzed under the various grid conditions, the relationship between the analyzed converter impedance and grid impedance is assessed by means of impedance based analysis method. Besides, a gain design method, which can improve the harmonic compensation error and harmonic instability, is proposed. Finally, the results including various grid conditions are proved by the simulation in order to verify theoretical approaches.

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