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MAF-PLL With Phase-Lead Compensator

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***Abstract*—A basic approach to improve the filtering capability of a standard phase-locked loop (PLL) is to incorporate a moving average filter (MAF) into its control loop. This improvement, however, is at the cost of a slow transient response for the PLL, which is undesirable in most applications. It is shown in this paper that this problem can be alleviated by adding a phase-lead compensator in the MAF-PLL control loop. The effectiveness of suggested approach is confirmed through numerical results.**

***Index Terms*—Moving average filter (MAF), phase-lead compensator, phase-locked loop (PLL), synchronization.**

I. Introduction

Phase-locked loop (PLL) is a closed-loop feedback control system that is used in variety of applications, particularly for synchronization and control of power-electronic based devices [1]-[3]. In recent years, with proliferation of new grid-connected equipment and growing interest towards generation of power based on renewable energies such as wind and solar, the importance of PLLs has increased [4].

To improve the filtering capability of a standard PLL under adverse grid conditions, different approaches have been proposed. A basic method is to include a moving average filter (MAF) into its control loop. Using the in-loop MAF, however, causes a considerable phase delay in the PLL control and, therefore, slows down its transient response. To deal with this challenge, using a quasi-type-1 PLL structure [5], and removing the in-loop MAF(s) and place them before the input of the PLL [6] have been proposed.

To improve the dynamic response of the standard MAF-PLL, including a phase-lead compensator, whose frequency response is almost inverse of that of the MAF, in the MAF-PLL control loop is suggested in this paper. The effectiveness of suggested approach is confirmed through numerical results.

II. Standard MAF-PLL

Fig. 1 shows the structure of standard MAF-PLL, which consists of a conventional synchronous reference frame PLL (SRF-PLL) with two MAFs. The MAF is a linear phase filter that is described in the continuous and discrete domains as

$$G_{\mathrm{MAF}}(s) = \frac{1 - e^{-T_w s}}{T_w s} \tag{1}$$

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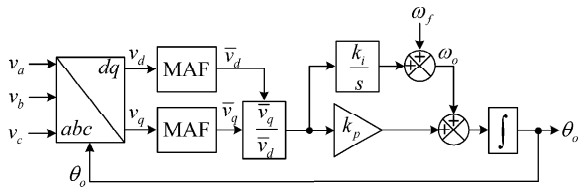

Fig. 1. Standard MAF-PLL.

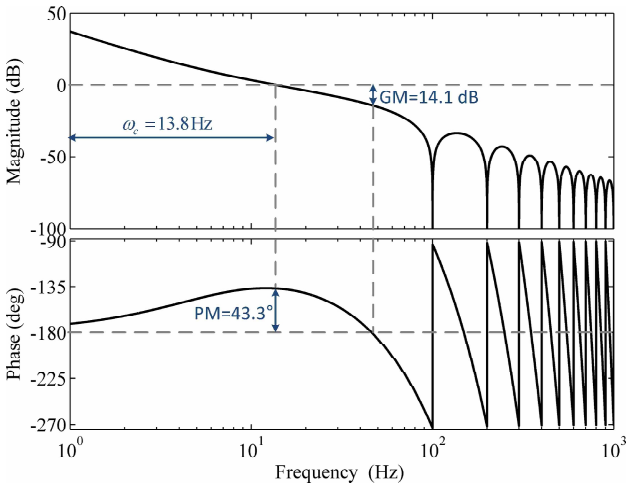

Fig. 2. Bode plot of the open-loop transfer function of the standard MAF-PLL. Parameters: $T_w = 0.01$ s, $k_p = 83.33$, and $k_i = 2893.5$.

$$G_{\mathrm{MAF}}(z) = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}} \tag{2}$$

where T_w is the MAF window length, and N is the number of samples within the window length of the MAF.

The MAF enables the PLL to effectively block the grid disturbances, but at the cost of slowing down its transient response. For example, Fig. 2 shows the open-loop Bode plot of the standard MAF-PLL. In obtaining plot, the MAF window length is set to the half of the fundamental period, i.e., $T_w = T/2 = 0.01$ s, to block the even order harmonic components in the PLL control loop (which are corresponding to the odd order harmonic components in the PLL input), and the proportional and integral gains are selected using the symmetrical optimum method to provide a phase margin of around $45°$ for the MAF-PLL [7]. From Fig. 2, it can be observed that the crossover frequency of the MAF-PLL is rather low, which implies the PLL suffers from a slow transient response.

III. Phase-Lead Compensator

To effectively compensate the phase delay caused by the MAF, the frequency response of the phase-lead compensator

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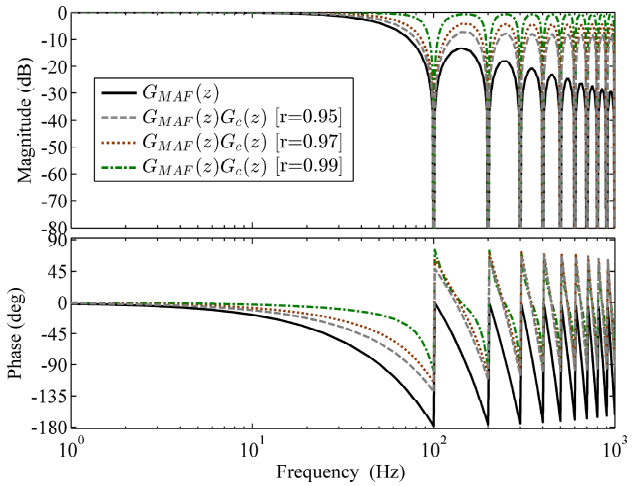

Fig. 3. Frequency response of the MAF (solid line), and the cascade connection of MAF and phase-lead compensator for three different values of r: $r = 0.95$ (dashed line), $r = 0.97$ (dotted line), and $r = 0.99$ (dashed-dot line).

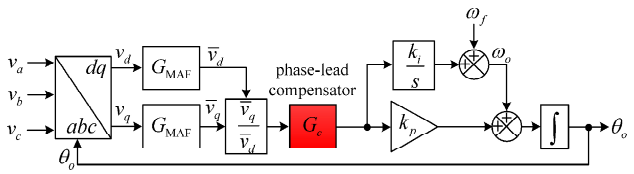

Fig. 4. Schematic diagram of the MAF-PLL with the phase-lead compensator

should be almost inverse of that of the MAF. Equation (3) describes such compensator [8]

$$G_c(z) = k\frac{1 - rz^{-1}}{1 - r^N z^{-N}} \tag{3}$$

in which $r \in [0 \quad 1)$ is called the attenuation factor, N, as defined before, is the number of samples within the MAF window length, and $k = (1 - r^N)/(1 - r)$ is a simple gain that normalizes the dc gain of compensator.

Fig. 3 shows the frequency response of the MAF (solid line) and the cascade connection of MAF and phase-lead compensator for three different values of r: $r = 0.95$ (dashed line), $r = 0.97$ (dotted line), and $r = 0.99$ (dashed-dot line). It can be observed that the phase-lead compensator can effectively compensate the phase delay caused by the MAF by selecting r very close to unity. In this paper, $r = 0.99$ is selected.

IV. MAF-PLL With Phase-Lead Compensator

Fig. 4 shows the structure of MAF-PLL with phase-lead compensator, in which the compensator is included between the MAF and PI controller. From Fig. 4, the small-signal model of this PLL can be simply obtained as shown in Fig. 5, in which Δ denotes perturbation around the nominal operating points. According to this model, the open-loop transfer function can be obtained as

$$G_{ol}(s) = \underline{G_{\text{MAF}}(s)G_c(s)}\frac{k_p s + k_i}{s^2}. \tag{4}$$

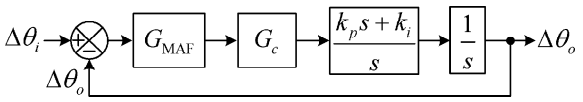

Fig. 5. Small-signal model.

TABLE I
PLLs CONTROL PARAMETERS

	proposed PLL	SRF-PLL	MAF-PLL
MAF window length, T_w	0.01 s	0.01 s	0.01 s
Proportional gain, k_p	177.71	177.71	83.33
Integral gain, k_i	15791	15791	2893.5
Attenuation factor, r	0.99	—	—

From Fig. 3, it can be observed that the cascade connection of the MAF and phase-lead compensator provides a close gain to unity (0 dB) with a near zero phase shift at low frequency range (frequencies lower than the first notch frequency). Therefore, the underlined term in (4) can be neglected, and (4) can be approximated by

$$G_{ol}(s) \approx \frac{k_p s + k_i}{s^2}. \tag{5}$$

Using (5), the closed loop transfer function of the PLL can be obtained as

$$G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)} \approx \frac{k_p s + k_i}{s^2 + \underbrace{k_p}_{2\zeta\omega_n} s + \underbrace{k_i}_{\omega_n^2}} \tag{6}$$

where ζ is the damping factor, and ω_n is the natural frequency. To achieve the best damping $\zeta = 1/\sqrt{2}$, and to obtain a fast transient response $\omega_n = 2\pi 20$ rad/s is selected. These selections give the proportional and integral gains as $k_p = 2\zeta\omega_n = 177.71$, and $k_i = \omega_n^2 = 15791$.

V. Simulation Results

In this section, the effectiveness of suggested PLL structure is confirmed through simulation results. Simulations are carried out in MATLAB/Simulink environment. Throughout the simulation studies, the sampling frequency is fixed at 10 kHz, and the nominal frequency is set to 50 Hz.

To further highlight the effectiveness of the proposed PLL structure, the conventional SRF-PLL and the standard MAF-PLL are also implemented and compared with the proposed PLL structure. In designing the control parameters of the SRF-PLL, an optimum damping factor $\zeta = 1/\sqrt{2}$ and the same bandwidth as that of the proposed PLL structure is considered. The SRF-PLL also uses an MAF in its d-axis to provide an estimation of grid voltage amplitude for amplitude normalization purpose. Designing the control parameters of the standard MAF-PLL, as mentioned before, is carried out using the symmetrical optimum method. Table I summarizes the control parameters of all PLLs, and Fig. 6 shows their open-loop Bode plots.

Fig. 7 and 8 show the simulation results when the grid voltage undergoes a phase angle jump of $+20^\circ$ and frequency step change of $+3$ Hz, respectively. It can be observed that the dynamic response of proposed PLL is as good as that achieved

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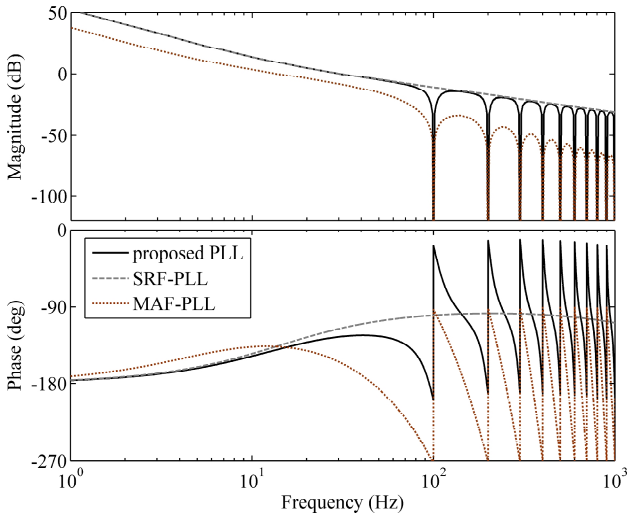

Fig. 6. Open-loop Bode plots of PLLs.

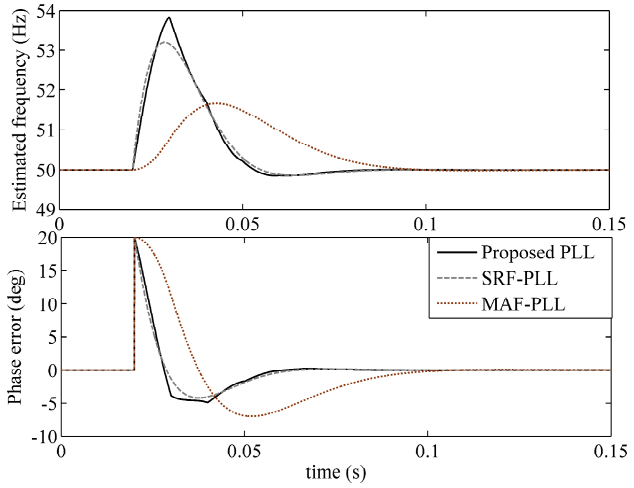

Fig. 7. Simulation results when the grid voltage undergoes a phase angle jump of $+20^{\circ}$.

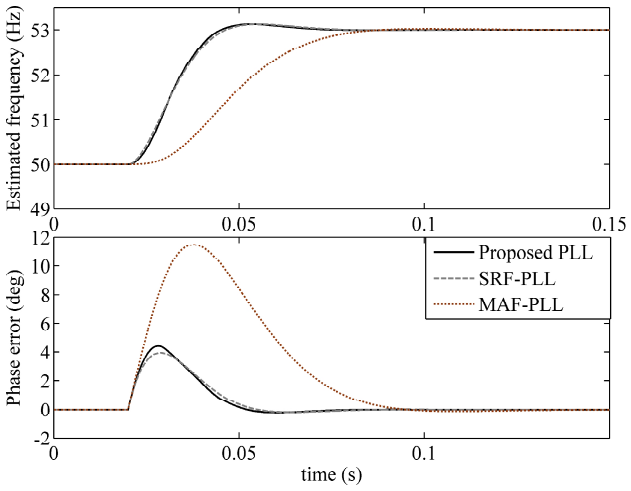

Fig. 8. Simulation results when the grid voltage undergoes a frequency step change of $+3$ Hz.

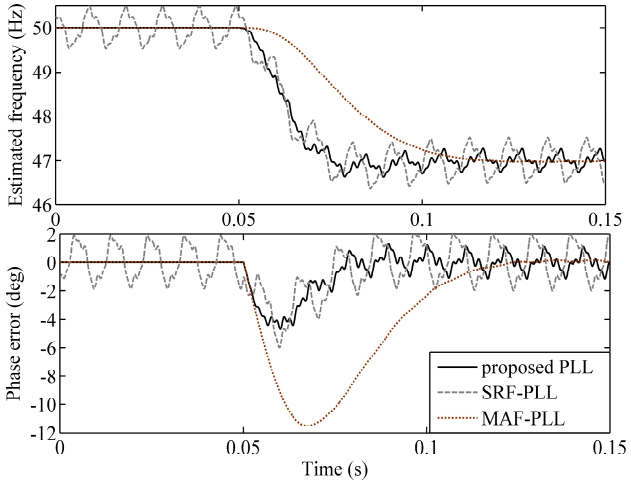

Fig. 9. Simulation results under distorted and unbalanced grid condition.

by the SRF-PLL. The MAF-PLL, however, suffers from a slow transient response. See table II for details.

Fig. 9 shows the simulation results under distorted and unbalanced grid condition. The parameters of grid voltage in this test are summarized in Table III. To analyze the effect of grid frequency variations on the filtering capability of PLLs, a step change of -3 Hz in the grid frequency is also programmed in this test. The detailed results can be found in Table II. It can be observed that, regardless of the value of the grid frequency, the standard MAF-PLL represents an excellent filtering capability, and the SRF-PLL shows a poor filtering capability. The filtering capability of the proposed PLL is the same as that of MAF-PLL when the grid frequency is at its nominal value, however it tends to worsen with increasing the deviation of grid frequency from its nominal value. Anyway, the grid frequency changes in a very limited range around its nominal value in most applications; however, for those applications where drastic change of frequency is expected, the filtering capability of the proposed PLL can be simply improved by adapting MAFs and phase-lead compensator to the grid frequency variations using one of the following ways: 1) feeding back the frequency estimated by the PLL to these units; and 2) using a variable sampling frequency [9]. It should be mentioned that the application of second method may not be always possible, as the PLL is often a small part of a more complex system that its restrictions may not allow using a variable sampling frequency [7], [10].

The simulation results shown in Fig. 10 compare the performance of the proposed PLL, SRF-PLL, and MAF-PLL for different levels of voltage sags at phase A of the grid voltage. The amplitudes of phase B and C are fixed at 1 pu during this test. Similar to the previous test, the MAF-PLL yields a very good performance regardless of the value of the grid frequency, while the SRF-PLL exhibits a very poor performance. The performance of the proposed PLL is quite good when the grid frequency is close to its nominal value, however its performance may not be acceptable in the

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TABLE II
SUMMARY OF RESULTS

	proposed PLL	**SRF-PLL**	**MAF-PLL**
+20° phase-angle jump			
2% settling time	35.9 ms (1.79 cycles)	38.8 ms (1.94 cycles)	73.7 ms (3.68 cycles)
phase overshoot	4.89° (24.45%)	4.2° (21%)	7.05° (35.25%)
peak frequency error	3.83 Hz	3.2 Hz	1.68 Hz
+3 Hz frequency step change			
2% settling time	44.3 ms (2.21 cycles)	47.3 ms (2.36 cycles)	59.2 ms (2.96 cycles)
frequency overshoot	0.13 Hz (4.33%)	0.13 Hz (4.33%)	0.03 Hz (1%)
peak phase error	4.42°	3.94°	11.41°
Distorted and unbalanced Grid			
peak-to-peak phase error (freq.=50 Hz)	0°	3.78°	0°
peak-to-peak phase error (freq.=47 Hz)	2.24°	4.04°	0.1°
Phase margin (PM)	55°	64.8°	43.3°

TABLE III
PARAMETERS OF DISTORTED INPUT VOLTAGE

Voltage component	**Amplitude** (p.u.)
Fundamental positive sequence	1
Fundamental negative sequence	0.1
5^{th} harmonic negative sequence	0.05
7^{th} harmonic positive sequence	0.05
11^{th} harmonic negative sequence	0.05
13^{th} harmonic positive sequence	0.05

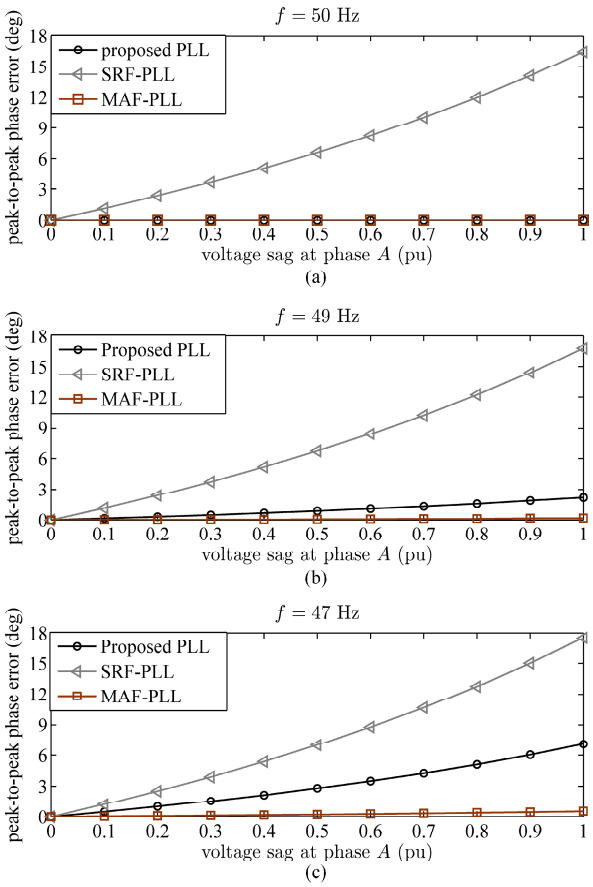

Fig. 10. Simulation results under asymmetrical voltage sag. During this test, the amplitude of phase B and C are kept at 1 pu. (a) $f = 50$ Hz; (b) $f = 49$ Hz; and (c) $f = 47$ Hz.

presence of large variations in the grid frequency and severe voltage sags. In such scenarios, as mentioned before, the PLL performance can be improved by adapting the MAFs and phase lead compensator to the grid frequency variations.

The last line in Table II compares the phase margin (PM) of all PLLs. The PM of the proposed PLL is higher than that of MAF-PLL, and lower than that of SRF-PLL.

VI. CONCLUSION

In this paper, it was shown that the dynamic response of the standard MAF-PLL can be improved by including a phase-lead compensator in its control loop. The effectiveness of proposed PLL structure was confirmed through numerical results and comparison with the standard MAF-PLL and the conventional SRF-PLL.

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