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Efficiency Analysis on a Two-level Three-Phase Quasi-Soft-Switching Inverter

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***Abstract*—When designing an inverter, an engineer often needs to select and predict the efficiency beforehand. For the standard inverters, plenty of researches are analyzing the power losses and also many software tools are being used for efficiency calculation. In this paper, the efficiency calculation for non-conventional inverters with special shoot-through state is introduced and illustrated through the analysis on a special two-level three-phase quasi-soft-switching inverter. Efficiency comparison between the classical two-stage two-level three-phase inverter and the two-level three-phase quasi-soft-switching inverter is carried out. A 10 kW/380 V prototype is constructed to verify the analysis. The experimental results show that the efficiency of the new inverter is higher than that of the traditional two-stage two- level three-phase inverter.**

***Keywords*- Efficiency, shoot-through, reverse recovery, quasi-soft switching, ZVS.**

I. INTRODUCTION

Recently, the solar photovoltaic and other regenerative power systems have attracted much attention due to the renewable character [1] [2]. The DC output voltage for these regenerative power systems may vary greatly, for example, from 300V to 800V for a PV panel system under the different temperature conditions [3]. A traditional two-stage two-level three-phase inverter with a boost DC/DC converter as shown in Fig. 1 (named as Topology A) has been widely applied in the industry due to its simple structure and high reliability [4]. The power losses of this inverter depend much on the performance of the devices. High efficiency can be achieved by using full silicon carbide or gallium nitride devices, but it results in the high cost.

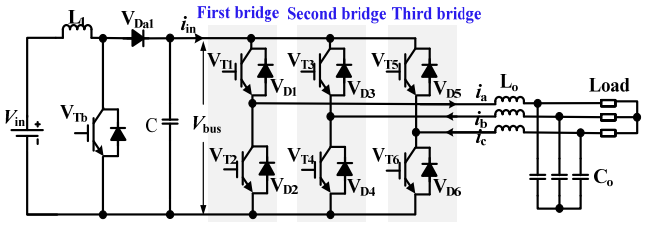


Fig. 1. A traditional two-stage two-level three-phase inverter (Topology A).

Combined with the characters of the voltage source inverter and the current source inverter, the Z-Source Inverter (ZSI) was proposed [5]. Since the number of the power semiconductors has been saved and the ZSI has the outstanding character of immunity to the electromagnetic interference, theoretically, the reliability of the ZSI may be higher than other two stage power inverters. However, the efficiency of this type inverter is still for discussion, e.g., [6] and [7] showed that the efficiency of the ZSI was not as high as the traditional two stage two-level three-phase inverter, but [8] showed that the efficiency of the Quasi-ZSI was high. For the standard inverters, many papers analyze the efficiency in detail [9], [10]. However, till now, few documents have provided the formulations in predicting the efficiency of the inverter with special shoot-through state in detail.

For the two-stage inverter as shown in Fig. 1, the power loss caused by the reverse recovery of the diodes (e.g. the diode V_{Da1} of Boost DC-DC stage) is high, if the silicon diode is used [9]. In order to achieve a good efficiency with low cost, a two-level three-phase quasi-soft-switching inverter was proposed [11], which is based on the traditional inverter with an extra auxiliary circuit composed of a small inductor, a diode and a switch as shown in Fig. 2 (named as Topology B). With proper control scheme, the inverter can alternate between the voltage source inverter and the current source inverter to reduce the reverse recovery power losses of both two power stages and so that achieve more soft- and quasi-soft switching transitions. Furthermore, unlike other traditional resonant soft-switching inverters, the soft- and quasi-switching states are independent of the variation of the parameters.

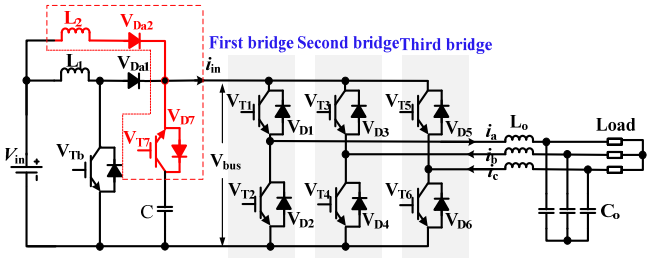


Fig. 2. A two-level three-phase quasi-soft-switching inverter (Topology B) [11].

This paper focuses on the efficiency analysis of this special two-level three-phase quasi-soft-switching inverter. A guideline for the efficiency calculation for this inverter with special shoot-through state is presented in detail. Power loss calculation of the traditional two stage inverter is introduced with the Space Vector Pulse Width Modulation (SVPWM) first. Then, the shoot-through state of the special inverter is considered and its effect on the power loss is analyzed. Last, the calculated efficiency and the power loss distributions of the two topologies are given. Experiments on a 10 kW prototype are carried out to verify the calculations done.

II. Efficiency Analysis of Traditional Inverter

During the calculations, the characters of all switches are assumed to be the same, the switching frequency f_s of all switches is the same and the switching time is T_s which is equal to $1/f_s$.

A. Power losses in the boost power stage

As shown in Fig. 1, the first power stage of Topology A is composed of a DC/DC boost converter.

1) Conduction power losses of Diode V_{Da1} *and IGBT* V_{Tb}

The current of inductor L_1 flows through V_{Tb} when V_{Tb} is on and freewheels through V_{Da1} while V_{Tb} is off. The conduction power loss of V_{Da1} and V_{Tb} can be calculated as,

$$P_{d\_con1} = V_F \cdot I_{L1} \cdot (1 - D_b) \tag{1}$$

$$P_{igbt\_con1} = V_{CEsat} \cdot I_{L1} \cdot D_b \tag{2}$$

where D_b is the duty cycle of V_{Tb}, V_F is the average forward voltage drop of V_{Da1}, V_{CEsat} is the collector-emitter saturation voltage drop of V_{Tb}, and I_{L1} is the average current of inductor L_1. V_F and V_{CEsat} are related to the junction temperature and the forward conduction current of diode and IGBT.

2) Power losses caused by the reverse recovery of Diode V_{Da1}

When the diode transits from the conduction state to the blocking state, the stored charge needs to be discharged. If the diode suffers the reverse voltage, it will cause reverse recovery power loss which is related to the collector-emitter voltage drop, the forward current, the junction temperature and the driving characteristics. The reverse recovery power loss of V_{Da1} can be calculated as

$$P_{rec1} = E_{rr} \cdot f_s \tag{3}$$

where E_{rr} is the reverse recovery energy loss per switching.

3) Power losses caused by turn-on and turn-off of IGBT V_{Tb}

The turn-on/off power loss of V_{Tb} can be calculated as,

$$P_{turn\_on1} = E_{on} \cdot f_s \tag{4}$$

$$P_{turn\_off1} = E_{off} \cdot f_s \tag{5}$$

where E_{on} and E_{off} are the turn-on and the turn-off energy loss per switching.

E_{rr}, E_{on} and E_{off} can be gotten from the datasheet of the module. They are different with the current, the voltage of the DC bus and the characters of the driver. In order to get a more accurate calculation result, the data fitting should be carried out.

4) Power losses caused by the choke L_1

The power loss of the filter choke L_1 is composed of the core power loss and the conducting power loss of the coil. The detailed power loss calculation will not be discussed in this paper but the calculation method in [12] is used.

B. Power losses in the second power stage

As shown in Fig. 1, the second power stage is just a two-level three-phase half bridge inverter. Power loss of the inverter depends on the modulation method and the power factor of the load current [10], when the other parameters and conditions are set. In this paper, the SVPWM scheme is adopted and the power factor is assumed to be unity. The distribution of the voltage vector states is shown in Fig. 3. The power losses in sector 1 is used to predict the total power losses, assuming that the output currents (shown in Fig.2) of i_a, i_b and i_c are $\sqrt{2}I_o\cos(\theta)$, $\sqrt{2}I_o\cos(\theta-120^o)$ and $\sqrt{2}I_o\cos(\theta+120^o)$ respectively.

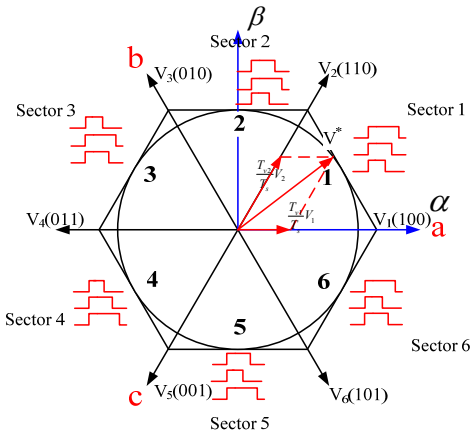


Fig. 3. Voltage vector states distribution.

The duty cycles of the upper switches (V_{T1}, V_{T3} and V_{T5} as shown in Fig. 1) can be derived as,

$$\begin{cases} D_1(\theta) = \dfrac{V_{bus} + \sqrt{3}V_m\left(\sin(\frac{\pi}{3}-\theta)+\sin\theta\right)}{2V_{bus}} \\ D_2(\theta) = \dfrac{V_{bus} - \sqrt{3}V_m\left(\sin(\frac{\pi}{3}-\theta)-\sin\theta\right)}{2V_{bus}} \\ D_3(\theta) = \dfrac{V_{bus} - \sqrt{3}V_m\left(\sin(\frac{\pi}{3}-\theta)+\sin\theta\right)}{2V_{bus}} \end{cases} \tag{6}$$

where V_m is the amplitude value of phase voltage and θ is the sampling angle.

1) Conduction power losses of Diode and IGBT

Since the output current is sinusoidal, the conduction power losses should be calculated by integrating the

instantaneous value of the current and the voltage. The total conduction power losses of the diodes of the second power stage, P_{d_con}, can be calculated as,

$$\begin{cases} P_{d\_con2\_1}=\frac{3}{\pi}\cdot\int_0^{\frac{\pi}{3}}V_F\cdot\sqrt{2}I_o\cos(\theta)\cdot(1-D_1(\theta))d\theta \\ P_{d\_con2\_2}=\frac{6}{\pi}\cdot\int_0^{\frac{\pi}{6}}V_F\cdot\sqrt{2}I_o\left|\cos(\theta-\frac{2\pi}{3})\right|\cdot D_2(\theta)d\theta \\ \quad +\frac{6}{\pi}\cdot\int_{\frac{\pi}{6}}^{\frac{\pi}{3}}V_F\cdot\sqrt{2}I_o\cos(\theta-\frac{2\pi}{3})\cdot(1-D_2(\theta))d\theta \\ P_{d\_con2\_3}=\frac{3}{\pi}\cdot\int_0^{\frac{\pi}{3}}V_F\cdot\sqrt{2}I_o\left|\cos(\theta+\frac{2\pi}{3})\right|\cdot D_3(\theta)d\theta \\ P_{d\_con2}=P_{d\_con2\_1}+P_{d\_con2\_2}+P_{d\_con2\_3} \end{cases} \quad (7)$$

where $P_{d\_con\_1}$, $P_{d\_con\_2}$ and $P_{d\_con\_3}$ are the conduction power losses of diodes of the first bridge, the second bridge and the third bridge as shown in Fig. 1 respectively.

In the similar way, the conduction power losses of IGBTs, P_{IGBT_con}, can be calculated as,

$$\begin{cases} P_{igbt\_con2\_1}=\frac{3}{\pi}\cdot\int_0^{\frac{\pi}{3}}V_{CEsat}\cdot\sqrt{2}I_o\cos(\theta)\cdot D_1(\theta)d\theta \\ P_{igbt\_con2\_2}=\frac{6}{\pi}\cdot\int_0^{\frac{\pi}{6}}V_{CEsat}\cdot\sqrt{2}I_o\left|\cos(\theta-\frac{2\pi}{3})\right|\cdot(1-D_2(\theta))d\theta \\ \quad +\frac{6}{\pi}\cdot\int_{\frac{\pi}{6}}^{\frac{\pi}{3}}V_{CEsat}\cdot\sqrt{2}I_o\cos(\theta-\frac{2\pi}{3})\cdot D_2(\theta)d\theta \\ P_{igbt\_con2\_3}=\frac{3}{\pi}\cdot\int_0^{\frac{\pi}{3}}V_{CEsat}\cdot\sqrt{2}I_o\left|\cos(\theta+\frac{2\pi}{3})\right|\cdot(1-D_3(\theta))d\theta \\ P_{igbt\_con2}=P_{igbt\_con2\_1}+P_{igbt\_con2\_2}+P_{igbt\_con2\_3} \end{cases} \quad (8).$$

where $P_{IGBT\_con\_1}$, $P_{IGBT\_con\_2}$ and $P_{IGBT\_con\_3}$ are the conduction power losses of IGBTs of the first bridge, the second bridge and the third bridge respectively.

2) Power losses caused by reverse recovery

Since one reverse recovery takes place for every bridge during one duty-cycle, the reverse recovery power losses of the second power stage, P_{rec_2}, can be calculated as,

$$P_{rec2}=3\cdot E_{rr}\cdot f_s \quad (9)$$

3) Switching Power losses caused by turn-on and turn-off

Similar, the switching power losses can be calculated as,

$$\begin{aligned} P_{turn\_on2}&=3\cdot E_{on}\cdot f_s \\ P_{turn\_off2}&=3\cdot E_{off}\cdot f_s \end{aligned} \quad (10).$$

4) Power losses caused by the choke L_o

Similarly, the power loss calculation method in [12] is used and not introduced in this paper.

III. Power Loss Difference between Topology B and Topology A

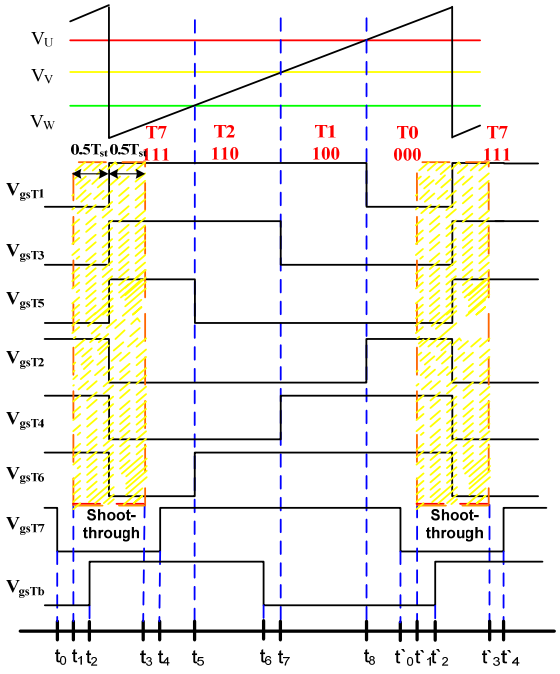


Fig. 4. Operating sequence of Topology B.

Fig. 4 shows the basic operating sequence of Topology B, where V_{gsTX} is the drive signal of switch V_{T1}~V_{T7}, V_{Tb}. The detailed operation principle of the special two-level three-phase quasi-soft-switching inverter was introduced in [11]. Here, the character of Topology B is summarized in the followings,

Topology B has a special shoot-through state. The shoot-through time, T_{st}, is the time when V_{T1}~V_{T6} all are on. The shoot-through time begins after the auxiliary switch, V_{T7}, turns off, ensuring that V_{T1}, V_{T3}, V_{T5} turn on in the quasi Zero Current State (ZCS) , and ends before V_{T7} turns on, ensuring that V_{T7} turns on in the Zero Voltage State (ZVS). T_{st} is divided into two parts as shown in Fig. 4.

V_{T7} turns on and turns off in the ZVS. V_{Tb} turns on in the ZVS. V_{Da1} recovers in the ZVS.

As shown in Fig. 4, the time period between t_1 and t_2 is assumed to be small and do not affect the efficiency calculations.

The power loss calculation is similar to Topology A. In this paper, the power loss difference between Topology B and Topology A is highlighted.

A. Power loss difference in the first power stage

1) Less power losses

Compared with the power losses of Topology A, the main power loss difference in the first power stage is that the reverse recovery power losses of V_{Da1} and the turn-off power loss of V_{Tb} are eliminated, and which have been calculated in (3) and (5).

2) Added power losses

The auxiliary circuit will introduce the extra conduction power losses of V_{DA2}, V_{D7} and V_{T7}.

a) Conduction power loss of Diode V_{Da2}

The conduction power loss of V_{Da2} can be calculated as,

$$P_{\text{d\_con1\_added\_1}} = V_F \cdot I_{L_2} \cdot \frac{T_{st} + T_{fr}}{T_s} \tag{11}$$

where I_{L2} is the average current of L_2 during the shoot-through state and the discharging of L_2, T_{st} is the shoot-through time, and T_{fr} is the discharging time of L_2, which can be calculated with T_{st}, L_2, V_{in} and the voltage across the DC capacitor.

b) Conduction power loss of Diode V_{D7}

The total conduction losses of V_{D7} can be calculated as

$$P_{\text{d\_con1\_added\_2}} = V_F . I_{V_{D7}} \tag{12}$$

where I_{Vd7} is the average currents charging the DC capacitor through V_{D7}.

c) Conduction power loss of IGBT V_{T7}

Similarly, the conduction power loss of V_{T7} caused by the current discharging the capacitor can be calculated as,

$$P_{\text{igbt\_con1\_added}} = V_{V_{CEsat}} . I_{V_{T7}} \tag{13}$$

where I_{VT7} is the average current discharging the DC capacitor following through the V_{T7}.

Note that (12) and (13) are simplified expressions. The detailed formulations for calculating the average values of the currents charging and discharging the DC capacitor are quite complicated. In the real application, the simulated values may be suggested to be used directly.

B. Power loss differnce in the second power stage

1) Less power losses

During the shoot-through time, since V_{T7} is off, the switches of V_{T1}, V_{T3} and V_{T5} will turn on in the quasi-soft-switching period. The related reverse recovery power losses saved can be calculated as,

$$\begin{cases} P_{rec2\_1} = \dfrac{3}{\pi} \cdot \int_0^{\pi/3} k \cdot E_{rr} \cdot f_s d\theta \\ P_{rec2\_2} = \dfrac{6}{\pi} \cdot \int_{\pi/6}^{\pi/3} k \cdot E_{rr} \cdot f_s d\theta \\ P_{rec2\_3} = 0 \\ P_{\text{rec2\_saved}} = P_{rec2\_1} + P_{rec2\_2} + P_{rec2\_3} \end{cases} \tag{14}$$

where k is the parameter, describing the extent of that soft-switching can be achieved.

The related turn-on power losses saved can be calculated as

$$P_{\text{turn\_on2\_saved}} = 1.5 \cdot k \cdot E_{on} \cdot f_s \tag{15}.$$

According to [13], a 3.6 μH inductor in the power loop can save 85% of the turn-on power losses.

2) Added power losses

Compared with Topology A, the additonal power losses in the second power stage of Topology B are the conduction losses due to the shoot-through operation.

Assuming that during the shoot-through operation, the current of L_2 is divided equally by the three bridge and the output current of each phase is halved by the two switches of each bridge. The current of L_2 can be calculated as,

$$i_{L_2}(t) = \frac{V_{in}}{L_2} \cdot t \qquad (0 \le t \le T_{\text{st}}) \tag{16}$$

a) In the first bridge

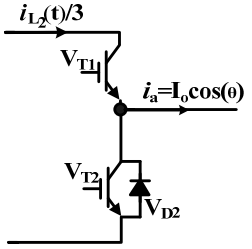


Fig. 5. Currents in the first bridge during the shoot-through in the sector 1.

Fig. 5 shows the currents of the first bridge during the shoot-though in sector 1. If the one third of the peak current of L_2 is larger than the half of the peak value of the output current, compared to Topology A, the additional conduction power losses of diode and IGBT can be calculated as followings,

$$\begin{aligned} P_{\text{d\_con2\_1\_added}} = {} & \frac{3}{\pi} \cdot \int_0^{\pi/3} V_F \cdot \frac{1}{T_S} \int_0^{T_2} \left[\frac{1}{2} I_o \cos(\theta) - \frac{1}{3} i_{L2}(t) \right] dt d\theta \\ & - \frac{3}{\pi} \cdot \int_0^{\pi/3} V_F \cdot I_o \cos(\theta) \cdot \frac{0.5 T_{st}}{T_S} d\theta \end{aligned} \tag{17}$$

$$\begin{aligned} P_{\text{igbt\_con2\_1\_added}} = {} & \frac{3}{\pi} \cdot \int_0^{\pi/3} V_{CEsat} \cdot \frac{1}{T_S} \int_{T_1}^{T_{st}} \left(\left[\frac{1}{3} i_{L2}(t) - \frac{1}{2} I_o \cos(\theta) \right] dt d\theta \right. \\ & + \frac{3}{\pi} \cdot \int_0^{\pi/3} V_{CEsat} \cdot \left[\frac{1}{3} I_{L2} + \frac{1}{2} I_o \cos(\theta) \right] \cdot \frac{T_{st}}{T_S} d\theta \\ & - \frac{3}{\pi} \cdot \int_0^{\pi/3} V_{CEsat} \cdot I_o \cos(\theta) \cdot \frac{0.5 T_{st}}{T_S} d\theta \end{aligned} \tag{18}$$

where i_{L2}(t) is the current of L_2 during the shoot-through. T_1 is the time when the one third current of L_2 is equal to the half of load current, $0.5 I_o \cos(\theta)$. T_1 can be calculated as,

$$T_1 = \frac{1/2 \cdot I_o \cos(\theta)}{1/3 \cdot V_{in} / L_2} \qquad 0 \le T_1 \le T_{st} \tag{19}.$$

If one third of the peak current of L_2 is smaller than half of the peak value of the output current, the formulations for calculating the power losses of diode and IGBT are quite complicated, due to that more considerations should be taken. In this paper, the calculations are based on that one third of the peak current of L_2 is higher than half of the peak value of the output current.

b) In the second bridge

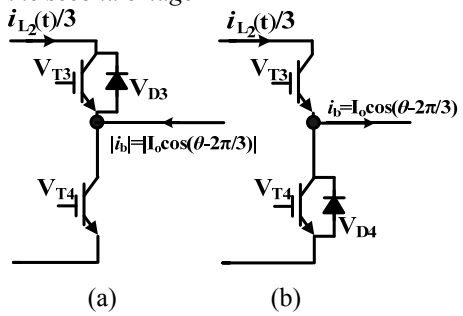


Fig. 6. Currents in the second bridge during the shoot-through in sector 1 (a) 0<θ<π/6, (b) π/6<θ<π/3.

Fig. 6 shows the currents of the first bridge during the shoot-though in sector 1. During 0<θ<π/6, the output current is negative and during π/6<θ<π/3, it is positive as shown in Fig. 6 (a) and Fig. 6 (b) respectively. During the shoot-through, the power loss difference in the second bridge can be calculated as (20) and (21) respectively,

$$P_{\text{d\_con2\_\_2\_added}}=\frac{3}{\pi}\cdot\int_0^{\pi/3}V_F\cdot\frac{1}{T_S}\int_0^{T_2}\left[\frac{1}{2}|I_o\cos(\theta-2\pi/3)|-\frac{1}{3}i_{L2}(t)\right]dtd\theta$$
$$-\frac{3}{\pi}\cdot\int_0^{\pi/3}V_F\cdot|I_o\cos(\theta-2\pi/3)|\cdot\frac{0.5T_{st}}{T_S}d\theta \quad (20)$$

$$P_{\text{igbt\_con2\_2\_added}}=\frac{3}{\pi}\cdot\int_0^{\pi/3}V_{CEsat}\cdot\frac{1}{T_S}\int_{T_2}^{T_{st}}\left(\left[\frac{1}{3}i_{L2}(t)-\frac{1}{2}|I_o\cos(\theta-2\pi/3)|\right]dtd\theta\right.$$
$$+\frac{3}{\pi}\cdot\int_0^{\pi/3}V_{CEsat}\cdot\left[\frac{1}{3}I_{L2}+\frac{1}{2}|I_o\cos(\theta-2\pi/3)|\right]\cdot\frac{T_{st}}{T_S}d\theta$$
$$-\frac{3}{\pi}\cdot\int_0^{\pi/3}V_{CEsat}\cdot|I_o\cos(\theta-2\pi/3)|\cdot\frac{0.5T_{st}}{T_S}d\theta \quad (21)$$

where T_2 is the time when one third of the current of L_2 is equal to the half of the load current, $0.5|I_o\cos(\theta-\pi/3)|$, which can be calculated as,

$$T_2=\frac{\frac{1}{2}\cdot|I_o\cos(\theta-2\pi/3)|}{\frac{1}{3}\cdot V_{in}/L_2}\qquad 0\le T_1\le T_{st} \quad (22)$$

c) In the third bridge

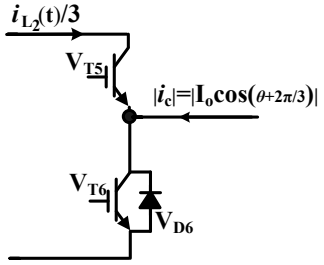


Fig. 7. Currents in the third bridge during the shoot-through in the sector 1.

Fig. 7 shows the currents of the third bridge during the shoot-through in sector 1. The output current of i_c is injected into the third bridge. During the shoot-through, the power loss difference in the third bridge can be calculated as (23) and (24) respectively,

$$P_{\text{d\_con2\_3\_added}}=\frac{3}{\pi}\cdot\int_0^{\pi/3}V_F\cdot\frac{1}{T_S}\int_0^{T_3}\left[\frac{1}{2}|I_o\cos(\theta+2\pi/3)|-\frac{1}{3}i_{L2}(t)\right]dtd\theta$$
$$-\frac{3}{\pi}\cdot\int_0^{\pi/3}V_F\cdot|I_o\cos(\theta+2\pi/3)|\cdot\frac{0.5T_{st}}{T_S}d\theta \quad (23)$$

$$P_{\text{igbt\_con2\_3\_added}}=\frac{3}{\pi}\cdot\int_0^{\pi/3}V_{CEsat}\cdot\frac{1}{T_S}\int_{T_3}^{T_{st}}\left(\left[\frac{1}{3}i_{L2}(t)-\frac{1}{2}|I_o\cos(\theta+2\pi/3)|\right]dtd\theta\right.$$
$$+\frac{3}{\pi}\cdot\int_0^{\pi/3}V_{CEsat}\cdot\left[\frac{1}{3}I_{L2}+\frac{1}{2}|I_o\cos(\theta+2\pi/3)|\right]\cdot\frac{T_{st}}{T_S}d\theta$$
$$-\frac{3}{\pi}\cdot\int_0^{\pi/3}V_{CEsat}\cdot|I_o\cos(\theta+2\pi/3)|\cdot\frac{0.5T_{st}}{T_S}d\theta \quad (24)$$

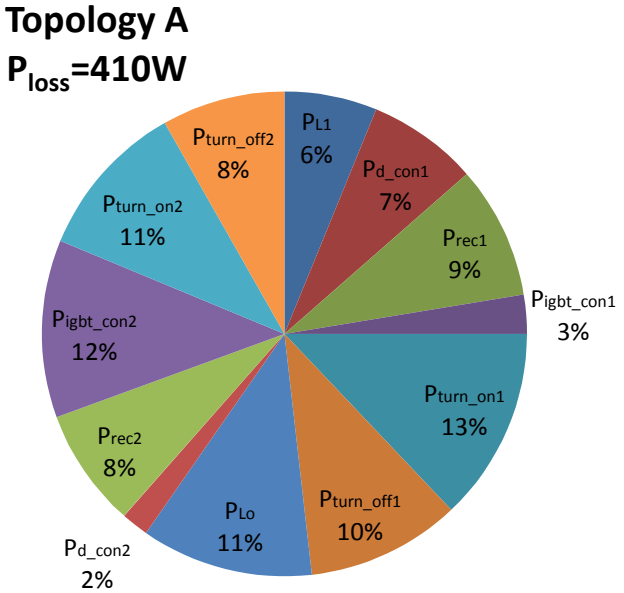
where the T_3 is the time when the one third current of L_2 is equal to the $0.5I_o|I_o\cos(\theta+\pi/3)|$, which can be calculated as,

$$T_3=\frac{\frac{1}{2}\cdot|I_o\cos(\theta+2\pi/3)|}{\frac{1}{3}\cdot V_{in}/L_2}\qquad 0\le T_1\le T_{st} \quad (25).$$

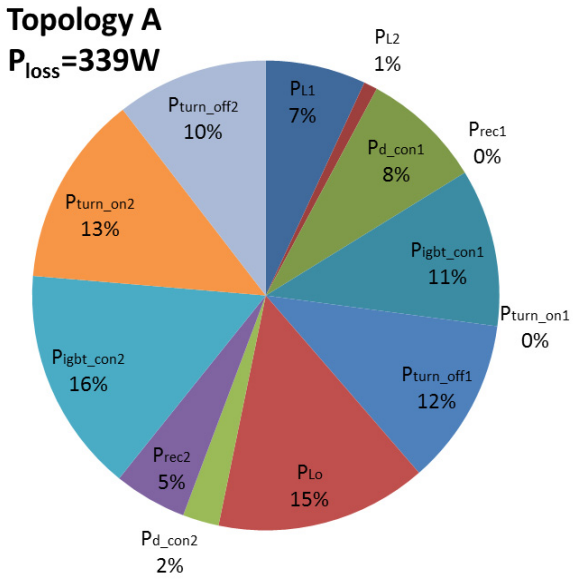
Base on the power loss calculation of Topology A, the total power losses of Topology B can be calculated with the expressions of (11)-(25).

IV. Calculated Losses and Experimental Validation

The power loss is calculated under the conditions that f_s = 15 kHz, L_1=1.2 mH, L_2=0.1 mH, L_o=1.6mH, C_o=10 μF, the phase to phase output AC voltage is 380V and the rated output power is 10 kW.



(a)



(b)

Fig. 8. Power loss distribution when V_{in}= 430 V and P_o = 10 kW, (a) of Topology A, (b) of Topology B.

Fig. 8 shows the calculated power losses of two topologies while the input DC voltage is 430 V and P_o is 10 kW (not including the power losses of control circuits). It can be seen that the total power losses of Topology B are 71W smaller than that of Topology A, mainly due to the improved reverse recovery power losses and the extra soft- and quasi-soft-switching states.

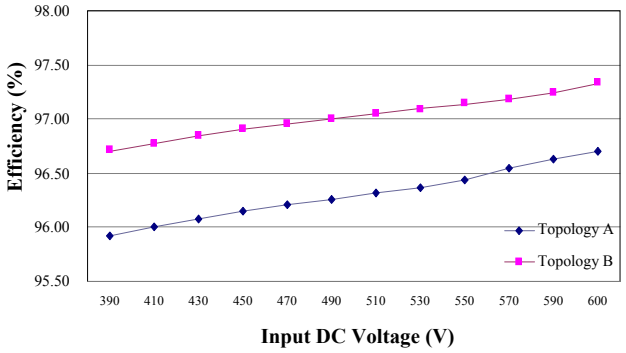


Fig. 9. Calculated Efficiency versus input DC voltage of Topology A and Topology B.

Fig. 9 shows the calculated efficiency versus the input voltage for both inverters under the condition of rated load. It can be seen that the higher input DC voltage, the higher efficiency, and the calculated efficiency of Topology B is about 0.6% higher than that of Topology A under the conditions that the modules of SKM50GB12T4 are adopted for main switches and V_{T7}.

In order to verify the theoretical analysis, a 10 kW prototype is constructed. The parameters are the same as those for the calculation. A DC source (Chroma 62120) provides the DC power and Yokogawa WT1600 is used to measure the efficiency. The photo of the prototype is shown in Fig. 10.

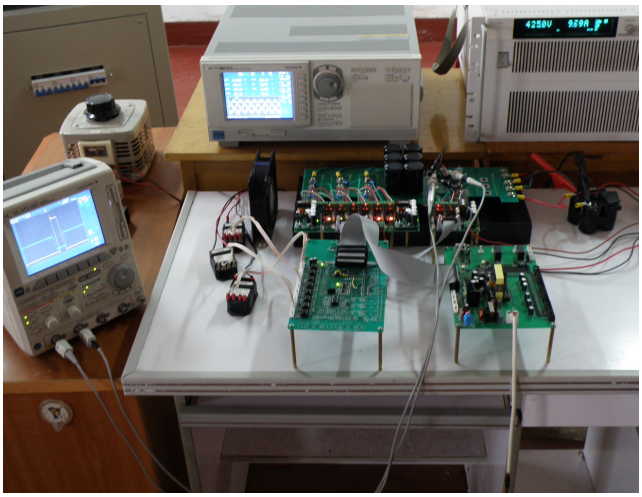


Fig. 10. Photo of a 10 kW experimental prototype.

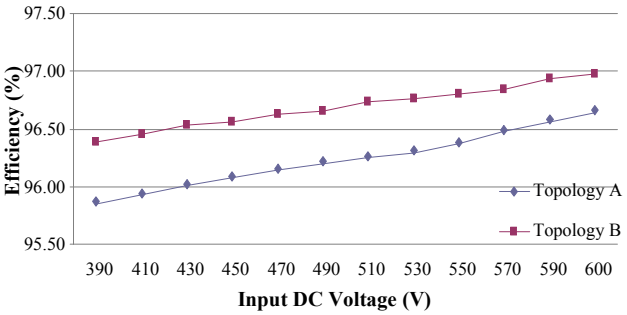


Fig. 11. Measured efficiency versus input DC voltage of Topology A and Topology B.

Fig. 11 shows the measured efficiency versus the input DC voltage for both inverters.

Comparing Fig. 9 with Fig. 11, one can see that the basic characteristic of the measured efficiency is much similar to the characteristic of the calculated efficiency. However, the measured efficiency of Topology B is lower than the calculated efficiency, mainly due to the reasons that since the data from the datasheet are not enough, only data for the junction temperature conditions of T_j = 25°C or 150°C can be obtained directly, and the deviation included the forward voltage drop of diode, the collector-emitter saturation voltage drop of IGBT and the reverse recovery power loss of diode may take place.

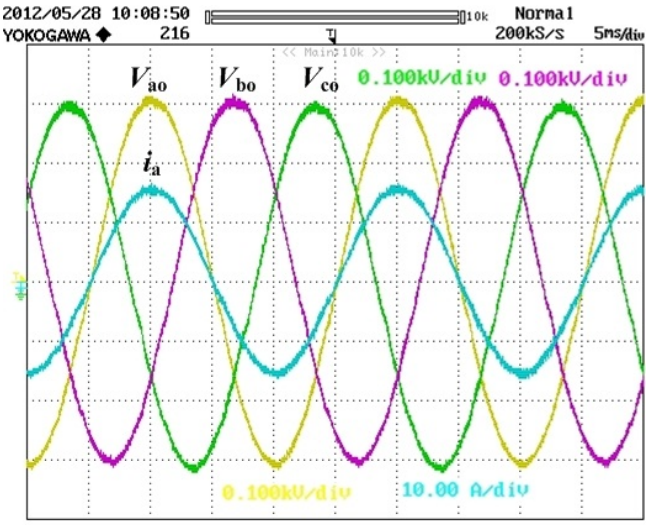


Fig. 12. Output voltages and current of i_a on the load of Topology B.

Fig. 13. Measured peak efficiency of Topology B when V_{in} = 417 V.

Fig. 12 shows the measured output voltages and current of Topology B. Fig. 13 shows that for the Topology B, the measured peak efficiency reaches to 97.1% when the input DC voltage is about 417 V and the output power is about 4 kW.

V. CONCLUSIONS

In this paper, an efficiency analysis method for the two-level three-phase quasi-soft-switching inverters with the special shoot-through state is introduced. An efficiency comparison between the traditional two-stage two-level three-phase inverter and the new inverter has been carried out. It can be seen that compared with the traditional inverter, the new inverter can improve the efficiency by about 0.6% in a wide range of input DC voltage.

A 10 kW experimental prototype has been designed and realized. The basic characteristic of the measured efficiency is much similar to the calculated efficiency. However, the measured efficiency of the new inverter is lower than the calculated efficiency, mainly due to the fact that the performance of the auxiliary switch is poor than expected.

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REFERENCES

[1] S.J. Chiang, H.J. Shieh and M.C. Chen, "Modeling and control of PV charger system with SEPIC converter," *IEEE Trans. on Ind. Electron.*,, vol. 56, no. 11, pp: 4344-4353, 2009.

[2] A. N. Ahmad and D. Rached, "Efficiency optimization of a dsp-based standalone PV system using fuzzy logic and dual-MPPT control," *IEEE Trans. on Ind. Informat.*, vol. 8, no. 3, pp: 573-584, 2012.

[3] J.M. Carrasco, L.G. Franquelo, J.T.Bialasiewicz, E. Galvan, R.C.P. Guisado, et al. "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey" *IEEE Trans. on Ind. Electron.*, vol. 53, no. 3, pp: 1002 - 1016, March. 2006.

[4] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewisz, E. Galvan, et al, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey *IEEE Trans. on Ind. Electron.*, vol. 53, no. 4, pp: 1002-1016, 2006.

[5] F. Z. Peng, "Z-source inverter," *IEEE Trans. on Ind. Applicat*., vol. 39, no. 2, pp: 504–510, Mar./Apr. 2003.

[6] R. Burkart, J. W. Kolar, G. Griepentrog , "Comprehensive Comparative Evaluation of Single- and Multi-Stage Three-Phase Power Converters for Photovoltaic Applications", *In proc. of INTELEC .2012*, Scottsdale, USA, September 30 - October 4, 2012.

[7] J. Li, J. Liu, Z. Liu, "Comparison of Z-source inverter and traditional two-stage boost-buck inverter in grid-tied renewable energy generation", *In Proc. of the IPEMC2009*, Wuhan, China,17-20 May 2009, pp: 1493 – 1497.

[8] Y. Zhou, L. Liu, H. Li, High Efficiency Cascaded Quasi-Z- Source Photovoltaic Inverter Module using eGaN FETs, *In Proc. of ECCE 2012*, Raleigh, North Carolina, Sept.15-20,2012, pp: 1615 – 1621.

[9] W. Wu, X.Wang, P. Geng, T. Tang, Efficiency analysis for three phase grid-tied PV inverter. *In Proc. of ICIT 2008*, Chengdu, China, April 21-24, 2008, pp: 1-5.

[10] Y. Wu, M.A. Shafi, A.M. Knight, R.A. McMahon, "Comparison of the Effects of Continuous and Discontinuous PWM Schemes on Power Losses of Voltage-Sourced Inverters for Induction Motor Drives," Power Electronics, *IEEE Trans. Power Electron.,* vol.26, no.1, pp: 182-191, Jan. 2011.

[11] W., P. Geng, J. Chen, et al, "A novel three-phase quasi-soft-switching DC/AC inverter", *In Proc. of PEDG2010*, HeFei, China, June 16-18, 2010, pp: 477-480.

[12] W. N. Mohan, T. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications, and Design. New York: Wiley, 2003.

[13] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, Application manual power semiconductors, SEMIKRON International, pp: 405, 2011, ISBN: 9783938843666.