Comparative Performance Evaluation of Orthogonal-Signal-Generators-Based Single-Phase PLL Algorithms

A Survey

Han, Yang; Luo, Mingyu; Zhao, Xin; Guerrero, Josep M.; Xu, Lin

Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2015.2466631

Publication date:
2016

Document Version
Accepted author manuscript, peer reviewed version

Comparative Performance Evaluation of Orthogonal-Signal-Generators based Single-Phase PLL Algorithms - A Survey

Yang Han, *Member, IEEE*, Mingyu Luo, Xin Zhao, Josep M. Guerrero, *Fellow, IEEE*, and Lin Xu

***Abstract*—The orthogonal signal generator based phase-locked loops (OSG-PLLs) are among the most popular single-phase PLLs within the areas of power electronics and power systems, mainly because they are often easy to be implement and offer a robust performance against the grid disturbances. The main aim of this paper is to present a survey of the comparative performance evaluation among the state-of-the-art OSG-PLLs (include Delay-PLL, Deri-PLL, Park-PLL, SOGI-PLL, DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL) under different grid disturbances such as voltage sags, phase and frequency jumps, and in the presence of dc offset, harmonic components, and white noise in their input. This analysis provides a useful insight about the advantages and disadvantages of these PLLs. The performance enhancement of Delay-PLL, Deri-PLL, and CCF-PLL by including a moving average (MAF) filter into their structure is another goal of this paper.**

***Index Terms*—Frequency estimation, orthogonal signal generator (OSG), phase estimation, phase-locked loop (PLL), single-phase, synchronization.**

Manuscript received February 01, 2015; revised June 15, 2015; accepted July 23, 2015. Date of current version ***. This work was supported in part by the National Natural Science Foundation of China under Grant 51307015, and in part by the State Key Laboratory of Power Transmission Equipment & System Security and New Technology under Grant 2007DA10512713405, and in part by the Open Research Subject of Sichuan Province Key Laboratory of Power Electronics Energy-Saving Technologies & Equipment under Grant szjj2015-067, and in part by the Open Research Subject of Artificial Intelligence Key Laboratory of Sichuan Province under Grant 2015RZJ02. Recommended for publication by Assocaite Editor *****.

Y. Han and M. Luo are with the Department of Power Electronics, School of Mechatronics Engineering, University of Electronic Science and Technology of China, No.2006, Xiyuan Avenue, West Hi-Tech Zone, Chengdu 611731, China (e-mail: hanyang@uestc.edu.cn; 352974017@qq.com), also with the State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing 400044, China, and also with Artificial Intelligence Key Laboratory of Sichuan Province, Sichuan University of Science and Engineering, Zigong 643000, China.

X. Zhao and J. M. Guerrero are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: xzh@et.aau.dk, joz@et.aau.dk).

L. Xu is with the Sichuan Electric Power Research Institute, Sichuan Electric Power Company, Chengdu 610072, China (xulinn@163.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier ******/TPEL.*******

I. INTRODUCTION

The accurate extraction of the grid voltage phase-angle and frequency is of vital importance to ensure stable operation of grid-connected power electronic based equipment such as active power filters, uninterruptible power supplies, dynamic voltage restores, etc. [1-3]. However, the power quality issues caused by ever increasing penetration of the renewable energy sources such as the photovoltaic (PV) and wind power into the utility grid, as well as the proliferation of power electronics based loads in power systems has made this task more challenging than before. To tackle this problem, many advanced synchronization techniques have been proposed in recent years [1-13].

The Fourier Transform based techniques such as the discrete Fourier Transform [4], [5] and the fast Fourier Transform [6] are the basic methods for the spectrum analysis of power signals and extraction of the grid voltage phase, frequency, and amplitude. However, these techniques often assume that the grid voltage waveform is periodic and repetitive, which may lead to spectrum leakage problem due to unsynchronized sampling effect, causing errors for frequency and phase angle detection [7]. The Kalman Filter (KF) and the Extended Kalman Filter methods are alternative techniques for instantaneous tracking of grid voltage parameters [8]. However, the KF method is computationally demanding [9]. Some other techniques, such as the methods based on adaptive notch filter [10], zero-crossing detection method [11] and frequency-locked loop (FLL) [12]-[13] were also presented in recent literature to analyze the grid voltage phase angle.

The PLL algorithms are probably the most popular synchronization techniques for the grid-connected inverters applications owing to their ease of implementation and robustness [14]-[21]. Generally, a PLL is composed of three parts: phase detector (PD), loop filter (LF) and voltage-controlled oscillator (VCO) [22]. The LF normally is a proportional-integral (PI) controller which results in a type-2 control system (a control system of type-N has N poles at the origin in its open-loop transfer function) [23]. In most cases, a first-order low-pass filter (LPF) is also cascaded with the PI controller to improve the PLL filtering capability. The first-order LPF, however, has a limited ability to suppress the grid disturbances. Therefore, under some scenarios, it may be useful to use higher order LPFs in the PLL control loop [24].

From the PD point of view, the simplest PLL is a power-based PLL (*p*PLL), which uses a sinusoidal multiplier as

the PD [25]. The *p*PLL, however, suffers from remarkable double-frequency oscillations in their estimated quantities. A dynamic analysis and performance evaluation of the *p*PLL can be found in [26]. To overcome this drawback of the *p*PLL, some modifications have been suggested. In [27], a method based on peak voltage detection was proposed by Thacker *et al*. and in [28], a modified *p*PLL with double frequency and amplitude compensation method was presented by Golestan *et al*. Another approach to deal with the aforementioned problem of *p*PLLs is using an orthogonal signal generation (OSG) based PD in the PLL structure. These PDs use an OSG unit to create a fictitious orthogonal signal from the original single-phase signal [29]-[32]. In retrospect, the delay-based PLL (here named as Delay-PLL) is regarded as the earliest and simplest OSG-PLL method and its performance analysis was presented in [32]. Another simple method to generater an orthogonal signal is used a derivator (here named as Deri-PLL), however, this kind of PLL is rarely used in practical application due to the high sensitivity under distorted grid voltage conditions.

In recently years, some new OSGs schemes have been presented, such as the PD based on second-order generalized integrator (corresponding to the SOGI-PLL) and inverse-park transform (corresponding to the Park-PLL), which showa relatively fast transient response, high disturbance rejection capability, and a robust performance [7], [22]. The SOGI scheme was first proposed in 2006 by Ciobotaru *et al*. [33]. In [34], a multiple SOGI plus a FLL scheme was proposed by Rodriguez *et al*., in which the dual SOGI acts as the basic module called MSOGI-FLL, which can be used to detect the different harmonic components of the input signal. A modified SOGI-based OSG was proposed by Karimi Ghartemani *et al*. [18], in which an integrator is added to the SOGI structure to deal with the problem of dc offset. The Park-PLL also shows satisfactory performance under various grid voltage disturbance scenarios. In [35], the Park-PLL was used in a single-phase PV-power generation system to make the system more robust. In [22], a detailed mathematical analysis about the Park-PLL and SOGI-PLL was proposed by Golestan *et al*. and it is shown that these two PLL structures are equivalent to each other, from the control point of view.

On the other hand, the complex-coefficient filter (CCF) also has drawn much attention. In [36], a detail analysis about the CCF and multiple-CCF was presented and in [37], the design oriented of the MCCF-PLL was suggested. In [38], the CCF-PLL based on the z-domain was introduced, in which the negative frequency component can be effectively removed by using the CCF block. Therefore, the CCF shown in [38] can be considered as another kind of OSG. In [39], the PLL using the dc offset error compensation (DOEC-PLL) was proposed, which is capable of eliminating dc component effectively. The variable time-delay PLL (VTD-PLL) was presented in [40], which is a software-PLL (SPLL) and can achieve a fast transient response with low computational burden. The PD of the VTD-PLL consists of a sinusoidal multiplier, thus, VTD-PLL can be seen as an extension of the *p*PLL. Further, in [41], a three-phase frequency-adaptive PLL (TPFA-PLL) was presented for single-phase applications, in which the input signal of the PLL was enhanced and the moving-average filter (MAF) was used to improve the filtering performance [42].

In this paper, a survey of some OSG-based PLLs is presented, and a detailed comparison among the Delay-PLL, Deri-PLL, Park-PLL, SOGI-PLL, DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLL algorithms are carried out to gain a deep insight about their advantages and disadvantages. The evaluation is conducted under different grid disturbances such as voltage sags, phase and frequency jumps, and in the presence of harmonics, DC offset, and noise in the PLLs input. The results of this analysis can be very helpful for researcher and designers in the areas of single-phase grid-connected inverters and distributed generators (DGs).

The rest of this paper is organized as follows. Section II presents the overview of the aforementioned OSG-PLLs. The LF parameters design in s-domain is presented in Section III. In Section IV, the comparison of the experimental results under different grid voltage disturbance scenarios are presented. In Section V, the MAF method is presented to improve steady state and dynamic performance of Delay-PLL, Deri-PLL and CCF-PLL. Finally, Section VI concludes this paper.

II. Overview of the Different PLL Algorithms

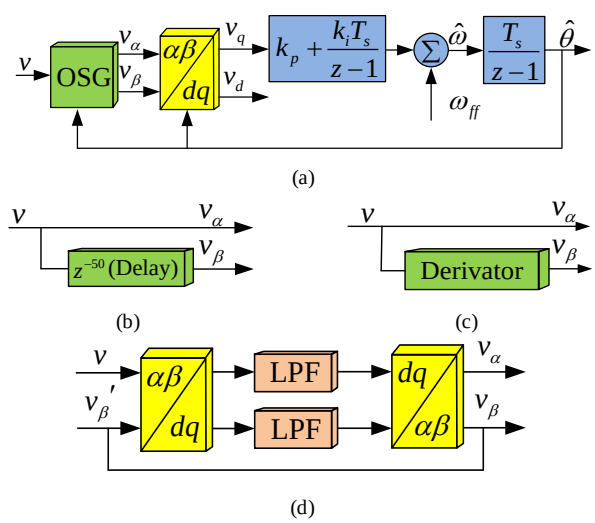
In this Section, eight different PLL algorithms mode are introduced and a generic mathematical model is also derived. Moreover, considering the practical implementation, all of the algorithms are conceived in the *z*-domain, and the following assumptions are considered: (i)The sampling frequency (f_s=1/T_s) is fixed to 10 kHz, and the fundamental angular frequency (ω_{ff}) is set to be 2π50 rad/s; (ii) The forward Euler method is used to discretize the LP and VCO except for the SOGI block, which is discretized by using the Tustin method in order to avoid the algebraic loop [38], [40].

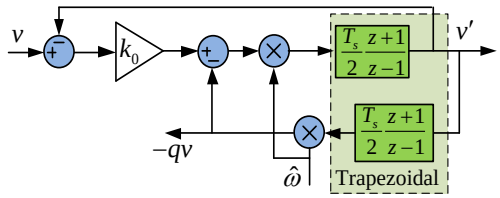
The grid voltage is presented in the discrete form as

$$v = V_g \sin(\theta_g) = V_g \sin(\omega_g k T_s + \phi_g) \qquad (1)$$

where V_g, θ_g, ω_g and ϕ_g are amplitude, phase-angle, angular frequency and initial phase of the grid voltage, respectively, and *k* denotes the *k*th sampling interval by the digital processor, and *k*=0,1,2,…,etc.

A. Conventional OSG-PLL





(e)

Fig. 1. A conventional OSG-PLL and different OSGs. (a) Block diagram of a typical OSG-PLL. (b) Delay based OSG. (c) Derivative based OSG. (d) Park transform based OSG. (e)SOGI based OSG.

Fig. 1(a) shows the general structure of a conventional OSG-PLL. Fig. 1(b) illustrates the delay based OSG, in which the orthogonal signal is created by $T/4$ (T is the grid fundamental period, and in discrete domain with a sample frequency f_s=10 kHz, the delay block is expressed as z^{-50}) cycle delaying the original single-phase signal.

When the $T/4$ delay algorithm is used as the OSG shown in Fig. 1(a), the mathematical expressions for v_α and v_β are

$$\begin{cases} v_\alpha = V_g \sin(\theta_g) \\ \phi(\omega_g) = -\dfrac{(\omega_g - \omega_{ff})T}{4} \\ v_\beta = -V_g \cos[\theta_g + \phi(\omega_g)] \end{cases} \tag{2}$$

where ω_{ff} is the nominal frequency (2π50 rad/s). By using Park's transformation, the mathematical expressions for v_q^{Delay} is

$$v_q^{Delay} = V_g \sin(\theta_g)\cos(\hat{\theta}) - V_g \sin(\hat{\theta})\cos[\theta_g + \phi(\omega_g)] \tag{3}$$

where $\hat{\theta}$ is the estimated value of the phase angle. From (3), as expected, only when the grid voltage frequency is at its normal value, $\phi(\omega_g)$ will equal to zero, and the Delay-PLL can track the grid frequency without steady-state error, and vice versa.

The derivative-based OSG is shown in Fig. 1(c), in which the orthogonal signals are produced by the differential operation. However, the differential operation will introduce high frequency noise and numerical errors. With the derivative-based OSG, the mathematical expressions of v_q^{Deri} can be expressed as

$$v_q^{Deri} = V_g\left(1+\frac{\omega_g}{\omega_{ff}}\right)\sin(\theta_g - \hat{\theta}) + \left(1+\frac{\omega_g}{\omega_{ff}}\right)V_g \sin(\hat{\theta})\cos(\theta_g) \tag{4}$$

As expected, (4) shows similar fluctuations characteristic as (3) when the grid frequency deviates from its nominal value. Moreover, if the gird voltage contains harmonics, the second term of (4) will increase with the increase of the order of harmonics. Especially in the condition of high-order harmonic and noise, the result of the estimated phase/frequency might be erroneous.

The park-based PD is shown in Fig. 1(d), where the Park transform is used typically as a tool to project an input voltage vector, defined by in-quadrature signal in $\alpha\beta$ stationary reference frame, on the orthogonal axes of the dq synchronous reference frame [43]. The SOGI-based PD and the integrator discretized by Tustin method is shown in Fig. 1(e). The equivalence of the Park and SOGI blocks was proved in [21], hence the transfer function of the OSG can be derived as

$$\begin{cases} G_\alpha(z) = \dfrac{v_\alpha(z)}{v(z)} = \dfrac{2k_0\hat{\omega}T_s(z^2-1)}{4(z-1)^2 + 2k_0\hat{\omega}T_s(z-1) + (\hat{\omega}T_s)^2(z+1)^2} \\ G_\beta(z) = \dfrac{v_\beta(z)}{v(z)} = \dfrac{k_0\hat{\omega}^2T_S^2(z+1)^2}{4(z-1)^2 + 2k_0\hat{\omega}T_s(z-1) + (\hat{\omega}T_s)^2(z+1)^2} \end{cases} \tag{5}$$

With the previously assumption, the output of the OSG block can be expressed as

$$\begin{cases} v_\alpha^{P,S} = V_g \sin(\theta_g) + g(k)e^{-\frac{\sqrt{2}\omega_g}{2}kT_s} \\ v_\beta^{P,S} = -V_g \cos(\theta_g) + h(k)e^{-\frac{\sqrt{2}\omega_g}{2}kT_s} \end{cases} \tag{6}$$

where the superscript P,S represents the Park-PLL and SOGI-PLL, $g(k)$ and $h(k)$ are the function of k, which can be expressed as [43]

$$\begin{cases} g(k) = -\dfrac{V_g}{\sqrt{1-(k_0/2)^2}}\sin(\omega_g\sqrt{1-(k_0/2)^2}kT_s) \\ h(k) = -\dfrac{V_g}{\sqrt{1-(k_0/2)^2}}\cos(\omega_g\sqrt{1-(k_0/2)^2}kT_s - \varphi) \\ \varphi = \arctan(\dfrac{k_0/2}{\sqrt{1-(k_0/2)^2}}) \end{cases} \tag{7}$$

It is worth noting that a gain k_0=1.414 implies the damping factor of (5) ξ_G=0.7 (ξ_G indicate the damping ratio of the equation (5) and depends the dynamic performance of the OSG block), which results in an optimal relationship between the setting time and overshoot in the dynamic response [35]. Thus, substituting k_0=1.414 into (7), the expressions for v_q is

$$\begin{cases} v_q^{P,S} = V_g \sin(\theta_g - \hat{\theta}) + f(k)e^{-\frac{\sqrt{2}\omega_g}{2}kT_s} \\ f(k) = -\sqrt{2}V_g \sin(\dfrac{\sqrt{2}}{2}\omega_g kT_s)\cos(\hat{\theta}) \\ \qquad -\sqrt{2}V_g \cos(\dfrac{\sqrt{2}}{2}\omega_g kT_s - \dfrac{\pi}{4})\sin(\hat{\theta}) \end{cases} \tag{8}$$

where $f(k)$ is the fluctuating terms, which decays to zero with a time constant of $\tau_p = k_0/\sqrt{2}\omega_g = \sqrt{2}/\omega_g$ and $v_q^{P,S}$ converges to $\theta_g - \hat{\theta}$ in the steady state conditions, which represents the steady-state error.

Then, v_q shown in (3), (4) and (8) is regulated to be zero and the phase angle of OSG output signal can be obtained. However, whether the phase angle of the input is equal to that of the output of the OSG is the key point to evaluate the performance of the OSG-PLL. Next, four recent OSG-PLLs are presented, namely, DOEC-PLL, VTD-PLL, CCF-PLL, and TPFA-PLL.

B. DOEC-PLL

Fig. 2 shows the general structure of the DOEC-PLL presented by Hwang *et al*. [39]. In this paper, the inverse-park transform is used to generate a virtual voltage (v_β), which is delayed by 90° from the measured grid voltage v_α.

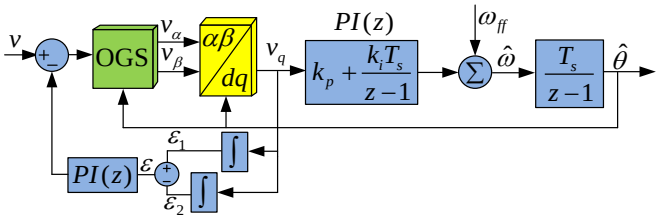


Fig. 2. The block diagram of the DOEC-PLL [39].

The grid voltage including the dc offset can be derived as

$$v = V_g \sin(\theta_g) + \Delta \tag{9}$$

where Δ is the amplitude of the dc offset.

Using the OSG technology and the Park's transformation, in the steady state, the following equations can be obtained

$$\begin{cases} v_{d,dc} = -1 - \Delta \sin\hat{\theta} + \Delta\cos\hat{\theta} \\ v_{q,dc} = \Delta\sin\hat{\theta} + \Delta\cos\hat{\theta} \end{cases} \tag{10}$$

To obtain the dc offset, the following expression is defined

$$\begin{cases} \varepsilon_1 = \int_0^{\pi} (\Delta\sin\hat{\theta} + \Delta\cos\hat{\theta}) d\hat{\theta} = 2\Delta \\ \varepsilon_2 = \int_{\pi}^{2\pi} (\Delta\sin\hat{\theta} + \Delta\cos\hat{\theta}) d\hat{\theta} = -2\Delta \end{cases} \tag{11}$$

The difference between ε_1 and ε_2 can be obtained as follows

$$\varepsilon = \varepsilon_1 - \varepsilon_2 = 4\Delta \tag{12}$$

Applying the integral operation at a specific interval in q-axis voltage, the dc offset can be separated as shown in (12). The PI controller is used to remove the dc offset error Δ.

C. VTD-PLL

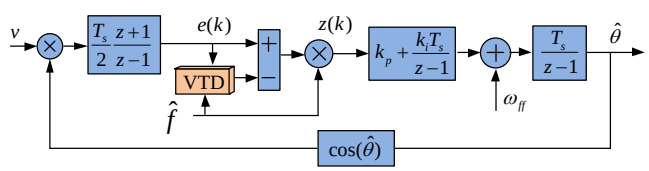


Fig. 3. Block diagram of the VTD-PLL [40].

Fig. 3 illustrates the block diagram of the VTD-PLL presented by A. Ozdemir *et al*. [40]. This algorithm adopts the variable time delay algorithm, which reduces the computation load remarkably. From Fig. 3, the error signal $e(k)$ can be denoted as

$$e(k) = V_g \sin(\Delta\theta) \tag{13}$$

where $\Delta\theta = \theta_g - \hat{\theta} = (\omega_g - \hat{\omega})kT_s = \Delta\omega k T_s$

After calculation of the VTD block, $z(k)$ is expressed as

$$z(k) = [e(k) - e(k-1)\hat{T}]\hat{f} \tag{14}$$

where $\hat{T}$ is the estimated period of input voltage and $e((k-1)\hat{T})$ is the delayed signal by $\hat{T}$, thus, equation (14) can be considered as derivative of $e(k)$ with respect to $\hat{T}$, which is derived as

$$z(k) = \frac{de(k)}{d\hat{T}} = \Delta\omega V_g \cos(\Delta\omega k T_s) \tag{15}$$

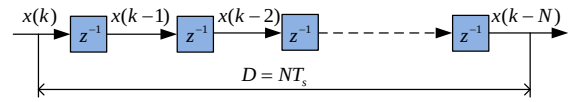


Fig. 4. Classical variable time-delay (VTD) structure [40].

Fig. 4 shows the block diagram of the classical variable time-delay structure. In EN 50160 standard, the frequency range is considered 47-52 Hz, and IEC considered 42.5-57.5 Hz. To consider a more adverse scenario, in this study, locking frequency range for the PLL is 40 Hz$\le f_{lock} \le$60 Hz, sampling period is T_s=100 μs. Accordingly, the range of N is calculated as $165 \le N \le 250$ [40].

Then, after convergence of the algorithm, $z(k)$ is regulated to be zero, which yields $\Delta\omega$=0, and the estimated frequency is controlled to be the pre-set value.

D. CCF-PLL

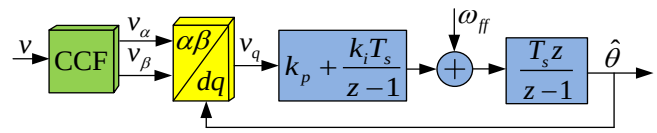


Fig. 5. Block diagram of the CCF-PLL [38].

Fig. 5 shows the lock diagram of the CCF-PLL presented by A. Ohoriet *al*. [38]. In this algorithm, the complex-coefficient filter is configured as a first-order IIR filter and is composed of two complex-coefficient band-pass filters (BPFs) and one notch filter (NF), which are shown in Fig. 6.

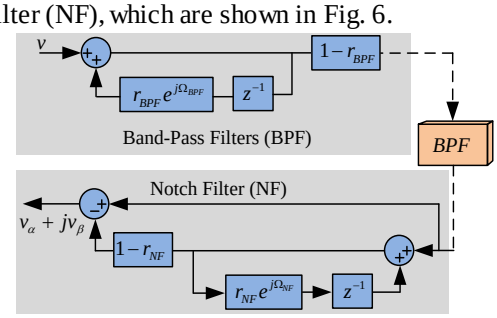


Fig. 6. The block diagram of complex-coefficient filters [38].

The input voltage can be rewritten as

$$v = V_g \sin(\theta_g) = \frac{V_g}{2j}\left(e^{j\theta_g} - e^{-j\theta_g}\right) \tag{16}$$

The negative frequency component ($-\theta_g$) is removed by the complex-coefficient filter, the output of the CCF block can be expressed as

$$v_{CCF} = \frac{V_g}{2j} e^{j\theta_g} = \frac{1}{2} V_g \sin(\theta_g) - \frac{j}{2} V_g \cos(\theta_g) = v_r + jv_i \tag{17}$$

The magnitude of (17) is normalized as follow

$$\frac{1}{\sqrt{v_r^2 + v_i^2}}(v_r + jv_i) = \sin(\theta_g) - j\cos(\theta_g) \tag{18}$$

By extracting the real and imaginary parts of (18), which are represented by v_α and v_β, respectively, a pair of orthogonal voltage vector can be obtained. Therefore, notice that the CCF can be seen as a special OSG.

E. TPFA-PLL

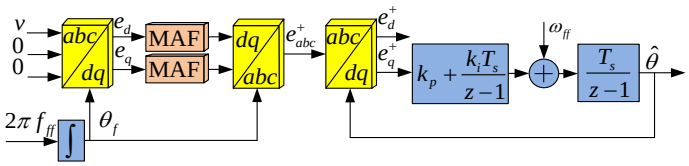


Fig. 7. Block diagram of the TPFA-PLL [41].

Fig. 7 shows a three-phase PLL to estimate the phase, frequency and amplitude of a single-phase system [41]. The *abc* input of the TPFA-PLL is assumed to be (v, 0, 0). If the window width of the MAF (T_ω) is equal $T/2$ all the second-order oscillation produced by unbalanced input voltage can be removed.

By applying the Park's transformation, e_d and e_q can be obtained as

$$\begin{cases} e_d = -\frac{V_g}{\sqrt{6}}[\cos(\theta_g+\theta_f)-\cos(\theta_g-\theta_f)] \\ e_q = \frac{V_g}{\sqrt{6}}[\sin(\theta_g+\theta_f)+\sin(\theta_g-\theta_f)] \end{cases} \tag{19}$$

where θ_f is an arbitrary angle at the grid frequency (ω_{ff}).If $T_\omega=T/2$, the terms with $\theta_g+\theta_f$ in (19) are filtered by MAF. Applying inverse Park's transformation to (19), the positive sequence is obtained in a stationary *abc* frame, as follows

$$e^+_{abc} = \frac{1}{3}V_g\left[\sin(\theta_g),\sin(\theta_g-\frac{2\pi}{3}),\sin(\theta_g-\frac{4\pi}{3})\right]^T \tag{20}$$

Then, the output angle of the TPFA-PLL $\hat{\theta}$ (the estimated phase angle) is used in the *dq* transformation to transform the set of voltage in (20). The following expression can be obtained

$$e^+_d = \frac{V_g}{3}\cos(\theta_g-\hat{\theta}), e^+_q = \frac{V_g}{3}\sin(\theta_g-\hat{\theta}) \tag{21}$$

Therefore, by controlling e_q^+ to be zero, the estimated frequency can be obtained. Unlike OGS-PLL, it is unnecessary for TPFA-PLL to produce a pair of orthogonal signals hence the additional numerical error can be avoided.

III. Parameter Design Guidelines

Since the PLL model is set up in z-domain, it seems to be more accurate to perform the LF parameters tuning in the z-domain instead of the s-domain. It should be noticed that the PLL bandwidth is much lower than its sampling frequency. Therefore, the s-domain analysis/tuning can provide an accuracy as good as that achievable in z-domain. In addition, the analysis/tuning in the Laplace domain is more convenient and straightforward than that in the z-domain [42]. For these reasons, in this Section, the generic linearized model of the PLL is presented in s-domain, which is shown in Fig. 8.

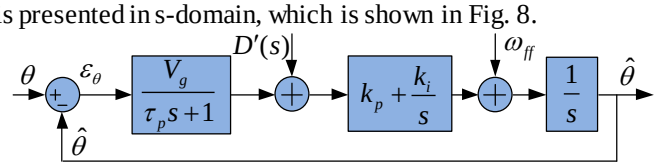


Fig. 8. Generic linearized model of the PLL.

For the sake of simplicity, in the PLL linearized model, the input voltage amplitude V_g is assumed to be unity. This assumption can be simply realized by dividing the PD output signal by an estimation of the input voltage amplitude before it was fed into the LF [22]. In this case, the open-loop transfer function of the PLL can be expressed as

$$G_{ol}(s) = \frac{k_p s + k_i}{s^2(\tau_p s+1)} = \frac{k_i(\tau_i s+1)}{s^2(\tau_p s+1)} \tag{22}$$

where $\tau_i=k_p/k_i$. It can be seen that (22) is a typical open-loop transfer function of the type-II system. In recent literature, many parameters design methods based on such transfer function have been presented. In this paper, a systemic way called symmetrical optimum method is introduced to design the parameters [44]. The core insight of the symmetrical optimum method is to obtain the maximum phase margin (PM) at the crossover frequency ω_c. Therefore, from (22), the amplitude and phase frequency characteristics can be written

$$|G_{ol}(j\omega)| = \frac{k_i}{\omega^2}\sqrt{\frac{(\tau_i\omega)^2+1}{(\tau_p\omega)^2+1}} \tag{23}$$

$$\angle G_{ol}(j\omega) = \arctan(\tau_i\omega) - 180° - \arctan(\tau_p\omega) \tag{24}$$

Therefore, the PM can be expressed

$$\gamma = \angle G_{ol}(j\omega_c) + 180° = \arctan(\tau_i\omega_c) - \arctan(\tau_p\omega_c) \tag{25}$$

In order to obtain the ω_c when $\gamma=\gamma_{\max}$, take the derivative of (25) with respect to ω_c, and equate the result to zero, gives

$$\omega_c = \frac{1}{\sqrt{\tau_i\tau_p}} \tag{26}$$

Thus, $\lg(\omega_c)=[\lg(\tau_i)+\lg(\tau_p)]/2$, which means in the bode diagram, $\lg(\tau_i)$ and $\lg(\tau_p)$ are symmetrical about $\lg(\omega_c)$. Then γ_{max} can be expressed as

$$\gamma_{\max} = \arctan(\sqrt{\tau_i/\tau_p}) - \arctan(\sqrt{\tau_p/\tau_i}) \tag{27}$$

According to trigonometric function operation

$$\sin(\gamma_{\max}) = \frac{\tau_i-\tau_p}{\tau_i+\tau_p} \tag{28}$$

Then, from (28)

$$\tau_i = \tau_p\frac{1+\sin(\gamma_{\max})}{1-\sin(\gamma_{\max})} \tag{29}$$

Normally, the PM with a range of $0<\gamma_{\max}\le 90°$ is considered, thus, the inequality $\tau_i \ge \tau_p$ can be obtained. Supposing that $\lg(1/\tau_p)-\lg(1/\tau_i)=2\lg\lambda$ ($\lambda\ge1$), it can be obtained that

$$\tau_i = \lambda^2\tau_p \tag{30}$$

Considering (26) and (30), and assuming the equation (23) equals to 1 when $\omega=\omega_c$, then

$$\begin{cases} k_i = \frac{1}{\lambda^3\tau_p^2} \\ k_p = \tau_i k_i = \frac{1}{\lambda\tau_p} \end{cases} \tag{31}$$

It can be seen that k_p and k_i is the function of λ and τ_p, thus, next step is to determine the value of λ and τ_p. From the open-loop transfer function (22), the closed-loop transfer function can be expressed as

$$G_{cl}(s)=\frac{G_{ol}(s)}{1+G_{ol}(s)}=\frac{k_i(\tau_i s+1)}{\tau_p s^3+s^2+k_i\tau_i s+k_i}$$
$$=\frac{\lambda^2\tau_p s+1}{(\lambda\tau_p s+1)[\lambda^2\tau_p^2 s^2+\lambda(\lambda-1)\tau_p s+1]} \quad (32)$$

From (32), the oscillating element should be design carefully. The damping ratio ξ = (λ - 1)/2, thus, ξ must be chosen to provide a fast transient response as well as a stable operation. Since most literature recommend ξ=0.7 for the best damping, this selection yield λ=2.4. Substituting λ=2.4 and (30) into (28), the value of $\gamma_{\max}$ can be derived as

$$\gamma_{\max}\approx 45° \quad (33)$$

which can be interpreted as a perfect PM.

Then, the disturbance rejection capability of the system is taken into consideration. The proper attenuation at $2\omega_{ff}$ (which is generated by the harmonic) is selected to be 25 dB in this paper. Substituting λ=2.4, (30) and (31) into (23), and assuming the equation (23) equals to -25 dB when ω=$2\omega_{ff}$, an approximate value of τ_p=0.004 can be calculated. Then the LF parameter can be calculated as k_i=4521 and k_p=104.

With the parameter designed, the PM of the PLL is about 44.8°, the crossover frequency ω_c=2π16.6 rad/s and the attenuation at $2\omega_{ff}$ is 24.3 dB. Thus, the PLL shows a high disturbance rejection capability and fast transient response.

IV. Experimental Results

The aim of this Section is to evaluate the performance of the eight PLLs under different grid scenarios, such as voltage sag, phase jump, frequency step, harmonics, DC offset and noise. To validate the analysis, the presented algorithms are tested in the Microgrid Research Lab of Aalborg University [45], and the experimental prototype was based on the 2.2 kW Danfoss inverter controlled in voltage control mode (VCM) using LCL output filter with resistive load, the capacitor voltage of the LCL filter was controlled to synthesize the virtual grid conditions. The inverter PWM frequency was set to be 10 kHz in order to evaluate the PLL algorithms with a discrete time-step of 100 microsecond, as analyzed in the paper. The dSPACE1006 platform was utilized to implement the Simulink-based control algorithms and the compiled executable file was downloaded to the dSPACE1006 controller to extract the real-time grid-synchronization signals.

The binary word size was only several kilobytes (kB) when the VCM was adopted for inverter control and the eight PLL algorithms were implemented, which facilities the practical implementation in both fixed point and floating point digital signal processors (DSPs). The phase and frequency step were set to be 90 degrees and 5 Hz, respectively. Throughout the experimental studies, the sampling frequency is fixed to be 10 kHz and the nominal angular frequency is set to 2π50 rad/s. The detailed comparison of eight PLL algorithms under different grid disturbance scenarios is shown in Table I.

A. Performance Comparison Under Voltage Sag

Figs. 9 and 10 show the experimental results of the estimated frequency and the phase estimation error when the grid is subjected to 0.4 per unit (p.u.) voltage sag. It can be observed that Deri-PLL presents a ripple of 0.1Hz in the estimated frequency with a slight overshoot. The Park-PLL, SOGI-PLL have similar dynamic performance, having all of them a respond time of about 3 cycles and an overshoot of 2.5 Hz. The Delay-PLL shows an overshoot of 3 Hz, but a smaller overshoot in phase error compared to the Park-PLL and the SOGI-PLL ones. The CCF-PLL shows a high frequency overshoot (10 Hz), and a relatively slow dynamic response with a respond time of 1.5 cycles. By comparison, VTD-PLL, DOEC-PLL and TPFA-PLL show a relatively fast overshoot compared to other grid synchronization schemes, with a transient overshoot of 0.7 Hz, 0.7 Hz and 1.5 Hz, respectively.

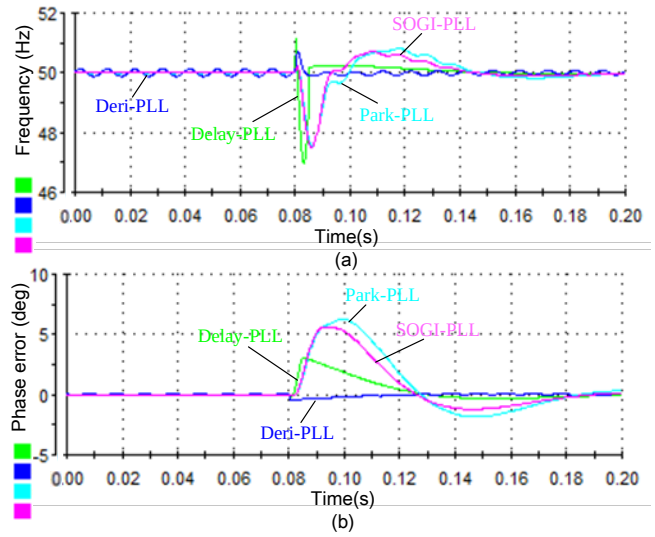


Fig. 9. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL and SOGI-PLL under 0.4 p.u. voltage sag in grid voltage. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

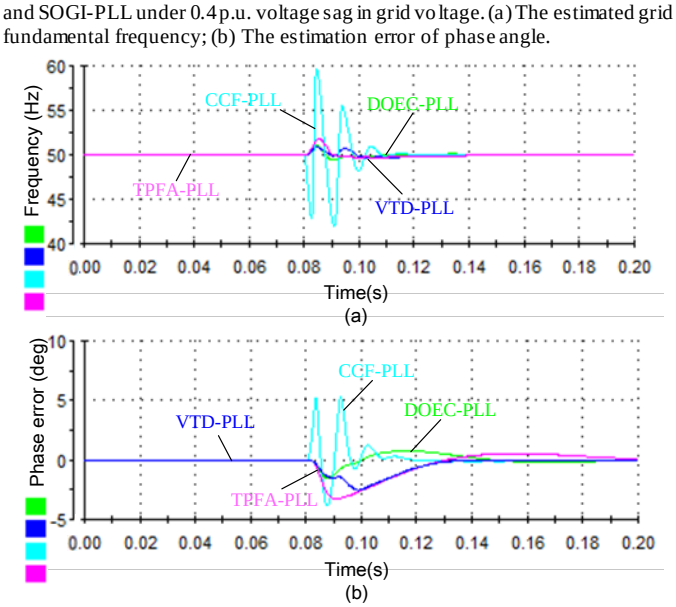


Fig. 10. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLLunder 0.4 p.u. voltage sag in grid voltage. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

B. Performance Comparison Under Phase-Angle Jump

Fig. 11 and Fig. 12 show the experimental results of the estimated frequency and the phase estimation error when the grid is subjected to 90 degrees phase-angle jump. Among the OGS-based PLLs, the Delay-PLL and Deri-PLL show better performance than the Park-PLL and SOGI-PLL with a response time of about 2 cycles. A similar performance can be observed

between Park-PLL and DOEC-PLL, due to the equivalence of the OSG block, with a response time of 4 cycles. The SOGI-PLL and VTD-PLL show a response time of 3.5 cycles. But for CCF-PLL and TPFA-PLL, the response time is about 5 cycles. Therefore, optimal dynamic performance can be obtained by using the Delay-PLL under grid voltage phase-angle jumps.

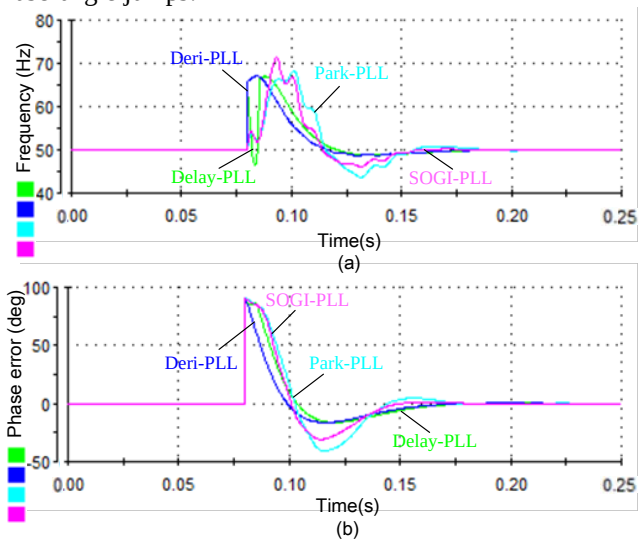


Fig. 11. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL and SOGI-PLL under 90 degrees phase jump in grid voltage. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

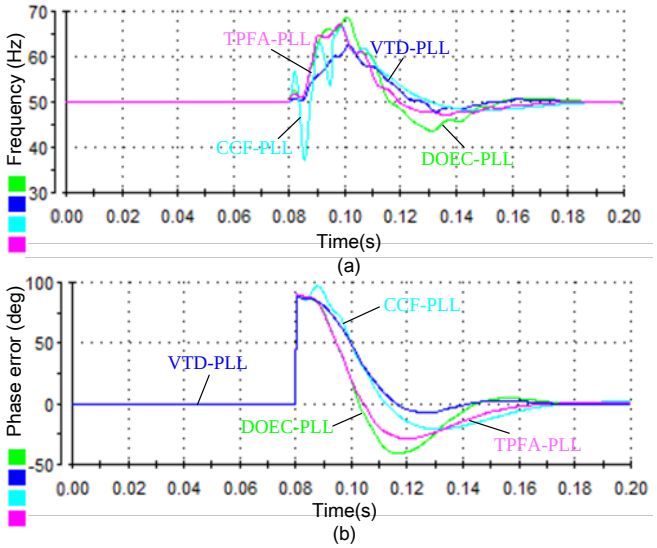


Fig. 12. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLL under 90 degree phase jump in grid voltage. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

C. *Performance Comparison Under Frequency Steps*

Figs. 13 and 14 show the experimental results of the estimated frequency and the phase estimation error when a sudden frequency jump of 5 Hz occurs in the grid voltage. The Delay-PLL and Deri-PLL show similar steady-state fluctuation, and in particular, the Delay-PLL shows steady-state error (about 5°) in phase estimation because of the fix time delay. The CCF-PLL shows a higher fluctuation of about 15 Hz due to the adoption of the band-pass filter, which has a narrow pass band. Because of the integral link in VTD-PLL, and the frequency-adaptive MAF in TPFA-PLL, the two PLLs show a slow dynamic response, both with a response time of about 4.5 cycles. For Park-PLL and DOEC-PLL, similar results are achieved, the estimated frequency is locked to the rated value in about 3.5 cycles, and for Deri-PLL and SOGI-PLL, the response time is around 2.5 cycles. Through the comprehensive comparison, the Park-PLL and SOGI-PLL show the relatively satisfactory performance when frequency step occurs.

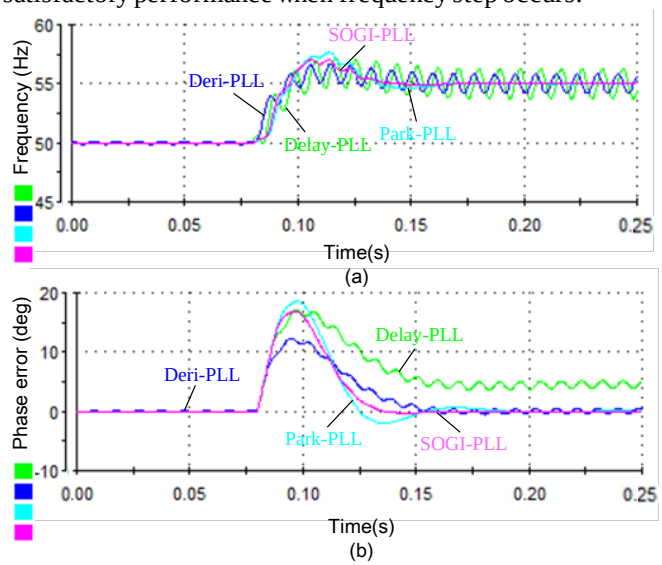


Fig. 13. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL and SOGI-PLL under a sudden frequency jump of +5 Hz. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

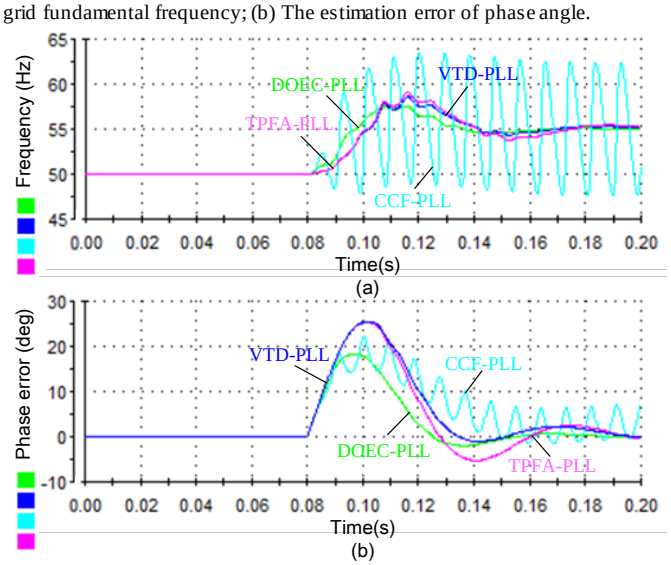


Fig. 14. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLL under a sudden frequency jump of +5 Hz. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

D. *Performance Comparison Under Grid Voltage Harmonics*

According to EN 50160 Standard [46], which the maximum allowed THD is 8%, 0.05p.u. 3rd, 0.05 p.u. 5th and 0.04 7th order harmonics components are applied to the grid voltage to test these algorithms. Figs. 15 and 16 show the experimental results of the estimated frequency and the phase estimation error. The Delay-PLL and Deri-PLL show noticeable oscillations in the estimated frequency due to the lack of filter. By comparison, the oscillations of Park-PLL, SOGI-PLL and DOEC-PLL are much smaller, with a frequency error of about 1 Hz. The

CCF-PLL shows a frequency error of about 1.5Hz. However, the VTD-PLL and TPFA-PLL show the lowest frequency oscillations with nearly zero steady-state errors compared to other PLL algorithms.

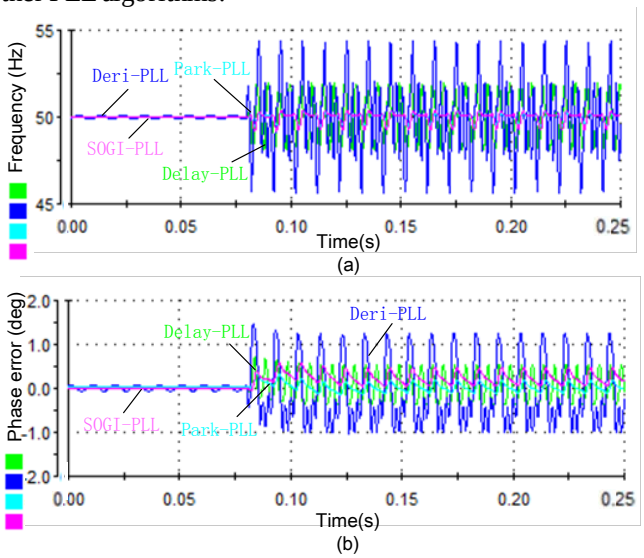


Fig. 15. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL and SOGI-PLL under 0.05 p.u. 3rd order, 0.05 p.u. 5th order and0.04 p.u. 7th order harmonics. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

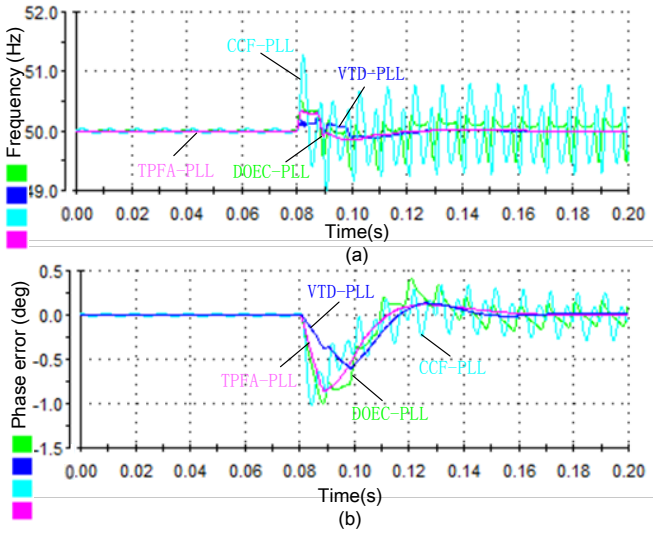


Fig. 16. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLL under 0.05 p.u. 3rd order, 0.05 p.u. 5th order and 0.04 p.u. 7th order harmonics. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

E. Performance Comparison Under DC Offset

Figs. 17 and 18 show the experimental results of the estimated frequency and the phase estimation error when a sudden dc offset of 0.04 p.u. occurs in the grid voltage. In this case, the four OGS-based PLLs have the similar steady-state oscillations with the peak-peak frequency error of nearly 1.5 Hz. However, the CCF-PLL undergoes the biggest steady-state oscillations of 3.2 Hz. The TPFA-PLL shows the estimation error of about 1.3 Hz in the estimation frequency. Because of the DC offset error compensator, the DOEC-PLL can acquire the zero steady-state error of both estimated frequency and phase. It is interesting to notice that the VTD-PLL also shows similar dynamic response to DOEC-PLL. Therefore, the best performance under dc offset scenario is achieved by DOEC-PLL and VTD-PLL.

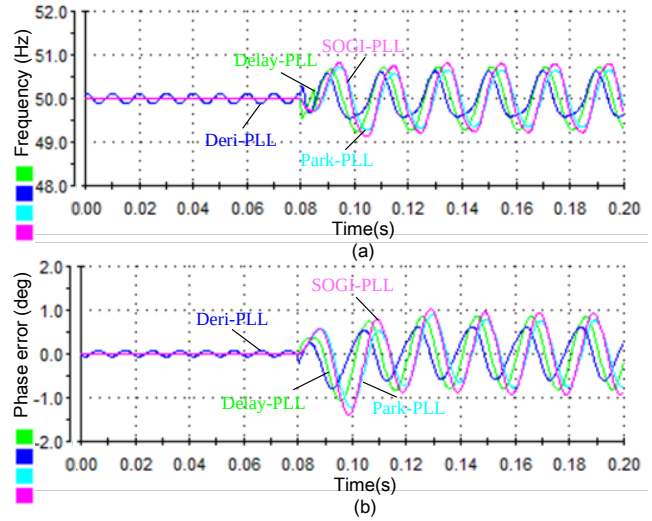


Fig. 17. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL and SOGI-PLL under a sudden dc offset of 10V. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

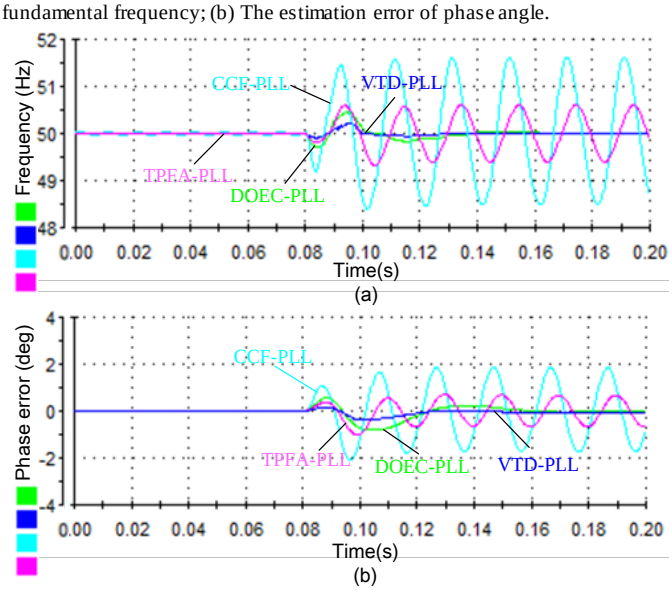


Fig. 18. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLL under a sudden dc offset of 10V. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

F. Performance Comparison Under White Gaussian Noise

To evaluate the electromagnetic interference (EMI) noise immunity of the PLLs, a white Gaussian noise of variance σ^2=0.01 is added to the grid voltage. The signal-to-noise-ratio (SNR) in the PLL input is SNR=10 log $(1/2\sigma^2)$ =17 dB. The noisy waveform is sampled at a rate of 100 kHz, and is then fed to a digital anti-aliasing. This high sampling rate is to avoid the aliasing effects and increase the accuracy of simulations. A digital first-order LPF with cutoff frequency of 4 kHz is considered as the anti-aliasing filter. The output of anti-aliasing filter is down sampled to 10 kHz and is fed to the PLL [42].

Figs. 19 and 20 show the experimental results of the estimated frequency and the phase estimation error. Similar to the case of harmonic contamination, the Delay-PLL and Deri-PLL show noticeable oscillations in the estimated

frequency with the amplitude of about 2.3 Hz and more than 100 Hz, respectively. The Park-PLL and DOEC-PLL show the estimation error of about 0.25 Hz. The VTD-PLL and TPFA-PLL show the lowest steady-state oscillations of about 0.12 Hz. For CCF-PLL, the peak-to-peak frequency error is about 0.6 Hz, which is bigger than SOGI-PLL (0.30 Hz).

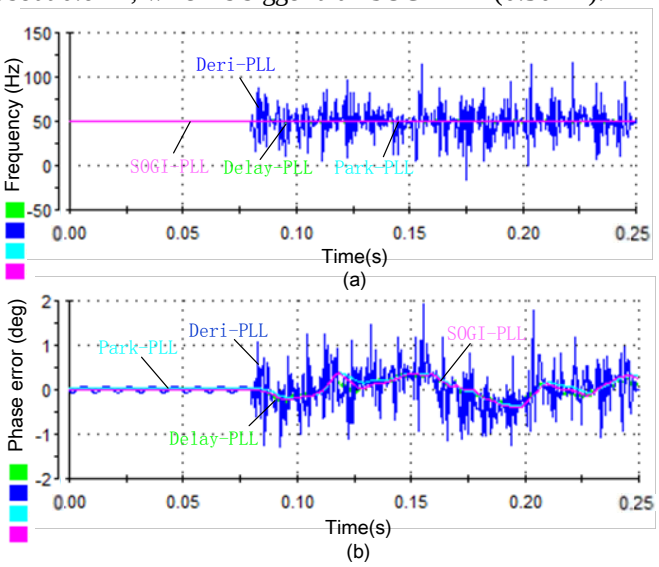


Fig. 19. Performance comparison among the Delay-PLL, Deri-PLL, Park-PLL and SOGI-PLL when the noise (variance σ^2=0.01) is suddenly applied in the grid voltage. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

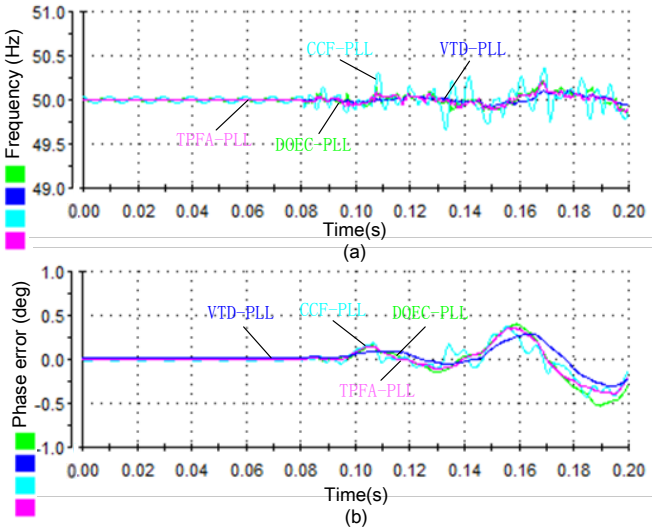


Fig. 20. Performance comparison among the DOEC-PLL, VTD-PLL, CCF-PLL and TPFA-PLL when the noise (variance σ^2=0.01) is suddenly applied in the grid voltage. (a) The estimated grid fundamental frequency; (b) The estimation error of phase angle.

V. Performance Improvement using MAF

From experimental results presented in the last section, the Park-PLL, SOGI-PLL, DOEC-PLL, VTD-PLL and TPFA-PLL show relatively satisfactory performance. However, the performance of Delay-PLL, Deri-PLL and CCF-PLL under grid frequency variations, harmonics and white noise scenarios is still unsatisfactory. In order to optimize the performance of Delay-PLL, Deri-PLL and CCF-PLL, the MAF is presented to achieve this propose as an inner loop filter. It should be noted that the application of MAF may reduce the open-loop bandwidth due to the large phase shift of the MAF [47].

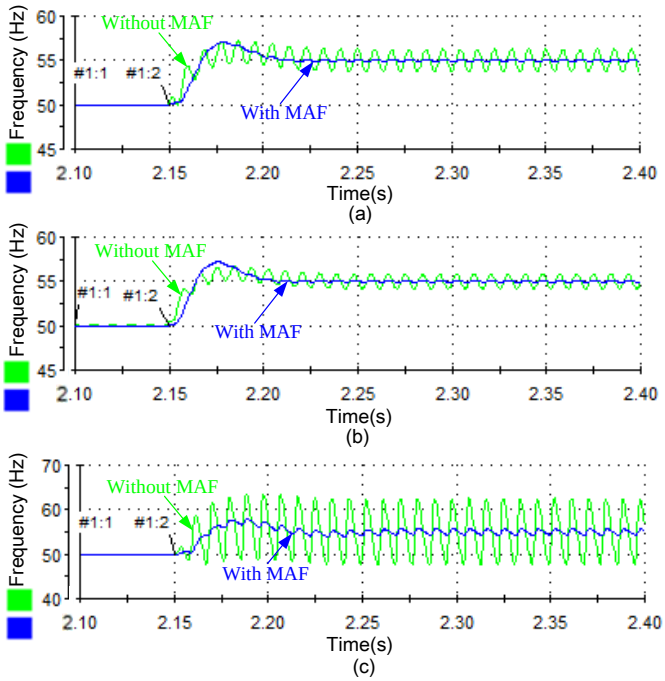


Fig. 21. Obtained results with and/or withoutMAF when the grid voltage undergoes a frequency of +5Hz. (a) Delay-PLL. (b) Deri-PLL. (c) CCF-PLL.

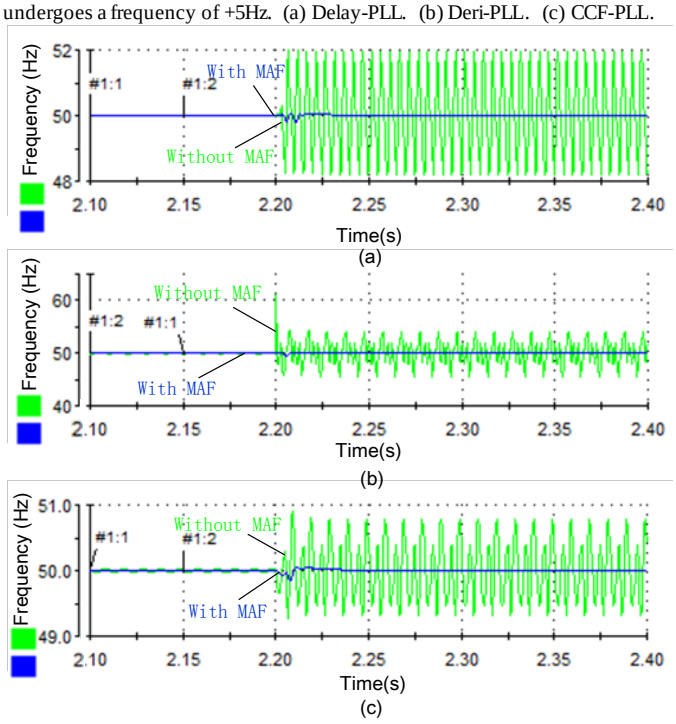


Fig. 22. Experimental results with and without MAF when the grid voltage undergoes 0.05 p.u. 3rd order, 0.05 p.u. 5th order and 0.04 p.u. 7th order harmonics. (a) Delay-PLL. (b) Deri-PLL. (c) CCF-PLL.

The experimental results under grid frequency variations, harmonics and white noise scenarios are shown in Figs. 21, 22, and 23, respectively. The detailed comparisons of Delay-PLL, Deri-PLL and CCF-PLL with and without MAF are shown in Table II.

Fig. 21 shows the comparative results between with and/or without MAF when the grid voltage undergoes a frequency jump of 5 Hz. It is obvious that the steady-state oscillations

have been mitigated by the use of the MAF. For the Delay-PLL, the estimation error in frequency is reduced from 2.5 to 0.2 Hz. For the Deri-PLL, the estimation error is reduced from 1.6 to 0.1Hz and for the CCF-PLL, the error is reduced from 14.7 to 1.2 Hz.

Fig. 22 shows the comparative results between with and/or without MAF when the grid voltage undergoes 0.05 p.u. 3rd order, 0.05 p.u. 5th order and 0.04 p.u. 7th order harmonics. Similarly as in the previously analysis, the estimation error in the frequency has been reduced to zero which means MAF almost eliminates the harmonics completely.

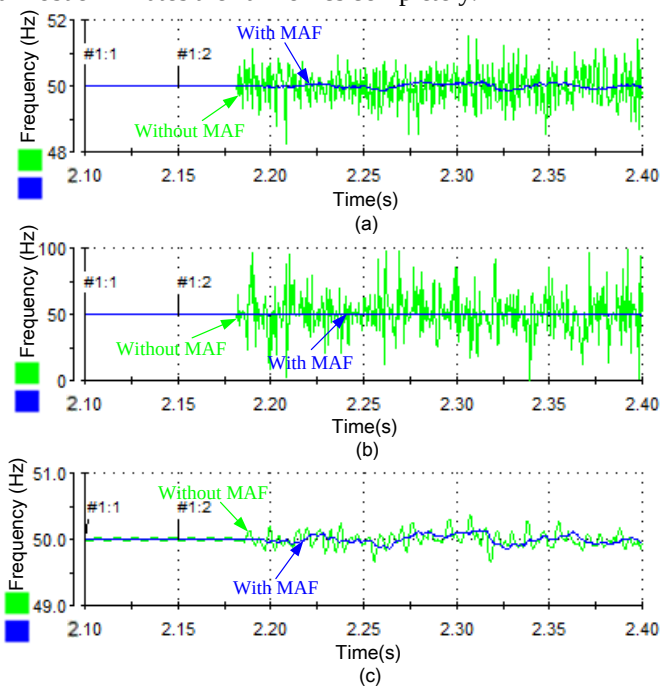


Fig. 23. Experimental results with and without MAF when the noise (variance σ^2=0.01) is suddenly applied in the grid voltage. (a) Delay-PLL. (b) Deri-PLL. (c) CCF-PLL.

Fig. 23 shows the comparative results between with and/or without MAF when the white Gaussian noise (variance σ^2=0.01) is suddenly applied in the grid voltage. For Delay-PLL and Deri-PLL, it shows that the steady-state errors are eliminated effectively. As for the CCF-PLL, it is interesting to notice that the fluctuation ripple of about 0.2 Hz in the estimated frequency is also suppressed.

VI. Conclusions

A detailed analysis and performance comparison of eight single-phase PLLs is presented in this paper. From the presented comprehensive comparison, it is found that Delay-PLL, Deri-PLL and VTD-PLL show relatively desired dynamic performance under voltage sag and phase-angle jump scenarios. When grid voltage undergoes frequency step, Park-PLL and SOGI-PLL may be a good choice. When grid voltage undergoes harmonic contamination scenario, TPFA-PLL can achieve zero steady-state error due to the use of MAF, and for dc offset scenario, DOEC-PLL and VTD-PLL show the best performance. When grid voltage undergoes random noise contamination scenario, all PLLs show some noise immunity capability except for Delay-PLL and Deri-PLL due to the lack of filter in their control structures. However, under a wide range of grid disturbance conditions, Park-PLL, SOGI-PLL, and TPFA-PLL show satisfactory performance for achieving a tradeoff between steady-state accuracy and dynamic response.

Finally, the MAF is applied to effectively attenuate steady state oscillation of the Delay-PLL, Deri-PLL and CCF-PLL under grid frequency step, harmonics and noise scenarios. The presented results provide useful guidelines for choosing and designing the proper grid synchronization schemes for single-phase grid-connected inverters and DGs.

TABLE I
Summary of Results for the Eight PLL Algorithms

	Delay-PLL	Deri-PLL	Park-PLL	SOGI-PLL	DOEC-PLL	VTD-PLL	CCF-PLL	TPFA-PLL
Voltage sag of -0.4 p.u.								
Settling time (5%)	22 ms	0	60 ms	55 ms	16 ms	20 ms	30 ms	15 ms
Frequency overshoot	2.9 Hz	0	2.5 Hz	2.5 Hz	0.7 Hz	0.7 Hz	10.0 Hz	1.5 Hz
Peak phase error	3.3°	0	6.7°	6.0°	2.0°	2.5°	5.5°	3.5°
Phase-angle jump of pi/2								
Settling time (5%)	40 ms	40 ms	81 ms	70 ms	82 ms	71ms	104 ms	105 ms
Frequency overshoot	17.0 Hz	17.0 Hz	18.9 Hz	22.0 Hz	18.9 Hz	12.4 Hz	16.6 Hz	17.1 Hz
Peak phase error	16.2°	16.0°	37.0°	25.0°	40.5°	10.8°	17.8°	28.8°
Frequency step of +5Hz								
Settling time (5%)	70 ms	70 ms	72 ms	53ms	72 ms	90 ms	75ms	90 ms
Frequency overshoot	2.2 Hz	2.0 Hz	2.5 Hz	2.1 Hz	2.5 Hz	3.5 Hz	8.1 Hz	2.6 Hz
Peak phase error	16.0°	12.5°	17.0°	15.5°	17.0°	25.0°	21.0°	25.0°
Harmonics								
Peak-peak frequency error	3.8 Hz	8.7 Hz	1.1 Hz	1.2 Hz	0.9 Hz	0	1.5 Hz	0
Peak-peak phase error	0.8°	2.2°	0.4°	0.4°	0.3°	0	0.6°	0
DC offset								
Peak-peak frequency error	1.6 Hz	1.5 Hz	1.5 Hz	1.7 Hz	0	0	3.2 Hz	1.2 Hz
Peak-peak phase error	1.7°	1.5°	1.8°	1.9°	0	0	3.8°	1.2°
White noise (power=0.01W)								
Peak-peak frequency error	2.30 Hz	120 Hz	0.25 Hz	0.30 Hz	0.23 Hz	0.12 Hz	0.60 Hz	0.13 Hz
Peak-peak phase error	0.4°	3.1°	0.7°	0.8°	0.8°	0.5°	0.5°	0.6°

TABLE II
COMPARISON OF DELAY-PLL, DERI-PLL AND CCF-PLL WITH OR WITHOUT MAF

	Delay-PLL		Deri-PLL		CCF-PLL	
With (w) or Without (w/o) MAF	w/o-MAF	w-MAF	w/o-MAF	w-MAF	w/o-MAF	w-MAF
Frequency step of +5Hz						
Steady-state oscillations	2.50 Hz	0.22 Hz	1.62 Hz	0.10 Hz	14.72 Hz	1.27 Hz
Harmonics						
Peak-peak frequency error	3.8 Hz	0	8.7 Hz	0	1.5Hz	0
Peak-peak phase error	0.8°	0	2.2°	0	0.6°	0
White noise (power=0.01W)						
Peak-peak frequency error	2.3 Hz	0.22 Hz	120 Hz	0.92 Hz	0.60 Hz	0.30 Hz
Peak-peak phase error	0.4°	0.3°	1.5°	0.4°	0.5°	0.3°

REFERENCES

[1] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, P. Fernandez-Comesana, and C. Martinez-Penalver, "A signal-processing adaptive algorithm for selective current harmonic cancellation in active power filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2829-2840, Aug. 2009.

[2] S. Golestan, M. Ramezani, and J. M. Guerrero, "Dq-frame cascaded delayed signal cancellation-based PLL: analysis, design, and comparison with moving average filter-based PLL,"*IEEE Trans. Power Electron*, vol. 30, no, 3, pp, 1618-1632, Mar. 2015.

[3] V. Soares, P. Verdelho, and G. D. Marques, "An instantaneous active and reactive current component method for active filters," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 660-669, Jul. 2000.

[4] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Tracking of time-varying grid voltage using DFT based second order generalized intergrator techniques," in *Proc. IEEE Int. conf. power Sys. Tech.*, 2012, pp. 1-6.

[5] S. Chandrasekaran and K. Ragavan, "Phase-locked loop technique based on sliding DFT for single phase grid converter application," in *Proc. IEEE Int. Conf. Power Elect. Drives and Ener. Sys. (PEDES)*, 2012, pp. 1-4.

[6] K. J. Lee, J. P.Lee, D. Shin, D. W.Yoo, and H. J. Kim, "A novel grid synchronization PLL method based on adaptive low-pass notch filter for grid-connected PCS," *IEEE Trans. Ind. Electron.*, vol. 61, no, 1, pp, 292-301, Feb. 2014.

[7] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Accurate estimation of single-phase grid voltage parameters under distorted conditions," *IEEE Trans. Power Del.*, vol. 29, no. 3, June 2014.

[8] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "Instantaneous power quality analysis using frequency adaptive Kalman filter technique," in *Proc. IEEE Int. Power Elect. Motion Cont. Conf. –ECCE Asia*, 2012, pp. 81-87.

[9] K. Q. Z. Chiang and M. L. Psiaki, "Kalman filter tracking of limb scan signal using a bank of correlators," *IEEE Trans. Aero. and Elect. Sys.*, vol. 49, no. 1, pp. 118-133, Jan. 2013.

[10] G. Yin, L. Guo, and X. Li, "An amplitude adaptive notch filter for grid signal processing," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2638-2641, Jun. 2013.

[11] B. Liu, F. Zhou, Y. Zhu, H. Yi, and F. Wang, "A three-phase PLL algorithm based on signal reforming under distorted grid conditions," *IEEE Trans. Power Electron.*, vol. pp, no. 99, pp. 1, Oct. 2014.

[12] R. N. Dean and A. K. Rane, "A digital frequency-locked loop system for capacitance measurement," *IEEE Trans. Instrum. Meas.*, vol. 62, no. 4, pp. 777-784, Feb. 2013.

[13] J. Matas, M. Castilla, J. Miret, L. G. Vicuna, and R. Guzman, "An adaptive prefiltering method to improve the speed/accuracy tradeoff of voltage sequence detection methods under adverse grid conditions," *IEEE Trans.Ind. Electron.*, vol. 61, no. 5, pp. 2139-2151, May. 2014.

[14] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A new hybrid PLL for interconnecting renewable energy systems to the grid," *IEEE Trans. Ind. App.*, vol. 60, no. 6, pp. 2709-2719, Nov. 2013.

[15] M. Karimi-Ghartemani, M. Mojiri, A. Safaee, J. A. Walseth, and A. Bakhshai, "A new phase-locked loop system for three phase applications," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1208-1218, March. 2013.

[16] L. Wang, Q. R. Jiang, L. C. Hong, C. P. Zhang, and Y. D. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4528-4549. Oct. 2013.

[17] M. Karimi-Ghartemani, "A unifying approach to single-phase synchronous reference frame PLLs," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4550-4556. Oct. 2013.

[18] M. Karimi-Ghartemani, S. A. Khajehoddin, P. L. Jain, A. Bakhshai, and M. Mojiri, "Addressing DC component in PLL and notch filter algorithms," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 78-86, Jan. 2012.

[19] A. Kulkarni and V. John, "Analysis of bandwidth-unit-vector-distortion tradeoff in PLL during abnormal grid condition," *IEEE Trans. Power Electron.*, vol. 60, no. 12, pp. 5820-5829, Dec. 2013.

[20] S. Golestan and J. M. Guerrero, "Conventional synchronous reference frame phase-locked loop is an adaptive complex filter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1679-1682, Mar. 2015.

[21] D. Dong, B. Wen, P. Mattavelli, D. Boroyevich, and Y. S. Xue, "Modeling and design of islanding detection using phase-locked loops in Three-Phase grid-interface power converters," *IEEE Trans. Ind. Electron.*, vol. 2, no. 4, pp. 1032-1040, Dec. 2014.

[22] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no 6, pp, 2167-2177, June 2013.

[23] S. Golestan, F. D. Freijedo, and A. Vidal, J. M. Guerrero and J. D. Gandoy, "A quasi-type-1 phase-locked loop structure," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6264-6270, Dec. 2014.

[24] S. Golestan, F. D. Freijedo, and J. M. Guerrero, "A systematic approach to design high-order phase-locked loops," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2885-2890, Jun. 2015.

[25] V. D. Bacon, S. A. O. D. Silva, L. B. G. Campanhol, and B. A. Angelico, "Stability analysis and performance evaluation of a single-phase phase-locked loop algorithm using a non-autonomous adaptive filter," *IET Power Electron.*, vol. 7, no. 8, pp. 2081-2092, Aug. 2014.

[26] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923-2932, Aug. 2008.

[27] T. Thacker, D. Boroyevich, R. Burgos, and F. Wang, "Phase-locked loop noise reduction via phase detector implementation for single-phase systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2482-2490, Jun.2011.

[28] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639-3650, Aug. 2012.

[29] C. Subramanian and R. Kanagaraj, "Single-phase grid voltage attributes tracking for the control of grid power converters," *IEEE Trans. Power Electron.*, vol. 2, no. 4, pp. 1041-1048, Jul. 2014.

[30] D. Dong, D. Boroyevich, and I. Cvetkovic, "A high-performance single-phase phase-locked-loop with fast line-voltage amplitude tracking," in *Poc.26th Ann. Conf. of IEEE Applied Power and Electron. (APEC)*, Mar. 2011, pp. 1622-1628.

[31] R. J. Ferreira, R. E. Araujo, and J. A. P. Lopes, "A comparative analysis and implementation of various PLL techniques applied to single-phase grids," in *Poc.3rd IEEE Int. Youth Conf. Energetics. (IYCE)*, Jul. 2011, pp. 1-8.

[32] S. M. Silva, B. M. Lopes, J. C. Filho, R. P. Campana, and W. C. Bosventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," *In Proceedings of the Industry Applications Conference2004 (IAS'04)*, Vol. 4, October 2004, pp. 2259-2263.

[33] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase

PLL structure based on second order generalized integrator," in *Proc. 37thIEEE PESC*, Jun. 2006, pp. 1511-1516.

[34] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp.127-138 2011.

[35] Z. Wang, S. T. Fan; Y. Zheng, and M. Cheng, "Control of a six-switch inverter based single-phase grid-connected PV generation system with inverse Park transform PLL," *Industrial Electronics (ISIE), IEEE International Symposium on* , vol., no., pp.258-263, 28-31 May 2012.

[36] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194-1204, Apr. 2011.

[37] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765-778, Feb. 2013.

[38] A. Ohori, N. Hattori, and T. Funaki, "Phase-locked loop using complex-coefficient filters for grid-connected inverter," *Electrical Engineering in Japan*, vol. 189, no.4, pp, 52-60, April 2013.

[39] S. H. Hwang, L. Liu, and H. Li, "DC offset error compensation for synchronous reference frame PLL in single-phase grid-connected converters," *IEEE Trans. Power Electron*, vol.27, no. 8, pp, 3467-3471, Aug. 2012.

[40] A. Ozdemir, and I. Yazici, "Fast and robust software-based digital phase-locked loop for power electronics applications," *IET Gener. Transm. Distrib.*, vol.7, lss. 12, pp. 1435-1441, May 2013.

[41] M. Mitra, P. Josep, and G. Vassilios, "A three-phase frequency-adaptive phase-locked loop for independent single-phase operation," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp, 6255-6259, Dec. 2014.

[42] S. Golestan, M. Ramezani, F. D. Freijedo, M. Monfared, and J. M. Guerrero, "Moving average filter based phase-locked loop: performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no, 6, pp. 2750-2763, Jul. 2013.

[43] R. Teodorescu, M. Liserre, and P. Rodrguez, "Grid synchronization in single-phase power converters," in *Grid converters for photovoltaic and wind power systems* 3rd ed., 2011, pp. 43-91.

[44] C. Tang, "Four design methods for proportional-integral controller of grid-connected inverter with LCL output filter," *Journal of Power system technology*, vol. 37, no. 11, pp. 3268-3275, Nov. 2013.

[45] Microgrid Research Programme, Aalborg University: www.microgrids.et.aau.dk.

[46] A. Moeini, H. Iman-Eini, and M. Bakhshizadeh, "Selective harmonic mitigation-pulse-width modulation technique with variable DC-link voltages in single and three-phase cascaded H-bridge inverters," *IET Power Electron.*, vol. 7, no. 4, pp. 924-932, Apr. 2014.

[47] J. Y. Wang, J. Liang, F. Gao, L. Zhang, and Z. D. Wang, "A method to improve the dynamic performance of moving average filter based PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5978-5990, Oct. 2015.

Yang Han (S'08-M'10) was born in Chengdu, China. He received his Ph.D. in Electrical Engineering from Shanghai Jiaotong University (SJTU), Shanghai, China, in 2010. He joined the Department of Power Electronics, School of Mechatronics Engineering, University of Electronic Science and Technology of China (UESTC) in 2010, and where he has been an Associate Professor since 2013. From March 2014 to March 2015, he was a Visiting Scholar at the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His research interests include phase-locked loop (PLL), AC/DC microgrids, power quality, grid-connected converters for renewable and DGs, active power filters and static synchronous compensators (STATCOMs). He has authored more than 20 ISI-indexed journal papers in the area of power electronics, power quality conditioners, and smart grid. He received Best Paper Awards from 2013 Annual Conference of HVDC and Power Electronics Committee of Chinese Society of Electrical Engineers (CSEE) in Chongqing, China, and the 4th International Conference on Power Quality in 2008, in Yangzhou, China.

Mingyu Luo was born in Sichuan, China in 1992. He received the B. S. degree in Electrical Engineering and Automation from university of electronic science and technology of china, Chengdu, China, in 2014. He is currently working toward the M. S. degree at the University of Electronic Science and Technology of China (UESTC), Chengdu, China. His research interests include phase-locked loop (PLL), power quality, power converters, and DFIG-based wind power generation systems.

Xin Zhao received the B.S. and M.S. degree in Power Electronics & Electrical Drives from Northwestern Polytechnical University, Xi'an, China, in 2010 and 2013, respectively. He is currently working toward the Ph.D. degree at Department of Energy Technology, Aalborg University, Denmark.
His research interests include control of power converters, power quality and microgrids.

Josep M. Guerrero (S'01-M'04-SM'08-FM'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program. From 2012 he is a guest Professor at the Chinese Academy of Science and the Nanjing University of Aeronautics and Astronautics; from 2014 he is chair Professor in Shandong University; and from 2015 he is a distinguished guest Professor in Hunan University.

His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, and optimization of microgrids and islanded minigrids. He is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and the IEEE Industrial Electronics Magazine, and an Editor for the IEEE TRANSACTIONS on SMART GRID and IEEE TRANSACTIONS on ENERGY CONVERSION. He has been Guest Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issues: Power Electronics for Wind Energy Conversion and Power Electronics for Microgrids; the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Special Sections: Uninterruptible Power Supplies systems, Renewable Energy Systems, Distributed Generation and Microgrids, and Industrial Applications and Implementation Issues of the Kalman Filter; and the IEEE TRANSACTIONS on SMART GRID Special Issue on Smart DC Distribution Systems. He was the chair of the Renewable Energy Systems Technical Committee of the IEEE Industrial Electronics Society. In 2014 he was awarded by Thomson Reuters as Highly Cited Researcher, and in 2015 he was elevated as IEEE Fellow for his contributions on "distributed power systems and microgrids."

Lin Xu received the Ph.D. degree in Electrical Engineering from Shanghai JiaoTong University (SJTU), Shanghai, China, in 2011. Currently, she is a Senior Engineering at Sichuan Electric Power Research Institute, State Grid Sichuan Electric Power Company, Chengdu, China. She has co-authored more than 20 journal and conference papers in the area of power electronics and power systems. Her research interests include power quality, power system analysis and real-time digital simulator (RTDS), flexible Ac transmission systems (FACTS), such as STATCOMs and power quality conditioners (DVRs, APFs). She is an active reviewer for IEEE Transactions on Industrial Electronics, IEEE Transactions on Power Electronics, Electric Power Components and Systems, etc.