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Modulation Schemes with Enhanced Switch Thermal Distribution for
Single-Phase AC-DC-AC Reduced-Switch Converters

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Abstract—Modulation schemes can significantly change the performance of a converter in the steady state. They have thus been extensively studied, but directed more at three-phase topologies, where triplen offsets are added. Single-phase systems, including ac-dc-ac, are less widely pursued, even though various topologies have since been proposed. The intention of this paper is thus to study two promising single-phase ac-dc-ac converters using reduced number of switches, and subsequently proposes modulation schemes for them. The proposed schemes help the converters achieve better thermal spread among their switches, while keeping their dc-link voltages low. Single points of failure are thus minimized, allowing the converters to have longer lifetimes. Simulation and experimental results have demonstrated the intended performances, hence verifying the analyses presented in the paper.

Index Terms—Thermal distribution, modulation scheme, single-phase converter, ac-dc-ac converter, reduced switch converter.
I. INTRODUCTION

Different modulation schemes applied to a converter are known to produce different performance features in terms of harmonics, power losses and maximum modulation indexes [1-8]. Despite their differences, most modulation schemes are, to a great extent, inter-related since they are derived from the same basic sine-triangle comparison, also known as carrier-based or sinusoidal pulse-width modulation (SPWM). The derivations are almost always done by adding a common offset to the modulating sine references used by the basic SPWM. This offset is usually of third-order or contains triplen harmonics in case of three-phase dc-ac or ac-dc conversion. Some examples mentioned in the literature are centered pulse-width modulation (PWM), 60°- and 30°-discontinuous PWM [3] [4] to name only a few. These schemes can alternatively be analyzed by using explicit space vectors [5] [6], which if implemented using built-in timers of digital signal processors, are not greatly different from sine-triangle comparison. Explicit space vector implementation will hence not be analyzed separately.

The same sine-triangle comparison and addition of common offset can also be applied to a single-phase dc-ac or ac-dc system, but are comparably less studied since the choices for offset are not plenty to begin with. Performance advantages expected from modifications of modulation for a single-phase system are therefore not as wide ranging as for a three-phase system. Although this is generally true, there may be an exception with single-phase ac-dc-ac systems implemented using topologies with lesser switches. Lesser switches in these topologies usually lead to interdependencies between their ac inputs and outputs, and hence a different set of performance requirements, which is presently not thoroughly discussed. It is thus chosen as the theme of this paper, but proposing modulation schemes for all possible ac-dc-ac topologies using lesser switches is nearly impossible since there are many invented over the past decades like in [9-20]. The focus has thus been narrowed to two six-switch ac-dc-ac converters.

The first is the promising B6 ac-dc-ac converter mentioned since year 2001 [9-11]. Its topological layout is no different from a three-phase six-switch converter with two switches per phase-leg, but not connected to a three-phase source or load. Instead, one phase-leg is tied to the single-phase ac input, and another is tied to the single-phase ac output. The last phase-leg is shared between the input and output as their respective return paths. Therefore, when compared with two full-bridge converters connected back-to-back, the B6 ac-dc-ac converter uses two lesser switches, while generating lower losses in some of the remaining switches. Losses in two switches will, in fact, drop to zero if the input and output ac currents are exactly equal. This is, no doubt, an advantage, but at the expense of losing independence between frequencies of the ac input and output. In other words, the input and output must have the same frequency, which although is restrictive, may not be a concern in applications like uninterruptible power supply (UPS) and power conditioner mentioned in [11]. Another demonstrated usage of the B6 ac-dc-ac converter is for decoupling power ripples with doubled line frequency.
commonly sensed with single-phase systems [12-16]. In this case, one set of ac terminals must be tied to an ac film capacitor for storing the power ripples.

Another topology with lesser switches investigated here is the six-switch ac-dc-ac converter proposed recently in [17-20], which conceptually, is a simplified single-phase version of the three-phase nine-switch converter proposed in [21-24]. Instead of having three phase-legs with two switches each, the six switches are now divided equally between two phase-legs sharing a common dc-link in parallel. Each phase-leg with three switches can then form two ac terminals per phase-leg. With two phase-legs, two upper ac terminals and two lower ac terminals are thus formed for connecting a source and a load. Moreover, with three switches per phase-leg, this second six-switch converter appears more like a full-bridge converter placed on top of another, rather than connected back-to-back. The upper two switches of the upper full-bridge and lower two switches of the lower full-bridge are retained, while the remaining four switches are merged to two. The total switches used are thus six, arranged equally along the vertical sides of a ‘H’. For convenience of referencing, this second six-switch topology will hence be referred to as the H6 ac-dc-ac converter, which has also been tested as a UPS, a power conditioner and a power decoupling converter [20] [23] [25].

The B6 and H6 converters are thus structurally different, even though they use the same number of switches, and face two similar concerns. The first concern is their higher dc-link voltages induced by improper modulation, and the second is their unequal thermal distribution among switches, especially with the H6 converter. The authors’ intention for the paper is thus to propose modulation schemes that can resolve both concerns for the converters, after studying their sources of problems. Simulation and experimental results obtained have validated the modulation concepts discussed.

II. B6 AC-DC-AC CONVERTER

A. Minimum DC-Link Voltage

Topology of the B6 converter is shown in Fig. 1, where a shared phase-leg between its input and output can clearly be seen. The purpose of the converter is to generate two single-phase voltages at its two ac terminals, whose normalized expressions with respect to half the dc-link voltage are notated as \(v_{ab}^*\) and \(v_{cb}^*\) and they are written as follows.

\[
v_{ab}^* = M_{ab}\sin(\omega_1 t), \quad v_{cb}^* = M_{cb}\sin(\omega_1 t + \varphi_1)
\]

where \(M_{ab}\) and \(M_{cb}\) are modulation indexes, \(\omega_1\) is the fundamental angular frequency, and \(\varphi_1\) is the phase difference between the two voltages. The simplest way of assigning modulating references to the three phase-legs will then probably be (2) with the shared phase-leg producing zero voltage with respect to the (virtual) midpoint of the dc-link.

\[
\text{Ref}_a = v_{ab}^*, \quad \text{Ref}_b = 0 \text{ and } \text{Ref}_c = v_{cb}^*
\]
Sine-triangle comparison using (2) can then be arranged like in Fig. 2 (a), if $\varphi_1$ is assumed to be zero. Alternatively, if the reference assignment is changed to (3), the sine-triangle comparison changes to Fig. 2 (b) with $\varphi_1 \equiv 0$ again assumed.

$$Ref_a^- = v_{ab}^* - 0.5M_{ab}, \quad Ref_b^- = -0.5M_{ab} \quad \text{and} \quad Ref_c^- = v_{cb}^* - 0.5M_{ab}, \quad \text{if} \quad Ref_a \geq 0, \quad M_{ab} \geq M_{cb} \quad \text{and} \quad \varphi_1 = 0$$

$$Ref_a^+ = v_{ab}^* + 0.5M_{ab}, \quad Ref_b^+ = 0.5M_{ab} \quad \text{and} \quad Ref_c^+ = v_{cb}^* + 0.5M_{ab}, \quad \text{if} \quad Ref_a < 0, \quad M_{ab} \geq M_{cb} \quad \text{and} \quad \varphi_1 = 0 \quad (3)$$

The triangular carrier drawn in Fig. 2 (b) is obviously smaller. Since the carrier peak usually represents the minimum dc-link voltage needed, the B6 converter modulated with (3) is undeniably more attractive, introduced by simply adding a common square offset with amplitude of $0.5M_{ab}$ to (2). This offset is however not universal, and is, in fact, only a simple non-optimized example included for illustration only. The ideal offset will change with $\varphi_1$ and the criteria defined for optimization. It will be addressed in the next subsection, where the criteria defined are to improve thermal distribution among switches of the B6 converter, while not compromising its minimum dc-link voltage. Here, the evaluation is directed more at finding the minimum carrier peak, which can more generally be determined after computing the third signal $v_{ac}^*$ expressed in (4) in terms of its magnitude $M_{ac}$ and phase $\varphi_2$.

$$v_{ac}^* = v_{ab}^* - v_{cb}^* = M_{ab}\sin(\omega_1 t) - M_{cb}\sin(\omega_1 t + \varphi_1) = M_{ac}\sin(\omega_1 t + \varphi_2)$$

$$M_{ac} = \sqrt{M_{ab}^2 + M_{cb}^2 - 2M_{ab}M_{cb}\cos\varphi_1} \quad (4)$$

The minimum carrier peak $M_{Tri,min}$ (or half normalized dc-link voltage) required is then given by (5).

$$M_{Tri} \geq M_{Tri,min} = \max(M_{ab}, M_{cb}, M_{ac})/2 \quad (5)$$

From (4) and (5), the largest minimum carrier peak in (6) will obviously be requested when $\varphi_1 = \pi$.

$$M_{Tri} \geq M_{ac}/2 = (M_{ab} + M_{cb})/2 \quad (6)$$
A simple square offset defined for showing this “$\varphi_1 = \pi$” case is added to (2), giving rise to those references in (7). Corresponding sine-triangle placement for demonstrating (7) is also drawn in Fig. 2 (c).

\[
\begin{align*}
\text{(a) References from (2) with } \varphi_1 &= 0 \\
\text{(b) References from (3) with } \varphi_1 &= 0 \\
\text{(c) References from (7) with } \varphi_1 &= \pi
\end{align*}
\]

Fig. 2. Different sine-triangle placements for modulating B6 converter.

B. Offset for Improving Thermal Distribution

As demonstrated earlier, adding of common offset provides a freedom for minimizing dc-link voltage needed by the B6 converter. Alternative or additional performance features can simultaneously be considered, which in this subsection, is targeted at improving thermal distribution of switches, while retaining minimum dc-link voltage expressed in (5). Before explaining the method, an assumption related to the input $i_a$ and output $i_c$ currents is clarified using their expressions in (8), defined in terms of their magnitudes $I_a$ and $I_c$, and phases $\theta$ and $\theta_1$.

\[
i_a = I_a \sin(\omega_1 t + \theta), \quad i_c = I_c \sin(\omega_1 t + \theta_1)
\]

These currents, according to Fig. 1, flow through different switches with $i_a$ flowing through either $S_1$ or $S_2$ of the non-shared input phase-leg and $i_c$ flowing through either $S_1$ or $S_5$ of the non-shared output phase-leg. Current through either $S_1$ or $S_5$ of the shared phase-leg is, on the other hand, given by (9), where $I_b$ and $\theta_2$ are again for representing magnitude and phase, respectively.

\[
i_b = i_a - i_c = I_a \sin(\omega_1 t + \theta) - I_c \sin(\omega_1 t + \theta_1) = I_b \sin(\omega_1 t + \theta_2)
\]

\[
I_b = \sqrt{I_a^2 + I_c^2 - 2 I_a I_c \cos(\Delta \theta)}, \quad \Delta \theta = \theta - \theta_1
\]
Based on (8) and (9), the assumption made for the B6 converter is \( I_b \leq \min(I_a, I_c) \). Otherwise, with a larger \( I_b \) flowing through the shared phase-leg, the incentive for using the B6 converter is greatly reduced when compared with two full-bridges connected back-to-back. Assuming \( I_b \leq \min(I_a, I_c) \) is thus reasonable, from which the permitted range of \( I_c \), in terms of \( I_a \), is determined as (10) after substituting the expression from (9). The range of \( I_c \) has also been shaded in Fig. 3, from which it can be seen that the maximum phase displacement \( \Delta \theta \) between \( i_a \) and \( i_c \) is \( \pi/3 \) when \( I_a = I_c \). This maximum \( \Delta \theta \) will reduce when the ratio between \( I_a \) and \( I_c \) moves away from unity, but must always remain within the shaded region in Fig. 3 to retain \( I_b \) as the smallest terminal current.

\[
I_b \leq \min(I_a, I_c) \Rightarrow \sqrt{I_a^2 + I_c^2 - 2I_aI_c\cos(\Delta \theta)} \leq \min(I_a, I_c)
\]

\[
\begin{align*}
&\text{if } I_c \leq I_a, \quad I_c \geq \frac{I_a}{2\cos(\Delta \theta)} \\
&\text{if } I_c > I_a, \quad I_c \leq 2I_a\cos(\Delta \theta)
\end{align*}
\]

(10)

Fig. 3. Range of \( I_c \) to ensure \( I_b \leq \min(I_a, I_c) \) in linear load condition.

With a smaller \( I_b \), conduction and switching losses of the shared phase-leg will then be comparably lower than those of the two non-shared phase-legs. Loss reduction through modulation changes should hence direct more at the two non-shared phase-legs, attempting to bring their losses closer to those of the shared phase-leg. The concepts involved can be explained using the simplest reference assignment defined in (2) and its sine-triangle arrangement drawn in Fig. 4 (a) for \( \varphi_1 \neq 0 \). In the figure, the carrier peak has been indicated as \( M_{tri} = M_{tri, min} + \Delta M_{SM} \), where \( \Delta M_{SM} \) is a small safety margin added for preventing over-modulation. Even so, the carrier in Fig. 4 (a) is still smaller than the references. Fig. 4 (a) is therefore not a practical possibility, but merely an illustrative example defined for finding the common offset to be added to (2). After adding the offset, all references will be confined within the carrier band, as illustrated later. Returning to Fig. 4 (a), its reference polarities allow each fundamental cycle to be divided into two categories, analyzed as follows.
**Category 1:** \((\text{Ref}_a \times \text{Ref}_c) \geq 0, \text{Ref}_b = 0\) from (2)

This category includes \((\text{Ref}_a, \text{Ref}_c \geq 0)\) and \((\text{Ref}_a, \text{Ref}_c \leq 0)\). For the former, it can be \(\text{Ref}_a \geq \text{Ref}_c \geq \text{Ref}_b = 0\) or \(\text{Ref}_c \geq \text{Ref}_a \geq \text{Ref}_b = 0\). Either case, the three references should be shifted up with the largest reference clamped to the positive carrier peak. This allows switching losses of a non-shared phase-leg to be removed. Shifting down to the negative carrier trough is also a possibility, but not encouraged since it removes switching losses from the shared phase-leg, which already has lower total losses. It is therefore recommended to clamp only the non-shared phase-legs so as to shrink their thermal differences with the shared phase-leg. The next two possible scenarios are \(\text{Ref}_a \leq \text{Ref}_c \leq \text{Ref}_b = 0\) and \(\text{Ref}_c \leq \text{Ref}_a \leq \text{Ref}_b = 0\), which in reverse, require the smallest reference of a non-shared phase-leg to be clamped to the negative carrier trough. Offset \(M_{B6,\text{off1}}\) needed for both directions of clamping can be obtained from (11), where \(\text{sgn}(\cdot)\) returns the polarity of the parameter enclosed by the parenthesis.

\[
M_{B6,\text{off1}} = \text{sgn}(\text{Ref}_a + \text{Ref}_c) \times \{M_{TRI} - \max(|\text{Ref}_a|,|\text{Ref}_c|)\} 
\]  

\(\text{Category 2: } (\text{Ref}_a \times \text{Ref}_c) < 0, \text{Ref}_b = 0\) from (2)

This category includes \((\text{Ref}_a < \text{Ref}_b = 0 < \text{Ref}_c)\) and \((\text{Ref}_c < \text{Ref}_b = 0 < \text{Ref}_a)\), which strictly, allow clamping to be done by either of the non-shared phase-legs. An additional criterion must therefore be introduced, which in terms of minimizing losses, should be to clamp the non-shared phase-leg which carries the largest current. The offset \(M_{B6,\text{off2}}\) required can then be defined as (12).

\[
M_{B6,\text{off2}} = \begin{cases} 
\text{sgn}(\text{Ref}_a) \times \{M_{TRI} - |\text{Ref}_a|\} & \text{if } |i_a| \geq |i_c| \\
\text{sgn}(\text{Ref}_c) \times \{M_{TRI} - |\text{Ref}_c|\} & \text{if } |i_a| < |i_c|
\end{cases} 
\]  

Combining the two categories, references needed for modulating the B6 ac-dc-ac converter with improved thermal distribution are given in (13). Its corresponding sine-triangle arrangement is shown in Fig. 4 (b), which clearly has all...
references confined within the carrier band. The figure also shows the reference clamping being not uniformly divided among the phase-legs, which is correct since the intention is to clamp only the non-shared phase-legs to lower their losses closer to those of the shared phase-leg. It is therefore directed at thermal distribution, rather than the usual discontinuous targets expected from a three-phase balanced system.

$$\text{Ref}_a = v_{ab}^* + M_{B6, off} \times \text{Ref}_b = M_{B6, off} \quad \text{and} \quad \text{Ref}_c = v_{cb}^* + M_{B6, off}$$

$$M_{B6, off} = \begin{cases} M_{B6, off1} & \text{if } (\text{Ref}_a \times \text{Ref}_c) \geq 0 \\ M_{B6, off2} & \text{if } (\text{Ref}_a \times \text{Ref}_c) < 0 \end{cases}$$  \hspace{1cm} (13)

In addition, it should be re-emphasized that the discontinuous expressions in (13) are formulated with $I_b$ considered as the smallest terminal current. As explained, this consideration should generally be true before the B6 converter is used to save switches without introducing additional stresses. If it cannot be ensured or where current cancellation cannot be effected because of harmonic currents at either the input or output terminal only (but not both), the modulation expression in (11) must be modified accordingly to give (14).

$$M_{B6, off1} = \begin{cases} \text{sgn}(\text{Ref}_a + \text{Ref}_c) \times \{M_{T, tri} - |\text{Ref}_a|\} & \text{if } |\text{Ref}_a| \geq |\text{Ref}_c| \text{ and } |i_a| \geq |i_b| \\ \text{sgn}(\text{Ref}_a + \text{Ref}_c) \times \{M_{T, tri} - |\text{Ref}_c|\} & \text{if } |\text{Ref}_a| < |\text{Ref}_c| \text{ and } |i_c| \geq |i_b| \\ -\text{sgn}(\text{Ref}_a + \text{Ref}_c) \times M_{T, tri} & \text{otherwise} \end{cases}$$  \hspace{1cm} (14)

In effect, (14) performs the same task as (11), but will additionally consider the common return current $i_b$. For example, consider the case of $\text{Ref}_a \geq \text{Ref}_c \geq \text{Ref}_b = 0$, (11) will clamp the non-shared phase-leg associated with $\text{Ref}_a$ to the upper dc rail. The same clamping will be demanded by (14) if $|i_a| \geq |i_b|$. Else, (14) will request for the shared phase-leg to be clamped to the (opposite) lower dc rail to reduce its stresses caused by a larger $i_b$. The proposed discontinuous scheme will therefore still function well so long as (11) is replaced by (14). Modification to (12) for category 2 is however not required because $\text{Ref}_b$ for the shared phase-leg is always between the other two references, and hence cannot be clamped to any of the dc rails.

### III. H6 AC-DC-AC CONVERTER

#### A. Minimum DC-Link Voltage

The H6 ac-dc-ac converter is shown in Fig. 5, where instead of only two switches, each phase-leg has three switches for forming an upper and a lower ac terminal. With two three-switch phase-legs, the ac source can then be connected to the two upper terminals, while the load can be connected to the two lower terminals. Interchanging the source and load positions is possible, but will not affect the modulation principles discussed later. Returning to the three-switch phase-leg, its switching is constrained such that at any time, only two switches are conducting. The number of switch combinations is hence limited to three in total. They are $SA1 = SA2 = \text{ON}$ to give $v_U = v_D = 0.5V_{dc}$, $SA1 = SA3 = \text{ON}$ to give $v_U = 0.5V_{dc}$ and...
$v_D = -0.5V_{dc}$, and $SA2 = SA3 = ON$ to give $v_U = v_D = -0.5V_{dc}$, where $v_U$ and $v_D$ are potentials of nodes $U$ and $D$ in Fig. 5 with respect to the virtual dc-link midpoint. The constraint faced by the three-switch phase-leg is thus its inability to produce $v_U = -0.5V_{dc}$ and $v_D = 0.5V_{dc}$ simultaneously.

In terms of carrier-based modulation, the constraint can be avoided by always placing modulating reference of the upper terminal above that of the lower terminal from the same phase-leg. In other words, the two references must not cross each other like shown in Fig. 6 (a), where they marginally touch each other for demonstrating the closest they can be placed. Even so, the carrier peak must be larger than the largest reference peak among the two references per phase-leg. It is therefore obvious that the minimum dc-link voltage demanded by the H6 converter is larger than that of a normal full-bridge converter. The carrier peak will only be equal to the largest reference peak when the phase shift between the two references per phase-leg is zero like drawn in Fig. 6 (b) [18]. The minimum carrier peak (or half normalized dc-link voltage) expected from the H6 converter is thus $M_{Tri,min} = max(M_U, M_D) = 0.5max(M_{UU}, M_{DD})$, if the modulating references used for the two phase-legs are defined in accordance to (15), where $M_U$, $M_D$, $M_{UU}$ and $M_{DD}$ are the corresponding reference magnitudes. This is also the minimum carrier peak required by a normal full-bridge converter when modulated with the same operating conditions.
First phase-leg: \( Ref_U = M_U sin(\omega_1 t) + M_{DC,U}, \) \( Ref_D = M_D sin(\omega_1 t + \phi_1) + M_{DC,D} \)

Second phase-leg: \( Ref_{U'} = -M_U sin(\omega_1 t) + M_{DC,U}, \) \( Ref_{D'} = -M_D sin(\omega_1 t + \phi_1) + M_{DC,D} \)

Normalized upper ac voltage: \( v_{uu'}^* = M_{uu'} sin(\omega_1 t) = 2M_U sin(\omega_1 t) \)

Normalized lower ac voltage: \( v_{dd'}^* = M_{dd'} sin(\omega_1 t + \phi_1) = 2M_D sin(\omega_1 t + \phi_1) \) (15)

where \( M_{DC,U} \) and \( M_{DC,D} \) are dc offsets added for ensuring that the upper reference is always above the lower reference from the same phase-leg.

B. Offset for Improving Thermal Distribution

To understand loss distribution in a phase-leg of the H6 converter, Fig. 7 is referred to, where a typical state sequence within half a carrier period has explicitly been drawn. Using terminal current notations indicated in Fig. 5, individual switch currents flowing down the phase-leg have also been derived and summarized in Fig. 7. These expressions and state sequence have indicated that \( SA1 \) and \( SA3 \) switch only one terminal current each at the end of time interval \( T_1 \) and start of interval \( T_3 \), respectively. Their switching losses are hence not greatly different from those expected from a full-bridge converter. The same is however not true for \( SA2 \), which switches twice per half carrier period even though each switching involves only one terminal current. Conduction losses of \( SA2 \) are also expected to be higher especially when \( T_1 \) and \( T_3 \) are lengthened by low modulation indexes or intentionally shifting the two references per phase-leg closer to the middle of the carrier band. Conduction losses of \( SA1 \) and \( SA3 \) are, on the other hand, much reduced especially when condition (16) regarding terminal currents \( i_U \) and \( i_D \) with magnitudes \( I_U \) and \( I_D \) is satisfied. Current \( |i_U - i_D| \) through \( SA3 \) during \( T_1 \) and
SA1 during $T_3$ will then be smaller, approaching zero when $i_U = i_D$.

$$i_u = I_u \sin(\omega_1 t + \theta), i_d = I_d \sin(\omega_1 t + \theta_1)$$

$$|i_u - i_d| = \sqrt{I_u^2 + I_d^2 - 2I_u I_d \cos(\Delta \theta)} \leq \min(I_u, I_d), \Delta \theta = \theta - \theta_1$$  \hspace{1cm} (16)

Switch SA2 will therefore heat up more because of its higher switching and conduction losses when modulation scheme shown in Fig. 6 is used [8]. To spread some of its losses to SA1 and SA3, the insight drawn is to shorten $T_1$ and $T_3$ by adding two modulating offsets, which is one more than the B6 converter. The B6 converter has only one common offset for its input and output because of their shared terminal. The same however does not apply to the H6 converter, whose input and output terminals are not shared even though their modulating references are restricted by some magnitude and phase constraints. The H6 converter can therefore have two separate modulating offsets with one for reducing $T_1$ by shifting the upper modulating references towards the positive carrier peak and another for reducing $T_3$ by shifting the lower modulating references towards the negative carrier trough. Ideally, the shifting should minimize $T_1$, $T_3$ or both to zero, which in other words, means there will be some discontinuous clamping in each fundamental cycle. The clamping can be done by adding offsets to (15), giving rise to those modified references in (17).

First phase-leg: $Ref_u^{'p} = Ref_u + M_{H6,off,UP}$, $Ref_d^{'p} = Ref_d + M_{H6,off,DN}$

Second phase-leg: $Ref_u^{'p} = Ref_u^{'p} + M_{H6,off,UP}$, $Ref_d^{'p} = Ref_d^{'p} + M_{H6,off,DN}$

$$M_{H6,off,UP} = \begin{cases} M_{Tri} - Ref_u & \text{when } Ref_u \geq 0 \\ M_{Tri} + Ref_u & \text{when } Ref_u < 0 \end{cases}$$

$$M_{H6,off,DN} = \begin{cases} -M_{Tri} + Ref_d & \text{when } Ref_d \geq 0 \\ -M_{Tri} - Ref_d & \text{when } Ref_d < 0 \end{cases}$$

$$M_{Tri} = M_{Tri,min} + \Delta M_{SM}$$  \hspace{1cm} (17)

Pictorially, for those initial references shown in Fig. 6 (b) with $\Delta M_{SM} = 0$, applying (17) leads to Fig. 8, where the minimum carrier peak and hence required dc-link voltage remain unchanged (references for the second phase-leg of the H6 converter are also shown in the figure). Unlike Fig. 6 (b) where the phase shift $\phi_1$ must be zero, Fig. 8 is drawn with a non-zero $\phi_1$, whose value can be raised until its two references touch each other. This happens when $Ref_u^{'p} = Ref_d^{'p}$, which when simplified, leads to the expression in (18).

$$M_{Tri} + 2Ref_u = -M_{Tri} + 2Ref_d \Rightarrow \sqrt{M_{D}^2 + M_{U}^2 - 2M_{D} M_{U} \cos(\phi_1)} = M_{Tri}$$  \hspace{1cm} (18)

Assuming the simple example of $M_U = M_D$ and $M_{Tri} = M_{Tri,min} = M_U$ or $\Delta M_{SM} = 0$, (18) then gives the maximum phase shift as $\phi_1 = \pi/3$ or $60^\circ$, which is a sizable value compared to zero in Fig. 6 (b). Other maximum phase-shift values larger than $60^\circ$ can be read from Fig. 9, depending on the $M_U$ and $M_D$ values specified. Advantages of the proposed scheme
represented by (17) can therefore be summarized as improved thermal distribution among switches and lengthened phase-shift range, while retaining the minimum dc-link voltage represented by carrier peak $M_{Trl, min}$. This minimum dc-link voltage is the same as that demanded by the B6 converter discussed in Section II. It is also the same voltage demanded by the classical full-bridge converter, which is certainly encouraged since the saving in switches is not accompanied by prominent tradeoffs.

![Discontinuous Sine-Triangle Placement](image)

Fig. 8. Discontinuous sine-triangle placement obtained from (17) for modulating H6 converter ($\phi_1$ not necessary at zero).

![Maximum Output](image)

Fig. 9. Maximum $\phi_1$ that H6 ac-dc-ac converter can produce using minimum dc-link voltage.

**IV. SIMULATION AND EXPERIMENTAL RESULTS**

Simulations for both B6 and H6 ac-dc-ac converters are performed using common parameters listed in Table I. The same parameters have also been used experimentally for testing the implemented B6 and H6 prototypes. As for calculation of
losses\(^1\), the PLECS simulation software has a feature for performing it after creating a custom look-up table based on parameters of the switch [27] (chosen similar to the IXGH30N120B3D1 switch from IXYS used in the experiments [26]). On the other hand, for the experiments, a DPO3014 digital phosphor oscilloscope, a P5200 voltage probe and a TCP0030 current probe have been used for measuring voltage and current of each switch with a sampling rate of 250 MS/s. Thus, for each 100-ns to 200-ns turn-on or turn-off transition [26], there are 25 to 50 samples for calculating the switching loss of the switch. The main concern here is different time delays of the current and voltage probes, which according to [28] and [29], are 14.5 ns and 20 ns, respectively. These delays will, no doubt, shift the \( \frac{dv}{dt} \) and \( \frac{di}{dt} \) transitions differently, and must hence be compensated by adding appropriate time advancements. In contrast, conduction loss of the switch is less affected by these constraints, and hence more easily computed from the sampled data. It should nonetheless be mentioned that this method of computation is not highly accurate, but is definitely sufficient for demonstrating relative differences in losses between the discussed modulation methods. The obtained results are described as follows.

A. B6 Converter

Fig. 10 (a) shows the modulating references, switched voltages and terminal currents generated by (2). The modulating references obviously match those shown in Fig. 2 (a), except with \( \varphi_1 \) set to \( \pi/4 \) instead of zero. The minimum dc-link voltage needed in this case must hence be doubled. The dc-link voltage is actually raised to 340 V with a small safety margin included for avoiding over-modulation, instead of the 190 V given in Table I. Its accompanied losses are computed and tabulated in Fig. 11 (a), where the shared phase-leg producing lower losses can clearly be seen. With the converter next modulated by the proposed scheme given in (13), the modulating references and switched voltages change to those shown in Fig. 10 (b), where discontinuous clamping can clearly be seen. However, instead of clamping the three phase-legs uniformly, clamping is done only by the two non-shared phase-legs since their losses are higher than those of the shared phase-leg. Moreover, when in intervals classified as Category 2 and explained in Subsection II(B), clamping is clearly imposed on the non-shared phase-leg carrying the larger current to bring down the overall converter losses even more.

Losses generated by the B6 converter with the proposed discontinuous scheme are subsequently computed and tabulated in Fig. 11 (b), which when compared with Fig. 11 (a), are obviously lower. These lower losses are obtained without raising the carrier frequency for the proposed discontinuous scheme, which unlike conventional three-phase discontinuous schemes, has a shared phase-leg which switches continuously. Raising the carrier frequency will hence increase losses of this phase-leg, which ideally, should be avoided. Other than lower total losses, Fig. 11 (b) also shows that the difference in losses between the shared and non-shared phase-legs is smaller than that in Fig. 11 (a). This is, no doubt, the expected outcome since the proposed scheme only clamps the non-shared phase-legs with higher losses, and not the shared phase-leg

\(^1\) Formulas for calculating switch losses analytically can be deduced from [8].
with lower losses.

Experimentally obtained results for demonstrating the converter performance are provided in Fig. 12 and Fig. 13. These results match well with those from simulations, which collectively, verify the discontinuous scheme proposed for the B6 ac–dc–ac converter. More experimental results are given in Fig. 14, where spectra of terminal current $i_a$ are plotted for the continuous and discontinuous schemes. As seen, discontinuous modulation produces a better spectrum with smaller spectral content around the switching frequency. This is due to its lower dc-link voltage mentioned at the beginning of the subsection, which certainly is another advantage of the proposed discontinuous scheme.

**TABLE I**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-link voltage</td>
<td>190 V (unless stated otherwise)</td>
</tr>
<tr>
<td>Input voltage $v_{ab}$ or $v_{UU'}$</td>
<td>110 V (RMS)</td>
</tr>
<tr>
<td>Output voltage $v_{cb}$ or $v_{DD'}$</td>
<td>110 V (RMS) (Resistive load)</td>
</tr>
<tr>
<td>Phase shift $\varphi_I$</td>
<td>$\pi/4$</td>
</tr>
<tr>
<td>Carrier frequency $f_s$</td>
<td>10 kHz</td>
</tr>
<tr>
<td>Nominal power</td>
<td>800 W</td>
</tr>
<tr>
<td>AC filter inductor</td>
<td>4.1 mH</td>
</tr>
<tr>
<td>Insulated gate bipolar transistor</td>
<td>IXGH30N120B3D1</td>
</tr>
</tbody>
</table>

(a) Continuous scheme (2) with $V_{dc} = 340$ V  
(b) Discontinuous scheme (13) with $V_{dc} = 190$ V

Fig. 10. Modulating references, switched voltages and terminal currents of B6 converter simulated with different modulation schemes.
Fig. 11. Simulated loss distributions of B6 ac-dc-ac converter when modulated by (a) continuous scheme in (2) and (b) discontinuous scheme in (13).

Fig. 12. Experimental switched voltages and terminal current of B6 converter driven by different modulation schemes.

(a) Continuous scheme (2) with $V_{dc} = 340$ V  (b) Discontinuous scheme (13) with $V_{dc} = 190$ V

Fig. 13. Experimental loss distributions of B6 ac-dc-ac converter when modulated by (a) continuous scheme in (2) and (b) discontinuous scheme in (13).
B. **H6 Converter**

Corresponding results obtained with the H6 ac-dc-ac converter using parameters tabulated in Table I are shown in Fig. 15 and Fig. 16. Fig. 15 (a) shows its modulating references, switched voltages and terminal currents obtained when modulated using those continuous reference expressions given in (15) and drawn in Fig. 6 (a) \( \varphi_1 \) in this case is \( \pi/4 \). The dc-link voltage needed by the H6 converter must then be raised to 240 V with a small safety margin included for avoiding over-modulation. The resulting losses generated by switches in a phase-leg are computed and plotted in Fig. 16 (a), which clearly shows the middle switch \( SA_2 \) stressed more. The difference in stress experienced by \( SA_2 \) will be even greater when the two terminal currents \( i_o \) and \( i_o \) per phase-leg in Fig. 5 are exactly the same. This is however not the case in Fig. 16 (a), where phase-shift between the currents is noted to be \( \approx \pi/4 \).

Now, with the H6 converter modulated by the proposed discontinuous scheme in (17), its modulating references and switched voltages change to those shown in Fig. 15 (b), where four distinct intervals per fundamental cycle can clearly be seen. Beginning from the vertical axis, the first interval noted does not have any clamping, and is hence not greatly different from the earlier mentioned continuous scheme. The second interval has \( SA_1 \) clamped to the upper dc rail, and hence \( T_1 \) in Fig. 7 reduces to zero. The remaining \( SA_2 \) and \( SA_3 \) then switch in complement like in a standard two-switch phase-leg with \( SA_2 \) no longer switching twice per half carrier period. Moreover, since \( i_o \) in Fig. 5 during this interval is positive, it flows through the anti-parallel diode of \( SA_1 \) rather than its transistor. The amount of switching losses reduced will hence be smaller than the next two intervals.

The third interval followed in Fig. 15 (b) has both \( SA_1 \) clamped to the upper dc rail and \( SA_3 \) clamped to the lower dc rail.
to reduce both $T_1$ and $T_3$ to zero. Switch $SA2$ in this interval is therefore always turned off with no switching and conduction losses. The last interval in Fig. 15 (b) eventually has only $SA3$ tied to the lower dc rail, while current $i_D$ in Fig. 5 is negative. Current $i_D$ therefore flows through the transistor of $SA3$, and not its antiparallel diode. Reduction of switching losses of $SA3$ in this last interval will therefore be more prominent than that of $SA1$ in the second interval. The remaining $SA1$ and $SA2$ in the last interval will then switch in complement like in a standard two-switch phase-leg with $SA2$ no longer commutating twice per half carrier period. Summarizing the four intervals, the heating stress of $SA2$ will be brought down significantly, as demonstrated by individual switch losses plotted in Fig. 16 (b) for the proposed discontinuous scheme. This is in addition to the lower dc-link voltage of 190 V needed, and bigger phase-shift $\varphi_1$ permitted between the two modulating references per phase-leg.

Experimentally obtained results for the H6 converter are provided in Fig. 17 and Fig. 18. These results match well with those from simulations, and hence verifying the practicality of the proposed discontinuous scheme for H6 ac-dc-ac converter. Experimental spectra of current $i_U$ from the H6 converter are also plotted for both continuous and discontinuous schemes, as shown in Fig. 19. The discontinuous scheme, in general, has higher sideband harmonics around the switching frequency, but much lower harmonics around the doubled switching frequency. Its spectral performance is therefore not compromised greatly by the reference clamping introduced for better thermal distribution.

![Fig. 15. Modulating references, switched voltages and terminal currents of H6 converter simulated with different modulation schemes.](image-url)
Fig. 16. Simulated loss distributions of H6 ac-dc-ac converter when modulated by (a) continuous scheme in (15) and (b) discontinuous scheme in (17).

Fig. 17. Experimental switched voltages and terminal currents of H6 converter driven by different modulation schemes.

Fig. 18. Experimental loss distributions of H6 ac-dc-ac converter when modulated by (a) continuous scheme in (15) and (b) discontinuous scheme in (17).
(a) Continuous scheme (15) with $V_{dc} = 240$ V  
(b) Discontinuous scheme (17) with $V_{dc} = 190$ V

Fig. 19. Experimental spectrum of current $i_U$ of H6 ac-dc-ac converter driven by different modulation schemes.

V. CONCLUSION

This paper analyzes constraints and performance characteristics inherited by the B6 and H6 single-phase ac-dc-ac converters using reduced switches. The understanding gained is then used to develop discontinuous modulation schemes for the converters with the common purpose being to better spread losses among their switches, while keeping their dc-link voltage low. Simulation and experimental results obtained have validated these expectations, and have demonstrated certain unique features of the schemes. For the B6 converter, it has been demonstrated that discontinuous clamping is performed by only the two non-shared phase-legs, rather than distributed evenly among the phase-legs like in a three-phase system. The H6 converter, on the other hand, has four distinct intervals created per fundamental period with three of them having discontinuous clamping for lowering stresses of the middle switch. Better thermal distributions are therefore experienced by the two converters in accordance to the theme of the paper.

REFERENCES


[29] Tektronix P5200,