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Abstract

The moving average filter (MAF) is widely utilized to improve the disturbance rejection capability of the phase-locked loops (PLLs), which is of vital significance for the grid-integration and stable operation of power electronic converters to the electric power systems. However, the open-loop bandwidth is drastically reduced after incorporating MAF into the PLL structure, which makes the dynamic response sluggish. To overcome this shortcoming, some new techniques were proposed recently to improve the transient response of MAF-based PLLs. In this paper, a comprehensive performance comparison among the advanced MAF-based PLL algorithms is presented, which includes HPLL, MPLC-PLL, QT1-PLL, and DMAF-PLL. Various grid voltage disturbance scenarios, such as grid voltage sag, voltage flicker, and harmonics distortion, phase-angle and frequency jumps, DC offsets and noise, are considered to experimentally test the dynamic performances of these PLL algorithms. Finally, an improved positive sequence extraction method for HPLL under frequency jumps scenario is presented to compensate the steady-state error caused by the non-frequency adaptive DSC, and a satisfactory performance has been achieved.

Key words: Grid-synchronization, moving average filter (MAF), phase-locked loop (PLL), transient response.

I. INTRODUCTION

Three-phase phase-locked loop (PLL) technique is widely used for the accurate estimation of phase-angle, frequency, and sequence components extraction of grid voltages in power systems, which is crucial for the grid-integration of the distributed generation (DG) systems, such as wind, PV, and flexible ac transmission systems (FACTS), and active power filters (APFs) [1-3]. However, a great challenge associated with the PLLs is the accurate and fast estimation of phase angle and frequency under adverse grid voltage disturbance scenarios. According to European standard EN50160, the

typical voltage disturbance scenarios include voltage sag, flicker, and harmonics distortion, phase-angle and frequency jumps, dc offsets and noise contaminations [4]. In order to achieve the purpose of accurate grid-synchronization under various grid disturbance scenarios, several new structures to enhance the performance of the PLL have been presented [5-14].

In addition to the use of these new structures, a more general approach to improve the performance of a PLL is to combine with the filters [15-36], such as the extended Kalman filters (EKFs) [15], the space vector filters (SVFs) [16], the notch filters [17], the digital filters [18], the complex-coefficient filter (CCF) [19], the delayed signal cancellation (DSC) block [20-24], and the MAF-based methods [25-36]. Among these filtering techniques, the DSC and the MAF show the similar filtering characteristic, which can almost block the specific frequency signal completely. From the view point of the discrete implementation of the DSC and MAF, they are both composed of some particular delay blocks. However, the DSC is often used to improve the

performance of the PLL under adverse grid conditions [23]. And in [24], a comparison of the MAF and DSC, as well as their derived methods, was presented from the aspects of dynamic response, steady-state performance, required data size, and harmonic and noise immunity ability. In [25], the dqCDSC-PLL and the MAF-PLL algorithms were proved to be mathematically equivalent under certain conditions.

The MAF technique is most popular and widely used technique (can be used in natural *abc* coordinates, *αβ* coordinates and *dq* coordinates) owing to its simple digital realization, low computational burden, and effectiveness under grid disturbance conditions [26]. However, the open-loop bandwidth of the PLL is drastically reduced after incorporating MAF into its structure, which may be beneficial for the stability, but degrades the dynamic performance of the PLL. To solve this problem, some advanced MAF-based PLL algorithms are presented recently [27-36].

In [26], the detailed analysis and design guideline of the MAF-PLL and its frequency adaptive implementation were presented, in which the performance comparison of the well-tuned MAF-based PLL with PI controller and the PID controller was presented. It was shown that the PID-type MAF-PLL has a higher bandwidth which means a faster dynamic response while decreasing the noise immunity and disturbance rejection capability, and in [27] a critical comparison among the PLL and FLL based on the MAF, CDSC and DSOGI filtering techniques was presented. It is shown that these kinds of filtering techniques all can effectively remove the noise, harmonic and negative sequence which the initial phase angle detector with MAF-based PLL shows the best performance under frequency and phase angle jump scenarios. A novel MAF-based PLL consists of a frequency detector and an initial phase was presented in [28], in which the effect of discrete sampling on MAF is analyzed and a linear interpolation is employed to enhance the performances of the MAF. And in [29], an enhanced MAF (EMAF) algorithm was presented, which shows superior performance in terms of response time, transient overshoot, computational load, harmonic and noise immunity compared with the DSC algorithm.

In [30], a MAF and a weighted least squares estimation (WLSE) scheme based PLL was proposed, in which the MAF was used to filter out all the odd-order harmonics and help the WLSE to detect the fundamental positive-sequence components accurately even under heavily distorted grid conditions. In [31], the MAF was used as a perfiltering stage in the *dq*-frame (PMAF-PLL) to remove the negative sequence and odd-order harmonic components, and then an enhanced method was proposed to improve the steady-state performance under frequency varying conditions. Furthermore, the small-signal model of the PMAF-PLL was

presented and it has been proved that the PMAF-PLL and space-vector Fourier transform- based PLL (SVFT-PLL) are theoretically equivalent, and in [32], a novel design of low-gain PLL with introducing an adaptive MAF before the loop-filter (LF) and its discrete domain model was presented. Compared with the conventional high gain SRF-PLL, the phase and voltage frequency error is reduced and the phase angle tracking is faster and more accurate.

In [33], a quasi-type-1 PLL (QT1-PLL) was presented. In this structure, the proportional integral (PI) controller was replaced by a simple gain, thus, a larger open-loop bandwidth can be realized. However, QT1-PLL cannot filter out the dc offset and even order harmonics. In order to tackle this problem, hybrid PLL (HPLL) was presented in [34]. In HPLL, the delayed signal cancellation (DSC) is used in the *αβ* axis to eliminate the dc offset and even order harmonics. The phase error compensation (PEC) method was adopted for QT1-PLL and HPLL to achieve zero steady-state error when frequency jump occurs. In [35], the MAF-PLL with a phase-lead compensator (MPLC-PLL) was presented. With the phase-lead compensator in the control loop, the dynamic response of the standard MAF-PLL can be effectively improved without deteriorating its disturbance rejection capabilities. A differential MAF-PLL (DMAF-PLL) was presented in [36]. Under this approach, a special loop filter structure was used to eliminate the negative sequence 2nd order harmonics in order to reduce the window length of the MAF and significantly improves the dynamic performance of the PLL.

The main objective of this paper is to provide performance evaluations (including the transient response and disturbance rejection capabilities) of the four MAF-based PLLs (QT1-PLL, HPLL, MPLC-PLL, and DMAF-PLL) by analytical comparison and experimental results. The steady-state and dynamic performance of these algorithms are compared in terms of settling time, phase tracking error and overshoots. Experimental results show that the QT1-PLL and MPLC-PLL lack the rejection capabilities of dc offset and even order harmonics, which are the shortcomings of these algorithms, and it can be overcome by employing the DSC in the *αβ* coordinates or MAF in the *abc* coordinates. In the last Section, the amplitude error compensation (AEC) method is proposed to achieve zero steady-state error for the positive sequence amplitude estimation under frequency jump scenario. The extensive experimental results are provided for validation, which facilitates the practical application of these MAF-based PLLs to achieve an accurate grid-synchronization for the three-phase grid-connected PWM inverters and the distributed generators (DGs) in smart grid.

II.   OVERVIEW OF THE MAF-BASED PLLS

In this Section, a brief overview of MAF is outlined, and four MAF-based PLL algorithms and discrete models are

described.

A. Moving Average Filter (MAF)

The transfer function of MAF can be simply obtained in s-domain and z-domain as [19]

$$G_{MAF}(s) = \frac{\bar{x}(s)}{x(s)} = \frac{1-e^{-T_\omega s}}{T_\omega s} \approx \frac{2}{T_\omega s + 2} \quad (1)$$

$$G_{MAF}(z) = \frac{\bar{x}(z)}{x(z)} = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} \quad (2)$$

where T_ω represents the window length, and $T_\omega = NT_s$, T_s is the sample time and is set to be 0.0001 s, and N is an integer. The transfer function (1) shows that MAF requires a time equals to its window length to gather the data and reach the steady-state conditions. Therefore, a smaller window length would result in a faster dynamic response of the MAF-based PLL algorithms.

As shown in (2), the application of the MAF in z-domain computationally efficient with simple delay blocks [26], which is shown in Fig. 1. From the aforementioned analysis, the delay factor N can be set to be a constant to remove the fix frequency signal or to be frequency adaptive according to the equation $N = round(m\pi/\omega_0 T_s)$, in which the MAF is used to remove the odd-order harmonic for $m=1$, and the MAF is used to remove the dc offset for $m=2$. The detailed discrete-time realization was discussed in [26].

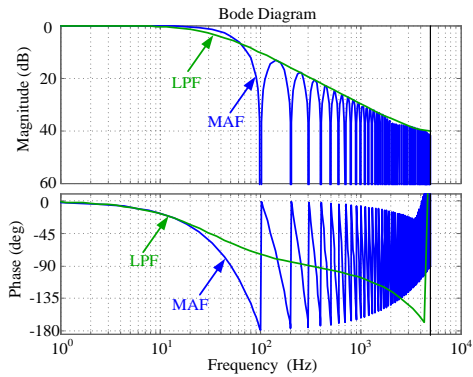Fig. 1. The realization of MAF in z-domain.

Fig. 2. Bode diagram comparison of MAF and first-order LPF.

Using the transfer functions (1) and (2), the bode diagram of MAF and low-pass filter (LPF) is shown in Fig. 2, in which T_ω is set to be 0.01 s ($N=100$) and the corresponding cutoff frequency in LPF is 200 rad/s. It shows that the even order harmonics are eliminated effectively since the MAF has a high attenuation at these harmonic frequencies.
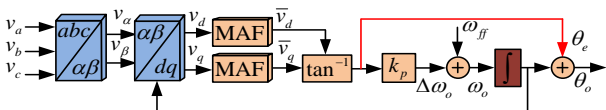
B. QT1-PLL

Fig. 3. Block diagram of the QT1-PLL proposed in [33].

Fig. 3 shows the general structure of the QT1-PLL, in which a MAF cascading a proportional controller act as the loop filter. Thus, from the view point of the structure, the QT1-PLL is a type-I PLL, which has a high stability margin compared with the typical MAF-PLL (in which a MAF and a PI controller act as the loop filter). However, the main disadvantage of a conventional type-I PLL lies on the phase tracking error under grid frequency step condition.

As shown in Fig. 3, the three-phase grid voltages with dc offset and harmonics can be defined as (here, the symmetrical load is taken into consideration, which corresponding to the -5th, $+7^{th}$, -11th, and $+13^{th}$ order harmonics)

$$\begin{cases} v_a = V_{a,dc} + \sum_{h=1,-5,7...} [V_h^+ \cos(\theta_h^+) + V_h^- \cos(\theta_h^-)] \\ v_b = V_{b,dc} \sum_{h=1,-5,7...} [V_h^+ \cos(\theta_h^+ - \frac{2\pi}{3}) + V_h^- \cos(\theta_h^- + \frac{2\pi}{3})] \\ v_c = V_{c,dc} + \sum_{h=1,-5,7...} [V_h^+ \cos(\theta_h^+ + \frac{2\pi}{3}) + V_h^- \cos(\theta_h^- - \frac{2\pi}{3})] \end{cases} \quad (3)$$

where V_h^+ (V_h^-) and θ_h^+ (θ_h^-) are the amplitude and the phase-angle of the hth harmonic components of the positive-(negative-) sequence of the input voltages, respectively. $V_{a,dc}$, $V_{b,dc}$ and $V_{c,dc}$ are the dc offset added into the phase-a, phase-b and phase-c voltage, respectively.

Applying the Clarke transformation to (3), v_α and v_β can be written as

$$\begin{cases} v_\alpha = V_{\alpha,dc} + \sum_{h=1,-5,7...} [V_h^+ \cos(\theta_h^+) + V_h^- \cos(\theta_h^-)] \\ v_\beta = V_{\beta,dc} + \sum_{h=1,-5,7...} [V_h^+ \sin(\theta_h^+) - V_h^- \sin(\theta_h^-)] \end{cases} \quad (4)$$

$$\begin{cases} V_{\alpha,dc} = (V_{a,dc} - 0.5V_{b,dc} - 0.5V_{c,dc}) \\ V_{\beta,dc} = \frac{\sqrt{3}}{2}(V_{b,dc} - V_{c,dc}) \end{cases} \quad (5)$$

Then, applying the Park transformation to (4), v_d and v_q can be written as

$$\begin{cases} v_d = g(\theta_0') + \sum_{h=1,-5,7...} [V_h^+ \cos(\theta_h^+ - \theta_0') + V_h^- \cos(\theta_h^- + \theta')] \\ v_q = h(\theta_0') + \sum_{h=1,-5,7...} [V_h^+ \sin(\theta_h^+ - \theta_0') - V_h^- \sin(\theta_h^- + \theta')] \end{cases} \quad (6)$$

where the $g(\theta_0)$ and $h(\theta_0)$ are the oscillating term caused by the grid voltage dc offset, where

$$\begin{cases} g(\theta_0') = V_{\alpha,dc}\cos(\theta_0') + V_{\beta,dc}\sin(\theta_0') \\ h(\theta_0') = -V_{\alpha,dc}\sin(\theta_0') + V_{\beta,dc}\cos(\theta_0') \end{cases} \quad (7)$$

Under quasi-locked condition ($\theta_1^+ = \theta_0$), (6) can be rewritten

$$\begin{cases} v_d = V_1^+ + f(\omega_n, 2\omega_n, 6\omega_n...) \\ v_q = V_1^+(\theta_1^+ - \theta_0') + f(\omega_n, 2\omega_n, 6\omega_n...) \end{cases} \quad (8)$$

where ω_n is the fundamental angular frequency. Through the use of MAF, the oscillating term $f(\omega_n, 2\omega_n, 6\omega_n...)$ can be almost removed. As mentioned earlier, a type-I PLL cannot achieve zero steady-state error when the frequency jump

occurs. Hence the phase tracking error of a type-I PLL under frequency jump is expressed as [33]

$$\theta_e = \frac{\Delta\omega_i}{k_p} \tag{9}$$

From equation (9), by selecting a sufficient high value for k_p, the phase error θ_e can be reduced to a very small value. However, this selection will increase the PLL's bandwidth remarkably which is not preferred under the distorted and unbalanced grid voltage condition. Notice that the average value of $\Delta\omega_o$ is equal to $\Delta\omega_i$ under the locked conditions. Thus, as highlighted in Fig. 3, the phase tracking error is added to output of the PLL to realize zero steady-state tracking error when frequency jump occurs.
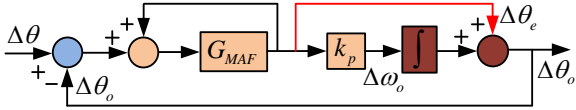

Fig. 4. Small-signal model of the QT1-PLL [33].

Fig. 4 shows the small signal model of the QT1-PLL. Since the s-domain transfer function has been expressed in [33], and considering the practical application, the open-loop transfer function in z-domain is expressed as:

$$G_{ol}^{QT1}(z) = \left(\frac{G_{MAF}(z)}{1 - G_{MAF}(z)} \right) \left(\frac{z - 1 + T_s k_p}{z - 1} \right) \tag{10}$$

As shown in (8), the lowest oscillating frequency is $\omega_n = 50$ Hz (in the 50 Hz system), by selecting $T_\omega = 0.02$ s (i.e., $N=200$), the oscillating term can be removed completely. However, this selection may lead to a slow dynamic response, in order to make a tradeoff between the response speed and filtering capability, the window length of the MAF is set to be 0.01 s (i.e., $N=100$), which means the MAF block cannot remove the fundamental frequency oscillation caused by the dc offset.
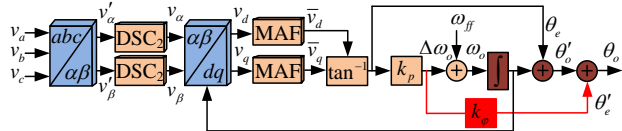
C. HPLL

Fig. 5. Block diagram of the HPLL proposed in [34].

Fig. 5 shows the general structure of the HPLL which was presented in [34] to overcome the main drawback of the QT1-PLL under dc offset and even-order harmonics scenarios. The main difference between HPLL and QT1-PLL is the application of the delay signal cancellation (DSC) in $\alpha\beta$ axis ($\alpha\beta$DSC). From Fig. 5, the $\alpha\beta$DSC input signal v_α' and v_β' is shown in (4), in order to filter out the dc offset ($V_{\alpha,dc}$, $V_{\beta,dc}$), the transfer function of $\alpha\beta$DSC applied in HPLL can be defined in the Laplace-domain as [23]

$$G_{\alpha\beta DSC_2}(s) = \frac{1}{2}(1 - e^{-\frac{T}{2}s}) \tag{11}$$

where $T=0.02$ s is the fundamental period of grid voltages.

By substituting $s=j\omega$ into (11), yields

$$G_{\alpha\beta DSC_2}(j\omega) = \left| \sin(\frac{\omega T}{4}) \right| \angle(\frac{\pi}{2} - \frac{\omega T}{4}) \tag{12}$$

From (12), it can be observed that the $\alpha\beta$DSC$_2$ operator has unity gain and zero phase-shift at 50 Hz, and provides zero gain at zero frequency and all the even order harmonic frequencies, which imply that the $G_{\alpha\beta DSC2}$ blocks all the dc offset and even order harmonics.

Therefore, v_α and v_β can be written as

$$\begin{cases} v_\alpha = \sum_{h=1,-5,7\ldots} [V_h^+ \cos(\theta_h^+) + V_h^- \cos(\theta_h^-)] \\ v_\beta = \sum_{h=1,-5,7\ldots} [V_h^+ \sin(\theta_h^+) - V_h^- \sin(\theta_h^-)] \end{cases} \tag{13}$$

Generally, the $G_{\alpha\beta DSC2}$ can be designed to be frequency adaptive to achieve zero steady-state error under frequency jump scenario. This feedback loop, however, makes it rather difficult to ensure system stability. In order to solve this problem, the phase error is compensated to the PLL output. In order to compensate the phase shift caused by the $G_{\alpha\beta DSC2}$ block under frequency jump scenarios, assuming that $\Delta\omega_i$ is the deviation value of the grid frequency from the nominal grid frequency, the phase shift can be obtained as

$$\angle \alpha\beta DSC_2(j\omega_i) = -\frac{T}{4}\Delta\omega_i \tag{14}$$

This phase-error can be easily compensated as highlighted in Fig. 5, where $k_\varphi = T/4$ can be selected.
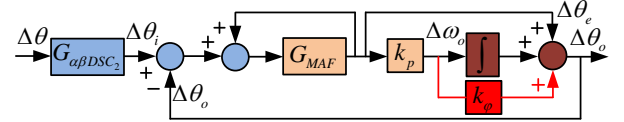

Fig. 6. Small-signal model of the HPLL [34].

The small signal model of the HPLL is shown in Fig. 6. The open-loop transfer function in z-domain can be derived as

$$G_{ol}^{HPLL}(z) = \left(\frac{G_{MAF}(z)}{1 - G_{MAF}(z)} \right) \left(1 + k_p k_\varphi + \frac{T_s k_p}{z - 1} \right) \tag{15}$$

Since the dc offset has been removed by the $G_{\alpha\beta DSC2}$, the lowest frequency needs to be filtered out is $2\omega_n = 100$ Hz, therefore, the window length of MAF is set to be $T_\omega = 0.01$ s.
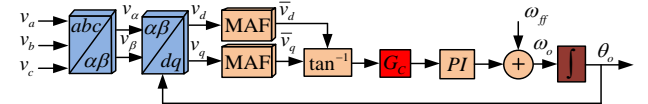
D. MPLC-PLL

Fig. 7. Block diagram of the MPLC-PLL proposed in [35].

Fig. 7 shows the general structure of the MPLC-PLL derived from the conventional MAF-PLL. The phase-lead compensator, as highlighted by G_c in Fig. 7, is applied in the control loop to effectively compensate the control delay caused by the MAF. The expression of v_d and v_q are shown in (8). The transfer function of this compensator can be derived

$$G_c(z) = k\frac{1-rz^{-1}}{1-r^N z^{-N}} \qquad (16)$$

where r is the attenuation factor, N is defined in equation (2), and $k=(1-r^N)/(1-r)$.
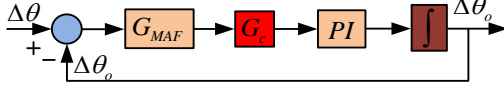

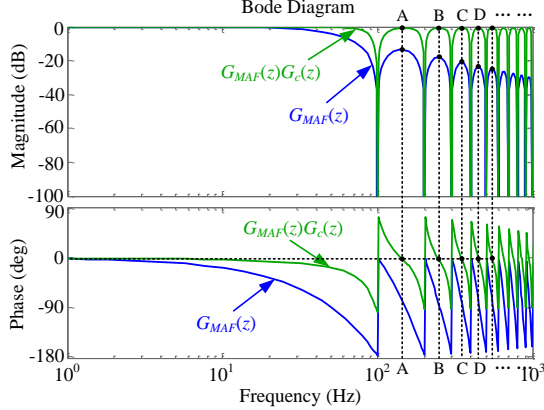Fig. 8. Small-signal model of the MPLC-PLL [35].

Fig. 9. Bode diagram of the MAF and the cascade connection of MAF and phase-lead compensator.

The small signal model of the MPLC-PLL is shown in Fig. 8. The open-loop transfer function in z-domain can be derived as

$$G_{ol}^{MPLC}(z) = G_{MAF}(z)G_c(z)PI(z)\frac{T_s}{z-1} \qquad (17)$$

where the window length T_ω is set to be 0.01 (i.e., $N=100$, this selection also ignores the dc offset), and the attenuation factor r is set to be 0.99.

From Fig. 9, it can be observed that the MAF with or without the phase-lead compensator have a similar filtering feature in frequency $f=100n$ ($n=1, 2, 3, …$). However, under other grid frequencies, especially in frequency point A, B, C, D, and so on, the MAF with phase-lead compensator may almost pass all these frequency signals without any change compared with the typical MAF, which means the phase-lead compensator actually amplify the frequency signal $f≠100n$ ($n=1, 2, 3, …$) and this feature will decrease the frequency adaptive of the MPLC-PLL under harmonic with off-nominal frequency scenario.
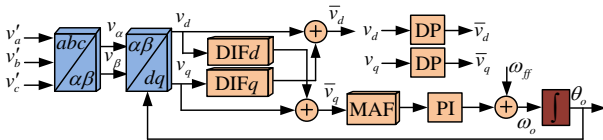
E. DMAF-PLL
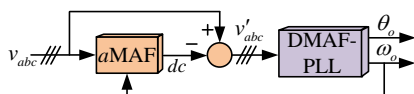

Fig. 10. Block diagram of the DMAF-PLL proposed in [36].

Fig.11. Block diagram of DMAF-PLL used in the experiment.

Fig. 10 shows the general structure of the DMAF-PLL. The 'DP' represents the decoupling transfer function. The expression of v_α and v_β is shown in (13). Fig. 11 shows the block diagram of PLL structure used in the experiment, in which one additional MAF (hereafter called aMAF) is added before the DMAF-PLL. Therefore, the DMAF-PLL input signal v_{abc}' is free of dc offset.

In [36], the aMAF block is designed to be frequency-adaptive using the rounding-down method $N=round (m\pi/\omega_0 T_s)$, which $m=2$. Although this structure can effectively filter out the dc offset, the aMAF requires a time interval of 0.02 s to reach the steady-state condition. In Fig. 10, the transfer functions of DIFd and DIFq are

$$G_{DIFd}(s) = -\frac{s}{2\omega_n}, G_{DIFq}(s) = \frac{s}{2\omega_n} \qquad (18)$$

Since v_q has a 90 ° phase lag compared with v_d, it can be obtained that $v_d/v_q=j$. Thus, substituting $s=j\omega$ into (18) and performing simple mathematical operation [36], we get

$$G_{DP}(j\omega) = 1 + \frac{j(-j\omega)}{2\omega_n} = 1 + \frac{\omega}{2\omega_n} \qquad (19)$$

Substituting $\omega=-2\omega_n$ into (19), the value of DP is zero, which implies that the DP eliminates the negative sequence 2nd order harmonics. Therefore, from (4), $\bar{v}_d$ and $\bar{v}_q$ can be expressed as

$$\begin{cases} \bar{v}_d = V_1^+ + f(6\omega_n...) \\ \bar{v}_q = V_1^+(\theta_h - \theta_0') + f(6\omega_n...) \end{cases} \qquad (20)$$

From (20), the lowest order harmonics needed to be blocked is the 6th order harmonic. Then, the T_ω is reduced to 1/300 s from 0.01 s, which significantly improves the response speed.

Fig. 12. Small-signal model of the DMAF-PLL [36].

The small signal model of DMAF-PLL is shown in Fig. 11. The decoupling transfer function DP in z-domain can be denoted as

$$G_{DP}(z) = Z\{G_{DP}(s)\} \qquad (21)$$

Therefore, the open-loop transfer function of DMAF-PLL in z-domain can be written as:

$$G_{ol}^{DMAF}(z) = G_{DP}(z)G_{MAF}(z)PI(z)\frac{T_s}{z-1} \qquad (22)$$

It should be noticed that the window length T_ω in MAF is calculated as 1/300, which results in approximately $N=33$. Thus, when the grid voltages are contaminated by harmonics, a small ripple may exist in the estimated frequency and phase angle.

III. PARAMETERS DESIGN GUIDELINES

In this Section, the control parameters design method of the MAF-based PLL is presented. And then, the frequency

domain analysis of these PLL algorithms is outlined.

In order to simplify the parameters design procedure, the parameters k_p and k_i is designed in s-domain, and then the discrete model and z-domain bode diagrams are used to test and adjust the control parameters. Therefore, the stability and disturbance rejection capability of the PLLs are ensured. The expression of MAF is approximated by the LPF, as shown in (1), and the PI regulator is denoted as k_p+k_i/s. Thus, for QT1-PLL, the open-loop transfer function can be derived as

$$G_{ol}(s) \approx \frac{2}{T_\omega} \frac{(s+k_p)}{s^2} \tag{23}$$

From (23), the proportional gain k_p is the only parameter that needs to be designed in QT1-PLL and HPLL, since the MAF window length have already been selected. Hence, the closed- loop transfer function can be derived as

$$G_{cl}(s) \approx \frac{2}{T_\omega} \frac{(s+k_p)}{s^2+(2/T_\omega)s+2k_p/T_\omega} \tag{24}$$

By comparing to the standard second order system, we get

$$2/T_\omega = 2\xi\omega_n', \; 2k_p/T_\omega = \omega_n'^2 \tag{25}$$

where ξ is the damping factor, and ω_n' is the natural frequency.

Substituting T_ω=0.01 s and ξ=0.707 into (25), yields $k_p{\approx}100$. Next step is to adjust k_p on the basis of the real transfer function in z-domain, as shown in (10) and (15). Since the k_φ in (15) is small, the expression (10) and (15) are almost identical to each other.

Thus, the phase margin (PM), crossover frequency (CF), and gain margin (GM) of (10) as the function of k_p are derived, as shown in Fig. 13. It can be seen that when k_p varies from 50 to 150, the PM (blue line) varies from 56.7 ° to 34.2 °, and the GM (red line) varies from 35.9 dB to 21.9 dB, which is suitable to ensure sufficient stability margin. The CF (green line) shows relatively smooth change (from 31.2 Hz to 35.5 Hz), which is much higher than the conventional PLLs and a fast dynamic response can be guaranteed. Therefore, k_p=92 is selected for QT1-PLL and k_p=94 is selected for HPLL.

As for MPLC-PLL, since the cascade connection of the MAF and phase-lead compensator provides a close gain to unity with a near zero phase shift at low frequency range [35]. Therefore, the transfer function (17) can be approximated by
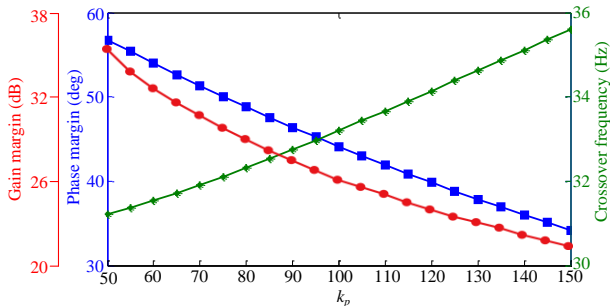

Fig. 13. The PM, CF, and GM of (5) as a function of k_p in z-domain.

a typical type-2 system. It can be obtained that

$$k_p = 2\xi\omega_n', \; k_i = \omega_n'^2 \tag{26}$$

In (26), by selecting ξ=0.707 and ω_n' =2π20rad/s, k_p and k_i can be calculated.

For DMAF-PLL, the DP is ignored at first, and when MAF is replaced by the LPF, the standard design procedure presented in [38] can be applied to design the parameters of DMAF-PLL. Therefore, the transfer function of DMAF-PLL is derived as

$$G_{ol}^{DMAF} \approx \frac{2}{T_\omega} \frac{(k_p s + k_i)}{s^2(s+2/T_\omega)} \tag{27}$$

According to the symmetrical optimum method, k_p and k_i can be expressed as

$$2/T_\omega = b\omega_c, \; k_p = \omega_c, \; k_i = \omega_c^2/b \tag{28}$$

where ω_c is the cutoff angle-frequency and b is a constant which is suggested to be 2.4 in [37]. In [36], T_ω=0.0033 s, and ω_c is set to be 250 rad/s. Therefore, k_p and k_i can be calculated. According to the aforementioned parameters design method, the control parameters of the four MAF-based PLL algorithms are summarized in Table I.

TABLE I
CONTROL PARAMETERS OF THE MAF-BASED PLL
ALGORITHMS

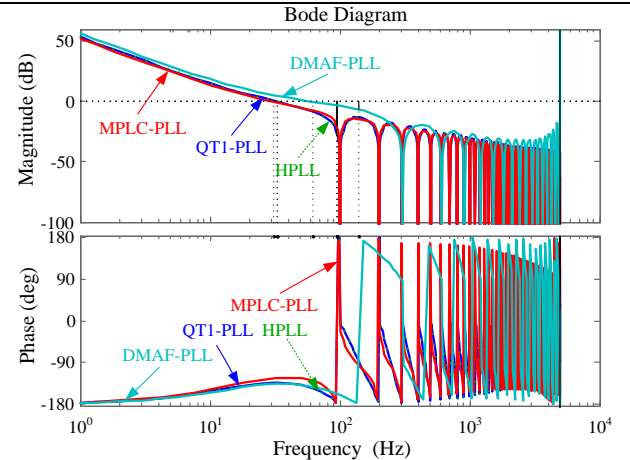|	QT1-PLL	HPLL	MPLC-PLL	DMAF-PLL
N(MAF)	100	100	100	33
k_p	92	94	177.71	250
k_i	--	--	15791	26041
r	--	--	0.99	--
k_φ	--	0.005	--	--
N(aMAF)	--	--	--	round $(2\pi/\omega_0 T_s)$
n(αβDSC)	--	2	--	--

Fig. 14. Bode diagram of open-loop transfer functions of the MAF-based PLLs.

The bode diagram of the QT1-PLL, HPLL, MPLC-PLL, and DMAF-PLL is obtained by using open-loop transfer function of (10), (15), (17), and (22), as shown in Fig. 14. It can be noticed from Fig. 14 that the QT1-PLL (blue solid line) and HPLL (green dot line) show almost the same frequency response, because the difference between QT1-PLL and

HPLL mainly lies on coordinate transformation instead of the control loop. The crossover frequencies (CFs) of QT1-PLL and HPLL are both 32.9 Hz, which ensures a relatively fast dynamic response. The GM and PM are both 27.6 dB and 45.5°, respectively, which ensures a sufficient stability margin of these PLLs.

The MPLC-PLL (red solid line) shows a similar frequency response compared with QT1-PLL and HPLL. And the CF of MPLC-PLL is approximately 30.7 Hz, which is much higher compare with the conventional MAF-based PLL. The GM and PM are 20.4 dB and 55°, respectively, which is the desired stability margin. However, the DMAF-PLL shows a different frequency response compared with other three PLL algorithms due to the difference between the MAF window lengths. The CF of DMAF-PLL is the highest (about 62 Hz) due to the small window length and the high proportional gain. And the system GM and PM are 6.61 dB and 37.7°, respectively.

In the high frequency range, the four PLLs show similar amplitude-frequency characteristics. The DMAF-PLL algorithm almost blocks the high frequency components of integer multiples of 300 Hz, however, for other three PLLs, that is 100 Hz.

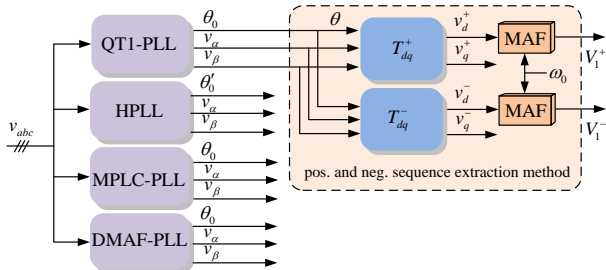## IV. SEQUENCE COMPONENTS EXTRACTION METHODS

Fig. 15. Block diagram of the fundamental frequency positive and negative sequence amplitude extraction.

Fig. 15 shows the block diagram of the fundamental frequency positive (pos.) negative (neg.) sequence amplitude extraction. The extraction method is shown in the dotted frame in which four input signals θ, v_α, v_β, and ω_0 are required. For HPLL, it should be noticed that the phase-angle used for amplitude extraction is θ_d' (not θ_0). If use θ_0, the input voltage should be v_α' and v_β' (not v_α, and v_β). However, this selection will make the extraction procedure sluggish. The signal mentioned in this Section are all shown in corresponding block diagram of each PLL. The transformation matrix to extract the positive and negative sequence is expressed as

$$T_{dq}^+ = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}, \; T_{dq}^- = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \quad (29)$$

Thus, v_d^+ and v_d^- can be expressed as

$$v_d^+ = \begin{cases} V_1^+ + f(2\omega_n, 6\omega_n...) & \text{HPLL, DMAF-PLL} \\ V_1^+ + f(\omega_n, 2\omega_n, 6\omega_n...) & \text{QT1-PLL, MPLC-PLL} \end{cases} \quad (30)$$

$$v_d^- = \begin{cases} V_1^- + f(2\omega_n, 6\omega_n...) & \text{HPLL, DMAF-PLL} \\ V_1^- + f(\omega_n, 2\omega_n, 6\omega_n...) & \text{QT1-PLL, MPLC-PLL} \end{cases} \quad (31)$$

where f is the oscillating term caused by unbalance grid voltage, harmonics, and dc offset.

The MAF window length is set to be frequency adaptive (the estimated period is $2\pi/\omega_0$). Therefore, the accuracy of the frequency estimation affects the accuracy for the positive and negative sequence components extraction to a large extent.

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

The aim of this section is to evaluate the performance of the four PLLs under different grid voltage disturbance scenarios which is generated by the grid simulator by using a three-phase voltage source inverter (VSI) controlled in the voltage control mode (VCM) [38]. To validate the analysis, the experimental prototype was based on the 2.2 kW Danfoss inverter controlled in VCM using LCL output filter with resistive load, the capacitor voltage of the LCL filter was controlled to synthesize the virtual grid conditions. The inverter PWM frequency was set to be 10 kHz in order to evaluate the PLL algorithms with a discrete time-step of 100 microseconds, as analyzed in the paper.

Fig. 16. Photo of the experimental set-up [38, 39].

The dSPACE1006 platform was utilized to implement the Simulink-based control algorithms and the compiled executable file was downloaded to the dSPACE1006 controller to extract the real-time grid-synchronization signals. The binary word size was only several kilobytes (kB) when the VCM was adopted for inverter control and the four PLL algorithms were implemented, which facilities the practical implementation in both fixed point and floating point digital signal processors (DSPs) [see Fig. 16] [39]. The detailed comparison of the four PLL under different grid disturbance scenarios are shown in Table II and Table III.

Case1. Performance Comparison Under 90° Phase-Angle Jump

Fig. 17 shows the pos. and neg. sequence amplitudes and Fig. 18 illustrates the estimated frequency and the phase

estimation error under phase-angle jump of +90 °. It can be noticed all the PLLs can achieve zero steady-state error of all amplitude, frequency and phase in 2.5 cycles. However, the DMAF-PLL shows an overshoot of 60 Hz in the estimated frequency, and HPLL shows the smallest overshoot of about 28 Hz. In terms of the phase-angle estimation, the HPLL shows an overshoot of about 50 °, and the MPLC-PLL shows the smallest overshoot of about 20 °.

Case2. Performance Comparison Under +5 Hz Frequency Jump

Fig. 19 shows the pos. and neg. sequence amplitudes under frequency jump of +5 Hz. It can be seen that all of the PLLs can achieve zero steady-state error in positive sequence

except for HPLL, where the steady-state error is caused by the non-frequency adaptive DSC. In negative sequence frame, all the PLLs can achieve zero steady-state error in about 3 cycles.

Fig. 20 illustrates the estimated frequency and the phase estimation error under frequency jump of +5 Hz. For the four PLLs, similar results are achieved, and the estimated frequency is locked to the rated value in about 2 cycles. The HPLL and DMAF-PLL show similar overshoots of about 2.5 Hz. In terms of phase-angle estimation, HPLL has the largest overshoot of 12 °, and other three PLLs show an overshoot of about 8 °.
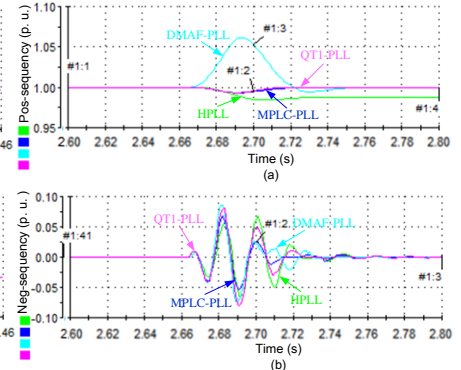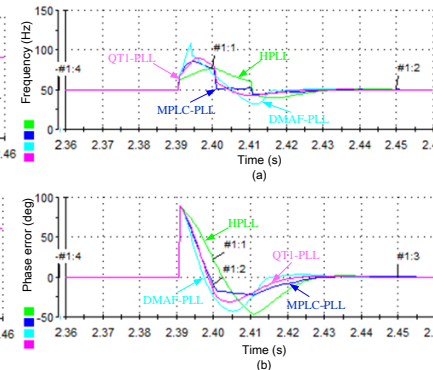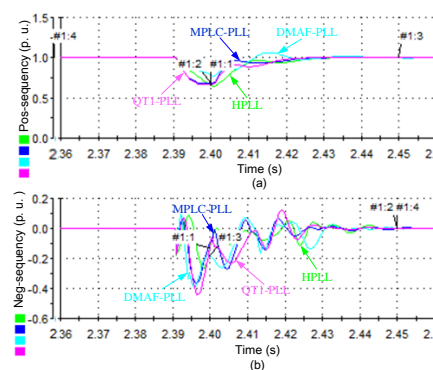

Fig. 17. Estimated pos. and neg. sequence amplitudes under +90 ° phase-angle jump.

Fig. 18. Estimated frequency and phase error under +90 ° phase-angle jump.

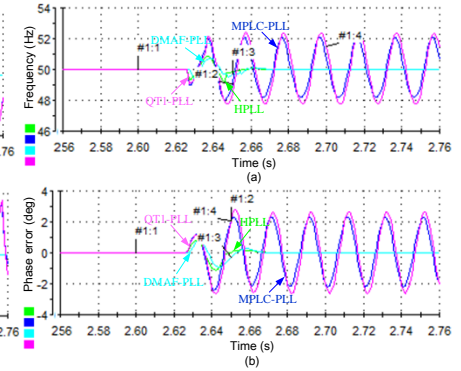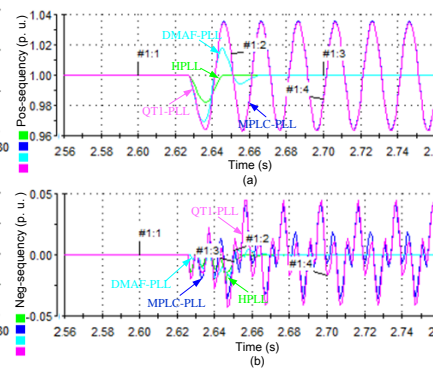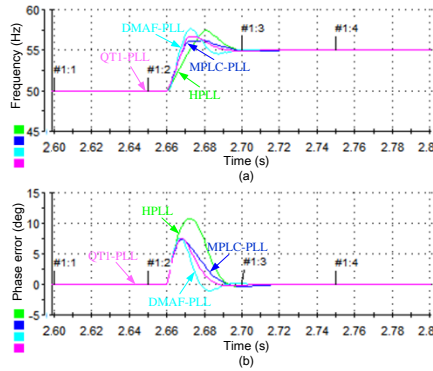Fig. 19. Estimated pos. and neg. sequence amplitudes under frequency jump of +5 Hz.

Fig. 20. Estimated frequency and phase error under frequency jump of +5 Hz.

Fig. 21. Estimated pos. and neg. sequence amplitudes under dc offset.

Fig. 22. Estimated frequency and phase error under dc offset.

Case3. Performance Comparison Under DC Offset

Fig. 21 shows the pos. and neg. sequence amplitudes under dc offset. Due to the application of *a*MAF in DMAF-PLL and DSC in HPLL, the two PLL can achieve zero steady state error in pos. and neg. sequence amplitudes. However, for QT1-PLL and MPLC-PLL, the noticeable fundamental frequency oscillation can be observed in positive and negative sequence amplitudes. Fig. 22 illustrates the estimated frequency and the phase estimation error under dc offset. Because the MAF in QT1-PLL and MPLC-PLL cannot filter out the fundamental frequency oscillations caused by dc offset, the two PLLs show similar fluctuations both in the estimated frequency and phase angle. For HPLL, the estimated frequency is locked to the rated value in about

one cycle. For DMAF-PLL, however, longer response time is needed (about 2 cycles) to achieve a zero steady-state error due to the large window length of *a*MAF.

Case4. Performance Comparison Under 0.4 p. u. Single-Phase Voltage Sag

Fig. 23 shows the pos. and neg. sequence amplitudes under 0.4 p. u. single-phase voltage sag. It shows that all PLLs achieve zero steady-state error in both positive and negative sequence amplitudes, which show the fastest dynamic response. However, DMAF-PLL algorithm shows the slowest transient response due to the use of *a*MAF.

Fig. 24 illustrates the estimated frequency and the phase estimation error under 0.4 p. u. single-phase voltage sag. It can be seen that QT1-PLL shows the shortest response time

(less than one cycle), but for DMAF-PLL, response time is greater than 2 cycles. For HPLL and MPLC-PLL, the setting time is about 2 cycles. Similar transient overshoots in

frequency can be observed in QT1-PLL, DMAF-PLL and MPLC-PLL (about 3 Hz), and HPLL shows a frequency overshoot of about 1.8 Hz.
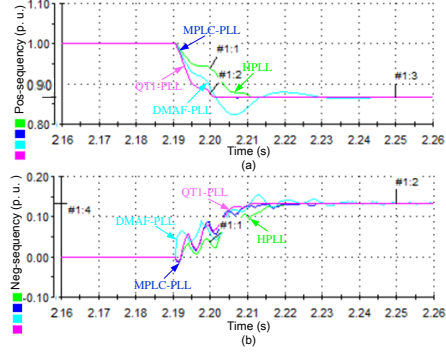

Fig. 23. Estimated pos. and neg. sequence amplitudes under single-phase voltage sag.
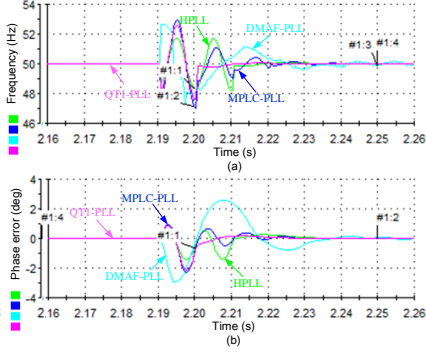
Fig. 24. Estimated frequency and phase error under single-phase voltage sag.
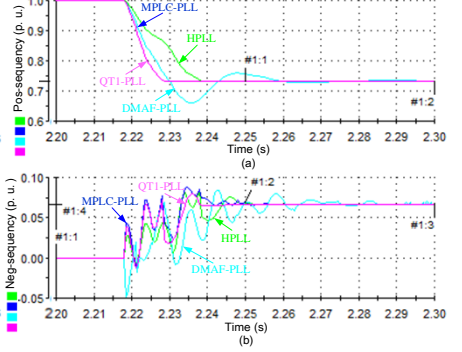
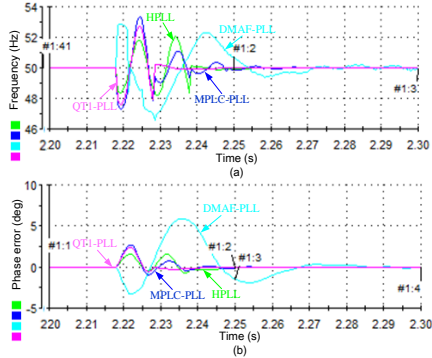Fig. 25. Estimated pos. and neg. sequence amplitudes under two-phase voltage sag.

Fig. 26. Estimated frequency and phase error under two-phase voltage sag.
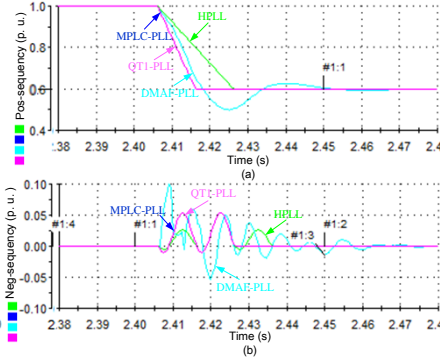
Fig. 27. Estimated pos. and neg. sequence amplitudes under three-phase voltage sag.
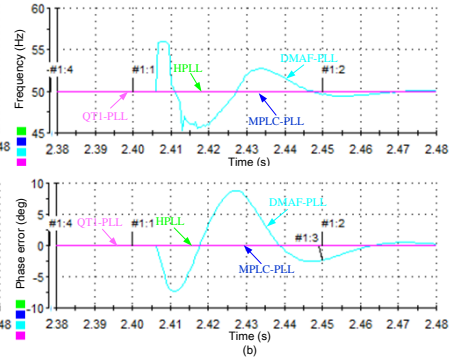
Fig. 28. Estimated frequency and phase error under three-phase voltage sag.

Case5. Performance Comparison Under 0.4 p. u. Two-Phase Voltage Sag

Fig. 25 shows the estimated pos. and neg. sequence amplitudes and Fig. 26 illustrates the estimated frequency and the phase estimation error under 0.4 p. u. two-phase voltage sag. Similar to the case of single-phase voltage sag, all PLLs can achieve zero steady-state error in the positive and negative sequence amplitudes, frequency and phase, and the QT1-PLL and DMAF-PLL show the fastest and slowest dynamic response, respectively. The highest and lowest overshoot in frequency is found in MPLC-PLL (about 3.5 Hz) and HPLL (about 1.5 Hz), respectively.

Case6. Performance Comparison Under 0.4 p. u. Three-Phase Voltage Sag

Fig. 27 shows the pos. and neg. sequence amplitudes and Fig. 28 illustrates the estimated frequency and the phase estimation error under 0.4 p. u. three-phase voltage sag. In positive and negative sequence amplitudes, the experimental waveforms are similar to the case of the single-phase and two-phase voltage sag. The estimated frequency and phase error of QT1-PLL, MPLC-PLL and HPLL is not affected by three-phase voltage sag. However, a high overshoot of about 6 Hz in the estimated frequency and slow dynamic response of about 3 cycles is found in DMAF-PLL, which is mainly because of the highly

nonlinear system caused by the *a*MAF.

Case7. Performance Comparison Under Voltage Flicker

Fig. 29 shows the pos. and neg. sequence amplitudes under voltage flicker. It can be observed that all the PLLs fail to achieve zero steady-state error and obvious ripple is found both in pos. and neg. sequence amplitude.

Fig. 30 illustrates the estimated frequency and the phase estimation error under voltage flicker. Similar to the case of three-phase voltage sag, all PLLs are not affected by voltage flicker except for the DMAF-PLL, which shows steady-state oscillations both in the estimated frequency of about 1.5 Hz and the estimated phase angle of about 3.5 °, which may also caused by the *a*MAF.

Case8. Performance Comparison Under Noise Contaminations

To evaluate the noise immunity of PLLs, a zero-mean Gauss white noise of variance $\sigma^2=0.01$ is added to the input. The signal-to-noise-ratio (SNR) is 10 log $(1/2\sigma^2)$ =17 dB. The noisy waveform is sampled at a rate of 100 kHz, and is then fed to a digital anti-aliasing filter. This high sampling rate is used to avoid the aliasing effects and increase the accuracy. A digital first-order LPF with cutoff frequency of 4 kHz is considered as the anti-aliasing filter. The output of anti-aliasing filter is down sampled to 10 kHz and is fed to the PLL.

Fig. 31 shows the pos. and neg. sequence amplitudes, and Fig. 32 illustrates the estimated frequency and the phase estimation error. It can be seen that all PLLs have similar peak to peak steady-state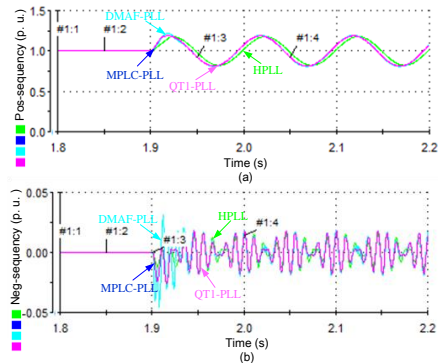 oscillation, for the estimated pos. and neg. sequence amplitude, that is about 0.005 p. u. and 0.04 p. u., respectively, for estimated frequency and phase, that is about 2 Hz and 0.4 °, respectively.

Fig. 29. Estimated pos. and neg. sequence amplitudes under voltage flicker.

Fig. 30. Estimated frequency and phase error under voltage flicker.

Fig. 31. Estimated pos. and neg. sequence amplitudes under noise contaminations.
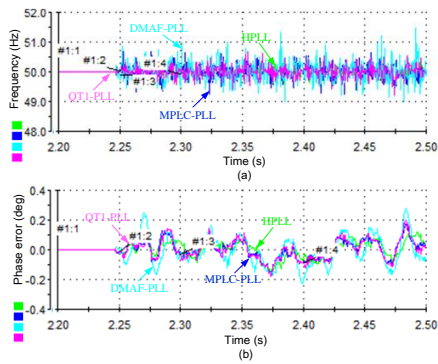
Fig. 32. Estimated frequency and phase error under noise contamination.

Fig. 33. Estimated pos. and neg. sequence amplitudes under harmonic with frequency jump.
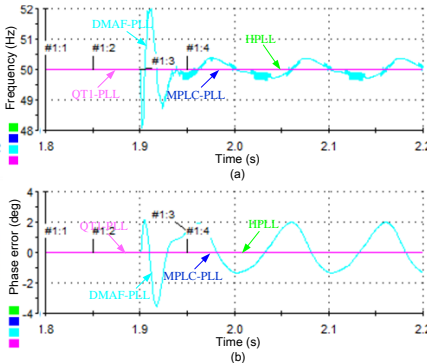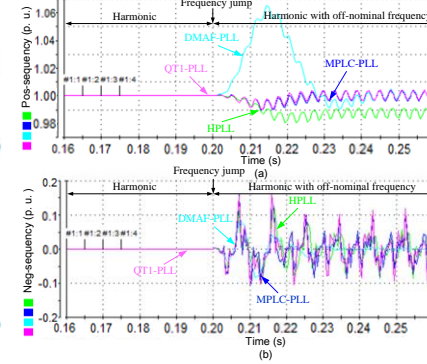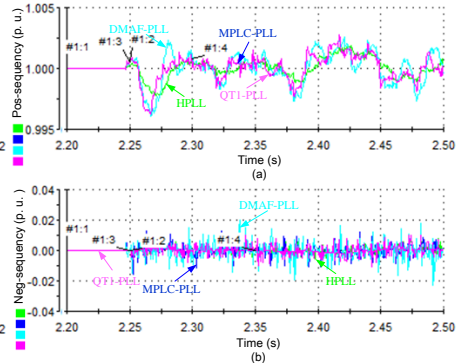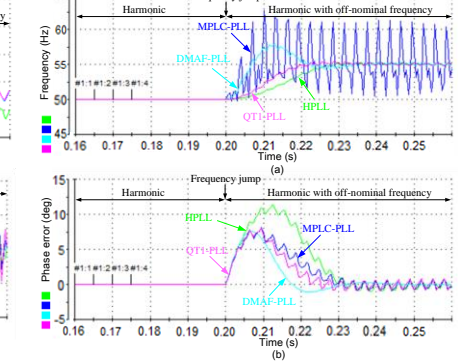

Fig. 34. Estimated frequency and phase error under harmonic with frequency jump.

Case9. Performance Comparison Under Harmonics with Frequency Jump

In order to analyze the frequency-adaptive performances of the four MAF-based PLLs, the harmonic (0.1 p. u. of -5th, and 0.05 p. u. of +7th, -11th, and +13th harmonics) with frequency jump (+5 Hz) scenario is subjected to the grid voltage.

Fig. 33 shows the estimated pos. and neg. sequence amplitude and Fig. 34 illustrates the estimated frequency and the phase estimation error. It can be seen that when the grid voltage only suffer from the harmonic (before 0.2s), the four MAF-based PLL all can achieve the zero steady-state error in amplitude, frequency and phase estimation. When the frequency jump occurs (0.2s), the DMAF-PLL shows the best steady-state performance with lowest oscillation. However, the MPLC-PLL shows the biggest oscillation in estimated frequency mainly because of the phase-lead compensator which will actually amplify the error signal under harmonic with off-nominal frequency condition. The detail steady-state oscillation amplitude is shown in Table III.

VI. PERFORMANCE IMPROVEMENT OF HPLL BY USING AMPLITUDE ERROR COMPENSATION METHOD

From the previously performance comparison, the four PLL all have satisfactory performance under various disturbances. For HPLL, when frequency jump occurs, some improvement method should be made to eliminate the steady-state error in the positive sequence amplitude estimation since extraction of positive sequence of fundamental components is critical for grid-connected inverters for grid synchronization. Therefore, inspired by the phase-error compensation (PEC) in HPLL, the amplitude error compensation (AEC) is proposed herein. From (12), the $\alpha\beta DSC_2$ output signal amplitude can be written as:

$$A = \sin(\frac{\omega + \Delta\omega_i}{4})T \tag{32}$$

Thus, the amplitude error caused by $\alpha\beta DSC_2$ operator can be expressed as:

$$\Delta A = 1 - \cos(\frac{\Delta\omega_i T}{4}) \tag{33}$$

Since the average value of $\Delta\omega_o$ is equal to $\Delta\omega_i$ under locked condition, the amplitude error at the output of HPLL can be compensated by online calculation of (33). The block diagram of HPLL with AEC is shown in Fig. 35. The V_d^+ indicates the positive sequence amplitude after AEC and $k_a = T/4$. It should be noticed that the AEC is not connected to

the control loop and the dynamics of HPLL is unaffected.

Therefore, from Fig. 35, V_d^+ can be expressed as

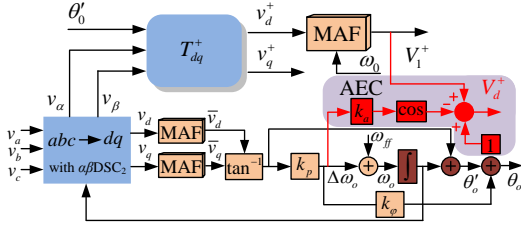$$V_d^+ = 1 + V_1^+ - \cos(\frac{\Delta\omega_i T}{4}) \qquad (34)$$

Fig. 35. Block diagram of HPLL with the proposed AEC.

The experimental result with and without AEC is shown in Fig. 36. It shows that the AEC effectively compensates the amplitude error and achieves a zero steady-state error in about 1.5 cycles.
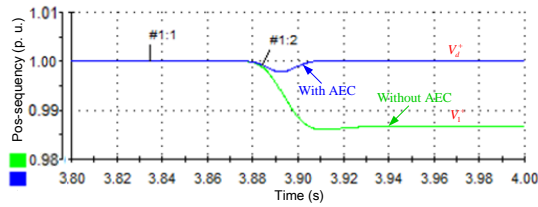

Fig. 36. Estimated positive sequence amplitude with and/or without AEC under frequency jump of +5 Hz.

VII. CONCLUSION

In this paper, a detailed analysis and performance comparison of the four MAF-based PLLs is presented. For the QT1-PLL, the introduction of the quasi-type-1 control structure effectively improves the dynamic response of the MAF-PLL. The lack of dc offset and even harmonic rejection is the main disadvantages of this PLL algorithm. Apart from this, the QT1-PLL shows a satisfactory steady-state and dynamic performance, and disturbance rejection capability under others grid voltage disturbance conditions.

The HPLL can be perceived as the improved version of the QT1-PLL algorithm. The application of the $\alpha\beta$DSC$_2$ block can effectively overcome the shortcomings of QT1-PLL without jeopardizing its dynamic performance and filtering capability. However, the disturbance rejection capability of the HPLL and QT1-PLL decreases with the frequency deviation from its nominal value under harmonic scenario caused by the non-frequency adaptive MAF and DSC, then a

associated drawback of the HPLL is the amplitude tracking error [see Fig. 19] and the to tackle this problem, the amplitude error compensation (AEC) method is proposed in last Section, which effectively compensates the amplitude error and ensures the accuracy of the positive sequence component extraction.

For the MPLC-PLL, the cascading of the MAF and phase-lead compensator results in the fast dynamic response of the SRF-PLL and the disturbance rejection capability of the MAF-PLL while increasing the frequency estimation error under harmonic with off-nominal frequency scenario. Similar to the QT1-PLL, however, the MPLC-PLL is also not suitable for grid-synchronization when the grid voltages contains the dc offset and even order harmonics, and under other grid voltage disturbance scenarios, the MPLC-PLL can be a good choice.

For the DMAF-PLL, the window length of the MAF in control loop is drastically reduced through the use of 'DP' which significantly improves the system dynamic response. The frequency adaptive aMAF (n=2 shown in Section II Part A) ensure the best steady-state performance under harmonic with off-nominal frequency scenario while making the dynamic response sluggish and may even lead to system instability under some circumstances like voltage sag and flicker. Hence, it can be concluded that the DMAF-PLL can be used for grid-synchronization when the grid voltage is free from sag and flicker. The research findings of this paper may provide some useful guidelines for grid-synchronization of the three-phase grid-connected PWM inverters and distributed generators (DGs) in the smart grid.

TABLE II COMPARISON OF THE MAF-BASED PLLS UNDER PHASE/FREQUENCY JUMP AND VOLTAGE SAG

	QT1-PLL		HPLL		MPLC-PLL		DMAF-PLL	
	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)
Phase-Angle Jump of +90°	36 ms	40 Hz	45 ms	25 Hz	38 ms	35 Hz	40 ms	60 Hz
Frequency Jump of +5 Hz	35 ms	1.7 Hz	37 ms	2.5 Hz	38 ms	1.3 Hz	40 ms	2.8 Hz
0.4 p. u. Single-Phase Voltage Sag	10 ms	2.5 Hz	20 ms	1.8 Hz	10 ms	3.2 Hz	43 ms	2.8 Hz
0.4 p. u. Two-Phase Voltage Sag	10 ms	2.8 Hz	20 ms	2.1 Hz	10 ms	3.4 Hz	41 ms	3.8 Hz
0.4 p. u. Three-Phase Voltage Sag	20 ms	0 Hz	20 ms	0 Hz	10 ms	0 Hz	42 ms	7.2 Hz

Note: (a) and (b) represent setting time and frequency overshoot, respectively.

TABLE III COMPARISON OF THE MAF-BASED PLLS UNDER DC OFFSET, FLICKER, NOISE AND HARMONIC

	QT1-PLL		HPLL		MPLC-PLL		DMAF-PLL	
	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)
DC Offset	4.6 Hz	5.2 °	0 Hz	0 °	4.0 Hz	4.5 °	0 Hz	0 °
Voltage Flicker	0 Hz	0 °	0 Hz	0 °	0 Hz	0 °	1.5 Hz	3.3 °
Noise	1.5 Hz	0.3 °	1.5 Hz	0.2 °	1.3 Hz	0.3 °	1.9 Hz	0.5 °
Harmonics without/with +5Hz	0/0.4 Hz	0 °/1.6 °	0/0.2 Hz	0 °/1.5 °	0/10.5 Hz	0 °/1.4 °	0.04/0.6 Hz	0.01 °/0.05 °

Note: (a) and (b) represent peak-to-peak frequency error and peak-to-peak phase error, respectively.

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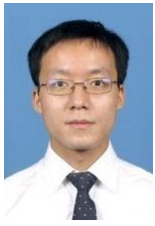
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