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Distributed Secondary Voltage and Frequency Control for Islanded Microgrids with Uncertain Communication Links

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***Abstract*—This paper presents a robust distributed secondary control (DSC) scheme for inverter-based microgrids (MGs) in a distribution sparse network with uncertain communication links. By using the iterative learning mechanics, two discrete-time DSC controllers are designed, which enable all distributed energy resources (DERs) in a MG to achieve the voltage/frequency restoration and active power sharing accuracy, respectively. In special, the secondary control inputs are merely updated at the end of each round of iteration, and thus each DER only needs to share information with its neighbors intermittently in a low-bandwidth communication manner. This way, the communication costs are greatly reduced, and some sufficient conditions on the system stability and robustness to the uncertainties are also derived by using the tools of Lyapunov stability theory, algebraic graph theory, and matrix inequality theory. The proposed controllers are implemented on local DERs, and thus no central controller is required. Moreover, the desired control objective can also be guaranteed even if all DERs are subject to internal uncertainties and external noises including initial voltage and/or frequency resetting errors and measurement disturbances, which then improves the system reliability and robustness. The effectiveness of the proposed DSC scheme is verified by the simulation of an islanded MG in MATLAB/SimPowerSystems.**

***Index Terms*—Distributed control, secondary control, discrete-time, islanded microgrid.**

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I. Introduction

MICROGRIDS are able to achieve the effective integration of large number of DERs via DC/AC inverters [1]. In general, MGs transfer from grid-connected mode to islanded mode induced by disturbances or faults autonomously. The local primary control (droop technique) embedded in inverters preserves the autonomy of each DER [2]. When load changes occur in islanded MGs, different DERs in the network should adjust their output powers to keep the dynamical balance between the loads and DERs across the MG. However, the inherent defect of droop control is that the deviations of frequency and voltage amplitude can be significantly impacted by loads [3]-[5]. Thus, the secondary control is employed to restore the frequency and voltage to the desired values.

Different from traditional centralized control for MGs with many deficiencies, including the high costs generated by the high-bandwidth communication links, difficulty for the future extension of MGs [6]-[8], the distributed structure provides a practically feasible and highly computational efficiency solution. In view of this, some DSC approaches have been proposed to achieve voltage/frequency restoration [8],[14], reactive sharing [9],[17], imbalance voltage compensation [13], etc. Specially, based on the distributed cooperative control of multi-agent systems [10],[11], a DSC method for voltage regulation was proposed [8], which relies on the feedback linearization technique with high gains. However, high gain has a negative impact on the overall stability of MGs. Then, a DSC for voltage imbalance compensation was investigated in [13], which guarantees the achievement of voltage regulation in a finite time. To regulate the power output of a MG dynamics consisting of a large number of DERs, a pinning-based DSC scheme was then presented with uncertain communication topologies [12], which is of benefit to meet the common requirements of line switches and plug-and-play operation in MGs. Further, a DSC approach to regulate the voltage, frequency, and reactive power was proposed [14], where each local DER is required to communicate with all the other DERs across the MG, which has almost the same communication costs as a centralized control approach. Besides, the detailed stability analysis is neglected. Moreover, to obtain the trade-off between voltage regulation and accurate reactive power sharing, the information (voltages and frequencies) communication among neighboring DERs plays a key ingredient [15]. However, in the above literatures, it is generally assumed that

all DERs can access the system parameters accurately, and the ubiquitous communication disturbances and noises between DERs are negligible.

Due to the impact of component mismatches, numerical errors [16], high frequency component of disturbances and noises, transient power oscillation caused by the flow of large reactive power currents [17], it is difficult for each DER to get the accurate information from its neighbors. Moreover, those impacts on the stability of low-voltage MGs are more severe than that of high-voltage ones [17]-[18]. Besides, it has been recognized that the perturbations existed in the information exchanges among DERs are usually unavoidable [13],[19],[20], which inspires us to take the impacts of communication disturbances and noises on the system stability into account when we design DSC schemes for MGs.

This paper aims to propose a novel DSC scheme for islanded MGs, which is robust to the interval uncertainties within information exchanges among all DERs. In detail, two DSC controllers with discrete-time control inputs for the achievement of the voltage/frequency restoration and the active power sharing accuracy will be designed and implemented on local DERs. With the proposed DSC scheme, each DER only needs to access partial or limited knowledge of the system parameters, perform merely local measurements, and then communicate with its neighbors intermittently. Stability analysis for the controlled system is also given. Moreover, the information exchanges among DERs are in the discrete form and thus greatly reduce the communication costs, which then makes our results essentially different from the existing methods that with the continuous-time communications [8],[12].

The rest of this paper is organized as follows. The system model is formulated in Sec. II, and the proposed DSC scheme containing two DSC algorithms with discrete-time control inputs is designed and analyzed in Sec. III. Then, the numerical results are simulated via an islanded MG in Sec. IV before we conclude the work in Sec. V. Finally, an important lemma of the main results is given in Appendix.

Some necessary notifications are given below. Let $\otimes$ be the Kronecker product. For any vectors $x, y \in R^n$, denote $x \odot y = (x_1 y_1, \cdots, x_n y_n)^T \in R^n$.

II. Problem Formulation and Preliminaries

A. Problem Formulation

Consider an inverter-based MG consisting of N DERs. For the ith DER, the basic internal multiple control loops as well as the primary and secondary control procedure can be drawn in Fig. 1. The common d-q reference frame transformation is used, where d-axis and q-axis for each DER are rotating with the common reference frequency [8].

As seen in Fig. 1, the current, voltage, and power control loops are employed in each DER. The primary control procedure is implemented during the power control loop with the nominal set points $V_i^{\rm nom}$ and $\omega_i^{\rm nom}$. With the reference values, $V_{\rm iref}^{\rm od}$ and $V_{\rm iref}^{\rm oq}$, provided by the power loop, the voltage loop generates the current reference, $i_{\rm iref}^{L\rm d}$ and $i_{\rm iref}^{L\rm q}$, for the current loop. Then, the current errors are calculated and finally used to regulate the outputs of the inverter by SPWM mode.

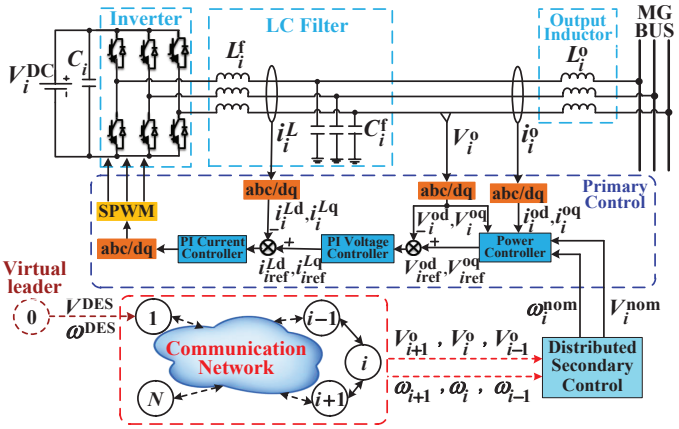


Fig. 1. Distributed control for MGs, the red dotted lines represent a sparse communication network for system information exchanges among DERs.

To compensate the voltage and frequency deviations caused by the primary control procedure, the secondary control procedure is applied to generate different nominal set points for different DERs in a distributed way. In detail, we will design a DSC scheme by the information exchanges among the neighboring DERs to update $V_i^{\rm nom}$ and $\omega_i^{\rm nom}$ in each primary control process, and further restore the terminal outputs, voltage V_i and frequency ω_i, to their desired values, $V^{\rm DES}$ and $\omega^{\rm DES}$ provided by a virtual leader DER$_0$ (can be controlled by the main grid in a connected mode or obtained by the command DER in a stand-alone mode).

Since an LCL filter is added in each DER so that the output impedance is highly inductive and dominate any resistive effects, the following primary control principle is used as the power control loop [4,14]:

$$\begin{cases} V_i = V_i^{\rm nom} - K_i^Q Q_i, \\ \omega_i = \omega_i^{\rm nom} - K_i^P P_i, \end{cases} \tag{1}$$

where V_i and ω_i are respectively the actual voltage magnitude and frequency, Q_i and P_i are the measured reactive and active powers after low-pass filters, and K_i^Q and K_i^P are the associated droop coefficients, respectively.

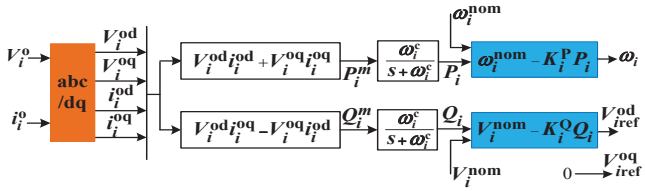


Fig. 2. Block diagram of the primary control in a power loop.

Here we choose the output voltage magnitude reference is aligned to the d-axis of reference frame of the ith DER. Rewrite the droop control principle (1) for the ith DER as

$$\begin{cases} \begin{cases} V_i^{\rm od} = V_i^{\rm nom} - K_i^Q Q_i, \\ V_i^{\rm oq} = 0, \end{cases} \\ \omega_i = \omega_i^{\rm nom} - K_i^P P_i. \end{cases} \tag{2}$$

The block diagram of the primary control principle is shown in Fig.2, where ω_i^c is the cut-off frequency of the

low-pass filters installed in the power control loop, P_i^m and Q_i^m are the instantaneous active and reactive power components calculated from the measured output voltage and output current [19]. Since the output voltage amplitude of the ith DER is $V_i = \sqrt{(V_i^{\rm od})^2 + (V_i^{\rm oq})^2}$, the restoration of voltage amplitude, $V_i \to V^{\rm DES}$, is achieved by choosing $V_i^{\rm nom}$ such that $V_i^{\rm od} \to V^{\rm DES}$ by equation (2). The secondary frequency control is to select $\omega_i^{\rm nom}$ such that $\omega_i \to \omega^{\rm DES}$.

B. Communication Network

For better describing the communication network structure of a MG, the algebraic digraph theory is adopted here. The communication network of a MG consisting of N DERs (labeled 1 through N) is mapped to a digraph $\mathcal{G}(\mathcal{V}, \mathcal{E}, A)$, where the node set $\mathcal{V} = \{v_1, v_2, \cdots, v_N\}$ represents all DERs and the set of edges $\mathcal{E} \subseteq \mathcal{V} \times \mathcal{V}$ represents the communication links for information exchange. $A = (a_{ij})_{N\times N}$ is a weighted adjacency matrix with elements $a_{ii} = 0$ and $a_{ij} \geq 0$. $a_{ij} > 0$ if and only if the edge $(v_i, v_j) \in \mathcal{E}$. The set of neighbors of the ith DER v_i is given by $N_i = \{v_j \in \mathcal{V} : (v_i, v_j) \in \mathcal{E}\}$. The Laplacian matrix $L = (\ell_{ij})_{N\times N}$ is defined as $\ell_{ij} = -a_{ij}$, $i \neq j$, and $\ell_{ii} = \sum_{j=1}^{N} a_{ij}$ for $i = 1, \cdots, N$, which satisfies $L1_N = 0$ with $1_N = (1, \cdots, 1)^T \in R^N$.

In addition, the digraph $\hat{\mathcal{G}}(A)$ is used to describe the interconnection topology of a MG consisting of one virtual leader-DER, denoted by 0, which cannot receive information from all other DERs, and N follower-DERs, denoted by $1, \cdots, N$ [25]. Diagonal matrix $B = \text{diag}\{a_{10}, \cdots, a_{N0}\}$ is called the leader adjacency matrix, where $a_{i0} > 0$ if follower-DER$_i$ is connected to DER$_0$ across the communication link (v_0, v_i), otherwise $a_{i0} = 0$.

For the uncertain communication links, we assume that each nonzero weight a_{ij} satisfies $0 < \underline{a_{ij}} \leq a_{ij} \leq \overline{a_{ij}}$ with the nonnegative bounds $\underline{a_{ij}}$ and $\overline{a_{ij}}$, which respectively correspond to the lower bound matrix $\underline{A}$ and the upper bound matrix $\overline{A}$. Denote the digraph associated with adjacency matrices $\underline{A}$ and $\overline{A}$ by $\mathcal{G}(\underline{A})$ and $\mathcal{G}(\overline{A})$, respectively. Obviously, $\mathcal{G}(\underline{A})$ is a spanning subgraph of $\mathcal{G}(A)$, and both $\mathcal{G}(\underline{A})$ and $\mathcal{G}(A)$ are spanning subgraphs of $\mathcal{G}(\overline{A})$, and their associated neighbor sets of DER$_i$ satisfy $\underline{N_i} \subseteq N_i \subseteq \overline{N_i}$.

The voltage and frequency may possess different network structures and weights. To derive the connectivity requirements for each variable, this paper relates to three digraphs, $\hat{\mathcal{G}}(A^V)$, $\hat{\mathcal{G}}(A^\omega)$, and $\mathcal{G}(A^P)$, corresponding to the networks of frequency, voltage, and active power, respectively.

III. DSC Scheme with Discrete Control Inputs

In practice, the DSC scheme can be implemented by the communication equipment and network, by which the continuous variables $V_i^{\rm od}$, ω_i, Q_i and P_i are discretized. Thus, different from the traditional secondary control approaches with continuous-time control dynamics [8],[12], this section will present a new DSC scheme with discrete-time control inputs to achieve the voltage and frequency restoration and the power sharing accuracy, respectively.

We firstly transform system (2) into a discrete-time system with sampling period T_s. Time is discretized into an finite time sequence of nonempty and bounded intervals, $[t_k, t_{k+1})$ with $t_0 = 0$ and $k = 0, 1, 2, \cdots$, representing the kth round iteration index, as shown in Fig. 3. During each interval $[t_k, t_{k+1})$, there is a sequence of nonoverlapping subintervals $[t_k^0, t_k^1)$, $[t_k^1, t_k^2)$, $\cdots$, $[t_k^{T^*-1}, t_k^{T^*})$ with $t_k^0 = t_k, t_k^{T^*} = t_{k+1}$, satisfying $t_k^{\ell+1} - t_k^\ell = T_s$ for any non-negative integers k and ℓ. Thus, there are totally T^* times state update (iteration) in each time interval $[t_k, t_{k+1})$, however, the control inputs will be designed to only update at the end of the kth iterative process, i.e., $[t_k^{T^*}, t_k^{T^*} + \Delta t)$ with $\Delta t \ll T_s$. For simplicity, we call T^* the step length of the control input update, and $t_k^{T^*} = k \cdot T^* \cdot T_s$ the terminal time of the system state output.

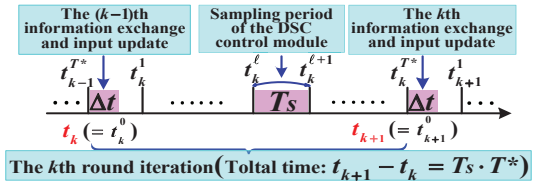


Fig. 3. Time diagram of the proposed DSC strategy.

Then, the discrete-time system states are updated as

$$V_i^{\rm od}(t_k^{\ell+1}) = V_i^{\rm od}(t_k^\ell) + u_{i,k}^V,\ \omega_i(t_k^{\ell+1}) = \omega_i(t_k^\ell) + u_{i,k}^\omega, \quad (3)$$

$$P_i(t_k^{\ell+1}) = P_i(t_k^\ell) + u_{i,k}^P,\ Q_i(t_k^{\ell+1}) = Q_i(t_k^\ell) + u_{i,k}^Q, \quad (4)$$

where $u_{i,k}^V$, $u_{i,k}^\omega$, $u_{i,k}^P$, and $u_{i,k}^Q$ are the distributed voltage, frequency, active, and reactive power controllers. According to the droop control principle given in equation (2), the nominal set points for the ith DER can be derived as

$$\begin{cases} V_i^{\rm nom}(t_k^{\ell+1}) = V_i^{\rm od}(t_k^{\ell+1}) + K_i^Q Q_i(t_k^{\ell+1}) \\ \qquad = V_i^{\rm od}(t_k^\ell) + K_i^Q Q_i(t_k^\ell) + u_{i,k}^V + K_i^Q u_{i,k}^Q \\ \qquad = V_i^{\rm nom}(t_k^\ell) + U_{i,k}^{VQ}, \\ \omega_i^{\rm nom}(t_k^{\ell+1}) = \omega_i(t_k^{\ell+1}) + K_i^P P_i(t_k^{\ell+1}) \\ \qquad = \omega_i(t_k^\ell) + K_i^P P_i(t_k^\ell) + u_{i,k}^\omega + K_i^P u_{i,k}^P \\ \qquad = \omega_i^{\rm nom}(t_k^\ell) + U_{i,k}^{\omega P}, \end{cases} \quad (5)$$

where $U_{i,k}^{VQ} \triangleq u_{i,k}^V + K_i^Q u_{i,k}^Q$ and $U_{i,k}^{\omega P} \triangleq u_{i,k}^\omega + K_i^P u_{i,k}^P$ are respectively the control inputs of the nominal set points.

Due to the inherent contradiction between precise voltage regulation and reactive power sharing in low-voltage MGs, we mainly focus on the precise voltage regulation. Then, the reactive power control inputs, $u_{i,k}^Q$, can be adopted from [8,19] as $u_{i,k}^Q = -\omega_c Q_i(t_k^\ell) + \omega_c Q_i^m(t_k^\ell)$, where ω_c is the cut-off frequency of the low-pass filters, Q_i^m is the instantaneous reactive power components calculated from the measured output voltage and current, as shown in Fig. 2.

We aim to regulate the voltage magnitudes and frequencies of all DERs to achieve the desired values and all DERs' active powers to achieve precise power sharing exactly at the terminal time $t_k^{T^*}$, which belongs to a class of desired finite-time synchronization problem [22]. However, the current control protocols, stability analysis, and the control objective are completely different. From this perspective, the proposed DSC scheme is essentially different from the secondary control problem considered in [8],[12],[14]. Then, the main objective

is to design the discrete-time controllers $u_{i,k}^V$, $u_{i,k}^\omega$, and $u_{i,k}^P$ such that the system terminal outputs, $V_i^{\rm od}(t_k^{T^*})$, $\omega_i(t_k^{T^*})$, and $P_i(t_k^{T^*})$, respectively satisfy

$$\lim_{k\to\infty} V_i^{\rm od}(t_k^{T^*}) = V^{\rm DES},\ \lim_{k\to\infty} \omega_i(t_k^{T^*}) = \omega^{\rm DES}, \quad (6)$$

$$\lim_{k\to\infty} (P_i(t_k^{T^*})/P_{i,\max} - P_j(t_k^{T^*})/P_{j,\max}) = 0, \quad (7)$$

for all $i \neq j = 1,\cdots,N$, where $P_{i,\max}$ is DER$_i$'s active power rating, $V^{\rm DES}$ and $\omega^{\rm DES}$ are the constant desired values of voltage and frequency, respectively.

Recall Fig. 3, during the kth round iteration, the state variables, $V_i^{\rm od}(t)$, $\omega_i(t)$, and $P_i(t)$, will be updated at each discrete time $t = t_k^1,\cdots,t_k^\ell,\cdots,t_k^{T^*}$ with the invariant control inputs $u_{i,k}^V$, $u_{i,k}^\omega$, and $u_{i,k}^P$, respectively. However, the information exchanges among DERs (used to constitute the control inputs) begins at $t = t_k^{T^*}$ and finishes at $t = t_k^{T^*} + \Delta t$, then $u_{i,k}^V$, $u_{i,k}^\omega$, and $u_{i,k}^P$ needs to be updated subsequently only once.

A. Restoration of Voltage Magnitudes and Frequencies

We design the following discrete-time controllers, $u_{i,k}^V$ and $u_{i,k}^\omega$, by incorporating the relative outputs between neighboring DERs at the terminal time $t_k^{T^*}$ into the updating law

$$\begin{cases} u_{i,k+1}^V = \sum_{j\in N_i^V} c\gamma_{ij}^V a_{ij}^V \left[V_j^{\rm od}(t_k^{T^*}) - V_i^{\rm od}(t_k^{T^*})\right] \\ \qquad\quad + c\gamma_{i0}^V a_{i0}^V \left[V^{\rm DES} - V_i^{\rm od}(t_k^{T^*})\right], \\ u_{i,k+1}^\omega = \sum_{j\in N_i^\omega} c\gamma_{ij}^\omega a_{ij}^\omega \left[\omega_j(t_k^{T^*}) - \omega_i(t_k^{T^*})\right] \\ \qquad\quad + c\gamma_{i0}^\omega a_{i0}^\omega \left[\omega^{\rm DES} - \omega_i(t_k^{T^*})\right], \end{cases} \quad (8)$$

for $i = 1,\cdots,N$, where the weighted adjacency matrices of voltage and frequency are $A^V = (a_{ij}^V)_{N\times N} \in [\underline{A^V}, \overline{A^V}]$ and $A^\omega = (a_{ij}^\omega)_{N\times N} \in [\underline{A^\omega}, \overline{A^\omega}]$, respectively. The corresponding leader adjacency matrices are $B^V = {\rm diag}\{a_{10}^V,\cdots a_{N0}^V\} \in [\underline{B^V}, \overline{B^V}]$ and $B^\omega = {\rm diag}\{a_{10}^\omega,\cdots a_{N0}^\omega\} \in [\underline{B^\omega}, \overline{B^\omega}]$, respectively. c is a positive constant representing the coupling strength of the cyber-network. Further, the associated gain matrices are respectively $\Gamma^V = (\gamma_{ij}^V)_{N\times N}$, $\Gamma^\omega = (\gamma_{ij}^\omega)_{N\times N}$, $\Xi^V = {\rm diag}\{\gamma_{10}^V,\cdots,\gamma_{N0}^V\}$, and $\Xi^\omega = {\rm diag}\{\gamma_{10}^\omega,\cdots,\gamma_{N0}^\omega\}$ that to be deigned.

The distributed voltage and frequency controllers (3) under control inputs (8) will enable the control objective (6) to be achieved asymptotically provided certain conditions are satisfied. Now we derive the conditions.

Denote $V^{\rm od} = (V_1^{\rm od},\cdots,V_N^{\rm od})^T$, $\omega = (\omega_1,\cdots,\omega_N)^T$, $u_k^V = (u_{1,k}^V,\cdots,u_{N,k}^V)^T$, and $u_k^\omega = (u_{1,k}^\omega,\cdots,u_{N,k}^\omega)^T$, then rewrite the distributed controllers (3) and control inputs (8) as

$$\begin{cases} V^{\rm od}(t_k^{T^*}) = V^{\rm od}(t_{k-1}^{T^*}) + T^* u_k^V, \\ \omega(t_k^{T^*}) = \omega(t_{k-1}^{T^*}) + T^* u_k^\omega, \end{cases} \quad (9)$$

and

$$\begin{cases} u_{k+1}^V = -\left(c\tilde{L}^V + cB^V \odot \Xi^V\right) V^{\rm od}(t_k^{T^*}) \\ \qquad\quad + \left(cB^V \odot \Xi^V\right) \otimes 1_N V^{\rm DES}, \\ u_{k+1}^\omega = -\left(c\tilde{L}^\omega + cB^\omega \odot \Xi^\omega\right) \omega(t_k^{T^*}) \\ \qquad\quad + (cB^\omega \odot \Xi^\omega) \otimes 1_N \omega^{\rm DES}, \end{cases} \quad (10)$$

where $\tilde{L}^V$ and $\tilde{L}^\omega$ are respectively defined as

$$\tilde{l}_{ij}^V = \begin{cases} \sum_{q\in N_i^V} a_{iq}^V \gamma_{iq}^V, j = i, \\ -a_{ij}^V \gamma_{ij}^V, \qquad j \neq i, \end{cases} \quad \tilde{l}_{ij}^\omega = \begin{cases} \sum_{q\in N_i^\omega} a_{iq}^\omega \gamma_{iq}^\omega, j = i, \\ -a_{ij}^\omega \gamma_{ij}^\omega, \qquad j \neq i. \end{cases}$$

Combining (9) and (10) gives

$$\begin{pmatrix} \tilde{V}(t_{k+1}^{T^*}) \\ \tilde{\omega}(t_{k+1}^{T^*}) \end{pmatrix} = \begin{bmatrix} \tilde{H}^V & O_{N\times N} \\ O_{N\times N} & \tilde{H}^\omega \end{bmatrix} \begin{pmatrix} \tilde{V}(t_k^{T^*}) \\ \tilde{\omega}(t_k^{T^*}) \end{pmatrix}, \quad (11)$$

where $\tilde{V} = ((V^{\rm od})^T, V^{\rm DES})^T$, $\tilde{\omega} = (\omega^T, \omega^{\rm DES})^T$, $\tilde{H}^V = [H^V, T^*(cB^V \odot \Xi^V) \otimes 1_N; O_{N\times 1}, 1]$, and $\tilde{H}^\omega = [H^\omega, T^*(cB^\omega \odot \Xi^\omega) \otimes 1_N; O_{N\times 1}, 1]$ with $H^V = I_N - T^*(c\tilde{L}^V + cB^V \odot \Xi^V)$ and $H^\omega = I_N - T^*(c\tilde{L}^\omega + cB^\omega \odot \Xi^\omega)$.

Clearly, $\begin{bmatrix} \tilde{H}^V & O_{N\times N} \\ O_{N\times N} & \tilde{H}^\omega \end{bmatrix}^k = \begin{bmatrix} (\tilde{H}^V)^k & O_{N\times N} \\ O_{N\times N} & (\tilde{H}^\omega)^k \end{bmatrix}$. If we can choose the elements of Γ^V, Ξ^V, Γ^ω, and Ξ^ω, such that

$$\begin{cases} T^* \left(\sum_{j\in\bar{N}_i^V} c\overline{a_{ij}^V}\gamma_{ij}^V + c\overline{a_{i0}^V}\gamma_{i0}^V\right) < 1,\ \forall i,j = 1,\ldots,N, \\ T^* \left(\sum_{j\in\bar{N}_i^\omega} c\overline{a_{ij}^\omega}\gamma_{ij}^\omega + c\overline{a_{i0}^\omega}\gamma_{i0}^\omega\right) < 1,\ \forall i,j = 1,\ldots,N, \end{cases} \quad (12)$$

then both $\tilde{H}^V$ and $\tilde{H}^\omega$ have only one eigenvalue $\rho(\tilde{H}^V) = \rho(\tilde{H}^\omega) = 1$ provided each of the digraphs $\hat{\mathcal{G}}(\underline{A^V})$ and $\hat{\mathcal{G}}(\underline{A^\omega})$ contains a spanning directed tree. Thus, it follows from Lemma 1 in Appendix that

$$\lim_{k\to\infty} \begin{bmatrix} \tilde{H}^V & O_{N\times N} \\ O_{N\times N} & \tilde{H}^\omega \end{bmatrix}^k = \begin{bmatrix} 1_{N+1}(\beta^V)^T & O_{N\times N} \\ O_{N\times N} & 1_{N+1}(\beta^\omega)^T \end{bmatrix}, \quad (13)$$

where $\beta^V \geq 0$ and $\beta^\omega \geq 0$ are respectively the normalized left eigenvectors of $\tilde{H}^V$ and $\tilde{H}^\omega$ corresponding to eigenvalue 1. By the forms of $(\tilde{H}^V)^k$ and $(\tilde{H}^\omega)^k$, we obtain that

$$1_{N+1}\beta^V = \begin{pmatrix} * & * \\ O_{N\times 1} & 1 \end{pmatrix},\ 1_{N+1}\beta^\omega = \begin{pmatrix} * & * \\ O_{N\times 1} & 1 \end{pmatrix}.$$

Then, we get $\beta^V = (0,\cdots,0,1)^T$ and $\beta^\omega = (0,\cdots,0,1)^T$, this together with (11) and (13) give the desired objective (6).

Now we conclude that if the elements of gain matrices, Γ^V, Ξ^V, Γ^ω, and Ξ^ω, are selected to satisfy condition (12), then the designed distributed discrete-time voltage and frequency controllers (3) with control inputs (8) can restore all DERs' voltage magnitudes and frequencies in a MG to their desired values as long as each of the communication digraphs $\hat{\mathcal{G}}(\underline{A^V})$ and $\hat{\mathcal{G}}(\underline{A^\omega})$ contains a spanning directed tree.

B. Active Power Sharing

Since there is no any priori information about the actual ideal output ratios of the active power for each DER in case of load changes or the switch of plug and play, the active power controller is designed without any reference information and is actually a kind of consensus-based algorithm. We then design the following discrete-time controller, u_i^P, by incorporating the relative active power outputs among neighboring DERs at the terminal time $t_k^{T^*}$ into the update law:

$$u_{i,k+1}^P = \sum\nolimits_{j\in N_i^P} c\gamma_{ij}^P a_{ij}^P \left[K_j^P P_j(t_k^{T^*}) - K_i^P P_i(t_k^{T^*})\right] / K_i^P, \quad (14)$$

for all $i = 1,2,\cdots,N$, where the weighted adjacency matrix $A^P = (a_{ij}^P)_{N\times N} \in [\underline{A^P}, \overline{A^P}]$, and the associated gain matrix is $\Gamma^P = (\gamma_{ij}^P)_{N\times N}$ to be determined.

Similarly, the distributed active power controller (4) under control inputs (14) will also enable the control objective (7)

to be achieved asymptotically provided certain conditions are satisfied. We next derive the conditions.

Denote $p = (P_1 K_1^P, \cdots, P_N K_N^P)^T$, $\tilde{L}^P = (\tilde{l}_{ij}^P)_{N\times N}$ with

$$\tilde{l}_{ij}^P = \begin{cases} \sum_{q\in N_i^P} a_{iq}^P \gamma_{iq}^P, & j = i, \\ -a_{ij}^P \gamma_{ij}^P, & j \neq i, \end{cases}$$

and $\hat{u}_k^p = (u_{1,k}^P, \cdots, u_{N,k}^P)^T$, then rewrite (4) and (14) as

$$p(t_k^{T^*}) = p(t_{k-1}^{T^*}) + T^* \hat{u}_k^p, \tag{15}$$

and

$$\hat{u}_{k+1}^p = -c\tilde{L}^P p(t_{k-1}^{T^*}). \tag{16}$$

Combining (15) and (16) gives

$$p(t_{k+1}^{T^*}) = (I_N - T^* c\tilde{L}^P) p(t_k^{T^*}). \tag{17}$$

Obviously, if the elements of Γ^P are selected to satisfy

$$\sum\nolimits_{j\in\bar{N}_i^P} c\overline{a_{ij}^P}\gamma_{ij}^P T^* < 1, \ \forall i, j = 1, \ldots, N, \tag{18}$$

then $I_N - T^* \tilde{L}^P$ has only one eigenvalue $\rho(I_N - T^* c\tilde{L}^P) = 1$ provided the digraph $\mathcal{G}(\underline{A^P})$ contains a spanning directed tree. Thus, by Lemma 1, we get

$$\lim_{k\to\infty} (I_N - T^* c\tilde{L}^P)^k = 1_N (\beta^P)^T \tag{19}$$

with the normalized left eigenvector $\beta^P \geq 0$ corresponding to eigenvalue 1. Then, by the above denotation of p, we deduce

$$K_1^P P_1 = K_2^P P_2 = \ldots = K_N^P P_N. \tag{20}$$

Since the droop coefficients of active powers, K_i^P, are chosen based on the active power ratings of DER$_i$, $P_{i,\max}$, then the objective (7) is achieved.

Now we conclude that if the elements of gain matrix, Γ^P, are selected to satisfy condition (18), then the designed distributed discrete-time active power controller (4) with control inputs (14) can drive all DERs in a MG to share their active powers precisely as long as the communication digraph $\mathcal{G}(\underline{A^P})$ contains a spanning directed tree.

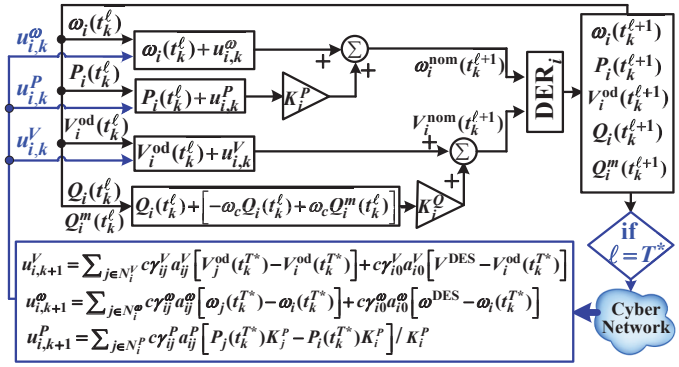


Fig. 4. The block diagram of the proposed DSC scheme.

The whole DSC framework is drawn in Fig. 4. As seen, the nominal set points, $V_i^{\rm nom}(t_k^{T^*})$ and $\omega_i^{\rm nom}(t_k^{T^*})$, obtained by equation (5), are sent to the primary control layer to synchronize each DER's output voltage and frequency, $V_i^{\rm od}$ and ω_i, to their desired reference states, $V^{\rm DES}$ and $\omega^{\rm DES}$. The detailed implementation can be designed as follows:

Step 1: **Initialization:** Set the reference trajectory $V^{\rm DES}$ and $\omega^{\rm DES}$, the initial inputs, $u_{i,0}^V$, $u_{i,0}^\omega$, and $u_{i,0}^P$, and the initial states, $V_i^{\rm od}(0)$, $\omega_i(0)$, and $P_i(0)$ for all $i = 1, \cdots, N$. Let the iteration index $k = 1$ and the tolerance ϵ^V, ϵ^ω, and $\epsilon^P > 0$.

Step 2: **Calculate gain matrices:** Determine Γ^V, Ξ^V, Γ^ω, Ξ^ω, and Γ^P, according to Algorithm 1.

Step 3: **Calculate nominal set points:** Apply $u_{i,k}^V$, $u_{i,k}^\omega$, and $u_{i,k}^P$ to compute $V_i^{\rm nom}(t_k^\ell)$ and $\omega_i^{\rm nom}(t_k^\ell)$ for $\ell = 0, 1, \cdots, T^*$ and $i = 1, \cdots, N$.

Step 4: **Measure terminal outputs:** Apply $V_i^{\rm nom}(t_k^{T^*})$ and $\omega_i^{\rm nom}(t_k^{T^*})$ to the primary control process and measure the terminal outputs, $V_i^{\rm od}(t_k^{T^*})$, $\omega_i(t_k^{T^*})$, and $P_i(t_k^{T^*})$, for $i = 1, \cdots, N$.

Step 5: **Analyze errors:** If $|V_i^{\rm od}(t_k^{T^*}) - V^{\rm DES}| < \epsilon^V$, $|\omega_i(t_k^{T^*}) - \omega^{\rm DES}| < \epsilon^\omega$, and $|P_i(t_k^{T^*})K_i^P - P_j(t_k^{T^*})K_j^P| < \epsilon^P$ for all $j \neq i = 1, \cdots, N$, then go to step 7; Otherwise go to step 6.

Step 6: **Calculate control inputs:** Let $k = k+1$, and update $u_{i,k}^V$, $u_{i,k}^\omega$, and $u_{i,k}^P$ according to the protocols (8) and (14), then go to step 3.

Step 7: Stop the iteration.

Note that the above Step 5 can be implemented in a distributed mode by an approximate estimation method. In special, recall that the control inputs designed for each DER given in (8) and (14) will finally converge to zero when the control objectives are achieved, thus they can be used to estimate the errors. By this way, each DER will generate a logic signal, representing its own error situation, and then send it to its neighbors. Due to the connectivity of the communication networks, the whole errors of the control objectives can be reflected in the logic signal for each DER after each around of information exchange and iteration update, then they can make decisions whether to stop the iteration accordingly.

Intuitively, the selected gain matrices should not break the original topologies of the communication digraphs. For example, all the active power gains are always selected to satisfy $\gamma_{ij}^P > 0$ when $N_i^P \neq \emptyset$ and $j \in N_i^P$, otherwise $\gamma_{ij}^P = 0$. Also, the voltage and frequency gains $(\gamma_{ij}^V)_{j=0}^N$ and $(\gamma_{ij}^\omega)_{j=0}^N$ own the same requirements. Thus we initialize all gain matrices as their associated communication weights, and further optimize their values by the following Algorithm 1.

Algorithm 1 Calculate gain matrices Γ^V, Ξ^V, Γ^ω, Ξ^ω, Γ^P.

Initialization:

Set $\varepsilon \in (0, 1)$, step length of input update T^*, and let $\{(\gamma_{ij}^V)_{j=0}^N, (\gamma_{ij}^\omega)_{j=0}^N, \gamma_{ij}^P\} \to \{c(\overline{a_{ij}^V})_{j=0}^N, c(\overline{a_{ij}^\omega})_{j=0}^N, c\overline{a_{ij}^P}\}$;

Iterative:

while both (12) and (18) hold **do**

$(\gamma_{ij}^V)_{j=0}^N \leftarrow (2-\varepsilon)(\gamma_{ij}^V)_{j=0}^N$, $\gamma_{ij}^P \leftarrow (2-\varepsilon)\gamma_{ij}^P$, and $(\gamma_{ij}^\omega)_{j=0}^N\} \leftarrow (2-\varepsilon)(\gamma_{ij}^\omega)_{j=0}^N$;

end while

while either (12) or (18) does not hold **do**

$\{(\gamma_{ij}^V)_{j=0}^N, (\gamma_{ij}^\omega)_{j=0}^N, \gamma_{ij}^P\} \leftarrow \varepsilon\{(\gamma_{ij}^V)_{j=0}^N, (\gamma_{ij}^\omega)_{j=0}^N, \gamma_{ij}^P\}$

end while

Set $\{\Gamma^V, \Gamma^\omega, \Gamma^P, \Xi^V, \Xi^\omega\} \to \{(\gamma_{ij}^V), (\gamma_{ij}^\omega), (\gamma_{ij}^P), (\gamma_{i0}^V), (\gamma_{i0}^\omega)\}$.

TABLE I
THE PARAMETER VALUES FOR MG TEST SYSTEM

	DER_1 & DER_3(65 kVA rating)			DER_2 & DER_4(115 kVA rating)		
DERs	V_{DC} : 800 V	$k^P : 1\times10^{-5}$	$k^Q : 3\times10^{-4}$	V_{DC} : 800 V	$k^P : 0.5\times10^{-5}$	$k^Q : 6\times10^{-4}$
	L^{f}: 2 mH	C^{f}: 16 μF	L^{o}: 2 mH	L^{f}: 1.95 mH	C^{f} : 15 μF	L^{o}: 1.95 mH
	$K^V_{\mathrm{PID}} : 10/100/1.5\times10^{-3}$		$K^i_{\mathrm{PI}} : 5/200$	$K^V_{\mathrm{PID}} : 8/110/1.4\times10^{-3}$		$K^i_{\mathrm{PI}} : 4/180$
R&L Lines1-3	0.64 Ω & 1.32 mH			0.51 Ω &1.05 mH		0.58 Ω & 1.21 mH
P&Q Loads1-4	34 kW& 34 $kVar$	44 kW& 44 $kVar$	46 kW& 46 $kVar$	36 kW& 36 $kVar$		

The coefficient $\varepsilon \in (0,1)$ characterizes the changing rate of the gain matrices to achieve their optimal values satisfying conditions (12) and (18). If the initial gain matrices satisfy these conditions, increase them by multiplying $(2-\varepsilon) > 1$ repeatedly. In contrast, reduce them by multiplying $0 < \varepsilon < 1$ repeatedly. By finite iterations, the maximum gain matrices to meet the requirements can be calculated for the given T^*. Since the smaller the coefficient ε, the less the number of iterations required to calculate the optimal gain matrices, and more optimized values of gain matrices will be calculated with a larger coefficient ε, then it is generally necessary to make a tradeoff between the above two factors.

Remark 1: If the upper bounds of the uncertain communication weights are previously known, we need to calculate the gain matrices only once. Then, the proposed DSC scheme can be implemented with the same gain matrices throughout the control process. However, for some more general cases where the upper bounds are unknown previously, a distributed control algorithm to obtain the control gain matrices should be designed. This will be our future research direction.

Remark 2: An ideal voltage controller should allow for a tunable compromise between voltage regulation and reactive power sharing [15]. Also, resetting voltages to a constant value is a little constraining in standard medium-voltage grids. Thus, we have designed a continuous time distributed secondary voltage controller together with a distributed voltage estimator, which not only guarantee the precise reactive power sharing but also allow the weighted average voltage of all DERs to converge to the desired reference value [23]. Although reactive power sharing problem is also important for the stability of the whole MG, it is still difficult to design a tunable voltage and reactive power controller by using discrete-time distributed control inputs that are updated in an intermittent communication manner. This will be our future work.

Remark 3: The proposed robust DSC scheme is an effective method to perfectly track the desired voltage and frequency values within the terminal time. Each DER only requires information about their owns and some nearest neighbors' to achieve synchronization. Even if there are interval uncertainties of the communication links (caused by the high frequency component of disturbances on voltages or currents) and/or transient power oscillation noises (caused by the flow of large currents), the synchronization can still be achieved if only the network contains a spanning tree. Since the distributed control structure can suit interval uncertainty networks, it is more robust against communication disturbances.

IV. PERFORMANCE VALIDATION

In this section, the effectiveness of the proposed DSC algorithms will be verified by simulating an islanded MG in MATLAB/SimPowerSystems. Fig. 5 shows the basic diagram of the MG test system which consists of four DERs along the feeder through the step-down transformers, four local loads, three lines, and the specifications are summarized in Table I.

Let the sampling period of the designed discrete-time DSC control module $T_s = 0.002$s, and the step length of input update $T^* = 100$. Thus, the control inputs, $u^{\omega}_{i,k}$, $u^{V}_{i,k}$, and $u^{P}_{i,k}$, will be updated in every $T_s \times T^* = 0.2$s (see Fig. 3).

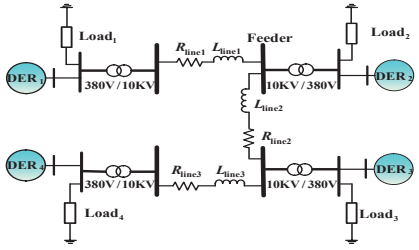


Fig. 5. A single line diagram of the test MG system.

The implemented communication digraphs are given in Fig. 6 with interval uncertain weights. As seen, the virtual leader-DER_0 in $\hat{\mathcal{G}}(A^V)$ and $\hat{\mathcal{G}}(A^{\omega})$ is used to send the desired values to DER_1, but it is not affected by other DERs. The desired terminal voltage RMS (root mean square) of DERs, V^{DES} and ω^{DES}, are set as 380V (the line voltage of three phases) and 314rad/s, respectively.

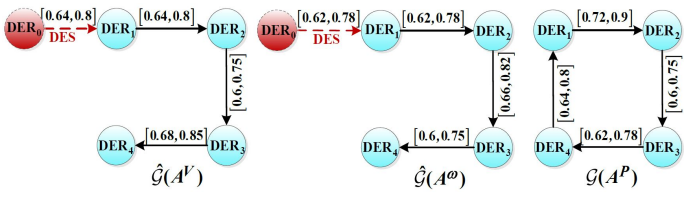
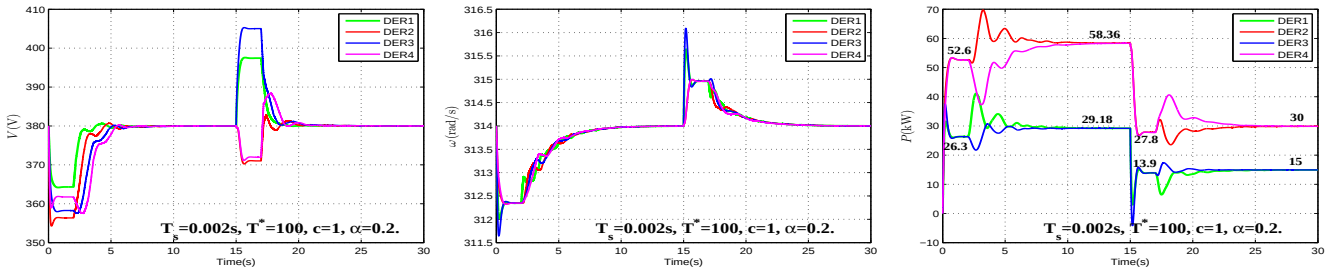


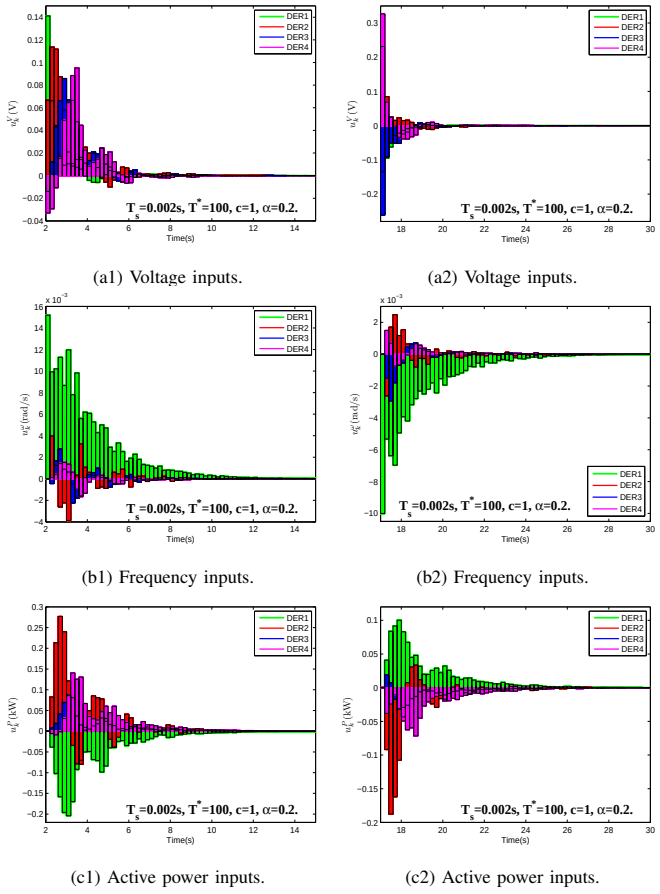
Fig. 6. The communication digraphs with interval uncertain weights.

With the upper bounds, $\overline{a^V_{ij}}$, $\overline{a^{\omega}_{ij}}$, and $\overline{a^P_{ij}}$, of the uncertain weights (see Fig. 6), the coupling strength $c = 1.125$, and the step length of input update $T^* = 100$, the learning matrices, $\Gamma^V = 0.01A^V$, $\Gamma^{\omega} = 0.01A^{\omega}$, $\Gamma^P = 0.01A^P$, $\Xi^V = 0.01B^V$, $\Xi^{\omega} = 0.01B^{\omega}$, can be calculated by Algorithm 1 (Set $\varepsilon = 0.9$, the total iterative number is 7 and elapsed time is 0.000344s.). Obviously, these gain matrices are also effective for a smaller coupling strength $c = 1$.



(a) Voltage response. (b) Frequency response. (c) Active power output.

Fig. 7. State evolutions of voltage, frequency, and active power in case of load variation.



(a1) Voltage inputs. (a2) Voltage inputs.

(b1) Frequency inputs. (b2) Frequency inputs.

(c1) Active power inputs. (c2) Active power inputs.

Fig. 8. Control input evolutions in case of load variation.

It should be noted that, the derived weakest connectivity requirements respectively for the communication digraphs, $\hat{\mathcal{G}}(A^V)$, $\hat{\mathcal{G}}(A^\omega)$, and $\mathcal{G}(A^P)$, are the same, i.e., containing a spanning directed tree. In this sense, as a special case, we can also set the three different digraphs shown in Fig. 6 as one unified digraph with the uniform communication weights in order to facilitate the implementation. However, to further reflect the robustness of the proposed DSC scheme to different networks with different weights, we intentionally impose different control variables with different communication digraphs, as shown in Fig. 6.

Take the uncertain communication weights, e.g. a_{ij}^V, as $a_{ij}^V = (1-\alpha)\overline{a_{ij}^V} + \alpha\overline{a_{ij}^V}\text{rand}$, where the parameter $\alpha \in (0,1)$ characterizes the degree of uncertainty and the Matlab command *rand* can randomly generate an element between 0 and 1. Other uncertain weights can be similarly taken. Herein, let $\alpha = 0.2$ if there is no special explanation. We next study the control performance of the islanded MG under four scenarios: 1) load changes, 2) plug and play capability, 3) link failure, and 4) control parameter test.

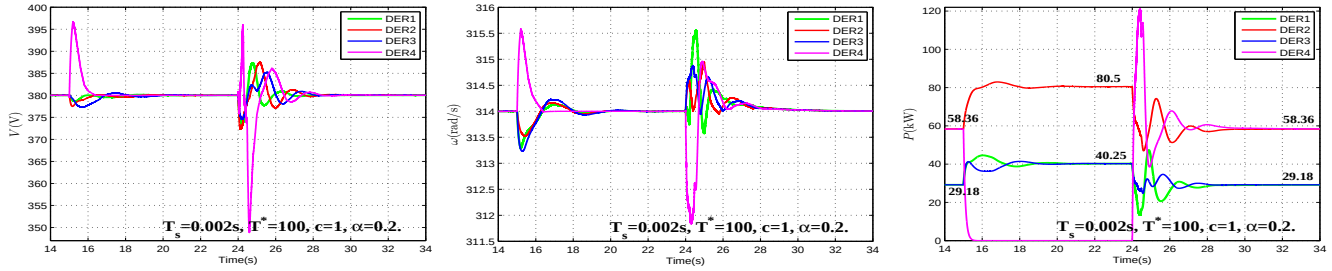
A. Load Change Performance Assessment

The control performance in case of load change is studied in Figs. 7-8. To make the transient process of voltage/frequency regulation more obvious, the DSC scheme is intentionally applied 2s after the load changes.

The MG begins to operate in island mode at $t = 0$s with Loads 1-4. As seen in Fig. 7, both the voltage and frequencies of all DERs go to different values less than the desired values due to primary control, while the active power outputs increase to different values. Since $\text{DER}_{1,3}$ and $\text{DER}_{2,4}$ respectively possess the same parameters (see Table I), their voltages and active power outputs have the similar evolutionary trend. As frequency is a global variable, all DERs' frequencies converge to the same value. When the DSC scheme is applied at $t = 2$s, both the output voltages and operating frequencies begin to return to their desired values, as shown in Figs. 7(a-b). Also, the proposed DSC scheme does not destroy the existing allocation pattern of the active power output generated by the primary control, as shown in Fig. 7(c).

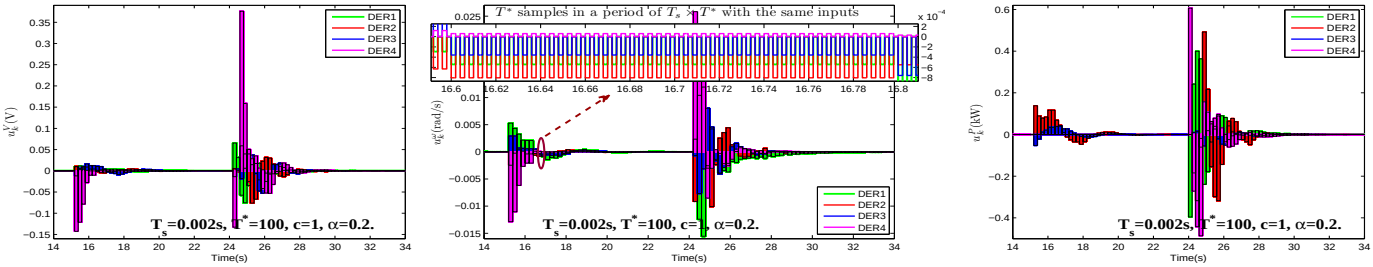
Then, we remove the local Load_1 and Load_3 at $t = 15$s. As seen in Fig. 7(a), the voltage magnitudes of $\text{DER}_{1,3}$ begin to increase due to the instant reduction of local $\text{Load}_{1,3}$. Simultaneously, the voltage magnitudes of $\text{DER}_{2,4}$ start dropping due to the impact of the instant power flow. After activating the DSC scheme at $t = 17$s, the evolutionary trends of all DERs' voltage magnitudes, frequencies, and active power outputs are nearly contrast to the case of load increase, and the final voltage/frequency restoration and accurate power sharing can still be observed in Fig. 7.

Fig. 8 shows the evolutions of the distributed control inputs of all DERs. Since DER_1 is the unique node that directly connected to the virtual leader-DER_0 (see Fig. 6), it has the fastest response speed and then leads to the maximum changing amplitude. According to the previously given input update period $T_s \times T^* = 0.2$s, we calculate that the control inputs (shown in Fig. 8) are updated totally $k = 65$ times in



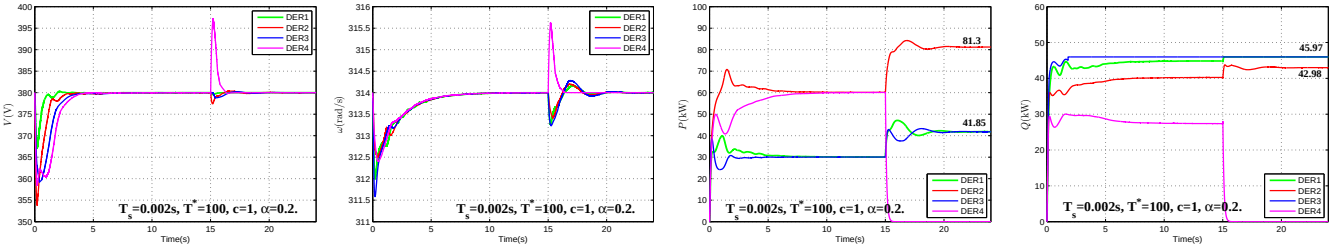
(a) Voltage response. (b) Frequency response. (c) Active power output.

Fig. 9. State evolutions of voltage, frequency, and active power in case of DER plug and play.



(a) Voltage inputs. (b) Frequency inputs. (c) Active power inputs.

Fig. 10. Evolutions of distributed control inputs in case of DER plug and play.



(a) Voltage response. (b) Frequency response. (c) Active power output. (d) Reactive power output.

Fig. 11. State evolutions of voltage, frequency, and active power in case of the power outputs of some DERs achieve their limits.

each of the time intervals $2\text{s} \leq t \leq 15\text{s}$ and $17\text{s} \leq t \leq 30\text{s}$. As seen, the control inputs of each DER converge to zero when the voltage and frequency restoration is achieved. Moreover, due to the uncertainty of the communication links, the control inputs are changing randomly and non-smoothly.

Although the adopted digraphs are with uncertain communication weights (interval uncertainties caused by the external noises), and not all DERs can access the precise reference information sent by DER_0 (be informed of limited parameter information determined by the internal communication network structure), the proposed DSC scheme is still robust against these uncertainties and disturbances.

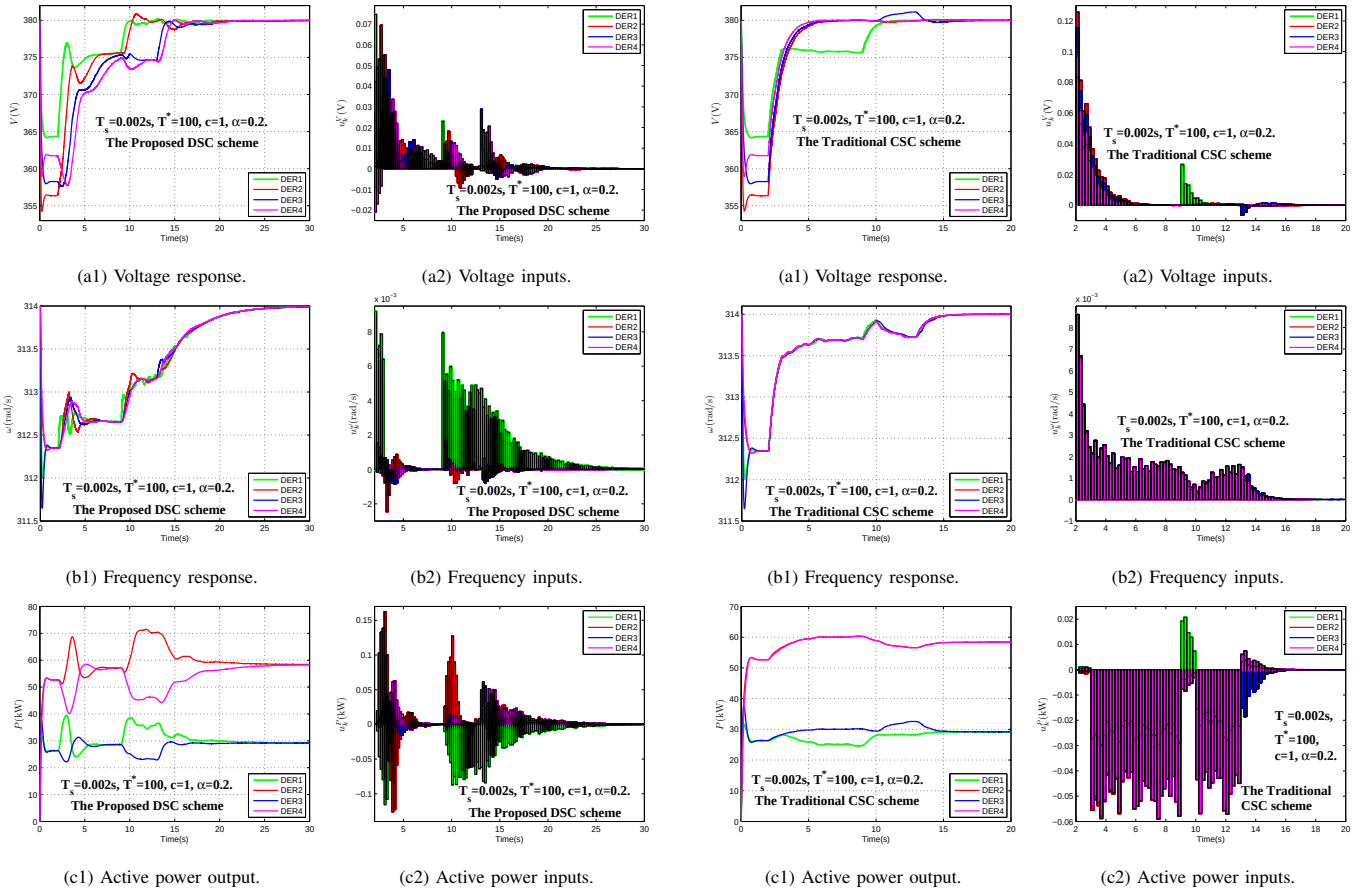
B. Plug and Play Capability

The effectiveness of the plug and play capability is analyzed here. The islanded MG is operating at $t = 0\text{s}$ with Loads 1-4, and the DSC scheme is simultaneously activated. It is assumed that DER_4 is plugged out and plugged back at $t = 15\text{s}$ and $t = 24\text{s}$, respectively. The corresponding state and control input evolutions are drawn in Figs. 9-10.

As seen in Fig. 9, the active power output of DER_4 instantly jump back to 0 after $t = 16\text{s}$, and its voltage and frequency also return to the nominal set points after a sharp rise. Removing DER_4 also implies the loss of communication links of a_{43}^V, a_{43}^ω, a_{43}^P, and a_{14}^P, and thus the control inputs of DER_4 shown in Fig. 10 do not change any more as $t \in [15, 24]\text{s}$. Nevertheless, the rest of the digraphs shown in Fig. 6 still meet the connectivity requirements. Thus, both the voltage magnitudes and frequencies of DERs 1-3 are restored to their desired values within 5s. Also, the proposed controllers readjust the load proportionally sharing among the remaining DERs 1-3, and a new distribution pattern of active power sharing can be then observed in Fig. 9(c).

When DER_4 is plugged back at $t = 24\text{s}$, all DERs' voltage magnitudes and frequencies are regulated to the desired values, and DER_4 affords the original active power output once again. The final excellent voltage and frequency restoration as well as accurate active power sharing can still be observed after $t = 30\text{s}$, which indicates that the proposed DSC scheme also possesses the excellent plug and play capability.

Note that a self-protection mechanism (e.g., saturation con-



(a1) Voltage response. (a2) Voltage inputs.

(b1) Frequency response. (b2) Frequency inputs.

(c1) Active power output. (c2) Active power inputs.

Fig. 12. State and control input evolutions for the DSC scheme in case of link failure.

(a1) Voltage response. (a2) Voltage inputs.

(b1) Frequency response. (b2) Frequency inputs.

(c1) Active power output. (c2) Active power inputs.

Fig. 13. State and control input evolutions for the CSC scheme in case of link failure.

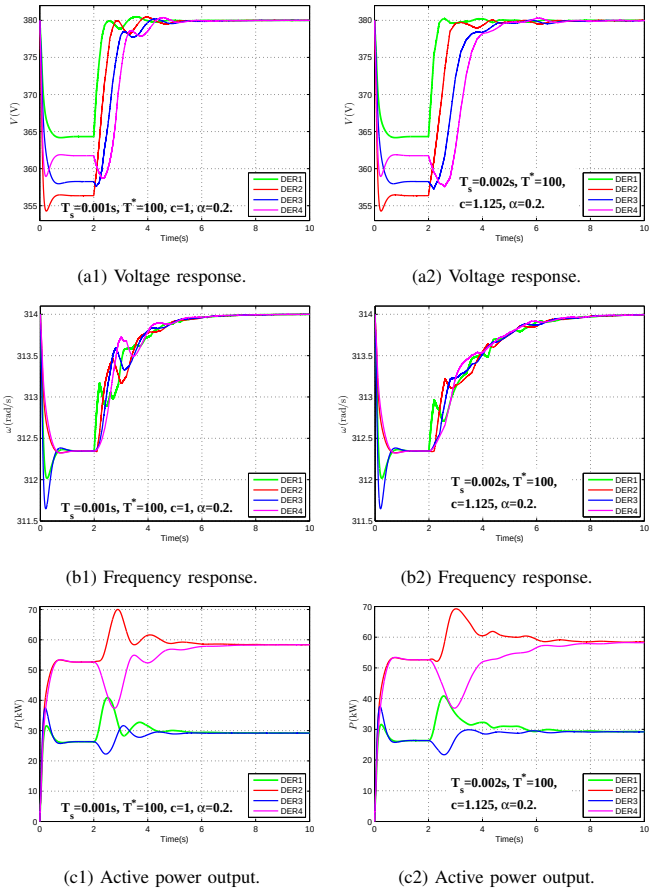
straints) installed in each DER inverter can be used to limit its power outputs if it becomes excessive. Then the associated DER will switch to a special operation mode with constant power outputs, and it will no longer participate in information iteratively exchanged among the other DERs. Afterwards, the rest DERs will automatically redistribute the rest load. To evaluate this, we increase the total load by $4kW + j4kVar$, then when DER_4 is plugged out at $t = 15$s, the active power output of DER_2 will be working beyond its capacity according to the original allocation pattern of power sharing. However, when implemented the switching control mode, DER_2 keeps its constant active power output as it achieves its limit 81.3kW. Then, the rest power demand is afforded by the remaining DERs 1-2, as shown in Fig. 11(c). Although the reactive power sharing is not our focus, we should control the DER inverter to limit the reactive power output if it becomes excessive. Then a voltage regulator containing reactive power constraints should be used. The associated state evolutions are drawn in Fig. 11(d), as seen, the reactive power outputs of DER_2 and DER_4 have reached their limits 45.97kVar. However, the excellent voltage regulation can still be observed in Fig. 11(a).

C. Link Failure Test

We analyze the robustness of the proposed DSC scheme to link failure by comparing it with the traditional centralized secondary control (CSC) scheme [6-8] under the same discrete-time control framework. Since the lack of robustness of CSC scheme with respect to controller failure can be coped with based on model predictive control [24], we only test the link failure situation here. For simplicity, only the load increasing scenario in subsection A is considered. Both the DSC and CSC schemes are activated at $t = 2$s.

For the DSC scheme, assume the link between DER_1 and DER_0 fails at $t = 3$s and is reconnected at $t = 9$s, then the link of DER_2 to DER_3 fails at $t = 10$s and is reconnected at $t = 13$s. For the CSC scheme, all measurements of the voltage, frequency, and active power for each DER are available to the centralized controller DER_0. Thus we assume the measurements of DER_1 are not available to DER_0 at $t = 3$s and re-available at $t = 9$s, then the ones of DER_3 are not available to DER_0 at $t = 10$s and re-available at $t = 13$s. The associated evolutions are shown in Figs. 12 and 13.

Due to the link failure, the voltage, frequency, and active power restoration processes of both DSC and CSC schemes slow down until the link is reconnected. Comparing Fig. 12(a1-c1) with Fig. 13(a1-c1), we conclude that relying on the high-bandwidth communication of the centralized controller, the regulation speed of the CSC scheme is faster than that of the DSC scheme. However, more imbalances among the control inputs of DERs under the CSC scheme can be observed by

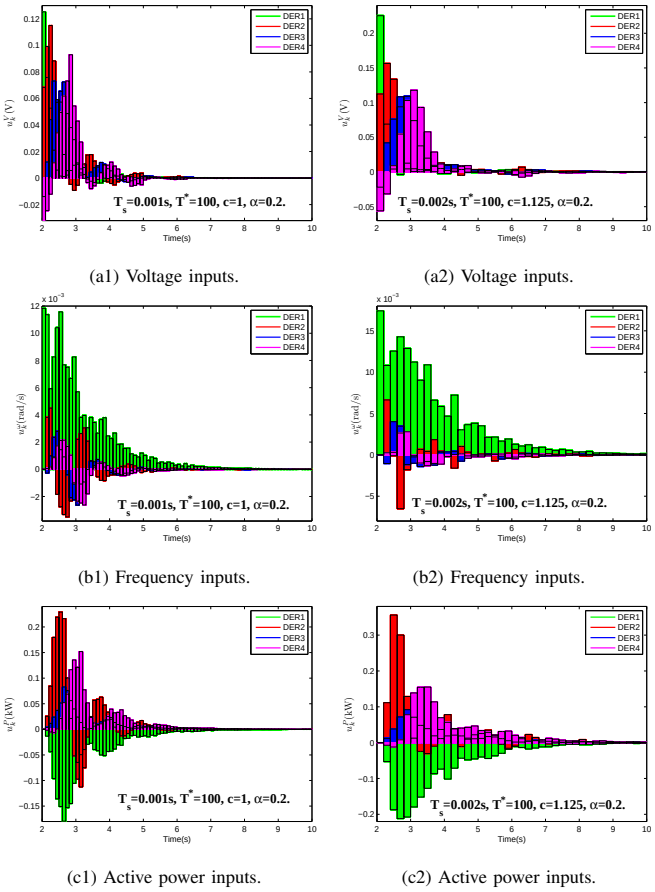


(a1) Voltage response. (a2) Voltage response.

(b1) Frequency response. (b2) Frequency response.

(c1) Active power output. (c2) Active power output.

Fig. 14. State evolutions with different T_s and c.



(a1) Voltage inputs. (a2) Voltage inputs.

(b1) Frequency inputs. (b2) Frequency inputs.

(c1) Active power inputs. (c2) Active power inputs.

Fig. 15. Control input evolutions with different T_s and c.

comparing Fig. 12(a2-c2) with Fig. 13(a2-c2). Thus, although both of the two schemes have their own advantages and disadvantages for different control problems, the proposed DSC scheme is more suitable for MGs containing a large number of DERs in terms of evenly sharing control costs and reducing the communication pressure of single DER.

D. Control Parameter Test

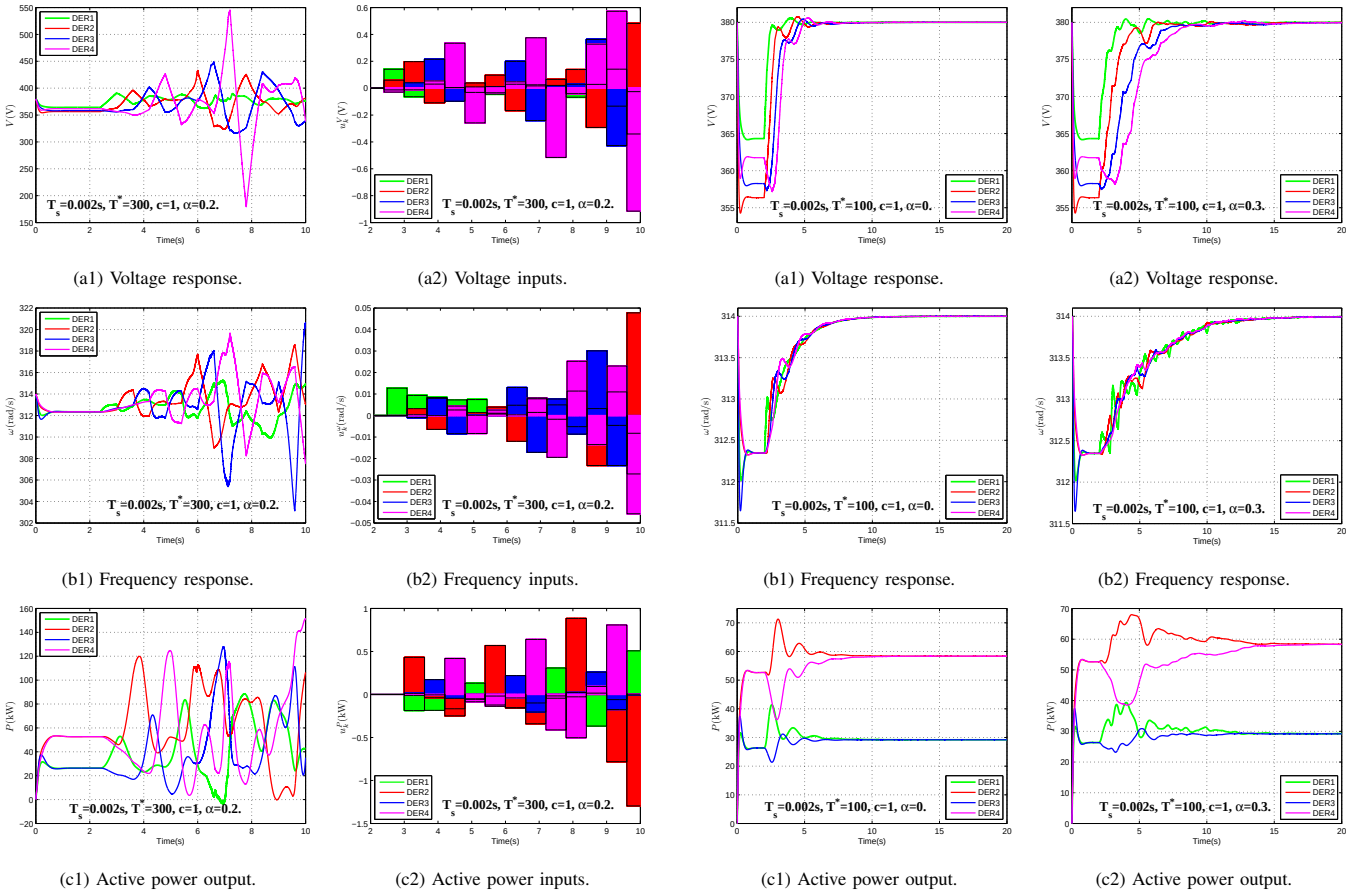
Intuitively, the sampling period T_s, the coupling strength c, the step length of input update T^*, and the degree of uncertainty α, will impact the global control performance. Thus, the test MG system with different control parameters will be simulated here. For simplicity, we only consider the load increasing scenario in subsection A.

Figs. 14-16 show the state and control input evolutions of the controlled system with different T_s, c, and T^*. Compared with Fig. 7, both smaller sampling period $T_s = 0.001$s shown in Fig. 14(a1-c1) and larger coupling strength $c = 1.125$ shown in Fig. 14(a2-c2) lead to a faster convergence speed. However, for a larger step length of input update $T^* = 300$ that does not satisfy conditions (12) and (18), the control objective could not be realized any more, as shown in Fig. 16(a1-c1). Note that different input update periods of $T_s \times T^*$ (e.g. 0.1s in Fig. 14(a1-c1), 0.2s in Fig. 7, and 0.6s in Fig. 16(a1-c1)) lead to different control performance. Hence, for the extreme situation, where the sampling period T_s is sufficiently small to approximate a continuous application of the proposed DSC scheme, the conditions (12) and (18) can still be satisfied to guarantee the stability of the test system. Thus a better tradeoff between control costs and performance should be made.

Figs. 17(a1-c1) and 17(a2-c2) respectively show the state evolution curves of the test MG system with fixed communication link ($\alpha = 0$) and uncertain communication link ($\alpha = 0.3$). Comparing with Fig. 7 ($\alpha = 0.2$), we conclude that a relatively smaller degree of uncertainty, α, will lead to a faster convergence speed. Figs. 18(a1-c1) and 18(a2-c2) reflect that the control inputs are updated more smoothly with a smaller degree of uncertainty.

To test the control performance of the MG with randomly switching communication links, we take the uncertain weights, e.g. a_{ij}^V, as $a_{ij}^V = \overline{a_{ij}^V}\text{randint}$, where the Matlab Command *randint* can randomly generate either 0 or 1, such that the connectivity requirements may not be satisfied. The associated simulations are shown in Fig. 19. However, the excellent control performance can still be observed. It's because that the sampling period, T_s, determines the switching frequency of the random communication link, and appropriate switching frequency can ensure the system stability. Thus, the proposed DSC scheme is also robust against the sparse network with randomly switching communication links if the sampling period is specified appropriately.

Remark 4: The proposed control aims at restoring DER



(a1) Voltage response. (a2) Voltage inputs. (a1) Voltage response. (a2) Voltage response.

(b1) Frequency response. (b2) Frequency inputs. (b1) Frequency response. (b2) Frequency response.

(c1) Active power output. (c2) Active power inputs. (c1) Active power output. (c2) Active power output.

Fig. 16. State and control input evolutions with a larger T^*.

Fig. 17. State evolutions with different α.

voltages to constant values. Under some operating conditions, it may required to adjust DER voltages to prevent the circuits that make up the MG from being overloaded. In this situation, the proposed DSC scheme can be extended by a less correction to handle excessive currents in the MG branches. In detail, the current errors among the branches will be injected into the locally voltage controllers by the current information exchanges among DERs. This will be our future work.

Remark 5: The proposed DSC scheme can also be extended to control voltages at buses with loads but without DERs. we need to re-establish a network of the MG model with heterogeneous nodes, including DER units, Loads, and Energy Storage Systems (ESS), and so on. Since each node possesses different dynamics and time scales, the consequent secondary distributed control strategies may be multi-stage, hybrid, and even heterogeneous. Alternatively, every node (i.e., DER, load bus, ESS) in the MG can be assigned with an "agent", which can automatically manage its own operation mode and exchange its measurements with neighbors. By imposing different action properties on these heterogeneous agents, the proposed DSC scheme can also be extended to control voltages at buses with loads without DER.

V. Conclusion

A robust DSC scheme for the restoration of voltage and frequency as well as active power sharing accuracy on the condition of directed communication links with interval uncertainties has been proposed, under which all DERs in a MG only need to access limited information of the system parameters, and communicate with their neighbors intermittently. Sufficient conditions containing the digraph connectivity requirements and learning gain inequalities that guarantee the system stability have been derived, which enable the proposed discrete-time DSC algorithms to robust to both the internal uncertainties and the external disturbances. The simulation results coincide with the present control methods.

Appendix

Lemma 1:[22] Let λ be an eigenvalue of matrix A, and α and β be two vectors such that (i) $A\alpha = \lambda\alpha$; (ii) $A^{\mathrm{T}}\beta = \lambda\beta$; (iii) $\alpha^{\mathrm{T}}\beta = 1$; (iv) $|\lambda| = \rho(A) > 0$; (v) λ is the only eigenvalue of A with modulus $\rho(A)$. Define $\hbar = \alpha\beta^{\mathrm{T}}$, and then $(\lambda^{-1}A)^{\zeta} = \hbar + (\lambda^{-1}A - \hbar)^{\zeta} \to \hbar$ as $\zeta \to \infty$.

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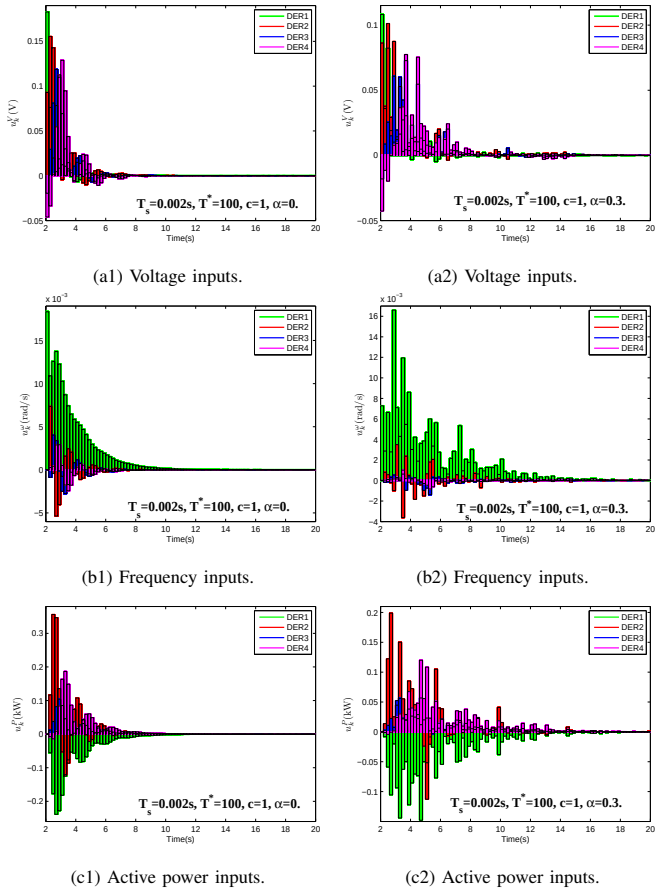
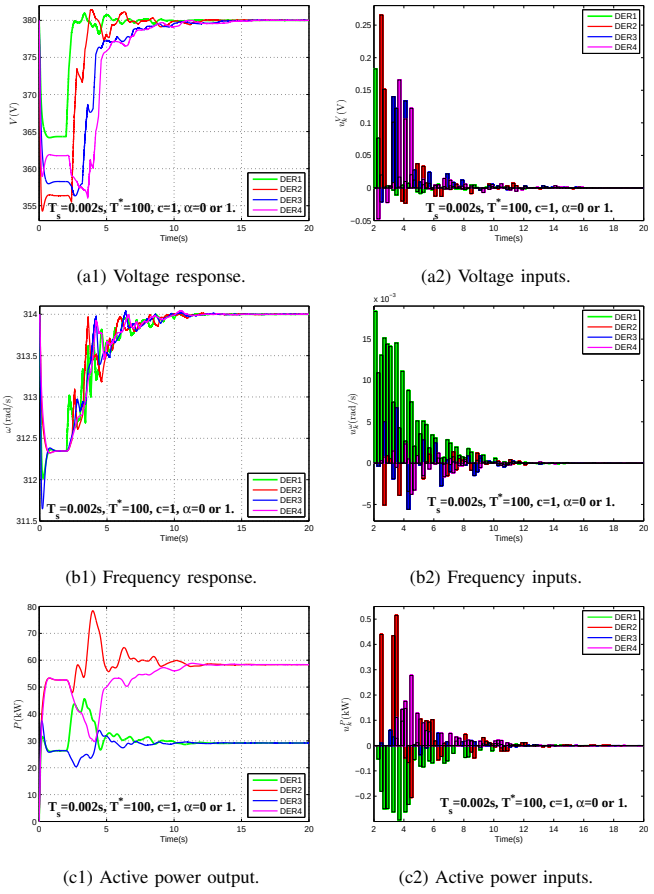


(a1) Voltage inputs. (a2) Voltage inputs.

(b1) Frequency inputs. (b2) Frequency inputs.

(c1) Active power inputs. (c2) Active power inputs.

Fig. 18. Control input evolutions with different α.



(a1) Voltage response. (a2) Voltage inputs.

(b1) Frequency response. (b2) Frequency inputs.

(c1) Active power output. (c2) Active power inputs.

Fig. 19. State and control input evolutions with $\alpha = 0$ or 1.

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