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A Voltage Doubler Circuit to Extend the Soft-switching Range of Dual Active Bridge Converters

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Abstract—A voltage doubler circuit is realized to extend the soft-switching range of Dual Active Bridge (DAB) converters. No extra hardware is added to the DAB to form this circuit, since it is composed of the dc blocking capacitor and the low side full bridge converter, which already exist in DAB. With the voltage doubler, the DAB converter can achieve soft switching and high efficiency when the low side dc voltage is close to 2 pu (1 pu is the high side dc voltage divided by the transformer turn ratio), which can be realized only when the low side dc voltage is close to 1 pu by using the conventional phase shift modulation in DAB. Thus the soft switching range is extended. The soft switching boundary conditions are derived. A map to show the soft switching or hard switching in the full load and voltage range is obtained. The feasibility and effectiveness of the proposed method is finally verified by experiments.

In this paper, a voltage doubler circuit is proposed in DAB to achieve a wide soft switching range even when the output voltage is doubled. Without extra hardware, the voltage doubler circuit is formed by the components already existing in the DAB. The voltage doubler circuit is realized by still using PSM with a little modification. The operation principle of proposed method is demonstrated, the soft switching area is obtained by deriving the soft switching boundary conditions, the analysis is finally verified by experimental results.

II. OPERATION PRINCIPLE

A DAB converter consists of two full bridges (formed by \(Q_1 \sim Q_8\)), a transformer \(T\) (turn ratio \(n:1\)), an inductor \(L_s\), two DC blocking capacitors \(C_{bp}\) and \(C_{bs}\), and dc bus capacitors \(C_h\) and \(C_l\), as shown in Fig. 1. Besides, \(i_p\) and \(i_s\) are the transformer currents at high and low side, respectively, \(v_p\) and \(v_s\) are the transformer voltages at high and low side, respectively, \(v_{AB}\) and \(v_{CD}\) are the voltages generated by the high and low side full bridge, respectively. It should be noted that the dc blocking capacitors are used to prevent the magnetic saturation of the transformer. Actually, the saturation issue of the transformer is rarely studied in the literature, where the solutions include peak current control [9], ‘magnetic ear’ [10, 11], etc. But the peak current signal can be easily distorted by noise especially when the switching frequency is high, while the magnetic ear is composed of an auxiliary core and an extra circuit. Compared with them, using DC blocking capacitors is an easier and more feasible method.

As mentioned in Section I the PSM is used in the DAB. The gate signals, voltage and current waveforms are shown in Fig. 2, where \(\phi\) is the phase shift angle between the high and low side square waveforms \(v_{AB}\) and \(v_{CD}\), and \(T_s\) is the switching cycle of the converter. The two parameters \(I_1\) and \(I_2\) are critical for identifying whether soft switching can be achieved. By solving the trigonometry shown in Fig. 2, they can be obtained as (1) and (2).

\[
I_2 = \frac{\phi}{2\pi L_s} \frac{T_s}{V_h + nV_l} = -I_1 \tag{1}
\]

\[
I_2 = I_1 + \frac{(\pi - \phi)T_s}{2\pi L_s} \frac{V_h - nV_l}{V_l} \tag{2}
\]
are shown in Fig. 3(a) where \( f \) is the parasitic capacitor of the power switch. Fig. 2. Gate signals, voltages generated by the full bridges, the voltage and current of the transformer in the DAB using PSM when (a) \( I_1 \geq 0, I_2 \geq 0 \) (b) \( I_1 \geq 0, I_2 < 0 \) (c) \( I_1 < 0, I_2 \geq 0 \).

Then \( I_1 \) and \( I_2 \) are derived as (3) and (4).

\[
I_1 = \frac{\pi n V_i - (\pi - 2\phi)V_h}{4\pi f_s L_s} \quad (3)
\]

\[
I_2 = \frac{\pi V_h - (\pi - 2\phi) n V_i}{4\pi f_s L_s} \quad (4)
\]

where \( f_s \) is the switching frequency of the DAB.

The equivalent circuits of the converter during the zero voltage turn on transient of the high and low side full bridges are shown in Fig. 3(a) (\( t = t_2 \)) and Fig. 3(b) (\( t = t_1 \)), respectively, where \( t_1 \) and \( t_2 \) are shown in Fig. 2, and \( C_{\text{oss},Qx} \) is the parasitic capacitor of the power switch \( Q_x \). In Fig. 3(a) when \( t = t_2 \), \( v_{\text{oss},Q2} = v_{\text{oss},Q3} = V_h \), thus the dynamic equations of the parasitic capacitors and the series inductor can be obtained as (5) and (6).

\[
L_s \frac{di_p(t)}{dt} = v_{\text{oss},Q2}(t) - n V_i \quad (5)
\]

\[
C_{\text{oss},Q2} \frac{dv_{\text{oss},Q2}(t)}{dt} = -\frac{1}{2} i_p(t) \quad (6)
\]

The parasitic capacitor voltage in time domain is then derived as (7), where \( \omega \) is defined as (8).

\[
v_{\text{oss},Q2}(t) = (V_h - n V_i)\cos(\omega t) - I_2 \omega L_s \sin(\omega t) + n V_i \quad (7)
\]

\[
\omega = \frac{1}{\sqrt{2L_s C_{\text{oss},Q2}}} \quad (8)
\]

Because Zero Voltage Switching (ZVS) of \( Q_2 \) and \( Q_3 \) can only happen if their parasitic voltages can get to zero by resonance. The boundary condition of the ZVS in high side full bridge is then obtained as (9) according to (7), and further derived to (10).

\[
\sqrt{(V_h - n V_i)^2 + I_2^2 \omega^2 L_s^2} \geq n V_i \quad (9)
\]

\[
I_2 \geq \frac{2C_{\text{oss},Q2}(2n V_h V_i - V_h^2)}{L_s} \quad (10)
\]

\[
\frac{n I_1 \cdot T_{\text{dead}}}{2 \cdot C_{\text{oss},Q6}} \geq V_i \quad (11)
\]

\[
I_1 \geq \frac{2C_{\text{oss},Q6} V_i}{n T_{\text{dead}}} \quad (12)
\]
the series inductor current $I_1$ times by the transformer turn ratio $n$. When $t = t_1$, the parasitic capacitor voltage of $Q_6$ is $V_i$, as shown in Fig. 2. Thus, in order to realize ZVS in $Q_5$, the parasitic capacitor voltage of $Q_6$ must be discharged to zero or $C_{oss,Q6}$ must be charged from zero to $V_i$. Because after $t = t_1$, $I_1$ will have a relatively small $di/dt$, as shown in Fig. 2, $nI_1$ is then considered to be constant during the short switching transient. Therefore, with the same principle, the boundary condition to achieve ZVS in low side full bridge is obtained in (11) and further derived to (12).

\[ Q = \frac{\phi I_1^2 n V_i}{2 \pi (I_1 + I_2)}, \quad \text{if } I_1 \geq 0 \land I_2 \geq 0 \]
\[ Q = \frac{\phi I_1^2 n V_i}{2 \pi (I_1 - I_2)}, \quad \text{if } I_1 \geq 0 \land I_2 < 0 \]
\[ Q = \frac{\phi I_1^2 n V_i}{2 \pi (I_1 + I_2)}, \quad \text{if } I_1 < 0 \land I_2 \geq 0 \]

The active power delivered by the DAB using PSM is well known, and it is shown in (17).

\[ P = \frac{n V_i V_i}{2 \pi l L_s} \phi (\pi - \phi) \]

Then, a map to show the soft switching and hard switching of the DAB as well as the circulating power ratio $(Q/P)$ in different load and low side voltage conditions with PSM is obtained and it is shown in Fig. 5(a). As seen, the soft switching range is wide when the low side dc voltage is close to 1 pu (1 pu = $V_i/n$), and the circulating power is relatively low as well. The soft switching range shrinks and the relative circulating power increases when the low side dc voltage decreases. The performance degrades even worsely when low side dc voltage increases. The soft switching area

![Fig. 3. Equivalent circuits of the converter during the zero voltage turn on transient of (a) the high side full bridge, $t = t_2$ (b) the low side full bridge $t = t_2$.](image)

![Fig. 4. The impact of $I_2$ on the parasitic capacitor voltage resonance of $Q_2$.](image)
almost disappears and the relative circulating ratio is larger than 1/10 in more than 80% of the load range when low side dc voltage increases to 2 pu. With this awful performance, a 2 pu low side dc voltage operation condition is not recommended.

In order to improve the performance of the DAB when low side voltage is close to 2 pu, a voltage doubler circuit is proposed. Instead of adding components into the DAB converter, the idea is to rearrange the gate signal sequence of the low side full bridge to generate a bias voltage on the low side dc blocking capacitor \( C_{bs} \). Then this voltage together with the voltage of low side transformer winding can generate a higher voltage level. The modulation strategy of the voltage doubler circuit is shown in Fig. 6, where the only difference compared with PSM shown in Fig. 2 is that \( Q_T \) is kept off and \( Q_b \) is kept on instead of having PWM signals. Thus, the low side full bridge will generate a square wave form \( v_{CD} \) with 50% duty ratio and two voltage levels \( V_l \) and \( V_0 \) instead of \( \pm V_l \). The dc component in this square wave form becomes \( V_l/2 \), and it will drop on the dc blocking capacitor \( C_{bs} \), as shown in Fig. 6 \( (v_{CD}) \). The low side voltage of the transformer then turns into \( \pm V_l/2 \) from \( \pm V_l \). Since the voltage doubler circuit is recommended for 2 pu low side dc voltage operation condition, the low side transformer voltage is thus close to \( \pm 1 \) pu.

Therefore, a similar soft switching area with Fig. 5(a), when \( V_l \) is close to 1 pu, is expected. The boundary conditions of soft switching area in the voltage doubler circuit are actually the same with PSM, which are (10) and (12), because the same equivalent circuits during ZVS as shown in Fig. 3 are still valid in the voltage doubler circuit. \( I_1 \) and \( I_2 \) can still be calculated as (3) and (4), but \( V_l \) should be changed to \( V_l/2 \) since the low side transformer voltage changes from \( \pm V_l \) to \( \pm V_l/2 \). The same change should also be applied to the calculations of the active power \( P \) and circulating power \( Q \) in (16) and (17). Then by using the proposed voltage doubler circuit the map in Fig. 5(a) becomes Fig. 5(b). As seen, just like expected, the soft switching area when \( V_l \) is 2 pu is very similar to the scenario when \( V_l \) is 1 pu, which is large and covers almost all the load range. The circulating power ratio is smaller than 1/10 in more than 80% of the load range. This much improved performance degrades slightly even \( V_l \) decreases or increases from 2 pu.

### III. Experimental results

Experimental results are obtained from a test platform shown in Fig. 7, where all the parameters are listed in Table I. Fig. 8 shows the square waveforms generated by the high and low side full bridges, and the low side transformer current of the DAB when \( V_l = 1.34 \) pu. As seen, the voltage square waveform \( v_{CD} \) generated by the low side full bridge jumps between \( \pm V_l \) and has no dc component when PSM is applied. While the voltage levels of \( v_{CD} \) become 0 and \( V_l \) when voltage doubler circuit is enabled, which introduces a \( V_l/2 \) dc component in \( v_{CD} \). These features matches with the analysis in Section II very well. Moreover, in the scenario shown in Fig. 8(a) @ 550 W, \( I_2 \) is below zero, and it cannot fulfill the soft switching condition of the high side full bridge in (10). Thus, the high side full bridge operates in hard switching condition, which not only leads to a low efficiency but also induces a high voltage spike in the high side full bridge that may destroy the power switches by overvoltage. The reason of the voltage spike is that in hard switching condition the parasitic capacitor voltage is larger then zero when the power switch in parallel turns on. The short circuit of the parasitic capacitor will then creates a very large \( \frac{dV}{dt} \) in the leg. Considering the stray inductance always exists in the leg, a voltage spike is thus generated. The amplitude of the voltage spike decreases when the load increases from 550 W to 850 W, then disappears when

![Fig. 7. A picture of the prototype and the test platform.](image)

### TABLE I. PARAMETERS USED FOR EXPERIMENTS.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal power</td>
<td>1000 W</td>
</tr>
<tr>
<td>High side voltage ( V_h )</td>
<td>200 V</td>
</tr>
<tr>
<td>Turn ratio of the transformer ( n : 1 )</td>
<td>3.5:1</td>
</tr>
<tr>
<td>Low side voltage ( V_l )</td>
<td>1 pu = ( \frac{V_h}{n} ) = 57 V</td>
</tr>
<tr>
<td>Series inductor ( L_s )</td>
<td>40 ( \mu )H</td>
</tr>
<tr>
<td>Switching frequency ( f_s )</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Deadtime ( T_{dead} )</td>
<td>200 ns</td>
</tr>
<tr>
<td>DC blocking capacitor ( C_{bp} )</td>
<td>10 ( \mu )F x 8</td>
</tr>
<tr>
<td>DC blocking capacitor ( C_{bs} )</td>
<td>10 ( \mu )F x 15</td>
</tr>
<tr>
<td>Output capacitors ( C_{oss, Q_1} \sim C_{oss, Q_4} )</td>
<td>158 ( \mu )F</td>
</tr>
<tr>
<td>Output capacitors ( C_{oss, Q_5} \sim C_{oss, Q_8} )</td>
<td>401 ( \mu )F x 2</td>
</tr>
</tbody>
</table>
the load is 950 W, because $I_2$ increases as load increases, and the parasitic capacitor is discharged more and thereby lower voltage is left for short circuit. This change in performance matches very well with the analysis in Fig. 4. Then voltage doubler circuit is enabled, and the waveforms change from Fig. 8(a) to Fig. 8(b). Because $I_2$ is much larger, so the voltage spikes in $v_{AB}$ disappear and efficiency increases a lot, e.g. from 84.5% to 94.2% when load is 550 W.

The efficiency of the DAB with different load and low side dc voltages is measured and it is shown in Fig. 9. As seen in Fig. 9(a), by using PSM, the efficiency is around 96% when $V_l = 1$ pu, then it drops dramatically as $V_l$ increases. The test of the DAB by using PSM at $V_l = 2$ pu is avoided for safety reasons, since the hard switching creates very high voltage spikes on power switches, which can break the power switches. While the efficiency can be evaluated according to the trend of the efficiency curves, and it should be lower than 90% or even lower. In Fig. 9(b), the voltage doubler is enabled when $V_l$ is beyond 1.25 pu. The improvement on efficiency is obvious. The efficiency starts to increase instead of dropping when $V_l$ increases beyond the threshold, and it increases to 96% when $V_l$ is around 2 pu.

**IV. CONCLUSIONS**

The DAB converter by using the conventional phase shift modulation can achieve soft switching and high efficiency when low side dc voltage is close to 1 pu, where 1 pu equals to the high side dc voltage divided by the transformer turn ratio. When low side dc voltage is close to 2 pu, the soft switching is very difficult to be achieved. The hard switching will not only reduce the efficiency of the converter but also induce high voltage spikes on the power switches. In order to achieve soft switching and high efficiency in DAB when low side dc voltage is close to 2 pu, a voltage doubler circuit is proposed. The circuit is composed of the dc blocking capacitor and the low side full bridge, thus no extra components are added to the DAB. It is realized by rearranging the PWM signals based on the phase shift modulation, which keeps the control complexity...
Fig. 8. The square waveforms generated by the high and low side full bridges, and the low side transformer current of the DAB using (a) PSM (b) voltage doubler circuit, when $V_t = 1.34$ pu.
low. By using the voltage doubler circuit, the DAB converter can again achieve soft switching as well as low circulating power and thereby high efficiency even the low side dc voltage becomes 2 pu.

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