

# CPSS Transactions on Power Electronics and Applications

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#### INAUGURAL SPECIAL ISSUE ON THE DEVELOPING TRENDS OF POWER ELECTRONICS: PART 1

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#### CPSS TRANSACTIONS ON POWER ELECTRONICS AND APPLICATIONS

CPSS Transactions on Power Electronics and Applications (CPSS TPEA) is sponsored and published by China Power Supply Society and technically co-sponsored by IEEE Power Electronics Society. It publishes original and high quality peer reviewed papers in the field of power electronics and its applications. With the goal of promoting the technology of power electronics including concepts, theory, modeling and control, analysis and simulation, emerging technology and applications, CPSS TPEA is expected to be a favorable platform to strengthen information exchange in this area. Interested authors are welcome to submit your papers via the Manuscript Central (https://mc03.manuscriptcentral.com/tpea-cpss) online submission system. You can find more information on our website: http://tpea.cpss.org.cn.

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# Editorial for the Inaugural Special Issue on the Developing Trends of Power Electronics: Part 1

WITH this editorial, we sincerely welcome our readers to the brand-new publication — CPSS Transactions on Power Electronics and Applications (CPSS TPEA). It is sponsored and published by China Power Supply Society (CPSS) and technically co-sponsored by IEEE Power Electronics Society (IEEE PELS).

CPSS was founded in 1983 and has been the only toplevel national academic society in China that solely focuses on the power supply/power electronics area. In the past 30plus years CPSS has dedicated to provide to its members. researchers, and industry engineers nationwide with high quality services including conferences, technical training, and various publications, and this in deed has helped the society build up its membership rapidly, which now totals up to more than 4000 individual members plus 500 enterprise members. The fast growth of membership in turn compels CPSS to always work out better services for its members. one of which being the open-up of this periodical - a new journal in English language as a publication platform for international academic exchanging. This of course needs to be done through international cooperation, and that's why IEEE PELS is tightly involved, being the premier international academic organization in power electronics area and one of the fastest growing technical societies of the Institute of Electrical and Electronics Engineers (IEEE).

To fulfill the publishing need of the fast-developing power electronics technology worldwide is a more important purpose of launching this new journal. So far there are only 3 or 4 existing journals which are concentrated on power electronics field and have global reputation. For quite a few years people in the international power electronics community have had the feeling that, the existing journals have not even come close to meeting the huge demand of global academic and technology exchanges. E.g., the two existing IEEE power electronics journals, i.e. IEEE Transactions on Power Electronics (IEEE TPEL) and IEEE Journal of Emerging and Selected Topics in Power Electronics (IEEE JESTPE), now publish about 1000 papers a year, which is under a very low paper acceptance rate of around 25%, but still have a back-log of about one year for the newly accepted papers to finally appear in printed form to the public. The addition of this new dedicated journal would be an ideal improvement to fulfill such a tremendous need.

The booming of publishing need really is an indicator of how fast power electronics has been developing in recent years. Innovations have been continuously coming up from component (both active device and passive device), module, circuit, converter, to system level, covering different technical aspects as topology or structure conceiving,

modeling and analysis, control and design, and measurement and testing. New issues and corresponding solutions have been continuously presenting as the applications of power electronics prevail horizontally in almost every area and corner of human society, from industry, residence and commerce, to transportations, and penetrate vertically through every stage of electric energy flow from generation, transmission and distribution, to utilization, in either a public power grid or a stand-alone power system. I personally believe that we are entering a world with "more electronic" power systems. The prediction around 30 years ago, that power electronics one day will become one of the major poles supporting the human society, is coming into reality. And I also believe, that power electronics is going to last for long time as an important topic since it is one of the keys to answer a basic question for human society, which is how human can harness energy more effectively and in a manner friendlier to both the user and the environment.

Therefore, I assume that there is probably no better fitting as for CPSS TPEA to publish its first few issues under a special topic about the developing trends of power electronics. We have invited a group of leading experts in different areas of power electronics to write survey/review papers or special papers with review/overview nature to some extent. To publish in a timely and regular style, we organize this inaugural Special Issue into different parts. Part 1 is in this issue and the other parts will appear in the following issues.

In Part 1 we are honored to have 8 invited papers. The first 4 address the state-of-the-arts application techniques of new power semiconductor devices and modules based on GaN or SiC and how these devices can be adequately used to improve the performance of converters and systems, while the rest 4 discuss the developing trends of different aspects of some currently hot or future promising application areas.

We begin with a review paper on the application of GaN devices for 1 kW server power supply with integrated magnetics. It is written by Dr. Fred C. Lee and his research group from Virginia Polytechnic Institute and State University. It presents how GaN devices coupled with softswitching techniques drastically reduce power losses and enable a switching frequency more than ten times higher than silicon devices, with much reduced EMI noises.

The second paper overviews the silicon carbide (SiC) based power conversion technology from device level up to system and application level. It is written by Dr. Fred (Fei) Wang and his research group from the University of Tennessee. The focus of this paper is on the benefits of SiC based power electronics for converters and systems, as well as their ability in enabling new applications.

The third paper is about a specific application of SiC-MOSFET dual modules to bidirectional isolated dual-active-bridge (DAB) DC-DC Converters. It is written by Dr. Hirofumi Akagi and his research group from Tokyo Institute of Technology. It illustrates how SiC-MOSFET is adopted to improve the efficiency and modular expandability of bidirectional isolated DAB DC-DC converter.

The fourth paper is regarding how to suppress turn-on oscillations for hybrid power modules combining Si IGBTs and SiC diodes. It is written by Dr. Dehong Xu and his research group from Zhejiang University in cooperation with Fuji Electric Co., Ltd. The paper reviews the causing, effect, and recently published damping methods of high frequency oscillation occurring during turning-on transients of Si IGBT and then proposes a novel suppression method.

The fifth paper is written by Dr. Deepak Divan and his research group from Georgia Institute of Technology, discussing the applications of power electronics to the future grid. It looks at the role that distributed power electronics could play where increasing levels of variable and non-dispatchable renewable energy resources are mixed into the grid and bidirectional power flows are adding complexity to grid operations.

The sixth paper is written by Dr. Jan A. Ferreira and his research group from Delft University of Technology, discussing wind turbine generator systems - another important application area of power electronics. It provides a comprehensive review and future trends prediction on how the availability of wind turbine generator system could be increased through appropriate design and control for reliability and fault tolerance.

The seventh paper is written by Dr. S.Y. Ron Hui from the University of Hong Kong and Imperial College London, about a recently emerging application area of power electronics — non-radiative wireless power transfer (WPT). The paper briefly reviews the history of some key concepts and techniques and particularly highlights a few misconceptions of WPT, and supplies the author's view on the present and future trends.

Last but not least, the eighth paper is written by Dr. Frede

Blaabjerg and his research group from Aalborg University, about a very hot application area of power electronics for the past years — grid-connected photovoltaic systems. The paper focuses on design for reliability (DfR) and it summaries in detail the technological challenges in DfR of power electronics with a systematic exemplification.

I'd like to thank the authors of all these 8 invited papers. It's their high-quality contributions that finally leads to the launching of this new journal. I'd like to thank Dehong Xu, President of CPSS, who in 2015 initiated the idea of publishing the new journal and since then has been persistently supporting my work as the founding Editor-in-Chief. I'd also like to thank Jiaxin Han, Secretary General of CPSS, Jan A. Ferreira, President of IEEE PELS, 2015-2016, Don F.D. Tan, President of IEEE PELS, 2013-2014, and Frede Blaabjerg, IEEE PELS Vice President for Products, 2015-2016, who form the CPSS and IEEE PELS Joint Advisory Committee for our new journal with Dehong Xu and myself. Other IEEE officers and leading staffs like Dushan Borojevich, PELS President, 2011-2012, Alan Mantooth, PELS President, 2017-2018, Mike Kelly, PELS Executive Director, and Frank Zhao, Director of China Operations, IEEE Beijing Office, just to name a few, also provided continuous support and constructive advices. My earnest thanks also go to the CPSS Editorial Office led by Lei Zhang, Deputy Secretary General of CPSS, for their wonderful editing work. It would not have been possible to create a new journal in such a short time without their efforts. I'd like to finally thank all the members of the Executive Council of CPSS and particularly the leaders of Chinese power electronics industry. They always firmly stand behind CPSS TPEA and ready to help whenever needed.

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**Jinjun L1U** received his B.S. and Ph.D. degrees in Electrical Engineering from Xi'an Jiaotong University (XJTU), China in 1992 and 1997 respectively. He currently holds the position of XJTU Distinguished Professor of Power Electronics, sponsored by Chang Jiang Scholars Program of Chinese Ministry of Education.

Dr. LIU coauthored 3 books (including a textbook), published over 200 technical papers in peer-reviewed journals and conference proceedings, and holds more than 30 invention patents (China/USA). He received for 7 times governmental awards at national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements. He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE Transactions on Power Electronics 2016 Prize Paper Award. His research interests are power quality control and utility applications of power electronics, micro-grids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu has served as the IEEE Power Electronics Society (PELS) Region 10 Liaison and then China Liaison for 9 years, an Associate Editor for the IEEE Transactions on Power Electronics for 9 years, and starting from 2015 the Vice President for membership of IEEE PELS. He is on Board of China Electrotechnical Society (CES) and was elected to a Vice President of the CES Power Electronics Society in 2013. He is the Vice President for International Affairs, China Power Supply Society (CPSS) and the inaugural Editor-in-Chief of CPSS Transactions on Power Electronics and Applications.

# Application of GaN Devices for 1 kW Server Power Supply with Integrated Magnetics

Fred C. Lee, Qiang Li, Zhengyang Liu, Yuchen Yang, Chao Fei, and Mingkai Mu

Abstract—In today's power electronics products, quality and reliability are given. Great emphases are placed on high efficiency, high power density and low cost. With recent advances made in gallium nitride power devices (GaNs), it is expected that GaNs will make significant impacts to all three areas mentioned above. Thanks to the absence of reverse recovery charge and smaller junction capacitances, the turnon loss of GaN is significantly reduced and Turn-off loss and driving loss are negligible, for the first time. These desired properties coupled with ZVS techniques will drastically reduce all switching related losses, thus enabling GaN to operate at a switching frequency more than ten times higher than its silicon counterparts. To illustrate the impact of GaN on efficiency, density and even design practice, a 1 kW server power supply is demonstrated which employs an interleaved CRM totem-pole PFC followed with an LLC resonant converter. Both operate beyond 1 MHz. All magnetic components are integrated into PCB with much reduced EMI noises, thus, only a simple onestage EMI filter is required. The system achieves a power density more than 150 W/in<sup>3</sup>, an efficiency above 96%, and much improved manufacturability with minimum labor content.

Index Terms—GaN device, soft switching, MHz, totem-pole PFC, LLC converter, coupled inductor, balance technique, matrix transformer, shielding.

#### I. Introduction

In today's power electronics products, quality and reliability are given, Great emphases are placed on high efficiency, high power density and low cost. Further advances alone these areas will be closely linked to advancement we can make in the area of power devices and materials and fabrication techniques. With recent advances made in wide-band-gap (WBG) power devices, the new generation of switches will make significant impacts to all three areas mentioned above.

It is evident that, for any given design, if simply replacing silicon devices with WBG, an improvement in efficiency can be made. Although it is an important contribution, to leave it at that, it does not do the justice to WBG. It is also clear that WBG devices can operate at much higher frequencies compared to their silicon counterparts. Consequently, as much as a factor of 5-10 reduction in size/weight using WBG are achievable and have been demonstrated in some

applications. Still it leave it at that, it does not realize the full potential of WBG. If we can design a converter with 10X, 20X or even 50X in switching frequency, comparing to our current practice using silicon devices, what has been taken for granted in our design practice is being challenged.

The ever increasing demand for high-efficiency and highdensity switch-mode AC/DC power supplies include but not limited to computers, telecommunication, data centers, electrical vehicle battery chargers, PV inverters, numerous industrials, and aerospace applications. Collectively, these products consume more than 10% of the total electric power. One percent of efficiency improvement, in this sector, represents 20 TWH of energy saving. The amount of energy saving is equivalent to the total energy outputs of three average size nuclear power plants, each at 7 TWH annual production. Moreover, with the increasing of cloud computing and big data, it is expected that data center alone will consume 10% of the total electricity by 2020. A typical example of a 1 kW AC/DC server power supplies is illustrated in Fig. 1. With 40% of the components manually inserted, manufacturing of this power supply is labor intensive. The trend will not reverse unless there is a paradigm shift in the way we design and manufacture these power supplies.

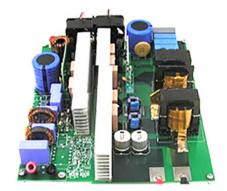


Fig. 1. A typical 1 kW AC/DC converter.

Within this industry sector, data center server power supplies are the most performance driven, energy and cost conscious. Within a data center, all major processor/memory devices are powered from a 12V bus. This 12V bus architecture was developed in the early 90's, when the power consumption was minuscule in comparison with today's usage. For example, each microprocessor is consuming 100A-200A current. The i<sup>2</sup>R loss for a 12V bus is excessive. To mitigate the heavy bus-bar loss in the power distribution

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path, industry leaders such as Google, Facebook, Cisco and IBM are already implementing new data center design with higher voltage distribution bus, such as 48V or 400V instead of 12V.

To support these power architecture changes, it is mandatory that the power supplies off the utility lines to be in a form of distributed power on the printed circuit board in the vicinity of the core processors and memory devices. The distributed power supplies have to be very efficient and with high power density to be compatible with core processors, memories, et al. Present power supplies are operating at 50-100 kHz with a power density less than 50 W/in<sup>3</sup>. An order of magnitude power density improvement is necessary for the wide spread use of the distributed power for all computer servers and data centers.

Advanced power semiconductor devices have consistently proven to be a major force in pushing the progressive development of power conversion technology. The emerging gallium-nitride-based power semiconductor device is considered a promising candidate to achieve high-frequency, high-efficiency, and high-power-density power conversion [1]-[17]. Due to the advantages of the material, the GaN HEMT has the features of a wide band gap, high electron mobility, and high electron velocity [1], [2]. Thus a better figure of merit can be projected for the GaN HEMT [3] than for the state-of-the-art Si MOSFETs, which allows the GaN HEMT to switch with faster transition and lower switching loss. By using the GaN HEMT in a circuit design, the switching frequency can be pushed up to MHz frequencies, and continue to have high efficiency [4]-[11].

To realize the benefits of GaN devices resulting from significantly higher operating frequency, a number of issues have to be addressed, such as converter topology, magnetics, control, packaging, and thermal management. In Section II, the switching characteristic of high voltage GaN devices is studied including comparison between hard switching and soft switching; a 1-3 MHz CRM totem-pole PFC with integrated coupled inductor is demonstrated in Section III; then an 1 MHz LLC resonant converter with integrated matrix transformer is presented in Section IV; finally, complete EMI performance is evaluated and the corresponding EMI filter design for this MHz server power supply is verified in Section V.

### II. SWITCHING CHARACTERISTICS OF GALLIUM NITRIDE TRANSISTORS

Gallium Nitride devices are gathering momentum, with a number of recent market introductions for a wide range of applications such as point-of-load converters (POL), off-line switching power supplies, battery chargers and motor drives. GaN devices have a much lower gate charge and lower output capacitance than silicon MOSFETs and, therefore, are capable of operating at a switching frequency 10 times greater. This can significantly impact the power density, form factor and even the current design and manufacturing practices.

#### A. Modeling of double-pulse tester

Understanding the switching characteristic of GaN switches is essential to use GaN devices in circuit design correctly and more efficiently.

In hard-switching converters, the overlap of voltage and current across drain and source of the device leads to significant power losses during switching event. To better illustrate the switching characteristic of high voltage GaN switches, a typical switching waveforms of the top switch in a buck converter, are shown in Fig. 2. During turn on transition, a large current overshoot is induced by the junction capacitor charge of the bottom switch. In addition, cascode GaN has additional charge due to the reverse recovery of the low voltage silicon MOSFET in the cascode configuration. The integral of voltage and current during turn on transition generates significant power dissipation, which is in the magnitude of tens of uJ. Even through, the turn on switching loss of GaN is still much lower compared with Si MOSFET which has the same breakdown voltage and same on resistance.

On the other hand, the cross time of the drain-source voltage and current during turn off transition is quite short and the energy dissipation is less than a few uJ. The major reason for such a small loss is due to high transconductance of GaN devices. In addition, the cascode GaN has smaller turn off loss at higher current condition due to intrinsic current source driving mechanism [18], [19]. The cascode structure minimizes the miller effect during turn off transition, and therefore, the loss is not sensitive to the turn off current.

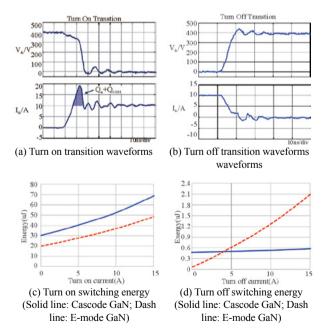


Fig. 2. Switching characteristic of high voltage GaN transistors.

#### B. Packaging Influence

Both e-mode GaN devices and cascode GaN devices

are able to switch very fast. However, parasitic inductance introduced by the bulky package became a limit which results in large switching loss and severe oscillations during switching transitions.

Regarding packaging influence study, many efforts are spent on the Si MOSFET with monolithic structure [20]-[22]. It is well studied the common-source inductance (CSI), which is defined as the inductance shared by power loop and driving loop, is most critical. The CSI acts as negative feedback to slow down the driver during the turn-on and turn-off transitions, and thus prolongs the voltage and current crossover time, and significantly increases the switching loss.

Similar theory can be applied to e-mode GaN devices. Fig. 3 shows package related parasitic inductance of a typical through-hole package (TO-220) and a typical surface-mount package (PQFN), while their inductance based on real devices are listed in TABLE I. Here the inductance value is extracted by FEA simulation in Ansoft Q3D. Through this comparison, it can be observed that surface mount package is effective to reduce the value of parasitic inductance while Kelvin connection (K) is able to decouple power loop with driving loop so that the source inductance is no longer the common source inductance.

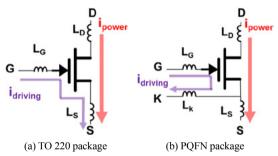


Fig. 3. Package related parasitic inductance distribution of e-mode GaN.

TABLE I
PACKAGE RELATED PARASITIC INDUCTANCE VALUE

	LG	LD	LS	LK
TO-220	3.6nH	2.3nH	3.9nH	N/A
PQFN	2.4nH	1.3nH	0.9nH	1.3nH

Unlikely to e-mode GaN devices, the cascode GaN device has much complex parasitic inductance distribution and the identification of the CSI is not straight-forward [23], [24]. In the first step, the CSI of the low-voltage Si MOSFET and of the high-voltage GaN HEMT are analyzed separately. From the perspective of the Si MOSFET,  $L_{\text{int3}}$  and  $L_{\text{S}}$  are the CSIs of the Si MOSFET; while from the perspective of the GaN HEMT,  $L_{\text{int3}}$  and  $L_{\text{int1}}$  are the CSIs of the GaN HEMT. Therefore, in terms of the cascode GaN device (Fig. 4), since  $L_{\text{int3}}$  is the CSI for both the GaN HEMT and the Si MOSFET, it is the most critical parasitic inductance.  $L_{\text{int1}}$  is the second critical inductance, since it is the CSI of the high-voltage GaN HEMT, which has the major switching loss. Finally,  $L_{\text{S}}$ 

is the third critical inductance.

According to the analysis, the traditional package has significant side effect on the device switching performance. Then stack-die package is proposed to solve the package related issues [25]-[27].

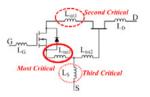


Fig. 4. Common source inductance distribution in cascode GaN device.

The stack-die package is able to eliminate all common source inductance. As shown in Fig. 5(b), in the stack-die package of cascode GaN device, the Si MOSFET (drain pad) is mounted on top of the GaN HEMT (source pad) directly. The interconnection between two dies are minimized in this way, thus the stack-die package is considered as the optimized package for cascode GaN device.

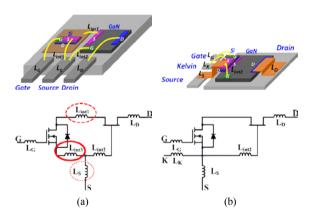


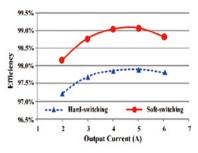
Fig. 5. Package bonding diagram and schematic for cascode GaN HEMT (a) TO-220, and (b) stack-die.

#### C. Comparison Between Hard-switching and Soft-switching

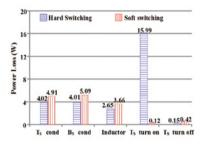
Even with a better package, the turn-on switching loss of high voltage GaN switch under hard-switching conditions is significant and dominant in high frequency applications, where the loss could be 10-20 W loss at 500 kHz operation, for example. ZVS turn-on is strongly desired to fully exploit the potential of the GaN switch. Critical conduction mode (CRM) operation is the most simple and effective way to achieve ZVS turn-on and is widely used in medium-low power applications.

Fig. 6 shows the efficiency comparison of soft-switching and hard-switching buck converter with GaN devices. The switching frequency at 6A full load output is designed to be 500 kHz. Fig. 6(b) shows the loss breakdown under full load condition. The chart clearly shows that the turn on loss is minimized with ZVS and only introduces a little more conduction loss. The increase of conduction loss is due to the increased ripple current and corresponding circulating

energy which is used to achieve ZVS.



(a) Efficiency comparison.



(b) Loss breakdown at full load

Fig. 6. Soft-switching vs. Hard-switching

# III. TOTEM-POLE PFC WITH INTEGRATED COUPLED INDUCTOR AND BALANCE TECHNIQUE

#### A. GaN-Based MHz Totem-Pole PFC

With the advent of 600V gallium-nitride (GaN) power semiconductor devices, the totem-pole bridgeless power factor correction (PFC) rectifier [28], [29], which was a nearly abandoned topology, is suddenly become a popular front end candidate for applications like 2-stage high-end adaptor, server and telecommunication power supply, and on-board battery charger. This is mostly attributed to the significant performance improvement of the GaN HEMT compared to Si MOSFET, particularly better figure-of-merit and significantly smaller body diode reverse recovery effect.

GaN-based hard-switching totem-pole PFC rectifier is demonstrated in literature [30]. As the reverse recovery charge of the GaN HEMT is much smaller than the Si MOSFET, hard-switching operation in totem-pole bridge configuration turned to be practical. By limiting switching frequency around or below 100 kHz, the efficiency could be above 98% for a 1 kW level single-phase PFC rectifier. Even the simple topology and high efficiency are attractive, the system level benefit is limited because the switching frequency is still similar to Si-based PFC rectifier.

Based on previous study, soft switching truly benefits the cascode GaN HEMT. As the cascode GaN HEMT has high turn-on loss and extremely small turn-off loss due to the current-source turn-off mechanism, critical mode (CRM) operation is very suitable. A GaN-based critical mode (CRM) boost PFC rectifier is first demonstrated which shows the high-frequency capability of the GaN HEMT and significant

system benefits as the volume of the boost inductor and the DM filter is dramatically reduced [31], [32].

With a similar system-level vision, the cascode GaN HEMT is applied in the totem-pole PFC rectifier while pushing frequency to above 1 MHz. Several important high-frequency issues, which used to be less significant at low-frequency, are emphasized and the corresponding solutions are proposed and experimentally verified. They are including ZVS extension in order to solve switching loss caused by non-ZVS valley switching; variable on-time control to improve the power factor, particularly the zero-crossing distortion caused by traditional constant on-time control; and interleaving control for input current ripple cancellation.

A 1.2 kW dual-phase interleaved MHz totem-pole PFC rectifier is built with 99% peak efficiency and 700W/in<sup>3</sup> power density (without bulk cap), as shown in Fig. 7 in which the inductor is significantly smaller compared to state-of-the-art industrial practice [33]-[37].

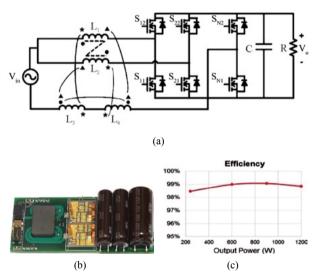


Fig. 7. GaN-based MHz totem-pole PFC (a) topology, (b) prototype, and (c) measured efficiency.

#### B. Integrated Coupled Inductor with Balance Technique

The concept of coupled inductor, developed at CPES [38], has been widely used in multi-phase VRM to reduce loss and improve transient performance. This concept has been extended to two-phase interleaved totem-pole PFC rectifier. One special feature of the coupled inductor in this application is that the effective inductance value will change with duty cycle, in a manner that when duty cycle is approaching 0.5, L value will increase. Subsequently, the switching frequency will decrease as shown in Fig. 8. The net benefit is a reduction of the switching losses by 35%.

One of the important concerns with using the GaN devices is the potential high EMI noises resulting from high di/dt and dv/dt during switching. While the concern may be a genuine one with the conventional design practice, the use of PCB integrated magnetics offers the opportunity for significant reduction of common mode (CM) noises. This is achieved

by incorporating CPES developed balancing technique [37] relatively easy in the PCB winding structure.

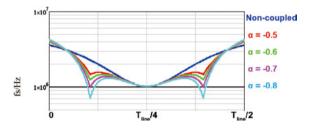


Fig. 8. Switching frequency variance during half line cycle.

In order to use the balance principle for CM noise reduction, two additional inductors L3 and L4 are employed and are coupled with L1 and L2 respectively. Fig. 9 shows the circuit topology and the integrated magnetic structure. By use the superposition theory to Fig. 10 (a), the equivalent circuit for the noise source Vs1, is shown in Fig. 10 (b). The number of turns of L1 and L2 is N1. The number of turns of L3 and L4 is N2. Thus, we have the balance condition for source V1 is  $N_1/N_2 = C_b/C_d$ .

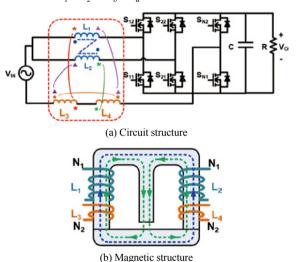


Fig. 9. Improved balance technique for interleaved totem-pole PFC converter with coupled inductor.

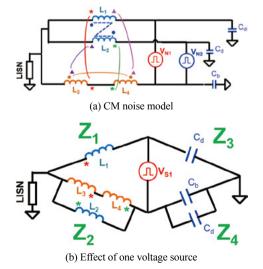


Fig. 10. Equivalent circuit of CM noise.

Similarly, the balance condition for noise source  $V_{N2}$  is also  $N_1/N_2 = C_b/C_d$ . The CM noise of this PFC converter can be minimized as long as this balance condition is achieved. Fig. 11 shows that with balance technique, CM noise can be effectively reduced.

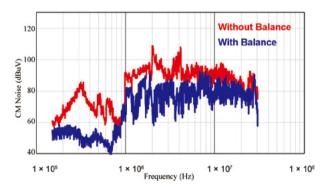


Fig. 11. CM noise reduction result with balance technique. v

Fig. 12 shows the proposed coupled inductor with coupling coefficient,  $\alpha = -0.7$ . The windings are partially interleaved to reduce winding losses and in the same time provide the desired negative coupling. The windings near the air gap are tapered to avoid fringing flux [37].

With the PCB winding, balance technique can be applied to reduce CM noise [37]. The balance winding can be easily implemented by replace the bottom layer of PCB winding with the one-turn balance inductor L3 and L4, as shown in Fig. 12. TABLE II shows the simulated loss breakdown of this coupled inductor with balance technique. The total loss is similar as the non-coupled inductor with litz wire.

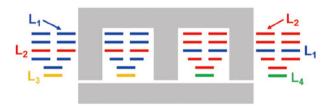


Fig. 12. Coupled inductor with balance

TABLE II

LOSS BREAKDOWN FOR INDUCTOR

	DC W. Loss/W	AC W. Loss/W	Core Loss/W	Total Loss/W
PCB winding coupled inductor	0.6	2.1	1.9	4.6
Litz wire non coupled inductor	0.7	1.6	2.3	4.6

For the sake of comparison, TABLE II also shows the loss breakdown for two non-coupled inductors using two ER23 core. The winding is 250/46 litz wire with 10 turns for each inductor. According to conventional wisdom, the PCB based inductor design is inferior to the conventional litz wire wrapped around a core. However with proposed design,

similar total loss is achieved by the proposed PCB based coupled inductor.

# IV. LLC Converter with Integrated Matrix Transformer

For the DC/DC stage, the LLC resonant converter is deemed the most desired topology because of its high efficiency and high power density. The LLC converter can achieve ZVS for the primary devices and ZCS for the secondary SRs. These features are not only beneficial for achieving higher efficiency but also for lower EMI noises.

For applications that require low-voltage, high-current outputs, such as computer servers, there are several important design considerations: 1) the state-of-the-art synchronous rectifiers (SRs) are best operated with 10-15A. For server applications, one should consider paralleling 4-8 SRs. Both static and dynamic current sharing, when paralleling a large number of SRs, are difficult to achieve. 2) The large sum of high frequency and high di/dt ac currents much flow through a common termination point between the transformer and the SRs. This can result in large termination losses. 3) Large leakage inductances at the transformer secondary-side windings result in large winding losses.

To overcome the challenges in low-voltage, high-current outputs application, the traditional single core structure was divided into a 4-core matrix transformer structure, as shown in Fig. 13, whose primary windings in series and the secondary windings in parallel. Since the primary current for the 4 transformers are the same, the secondary current are perfectly balanced. The termination point, where all currents are summed, occurs on the DC side, thus, no termination loss. Transformer winding losses are significantly reduced as well as the leakage inductances [39], [40].

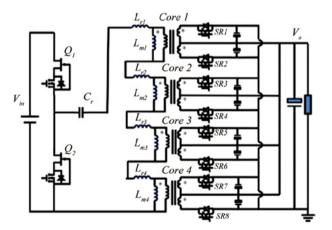


Fig. 13. LLC converter with matrix transformers incorporating 4 sets of outputs.

Furthermore, the four transformers can be integrated into two-core structure by means of flux cancellation, thus, resulting in reduced core volume and core loss [40]. The first generation of the prototype LLC converter, as shown in Fig. 15(a), achieved a peak efficiency of 95.5% and power

density over 700W/inch<sup>3</sup>. By increasing the switching frequency to be ten times higher than the state-of-the-art industry practice, the power density is much better than the state-of-the-art even the output is changed from 1 set of output to 4 sets of outputs.

In the loss analysis, it is found that the winding losses are dominating. Further division of the 4-transformer structure into an 8-transformer structure, as shown in Fig. 14, would yield a significant reduction in losses, both in transformer windings and SRs. The transition from 4 sets of outputs to 8 sets of outputs, although at the expense of increased core loss, is worth doing since the core loss is a small portion of the total loss with MHz switching frequency. Increasing the number of outputs to improve efficiency is only achievable with high switching frequency due to the much reduced core loss [41] and higher di/dt ac currents compared to the state-of-the-art industrial practice operating at around 100 kHz.

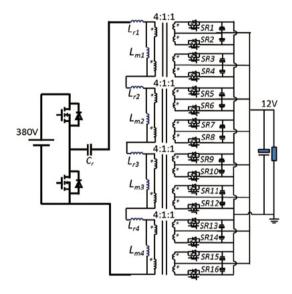


Fig. 14. LLC converter with matrix transformers incorporating 8 sets of outputs and flux cancellation.

Subsequently, the second-generation prototype was developed as shown in Fig. 15(b), leading to a much improved efficiency as shown in Fig. 16 [42]. It should be noted that the improvement of efficiency is not at the expense of power density. The power density remains essentially the same, at 700W/in<sup>3</sup>. The efficiency is higher than the state-of-the-art industry practice while the power density is ten times better. The windings were implemented using only 4-layer PCB. The system cost is considerably lower and the design can be fully automated.



Fig. 15. (a) Prototype of 1st generation.



Fig. 15. (b) Prototype of 2nd generation.

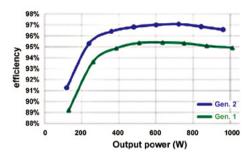


Fig. 16. Efficiency of the two generations.

For the matrix transformer, the PCB windings are fully interleaved, which leads to large distributed inter-winding capacitors and, hence, large CM noise current. In this design, the inter-winding capacitance is estimated at 800pF. The CPES patent shielding technique [43], [44] is incorporated in the design, by placing shielding layers in between primary and secondary windings. Fig. 17 illustrate the transformer structure with shielding. Each shielding layer is connected to the primary ground. Therefore the CM noise current can only circulate in the primary side.

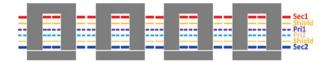


Fig. 17. Transformer structure with shielding.

The shielding layers are made identical to the secondary windings, both are single-turn windings. Therefore, there is zero potential difference between the shielding winding and the secondary winding, thus, no CM current. Fig. 18 demonstrated the effectiveness of this shielding concept. The noise spectrum in red is without shielding and the noise spectrum in blue is with shielding. A maximum 23 dBuV CM noise reduction is realized by this simple technique.

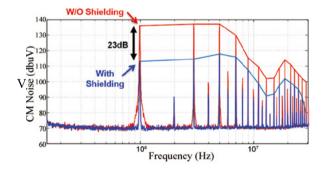


Fig. 18. CM noise test result.

When operating LLvvC converter at very high switching frequency, the control is very challenging due to the fast dynamics of the resonant tank. Recently, CPES has successfully developed a digital based state-trajectory control with a nearly one-cycle response. This proposed controller incorporates the state-trajectory control techniques [45], [46]. A multitudes of technology breakthroughs have

been reported in recent literature including: soft start-up and short-circuit protection to minimize stresses; auto-tuning to minimize SR losses; fast load transient response; burst mode for improved light load efficiency [47]-[52]. These techniques, over several generations of developments, have reached a point where they can finally be realized using a low-cost digital controller to control the high frequency LLC converters.

In summary, the transformer design methodology, CM noise reduction and digital control for high frequency LLC converters have been successfully demonstrated.

#### V. System Demonstration

Conventionally, in order to achieve enough noise attenuation, people have to use two stage EMI filter, which has high cost and large volume. Thanks to the high switching frequency and all the EMI reduction techniques, it is possible to use simple one stage filter to achieve required attenuation. Fig. 19 and Fig. 20 show the demonstration of single stage filter. Compared to traditional two stage filter, the single stage filter can achieve 80% volume reduction.

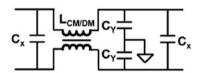


Fig. 19. Single stage EMI filter topology.



Fig. 20. Picture of single stage EMI filter.

Fig. 21 and Fig. 22 show the EMI noise measurement results. It can be seen that with one stage filter, the noise is below EMI EN55022B standard.

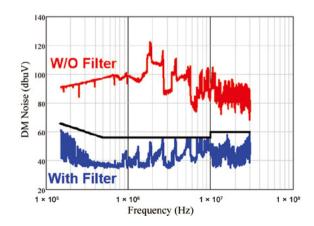


Fig. 21. DM noise measurement.

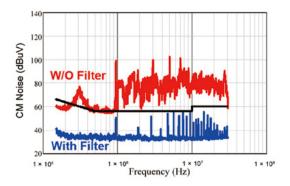


Fig. 22. CM noise measurement.

Finally, the total system is demonstrated as Fig. 23 and Fig. 24. The key features are including 1-3 MHz high frequency, soft switching for all GaN devices, integrated magnetics design, simple 1-stage EMI filter, and designed for manufacturability. Fig. 25 shows the efficiency curve of the system. It even outperforms the state-of-the-art products who is qualified of 80 Plus Titanium standard.

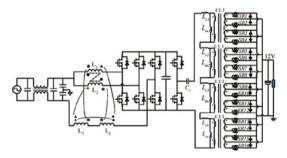


Fig. 23. Topology of total system.

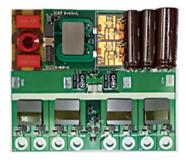


Fig. 24. Prototype of total system.

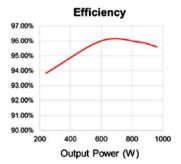


Fig. 25. Tested system efficiency.

#### VI. CONCLUSION

The switching characteristics of high voltage GaN devices are evaluated. It is shown that the switching related losses are significantly reduced when compared to silicon MOSFET. Specifically, the turn-off loss and driving loss are negligible. If the ZVS technique is employed to eliminate the turn-off loss, the GaN based converters are capable of operating at a switching frequency more than ten times higher than its silicon counterparts. However, a number of important issues have to be address in order to better utilize GaN devices in high-frequency circuit design. Advanced packaging and circuit layout with minimized parasitics are essential to realize the promising performance of GaN.

At the system level, a design of 1 kW server power supply operating at a switching frequency beyond 1 MHz is used to demonstrate the impact of GaN in such important issues as efficiency, power density and manufacturability. As the switching frequency is extended beyond 1 MHz, windings for both PFC inductors and LLC transformers can be integrated into PCB with significantly improvement in efficiency, density, and EMI.

The impact of GaN devices on power electronics goes beyond efficiency and power density improvement. Even though GaN is still in an early stage of development, it is presumably a game-changing device with a scale of impact yet to be defined. Certain design trade off previously inconceivable can be realized with not only significant performance enhancement but also drastic reduction of the labor contents in the manufacturing.

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# Overview of Silicon Carbide Technology: Device, Converter, System, and Application

Fei (Fred) Wang and Zheyu Zhang

Abstract—This paper overviews the silicon carbide (SiC) technology. The focus is on the benefits of SiC based power electronics for converters and systems, as well as their ability in enabling new applications. The challenges and research trends on the design and application of SiC power electronics are also discussed

Index Terms—SiC power semiconductors, SiC based converters

#### I. Introduction

A T the heart of modern power electronics converters are power semiconductors switching devices. Today's power semiconductor devices are dominated by the mature and well established silicon (Si) technology. Since the advent of Si thyristors in 1957, many Si based switching devices have been developed to meet different application and performance needs. The most popular Si switching devices are insulated-gate bipolar transistors (IGBT) and power metal-oxide-field-effect transistors (MOSFET), with IGBT for high voltage, high power, and low frequency applications, and MOSFET for low voltage, low power and high frequency applications. Thyristors and their derivatives such as integrated-gate-commutated thyristors (IGCT) are still used in special high power applications.

Si power semiconductor devices have gone through many generations of development in the last 50 years and are approaching material theoretical limitations in terms of blocking voltage, operation temperature, and conduction and switching characteristics. Due to limited performance, the highest voltage rating of the state-of-art commercial Si IGBT has been 6.5 kV for the last 15 years. There are no commercial Si based devices with junction temperature capability above 175 °C. These intrinsic physical limits become a barrier to achieving higher performance power conversion.

The emergence of wide bandgap (WBG) semiconductor devices promises to revolutionize next-generation power

electronics converters. Compared with Si devices, WBG devices feature high breakdown electric field, low specific on-resistance, fast switching speed and high junction temperature capability. All of these characteristics are beneficial for the efficiency, power density, specific power, and/or reliability of power electronics converters. The WBG devices under rapid development and commercialization include silicon carbide (SiC) and gallium nitride (GaN) devices, with SiC mainly targeting high voltage high power (600 V, kilowatts or above) applications, and GaN for low voltage low power (600 V, kilowatts or below) applications [1]. This paper focuses on SiC technology.

SiC devices can improve and impact power electronics in several ways [2]: 1) At converter level, through substituting Si devices directly or simplifying circuit topologies, SiC devices can improve converter efficiency, reduce cooling needs, and reduce active and passive component numbers and size, with their high voltage, low loss and fast switching capabilities; 2) At system level, SiC based converters can have better dynamic performance and more system functionalities as a result of their high frequency capability and high control bandwidth enabled by fast switching speed, and 3) SiC can enable new applications, such as high-efficiency high-density solid-state transformers (SST) and high speed motor drives. A number of commercial and research prototype converters using SiC devices have been developed with promising results on significantly improved efficiency and power density [3]-[49].

The extremely fast switching and other superior characteristics of SiC devices have nonetheless also posed severe challenges to their applications. Pervasive dv/dt and di/dt slew rates of up to 100 V/ns and 10 A/ns, augmented electromagnetic interference (EMI) emissions, single-device blocking voltages as high as tens of kV with corresponding insulation requirements, switching frequencies in the 100s of kHz range, and junction temperatures surpassing 200 °C, have called for a comprehensive reformulation of design procedures developed for Si-based power electronics. Addressing these design and application issues are critical to the adoption and success of SiC power electronics.

This paper overviews the SiC technology and recent advances on devices, converters, systems, and applications. The focus is on the benefits of SiC based power electronics for converters and systems, as well as their ability in enabling new applications. The challenges and research trends on the design and application of SiC power electronics are also discussed.

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#### II. SiC Power Semiconductor Devices and Modules

The discussion in this section focuses on the characteristics of SiC devices versus their Si counterparts, status of SiC power semiconductors as well as SiC version of the intelligent power modules.

#### A. Introduction of SiC in Comparison to Si

WBG refers to electronic energy band gaps significantly larger than one electron-volt (eV). SiC materials have several characteristics that make them attractive compared to narrow bandgap Si for power electronics converters. Fig. 1 highlights some key material properties of SiC semiconductor candidates as compared to traditional Si [50]. Generally speaking, for SiC material, the energy gap, breakdown electric field, thermal conductivity, melting point, and electron velocity are all significantly higher. These characteristics allow SiC semiconductor based power devices to operate at much higher voltage, switching frequency and temperature than Si [1], [51], [52].

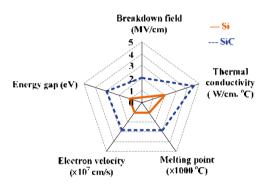


Fig. 1. Summary of Si and SiC relevant material properties [50].

For example, with the breakdown field higher than that of Si, a thinner drift layer with a higher doping concentration can be used for SiC power devices at the same blocking voltage. For unipolar device such as Schottky diodes and MOSFETs, the combination of thinner blocking layer and higher doping concentration yields a lower specific onresistance compared with Si majority carrier devices.

The fast switching-speed capability of SiC devices can be expected due to higher breakdown field and electron velocity. First, with lower on-resistance at the same breakdown voltage, a reduced chip size is achieved in SiC unipolar devices such as MOSFET. Considering the tradeoff between thinner drift region and smaller chip size, the junction capacitance of SiC MOSFETs is still lower than that of the Si counterparts, therefore the switching speed becomes faster. Second, minority carriers are swept out of the depletion region at the saturated drift velocity during the turn-off transient. The electron saturated drift velocity of SiC is higher than that of Si, leading to an increased switching speed of SiC devices.

Additionally, the excellent thermal conductivity allows SiC dissipated heat to be readily extracted from the device.

Hence, a larger power can be handled by the device at a given junction temperature. Also, higher thermal conductivity together with wide bandgap makes it possible for SiC devices to work at high temperature.

In summary, SiC based power devices offer low specific on-state resistance, fast switching speed, and high operating temperature and voltage capabilities.

#### B. Status of SiC Devices

This subsection summarizes available information on SiC power devices, including device types, voltage/current ratings, status of commercialization, as well as the latest trend of SiC device development. Note that the hybrid power modules consisting of Si active switches and SiC Schottky barrier diodes (SBDs), which have been commercially available, are not focused in the following discussion.

The availability of high quality SiC wafers allows a reasonable yield of large-area SiC power devices. Currently, 150 mm or 6 inch SiC wafers are commercially available [53]. Fig. 2 summarizes the status of SiC based power devices, including Schottky diodes, PIN diodes, MOSFETs, junction gate FETs (JFETs), IGBTs, bipolar junction transistors (BJTs), and thyristors with the voltage range from 400 V to 22.6 kV. It is observed that the low voltage (from 400 V to 1700V) SiC devices are becoming commercially available. Among them, the current rating per die approaches up to 100 A, and with multiple dies in parallel, state-ofart SiC power modules on market can deliver hundreds of amperes current. On the other hand, the high voltage SiC (referred here as 3.3 kV and above) are generally in developmental stages with limited commercial availability and small current rating per die [54].

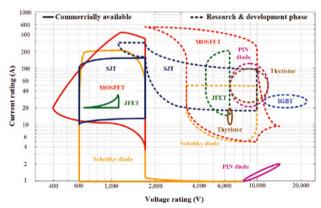


Fig. 2. Summary of status of SiC power devices [55]-[65].

Currently SiC MOFETs are the most developed active switches, with some JFETs, IGBTs, BJTs, and thyristors also available. For SiC diodes, at low breakdown voltage (< 1700 V), SBDs are popular since they show extremely high switching speed and low on-state loss. But high leakage current and low blocking voltage limit their utilization in high voltage applications. PIN diodes and Junction Barrier Schottky (JBS) diodes are preferred in high voltage applications. Compared with PIN diodes, JBS diodes have

excellent reverse recovery characteristic but poor static performance, making them suitable as anti-parallel diodes of active switches.

SiC power devices are developing rapidly. Compared with the data summarized in [2] a year ago, a few updates are highlighted as follows

### 1) Increased Current Ratings and More Available Voltage Ratings

Current ratings have been significantly improved at both die level and power module level under wide voltage ratings. For example,  $650 \text{ V}/17 \text{ m}\Omega$  discrete SiC MOSFET has been released with the current rating of 118 A at room temperature [55], which is comparable with the current rating of the state-of-the-art 650-V C7 Si CoolMOS on the market. Also, at medium voltage (MV) level, several large current power modules have been developed and demonstrated, including but not limited to 1.7 kV/550A, 3.3 kV/180 A, 10 kV/240 A SiC MOSFETs based phase-leg power modules, and 6.5 kV/200 A SiC JFETs based phase-leg power modules [66], [67].

More voltage ratings are available mainly due to the application orientated consideration. One example is that a 1000 V SiC MOSFET has been released recently targeting the electric vehicle application. Compared with 900 V and 1200 V voltage ratings, which are typical values for traditional Si devices, a dedicated 1000 V SiC MOSFET is developed to achieve better tradeoff between performance (e.g. switching and conduction loss) and reliability (e.g. adequate voltage margin) [61]. As expected, with the acceleration of acceptance and adoption of SiC devices in industrial products, SiC manufacturers may be willing to develop more dedicated power semiconductors to best serve specific markets.

#### 2) Improved Packaging Techniques

Advanced packaging techniques have been adopted for SiC devices for parasitic minimization, weight/size reduction, and high temperature operation.

For example, TO-247-4 pin package with separated Kelvin source has been utilized for discrete SiC MOSFETs at 1000 V and 1200 V levels [56], [61]. Thanks to the Kelvin source connection and its resultant lower common source inductance, the switching performance can be greatly improved with fast switching and low loss. Also, power modules with < 5nH parasitic inductance are developed for 1200-1700 V power modules with more than 400 A current capability [61], [65]. Additionally, ultra-light SiC power modules based on Easy1B PressFIT package are available for high density power conversion system [56]. Furthermore, high temperature packaging techniques are employed so as to allow commercially available SiC devices (e.g. Schottky diodes and supper junction transistors) to operate up to 210 °C [57].

#### 3) Availability of More Power Module Configuration

In addition to the phase-leg power module, more options with respect to the configuration of power modules are

available, such as boost chopper, buck chopper, full bridge, three-level neutral point clamped (NPC), three-level T-type, triple phase-leg [59]. With this, users are able to more conveniently develop high performance power electronics circuits based on different topologies for various applications.

#### 4) Enhanced Short-circuit Withstand Capability

Short circuit withstand capability is challenging for tiny and fast SiC devices [68]-[71]. Compared with traditional Si devices with > 10  $\mu$ s short circuit withstand time, the typical short circuit withstand time of SiC MOSFETs is on the order of 1  $\mu$ s. Recently, an enhanced short circuit capability SiC MOSFETs has been developed at MV level (> 3.3 kV). It is demonstrated that these new devices are capable of sustaining short circuit current up to 13  $\mu$ s, which significantly benefits the reliable operation of SiC MOSFETs for voltage source based high power conversion system [66].

## 5) Better SiC MOSFET's Body Diode Performance and Trend of Eliminating SBDs in Power Modules

The body diode of the SiC MOSFET is structurally similar to the p-n junction diode formed in the body of a Si MOSFET. The lifetime of minority carriers in SiC is shorter than Si, so the reverse recovery charge is reduced.

To mitigate the reverse recovery induced by MOSFET's body diode, a dedicated SiC SBD is generally added. However, considering the charging of SBD junction capacitance, employing an SBD in parallel does not necessarily result in low total switching energy loss. Specifically, at room temperature, the charging of SBD junction capacitance is greater than reverse recovery charge introduced by MOSFET's body diode [72]. Under elevated temperature, reverse recovery charge was observed to increase significantly; as a result, the switching energy loss may be higher as compared to that with SBD case. Recently, it is demonstrated that for the latest generation Wolfspeed SiC MOSFETs, at 150 °C, the total switching energy loss without SBD does not exceed the loss with employing SBD [72]. Therefore, under wide operating range, the excellent switching performance can be achieved by SiC MOSFET without the extra SBD. Regarding the conduction loss, the channel of SiC MOSFETs, instead of its body diode, can efficiently conduct reverse current. In the end, the penalty without antiparallel SBD with respect to efficiency is limited.

Furthermore, reduced size and cost due to the lack of SBDs in power module can improve the power density and cost of overall power conversion system. Accordingly, it is observed that there is a trend of eliminating SBDs in SiC based power modules [65].

#### C. SiC Intelligent Power Module

Intelligent power modules (IPMs) are advanced power conversion units that combine power semiconductor chips with optimized gate drive and protection circuitry, such as over-current (OC), short-circuit (SC), over temperature (OT), and under voltage lock out (UVLO). The compact, easily assembled IPMs can be beneficial to reducing system size/weight, cost, and time to market, and have been successfully applied for Si based high power conversion system [73].

A similar concept is being leveraged to SiC power semiconductors by different approaches. By replacing Si devices with SiC, SiC based IPMs are starting to be commercially available [74]. Also, several gate drives optimized for the commercial-off-the-shelf SiC modules

were developed and released recently [75], [76]. Although gate drive is not packaged with power module in an integrated fashion, the basic function of the IPMs defined above can be achieved. More versions of SiC based power module integrated with gate drive have been investigated and demonstrated [77]-[80]. They are generally in developmental stages.

TABLE I summarizes the state-of-the-art SiC IPMs. Note that the direct replacement of Si devices by SiC offers limited improvements in actual power electronics circuit as

TABLE I
STATUS OF THE STATE-OF-THE-ART SIC IPMS

No.	Manufacturer/Model	Description	Circuit	Special consideration for SiC
1	Powerex [74] PMF75CL1A120	SiC six pack IPM	Three-phase	Short-circuit protection, soft shutdown
2	Cree (now Infineon) [75] CGD15HB62LP	Gate drive board optimized for SiC modules	Phase-leg	High common mode (CM) transient immunity
3	Agile Switch [76] EDEM3	Gate drive board optimized for SiC modules	Phase-leg	2-level turn-off driving, multi-level shutdown
4	Univ. of Tennessee [77] Research & development	Power module integrated with gate drive in board level	Phase-leg	High temperature, low parasitics and fast switching, fast short-circuit protection
5	Virginia Tech [78] Research & development	Power module integrated with gate drive in board level	Phase-leg	High temperature, decoupling capacitor built in, low parasitic and fast switching
6	North Carolina State Univ [79] Research & development	Power module integrated with gate drive in module level	Phase-leg	Decoupling capacitor built in, low parasitics and fast switching
7	Fraunhofer [80] Research & development	Device chips integrated with gate drive in board level	Phase-leg	Decoupling capacitor built in, low parasitics and fast switching, high CM transient immunity

compared to the inherent capability offered by SiC materials. Therefore, special design considerations of SiC IPMs have to be given, which are highlighted in TABLE I as well.

#### III. SiC Based Power Electronics and Their Benefits

Thanks to superior characteristics offered by SiC at power semiconductor device and module level, SiC based power electronics can be significantly beneficial from converter level and system level. More importantly, with much enhanced capability, SiC based power electronics are able to replace or enhance conventional functions performed by electromagnetic or electromechanical devices, leading to SiC enabled new applications.

This section focuses on the benefits achieved by utilizing SiC in power electronics converters from different aspects along with several examples for effectiveness demonstration.

#### A. Converter Level Benefits

Converter level benefits mainly include improved efficiency, smaller size and lighter weight, enhanced reliability, and reduced cost. They can be realized mainly in the following three ways

1) Substitution of Si PIN Diodes with SiC Schottky Diodes Without any other modification to power converters, the

excellent reverse recovery characteristics of SiC Schottky diodes lead to less switching loss. It is reported that the substitutions of Si PIN diodes with SiC Schottky diodes in applications using 600 V and 1200 V devices enabled more than 50% switching loss reduction [81]. As a result, improved efficiency and reduced cooling requirement can be achieved. For example, based on a 55-kW three-phase inverter in motor drives, test results show that, by merely replacing Si PIN diodes with their SiC Schottky diode counterparts, the losses of an inverter decrease up to 10.7% under motoring mode and 12.7% under regeneration mode [82].

Alternatively, with the given loss budget, increased switching frequency and reduced passive components need can also be realized. Since 2001 when SiC SBDs became commercially available, they have been successfully employed in many products and demonstrated the expected performance in terms of improved efficiency and reliability [1]. Also, hybrid power modules consisting of Si IGBTs or MOSFETs with SiC SBDs are commercially available by multiple suppliers on the market [56], [60].

#### 2) Substitution of Si Active Switches with SiC Devices

In addition to the mitigated reverse recovery, low onstate resistance and fast switching-speed capability of SiC active switches can further reduce power loss, therefore improve power conversion efficiency. Together with high operating temperature of SiC devices, they can also lead to reduced cooling requirement. Moreover, they can lead to high switching frequency and therefore reduced passive components need. In the end, converter power efficiency, power density, and/or temperature capability can be improved.

For example, in the data center power supply system, a 7.5 kW all-SiC three-phase buck rectifier was developed and demonstrated with 98.54% efficiency tested at full load, approximately 70% less loss than Si IGBT based converter. Moreover, SiC version is 10% lighter and 4% smaller [49]. Recently, General Electric has released megawatt level photovoltaic (PV) inverter utilizing SiC MOSFETs with CEC efficiency approaching 99% [14]. Also note that more and more all SiC based power modules with increased current capability become commercially available, which will accelerate the adoption of SiC active devices in commercial products.

### 3) Topology Simplification with High Voltage (HV) SiC Devices

Limited by the voltage and frequency capabilities of Si devices, today's MV drives typically employ complicated multi-level topologies, such as three-level NPC topologies and cascaded H-bridge (CHB) topologies. High voltage and fast switching SiC devices offer an opportunity to achieve the same functions and performance with the simple two-level voltage source converter. The number of active and passive components can be reduced. Therefore, complexity of converter design and operation is reduced, resulting in higher density, higher reliability and lower cost.

It was investigated that in MV motor drive application, high voltage SiC based two-level voltage source inverter exhibited the most promising performance as compared to Si, Si/SiC hybrid, all SiC based three-level NPC inverter, with the fewest number of components, lowest power loss, and smallest cooling system size/weight [83]. Recently the U.S. Department of Energy (DOE) initiated the Next Generation Electric Machines program. One of the main research and development efforts is to leverage recent SiC technology advancements in power electronics of MV megawatt (MW) drive systems for a wide variety of critical energy applications. Using high voltage SiC power semiconductor devices with simplified topology is one of the promising approaches to improve the density by the factor of 3 along with 50% reduction of loss for MV MW level power electronics converter [84]. Also, DOE targets the Technology Readiness Levels (TRL) will improve to 6 or beyond at the end of the program as compared to current TRL of 4 or below. Therefore, it can be expected the commercial product based on this technology will be ready in the near future. Furthermore, SiC device manufacturers have taken the initiative to develop high voltage large current SiC power module to support this effort. It is reported that 10 kV/240 A SiC MOSFETs based phase-leg power modules, and 6.5 kV/ 200 A SiC JFETs based phase-leg power modules have been developing with some promising demonstrations [66], [67].

#### B. System Level Benefits

In addition to power converters themselves, SiC devices also bring benefits at system level as a result of the high switching frequency capability and high control bandwidth, especially for the system where the high controllability is required. One example focusing on the distribution energy resource interface converters in microgrid system is presented here.

A microgrid may contain a number of distribution energy resources (DER), such as photovoltaic (PV), battery energy storage system (BESS), wind turbine generator, etc. Considering the characteristics are similar for grid-interface power electronics converters for different kinds of DER, a PV system and a BESS system are selected as representatives of DERs in this case study. Fig. 3 illustrates the configuration of the 1 MW microgrid with the DER interface converters highlighted. In the following analysis, comparisons based on simulation between Si based interface converter with 3 kHz switching frequency and SiC based one with 10 kHz switching frequency are conducted from different aspects.

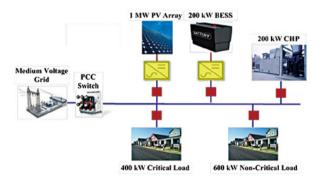


Fig. 3. Configuration of microgrid system.

#### 1) Power Quality Improvement

The growing use of electronic equipment produces a large amount of harmonics in the power distribution systems because of non-sinusoidal currents consumed by nonlinear loads. Traditionally, harmonic distortion in power distribution systems can be suppressed using passive and/or active filters. Thanks to the high voltage high frequency SiC devices, the harmonic compensation function can be integrated into the SiC based DER interface converter. In other words, no dedicated filters are needed.

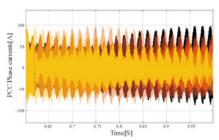
A simulation study was carried out based on configuration in Fig. 3 at 1 MW power rating with six-pulse uncontrolled rectifier as the representative of the non-linear load. It shows that to maintain the Total Demand Distortion (TDD) of the Point of Common Coupling (PCC) on grid side smaller than 5%, in Si based solution with 3 kHz switching frequency, a dedicated active power filter (APF) is required, then the total current rating of the power converter equals the sum of the rms value of the PV output current and the APF output current. In SiC version with 10 kHz switching frequency, the total current rating is almost the same as the rms value of the

PV output current. The simulation results show that in a wide range of grid impedance from 0.01p.u. to 0.15p.u., Si version design needs an extra 150 kVA (15% more) converter for APF while the impact on SiC based converter rating is minimal (~1%). By eliminating the dedicated active filters, the SiC based approach saves about 14% converter rating.

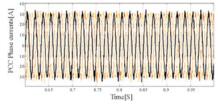
#### 2) System Stability Enhancement

Multiple renewable energy and energy storage interface converters in microgrids, connected to relatively weak grids, can lead to harmonic resonance and stability issues [85], [86]. SiC-based converters, with their switching frequency and high control bandwidth, can help damp the resonance/oscillation and enhance stability.

To investigate the benefits of SiC-based interface converters on the system stability, two cases based on Si and SiC are set up and compared. Specifically, Si based interface converter has lower switching frequency (3 kHz) and limited current control bandwidth (300 Hz) while SiC based converter is with higher switching frequency (10 kHz) and current control bandwidth (1 kHz). As shown in Fig. 4, under the weak grid condition where the grid impedance in 0.1 p.u., integration of Si based interface converter into the microgrid system becomes unstable with the resonance of about 1 kHz while SiC based interface converter is able to ensure the system stability. Due to the advantage of a higher switching frequency and a smaller time delay in the control loop, the SiC-based converter possesses a non-passive range in the higher frequency range, compared with that of the Si-based converter. Therefore, when connecting to a weak grid, the SiC-based converter has a smaller destabilization effect on the system stability, compared with the Si-based converter. In other words, weak grids with SiC-based converters have better stability than those with Si-based converters.



(a) PCC phase current with Si based interface converter.



(b) PCC phase current with SiC based interface converter.

Fig. 4. Simulation results comparison when the grid impedance is 0.1 p.u..

#### C. Enabled Emerging Applications

SiC based converters, with much enhanced capability can

replace or enhance conventional configurations or functions that cannot be achieved by traditional Si based converters with limited capability. This is also an active area of research. Three examples are highlighted here.

#### 1) High-Speed Motor Drive System

The high switching frequency can enable high speed motor which will have higher power density and smaller footprint. The system impact of high speed motors depends on applications.

One example is for the natural high speed loads like compressors, the gearbox can be eliminated for reduced maintenance, high reliability, and potentially lower system cost. The footprint of the high-speed direct-coupled system can be only 41% of the traditional low-speed system with gearbox, and the power density can increase to 2.5 times [83]. Note that there are Si based high speed motor drives available commercially. They either involve de-rating at the high speeds or involve special complex topologies (e.g. multi-level, interleaving).

#### 2) High Performance Solid-state Transformer

Another attractive application of SiC devices is in the replacement of bulky line-frequency 50 or 60 Hz transformers with solid-state alternatives based on high frequency link transformers especially in MV applications, such as distribution grid, shipboard power systems, high-speed train traction drives [87]. A significant size and weight reduction can be achieved for the transformer since the magnetic core size is, as a first order approximation, inversely proportional to its operating frequency, as shown in Fig. 5.



Fig. 5. High frequency vs line frequency transformers.

To realize high frequency (e.g. 20 kHz as in Fig. 5) link for a MV transformer, it would take a large number of low voltage high frequency Si IGBT devices or converters to series, or high voltage low frequency Si IGBT devices or converters to parallel. In contrast, high voltage SiC MOSFETs with their faster switching speed enable power modules with decreased size and weight, and high switching frequency operation (20-40 kHz). Fig. 6 shows the reduction in size achievable with a single high voltage SiC device instead of a stack of lower voltage silicon IGBTs as well as the key static and dynamic characteristics comparison.



Fig. 6. SiC 10 kV modules vs Si IGBT stack.

Fig. 7 shows a prototype SST based on 10-kV, 120-A SiC MOSFETs phase-leg power module, a 1-MW, 4160-V three-phase ac to 1000-V dc converter with a 40 kHz isolation transformer. This unit has a weight of 900 kg, which is approximately 10% of the 60 Hz transformer-rectifier unit used currently. The volume is also reduced to a third of the existing unit.



Fig. 7. Prototype 1 MW, 4160-V ac/1000-V dc converter.

#### 3) Solid-state Fault Current Limiter and Circuit Breaker

Substitution of fuses and circuit breakers (CBs) with SiC based fault current limiters for short-circuit protection is another promising application. Fuses and CBs are proven and reliable protection equipment. However, fuses are single-use devices, which have to be manually replaced and cause prolonged service interruptions; CBs with high-current interrupting capabilities are bulky and expensive electromechanical systems. More importantly, electromechanical CBs are relatively slow and cannot break dc current. Furthermore, due to the increasing power demand in modern electric power system, the higher fault currents are expected. This increased fault current levels may in the future exceed the interrupting capability of existing CBs [88].

Solid-state fault current limiter (SSFCL) and solidstate circuit breaker (SSCB) have been proposed as a new device to limit and/or interrupt fault currents before their first maximum peaks are reached through fast isolating faulted sections. Similar to SSTs, SSFCLs and SSCBs can be realized by both Si and SiC devices. With higher blocking voltages, greater current densities, higher operating temperatures, and faster switching speeds, SiC based SSFCLs and SSCBs can achieve better protection while also have smaller size and high reliability, and eventually lower and acceptable cost. Recently, several MV SiC based SSFCLs have been designed and installed in electric power distribution systems which have successfully demonstrated their functionality and feasibility [6], [89].

#### IV. SIC BASED APPICATIONS

This section summarizes the applications where SiC power devices have been adopted or have potentials to be beneficial and commercialized. It includes but should not be limited to electric utility grid, transportation, industrial motor drive, and power supply. For each example in a given application, specifications, performance and/or benefits with employing SiC are highlighted. Also, the specific realization approaches (e.g. replacement of diode and/or active switch, modification of topology) are presented.

Note that SiC based power conversion systems and applications have been extensively investigated for years and are still active area of research. It is hardly possible to cover all SiC related research activities and product development. The purpose here is to present a few examples to highlight the existing and potential applications for SiC devices along with the benefits due to SiC devices. The resources summarized as follows are mainly from U.S. with some other countries included as well.

#### A. Utility Grid

TABLE II summarizes the selected SiC power converters in utility application, including renewable energy (e.g. PV, wind), distribution grid (e.g. SST), energy storage (e.g. flywheel, BESS), protection (e.g. SSFCL, SSCB), Flexible AC Transmission System (FACTS), and High Voltage Direct Current (HVDC) system.

Efficiency is a key consideration for utility application by adopting SiC based solution. The reduced cooling and passive requirements and the resultant cost reduction and reliability enhancement are also important. Furthermore, the fast dynamics and high control bandwidth as discussed in Section III introduces further benefits.

Also note that some equipment, such as SST, SSFCL, and SSCB, are not limited to utility application but can be leveraged to any applications with electric power system, such as shipboard, electrified train.

#### B. Transportation

TABLE III summarizes several examples of SiC based transportation application, including hybrid electric vehicle (HEV) and electric vehicle (EV), train (including metro), more electric aircraft (MEA). Also, as discussed above, SiC based converter, such as SST, are being developed for shipboard and train as well.

TABLE II
SUMMARY OF SELECTED SIC POWER CONVERSION SYSTEMS IN UTILITY APPLICATIONS

Application	Commercial or R&D, Year	Researcher/ Developer	Specifications, Performance and/ or Benefits by Employing SiC	Realization Approach
PV [16]	R&D, 2016	Technical University of Denmark, Denmark	T-type inverter for Grid-Tie application, 800 Vdc, reduced semiconductor losses by more than 50%, increased converter efficiency up to 1% at light load and more than 60% reduction of cooling requirement with 16 kHz switching frequency, up to 192 kHz switching frequency at 1.5 kW with reduced magnetic size	Substitution of Si IGBTs with SiC MOSFETs
PV [15]	R&D, 2014	Infineon Technologies, Germany	17 kW, 650 Vdc, reduced semiconductor losses in the converter, which maintains electrical performance at high switching frequency and then lowering costs. In the end, achieve up to $20\%$ system cost reduction	Substitution of Si IGBTs with SiC JFETs & topology simplification (3 level to 2 level)
PV [14]	Commercial Product, 2016	General Electric, U.S.	MW class, 1500Vdc, 99% CEC efficiency	Substitution of Si IGBTs with SiC MOSFETs
PV [13]	R&D, 2016	Florida State University, U.S.	T-type inverter, 50 kW, 50 kHz switching frequency, natural convection, 99.1% peak efficiency, 22.7 W/in3 volumetric power density, 2.5 kW/kg specific power, improved power density by a factor of 3 vs Si based state-of-the-art product	Substitution of Si IGBTs with SiC MOSFETs
Wind [12]	R&D, 2006	Peregrine Power LLC, U.S.	Multi-megawatt rating, 30%-50% switching loss reduction and 15%-25% total loss reduction by Substitution of Si diode with SiC SBD, leading to 0.4% increase in average efficiency and energy production. Expected to employ SiC active devices for wind turbine with nominal voltage from 690 to 4,160 Vac	Substitution of Si diodes with SiC Schottky diodes
Wind [11]	R&D, 2011	Tuskegee Univ. / Univ. of Tennessee, U.S.	1.5MW, 690Vac, 1.1 kVdc, improved wind system power conversion efficiency and reduce the system size and cost due to increasing the switching frequency from 3 kHz by Si IGBT to 50kHz by SiC MOSFET with high temperature properties	Substitution of Si IGBTs with SiC MOSFETs
SST [10]	R&D, 2011	Cree, GE, Powerex Inc., NIST, U.S.	10 kV SiC MOSFETs with low switching and conduction losses leads to 75% reduction in weight, 50% reduction in size, 97.1% efficiency, and cooler operation. Note that in addition to utility, SST can be used in other power distribution systems, such as shipboard power system, railway traction system	SiC enabled new application
SST [9]	R&D, 2015	North Carolina State Univ., U.S.	13.8 kV to 480 V grid-interfaced three-phase SST using 15 kV SiC n-IGBT, 96.75% efficiency for transformer-less intelligent power substation	SiC enabled new application
Flywheel ESS [8]	R&D, 2015	Sanken Electric Co. / Nagaoka Power Elec. Co., Japan	Matrix converter, 5 kW, 200 Vac, 25 kHz switching frequency, 98% efficiency, increased lifetime over 20 years, reduced maintenance time and cost by eliminating low lifetime components in the system.	Substitution of Si devices with SiC MOSFETs & topology modification
Battery ESS [7]	R&D, 2016	Univ. of Cambridge/ Univ. of Warwick, UK	1-10 kW converter application range where battery storage is applied, 50.8% loss reduction at 20 kHz by SiC MOSFET vs Si IGBT, 98.8% efficiency at 40kHz by using SiC MOSFETs and 98.6% by using SiC BJT	Substitution of Si IGBTs with SiC active devices
SSFCL [6]	R&D, 2014	Univ. of Arkansas, U.S.	4.16 kV SiC super gate turn-off thyristor based solid state fault current limiter successfully blocked an overcurrent within 40 $\mu s.$	SiC enabled new application
SSCB [5]	R&D, 2016	Wolfspeed, U.S.	SiC module based solid state circuit breaker handles a 250A fault in 10us and a 450A fault in 70us on a 270 VDC bus, reduced space and weight, higher power density, longer lifetime due to absence of mechanical parts	SiC enabled new application
FACTS [4]	R&D, 2014	Central Queensland University, Australia	30 kVA dSTATCOM, reduced power loss, increased allowable environment temperature by using SiC devices, fast switching frequency can lower required DC bus capacitance, which is beneficial to cost and failure rate in power conversion system	Substitution of Si devices with SiC active devices
HVDC [3]	R&D, 2015	SuperGrid Institute / University of Toulouse, France	Insulated dc-dc converter for off-shore wind application, 735 kVA, 20 kVdc output voltage, 10 kHz switching frequency, 99% efficiency by using 10 kV SiC MOSFET	Topology modification

TABLE III
SUMMARY OF SELECTED SIC POWER CONVERSION SYSTEMS IN TRANSPORTATION APPLICATIONS

Application	Commercial or R&D, Year	Researcher/ Developer	Specifications, Performance and/or Benefits by Employing SiC	Realization Approach
HEV [35]	R&D, 2011	Univ. of Tennessee, U.S.	Inverter efficiency up from 74.3% to 89.1 %, system efficiency up from 32.9% to 37.3%	Substitution of Si IGBTs with SiC JFETs
HEV [33]	Commercial product, 2014	Toyota, Japan	5% higher fuel efficiency, 80% reduction in size	Substitution of Si with SiC devices
HEV [31]	R&D, 2013	Nissan research center, Japan	25 kVA, 600 Vdc, 8 kHz switching frequency, 70 kVA/L air-cooled inverter module, 98.8% efficiency with 15 kW-class induction motor	Substitution of Si devices with SiC JFETs
HEV [27]	Commercial product	McLaren Technology Centre, UK	Motor control unit (MCU) -500 used in McLaren P1 road car, 120 kW, > 20 kW/kg specific power	Substitution of Si devices with SiC MOSFETs
HEV [32]	R&D, 2016	North Carolina State Univ., U.S.	Up to 55 kW, 2% higher efficiency, 12.1 kW/L power density	Substitution of Si devices with SiC MOSFETs
HEV [30]	R&D, 2008	National Technical Univ. of Athens, Greece, Lund Institute of Tech., Sweden	5 kW, Efficiency higher than 98%, smaller size, less cooling requirement, 130 $^{\circ}\mathrm{C}$ operation	Substitution of Si devices with SiC BJT
EV [29]	Commercial product, 2014	Mitsubishi Electric, Japan	60 kW/14.1 L	Substitution of Si with SiC devices
EV [26]	R&D, 2016	Siemens / Porsche, Germany	40 kHz switching frequency, 140 kW, 450~850 Vdc, High switching frequency/lower loss, smaller size	Substitution of Si devices with SiC MOSFETs
EV [25]	R&D, 2014	University of Padova, Italy	80 kW, 20 kHz switching frequency, 100 kJ energy saving per driving cycle (5% longer range)	Substitution of Si IGBTs with SiC MOSFETs
EV [24]	R&D, 2014	Fraunhofer IISB, Germany, Swerea IVF, Sweden	290 kVA, 800 Vdc, up to 175 °C operating temperature, smaller size	Substitution of Si IGBTs with SiC BJTs
EV [23]	R&D, 2014	Leibniz University of Hanover, Germany	10 kHz switching frequency, up to 70% loss reduction in energy loss and 66% reduction in chip area	Substitution of Si devices with SiC devices.
EV [28]	Commercial product	Venturi Automobiles, Monaco McLaren, UK	Venturi VM200, up to 200 kW, over 19,000 rpm and over 150 Nm torque peak performance, more competitive to win the FIA Formula-E Championship	Substitution of Si devices with SiC devices.
Metro [17], [18]	Commercial product, 2013	Mitsubishi Electric, Japan	140 kVA, 600 Vdc, Natural air-cooling, installed in Tokyo Metro's Tozai Line subway, 30% less power loss, 20% smaller, 15% lighter, reduced transformer noise by 4dB due to a 35% improvement in the distortion rate of output voltage waveforms, 51% energy regeneration compared to 22.7% of Si based	Substitution of Si IGBTs with SiC devices
MEA [22]	R&D, 2007	ETH Zurich, Switzerland	1.5 kW continuous output power, 5 kW peak output power, 115 Vrms input voltage, 94% efficiency, 1.5 kW/L volumetric power density	Substitution of Si devices with SiC JFET in cascode structure
MEA [21]	R&D, 2016	Microsemi, Ireland University of Nottingham, UK	5 kVA, 540 Vdc, 40 °C lower skin temperature, continued SiC based module operation for 150,000 flight hours	Substitution of Si IGBTs with SiC MOSFETs
MEA [19]	R&D, 2010	Virginia Tech, Boeing, U.S.	10 kW, 70 kHz switching frequency, 3.59 kW/kg specific power, 3.03 kW/L volumetric power density, 95.4% efficiency at 5.1 kW load	Substitution of Si devices with SiC JFETs
MEA [20]	R&D, 2010	Virginia Tech, Boeing, U.S.	15 kW, 650 Vdc, 70 kHz switching frequency, 6.3 kW/L volumetric power density, 2.78 kW/lb specific power, up to 250 °C device operating temperature	Substitution of Si devices with SiC JFETs

In general, high density is a key goal for the SiC based converter in transportation application. High temperature capability may also be important in this application since the ambient temperature of transportation system is usually higher than room temperature. Also, by elevating the device junction operating temperature, less cooling requirement and high density can be realized.

#### C. Industrial Motor Drive

TABLE IV summarizes the selected SiC power converters in industrial motor drive application.

In general, high efficiency, low cost, as well as small volume/footprint are main objectives for SiC based motor drives. For special cases, such as compressors applied in oil

Application	Commercial or R&D, Year	Researcher/ Developer	Specifications, Performance and/or Benefits by Employing SiC	Realization Approach
MV Drive [36]	R&D, 2016	North Carolina State Univ., U.S.	Medium voltage two-level converter using 10 kV SiC MOSFETs, 20 kVA, 6 kVdc, estimated 96.64% efficiency at 20 kHz switching frequency, 4.11 W/inch³ volumetric power density	Topology Simplification with 10 kV SiC MOSFETs
Motor Drive [39]	R&D, 2015	Danfoss Drives, Denmark	18.5 kW, 16 kHz switching frequency, 3% efficiency increase across wide power range (6-17kW) over Si IGBTs	Substitution of Si IGBTs with SiC MOSFETs and SBDs
Motor Drive [38]	R&D, 2007	Cree/ North Carolina State Univ., U.S.	60 kW, 600 Vdc, 10 kHz switching frequency, 68% reduction in conduction loss, 78% reduction in switching loss, 99.1% efficiency with 2% overall increase, and 75% size reduction of heat sink by using SiC vs Si	Substitution of Si IGBTs with SiC MOSFETs
Motor Drive [37]	R&D, 2014	KTH Royal Institute of Technology, Sweden	312 kVA, 550 Vdc, 20 kHz switching frequency 99.3% efficiency over entire load range	Substitution of Si IGBTs with SiC MOSFETs

TABLE IV
SUMMARY OF SELECTED SIC POWER CONVERSION SYSTEMS IN INDUSTRIAL MOTOR DRIVE APPLICATIONS

and gas industry, high temperature capability is also critical. Moreover, compared with low voltage motor drives, medium voltage application is more suitable to fully utilize the advantages of SiC devices, especially with the consideration of integrating high speed medium voltage motors. Then, the high voltage high frequency SiC devices offer a unique opportunity to achieve highly efficient ultra-dense medium voltage integrated motor drive system with relatively simple topology and control.

#### D. Power Supply

TABLE V summarizes several examples of SiC based power converters for power supply, including data center power system, battery charger, and power factor correction (PFC).

In general, efficiency and volume/weight are the main focuses for SiC based power supply. More soft switching topologies with hundreds of kHz up to MHz switching frequency can be observed in this application. As a result, the passive need is significantly reduced, and the small size along with high efficiency can be achieved.

# V. CHALLENGES FOR SIC BASED POWER CONVERSION SYSTEM

Superior characteristics of SiC devices promise to significantly improve today's power conversion system. In the meanwhile, these small and fast devices also pose new design challenges. Special considerations must be given to the converter design with SiC devices in order to utilize them effectively and reliably. The SiC based converter design is still an active area for research. Several key topics are highlighted here.

#### A. Power Module and Packaging

Packaging device dies into power modules involve electrical,

thermal, and mechanical design. The key considerations for SiC based power module packaging are summarized here.

Parasitic minimization: In general, parasitic electrical parameters involved in the switching loop can be categorized as either power device related internal parasitics or interconnection related external parasitics. The internal parasitics include gate-source capacitance, drain-source capacitance, Miller capacitance, and internal gate resistance; the external parasitics mainly include parasitic inductances, such as gate loop inductance, power loop inductance, and common source inductance. All these parasitics can significantly impact the switching performance of power devices, especially for the fast switching SiC devices [90], [91].

For the device module design, we have to accept the internal parasitics, and try to avoid adding extra parasitics to these parameters externally. At the same time, interconnection related external parasitics should be minimized. Some of the effective parasitic minimization techniques include magnetic field cancellation technique and P-cell and N-cell concept [92], [93].

Also, there is a trend to utilize 3D packaging technique to further reduce the power loop inductance inside the module [94]-[97]. With 3D designs, the commutation loop area can be effectively reduced by restricting the commutation loop in the thickness level of the device. Some existing designs revealed significant reductions of power loop inductance due to package [94]-[97].

High temperature packaging: High temperature operation of power modules reduces the cost of power electronics systems through less semiconductor use and/or lower cooling need. As SiC power devices offer higher temperature capability, high temperature packaging becomes critical. New materials and optimized thermo-mechanical design are necessary to prevent the accelerated degradation of the power modules due to high temperature or temperature excursion [98]. The high temperature technologies cover almost all aspects of the packaging: die attach, substrate,

TABLE V
SUMMARY OF SELECTED SIC POWER CONVERSION SYSTEMS IN POWER SUPPLY APPLICATIONS

Application	Commercial or R&D, Year	Researcher/ Developer	Specifications, Performance and/or Benefits by Employing SiC	Realization Approach
Data Center [49]	R&D, 2012	Univ. of Tennessee, U.S.	Three-phase buck rectifier, 7.5 kW, 400 Vdc, 28 kHz switching frequency, 98.54% efficiency, >70% more efficient than Si IGBTs, 10% lighter and 4% smaller than Si	Substitution of Si IGBTs with SiC MOSFETs and SBDs
Data Center [43]	R&D, 2016	ETH Zuric / ABB Switzerland	Three-phase buck-type rectifier, 8 kW, 380 Vdc, 27 kHz switching frequency, 99% efficiency, 4 kW/dm³ volumetric power density	Substitution of Si devices with SiC MOSFETs
Battery Charger [48]	R&D, 2006	Univ. of Tennessee / Oak Ridge National Lab, U.S.	Utility interface for battery system, three-phase voltage source inverter, 3.1% efficiency increase during discharging vs Si; 5.4% efficiency increase during charging vs Si	Substitution of Si IGBTs with SiC JFETs and SBDs
Battery Charger [45]	Near commercially available, 2016	ABB Switzerland	Train application, 10x smaller (1 kW/liter), 80% weight reduction (1 kW/kg), more efficient compared to previous generations	Substitution of Si devices with SiC active devices
Battery Charger [44]	R&D, 2014	Global Power Electronics, U.S.	On-board vehicle battery charger, 3.3 kW, 200 kHz switching frequency, 97.7% peak efficiency and 94.7% overall efficiency, > 1 kW/L volumetric power density	Substitution of Si Super Junction MOSFETs with SiC MOSFETs
Battery Charger [40]	R&D, 2013	APEI, U.S.	On-board vehicle battery charger, phase-shifted full-bridge converter, 6.06 kW, 93.4% efficiency at 500 kHz and 96.5% efficiency at 200 kHz, 12.0 kW/L volumetric power density and 9.1 kW/kg specific power	Substitution of Si devices with SiC active devices
Battery Charger [42]	R&D, 2014	Ikerlan Technological Research Center, Spain	HEV, railway applications, 2.5 kW, 540 Vdc, 100 kHz switching frequency, 97.4% global efficiency, 53.54% reduction in volume of magnetic elements, reduced semiconductor operating temperature	Substitution of Si devices with SiC MOSFETs and SBDs
Battery Charger [41]	R&D, 2016	North Carolina State Univ., U.S.	EV fast charger, single phase medium voltage rectifier, 50 kW, up to 50 kHz, > 96% efficiency at 25 kHz, 0.81 kW/dm³ volumetric power density	Substitution of Si devices with SiC MOSFETs and SBDs
PFC [47]	R&D, 2003	Virginia Tech, U.S.	Single-phase PFC with Si CoolMOS and SiC SBD, 1 kW, 400 kHz, 0.5% efficiency increase at full power, 11W/in <sup>3</sup> volumetric power density	Direct SiC SBD placement
PFC [46]	R&D, 2007	North Carolina State Univ./ CREE, U.S.	250 W, up to 1 MHz switching frequency, 2% efficiency increase and 33% smaller heat sink (SiC MOSFET vs. Si CoolMOS)	Substitution of Si CoolMOS with SiC MOSFETs

encapsulant, and interconnection structure.

Device paralleling: Today, due to the limited current rating of single die of SiC device, development of SiC based power module with multiple dies in parallel is necessary for high power conversion system. The positive coefficient of onstate resistance of most SiC devices allows each paralleled device to achieve current sharing naturally. However, special attention must be paid to the dynamic current sharing during fast switching transient since the switching behavior of SiC devices is highly sensitive to the mismatch of parasitics in the switching loop (e.g. gate loop inductance). Accordingly, parasitics of each die should be carefully controlled via packaging and layout design to ensure good dynamic current sharing.

Capacitive coupling effect: Inside the power module, a layer of insulating material is used to separate the SiC devices from the electrically conductive baseplate. Thus, a chip to baseplate capacitance is formed [99]. Via the baseplate of power module, this coupling capacitance is

paralleled with SiC devices, which increases their equivalent output capacitance, and worsens the switching behavior. Additionally, the chip to baseplate capacitance together with high *dv/dt* during fast switching transient will generate large CM current (37.5 A in three-phase voltage source inverter reported in [100]), causing severe EMI issue.

#### B. Gate Drive

As the interface between the micro-controller and power semiconductor devices, gate driver is a key component to achieve the optimal performance of devices in actual power converters. To fully utilize the potential benefits of SiC devices in actual converters, specifically the fast switching speed, the gate driver design is critical. Fig. 8 displays the components of gate driver circuits in the phaseleg configuration. Generally, gate driver mainly consists of driver integrated circuit (IC), signal isolator, and isolated power supply.

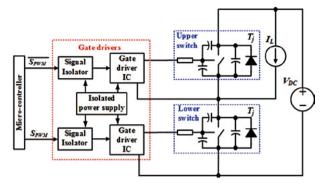


Fig. 8. Gate driver circuits in a phase-leg configuration.

Special attention needs to be paid to gate driver IC, since it directly interfaces with the gate terminals of power devices and is a key component to switching performance of power devices. There are three critical parameters for a gate driver IC that determine the gate driving capability, including pull-up (-down) resistance of gate driver, rise (fall) time, and amplitude of gate driver output voltage. For SiC MOSFETs, considering the modest transconductance and relatively high Miller voltage as compared to the Si counterparts, the amplitude of gate driver output voltage plays a significant role on the switching behavior [101]. Based on this, an intelligent gate driver for SiC was proposed via actively tuning gate voltage during switching transient to enhance the gate driving capability to best serve SiC MOSFETs [102].

Additionally, signal isolator and isolated power supply can also become the limitations of the switching speed if the fast switching transient causes them to operate abnormally. In a phase-leg configuration, the ground of the secondary side of signal isolator and isolated power supply for the upper switch associated gate driver circuit swings from dc bus voltage to 0 when the states of power devices are changing. Therefore, the primary and secondary sides of isolation components suffer high dv/dt during the switching transient. Meanwhile, the input-to-output parasitic capacitance offers a path to conduct CM noise induced by dv/dt [103], [104]. In the end, pulse-width-modulation (PWM) signals from micro-controller will be interfered; and the output voltage quality of the isolated power supply will be affected. For SiC devices with high dv/dt during fast switching, high CM noise immunity capability or low input-to-output parasitic capacitance is a critical selection criterion of signal isolator and isolated power supply.

To fully utilize the high operating temperature capability of SiC devices, their neighboring components must be capable of enduring high temperature. Considering that the gate driver circuits are preferred to be near the power devices for parasitic minimization, high temperature gate driver is an important design consideration. Currently, several gate drivers based on silicon on insulator (SOI) technology have been developed to operate at high temperature (e.g. > 200 °C). However, they are generally bulky and expensive [105], [106].

Furthermore, SiC gate drive design also faces several

unique challenges due to the inherent properties of these emerging power devices. For example, for normally-off SiC JFETs, the gate is not insulated from the channel by an oxide as MOSFETs, but forms a pn-junction with drain and source terminals, it is therefore required to inject hundreds of milliamps gate-source current during the onstate. On the other hand, during the switching transient, the gate drive should sink or source several amperes peak gate current to achieve fast switching [107]. To meet the different requirements for turn-on and turn-off switching transients on one hand and the steady on-state on the other hand, a gate driver with multiple driving stages should be designed [108].

#### C. Protection

Considering their intrinsic properties, SiC devices pose two unique challenges that can threaten the reliable operation of the power converters. One is the cross-talk among devices in a converter, e.g. between two devise in a voltage source converter (VSC) phase-leg, and the other is the limited overcurrent capability [109].

High dv/dt during a fast switching transient of one device will affect the operating behavior of its complementary device in the same phase leg. This interaction between two switches is cross-talk. Specifically, during the turnon transient of the lower switch, as can be observed in Fig. 9(a), the positive charge stored in the Miller capacitance of the upper switch is transferred via its gate loop, inducing a positive spurious gate voltage. Thus, the upper switch may be partially turned on; and a shoot-through current will be generated, leading to additional switching losses in both switches and even shoot-through failure. On the other hand, during the turn-off transient of the lower switch, as shown in Fig. 9(b), the negative spurious voltage induced at the gate-source terminals of the upper switch may overstress the power device if its magnitude exceeds the maximum allowable negative gate voltage acceptable to the semiconductor device. With low threshold voltage, large internal gate resistance, and fast switching-speed, crosstalk is a clear hazard for safe operation of SiC devices in the VSC. Often, to avoid cross-talk, the high switchingspeed capability of SiC devices has to be compromised. To suppress cross-talk without sacrificing fast switching, several gate assist circuits were developed [102], [110]-[114]. Some are all transistor-based, which can be conveniently integrated with conventional gate driver IC [115], [116]. In the end, there is no extra complexity for end users.

Additionally, compared with Si devices, the short circuit protection of SiC MOSFETs is more challenging in several aspects. From thermal standpoint, SiC MOSFETs tend to have lower short circuit withstand capability, compared with Si IGBTs and MOSFETs, due to smaller chip area and higher current density [68]-[71]. The lower short circuit withstand capability requires a faster response time of the protection circuit to guarantee SiC MOSFETs operating within the safe operating areas (SOA). In addition to thermal breakdown, an overcurrent condition also has negative

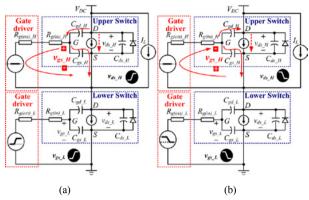


Fig. 9. Mechanisms causing cross-talk: (a) Turn-on transient; and (b) Turn-off transient

impact on the long term stability of SiC MOSFETs, which had in the past suffered gate oxide reliability issues caused by poor interface quality [117]. Under high di/dt and dv/dtcondition, it is difficult for a short circuit protection scheme to achieve fast response time and strong noise immunity simultaneously. Currently, no IEEE standards or published work exists on the allowable response time for protection of WBG devices. A faster fault response time is always desirable to avoid device damage and/or degradation, as long as sufficient noise immunity can be guaranteed. To cope with this issue, a desaturation technique suitable for WBG devices was proposed to provide fast detection. It can help to clear a short-circuit fault within 200 ns [118]. Also note that several latest generation SiC MOSFETs with enhanced short-circuit withstand capability have been developed and demonstrated with more than 10 µs short-circuit sustaining time. But currently these devices are only available at medium voltage level. Also, to enhance the short-circuit withstand capability, device's switching performance often has to be compromised. Therefore, to maximize the benefits of SiC devices, the fast response short-circuit protection with strong noise immunity capability is always preferred.

Voltage spikes during switching transients can cause device breakdown. SiC devices with high switching-speed capability and small on-state resistance exacerbate the problem. Note also that compared with the overvoltage of the operating switch during the turn-off transient, which has been extensively investigated for Si devices, the voltage spikes of the non-operating switch in the same phase leg during the turn-on transient can be more severe for SiC devices [119]. Advanced packaging techniques and optimal layout design for parasitics minimization can relieve the overvoltage.

#### D. Interaction with Loads

High switching-speed of SiC devices leads to low switching loss and enables high switching frequency. However, high *di/dt* and *dv/dt* during the fast switching transient worsens the electromagnetic environment of loads. In the meantime, fast switching makes the switching performance of SiC devices significantly susceptible to the loads' parasitics. In the end, the interaction between converter and load due to fast switching

SiC devices challenges the performance and reliability of the whole system.

First, voltage pulses with fast rise time generated by PWM switching of power devices can cause serious non-uniform voltage distribution in motor windings, and voltage doubling effect at motor terminals for motor loads with long power cables. The phenomenon is detrimental to motor insulation, and would require dedicated filter or special motor to mitigate. This is a well-known issue with Si device based PWM drives, and becomes more severe when SiC devices are utilized. Moreover, high *dv/dt* induced by SiC devices can cause larger shaft voltage and bearing current in motor loads, detrimental to motor reliability.

Furthermore, high switching-speed performance of SiC devices will be affected by parasitics of loads. Fig. 10 depicts the impedance of 7.5-kW induction motor plus 2-meter power cable with the frequency range from 10 kHz to 100 MHz. It can be observed that the motor load is no longer inductive in the switching-related frequency range which is determined by the switching speed and typically at several MHz to tens of MHz for SiC devices considering switching intervals of tens of nanoseconds [120]. The load and cable parasitic impedances worsen the SiC devices' switching performance. It is reported that due to parasitics of the inductive load in Fig. 10, the tested switching time of SiC MOSFETs increases up to 42% during turn-on, and doubles during turn-off; an additional 32% of energy loss is dissipated during the switching transient. Also, for the higher power rating induction motor with longer power cable, the associated impedance at high frequency is even lower [121]. One solution to address this issue is to insert an auxiliary filter between converter and load to reshape the high frequency impedance of load such that parasitics of the load will "not be seen" or be masked from the converter side during the switching transient [122].

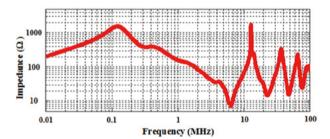


Fig. 10. High frequency impedance of 7.5-kW induction motor plus 2-meter power cable.

#### E. EMI Filter

SiC devices with high switching frequency operation provide the opportunity to shrink the size of passive EMI filters. However, electromagnetic noise will also trend to concentrate in the high frequency range and increase filter design difficulties due to the non-ideal behaviors of passive components at high frequencies. When switching frequency is in the EMI standard range, the non-ideality of the passive filter, i.e. the equivalent parallel capacitance (EPC) of

inductors and the equivalent series inductance (ESL) of capacitors and related self-resonant frequency, will present significant impact on filter insertion gain. This challenges the filter component design. Better winding schemes to reduce the EPC and better filter scheme to reduce inductance/ capacitance values and filter size to further reduce EPC and ESL, may be needed. Also, high frequency has more to do with the non-ideality of core material property, e.g. the widely used nanocrystalline core for CM choke has fast permeability drop above hundreds of kHz. Better solution on choke design may be needed, such as combination of core materials associated with different frequency properties [123], combination of active and passive filters to cancel the lower frequency CM noise via active filter and reduce the needed value/size of passive filter to enhance its high frequency performance [124].

At high frequencies, the coupling effect of filter components through capacitive path and inductive path also becomes worse. In low switching frequency converters, though coupling exists, converter noise can be already attenuated considerably at the typical coupling frequency range. Whereas, in high switching frequency converters, since the main noise spectrum is in or closer to the range of coupling frequency, filter attenuation will be significantly degraded. Careful filter layout and component placement to mitigate the coupling, coupling cancellation schemes [125], or filter approaches that can avoid component coupling are desired.

#### F. Thermal Management

Generally, due to the highly-efficient SiC based power conversion system, less cooling is required. However, similar to the capacitive coupling effect within the power module, usually a thin layer of insulating material is used to separate the SiC devices from the electrically conductive heat sink. Thus, a parasitic capacitance is formed between the drain base plate of the SiC devices and the common heat sink plate, as shown in Fig. 11 [99]. In the end, this capacitance is paralleled with devices, which increases their effective output capacitance, and then negatively affects the switching speed.

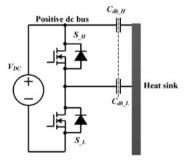


Fig. 11. Capacitive coupling between devices and heat sink.

The key reason for the capacitive coupling effect is the existence of a common heat sink for the upper and lower switches in the phase-leg. One approach to cancel the effect

of capacitive coupling is to decouple the lower and upper switches to separate heat sinks, i.e. one heat sink is used for all upper switches and the other for all lower switches in the phase-leg [99]. The method is effective only if two heat sinks can have different potentials.

#### G. Control

Control is an essential part of the power electronics converter system. There are many levels of controls. A suitable control architecture, based on the layered hierarchical control for high power converters, is recommended in [126] and illustrated in Fig. 12. There are many levels of controls, including hardware control layer, switching control layer, converter control layer, application control layer, and system control layer. Compared with the traditional Si based power conversion system, fast switching SiC devices pose several challenges, which are highlighted in Fig. 12 as well.

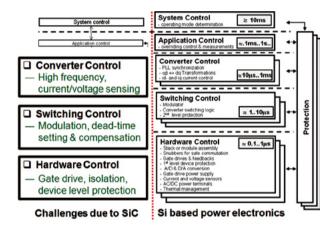


Fig. 12. Control architecture based on Si power electronics converter and challenges due to SiC.

Hardware control layer: Manages everything specific to the power devices, such as gate drives and it may consist of multiple modules depending on the power requirements. For SiC devices, gate drive, isolation, and device level protection are challenging. Details are discussed in Parts B and C in this section. Also note that compared with Si devices with 0.1 -1 μs control time in hardware control layer, fast switching SiC devices shorten it by a factor of 10 in the range of 0.01-0.1 μs.

Switching control layer: Enables the power electronics to behave as a switch-mode controlled source and includes modulation control and pulse generation. For SiC, modulation, especially considering the impact of dead-time for high frequency converter, is critical. More details are discussed as follows. Similar as the hardware control layer, the allowable control time for SiC devices becomes shorter.

Converter control layer: Enables the application control layer to perform its mission by implementing many of the functions common to all converters such as synchronous timing (phase-locked-loop), current and voltage filtering, measurements, and feedback control calculations. This layer will include the current control loop, which is independent of the application. Fast switching SiC enables higher switching

frequency and control bandwidth, in the meantime, shortens the control algorithm execution time and challenges the computing capability of micro-controller. For 100s of kHz to MHz switching frequency application, depending on the complexity of the control strategy, probably, the duty cycle (i.e. comparator value) of the PWM signal has to be updated per several switching cycles. Additionally, current/voltage sensing becomes highly susceptible to the noise introduced by high speed devices operating at high frequency. Detailed discussion of current/voltage sensing is presented as follows.

System and application control layers: System control layer covers all functions involved in the determination of the system mission and thus the duties of the power electronics system or their mode of operation. And application control layer dictates the operation of the power electronic system in order to meet the mission determined by the system control. Impact of SiC devices on these two control layers includes added functionalities as discussed in Section III.

Two unique challenges due to SiC devices with respect to control are highlighted as follows. It includes modulation with the consideration of dead-time effect and current/voltage sensing.

#### 1) Dead-Time Setting and Compensation

Modulation with the consideration of finite switching interval and associated dead-time effect significantly affect the performance of high frequency power conversion system. For example, turn-off time of SiC devices is highly sensitive to the operating conditions. As can be observed in Fig. 13, based on 1200-V/20 A SiC MOSFETs, compared to the tested turn-off time at the operating current of 20 A, turn-off time at 5 A increases by a factor of 5 [102]. Thus, the traditional fixed dead-time depending on turn-off time at the worst operating point (i.e. 600-V/20-A in Fig. 13) is not suitable for SiC based voltage source converter. Also, for the SiC MOSFETs without SBD in parallel, the reverse conduction induced extra energy loss during the superfluous dead-time is significantly higher than the loss dissipated in the switch channel. Moreover, this reverse conduction loss is dissipated during each switching cycle and comparable to the switching loss [127]. Accordingly, dead-time setting for SiC devices is more critical as compared to the traditional Si counterparts. Adaptive dead-time regulation has been investigated to achieve the satisfactory tradeoff between efficiency and reliability [127].

Also, fast speed switching intensifies the impact of parasitics on switching commutation, and affects the power quality of the power converter. For example, when SiC based ac/dc converter is operated at high switching frequency, non-ideal voltage commutation becomes a key distortion factor for power quality control especially around each current zero crossing region. Also note that the parasitics of inductive load in practice significantly affect the switching commutation. Fig. 14 illustrates that under the same operating condition, turn-off time with the motor load is doubled as compared to that when an optimally-designed inductor load is employed [128]. This voltage ramping

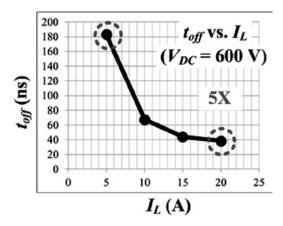


Fig. 13. Turn off time dependence on inductive load current.

introduces voltage loss compared to the ideal PWM voltage, leading to even harmonics for single phase ac/dc and 6k±1 order harmonics for three phase converter [129]. The higher the switching frequency is, the more severe voltage loss in a shorter switching period becomes. This effect shows the worst distortion in switch-diode configured converters such as Vienna-type rectifier, and it can also be accompanied with dead time effect or overlap time effect in phase-leg configured voltage source converters or current source converters. Compensation methods from voltage-second equivalence by adjusting duty cycle in each switching cycle [130] or by modulation compensation [129], [131], to feedback control [132]-[135] have been studied in recent years.

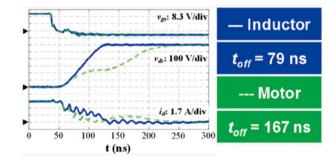


Fig. 14. Turn-off commutation time dependence on different inductive loads.

#### 2) Current/Voltage Sensing

The integrity of current and voltage sensing signals is the basis for feedback control. However, a current sensor works normally at low switching speed in a typical Si based converter might be severely distorted under high-frequency high-speed conditions when SiC devices are adopted. It is found that for current sensors, the capacitive coupling due to high dv/dt and magnetic coupling due to high di/dt from the SiC device switching node and loop, have impeded the effective control of current quality. Different approaches have been considered to mitigate these two distortion effects, such as better arrangement of sensor location (e.g. instead of placing the current senor to the terminal of the converter, one can put it on the other side of the inductor), selection of

sensor with built-in capacitive shielding or applying proper exterior shielding, di/dt decoupling solutions, and etc.

#### VI. CONCLUSIONS AND FUTURE TRENDS

This paper overviews the wide bandgap SiC technology. The focus is on the benefits, opportunities, and challenges with SiC based power electronics. The following observations and conclusions can be made and drawn from this paper:

- With smaller size, lower loss, faster switching, and higher temperature capability, SiC devices can improve power conversion systems in several ways: by direct substitution of Si devices in existing circuits for improved efficiency and power density, by simplifying the circuit topology for reduced complexity and further enhanced power density, and by enabling system configuration modification for overall system power density improvement and lower cost.
- 2) In addition to the converter level benefits, SiC power electronics can further introduce system-level benefits as a result of fast switching capability and high available control bandwidth. The examples of system-level benefits include integrated harmonic filtering and stabilizer functions of the SiC based DER interface converters in a distribution grid or a microgrid.
- 3) SiC can also enable new power electronics applications that were previously not feasible with Si technology due to performance, cost, efficiency, reliability or density concerns. Examples include high-speed motor drive, SST, SSCB, and SSFCL. More emerging applications can be expected with SiC as a key enabling technology.
- 4) With faster switching, higher temperature, and smaller size, SiC also raise new design and application challenges. Gate drive and protection need to be faster and more adaptive. Loads can interfere with converter switching, therefore may require additional filters. High temperature and fast switching also demands better device packaging. Other challenges include thermal management, EMI filters, sensors and control. Many solutions have been and are being developed. However, the design and application methodology for SiC power electronics will remain an active research area for the foreseeable future.

Many of the advances presented in this paper are not yet mature and under rapid development. It is expected that SiC devices and related technologies will become mature, resulting in devices with lower cost, higher current ratings, better reliability, better gate drive and protection technologies, and more robust high temperature package. Consequently, they will be applied in more commercial power electronics converters.

One key to overcome adoption barrier of SiC and other WBG technologies is to train a new generation of engineers in the area of WBG power electronics. The U.S. DOE sponsored WBG Traineeship Program at University of Tennessee and Virginia Tech is a step in the right direction.

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# Bidirectional Isolated Dual-Active-Bridge (DAB) DC-DC Converters Using 1.2-kV 400-A SiC-MOSFET Dual Modules

Hirofumi Akagi, Shin-ichi Kinouchi, and Yuji Miyazaki

Abstract—This paper describes the 750-Vdc, 100-kW, 20-kHz bidirectional isolated dual-active-bridge (DAB) dcdc converters using four 1.2-kV 400-A SiC-MOSFET dual modules with or without Schottky barrier diodes (SBDs). When no SBD is integrated into each dual module, the conversion efficiency from the dc-input to the dc-output terminals is accurately measured to be 98.0% at the rated-power (100 kW) operation, and the maximum conversion efficiency is as high as 98.8% at 41-kW operation, excluding the gatedrive and control-circuit losses from the total power loss. The bidirectional isolated DAB dc-dc converters are so flexible that series and/or parallel connections of their individual input and output terminals make it easy to expand the voltage and current ratings for various applications such as the so-called "solid-state transformer" or "power electronic transformer."

Index Terms—Bidirectional isolated dc-dc converters, conversion efficiency, dual-active-bridge configuration, SiC-MOSFET modules.

#### I. Introduction

BIDIRECTIONAL isolated dc-dc converters have been expected to play an important role in integrating battery energy storage systems into medium-voltage and/or low-voltage dc power systems. Particular attention has been paid to a bidirectional isolated dc-dc converter combining two single-phase or three-phase full-bridge voltage-source converters with a single-phase or three-phase high-frequency transformer [1].

Fig.1 shows the basic circuit configuration of the bidirectional isolated dc-dc converter based on two single-phase voltage-source converters using eight MOSFETs and antiparallel diodes as the power switching devices. This kind of dc-dc converter is often referred to as the "dual-active-

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bridge v(DAB) converter." This naming comes from circuit topology [2], while the original naming of the "bidirectional isolated dc-dc converter" comes from functionality. Strictly speaking, this dc-dc converter should be referred to as the "bidirectional isolated DAB dc-dc converter," to identify itself clearly and to avoid confusion.

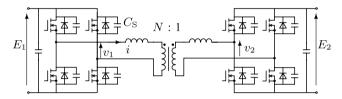


Fig. 1. Bidirectional isolated dual-active-bridge (DAB) dc-dc converter.

The DAB dc-dc converter is symmetrical in circuit topology when the two voltage-source converters are seen upstream and downstream of the high-frequency transformer whose turns ratio is unity (N=1) in Fig. 1. The dc-dc converter is characterized by less switching stress on the MOSFETs and diodes, and less ripple voltage/current stress on the dc two capacitors. The reason is that the auxiliary lossless snubber capacitor Cs, connected across each MOSFET, allows the dc-dc converter to achieve zero-voltage switching (ZVS). This makes it possible to construct bidirectional isolated dcdc converters in a range from a few tens to several hundreds of kilowatts, depending strongly on available power devices and their optimal switching frequencies. However, one of the most important research items for putting them into practical use is to improve conversion efficiency at high-frequency operation [3]-[14].

Recently, a significant progress has been made in SiC (Silicon Carbide) power devices as a result of continuous efforts by research scientists and engineers. This progress has made it possible to fabricate not only discrete SiC-SBDs (Schottky barrier diodes), SiC-JFETs and SiC-MOSFETs but also SiC-MOSFET/SBD modules [15]. Conventional 1.2-kV Si-IGBT/PND modules can be replaced with emerging 1.2-kV SiC-MOSFET/SBD modules, thus leading to higher conversion efficiencies and/or higher switching frequencies [16], [17].

This paper design, construct, and test two 750-Vdc, 100-kW, 20-kHz bidirectional isolated DAB dc-dc converters using four 1.2-kV 400-A SiC-MOSFET dual modules. Note that the "dual module," forming one leg by itself, is referred

to as the "two-in-one" module in some cases. One dc-dc converter has a Schottky barrier diode (SBD) connected in anti-parallel to each SiC MOSFET, and the other has no SBD connected. The two converters are the same in voltage, current, and operating frequency except that the SiC-MOSFET dual modules have SBDs integrated or not.

Unlike an insulated-gate bipolar transistor (IGBT), any MOSFET, irrespective of Silicon or Silicon Carbide, has the capability of bidirectional current flow as long as a much higher positive voltage than the so-called "threshold voltage" is applied to the gate terminal with respect to the source terminal. Since the MOSFET has no "built-in voltage," it has a lower on-state voltage at small drain currents than does the IGBT. Moreover, the MOSFET has the so-called "body diode" inherent in it. Hence, operating the MOSFET with synchronous-rectification mode makes it possible to remove the anti-parallel SBD from the MOSFET because the body diode acts as the anti-parallel diode during a dead or blanking time. The removal of the anti-parallel SBDs would make a significant contribution to cost reduction from a business point of view.

One objective of this paper is to accurately measure the overall power loss of the 750-Vdc, 100-kW, 20-kHz DAB dc-dc converters using 1.2-kV 400-A SiC-MOSFET dual modules with or without SBDs, excluding the gate-drive and control-circuit power losses. The other is to verify stable operation of the DAB dc-dc converter using SiC-MOSFET dual modules without SBDs in synchronous-rectification mode. Experimental results obtained from the dc-dc converter using SiC-MOSFET dual modules verify that the maximum conversion efficiency from the dc input terminals to the dc output terminals is 98.8% at 41 kW and that the conversion efficiency at 100 kW is 98.0% with a tolerance of 0.03%.

In the near future, the conversion efficiency will reach higher than 99% in a broad power range from an extremely-light load to the rated load when the next-generation trenchgate SiC-MOSFET modules and new magnetic materials are available. Finally, this paper provides three possible circuit configurations making series and/or parallel connections of two identical DAB dc-dc converters, intended for expanding their voltage and current ratings.

#### II. OPERATION OF THE DAB DC-DC CONVERTER

Fig. 1 shows a general bidirectional isolated dual-active-bridge dc-dc converter suitable for high-power applications [1]-[3]. When the phase-shift control proposed in [1] is applied to the dc-dc converter, the two bridge converters produce two "180°-conducting" rectangular voltages,  $v_1$  and  $v_2$ , with a phase difference of  $\delta$  and different amplitudes of  $E_1$  and  $E_2$ , respectively. The dc-output power can be controlled by adjusting the phase-shift angle  $\delta$  between  $v_1$  and  $v_2$  is given by

$$P = \frac{E_1 N E_2}{\omega L} \delta \left( 1 - \frac{|\delta|}{\pi} \right). \tag{1}$$

Here,  $\delta$  takes a positive value when  $v_1$  leads  $v_2$  by  $\delta$ , N is a voltage ratio of the transformer, f is the switching frequency ( $\omega = 2\pi f$ ), and

$$L = L_{\mathcal{A}} + l,\tag{2}$$

where L is the equivalent inductance given by the summation of the four auxiliary inductors and the leakage inductance of the transformer, in which both inductance values are referred to the primary side of the transformer. When  $\delta$  takes a positive value, power flow occurs from left to right in Fig. 1. Both bridges 1 and 2 are operated with "synchronous rectification mode" in which an arm current flows through the corresponding MOSFET. Therefore, no current flows through the SBD connected in anti-parallel to the MOSFET under such an ideal condition that no dead time exists in each leg of bridges 1 and 2.

#### III. EXPERIMENTAL SYSTEM

#### A. Circuit Configuration and Conversion Efficiency

Fig. 2 shows the experimental circuit configuration of the 750-Vdc, 100-kW, 20-kHz bidirectional isolated dcdc converter using 1.2-kV 400-A SiC-MOSFET/SBD dual modules. Note that the MOSFET and SBD power chips designed and fabricated by Mitsubishi Electric were mounted on each dual module. This converter is designed, constructed for accurately measuring the overall power loss from the dc input terminals to the dc output terminals. This circuit configuration is characterized by directly connecting the dc output terminals of bridge 2 back to the dc input terminals of bridge 1.

TABLE I summarizes the circuit parameters used in Fig. 2. The dc-dc converter consists of the four 1.2-kV, 400-A SiCMOSFET/ SBD dual modules, a single-phase 20-kHz transformer with unity voltage ratio, four auxiliary inductors  $L_{\rm A}$ , and eight auxiliary snubber capacitors  $C_{\rm S}$ . If 3.3-kV SiCMOSFET modules were available, it would be possible to design, build and test another bidirectional isolated dc-dc converter with a voltage ratio of N:1 in which N is not unity. In the following experiments, however, used are only the 1.2-kV, 400-A SiC-MOSFET dual modules with or without SBDs. Therefore, a transformer with unity voltage ratio is

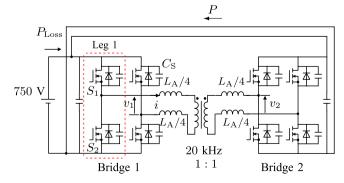


Fig. 2. Experimental circuit using four 1.2-kV 400-A SiC-MOSFET dual modules, each of which has two SBDs integrated.

used with paying attention to the overall power loss of the dc-dc converter rated at 750 Vdc, 100 kW, and 20 kHz.

TABLE I
CIRCUIT PARAMETERS OF THE EXPERIMENTAL
CIRCUIT SHOWN IN FIG. 2.

Power rating		100 kW
Input/output voltage rating	E	750 Vdc
Switching frequency	f	20 kHz
Auxiliary inductor	$L_{\rm A}$	16.6 μΗ (37.1%)
Leakage inductance	l	0.7 μΗ (1.6%)
Phase shift angle	δ	$0-\pm 26.6^{\circ}$
Snubber capacitor	$C_{\mathrm{s}}$	4.5 nF / 9 nF
Dead time	$T_{\mathrm{D}}$	0.6 μs / 0.8 μs
Transformer core material		FINEMET*
Maximum flux density		0.48 T at 20 kHz
Transformer voltage ratio	·	1:1

<sup>\*</sup> Nano-crystalline soft-magnetic material.

Generally, a university laboratory has the difficulty of providing the 750-Vdc 100-kW dc power supply and resistive load necessary for this experiment. This difficulty can be solved by actively using the functions of galvanic isolation and unity voltage ratio between the dc input terminals and the dc output terminals. In other words, the dc output terminals of bridge 2 are directly connected to the dc input terminals of bridge 1, so as to regenerate the output power P to the dc input terminals [4]. As a result, the 750-V dc power supply feeds a small amount of electric power, which corresponds to the overall power loss  $P_{\rm Loss}$ . This configuration allows the direct measurement of  $P_{\rm Loss}$ , independent of the measurement of P.

The conversion efficiency from the dc input terminals to the dc output terminals,  $\eta$  can be calculated by

$$\eta = \frac{P}{P + P_{\text{Loss}}}. (3)$$

A digital power analyzer (HIOKI 3390-10) was used to measure P and  $P_{\rm Loss}$  simultaneously and individually. As a result, the accurate conversion efficiency obtained from (3) has a tolerance as small as 0.03% under such an acceptable assumption that  $P_{\rm Loss}$  is much smaller than P. It would be impossible to attain such a small tolerance when the dcinput power and the dc-output power were measured simultaneously and individually even if a high-performance digital power analyzer were used.

### B. Design of Auxiliary Snubber Capacitors and Inductors

As shown in Fig. 2, the auxiliary snubber capacitor  $C_{\rm S}$  is connected across each SiC-MOSFET/SBD in order to reduce both switching loss and overvoltage. Like the equivalent inductor given by (2), the equivalent capacitance C is defined

by

$$C = C_{\rm S} + C_{\rm ds},\tag{4}$$

where  $C_{\rm s}$  is the auxiliary snubber capacitor, and  $C_{\rm ds}$  is the parasitic drain-to-source capacitance across each SiC-MOSFET/SBD. The series resonance between the equivalent inductance and the equivalent capacitance C allows the dc-dc converter to achieve zero-voltage switching (ZVS).

A tradeoff or compromise exists in selecting the auxiliary inductor  $L_{\rm A}$ . As the inductor value is reduced, the phase-shift angle becomes smaller as long as the dc output power P is constant, as seen from (1). This requires a fine adjustment and a high resolution to the phase-shift angle  $\delta$  although the inductor size, volume and cost are minimized. Thus, the authors have designed the phase-shift angle  $\delta$  to be in a range from  $-26.6^{\circ}$  to  $26.6^{\circ}$ .

#### C. Design of an Optimal Dead Time

The authors of [18] have presented an optimal dead time  $T_{\rm DOpt}$  for minimizing the snubber loss as follows:

$$T_{\rm DOpt} = \frac{\pi\sqrt{LC}}{2}. (5)$$

Equation (5) includes the equivalent capacitance C, so that the optimal dead time should be changed, according to the capacitance value of  $C_{\rm S}$ . Experimental voltage waveforms allow the authors to set the optimal dead time to  $0.6~\mu \rm s$  for  $C_{\rm S} = 4.5~\rm nF$  and to  $0.8~\mu \rm s$  for  $C_{\rm S} = 9~\rm nF$ . Under the ZVS operation, the duration of the current flowing through each SBD is shorter than the optimal dead time. Moreover, the duration of the current flowing through the equivalent capacitance C becomes longer as the output power P decreases.

#### D. Phase-Shift Control and Synchronous Rectification

As to the control method for the dc-dc converter, this paper does not use any pulsewidth modulation (PWM) but uses the phase-shift control proposed in [1]. This phase-shift control yields two  $180^{\circ}$ -conducting rectangular voltages,  $v_1$  and  $v_2$ , with the same amplitude as 750 V but with a phaseangle difference of  $\delta$ , as shown in the voltage waveforms of Fig. 3. The phase-shift control is characterized by being able to achieve zero-voltage switching in a broad range of 20 to 100 kW, as shown in Fig. 5 later on. However, once a PWM method is used for the dc-dc converter, hard switching happens in all the range of power transfer, so that the switching loss increases.

As mentioned in section II, the use of MOSFET modules make both bridges 1 and 2 operate with synchronous rectification mode. Note that it is impossible to apply synchronous rectification mode to the dual-active-bridge converter using IGBT modules. Synchronous rectification mode allows the "reverse" current to flow in the MOSFET from the source to the drain with a voltage drop across the

MOSFET as low as 1.1 V at 150 A, not to flow in the antiparallel Schottky barrier diode (SBD) as long as a positive gate-to-source voltage of 15 V is applied to the MOSFET. It is well known that the MOSFET is lower in on-resistance than the external SBD and the parasitic or internal pnjunction diode (PND) inherent in the MOSFET. Moreover, the conducting time of each SBD is shorter than an optimal dead time (=  $0.6 \mu s$ ) in Fig. 2, which is much shorter than a period of time of 20 kHz (=  $50 \mu s$ ).

# IV. WHEN THE 1.2-KV 400-A SIC-MOSFET DUAL MODULES WITH SBDs ARE USED

# A. Experimental Waveforms, Overall Power Loss, and Conversion Efficiency

Fig. 3 shows experimental waveforms of the ac terminal voltages appearing across bridges 1 and 2,  $v_1$  and  $v_2$ , respectively, and the ac current flowing at the ac side of bridge 1, i, at f = 20 kHz when  $C_{\rm S} = 4.5$  nF and  $T_{\rm DOpt} = 0.6$   $\mu \rm s$ . Fig. 3 (a) presents those at the rated-power (P = 100 kW) operation, where the waveform of  $v_1$  leads that of  $v_2$  by 26.6°. This means that power flow occurs from bridge 1 to bridge 2. The peak voltage appearing in the waveforms of  $v_1$  and  $v_2$  is lower than 950 V, which is within an acceptable level because of using the 1.2-kV SiC modules in Fig. 2. Fig. 3 (b) and Fig. 3(c) are in the cases of P = 30 kW and P = 10 kW, respectively.

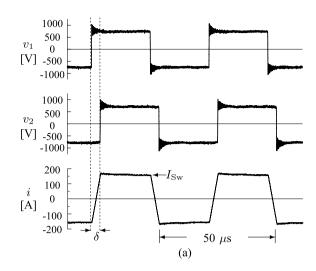
Fig. 4 plots overall conversion efficiencies  $\eta$ , calculated from (3), with operating frequencies of f=20 kHz and 10 kHz when  $C_{\rm S}=4.5$  nF and  $T_{\rm DOpt}=0.6$   $\mu s$ . The maximum conversion efficiency  $\eta_{\rm max}$  is 98.7% at P=42.0 kW, and the conversion efficiency at P=100 kW is 97.9% during the 20-kHz operation.

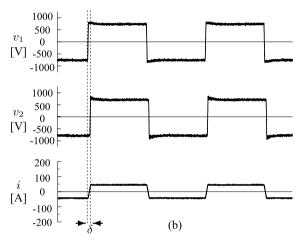
Fig. 5 plots overall power losses  $P_{\rm Loss}$  under the same conditions as those in Fig. 4. In the ZVS (zero-voltage-switching) region ranging from 20 to 100 kW, the power loss decreases as the output power decreases. In the incomplete-ZVS region ranging from 0 to 20 kW, however, the power loss increases as the output power decreases. This interesting trend comes from an increase in the "power loss" caused by incomplete ZVS.

Fig. 6 and Fig. 7 plot overall conversion efficiencies and overall power losses at f= 20 kHz and 10 kHz when  $C_{\rm S}$  = 9 nF and  $T_{\rm DOpt}$  = 0.8  $\mu$ s. The incomplete ZVS region expands into a range from 0 to 26 kW because the snubber capacitor is larger in capacitance value than that in Fig. 5. The overall power loss at P = 0 increases from 862 W in Fig. 5 to 1210 W in Fig. 7 because the snubber loss increases as the snubber capacitor  $C_{\rm S}$  becomes larger. On the other hand, the overall power loss at P = 100 kW decreases from 2136 W to 2027 W [19].

## B. Comparison With a DAB DC-DC Converter Using Four Si-IGBT/PND Dual Modules

TABLE II summarizes comparisons between the 750-Vdc, 100-kW, 20-kHz dc-dc converter using the 1.2-kV 400-A SiC-MOSFET/SBD dual modules [19] and the 750-Vdc, 60-kW, 4-kHz dc-dc converter using 1.2-kV 300-A Si-





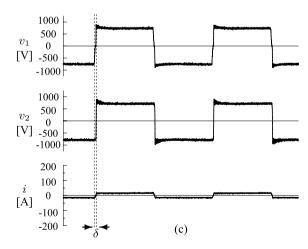


Fig. 3. Experimental waveforms when f=20 kHz,  $C_{\rm S}=4.5$  nF and  $T_{\rm Dopt}=0.6$  µs. (a) P=100 kW and  $\delta=26.6^{\circ}$ . (b) P=30 kW and  $\delta=7.0^{\circ}$ . (c) P=10 kW and  $\delta=1.5^{\circ}$ .

IGBT/PND dual modules [20]. The two power ratings are not the same because the Si module is different in current rating from the SiC module. Moreover, the two operating frequencies are not the same because it would be impractical to operate the dc-dc converter using the Si modules at 20 kHz in terms of increased switching loss. However, note that

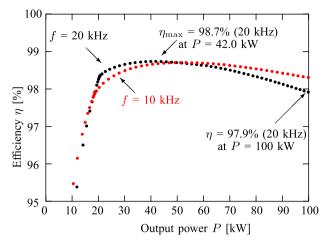


Fig. 4. Conversion efficiency when  $C_S = 4.5$  nF and  $T_D = 0.6$   $\mu$ s.

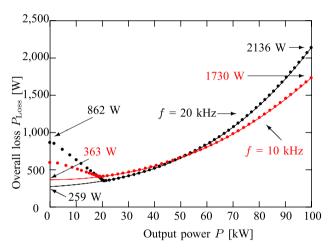


Fig. 5. Measured overall power loss when  $C_{\rm S} = 4.5$  nF and  $T_{\rm D} = 0.6$   $\mu s$ .

the SiC module adopts the same packaging in size, shape, and terminal/pin arrangement as the Si module does. A main reason for having the same packaging in appearance is to make it easy for power electronics engineers to replace the Si module with the SiC module.

TABLE II concludes that the use of the SiC modules makes the maximum efficiency higher by 0.9% and the rated-power efficiency higher by 1.0% than the use of the Si

TABLE II
COMPARISON BETWEEN THE TWO DAB DC-DC CONVERTERS
USING SIC-MOSFET/SBD AND SI-IGBT/PND MODULES.

Power module	1.2-kV, 400-A SiC-MOSFET/SBD	1.2-kV, 300-A Si-IGBT/PND
Power rating	100 kW	60 kW
Input/output voltage rating	750 Vdc	750 Vdc
Switching frequency	20 kHz	4 kHz
Snubber capacitor	4.5 nF	10 nF
Maximum efficiency	98.7%	97.8%
Rated power efficiency	97.9%	96.9%

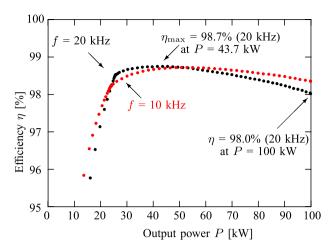


Fig. 6. Conversion efficiency when  $C_s = 9$  nF and  $T_D = 0.8 \mu s$ .

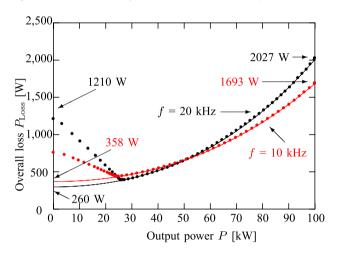


Fig. 7. Measured overall power loss when  $C_S = 9 \text{ nF}$  and  $T_D = 0.8 \mu\text{s}$ .

modules, although the switching frequency is increased from  $4\,\mathrm{kHz}$  to  $20\,\mathrm{kHz}$ .

# V. ELIMINATION OF TWO SBDs FROM EACH SIC-MOSFET DUAL MODULE

### A. Experimental System

Fig. 8 shows the experimental circuit configuration of the 750-Vdc, 100-kW, 20-kHz bidirectional isolated dc-dc converter using 1.2-kV 400-A SiC-MOSFET dual modules. Note that the MOSFET power chips designed and fabricated by Mitsubishi Electric were mounted on each dual module. This means that each module has no SBD integrated. TABLE III summarizes the circuit parameters used in the experimental system of Fig. 8. Carefully looking at TABLE I and TABLE III enables one to notice that small differences exist in a few parameters as a result of having tuned to the 1.2-kV 400-A SiC-MOSFET dual modules used in this experiment. Exactly speaking, the dual modules used for Fig. 2 and Fig. 8 are not the same in SiC-MOSFET chip although the dual modules are the same in voltage and current ratings,

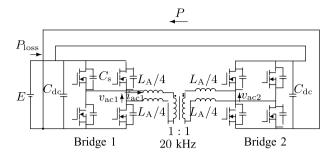


Fig. 8. Experimental circuit using four 1.2-kV 400-A SiC-MOSFET dual modules, each of which has no SBDs integrated.

TABLE III
CIRCUTT PARAMETERS OF THE EXPERIMENTAL
CIRCUIT SHOWN IN FIG. 8.

Power rating		100 kW
Input/output voltage rating	E	750 V dc
Switching frequency	f	20 kHz
Auxiliary inductor	$L_{A}$	16.6 μΗ
Leakage inductance	l	1 μΗ
Phase shift angle	δ	0 — ± 27.4°
Snubber capacitor	$C_{\rm s}$	4 nF
Dead time	$T_{\mathrm{D}}$	0.6 μs
Transformer core material		FINEMET*
Maximum flux density		0.48 T at 20 kHz
Transformer turns ratio		1:1

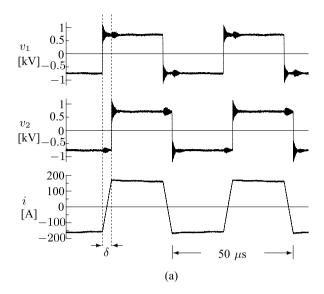
<sup>\*</sup>Nano-crystalline soft-magnetic materidal.

and the SiC-MOSFET chips are integrated into the same packaging in size, shape and terminal/pin arrangement.

### B. Experimental Waveforms

Fig. 9 shows experimental waveforms of the ac terminal voltages appearing across bridges 1 and 2,  $v_1$  and  $v_2$ , respectively, and the ac current flowing at the ac side of bridge 1, i, at f = 20 kHz when  $C_S = 4$  nF and  $T_D = 0.6$  µs. Fig. 9(a) presents those at the rated-power (P = 100 kW) operation, where the waveform of  $v_1$  leads that of  $v_2$  by 27.4°. This means that power flow occurs from bridge 1 to bridge 2. The peak voltage appearing in the waveforms of  $v_1$  and  $v_2$  is slightly higer than those in Fig. 2. However, it is still within an acceptable level. Fig. 9(b) is in the case of operation at 41 kW where the maximum conversion efficiency of 98.8% was achieved, whereas a conversion efficiency was 98.0% at 100 kW [21].

TABLE IV summarizes a comparison in conversion efficiency among four different bidirectional isolated DAB dcdc converters using Si-IGBT modules or SiC-MOSFET modules in the past, the present, and the near future. The next-generation trench-gate SiC-MOSFET modules in terms of structure and performance are under research and development. The combination of the next-generation SiC-MOSFET modules with new magnetic materials for high-frequency transformers and auxiliary inductors will make a



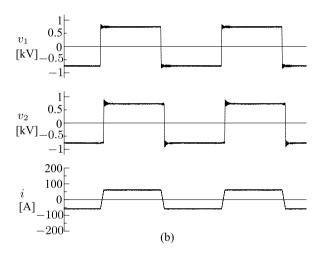


Fig. 9. Experimental waveforms of the ac terminal voltages of bridges 1 and 2,  $v_1$  and  $v_2$ , and the primary current of the transformer, *i*. (a) P = 100 kW (rated power) at  $\delta = 27.4^{\circ}$  and (b) P = 41 kW (maximum efficiency) at  $\delta = 11^{\circ}$ .

significant contribution to reducing the total power loss. As a result, the conversion efficiency of the 750-Vdc 100-kW 20-kHz dc-dc converter will reach higher than 99% in a broad output power range of 5 to 100 kW.

### VI. SERIES AND/OR PARALLEL CONNECTIONS OF BIDIRECTIONAL ISOLATED DAB DC-DC CONVERTERS

It is clear from the basic circuit configuration shown in Fig 1 that this DAB dc-dc converter has the capability of galvanic or electric isolation between the input terminals and the output terminals. This capability makes it easy to series and/or parallel connections of multiple DAB dc-dc converters, intended for expanding voltage and/or current ratings.

Fig. 10 to Fig. 12 show three possible circuit configurations making series and/or parallel connections of two DAB dc-dc converters. Fig. 10 shows the circuit configuration making parallel connections of both input terminals and

CONVERSION EFFICIENCY OF BIDIRECTIONAL ISOLATED DC-DC CONVERTERS: YESTERDAY, I ODAY, AND I OMORROW						
Year and Reference	1992 [2]	1992 [2] 2007 [4] 201		2016 [21] 2020?		
Power Switching Devices	Planar-Gate Si-IGBTs	Trench-Gate Si-IGBTs	Planar-Gate SiC-MOSFETs	Trench-Gate SiC-MOSFETs		
Rated Output Power and Switching Frequency	50 kW and 50 kHz	10 kW and 20 kHz	100 kW and 20 kHz	100 kW and 20 kHz		
Magentic Materials Used for Transformers	Ferrite	FINEMET	FINEMET	New Materials?		
Conversion Efficiency from DC Input to DC Output	Below 90%	96.8% at 10 kW 97.4% at 3.8 kW	98.0% at 100 kW 98.8% at 41 kW	Over 99%		

TABLE IV

The term "FINEMET" is a trade name that means a nano-crystalline soft-magnetic material.

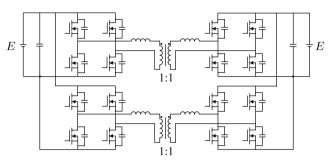


Fig. 10. Input-parallel output-parallel isolated dc-dc converter.

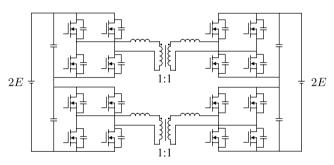


Fig. 11. Input-series output-series isolated dc-dc converter.

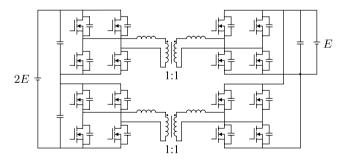


Fig. 12. Input-series output-parallel isolated dc-dc converter.

output terminals. This parallel connections make no circulating current flow between the two dc-dc converters. Therefore, no concern is provided to current sharing between the two.

Fig. 11 shows the circuit configuration making series connections of both input terminals and output terminals. Unlike the parallel connections shown in Fig. 10, the series connections take care of individual voltage balancing in either dc input terminals or dc output terminals although no attention is paid to current balancing.

Fig. 12 shows the circuit configuration making the series connection of the input terminals and the parallel connection of the output terminals. This configuration is so interesting that the dc voltage at the input terminals can be stepped down by half at the output terminals although all the SiC-MOSFET modules have the same voltage rating and the two transformers have unity turns ratio. Moreover, any concern is provided to neither current sharing nor voltage balancing.

#### VII. CONCLUSION

This paper has designed, built, and tested two 750-Vdc, 100-kW, 20-kHz bidirectional isolated dual-active-bridge (DAB) dc-dc converters using four 1.2-kV, 400-A SiC-MOSFET dual modules with or without SBDs. When the 1.2-kV, 400-A SiC-MOSFET dual modules without SBDs are used, the maximum conversion efficiency from the dcinput terminals to the dc-output terminals is as high as 98.8% at 41 kW, and 98.0% at 100 kW, which are calculated from the accurately-measured overall power loss excluding gatedrive and control circuit losses.

When the next-generation trench-gate SiC-MOSFET modules come across, the conversion efficiency of a welldesigned DAB dc-dc converter is expected to be higher than 99% in a broad power range, even at the rated power.

Series and/or parallel connections of multiple DAB dc-dc converters would make it easy to expand the voltage and/or current ratings as if the converter were operating as a single high-power DAB dc-dc converter. In particular, the inputseries and output-parallel connections show considerable promise as a dc-dc converter for medium-voltage highpower battery energy storage systems and an interface circuit between two dc power networks with different dc voltages.

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devices, and its reliability.

# Turn-On Oscillation Damping for Hybrid IGBT Modules

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Abstract-In a hybrid IGBT module with SiC diodes as free-wheeling diodes, high frequency oscillation occurs during turn-on due to the fast switching transient of SiC diode and the resonance between circuit parasitic inductances and the junction capacitance of SiC diode. Such oscillation causes EMI noise which may affect the performance of the system. Methods to mitigate the turn-on oscillation are studied. Firstly, the effect of gate drive parameters on turn-on oscillation is investigated with respect to different gate voltages and gate charging currents. Then a novel turn-on oscillation suppression method is proposed with combination of damping circuit and active gate driver. The proposed oscillation suppression method can achieve the lowest EMI noise while remaining the advantage of lower switching loss brought by SiC diodes. Detailed theoretical analysis of the turn-on oscillation is conducted, and experimental results are given to verify the effectiveness of the proposed oscillation suppression method.

Index terms—Hybrid IGBT module, SiC SBD, turn-on oscillation damping, active gate driver

### Nomenclature

$v_{CEI}$ , $v_{CE2}$ , $v_{CE}$	Collector-emitter voltage of the IGBT
$i_{CI}$ , $i_{C2}$ , $i_C$	Collector current of the IGBT
$v_{\mathit{GE}}$	Gate-emitter voltage of the IGBT
$i_{GI}$ , $i_{G2}$ , $i_{G}$	Gate current of the IGBT
$V_G$	Gate voltage provided by the voltage source gate drive circuit
V <sub>+</sub> , V <sub>-</sub>	High and low level voltages of the voltage source gate driver
$I_G$	Gate current of IGBT provided by the current source gate driver
$V_{DC}$	DC bus voltage
$I_L$	Load current of the inductive switching
	test
$R_{g,int}$	Internal gate resistance of IGBT module
$R_{g,ext}$	External gate resistance of IGBT module

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$C_S$	Capacitance of the RC damping circuit
$R_S$	Resistqance of the RC damping circuit
$v_{Cs}$	Voltage of the damping capacitor
$i_S$	Current flowing though the RC damping
	circuit
$i_{dc}$	DC bus current
$I_{OSC\ MAX}$	Maximum oscillation current
$t_s$	Settling time of oscillation
$L_p$	Stray inductance of the DC bus bar
$L_{IC}$ , $L_{IeE}$ , $L_{IE}$ , $L_{2C}$	, $L_{2eE}$ , $L_{2E}$
	Stray inductances in the IGBT module
$L_m = L_{IC} + L_{IeE} + L_{II}$	$_{E}$ + $L_{2C}$ + $L_{2eE}$ + $L_{2E}$
	Lumped stray inductance of the IGBT
	module
$R_p$	Parasitic resistance of the commutation
1	loop
$C_{CEI}$ , $C_{CE2}$	Combination of the collector-emitter
	capacitance of IGBT and junction capaci-
	tance of the anti-parallel SiC SBD
$C_{GEI}$ , $C_{CGI}$ , $C_{GE2}$ ,	$C_{CG2}$
	Gate-emitter and collector-gate capa-
	citances of the IGBT
$g_{\it fe}$	Transconductance of the IGBT
$g_{fe} \ E_{on}$	Turn-on energy loss of the IGBT
$E_{\it damp,on}$ , $E_{\it damp,off}$	Loss in the damping resistor during turn-

#### I. Introduction

on and turn-off

**T**OW to reduce power semiconductor device losses Taseems to be a permanent topic in power electronics world. In recent years, SiC devices have attracted more and more attention due to their superior characteristics. Since the reverse recovery loss of free-wheeling diode has a big share of the total switching loss of all-Si IGBT module, hybrid IGBT modules occurs by replacing the Si free-wheeling diodes with SiC schottky barrier diodes (SiC SBDs) [1]-[3]. Hybrid IGBT module has eliminated the diode reverse recovery process so that the IGBT turn-on loss and diode reverse recovery loss are largely reduced. It is a promising solution with the optimization of both performance and cost. However, although diode reverse recovery process is eliminated by using SiC SBD, the effects caused by junction capacitance are still present. Since the drift layer of a SiC SBD is thinner than Si diode, with the same chip area, the junction capacitance of SiC SBD is larger than Si diode [4]. Due to the extremely fast recovery process of SiC SBD and the resonance between the junction capacitance of SiC

SBD and the circuit parasitic inductances, high frequency oscillation occurs during the turn-on process of hybrid IGBT module. This problem has been found by previous researchers as reported in [1]. In [5], the conducted EMI noise in a Boost converter utilizing SiC diode is evaluated. It is shown that compared to Si diode, the Boost converter with SiC SBD has larger conducted noise in the high frequency range caused by the oscillations in the SiC SBD. Fig. 1 shows the turn-on waveforms under 500 V DC bus voltage and 100 A load current. Fig. 1(a) is the result of a hybrid IGBT module while Fig. 1(b) is the result of a traditional all-Si IGBT module, where  $v_{CE}$  is the collector-emitter voltage, iC is the collector current and  $v_{GE}$  is the gate-emitter voltage, respectively. The reverse recovery current is significantly reduced in the hybrid IGBT module. However, a high frequency oscillation occurs in the collector current of IGBT during turn-on process. It may cause EMI problems affecting the operation of other systems [1].

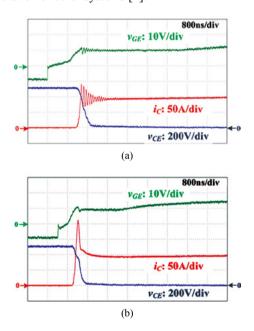


Fig. 1. Turn-on waveforms of (a) Hybrid IGBT module and (b) All-Si IGBT module

It is natural to consider about improving the gate driver to damp this turn-on oscillation. Previous studies have considered using active gate driver to solve the EMI issues related to di/dt and dv/dt and the current and voltage overshoots that may affect the safe operation of IGBT module [6]-[22]. Applying the active gate driver solutions, the collector current overshoot during the turn-on interval of an IGBT can be reduced by steering the current slew rate. Meanwhile, by accelerating the other stages the total turn-on time and loss would not increase significantly. In [20], a method of optimizing the gate resistance of the low side switch is proposed to accelerate the damping of the phase node ringing in a synchronous Buck converter. A simplified RLC model is developed to study the relation between the phase node ringing and circuit parasitics. In

[21], a gate charge control method is studied to suppress the turn-off voltage oscillation of SiC MOSFET. However the effectiveness of active gate driver on suppressing the high frequency turn-on oscillations of hybrid IGBT modules has not been fully analytically and experimentally discussed which will be one of the purposes of this paper.

Another possible solution for the oscillations is the application of additional damping circuits. As illustrated in [23], RC and RCD snubber networks are effective in suppressing the voltage overshoot during IGBT turn-off and the diode voltage spike during IGBT turn-on (free-wheeling diode turn-off). In [24], RC snubbers are parallel connected to SiC MOSFETs to mitigate the dv/dt and voltage oscillation during turn-off. In [25], SiC PiN diodes are used with Si IGBTs in a Buck converter. The oscillations during diode turn-off (IGBT turn-on) are studied. To mitigate the oscillations, an RC circuit is parallel connected to the SiC PiN diode. The added capacitor charges and discharges in every switching cycle, causing a regardless amount of extra loss. In [26], methods to damp the switching oscillations of normally-off SiC JFET are studied. An RC circuit is used across the DC bus, and the values of the resistor and capacitor are experimentally adjusted to reach the most satisfied performance. In [27], SiC SBD and SiC MOSFET are used in a double pulse switching test circuit, and the turn-on and turn-off oscillations are analyzed. A similar RLC model as in [21] is derived to analyze the oscillation effects. RC snubbers are used to bring the system into overdamped condition so that oscillations can be mitigated. However, the side-effects such as the extra loss caused by the RC snubber circuit are not evaluated. It is still unclear whether the snubber circuit is effective in mitigating the turn-on oscillation of hybrid IGBT module without causing significant side-effects. Therefore, it is one of the objectives of this paper to find the appropriate structure and design of the damping circuit which can effectively suppress the turnon oscillation of hybrid IGBT module without causing large increases in current overshoot and switching losses.

In this paper, a turn-on oscillation suppression method is proposed with combination of damping circuit and active gate driver. First to evaluate the influences of active gate driving on turn-on oscillation, different gate voltages and gate charging currents are used. It is found that by changing gate drive parameters the current overshoot can be reduced, however the duration of oscillation cannot be shortened. To accelerate the damping of turn-on oscillation, oscillation damping circuits are studied. The detailed theoretical analysis of the damping circuit is given to illustrate the optimized design of damping circuit parameters. Then the experimental results of the damping circuit are given to verify its effectiveness in accelerating the damping of turnon oscillation and to validate the theoretical analysis. At last, to suppress the turn-on current overshoot, active gate driver method is used without largely increasing the turn-on energy loss. The combination of damping circuit and active gate driver makes it possible to simultaneously realize turnon current overshoot suppression and turn-on oscillation damping, which will be an optimized solution to achieve the desired low EMI performance.

# II. Influences of Gate Driver on Turn-On Oscillation

To study the gate drive controllability of turn-on current oscillation in hybrid IGBT module (Fuji Electric: 400 A/1700 V, 2MSI400VE-170-50), experimental research on the influence of gate driver is carried out. Basically IGBT gate drivers can be divided into two categories: voltage source gate driver and current source gate driver. Therefore, by analyzing the performances of different voltage source and current source gate drivers, the influence of gate drive parameters on turn-on oscillation can be evaluated.

### A. Voltage Source Gate Drive

First, turn-on characteristics of the hybrid IGBT module are tested using the voltage source gate driver with different positive gate drive voltages. The tests are done in a doublepulse test circuit shown in Fig. 2 with 550 V DC bus voltage and 200 A load current, the external gate resistance used is 10  $\Omega$ . In Fig. 2,  $V_{DC}$  is the DC bus voltage,  $I_L$  is the current of the load inductor at the turn-on event, ic is the collector current of the lower arm IGBT,  $R_{G ext}$  is the externally connected gate resistor,  $v_G$  is the gate voltage provided by the gate drive circuit and  $v_{GE}$  is the gate-emitter voltage measured at the terminals of the module. The positive gate voltage of  $v_G$  provided by the gate driver is denoted as  $V_+$ . The turn-on waveforms under different positive gate voltages  $(V_{+})$  are shown in Fig. 3. The maximum oscillation current  $I_{OSC\ MAX}$  and the oscillation settling time  $t_s$  are measured as shown in Fig. 4 (a) and (b). The maximum oscillation current  $I_{OSC\ MAX}$  is the maximum current overshoot exceeding the load current as shown in Fig. 3. The oscillation settling time  $t_{\rm s}$ , which is the time for the amplitude of oscillation current to drop from  $I_{OSC\ MAX}$  to 5%• $I_{OSC\ MAX}$ , represents the duration of oscillation.

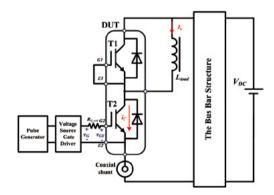


Fig. 2. Test setup for turn-on characteristics under different gate voltages.

It can be seen from the test results that when the applied gate voltage is reduced from 17 V to 11 V, the maximum oscillation current decreases from 87.3 A to 47 A, however

the oscillation settling time fluctuates around 1200 ns with no clear link with the applied gate voltage.

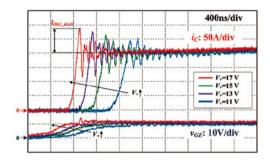


Fig. 3. Turn-on waveforms under different voltage source gate drivers.

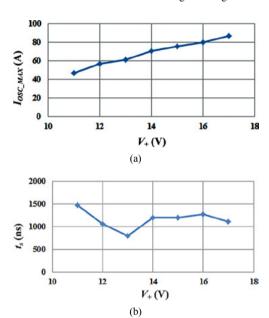


Fig. 4. Turn-on current oscillation under different gate voltages: (a) Maximum oscillation current; (b) Oscillation settling time.

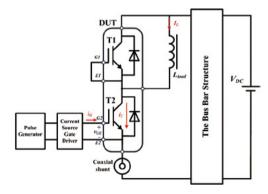


Fig. 5. Test setup for turn-on characteristics under different gate currents.

### B. Current Source Gate Drive

Then a current source gate driver is used to study the turnon characteristics under different gate charging currents. The test setup is shown in Fig. 5 with 550 V DC bus voltage and 200 A load current. In Fig. 5,  $i_G$  is the gate current provided by the current source gate driver while all the other variables have the same definitions as in Fig. 2. During a turn-on interval, a constant gate charging current IG is provided by the current source gate driver. The turn-on waveforms under different gate charging currents ( $I_G$ ) are shown in Fig. 6. Similarly, the maximum oscillation current  $I_{OSC\_MAX}$  and the oscillation settling time  $t_s$  are measured as shown in Fig. 7 (a) and (b).

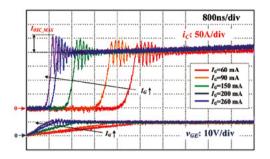
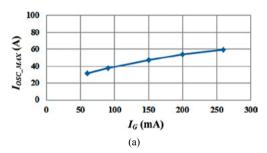


Fig. 6. Turn-on waveforms under different current source gate drivers.



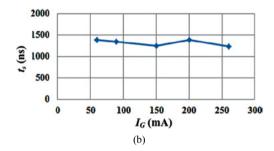


Fig. 7. Turn-on current oscillation under different gate currents: (a) Maximum oscillation current; (b) Oscillation settling time.

It can be seen that when the gate charging current changes from 260 mA to 60 mA, the maximum oscillation current decreases from 59.3 A to 31.7 A, however the oscillation settling time fluctuates around 1200 ns and does not have a clear relation with the gate charging current.

To sum up, by lowering the gate voltage and reducing gate charging current, the maximum oscillation current can be mitigated but the switching speed will be reduced and the on-state voltage drop will increase, thus causing increase in switching and conduction losses. Moreover, the attenuation of the oscillation cannot be accelerated by changing the gate drive parameters alone. Therefore, lowering gate voltage and reducing gate charge current are not the recommended methods to suppress turn-on oscillation. To accelerate the damping of turn-on oscillation, further countermeasures

should be taken.

## III. TURN-ON OSCILLATION SUPPRESSION WITH DAMPING CIRCUIT

### A. Theoretical Analysis of Turn-on Oscillation

To accelerate the damping of turn-on oscillation, the utilization of additional damping circuits is investigated. To have a better understanding of turn-on oscillation, first the theoretical analysis of the oscillation is carried out to reveal the relation between turn-on oscillation and circuit parasitics. The inductive switching test circuit is shown in Fig. 8 where the lower arm IGBT is switching and the upper arm SiC SBD is the free-wheeling diode. As depicted in Fig. 8,  $L_n$  represents the stray inductance of the DC bus,  $R_n$  stands for the parasitic resistance of the commutation loop,  $L_{IC}$ ,  $L_{IeE}$ ,  $L_{IE}$ ,  $L_{2C}$ ,  $L_{2eE}$ ,  $L_{2E}$  are the stray inductances in the hybrid IGBT module,  $C_{CEI}$  and  $C_{CE2}$  are the combination of the collector-emitter capacitance of the IGBT and the junction capacitance of the anti-parallel SiC SBD,  $C_{GEI}$ ,  $C_{CGI}$ ,  $C_{GE2}$ ,  $C_{CG}$  are the gate-emitter and collector-gate capacitances of the IGBT, Rg,ext and Rg,int are the external and internal gate resistors of the IGBT respectively. In the figure,  $V_{DC}$  is the DC bus voltage,  $I_L$  is the load current,  $i_{dc}$  is the DC bus current,  $i_{CI}$  and  $i_{C2}$  are the collector currents of the upper arm and lower arm devices respectively,  $v_{CEI}$  and  $v_{CE2}$  are the collector-emitter voltages of upper arm and lower arm devices respectively, and  $v_{GE2}$ ,  $v_{CG2}$ ,  $i_{G2}$  are the gate-emitter voltage, collector-gate voltage and the gate current of the lower arm IGBT.

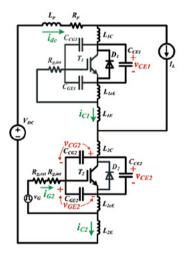


Fig. 8. Inductive switching circuit of hybrid IGBT module

The conceptual waveforms of a turn-on event of the lower arm IGBT T2 are shown in Fig. 9, where  $V_{GE, \text{th}}$  is the gate threshold voltage,  $V_{GE, \text{miller}}$  is the miller plateau voltage.

The parasitic capacitances of the IGBT are highly nonlinear depending on the collector-emitter voltage. To simplify the analysis, the similar approximation as in [28] is adopted that the capacitances are approximated as two discrete values in different operating regions. The output characteristic of

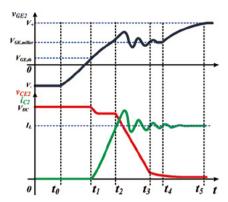


Fig. 9. Conceptual turn-on waveforms of the hybrid IGBT module.

the IGBT can be divided into three regions: cut-off region, linear region and saturation region. The capacitances in each operating region are shown in TABLE I where  $C_{\text{CE},L} << C_{\text{CE},H}$  and  $C_{\text{CG},L} << C_{\text{CG},H}$ .

 $\begin{array}{c} \text{TABLE I} \\ \text{Operating Regions and Parasitic Capacitances of the} \\ \text{IGBT} \end{array}$ 

Time interval	$t_0 \sim t_1$	$t_1 \sim t_2$	<i>t</i> <sub>2</sub> ~ <i>t</i> <sub>3</sub>	<i>t</i> <sub>3</sub> ~ <i>t</i> <sub>4</sub>	<i>t</i> <sub>4</sub> ~ <i>t</i> <sub>5</sub>
Operating region of T2	Cut-off	Linear	Linear	Linear	Saturation
$C_{CE2}$	$C_{\mathit{CE},L}$	$C_{\mathit{CE},L}$	$C_{\mathit{CE},L}$	$C_{\mathit{CE},H}$	$C_{\mathit{CE},H}$
$C_{cG2}$	$C_{CG,L}$	$C_{CG,L}$	$C_{CG,L}$	$C_{CG,H}$	$C_{CG,H}$
$C_{CE1}$	$C_{\text{CE,H}}$	$C_{\mathit{CE},H}$	$C_{\mathit{CE},H}$	$C_{\scriptscriptstyle{CE,L}}$	$C_{\mathit{CE},L}$

As shown in Fig. 9, the turn-on interval can be roughly divided into five stages:

• Stage 1 ( $t_0 \sim t_1$ ): turn-on delay time

Gate-emitter voltage  $v_{GE2}$  rises from the negative gate potential V- and reaches the threshold voltage  $V_{GE,th}$  at  $t_l$ . The IGBT operates in cut-off region in this stage.

• Stage 2  $(t_1 \sim t_2)$ : collector current rising stage

After  $t_I$ , the collector current  $i_{C2}$  begins to rise and reaches the load current  $I_L$  at  $t_2$ . The IGBT operates in linear region in this stage.

• Stage 3 ( $t_2 \sim t_3$ ): collector-emitter voltage dropping stage

After  $t_2$ , the upper arm diode begins to take up voltage, and the collector-emitter voltage of the lower arm IGBT  $v_{CE2}$  begins to drop at a high slew rate and reaches a certain level at  $t_3$ . The IGBT operates in linear region in this stage.

The value of the collector-emitter voltage at the stage transition needs some more insight into the device physical model, as discussed in [29]. Since the physical modeling of IGBT is not the focus of this study, the value of  $v_{CE2}$  at stage transition is approximated from the test waveforms.

• Stage 4 ( $t_3 \sim t_4$ ): collector-emitter voltage dropping stage

After  $t_3$ , the collector-gate capacitance  $C_{CG}$  of the IGBT increases to a much larger value so the slew rate of  $v_{CE2}$  decreases dramatically. At  $t_4$ ,  $v_{CE2}$  drops to the on-state voltage, and the IGBT enters saturation region. The IGBT

operates in linear region in this stage.

For the sake of simplicity, the on-state voltage drop is approximated as 0 in this analysis.

• Stage 5 ( $t_4 \sim t_5$ ): gate-emitter voltage rises to positive supply voltage

After  $t_4$ , the gate-emitter voltage  $v_{GE2}$  starts to rise again and reaches the positive gate potential  $V_+$  at  $t_5$ . The IGBT operates in saturation region in this stage.

The detailed analytical expressions of each stage are presented as follows.

Stage 1  $(t_0 \sim t_1)$  - turn-on delay time:

At  $t_0$ , the voltage  $v_G$  provided by the gate driver jumps from  $V_1$  to  $V_+$ . The input capacitance starts to charge up. The gate-emitter voltage  $v_{GE2}$  in this stage can be expressed as:

$$v_{GE2}(t) = V_{+} \cdot \left[1 - e^{-(t-t_0)/\tau_{ies}}\right] - V_{-}$$
 (1)

where  $\tau_{ies} = R_g \cdot (C_{GE2} + C_{CG2}) = R_g \cdot (C_{GE} + C_{CG,L}), R_g = R_{g,ext} + R_{g,int}$ .

In this stage, the collector current  $i_{C2}$  remains at 0, and the collector-emitter voltage  $v_{CE2}$  remains at  $V_{DC}$ . At  $t_l$ ,  $v_{GE}$  reaches  $V_{GE}$ , th and the IGBT enters Stage 2.

Stage 2  $(t_1 \sim t_2)$  - collector current rising:

In this stage, the collector current  $i_{C2}$  begins to rise. Free-wheeling diode D1 still conducts part of the load current, so the voltage  $v_{CEI}$  remains at 0 in this stage.

The initial conditions of this stage are listed below:

$$\begin{cases} i_{C2}(t_1) = 0 \\ v_{GE2}(t_1) = V_{GE,th} \\ v_{CE2}(t_1) = V_{DC} \end{cases}$$
 (2)

As the IGBT is operating in the linear region, the collector current can be expressed with the following equation:

$$i_{C2}(t) = g_{fe}[v_{GE2}(t) - V_{GE,th}]$$
 (3)

where gfe is the transconductance of the IGBT. Note that in this stage the collector-emitter voltage is not changing abruptly, thus the current flowing through the output capacitance is neglected in equation (3).

For the gate loop, the following equations can be derived:

$$R_g \cdot i_{G2}(t) = V_+ - v_{GE2}(t) - L_{eE2} \frac{di_{C2}(t)}{dt}$$
 (4)

$$i_{G2}(t) = C_{GE} \frac{dv_{GE2}(t)}{dt} - C_{CG,L} \frac{dv_{CG2}(t)}{dt}$$
 (5)

$$v_{GE2}(t) = v_{CE2}(t) - v_{CG2}(t)$$
 (6)

For the main power loop, the following equation can be obtained:

$$V_{DC} = (L_p + L_m) \frac{di_{C2}(t)}{dt} + R_p \cdot i_{C2}(t) + v_{CE2}(t)$$
 (7)

where  $L_m(=L_{IC}+L_{IeE}+L_{IE}+L_{2C}+L_{2eE}+L_{2E})$  represents the stray inductance within the hybrid module.

Combining equations (3)-(7),  $i_{C2}(t_2)$ ,  $v_{GE2}(t_2)$  and  $v_{CE2}(t_2)$  can be derived which are the initial conditions of the next stage.

Stage 3  $(t_2 \sim t_3)$  – collector-emitter voltage dropping 1:

When the collector current  $i_{C2}$  reaches the load current  $I_L$  at  $t_2$  shown in Fig. 9, the upper arm diode D1 starts to take up voltage, so the collector-emitter voltage of the lower arm IGBT  $v_{CE2}$  begins to drop, and the collector current starts to oscillate

The initial conditions of this stage are listed as below:

$$\begin{cases} i_{C2}(t_2) = I_L \\ v_{GE2}(t_2) = I_L/g_{fe} + V_{GE,th} \\ v_{CE2}(t_2) & \text{derived from the last stage} \\ v_{CE1}(t_2) = 0 \end{cases}$$
(8)

For the main power loop, the following equations can be derived:

$$V_{DC} = L_{p} \frac{di_{cc}(t)}{dt} + R_{p}i_{dc}(t) + (L_{1C} + L_{1E} + L_{1eE}) \frac{di_{C1}(t)}{dt} + v_{CE1}(t) + (L_{2C} + L_{2E} + L_{2eE}) \frac{di_{C2}(t)}{dt} + v_{CE2}(t)$$
(9)

$$i_{dc}(t) = i_{C2}(t)$$
 (10)

$$i_{C1}(t) = i_{C2}(t) - I_L$$
 (11)

Combining with equations (10) and (11), equation (9) can be simplified as:

$$V_{DC} = \left(L_p + L_m\right) \frac{di_{C2}(t)}{dt} + R_p i_{C2}(t) + \nu_{CE1}(t) + \nu_{CE2}(t)$$
 (12)

For the upper arm IGBT T1, the following equation can be obtained:

$$C_{CE,H} \frac{dv_{CE1}(t)}{dt} = i_{C1}(t) = i_{C2}(t) - I_L$$
 (13)

For the gate loop, equations (4)-(6) are still valid in this stage. Since the collector-emitter voltage drops rapidly in this stage, the current flowing through the output capacitance of the IGBT cannot be neglected. Therefore, equation (3) has to be modified as the following equation:

$$i_{C2}(t) = g_{fe} \left[ v_{GE2}(t) - V_{GE,th} \right] + C_{CE,L} \cdot \frac{dv_{CE2}(t)}{dt} + C_{CG,L} \cdot \frac{dv_{CG2}(t)}{dt}$$
(14)

Combining equations (4)-(6) and (12)-(14), the current and voltages of this stage can be derived. As mentioned

before, the value of  $v_{CE2}$  at stage transition is approximated from the test waveforms. When  $v_{CE2}$  drops to the transition voltage, the IGBT enters the next stage.

Stage 4  $(t_3 \sim t_4)$  – collector-emitter voltage dropping 2:

The initial conditions ( $i_{C2}(t_3)$ ,  $v_{GE2}(t_3)$ ,  $v_{CEI}(t_3)$  and  $v_{CE2}(t_3)$ ) of this stage can be obtained by solving the equations describing the last stage. Since the circuit status in this stage is the same as last stage, equations (4)-(6) and (12)-(14) are still valid in this stage with only the changes in parasitic capacitances. The capacitances in (5) and (14) change from  $C_{CE,L}$ ,  $C_{CG,L}$  to  $C_{CE,H}$ ,  $C_{CG,H}$ . The capacitance in (13) changes from  $C_{CE,H}$  to  $C_{CE,L}$ .

At  $t_4$ , the collector-emitter voltage  $v_{CE2}$  drops to the onstate voltage, and the IGBT enters the saturation region. For the sake of simplicity, the on-state voltage drop is approximated as 0 in this analysis.

Stage 5  $(t_4 \sim t_5)$  – gate-emitter voltage rises to positive supply voltage:

After  $t_5$ , the IGBT enters saturation region. The gateemitter voltage begins to charge up again, and reaches the positive gate potential  $V_+$  at the end of this stage.

Equation (14) is no longer valid in this stage since the IGBT enters the saturation region. While all the other equations describing the last stage can still be used in this stage.

According to the device datasheet and some preliminary test waveforms, the parasitic parameters of the module are estimated as  $L_m$ =15 nH,  $L_{eE}$ =1 nH,  $C_{GE}$ =15 nF,  $C_{CG,L}$ =0.05 nF,  $C_{CG,H}$ =9 nF,  $R_p$ =0.4  $\Omega$ ,  $g_{fe}$ =200. In the calculations, the DC bus voltage is  $V_{DC}$ =550 V, the load current is  $I_L$ =200 A, the positive gate voltage is  $V_+$ =15 V and the gate resistance used is  $R_g$ = $R_{g,int}$ + $R_{g,ext}$ =15  $\Omega$ . For the sake of simplicity, the collector-emitter capacitance of the IGBT in combination with the junction capacitance of SiC SBD is approximated as a constant value  $C_{CE}$ .

The maximum oscillation current  $I_{OSC\_MAX}$  and oscillation settling time ts under different DC bus stray inductance  $L_p$  and device parasitic capacitance  $C_{CE}$  are calculated using the equations given above and the results are shown in Fig. 10 (a) and (b) respectively.

As shown in Fig. 10, with the increase of DC bus stray inductance, both the maximum oscillation current and oscillation settling time increases significantly. At a fixed stray inductance, with the increase of parasitic capacitance  $C_{CE}$ , the maximum oscillation current increases rapidly while the changes in the settling time of oscillation is not significant.

To evaluate the accuracy of the calculations, as shown in Fig. 11, the calculated maximum oscillation current and oscillation settling time are depicted alongside the tested results shown in Fig. 4 (a) and (b). Different positive gate potentials are used, and the parasitics parameters used for the calculations are:  $L_p$ =70 nH and  $C_{CE}$ =6 nF.

As shown in Fig. 11, the analytical model introduced in this paper is able to provide a relatively accurate estimation of turn-on oscillation of hybrid IGBT modules.

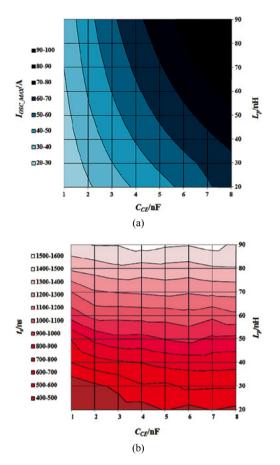


Fig. 10. Calculated results of current oscillation under different circuit parasitics: (a) Maximum oscillation current; (b) Oscillation settling time.

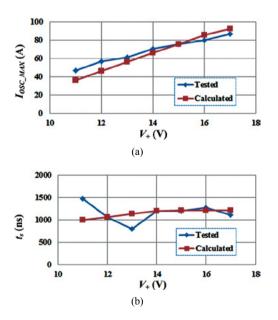


Fig. 11. Comparison between the calculated and tested current oscillation characteristics under different gate voltages:

(a) Maximum oscillation current; (b) Oscillation settling time.

Note from Fig. 11 (b) that some deviations from the theoretical values are present in the experimental oscillation settling time characteristics. The noise and inaccuracy in

the test system may be the cause of the fluctuations in the test results. The deviations from the theoretical values are in the range of several hundred nanoseconds which is just a few oscillation cycles. However, the trend in the figure still shows that the oscillation settling time is not clearly relevant with the gate voltage. Therefore, the faster attenuation of turn-on oscillation cannot be achieved by modifying the gate driver alone.

### B. Theoretical Analysis of Damping Circuit

RC and RCD networks have previously been used on Si and SiC power devices to mitigate the turn-off voltage overshoot and oscillations caused by circuit parasitics [23]-[27], [30]-[33]. The RC damping circuit may also be able to mitigate the turn-on current oscillations of hybrid IGBT module. However, since the primary purpose of the damping circuit is to mitigate the turn-on oscillation, the design and working principles of the damping circuit is different from the snubber circuit which is primarily aimed at suppressing the turn-off voltage overshoot. Two typical damping circuits are shown in Fig. 12 (a) and (b) respectively.

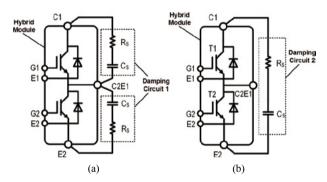


Fig. 12. Typical damping circuit topologies: (a) Damping circuit 1; (b) Damping circuit 2.

The damping circuit provides a conducting path for high frequency currents during the turn-on process, and the damping resistor damps the high frequency components of the current. The damping capacitor and resistor should be carefully chosen to achieve the best trade-off between oscillation damping and extra energy loss caused in the damping circuit.

A theoretical analysis is conducted for damping circuit 2 to illustrate the influence of damping circuit parameters on the performance of oscillation damping and additional switching loss. The inductive switching test circuit with the application of damping circuit is shown in Fig. 13. The damping circuit should be placed closely to the module and the connections are kept as short as possible to minimize the loop stray inductance, thus, for the sake of simplicity, the stray inductance of the damping circuit is not included in the circuit diagram.

The conceptual waveforms and the stages of the turnon interval are the same as demonstrated in the last section, which will not be repeated here. The detailed analytical

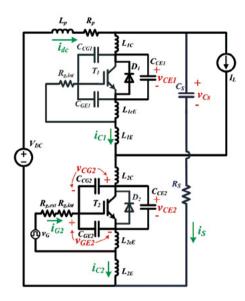


Fig. 13. Inductive switching circuit of hybrid IGBT module with damping circuit.

expressions of each stage with the presence of damping circuit are presented as follows.

Stage 1  $(t_0 \sim t_1)$  – turn-on delay time:

The expressions of this stage are the same with those without damping circuit and will not be repeated here.

Stage 2  $(t_1 \sim t_2)$  – collector current rising:

The initial conditions of this stage are listed below:

$$\begin{cases} i_{C2}(t_1) = 0 \\ v_{GE2}(t_1) = V_{GE,th} \\ v_{CE2}(t_1) = V_{DC} \\ v_{Cs}(t_1) = V_{DC} \\ i_{dc}(t_1) = 0 \end{cases}$$
(15)

For the gate loop, equations (3)-(6) are still valid with the presence of damping circuit.

For the main power loop, the following equations can be derived:

$$V_{DC} = L_{m} \frac{di_{C2}(t)}{dt} + L_{p} \frac{di_{dc}(t)}{dt} + R_{p} \cdot i_{dc}(t) + v_{CE2}(t)$$
 (16)

$$V_{DC} = v_{Cs}(t) + R_s C_s \frac{dv_{Cs}(t)}{dt} + L_p \frac{di_{dc}(t)}{dt} + R_p i_{dc}(t)$$
 (17)

$$i_{dc}(t) = i_{C2}(t) + C_S \frac{dv_{Cs}}{dt}$$
 (18)

Solving equations (3)-(6) and (16)-(18),  $i_{C2}(t_2)$ ,  $v_{GE2}(t_2)$ ,  $v_{CE2}(t_2)$ ,  $v_{CS}(t_2)$  and  $i_{dc}(t_2)$  can be derived which are the initial conditions of the next stage.

Stage 3  $(t_2 \sim t_3)$  – collector-emitter voltage dropping 1: The initial conditions of this stage are listed as below:

$$i_{C2}(t_2) = I_L$$

$$v_{GE2}(t_2) = I_L/g_{fe} + V_{GE,th}$$

$$v_{CE1}(t_2) = 0$$

$$v_{CE2}(t_2) \text{ derived from the last stage}$$

$$v_{Cs}(t_2) \text{ derived from the last stage}$$

$$i_{ds}(t_2) \text{ derived from the last stage}$$

For the main power loop, equations (17) and (18) are still valid in this stage, while equation (16) should be modified as:

$$V_{DC} = L_m \frac{di_{C2}(t)}{dt} + L_p \frac{di_{dc}(t)}{dt} + R_p \cdot i_{dc}(t) + v_{CE1}(t) + v_{CE2}(t)$$
(20)

For the upper arm IGBT T1, equation (13) still holds with the presence of damping circuit.

For the gate loop, equations (4)-(6) and (14) can still be used here.

Combining equations (4)-(6), (13), (14) and (20), the current and voltages of this stage can be derived. When the collector-emitter voltage drops to a certain level, the IGBT enters the next stage.

Stage 4  $(t_3 \sim t_4)$  – collector-emitter voltage dropping 2:

The initial conditions  $(i_{C2}(t_3), v_{GE2}(t_3), v_{CE1}(t_3), v_{CE2}(t_3), v_{CS}(t_2)$  and  $i_{dc}(t_2)$ ) of this stage can be obtained by solving the equations describing the last stage. Since the circuit status is the same as last stage, equations (4)-(6), (13), (14) and (20) are still valid in this stage with only the changes in parasitic capacitances. The capacitances in (5) and (14) changes from  $C_{CE,L}$ ,  $C_{CG,L}$  to  $C_{CE,H}$ ,  $C_{CG,H}$ , respectively. The capacitance in (13) changes from  $C_{CE,L}$  to  $C_{CE,L}$ 

Stage 5  $(t_4 \sim t_5)$  – gate-emitter voltage rises to positive supply voltage:

After  $t_5$ , the IGBT enters saturation region. The gateemitter voltage begins to charge up again, and reaches the positive gate potential  $V_+$  at the end of this stage.

Equation (14) is no longer valid in this stage since the IGBT enters the saturation region. While all the other equations describing the last stage can still be used in this stage.

According to the device datasheet and preliminary test results, the parasitic parameters of the module and the test circuit are estimated as:  $L_p$ =70 nH,  $L_m$ =15 nH,  $L_{eE}$ =1 nH,  $C_{GE}$ =15 nF,  $C_{CG,L}$ =0.05 nF,  $C_{CG,H}$ =9 nF,  $C_{CE}$ = 6nF  $R_p$ =0.4  $\Omega$ ,  $g_{fe}$ =200. In the calculations, the DC bus voltage is  $V_{DC}$ =550 V, the load current is  $I_L$ =200 A, the positive gate voltage is  $V_+$ =14 V and the gate resistance used is  $R_g$ = $R_{g,int}$ + $R_{g,ext}$ =15  $\Omega$ .

The maximum oscillation current  $I_{OSC\_MAX}$  and oscillation settling time ts are the most concerned parameters of the oscillation. The calculated maximum oscillation current  $I_{OSC\_MAX}$  and oscillation settling time ts under different damping resistors and damping capacitors are shown in Fig. 14 (a) and (b) respectively. The additional energy loss caused in the damping resistor during a turn-on event is also calculated,

as shown in Fig. 14 (c). To evaluate the loss in the damping resistor during turn-off of the IGBT, a similar analysis of the turn-off interval is carried out as well, and the calculated damping resistor loss during a turn-off event is shown in Fig. 14 (d).

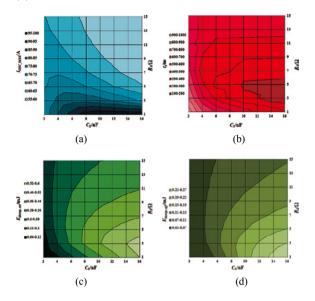


Fig. 14. Calculated results under different damping circuit parameters:
(a) Maximum oscillation current; (b) Oscillation settling time;
(c) Energy loss in the damping resistor during turn-on; (d) Energy loss in the damping resistor during turn-off.

It can be seen from the calculation results that the maximum oscillation current decreases with increasing  $C_S$  and  $R_S$ , however when  $R_S$  is larger than 5  $\Omega$ , the maximum oscillation current is only slightly influenced by  $C_S$  and  $R_S$ . The oscillation settling time represents the time for the damping circuit to attenuate the oscillation. The minimum value of oscillation settling time  $t_S$  occurs when  $C_S$ =10~16 nF, and  $R_S$ =3~5  $\Omega$  under the given conditions. The additional energy loss in the damping resistor increases with larger damping capacitor  $C_S$ , however both the additional energy losses during turn-on and turn-off remain small (<0.5 mJ) in the whole range of  $C_S$  and  $R_S$ .

If the damping resistor and capacitor are chosen as  $R_s$ =10  $\Omega$  and  $C_s$ =10 nF, the oscillation currents with and without damping circuit can be depicted by performing the analysis above, as shown in Fig. 15. Fig. 15 (a) presents the calculated results while Fig. 15 (b) shows the experimental results under the same conditions. It can be seen that by applying the damping circuit, the oscillation settling time is largely reduced, thus the attenuation of current oscillation can be accelerated by the damping circuit.

The calculated waveforms of gate-emitter voltages of the IGBT during the turn-on event with and without damping circuit are shown in Fig. 16. As shown in the figure, because of the transconductance and common emitter inductance  $L_{\it eE2}$ , the oscillations in collector current cause oscillation in the gate-emitter voltage. By introducing the damping circuit, the oscillation in gate-emitter voltage is mitigated as well.

The theoretical analysis of the damping circuit is helpful to

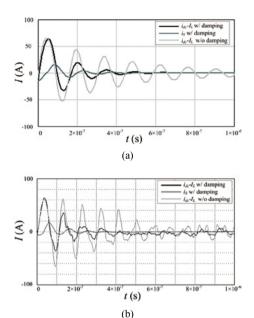


Fig. 15. Calculated (a) and tested (b) waveforms of current oscillation with and without damping.

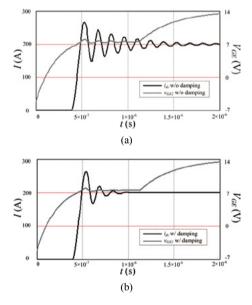


Fig. 16. Calculated waveforms of gate-emitter voltage and DC bus current: (a) without damping; (b) with damping.

determine the range of the resistance and capacitance for the damping circuit. It should be noted that the analytical model introduced in this paper is largely dependent on the parasitic elements of the module and the test circuit. The parasitic capacitances of the devices are especially critical because the variations in these capacitances may largely affect the calculation results. The parasitic capacitances are strongly non-linear components and sometimes may not be obtained from the device datasheet. Therefore, further experimental adjustment of the damping resistor and capacitor is still necessary since the values of parasitic components used in the theoretical estimation may differ from the actual values in the experiment system.

C. Difference between the Designs of Damping Circuit and Snubber Circuits

To overcome the turn-off over-voltage caused by the loop inductance, several variations of snubber circuits are investigated in the literature [32], [33]. The typical topologies of snubber circuits and the damping circuit are shown in Fig. 17, where LS is the stray inductance of the commutation loop,  $C_{CEI}$  and  $C_{CE2}$  are the parasitic capacitances of the switching devices. In the figures, the parastic components that each circuit is mainly dealing with are highlighted.

The discharge suppressing RCD snubber shown in Fig. 17 (c) and the decoupling capacitor (C snubber) shown in Fig. 17 (d) are the most commonly used snubber circuits for IGBT modules [32], [33]. The snubber circuit is aimed to suppress the turn-off voltage spike, thus the snubber capacitance  $C_{Sn}$  is designed to absorb the energy stored in the loop stray inductance LS during the conduction state of the IGBT. The snubber capacitor should be of high

frequency type with low ESR and ESL. As reported in [23], the discharge suppressing RCD snubber shown in Fig. 17 (c) is also able to suppress the turn-on oscillations caused by the reverse recovery of the Si free-wheeling diode. However, since suppressing turn-on oscillation is not the primary purpose of snubber circuit, the designs of the capacitance and resistance are not optimized for turn-on oscillation suppression. While on the other hand, the damping circuit for Hybrid IGBT is dedicated to attenuating the turn-on current oscillation. During turn-on process, the damping circuit is used to damp the oscillation between the loop stray inductance LS and the parasitic capacitances of the switching devices  $C_{\it CE1}$  and  $C_{\it CE2}$ . The damping circuit provides a conducting path for high frequency currents. Part of the high frequency currents flowing through the parasitic capacitors of the switching devices are directed to the damping circuit and dampened by the damping resistor.

There are many references concerning the design of snubber circuits to mitigate the turn-off voltage spike and voltage oscillation [23],[30],[31]. The capacitance of the

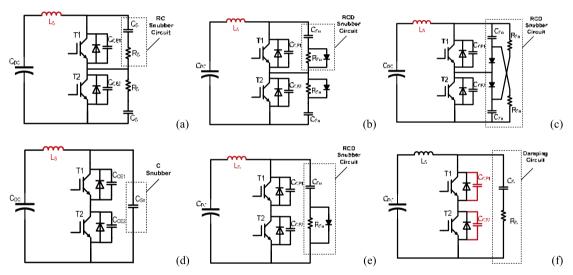


Fig. 17. Typical topologies of snubber circuits and the damping circuit

snubber capacitor CSn can be estimated by the following equation [23]:

$$C_{Sn} = L_S \cdot I_L^2 / (V_{pk} - V_{DC})^2$$
 (21)

where  $V_{pk}$  is the desired peak voltage during turn-off. Applying the same conditions used in the analysis of damping circuit, i.e.  $L_s$ =75 nH,  $I_L$ =200 A, and the allowable voltage overshoot is set to 100 V, it can be estimated that the snubber capacitor is  $C_{Sn}$ =300 nF.

During turn-on interval of the IGBT, as the IGBT current rises with a slew rate of di/dt, the voltage induced on the loop stray inductance  $L_S$  causes the voltage across the positive and negative terminals of the module to drop by  $L_S$ •di/dt while the snubber capacitors are charged to the DC bus voltage VDC, thus the diodes of the RCD snubber is reverse biased, yielding a turn-on equivalent circuit of the RCD snubber shown in Fig. 18 (a) which can be further

simplified as Fig. 18 (b).

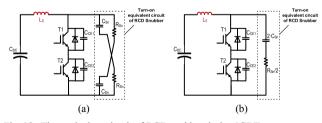


Fig. 18. The equivalent circuit of RCD snubber during IGBT turn-on.

As shown in Fig. 18 (b), the equivalent circuit of RCD snubber at turn-on has the same structure as the damping circuit. However, since the snubber circuit is used to mitigate voltage spikes, the capacitance is much larger than that of the damping circuit. In the turn-on equivalent circuit of RCD snubber, the capacitance is  $2 \cdot C_{Sn} = 600$  nF which may largely increase the loss in the resistor. By performing the same analysis procedure of the damping circuits, the turn-

on current waveforms with snubber circuit can be derived as well. As shown in Fig. 19 (a), if a small value of 5  $\Omega$  is chosen for the snubber resistor, the snubber circuit has some ability of mitigating the turn-on oscillation, however the loss in the snubber resistor is 2.29 mJ for a turn-on event, much larger than the damping circuit (<0.5 mJ). If the snubber resistor uses a large value to reduce the losses, as shown in Fig. 19 (b) where the snubber resistor is set to 50  $\Omega$ , the loss in the snubber resistor is reduced to 0.71 mJ at the cost of losing the oscillation damping capability.

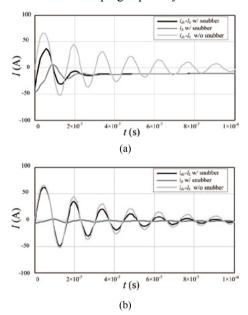


Fig. 19. Calculated turn-on waveforms with snubber circuit: (a) RSn=5  $\Omega$ ; (b) RSn=50  $\Omega$ .

Therefore, by using the conventional snubber circuit design for turn-off over-voltage suppression, the features of effective turn-on oscillation damping and low loss in the snubber resistor cannot be achieved simultaneously. It might be a better solution to combine the decoupling capacitor (C snubber) and the damping circuit, as shown in Fig. 20. A large decoupling capacitor can be used to mitigate the turn-off voltage spike caused by loop stray inductance  $L_s$ , and the design of damping circuit can be implemented to mitigate the turn-on oscillation caused by the resonance between the loop stray inductance  $L_s$  and the parasitic capacitances of the switching devices  $C_{CEL}$  and  $C_{CEL}$ .

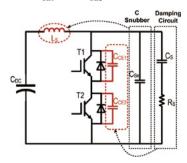


Fig. 20. Combining decoupling capacitor (C snubber) and RC damping circuit to suppress both the current oscillation at turn-on and voltage overshoot at turn-off

### D. Experiment Results of Damping Circuit

The test setup for damping circuit 2 is the same as the test circuit shown in Fig. 2 where the RC damping circuit is connected across the phase leg. Different RC values for the damping circuit are tested to determine the optimized parameters for the suppression of turn-on oscillations. The tests are carried out under 550 V DC bus voltage and 200 A load current, the positive gate voltage provided by the voltage source gate driver is  $V_+$ =14 V, the external gate resistor is  $R_{G,ev}$ =10  $\Omega$ .

To minimize the parasitic inductance of the damping circuit and to simplify the mounting of damping circuit on the hybrid IGBT module, a damping circuit board is made as shown in Fig. 21. In this way, the connection between the damping circuit and the hybrid IGBT module can be minimized. In order not to affect the low inductance connection between the damping circuit and the hybrid module, only the DC bus current idc are measured in the experiments.

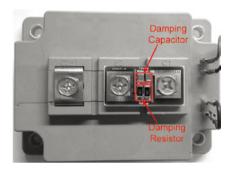


Fig. 21. The mounting of damping circuit on the hybrid IGBT module.

The first step is to keep the damping resistance at  $R_s$ =5  $\Omega$ , and the damping capacitance is set to  $C_s$ =2.2 nF, 4.4 nF, 6.6 nF, 8.8 nF, 11 nF and 13.2 nF respectively. The maximum oscillation current  $I_{OSC\_MAX}$ , the oscillation settling time ts and the additional damping resistor energy losses during turn-on and turn-off ( $E_{damp, on}$  and  $E_{damp, off}$ ) with different damping capacitors are shown in Fig. 22. To evaluate the error between the calculations and the experimental results, the calculated and tested results are depicted in the same figures.

Fig. 22 illustrates that the damping circuit is effective in suppressing the turn-on oscillation. By using the damping circuit, the oscillation settling time is largely reduced while around 10 A over-current is added to the maximum oscillation current. The additional damping resistor loss increases with increasing damping capacitor, which is in good match with the theoretical analysis. The additional damping resistor loss is relatively small compared to the turn-on loss of the IGBT which is 24.1 mJ under the given conditions, thus no significant loss increase is introduced.

As can be seen from Fig. 22, when  $C_s$ =11 nF, the damping circuit has the best balance between oscillation suppression and unwanted side-effects.

The next step is to fix the damping capacitance at 11 nF, and the damping resistance is chosen as RS=0.8  $\Omega$ , 1.1

 $\Omega$ , 1.7  $\Omega$ , 2.5  $\Omega$ , 3.3  $\Omega$ , 5  $\Omega$ , 6.8  $\Omega$  and 10  $\Omega$  respectively. Fig. 23 shows the maximum oscillation current  $I_{OSC\_MAX}$ , the oscillation settling time ts and the additional damping resistor energy losses  $E_{damp, on}$  and  $E_{damp, off}$  with different damping resistors. Again, the calculated and experimental results are depicted in the same figures.

It can be seen from the test results that the best balance between oscillation suppression and side-effects is achieved when  $R_s$ =2.5~3.3  $\Omega$ . Finally,  $R_s$ =2.5  $\Omega$  is chosen. Therefore, the optimized parameters for the damping circuit are:  $C_s$ =11 nF and  $R_s$ =2.5  $\Omega$ .

Note that in Fig. 22 and Fig. 23, the tested and calculated results bare the same trends. The calculated maximum oscillation current and oscillation settling time are very

losc\_MAX (A) 70 10  $C_S(nF)$ (a) 1200 700 w/o damping circuit 600 500 (Su) 53 300 200 100  $C_S(nF)$ (b) 0.4 Tested Edamp, on (mJ)  $C_S(nF)$ (c) 0.2 0.16 0.12 0.08 0.04 Calculated 0  $C_S(nF)$ 

Fig. 22. Turn-on oscillation using damping circuit with different damping canacitors:

- (a) Maximum oscillation current; (b) Oscillation settling time;
- (c) Energy loss in the damping resistor during turn-on; (d) Energy loss in the damping resistor during turn-off.

close to the experimental values. Therefore, the theoretical analysis introduced in this paper is able to provide a good estimation of the turn-on oscillations.

The same experiment procedure is also performed for damping circuit 1, and the achieved optimal parameters of damping circuit 1 are  $C_s$ =5.2 nF and  $R_s$ =6.8  $\Omega$ .

The waveforms of the DC bus current  $i_{dc}$  and the collectoremitter voltage of the upper arm IGBT  $v_{CEI}$  in a turn-on event of the lower arm IGBT with and without the damping circuits are shown in Fig. 24. The performances of oscillation suppression and side-effects of the damping circuits are listed in Fig. 25 alongside each other. It should be noted that the turn-on energy losses  $E_{on}$  listed in Fig. 25 also include the additional energy loss of the damping resistor.

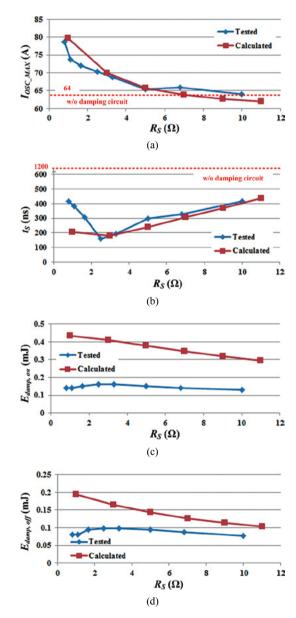


Fig. 23. Turn-on oscillation using damping circuit with different damping resistors:

- (a) Maximum oscillation current; (b) Oscillation settling time;
- (c) Energy loss in the damping resistor during turn-on; (d) Energy loss in the damping resistor during turn-off.

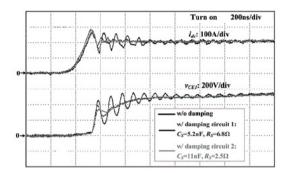


Fig. 24. The comparison of turn-on waveforms with and without the damping circuit.

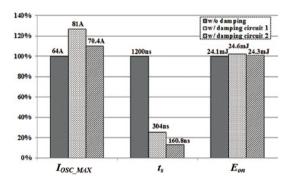


Fig. 25. The performance of oscillation suppression by the damping circuit.

According to the test results, the damping circuits are able to effectively suppress the turn-on current oscillation of the hybrid module. It should be noted that by applying the damping circuits, the maximum oscillation current  $I_{OSC\ MAX}$ increases due to the discharging of damping capacitor, which is a disadvantage of this method. The oscillation settling time is reduced to  $1/4 \sim 1/8$  of the original value by attaching the damping circuit. Moreover, no significant turn-on energy loss increase (<1%) is caused by attaching the damping circuit. Comparing the two damping circuits, damping circuit 2 is able to achieve the lower turn-on current overshoot and the faster attenuation of oscillation. Damping circuit 1 is the RC circuit parallel connected to each device. Therefore, at each turn-on event, the capacitor is fully discharged, and at each turn-off event, the capacitor is charged to DC bus voltage. During the turn-on event, the discharging current of the damping capacitor flows through the IGBT causing a rise in the maximum oscillation current  $I_{OSC\ MAX}$ . Also, the charging and discharging current flowing through the damping resistor cause a larger loss in the damping resistor. While for damping circuit 2, the voltage of the damping capacitor does not change much during turn-on and turnoff, only high frequency ripples are present, thus the added current and losses are lower than that of damping circuit 1.

To evaluate the influence of damping circuit on the turn-off characteristics, the turn-off voltage and current waveforms with and without damping circuit are shown in Fig. 26. The testing conditions are the same as those used to obtain the waveforms in Fig. 24. The damping circuit used is damping circuit 2 with the parameters of  $C_s$ =11 nF and  $R_s$ =2.5  $\Omega$ .

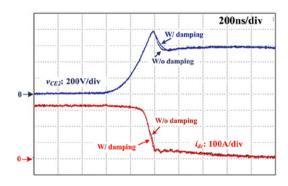


Fig. 26. The comparison of turn-off waveforms with and without the damping circuit.

As shown in Fig. 26, because of the turn-off tail current effect of the IGBT, no major oscillations in the current and voltage waveforms are observed during the turn-off process. Because of the relatively small capacitance of the damping circuit, the damping circuit has little effect on the turn-off voltage waveform. There are no significant changes in the voltage overshoot and current slew rate before and after attaching the damping circuit.

# IV. COMBINING DAMPING CIRCUIT WITH ACTIVE GATE DRIVER

In certain applications, besides the duration of current oscillation, the peak current overshoot may be restricted as well. From the studies introduced in the previous sections, it is found that by steering the gate voltage and gate current, active gate drivers are able to suppress the peak current overshoot during turn-on process of hybrid IGBT module. Therefore, by combining the active gate driver with the damping circuit method proposed above, both the suppression of current oscillation and current overshoot can be achieved simultaneously.

Since gate voltage and gate charging current both have large effects on the turn-on maximum oscillation current of the hybrid module, the function of current overshoot suppression can be achieved by adjusting the gate voltage or gate charging current during collector current rising stage in the turn-on process. On the other hand, since gate charging current has large effect on the turn-on delay time and the duration of miller plateau stage, to reduce the total turn-on time and turn-on energy loss, the duration of miller plateau can be reduced by injecting an extra current into the gate during the collector-emitter voltage falling stage. The schematic diagram of the active gate driver used in this paper is shown in Fig. 27.

As shown in Fig. 27, a gate current sink formed by a MOSFET and a diode is used to bypass part of the gate current during the collector current rising stage of the turn-on process, thus the current rising rate is decreased to suppress the current overshoot [6]-[9], [22]. The gate voltage  $v_{GE}$  is detected in the turn-on process for the determination of different switching stages. When  $v_{GE}$  reaches a preset

threshold voltage, the sink MOSFET will be turned on.

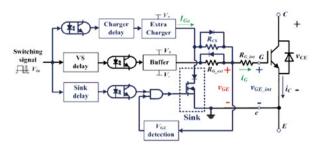


Fig. 27. Schematic diagram of active gate driver

A current source is used as an extra gate charger during the collector-emitter voltage dropping stage to accelerate the voltage drop. The conceptual turn-on waveforms of the active gate driver are shown in Fig. 28, where the dashed lines represent the waveforms achieved by traditional voltage source driver and the solid lines are the waveforms of the active gate driver.

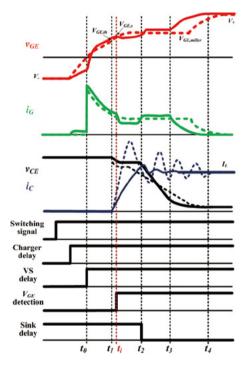


Fig. 28. Conceptual turn-on waveforms of active gate driver.

As shown in Fig. 28, when the turn-on signal comes, the extra gate charger turns on after a short delay. Before time point  $t_i$ , when  $v_{GE}$  has not reached the preset threshold value  $V_{GE,s}$ , the sink MOSFET is turned off, and the extra charger charges the gate, reducing the turn-on delay time. At time point  $t_i$ ,  $v_{GE}$  reaches  $V_{GE,s}$ , the sink MOSFET turns on and bypasses part of the gate current, reducing the collector current rising rate of the IGBT. Then at time point  $t_2$ , when collector current reaches the maximum value, the sink MOSFET is turned-off, and the extra charger charges the gate again to reduce the time duration of miller plateau stage. It should be noted that the gate-emitter voltage  $v_{GE}$  during

turn-on transient is largely dependent on the characteristics of the IGBT, such as input capacitance and transconductance. Therefore, the pre-set threshold value  $V_{GE,s}$  of the active gate driver should be experimentally adjusted for the specific IGBT to reach the optimal performance.

To achieve the optimized turn-on performance, the values of  $R_{CS}$ ,  $I_{Ga}$  and the sink delay time should be selected carefully.  $R_{CS}$  determines how much of the gate current is bypassed during the current rising stage,  $I_{Ga}$  is the extra gate charging current provided by the current source which determines the voltage dropping rate of the miller plateau stage, and the sink delay time should be carefully set so that the sink MOSFET turns off exactly at the time point when collector current reaches its peak value.

The experimental study of the active gate driver is done in the double-pulse test bed shown in Fig. 2. The positive gate voltage  $V_+$  is 13 V and the external gate resistance  $R_{G\_ext}$  is 3.3  $\Omega$ . Tests of turn-on characteristics have been done under 550 V DC bus voltage and 200 A load current. The achieved turn-on waveforms of the active gate driver when  $R_{CS}$ =12  $\Omega$  and  $I_{Ga}$ =300 mA are shown in Fig. 29 along with the turn-on waveforms of the conventional voltage source gate driver.

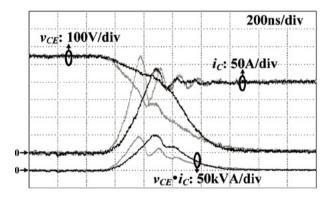


Fig. 29. Achieved turn-on waveforms of active gate driver

As shown in Fig. 29, the grey traces are the waveforms of the conventional voltage source gate driver and the black traces are those of the active gate driver. With the help of the active gate driver, the current rising rate is declined and the current overshoot reduces from 86.2 A to 44.6 A, a 50% reduction is achieved. On the other hand, the turn-on energy loss increases from 29.8 mJ to 34.3 mJ, 15% turn-on energy loss increase is introduced by the active gate driver.

The gate voltage waveforms of the active gate driver and the conventional voltage source driver are shown in Fig. 30. As shown in the waveforms, the gate voltage  $v_{GE}$  during the current rising stage is reduced while in the other stages  $v_{GE}$  is boosted by the extra gate charger, thus the current rising rate is reduced while the other stages are accelerated, achieving the desired turn-on performance.

Also can be noticed form Fig. 29 and Fig. 30 that since damping circuit is used, the turn-on oscillation is largely mitigated. Now the turn-on current waveform is approaching the ideal waveform with low overshoot and little oscillation.

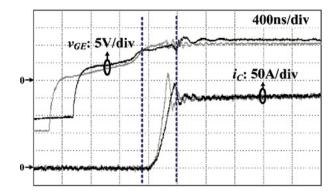


Fig. 30. Gate voltage waveform of the active gate driver

### V. CONCLUSION

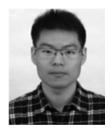
In this paper, methods to suppress the turn-on oscillation of hybrid IGBT module are studied. First, experimental analysis is used to evaluate the impacts of gate driver on the collector current oscillation during the turn-on interval of hybrid IGBT module. It is found that by decreasing gate drive voltage and gate charging current, the current overshoot can be suppressed. However, the active gate driver is not effective in reducing the settling time of oscillation. To mitigate the oscillation, a turn-on oscillation suppression method is proposed with combination of damping circuit and active gate driver. According to the analytical and experimental results, the damping circuit is able to effectively reduce the settling time of turn-on oscillation of hybrid IGBT module. Moreover, the damping circuit does not have much impact on the switching losses. The differences between the designs and working principles of snubber circuits and damping circuit are analyzed. It is shown that because the main purpose of snubber circuit is to suppress turn-off over-voltage, the designs and selection of capacitor types are different with damping circuit. By using the conventional snubber circuit design the features of effective turn-on oscillation damping and low loss cannot be achieved simultaneously. It is thus recommended to use the proposed damping circuit design to suppress the current oscillation at turn-on. Then an active gate driver is experimentally studied to illustrate its effectiveness in suppressing the turn-on current overshoot without largely increasing the turn-on energy loss. Combining the damping circuit with the active gate driver, both the suppression of current overshoot and the fast attenuation of current oscillation can be achieved without largely increasing the switching times and switching losses.

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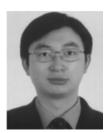
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# Distributed Power Electronics: An Enabler for the Future Grid

Deepak Divan and Prasad Kandula

Abstract—Rapidly decreasing prices for renewable energy, increasing industrialization and electrification of the global economy, and a world-wide focus on reducing carbon emissions, is causing a reexamination of the power system of the future. A reliance on centralized planning and control, scheduled and dispatched generation, and unidirectional power flows, allowed the design of a robust and scalable power system, that did not require dynamic controls infused into the grid. As a result, the existing grid, the most complex machine built by man, has been the driver of sustained global economic growth for well over a century. Increasing levels of variable and non-dispatchable renewable energy resources mixed into the grid, bidirectional power flows resulting from a dramatic increase in the number of prosumers ('producer + consumer'), are adding complexity, volatility and economic inefficiency to grid operations, making grid control with conventional centralized technologies very challenging. This paper looks at the role that distributed power electronics could play in the grid of the future, allowing a costeffective approach to grid control that can help achieve global objectives of operating with high renewable penetration.

*Index Terms*—Power electronics, dynamic control, power flow control, dynamic VAR control.

### I. Introduction

THE electricity infrastructure has powered the global L economy over the last 100 years. A primary objective has been to provide universal and affordable energy for all, an objective that has guided the architecture and design of the power system. Early efforts at distributed, even local DC generation, were quickly replaced by centralized AC generation and transmission/distribution networks that spanned entire continents. The economics of generation from coal based thermal plants and large hydroelectric plants were tough to beat at small local scale. Further, the ability to transmit power over hundreds of miles at elevated voltages allowed the aggregation of loads such that the generation plants could be larger and more economical. Load diversity also allowed the actual thermal rating of generation and power delivery assets to be significantly lower than the total peak load connected to the grid. Similar capacity reductions are seen for power delivery assets.

The growth of the power system occurred in an era when slow electro-mechanical controls were the only option. Large generators in vast interconnected systems had to operate with millisecond precision, balancing generation and load instantly, while maintaining voltage across geographically dispersed networks. This needed inherently stable control mechanisms that would ensure that the system operated reliably and met its performance objectives. This was achieved with an array of tools including generator frequency-voltage droop profiles, slack busses, (N-X) redundancy in assets, meshed transmission systems, and a balancing process that included day ahead markets, locational margin pricing, as well as load-shedding as a last-ditch mechanism. With the basic system operating stably and predictably, efforts moved to overlay complex system optimization control on the power system such that availability and reliability could be further improved, and cost could be reduced. This approach has resulted in a centralized command and control structure with dispatchable generation, unassailable rights that customers have to access as much power whenever they want it, and to handle affordability for poorer customers by moving to a flat pricing structure for all residential customers, and many industrial/ commercial customers as well.

While this strategy has delivered sustained economic growth globally over 100 years, it has also led to a bloated electricity infrastructure, high greenhouse gas emissions [1], climate change and an inflexible system that is not sustainable. The power infrastructure is poised for dramatic change with rapid growth in non-schedulable renewable resources [2], and an increased focus on improving economic, operational and energy efficiency while reducing technical and non-technical losses. Perhaps the most profound change is the continuing year over year exponential decrease in solar PV prices [3]. With levelized cost of energy (LCOE) for PV solar farms approaching \$0.03/kWHr in some new bids and US\$0.60/watt for PV panels, it is clear that solar is affordable and is at grid parity for a large part of the world [4]. Wind energy has followed a similar steep decrease in prices, and is seeing broad adoption globally. These successes have led to ambitious targets for renewable energy on the grid, with targeted penetration levels of greater than 50% on the power system [5]. The challenges of integrating high levels of renewable energy onto the grid cannot be underestimated - power electronics will play an increasing role in achieving this objective.

# II. HVDC AND FACTS – FIRST NEED FOR POWER ELECTRONICS

The ability to transfer AC power over increasing distances

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was limited by the inductive impedance of overhead transmission lines, requiring ever higher voltages (now approaching 1 million volts). For underground or undersea cables, it was the capacitance of the cable that limited the distance over which power could be transferred. It was recognized early on that DC power could be transferred over longer distances for both over-ground transmission lines and for underground cables. In the 1950's, the first high voltage DC (HVDC) link was built in Sweden and transferred 20 MW at 100 kV using thyratron devices [6]. Growth of this technology required the development of the silicon thyristor by GE in the late 1950s, resulting in widespread deployment of HVDC links. This technology, the first use of power electronics on the grid, allowed delivery of gigawatts of bulk power over thousands of miles, connecting resource rich hydropower areas with large urban centers that needed the energy. Thyristor based HVDC links were very customized, required large investments in the converter stations, transformers, and the build of the line itself (not including permitting, right of way and other non-technical issues). Further, HVDC lines operated with poor and variable power factor and high harmonic levels, requiring the development of techniques to mitigate these issues [7].

The second major issue is dynamic control on the grid, the need for which has been understood for a while. Unlike traditional control systems where the variable 'analog' control is located near the source of the disturbance, in existing power systems the only 'analog' control is the AGC control on the generator - as far from loads and location of disturbances as possible. It is a testament to the ingenuity of past generations of power engineers that they made this 'backwards' control strategy work, and actually work well. As the system grew increasingly vast and loaded, there was a need to provide VAR support, not just at the generator end, but nearer the load. Synchronous condensers, often using retired generators, provided voltage support using VAR injection. Switched capacitor banks were also used to provide support when needed. However, synchronous condensers were not always available where needed, and switched capacitors were slow and had limited life. With the advent of the thyristor, a better solution was static VAR compensators (SVC), using fixed capacitor banks along with thyristor controlled reactors. For almost three decades,

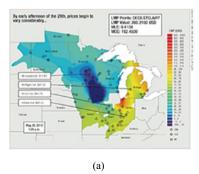
SVC's rated at 50-100 MVAR provided dynamic VARs to stabilize the voltages, to improve system stability and to increase the penetration of variable wind energy on the grid. The SVC was the first of different types of flexible AC transmission systems (FACTS), devices that provided dynamic control, mostly at the transmission grid level.

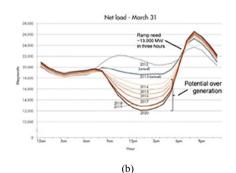
As gate turn-off devices, such as IGBT's, became available, a new type of FACTS device based on voltage source converter (VSC) technology became the new gold standard. STATCOMs that could provide leading and lagging VAR support offered enhanced dynamic performance without issues related to harmonics, albeit at higher cost [8]. The concept of the unified power flow controller (UPFC) was proposed, and several were built to demonstrate voltage/ power-flow control and VAR injection capability at the transmission level [9]. While such large FACTS devices have been commercially available for decades, deployment has been limited due to cost, complexity, large footprint and high mean time to repair. Further, as wide scale deployment of renewable resources has occurred, it has become clear that dynamic control is needed at a more distributed level, and with control philosophies and cost points that are very different from existing centralized FACTS solutions.

### III. NEED FOR DISTRIBUTED DYNAMIC CONTROL

Moving from centralized control and dispatched generation to higher levels of renewable energy penetration, cause impacts that cannot easily be managed under the old paradigm. There are several distinct issues – grid integration of bulk wind and PV generation in remote areas connected to the transmission grid, dynamic balancing of instantaneous generation and load imbalances (including spatial and temporal balancing), and integration of distributed solar located at the edge of the grid. Several major challenges have been identified in all cases. The most obvious issue is the variability and lack of dispatchability of renewable resources. This leads to price volatility, ramp rates that are difficult to manage with conventional thermal generation resources, as shown in Fig. 1, and grid congestion that can lead to severe curtailment of renewable resources [10].

Issues such as time varying LMPs are all caused by dynamic balancing issues, even as the ISO operates its





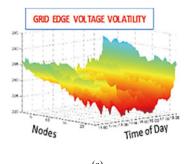


Fig. 1. Impact of high renewable penetration, a) Midwest Independent System Operator Locational Margin Pricing maps showing temporal and spatial variability from -\$11/MWHr to +\$500/MWHr; b) California thermal ramp rates in excess of 13,000 MW/3 hours needed to counter solar impact; c) voltage volatility on distribution feeder limits PV hosting capacity of distribution feeders [10].

various wholesale market mechanisms. The ability to direct power from low-cost areas to high-cost areas over the existing network would help improve system efficacy. With the existing meshed sub-transmission and transmission networks, directing power flows is challenging, often resulting in heavy congestion of corridors, severe curtailment of renewable resources, and an unnecessary increase in the use of non-optimal resources that results in higher cost and higher emissions [11].

Mainly two control levers exist to achieve dynamic control on the grid – Voltage control and VAR injection. These levers can be used to achieve significant objectives including power flow control in meshed grids, demand control, and integration of high levels of renewable energy into the grid.

Fig. 2 shows various power electronic technologies that can provide the above mentioned two control levers at different locations on the grid. The next three sections provide a brief description of some of the technologies.

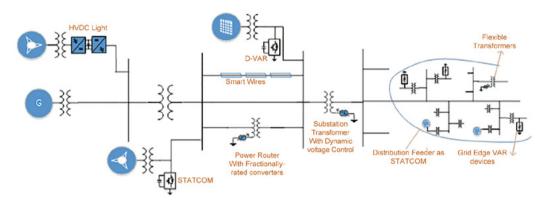


Fig. 2. Various power electronic technologies that can provide Volt/VAR control and phase angle control to realize power flow control, voltage support and other dynamic control functions at different locations on the grid.

# IV. Dynamic Power Flow Contro – Transmission Systems

### A. HVDC Light

HVDC light, successor to conventional HVDC technology, is based on voltage source converter technology using IGBTs and other gate turn-off devices [12]. Compared to conventional HVDC, HVDC light technology has superior reactive power control capability. It can provide independent control of active and reactive powers increasing the transfer capacity of the AC network surrounding the terminal. Such features enable applications in areas such as:

- · Connecting wind farms to power grids
- Underground power links
- Providing shore power supplies to islands and offshore oil & gas platforms
- Connecting asynchronous grids
- City center infeed

A variant of HVDC light using back-to-back (BTB) converter (no DC cables) can be used to achieve power flow control, which can aid in integrating variable renewable resources. An example is the 220 MW HVDC BTB system at Oklaunion, Texas, USA [13]. The schematic of HVDC light with back-to-back converter is shown in Fig. 3. It consists of two transformers and two converters each rated at 1.0 pu of the throughput power. A HVDC BTB system can inject 1.0 pu voltage in series with the line.

HVDC Light technology now reaches 1,800 MW and ±500 kV. But in most applications, 1.0 pu power flow

control can be achieved with 0.05 - 0.15 pu voltage injection mainly because of the low line impedance (5-15 %) [14]. Hence, HVDC BTB may be an overkill for simple power flow control applications, but is a viable option when needed to integrate asynchronous systems, provide low-frequency power oscillation damping, improve stability margins etc.

### B. Multi-Point HVDC Light

An extension of HVDC light is the HVDC multi-terminal system, which can be used to form regional and interregional HVDC systems [15]. Regional multi-terminal HVDC system (Fig. 4) can reduce the number of converters required to connect multiple sources to the grid. Interregional HVDC multi-terminal systems (Fig. 5) can form the basis for HVDC grids. HVDC grids present an alternative to conventional HVAC systems, which are becoming increasingly difficult to build because of environmental, right-of-way issues [16].

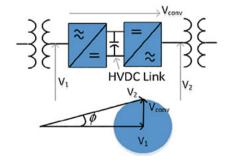


Fig. 3. Schematic of HVDC Light implementation with back-to-back converter.

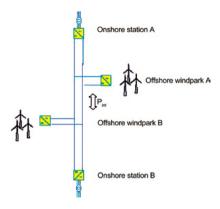


Fig. 4. Regional multi-terminal HVDC grid [15].

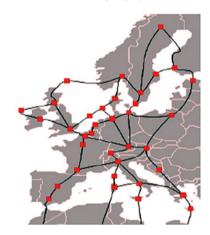


Fig. 5. Interregional multi-terminal HVDC grid [15].

## C. Power Flow Control Using Fractionally-Rated Converters

As stated above, HVDC BTB technology may be too expensive for simple power flow control applications within AC networks. FACTS devices such as unified power flow controller (UPFC) [17] based on fractionally-rated converter topologies have been proposed for dynamic power flow control. The UPFC concept uses two fractionally-rated, transformer-coupled inverters to achieve independent control of the real and reactive power flow on the transmission line. Several UPFCs have been built to demonstrate the concept. including a 300 MVA device in New York, but widespread deployment has not occurred. The cost and complexity of the solution, including the ability of the series transformer to withstand short circuit faults, are perhaps key challenges. Further, even infrequent downtime due to failures and a long mean time to repair can have significant impact on UPFC availability/reliability. Based on many conversations with utility engineers in the US, it appears that the complexity and cost associated with large centralized FACTS devices, and the dependence of the utility on vendors for critical maintenance and operations, has made the business case very challenging. As a result, even though FACTS solutions, such as the UPFC, have been commercially available for 20+ years, very few have been deployed. Another approach is required to achieve these very real and tangible benefits.

## D. Power Flow Control Using Distributed 'Fail-Normal' Devices

Based on utility feedback, Divan [18] proposed the concept of distributed power flow control devices, where several devices could be used to achieve the desired control range. Each device would operate over a narrower range. and would be used to augment existing/conventional utility assets by overlaying the dynamic control capability on what is otherwise a passive asset. The power converters used would be small-rated and modular, and would be designed with 'fail-normal' capability, such that the asset would operate conventionally (i.e. without dynamic control) if the converter were to fail, or under short-circuit system faults. This also provided the utility with assurance that the desired control capability could be maintained even when individual control devices failed. This set of basic principles provides the basis for a new class of distributed utility solutions that better meet utility operational requirements at modest cost.

Implementations of 'fail-normal' power router technologies based on fractionally-rated converter and magnetics include the controllable network transformer (CNT), which consists of a load tap changing transformer augmented by a direct AC converter [19], and a power router that consists of a transformer augmented with a fractionally-rated back-to-back converter (FR-BTB) [20], Implementation of CNT and FR-BTB are shown in Fig. 6. Since the converter is connected across the taps, the converters have to handle only fractionally voltage and hence, the fractional rating. These technologies affect control over real and reactive power by series injecting voltage with different phase angle and amplitude, respectively.

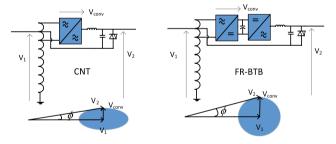


Fig. 6. Schematic of controllable network transformer (CNT) and power router based on fractionally-rated BTB converter (FR-BTB). The 'fail-normal' thyristor switch can be seen in both schematics.

The CNT however is optimized for applications that require more reactive power flow control than real power flow control such as in loop-flow management in a meshed grid. The FR-BTB topology uses standard three level converters in a back-to-back configuration to achieve symmetrical control over both real and reactive power. On the other hand, the FR-BTB utilizes bulk-energy storage in the form of electrolytic capacitors, with size and life limitations. Another approach called the compact dynamic phase angle regulator (CD-PAR) [21] addresses implementation of a power flow control device optimized for control over real power without using any bulk energy storage.

Both the CNT and FR-BTB topologies have been demonstrated at the 13 kV/1 MW level, demonstrating the ability to control power flows with small rated transformers and converters, as well as the concept of fail-normal operation. However, both topologies require the electronics to be floating at the line voltage. Implementations of floating converters have challenges such as protecting sensitive electronics against corona damage, and ensuring adequate isolation exists between the floating and grounded parts and between components floating at two different phases [21]. Further, like any piece of utility gear, the BIL rating needs to be well coordinated with the surrounding protective gear on the system. For example, any equipment operating in a 13 kV system typically require a BIL rating ranging from 90 to 120 kV. A design must be able to incorporate sensitive electronics within a product that is able to sustain this level of voltage impulse without any damage.

To avoid challenges of a floating system, a modified approach of CD-PAR, with changes to the design such that the electronics are much more closely coupled to the ground potential is proposed in [22]. As shown in Fig. 7, the "grounded" CD-PAR employs a fully-rated LTC-like transformer augmented with fractionally-rated direct AC converters [23], [24]. With a small modification of the transformer configuration, and with the addition of power converters connected across the neutral-side taps, a device that provides dynamic phase angle control can be obtained.

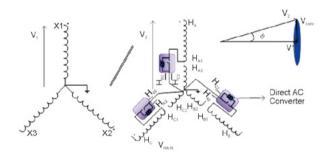


Fig. 7. Grounded compact dynamic phase angle regulator schematic [24].

A 13 kV, 1 MVA 3-phase grounded CDPAR has been built and tested in the field on a 13 kV distribution feeder [25]. The device was connected across two distribution feeders and was shown that the power flow between the substations can be dynamically controlled by varying the orthogonal series voltage injection. The advantages of fractionally-rated converter based solution was demonstrated by achieving 600 kVA of power flow control at 13 kV with a converter rated for 35 kVA and rated to handle 500 V.

In contrast with CDPAR with floating converter, the grounded CDPAR implementation requires a full-rated transformer, which makes it more cost effective for applications that also require voltage step up/down and/or galvanic isolation functionality. For simple power flow control applications, the grounded CDPAR provides a practically implementable solution in short term. Once the issues associated with floating electronics are addressed and

demonstrated at reasonably higher voltages, CDPAR with floating converter nay prove to be even more economical.

### E. Distributed Series Impedance (DSI)

Distributed Series Impedance (DSI) module wires is an impedance control device belonging to distributed FACTS (D-FACTS) family [18]. DSI converts a transmission line to a smart asset providing ability to control power flows in meshed transmission systems. The schematic of DSI, shown in Fig. 8, consists of a single turn transformer with control circuitry on the secondary. The control circuitry, consisting mainly of a fast switching switch, acts to add either inductance ( $X_M + X_L$ ) or capacitance ( $X_C$ ) to the line, thereby increasing or decreasing line impedance, respectively.

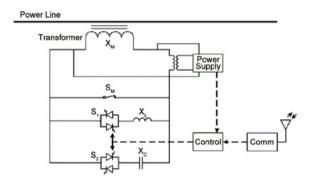


Fig. 8. Schematic of Distributed Series Impedance (DSI).

As the name suggests, DSI is a distributed solution, with multiple modules clamped directly over the line conductor as shown in Fig. 9(a). With a large number of modules operating together, it is possible to have a significant impact on the overall power flow in the line. If N device are used in series along a power line, one can realize 2N discrete values as shown in Fig. 9(b). In N is large, say 100, a resolution of 0.5 % can be achieved, approximating a linearly varying line impedance.

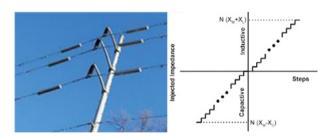


Fig. 9. (a) Distributed modules of Smart Wires [26]. (b) Control range of N DSI modules.

DSI is an inverter-less solution that can be installed on an existing transmission line without requiring a break-in-the-wire. The simplicity allows the DSI module to withstand short circuit current, meet basic insulation level (BIL) requirements, handle high E-fields, eliminate corona discharge, and operate through punishing freeze/thaw and heat/cool cycles. A variant of DSI, calvled

Powerline Guardian<sup>™</sup> by Smart Wires Inc, is commercially available, with multiple modules operating on high voltage transmission lines [26].

### V. Dynamic Volt/Var control-Transmission

Intermittent sources of energy such as wind and solar can impact the quality and reliability of the electrical network. Dynamic shunt VAR support devices can detect and instantly compensate for voltage fluctuations, mitigate impacts of flicker, and correct power factor, protecting wind farms, solar parks and the electrical grid. Some of the prominent shunt VAR support devices are presented here.

### A. STATCOM

Static Synchronous Compensator (STATCOM) is a second generation FACTS device, which is based on gate turn-off devices [27]. STATCOM works on the principle of generating reactive power by circulating currents in the phases through a switching converter. It consists of a Voltage Source Converter (VSC) connected in shunt with the line through a relatively small reactance (0.1-0.15 p.u.). On the input side of the converter is a DC capacitor, essential to maintain the equality of the instantaneous input and output powers. The converter is usually an array of semiconductor switches with forced turnoff capability (GTO thyristors or IGBTs).

STATCOM can either generate or absorb reactive power, and can respond quickly to damp any big disturbance on the power system, which is possible because the reactive power generated by STATCOM is not voltage dependent. The first STATCOM in U.S. was a +/- 100 MVAR installation at Sullivan substation of Tennessee Valley Authority (TVA), in 1995, for regulating the 161 kV bus voltage [8]. Other prominent U.S. installations are as follows: +/- 86 MVAR, 115kV STATCOM at Essex substation, in 2001 [28]; +/- 100 MVAR STACOM at Talega, in 2002; the +/- 95 MVAR STATCOM at Holly substation in 2004.

### B. D-VAR

Dynamic VARs (D-VARs) are modular STATCOMs offered by American Semiconductor Inc. [29]. The modular approach offers a cost-effective, scalable system that allows utilities to install properly sized systems in the most effective power grid locations, staging the installation as desired, and quickly augmenting capability as demands increase. D-VAR solutions are available up to 46 kV and 100s of MVARs. The necessity of dynamic voltage support in future grid is supported by the number of recent D-VAR commercial installations at wind power plants, providing voltage regulation that will respond dynamically to varying load conditions [30].

### VI. DYNAMIC VOLT/VAR CONTROL-DISTRIBUTION

Utilities are observing greater voltage volatility at the

grid. Though a number so studies have shown that voltage volatility can occur because of high residential photo-voltaic (PV) [31]-[34], filed studies have shown that volatility can exist on systems even without significant PV [35]. Voltage volatility at grid-edge cannot be managed using traditional electromechanically switched centralized command and control solutions, which all have slow response and a limited number of operations [36]. Control at grid edge is required to meet the new challenges that utilities are facing as a result of grid modernization initiatives such as energy conservation, peak demand management, grid integration of distributed PV, grid integration of distributed PV, and improved service reliability and quality [35], [37].

Power electronics-based solution implemented on the secondary side of the distribution transformer for voltage regulation are commercially available [38], [39]. Some of the solutions are presented here.

### A. Thyristor-Assisted Tap Changer

The voltage fluctuations caused by PV are much more frequent and a standard electro-mechanical tap-changer (ex. OLTC) may not withstand the resulting wear and tear. Thyristor-assisted tap changers have been proposed to improve reliability, useful life and tolerance against voltage spikes and thermal endurance under fault currents.

The schematic of typical thyristor-assisted tap changer is shown in Fig. 10 [40]. The structure is similar to a standard mechanical tap-changer except that the taps are now selected using thyristors. Also the voltage is injected using an additional auxiliary transformer, which aids in providing isolation between the electronic circuit and the HV winding.

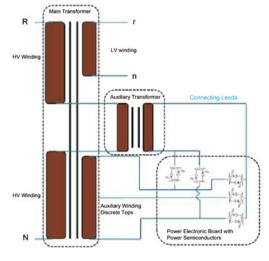


Fig. 10. Schematic of thyristor-assisted tap changer [40].

### B. Flexible Field-Upgradable Transformers

The major drivers for voltage control on distribution systems are the cost and reliability. The standard distribution transformer is pretty inexpensive (\$1200 for 1-phase 50 kVA unit) and is very robust. To be commercially viable,

addition of a new controller should not impact either the cost or the reliability. One of the methods to achieve this is the flexible transformers consisting of a standard distribution transformer with a slight modification to add taps at the low voltage end, as shown in Fig. 11 [41]. A cold plate is also integrated with the transformer housing, which will be used for mounting the electronic module. This mechanism allows passive cooling design, significantly extending the device life time by removing fans. The electronic module can include a power converter that provides voltage and/or VAR control, and can do so at very low cost.

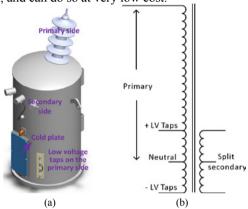


Fig. 11. Flexible transformer: a) CAD model; and b) winding schematic [41].

When the electronic module fails, the transformer retains basic passive transformer functionality. The converter is only fractionally-rated (5 kVA for 50 kVA unit), avoids direct fault current and is located near the ground potential to avoid BIL issues [42]. Hence, the converter contributes very little additional weight and loss for the system while achieving wide-range dynamic voltage control.

### C. Grid Edge Volt-Var Devices

Use of reactive power support available from solar converters is suggested to address voltage volatility [31]. But this approach has issues. Utilities cannot control where the PV systems are deployed or mandate VAR support from customer owned devices. Further, multiple inverters connected to the grid acting autonomously can result in interactions, causing 'hunting' and compromising stability. This concern has been recognized and is being addressed by groups such as the Smart Inverter Working Group in California [43].

Another approach is through the use of fast-acting distributed power electronics devices at the grid edge to achieve volt-var control [44]. The edge-of-network grid optimization (ENGO<sup>TM</sup>) devices are basically low-cost fast acting switched capacitor solution. They operate autonomously on the secondary side of the distribution system and eliminate the nasty variations that are seen due to poor power factor loads and other grid disturbances. A swarm of these gridedge VVC controllers can act in unison to tame the grid into

a well-behaved system and unlock a simple grid-edge VVC scheme to achieve 5-7% of energy and demand control, increase system efficiency by 10% and dramatically increase PV hosting capacity of distribution feeders.

An image of the installed ENGO device and the feeder voltage control achieved is shown in Fig. 12. More than 3000 ENGO devices managed by GEMS have been deployed at over 15 utilities around the world and have been shown to achieve voltage support, peak demand, energy savings, loss minimization, increased PV hosting [45], and the ability to use the distribution feeder itself as a STATCOM [46].

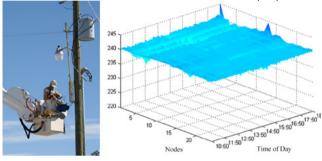


Fig. 12. a) Installed grid edge VVC devices (courtesy Varentec), b) feeder voltage profile after correction. (see Fig. 1(c) for profile before correction)

### VII. CONCLUSIONS

This paper has looked at the role that power electronics has played in grid control, and has presented a view of how distributed power electronics devices may shape the grid of the future. Many of the problems in the future grid are distributed in nature, due to increasing use of distributed generation, and the evolution of smart autonomous devices. The existing centralized control paradigm is unable to manage the increased complexity and volatility. The possibility of interactions between intelligent autonomous devices is real and must be addressed.

New solutions have been demonstrated and are being deployed in the field to attest to these new capabilities. New concepts are necessary for distributed power electronics to meet the reliability and ruggedness demanded in grid applications. This includes 'fail-normal' operation, an overlay and augment strategy, and the use of fractionally rated converters and passive components. The era of distributed control is just beginning, and the future grid cannot be controlled using passive techniques, the way it has been for the past 100 years.

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# A Review of Methods to Increase the Availability of Wind Turbine Generator Systems

Udai Shipurkar, Henk Polinder, and Jan A. Ferreira

Abstract—Availability is an important factor to be considered when designing wind turbine generator systems. The quest for increased availability is based on the following five design approaches - design for component reliability, active control for reliability, design for fault tolerance, prognostics, and design for maintainability. This paper reviews methods focusing on the first three, i.e. component reliability, active control, and fault tolerance. The paper further identifies some promising directions for further research.

*Index Terms*—Availability, reliability, wind energy, generator systems.

### I. Introduction

WIND energy is playing a major role in the energy transition from fossil fuels to renewable energy. In 2015 the world saw a net increase of 17% in the installed global wind power capacity to 432GW [1]. Although extensive research and development has been successful in increasing the size and power production of wind turbines, there is now renewed focus on maintenance costs as they account for a quarter of the Levelised Production Costs (LPC) [2], [3].

Offshore wind turbines have additional challenges for maintenance due to the difficulty of access and the logistics involved in repair. Therefore, failures in wind turbines are not only expensive but also affect the availability of the turbine.

Increasing the availability of wind turbine generator

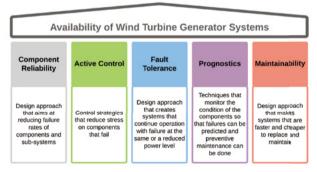


Fig. 1. How can availability in wind turbine generator systems be increased?

systems is based on five pillars or approaches as shown in Fig. 1. These include the design for component reliability, active control for reliability, design for fault tolerance, prognostics, and design for maintainability. This paper focusses on the first three, i.e. component reliability, active control, and fault tolerance.

The remainder of this paper is organised in the following sections; Section II gives an overview of the failures in wind turbine generator systems followed by the mechanisms behind failures in Section III. Section IV introduces the approaches taken in this review and Section V and Section VI review the methods for improving availability for the converter and the generator. Finally, Section VII identifies some promising research directions and Section VIII draws some conclusions from the review.

### II. FAILURES IN WIND TURBINE GENERATOR SYSTEMS

A number of papers have studies failure rates of wind turbine assemblies [4]-[9]. These studies have shown that the generator and the power electronic converter are components of the drivetrain that have a large share of the annual failures. Fig. 2 shows this distribution.

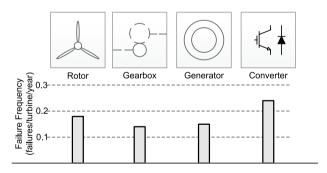


Fig. 2. Failure rate distribution in the wind turbine drivetrain. From [8].

However, to break down the failure rates to a component level failure is difficult, as there is little published data on this. *Lyding et al.* published a distribution of failures of wind turbine converter components in [10] which is shown in Fig. 3, while *Alewine et al.* published the distribution for wind turbine generators in [11] and this is shown in Fig. 4.

It can be seen that for the converter, the highest failure rates are for the power semiconductor and control. For the generator, the bearings have the highest failure rates followed by the stator windings and wedges.

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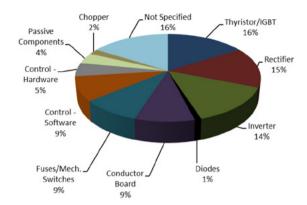


Fig. 3. Converter components failure distribution. From [10], [12].

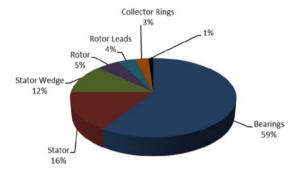


Fig. 4. Generator components failure distribution. From [11], [12].

#### III. FAILURE MECHANISMS

This section describes the failure mechanisms of the converter and generator. This is based on the review in [12].

#### A. Converter Failure Mechanisms

The components that fail most in a converter are: the power semiconductors, the control, the passives, conductor boards, and the fuses. Here, the failure mechanisms for the semiconductors, the control, and the capacitors are discussed.

1) Power Semiconductor: Power semiconductors suffer from a number of failures such as - bond wire lift-off, bond wire heel cracking, aluminium reconstruction, corrosion of interconnections, solder fatigue and voids, latch-up and cosmic ray failures among others [12], [13].

Solder joint fatigue and bond wire lift-off are the two major failure mechanisms plaguing power semiconductors. Solder joint failure occurs due to the solder layer being subjected to mechanical stress by the materials between which the solder is sandwiched. When the power semiconductor undergoes a change in temperature, the materials on either side of the solder expand to different extents due to their different coefficients of thermal expansions (CTEs). This differential expansion gives rise to the mechanical stress in the solder layer. Similarly, the different CTEs of the bond wire and the silicon they are attached to gives rise to shear stress when subjected to temperature variations which causes the lift-off of the bond wire. A variation of

the bond wire lift-off is the heel cracking where the bond wire undergoes flexure fatigue and cracks at the point of attachment to the silicon. These mechanisms are driven by temperature cycles that may be caused by thermal cycling (heating due to external sources) or power cycling (heating due to semiconductor losses).

Such temperature cycles also induce stresses on the device upper metallisation because of the CTE mismatch between it and the silicon leading to aluminium reconstruction. This becomes an issue for reliability when there are pre-existing step coverage problems at the emitter contact in the IGBT [13]. Essentially, aluminium reconstruction reduces the cross-section of metallisation resulting in an increase in the resistance of the aluminium contact.

The press-pack package technology eliminates the dominant failure mechanisms of wire bonded semiconductors like bond wire lift-off and solder joint failure. However, the differential expansion of materials under temperature cycles cause a different set of failure mechanisms such as fretting, spring fatigue and spring relaxation.

Latch-up is another failure mechanism that occurs in IGBTs. This occurs when the parasitic thyristor in the IGBT is turned on and the collector current can no longer be controlled through the gate. Static latch-up can occur due to high collector currents while dynamic latch-up occurs due to switching transients at turn off [14]. Further, failures can be initiated through self-sustaining discharges in the silicon by recoil nuclei caused by cosmic radiation. It has been shown that this is a problem for devices with a voltage class as low as 500V which makes it an important consideration for wind turbine converters [15].

The failure mechanisms and their drivers are summarised in Fig. 5.

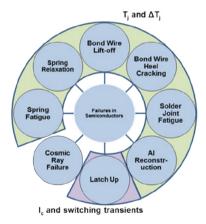


Fig. 5. Failure mechanisms in power semiconductors. From [12].

2) Control: The control unit is another component that has a high failure rate in the drivetrain. Here too the failures are driven by temperature cycles [16]. Furthermore, continued narrow overvoltage spikes between collector and emitter may open the gate-emitter resistance resulting of a loss in the driving signal and misfiring of the IGBT [16]. This can result in thermal breakdown [17].

Also, as modern IGBTs can work at much higher temperatures than the gate drive circuit components the driver circuit could suffer from the thermal effects in such a scenario.

3) Capacitor: Two types of capacitors are used in wind turbine converters - aluminium electrolytic capacitors and metallised polypropylene film capacitors. The electrolytic capacitor offers high power density at a lower cost but suffers from reliability issues, which requires them to be oversized, while the film capacitor offers higher reliability but has a lower power density [18].

Both Aluminium Electrolytic Capacitors and Metallised Polypropylene Film Capacitors have parameter degradation as a dominant failure mode. Capacitor voltage stress and temperature stress are two major causes of this failure mode while humidity also plays a role (especially for polypropylene film capacitors).

Capacitors can also suffer from short circuit failures that are a result of a breakdown, such as thermal breakdown. Propylene film capacitors can undergo a short circuit failure due to the absorption of moisture by the dielectric film.

Open circuit failures occur either due to electrochemical corrosion leading to lead fractures or the drying of capacitor cores when they are subjected to high working temperatures [19]. A further review of failures in capacitors is presented in [20]. A schematic overview of failure mechanisms and drivers is shown in Fig. 6.

#### B. Failure Mechanisms in Generators

The components that have the largest share of failures in the generator are bearings, the windings, the stator wedges, the rotor leads, and the slip ring assembly. However, this section does not discuss failure mechanisms in the generator bearings.

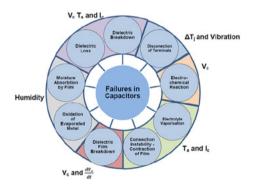


Fig. 6. Failure mechanisms in capacitors. From [12].

3.2.1. Windings: The ageing and failure of generator windings is due to thermal degradation, mechanical stress due to vibrations, electrical stress, and shear stress due to different CTEs of the winding and insulation materials [21].

Thermal ageing is a well known and modelled phenomenon. However, another factor that affects the lifetime of winding insulation is thermal cycling. This has been shown to be a factor for large generators that go through

start and stop cycles, like hydro-generators [22], [23]. Kokko et al. investigated the root causes for poor and critical condition index of hydroelectric generator stator windings and found that 38% are due to ageing by thermal cycling [22]. Therefore, it can be estimated that wind turbine generators would also be affected by thermal cycling, due to the large variations in their duties. Thermal cycling causes shear stresses between the conductor and the insulation (due to their different Coefficients of Thermal Expansions) which causes mechanical fatigue. This causes the formation of voids, which result in the breakdown of the insulation. It can be expected that the stress and hence the ageing depends on the magnitude of the temperature difference in the thermal cycle. However, further study is required to confirm the effect of this thermal cycle on the insulation lifetime in wind turbine generators.

The electrical stress experienced by generator windings is intensified by the use of PWM based converters. The PWM switching regime can cause fast travelling voltage wavefronts that generate reflected waves that can cause large voltage spikes [24], [25].

The environment can also play a role in the degradation of windings. Offshore wind turbines are exposed to moisture and corrosive salt water, both of which degrade windings. Also, DFIG based wind turbines use carbon brushes whose wear can lead to carbon deposits on the windings which may also initiate surface tracking in winding insulation.

- 2) Stator Wedges: Alewine et al. identified the loosening of magnetic stator wedge as a major failure mechanism in wind turbine generators. The benefits of using magnetic stator wedges are the smoothing of the air-gap flux, improved efficiency and reduced temperature rise [26]. With stator wedges being made out of magnetic material they will vibrate under the effect of rotating fields causing the weakening of the stator wedge bonding. Also, the ferrous nature of the wedges speeds up corrosion through oxidation [11].
- 3) Rotor leads and Slip Ring Assembly: For a DFIG based system, the power is fed to the rotor windings through rotor leads which usually run through the shaft of the generator. This can lead to thermal issues and degrade the insulation of these leads by the mechanisms discussed in the previous section. The DFIG also uses slip ring assemblies that are prone to failure. The brushes on these assemblies wear out with time, however, this wear can be unpredictable based on the operating conditions and can lead to failures. Voltage spikes can cause flash-over between rings and the insulation in these assemblies can be degraded due to thermal ageing.

### IV. IMPROVING AVAILABILITY

The availability of a wind turbine is the amount of time it is operational and produces energy in a specified period divided by the total time in that period. Availability takes into account both failure frequency and downtime into its calculation and therefore is a good measure of the power production performance of a wind turbine.

This paper reviews the methods of increasing the availability of wind turbine generator systems. For this paper, the framework focusses on three pillars or approaches:

Component Reliability - The first approach takes into account steps that can be realised at the design stage. The design aim of increasing the reliability can be achieved by:

- Eliminating components that fail.
- Increasing the strength of components/materials so that they can sustain a larger stress.
- Reducing the stress on failure prone components.

Active Control - the second approach utilises active control strategies that reduce the stress on components. Again, the focus is on increasing lifetimes of the components.

Fault Tolerance - even with the above two approaches being employed there is the chance of failure in the system. Therefore, including fault tolerance will allow the system to continue operation under fault till maintenance and repair can be done on the machine, further increasing availability.

#### V. Addressing Converter Availability

The framework for improving converter availability with the three approaches is shown in Fig. 7.

The focus in this section remains with the power semiconductors and improving their lifetimes.

#### A. Component Reliability - Power Module Level

The design for reliability can be tackled at two levels, the power module level and the converter level. At the power module level, connection techniques for interconnects and die attach are reviewed along with the baseplate design and package cooling. These aspects are shown in the schematic in Fig. 8.

1) Interconnects: Wire bonds have been shown to be a limitation for the reliability of power semiconductors. When subjected to thermal and power cycling, the flexure stress can lead to a liftoff or a crack in the heel of the aluminium bond wire; leading to failure. There are a number of methods and design choices that can improve the lifetime performance of these interconnects:

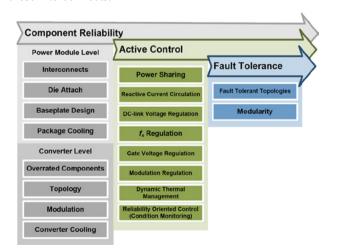


Fig. 7. Framework for increasing converter availability.

Molybdenum Strain Buffers - Bond wire failure occurs due to the stresses caused by the CTE mismatch between the aluminium of the bond wire and the silicon. This stress can be reduced by the addition of a molybdenum strain buffer soldered to the chip [27], [28]. The CTE of molybdenum is close to that of the silicon chip, which reduces the thermal stress and improves the lifetime. *Hamidi et al.* showed that the introduction of these strain buffers could increase lifetimes by a factor of 2-3 [27].

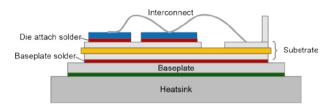


Fig. 8. Schematic of the power semiconductor module.

Copper Wire Bonding - In the heel cracking failure mechanism the crack develops in the aluminium bond wire near the semiconductor surface and propagates along the grain boundaries. An increase in the yield strength of the bond wire material will allow the interconnection to sustain the thermal stresses for a longer period of time. Copper is therefore a suitable choice and can increase the lifetimes of bond wires by an order of magnitude under certain test conditions [29], [30]. Fig. 9 shows an example of copper wire interconnects. The use of copper wires will require a change in the aluminium topside contacts on the chip. Therefore, the use of copper wires cladded with aluminium (an example for this is shown in Figure 10 for ribbon bond wires) allows the use of standard chip contacts while increasing the lifetime of the bond wires [31], [32]. Also, research on other materials, usually alloys of aluminium, as a replacement to aluminium have shown promising results [33], [34].

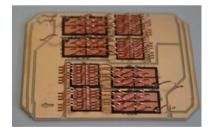


Fig. 9. Copper wire bonds on Cu metallised IGBTs. Figure from [30].

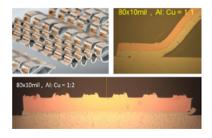


Fig. 10. Al-Cu ribbon bonds. The figure shows crosssections of ribbon

bonds with different Al:Cu thickness ratios. Figure from [32].

Ribbon Bonding - This technique makes use of rectangular ribbons of bond wire (Fig. 10) in place of the round bond wires. This allows better contact with the surface of the die area and lower thicknesses which improves the ultrasonic bonding process [35]. The study in [36] found that lifetime with a ribbon bond wire is 2.3 times that of a round wire bonded technology. This is attributed to the higher contact surface and stiffness which reduces crack propagation.

Sintered Interconnects - This technique eliminates the need for wire bonds by sintering the top side of the power chip to a connector. The connector may be in the form of flexible circuit board (Fig. 9) as in [37], [38] or planar copper interconnects (Fig. 12) as in [39], [40]. Such an interconnection gives the opportunity for double-sided cooling that can greatly increase the cooling efficiency.

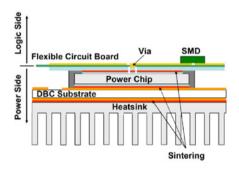


Fig. 11. Planar interconnects with flexible PCB. Figure from [38].

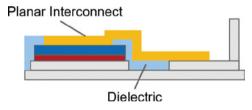


Fig. 12. Planar copper interconnects. Based on [40].

Press-pack - The press-pack technology uses pressure to obtain electrical and thermal contacts, thus eliminating wirebonds and minimising solder connections. Studies in [41] showed that press-pack IGBTs have improved lifetime performance compared to the flat-pack IGBTs. However, [42] found early failures that could be attributed to damaged gate-oxide and micro-eroding. The press-pack also addresses the solder fatigue failure mechanism.

2) Die Attach: In a power semiconductor, the silicon die is in most cases attached to the substrate by a solder layer. This introduces a failure mechanism driven by temperature cycles leading to solder fatigue. In [43] it is shown that for power cycling tests with  $\Delta T_j < 100K$  the solder fatigue failure mode dominates. Therefore, for wind power applications this failure mode should be the focus for the design for reliability approach.

There are a number of replacements for the conventional lead based solder that have the potential of improving the lifetime with respect to solder fatigue. The use of new solder material such as the lead-free tin-silver based solder in [44] can be one solution, although it brings its own challenges. Another possibility is the use of diffusion bonding which forms bonds based on intermetallics leading to improved performance against thermo-mechanical loading [30], [45]. Fig. 10 shows the cross section of such a diffusion soldering sample.

Another promising technique for the die attach is silver sintering where micro or nano silver particles are applied between the die and the substrate followed by the sintering process resulting in a metallic bond [45]. A number of studies have shown the improvement in lifetime performance of silver sintered joints compared to solder joints [45]-[48].

Further, a more focussed and detailed review on the die attach methods and materials can be found in [49].

- 3) Baseplate Design: The power semiconductors have a solder layer between the ceramic substrate and the baseplate. This layer undergoes fatigue under cycling of temperature due to the different expansions the ceramics and the baseplate undergo. This fatigue can be reduced by matching the CTEs of the ceramic substrate and the baseplate. This can be achieved by the use of AlSiC baseplates with AlN substrates. This can reduce reduce fatigue on the solder and increase lifetime [50]-[52]. However, this comes at the cost of higher temperatures due to the lower thermal conductivity of AlSiC compared to copper [52].
- 4) Package Cooling: As failures in the power semiconductor are temperature driven, effective cooling can enhance reliability. One way to do this is the use of microchannel based water cooled baseplates. [53] shows a 60% reduction in thermal resistance compared to a standard module. This can be extended to jet impingement cooling for the baseplate or the substrate itself [54] with both methods thermally outperforming modules with cold plate technology. The integration of metallic phase change material into the design of the chip silicon as in [55] or the integration at the DBC level as in [56] could also be explored. Furthermore, the use of modules designed as a sandwich between two DBC layers for double-sided cooling as in [57], [58] could

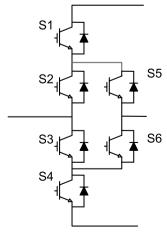


Fig. 13. 3L Active Neutral Point Clamped (3L-ANPC) topology leg. The additional switches S5 and S6 allow the even distribution of losses.

result in large improvements in thermal performance.

#### B. Component Reliability - Converter Level

At the converter level, the use of overrating, topology, modulation and converter cooling are discussed.

- 1) Over-rating: For power semiconductors, the failure mechanisms are driven by the cycling of the junction temperature and the mean junction temperature. The use of multiple parallel converters, which would overrate the switches in use, or the use of switches with a higher rating would reduce the junction temperatures and hence boost reliability. This has been explored for PV systems in [59]-[61] and can be extended to wind turbine systems.
- 2) Topology: The choice of topology can also have an effect on the lifetime of the power semiconductor. The three-level Neutral Point Clamped (3L-NPC) converter is a popular choice for large power wind turbines. This topology has an uneven distribution of losses amongst the semiconductors in each leg. Therefore, topologies that can evenly distribute the losses, and hence the stresses on the semiconductors would result in an increased lifetime of the converter. For this, the T-type and the Active Neutral Point Clamped (ANPC) topologies are promising [62].

Furthermore, the number of converter levels can be extended further than 3. This would introduce additional switching states in the operation and improve thermal performance thereby improving reliability as has been shown with a five-level converter in [63].

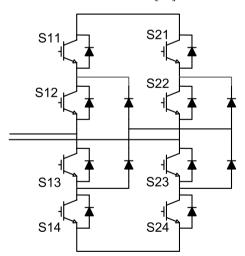


Fig. 14. 5L H-Bridge topology leg. The additional levels reduce the losses in the switches.

3) Modulation: The use of the Discontinuous PWM modulation technique can reduce the effective switching frequency of a converter and increase lifetime. This use of this modulation strategy has been shown to have a modest effect on the lifetime of the converter for DFIGs in [64]. However, the DPWM leads to increased current harmonics at low modulation levels.

The use of optimal modulation schemes can reduce switching frequencies without increasing harmonic distortion. Reducing switching frequency results in lower losses in the semiconductor which is advantageous from the point of view of reliability. The Synchronous optimal PWM (SoPWM) is one such technique that has been explored and has been shown to be successful in reducing the switching frequency without affecting the harmonic distortion [65]-[67].

4) Converter Cooling: The thermal management of the converter is important not only from the point of view of the power semiconductors, but also the other sub-components like the capacitors as well. A number of failure mechanisms in these sub-components can be linked to temperature and therefore, methods that can improve thermal management of the converter can be beneficial for the overall reliability of the converter. The power sandwich integration is one such concept [68], [69] that uses new passive components that have equal heights and are sandwiched between two substrates allowing heat transfer in both directions.

#### C. Active Control

Once the converter has been designed there are still opportunities where active control methods can be applied to reduce the stress on components.

- 1) Power Sharing: Today's large wind turbine converters are built up of multiple modular converters in parallel to handle the large amount of power they need to process. The variation of components in these converters, even within the tolerance limits, may lead to a variation in junction temperature amongst the parallel converters. This would lead to larger stresses on certain converters and drive them to premature failure. However, if the power processed by each converter is partitioned on the basis of the temperature of the components as in [70], [71], the stresses on converters can be reduced and lifetimes extended. Therefore, the control strategy is based on equalising temperatures in converters rather than current. This method is also shown to improve efficiencies compared to current sharing controls in [72].
- 2) Reactive Current Management: Today's wind turbines are required to support the grid with reactive power injection. This can have a significant effect on the lifetimes of the converters. For a DFIG based system, this reactive power injection can be achieved from the grid side converter or the rotor side converter via the stator circuit. [73] shows that injection of reactive power from the rotor side converter produces less current stress and is, therefore, better for lifetimes. Furthermore, [74] optimises the reactive power flow between the grid and rotor side converters to achieve an overall balanced lifetime.

The reactive current can further be used to minimise temperature variations in the power semiconductors of the converter. [75] explores the circulation of reactive power between the rotor side and the grid side converter of a DFIG based system resulting in lower temperature variations during normal operation as well as during gusts. [76] explores this circulation of reactive power between parallel connected converters for full converter based wind turbines

to significantly reduce temperature variations during wind gusts.

- 3) DC-link Voltage Regulation: A DC-link regulation strategy adapts the DC-link voltage to the requirement of the operating point. Such a strategy can reduce losses in the converter significantly resulting in reduced junction temperatures and therefore; increased lifetime. The DC-link voltage regulation strategy can be used in conjunction with the other methods described in this section to further increase the effect on lifetime. This has been implemented for traction drives in [77].
- 4) Switching Frequency Regulation: The losses in a power semiconductor are dependent on the switching frequency. Therefore, the control of switching frequency can be used to regulate the temperature of the device.

First, the switching frequency can be used to ensure that semiconductor temperatures remain within the safe limits. As the junction temperature rises to a set value, the switching frequency can be reduced. This would reduce losses and hence protect the semiconductor from overheating. Such a system has been proposed in [78] and for traction applications in [79].

Another regulation method uses the frequency to reduce the amplitudes of temperature cycles in converters. A hysteresis controller is used to regulate switching frequency according to the amplitude of the temperature cycling with the frequency being increased as temperature cycle amplitude reduces, leading to a smaller temperature cycle. A number of variations of this control strategy are available in [80]-[83].

5) Gate Voltage Regulation: Like with the power sharing method, the gate voltage regulation can be used to prevent thermal imbalance in parallel connected converters. This is achieved by adjusting the gate voltage or the gate resistance. [84], [85] show such systems for the thermal balance of parallel connected converters by active gate control.

Active gate control can also be used to control the amplitude of temperature cycles in the power semiconductor. [86] uses a system of switchable gate resistors such that the largest gate resistors are selected when the current is at the low magnitude points while the lowest gate resistors are used at high currents. This results in slow switching at low current magnitudes and fast switching at high currents resulting in reduced losses. The reduction in temperature cycle amplitude was experimentally validated. Apart from controlling the gate resistance, the control of gate voltage can also be used to regulate losses as proposed in [87].

6) Modulation Regulation: The Discontinuous PWM (DPWM) has been discussed in section 5.2.3 and has been used to reduce losses in a converter. Using a combination of the Space Vector PWM (SVPWM) and DPWM, the switching losses can be varied within a certain band. This can be used to reduce the junction temperature cycling amplitude. This Hybrid Discontinuous PWM (HDPWM) technique has been discussed and shown to be effective in [88]-[90].

- 7) Dynamic Thermal Management: The active control methods discussed above are based on controlling electrical parameters. Another opportunity for active control lies in the thermal management system.
- [91] proposes such a system that provides adaptive cooling where the efficiency of the cooling system can be adjusted based on the temperature of the power semiconductor. Such a dynamically controlled thermal system can reduce junction temperature cycles leading to higher lifetimes. Furthermore, active cooling regulation by control of forced air speed has been studied in [92], [93].
- 8) Reliability Oriented Control: Conventional control schemes for wind turbines are based on the extraction of maximum energy from the wind. However, considering the cost of maintenance for far offshore wind turbines, it may be important to look at reliability oriented control strategies or condition based operation that looks to maximise the availability of the wind turbines rather than maximise the power production at each instant. Such a system is conceptualised in [94], [95].

One possibility is to use a de-rated power curve to reduce the stresses on the converter or generator. For offshore wind turbines, once a failure occurs, there can be considerable time lost in the logistics of organising maintenance visits. If a de-rated power curve would result in lower stresses allowing the converter to operate for a longer period, it could result in an overall improvement in power production. This approach could be extended such that the de-rated power curve is designed to allow the operation of the converter for a longer period, wherein the component is replaced only in the next maintenance visit. These two approaches are represented in Fig. 15.

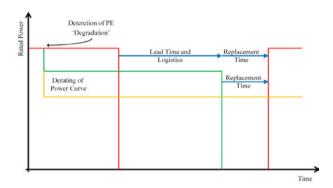


Figure 15: Opportunities for increased availability using the de-rating of power curves.

This active control technique would require inputs from the prognostics or condition monitoring mechanism.

#### D. Fault Tolerance

This section discusses two aspects of achieving fault tolerance in the converter - fault tolerant topologies, and modularity. This section is based on the review of modularity in [96] and fault tolerance in [97].

1) Fault Tolerant Topologies: There are a number of

topologies that can be used to make the converter system tolerant to faults. A review of such topologies can be found in [98]-[100]. Fault tolerant topologies use redundancy in one form or another to introduce fault tolerant capabilities.

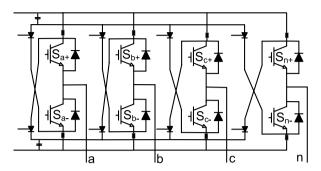


Fig. 16. Double switch redundant topology.

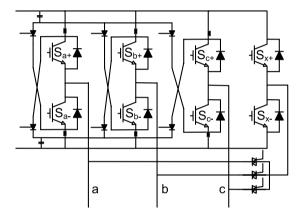


Fig. 17. Phase redundant topology.

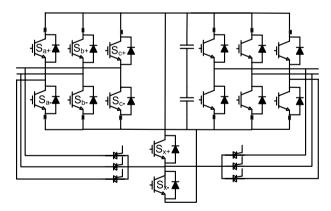


Fig. 18. Phase redundant topology with a common redundant phase leg.

The switch redundant topology introduces extra switches to the two-level converter to make it able to accommodate open phase and switch short circuit faults. The double switch redundant topology (Fig. 16) adds an extra leg connected to the neutral point of the machine. This has the advantage of making the converter tolerant to switch short and open circuits along with phase leg short and open circuits. However, the power handling capability of the topology is reduced. The phase redundant topology (Fig. 17) adds and extra phase leg that can be connected to any leg of the

machine by triggering connecting switches. This topology too is tolerant to most types of faults and is capable of handling rated power.

In back to back converters, the phase redundant topology can be used with a common redundant phase leg for both (Fig. 18), the generator side and the grid side converters [101]. This reduces the overall cost for redundancy without affecting the fault tolerant capability. Furthermore, a converter topology without redundancy but with the possibility of reconfiguration which allows operation after a switch fault as a five-leg converter is proposed in [102].

2) Modularity: This section is based on the review of modularity in [96]. The use of multiple modules in a converter also introduces a degree of redundancy in the system. In the event of a failure in a module, it can be disconnected from the system and allow the rest of the converter modules to process the generated power. As wind turbines operate at partial load for significant periods of time, such a system can be especially attractive. Modularity can be introduced in two layers - the first is the functional layer, where the modules operate as separate functional blocks. The second is the physical layer, which builds on functional modularity by adding physical separation.

[16], [103] discuss the use of six parallel converter modules for a 4.5MW turbine. The study shows that the system not only increases efficiency and reduces grid harmonics, but it also boosts availability when mean time to repair is considered. [104] shows the improvement in reliability with modular converters using Markov models.

One method of increasing the modularity of the system is the use of tooth wound concentrated modular windings with a converter unit. This system brings in modularity both in the converter unit and the generator unit. There have been a number of applications where such a system has been employed as a means of incorporating fault tolerance. [105]-[107] uses this design concept for traction applications and [108] uses this for aerospace applications.

With a high level of physical modularity, such as with modular stator windings with independent H-bridge converters for each coil, there is an opportunity to design compact converters that would reduce replacement costs. Converter modules can be designed so that they can be replaced by a single worker without heavy lifting equipment. This would increase the maintainability of the converters and increase the availability of the converter system [96].

#### VI. Addressing Generator Availability

The framework for improving generator availability is shown in Fig. 19.

#### A. Component Reliability

Considering the major sources of failure in the generator, this section discusses design solutions for the magnetic stator wedges, slip ring assemblies, winding insulation, bearings, and cooling systems.

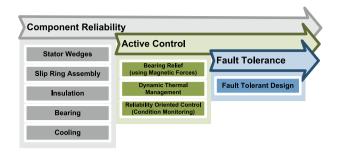


Fig. 19. Framework for increasing generator availability.

1) Magnetic Stator Wedges: A study of failures of wind turbine generators and found that approximately 15% of failures in generators rated above 2MW were due to stator wedges [11]. One explanation of this is that when magnetic stator wedges are used, they are subjected to pulsating forces which speed up the failure process.

Magnetic wedges offer a number of improvements to machines resulting in increased efficiency [109], [26], [110]. However, looking at their propensity to failure in wind turbines, it may be important to look at their impact once again. In this paper, analytical models were used to compare the performance of wind turbines with and without magnetic wedges based on generator designs in [111]. The comparison includes the DFIG with a three stage gearbox, and the permanent magnet direct drive. The results of this comparison are shown in TABLE I.

These results show that the advantage offered by the inclusion of magnetic wedges is small. Therefore, replacing the magnetic wedges with non-magnetic wedges could increase reliability without a large effect on energy production, leading to a net reduction in Cost of Energy (CoE).

TABLE I:
EFFECT OF MAGNETIC STATOR WEDGES ON ELECTRICAL
PERFORMANCE.

	DFIG 3-stage Gearbox	PM Direct Drive	
Without Magnetic Stator Wedges			
Annual Energy Yield (GWh)	7.73	8.04	
With Magnetic Stator Wedges			
Optimal wedge Annual Energy Yield (GWh)	9.1 7.73	10 8.05	
Difference in Annual Energy Yield (MWh) Equivalent hours of Energy Production		8.42 9.16	

2) Slip Ring Assembly: The brush and slip ring assembly is a major contributor to failures in DFIG based wind turbine systems. According to [112], more than half the failures in DFIGs are brush-slip ring failures. Even though more than half these failures are classified as minor repair based, for far offshore wind turbines minor failures can be very expensive

as well. This failure mode can be addressed by either doing away with the slip ring system or by improving the design such that it fails less often. Apart from the slip ring in the generator, turbines that use electrical pitch actuators require power transfer to the rotating hubs thereby requiring slip ring assemblies as well.

Brushless DFIG - The B-DFIG is yet to be commercialised for use in wind turbine generators. A 250kW has been designed and tested in [113]. The B-DFIG eliminates the need of brushes and slip rings. This can be especially beneficial for wind turbines in offshore applications. Due to the structure of the B-DFIG design, it has higher values of leakage inductance, which results in lower efficiencies [114]. However, the trade-off between higher reliability and lower efficiencies needs to be explored further. Another advantage of the B-DFIG is its improved low voltage ride through capability [115]. The B-DFIG is able to handle low voltage events without the use of an extra crowbar circuit. Therefore, the power electronic converter is protected without the use of extra components, improving reliability.

Brushless Excitation - The slip ring assembly can also avoided by the use of brushless excited machines. Apart from the permanent magnet synchronous machine, the use of rotary transformers for contactless power transfer to the rotor is also a solution. Examples of the design of such systems can be found in [116], [117].

Lubricated Slip Ring Assemblies - In sliding contacts, the conduction takes place across an insulating film (which is a moisture film in many applications) by the tunnel effect. In the absence of such a film, the two clean metallic surfaces will cold weld such that the surfaces will be destroyed during sliding and the wear on the brushes will be very high [118]. One of the ways of improving the wear resistance of the brush-slip ring assembly is by the use of boundary lubrication. This is done through the formation of thin films on the contact surfaces that do not strongly affect the current but reduce the wear [119]. The use of oil that is a suspension of conducting particles has been shown to have good results [120]. Apart from improving the wear characteristics, a good lubricant could damp vibrations leading to lower noise levels in the transmitted signal (this is more important in the use of slip rings for signals and instrumentation) as well as act as protection against corrosion of the slip ring assembly. As wind turbines, especially those erected offshore, operate in harsh and corrosive conditions (salt spray etc.) protection from corrosion is an important aspect of lubricants in slip ring assemblies for wind turbines.

3) Insulation: Thermal degradation is a dominant factor in the ageing of electrical machine winding insulation systems [121], [122]. Lifetimes of insulation can be estimated using the Arrhenius rate law. The thermal class of the insulation has an effect on the lifetime. Therefore, using an insulation with a higher thermal class would increase the life expectancy of the insulation.

The use of PWM based converters can cause electrical stresses in the insulation due to the voltage spikes created

by the fast front voltage waves [24]. Further, this large dV/dt due to switching of the converter can give rise to large capacitive currents in the insulation, and voltage gradients in within windings. [123] gives an overview of possible solutions for relieving these stresses. These solutions could be design choices like the length of connecting cables, the switching speed, the machine insulation material as well as the use of additional components like filters.

4) Bearings: Bearings are a major reason for failures in wind turbines. The causes of failure may be due to problems in lubrication, contamination, misalignment etc. The solutions to such problems are beyond the scope of this paper.

However, another reason for accelerated bearing wear is bearing current. These bearing currents can be produced by high motor frame voltage due to common mode current, high frequency axial shaft voltage due to circumferential magnetic flux around the motor shaft, the coupling of common mode voltage via the bearing capacitances [124]. It is possible to prevent the discharge of current through the bearings by using insulation in the bearings or by creating alternative paths for the current like using a grounding brush [124], [125]. Furthermore, converter design to minimise the common mode voltage can also help reduce bearing currents [126].

Eccentricity in the machine rotor may be caused by a manufacturing defect or from wear in the bearings. This eccentricity causes Unbalanced Magnetic Pull (UMP) which can further effect an increase in bearing wear. This UMP is damped to some extent by the cage in the caged induction machines and by the pole dampers in synchronous machines [127], [128], however, wound rotor machines (like the DFIG) can still benefit from the addition of damper windings. The use of stator damper windings to attenuate UMP in induction machines has been investigated in [129].

5) Generator Cooling: As the temperature is the main driving factor for insulation ageing, improved cooling systems for generators would prolong lifetimes of windings. Liquid cooling is one such technology that can give good results. Many high power wind turbines today already use liquid cooling for the generator and converter [130]. This cooling performance may be improved by using hydrogen cooling as in [131].

Another possibility is to use liquid flow within the stator winding to remove heat. This uses hollow conductors which allows the cooling liquid to flow within them and remove heat straight from the source. Such a system has been proposed in [132] and [133].

#### B. Active Control

This section looks at opportunities for reducing stress on components of the wind turbine generator.

1) Bearing Relief: The issues with bearings have already been discussed in Section II. It is evident that improving the life of bearings can have a major impact in improving the availability of wind turbines as they account for the highest downtime for any wind turbine component [8].

One of the ways of addressing the bearing failures is the use of the inherent magnetic forces in the machines to reduce the load on the bearings and hence accomplish bearing relief. For large direct drive generators, the weight of the rotor is carried by the generator bearings. The use of magnetic forces to take this load off the mechanical bearing would reduce their wear and hence increase their lifetime. Here, the weight of the turbine and the moments generated by it would have to be handled. The reduction of bearing forces can be achieved by using a number of methods of which the use of passive damper windings has been discussed in section the Part 4 of Subsection A in Section VI,

Control Windings - One possibility is the use of an additional winding in the stator which can be controlled to produced the required radial forces. This may be compared to a magnetic bearing or bearingless machine, however, the idea here is to keep the mechanical bearing and only use the additional winding to reduce the load on the bearing thus reducing the load handled by such windings. One of the disadvantages of such a system is the additional need for control. This would require the addition of power electronic converters, controllers and sensors [134]. A system that uses additional windings to generate radial forces and cancel the rotor weight to effect bearing relief has been investigated in [135].

Active Generator Control - Another option is the use of control schemes in existing machine systems to reduce the rotor radial forces [136]. This would have the advantage of not requiring additional windings, however, it would make the control of the machine more complex. The use of modular machine concepts (with tooth wound generators with independent h-bridge converters for each turn) could be extended to include active generator control to counteract the weight of the rotor and reduce the load on the bearings. The use of sensorless control would also reduce the need of sensors and have been proposed in [137], [138] for small bearingless machines.

Furthermore, the use of active magnetic force control in modular generators also afford the opportunity to counteract dynamic bearing forces that may arise, for example, due to wind gusts. The challenge here is being able to measure the stress in the bearing system to be able to counter them.

- 2) Dynamic Thermal Management: It has been discussed in Part 1 of Subsection B in Section III that temperature cycling of the winding could lead to accelerated failure, therefore, dynamic thermal management as discussed for the converter in Part 7 of Subsection C in Section V could reduce the temperature cycling.
- 3) Reliability Oriented Control: Reliability based control or condition based operation has been described in Part 8 of Subsection C in Section V and can be used to extend the lifetime of generator components as well. [139] explores a prognostics based life extension methodology for generation systems and focusses on the bearing system.

#### C. Fault Tolerance

This section is also based on the review of modularity in [96] and fault tolerance in [97]. For a machine to be tolerant to its failures, it has to satisfy certain requirements [140],

Electrical Isolation - To limit the effect of the faulty winding on the healthy part of the machine, the different 'modules' of the machine should be electrically isolated. For modular systems that use independent converters for each module (be it a single coil or three phase coil module) this requirement is already built into the design.

Limiting Fault Current - If the short circuit fault occurs at the machine winding terminal or in the converter, both scenarios could result in a very large currents. To limit the fault current, stator phase inductance has to be designed to be close 1 pu inductance so that fault current is limited to the rated value. Furthermore, techniques for reducing the short circuit current by using magnet subdivisions have been investigated in [141], [142].

Magnetic Isolation - Fault current will induce a voltage in the neighbouring phases, because of the presence of mutual inductance between phases. This would make control of the machine difficult. To reduce the effect of one phase on another, the mutual inductance between phases or modules must be small.

Thermal Isolation - Short circuit current can produce large amounts of heat in the slot, therefore, thermal isolation between the different windings is recommended. Modular stator windings with a single coil in each slot would serve this need well.

The use of a modular design with a distributed control architecture with multiple processors would allow operation under the failure of control modules as well. The addition of physical modularity to the generator design by using segmented cores introduces the ability of a core module of the generator being replaced in case of any winding failure. Stator winding failures account for about 20-30% of all generator failures [11]. These failures are expensive to fix and take considerable time. According to [8], a generator failure averages about 150 hours of downtime. The use of segmentation would reduce the time and cost of faulty winding replacement. Physical modularity in the form of segmentation could, therefore, be especially attractive for offshore wind turbines [96]. Such a system is proposed in [143] where the direct drive PM generator is constructed from physically separate E-core modules as shown in Fig. 20.

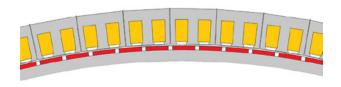


Fig. 20: Physical modularity in the generator.

Fault tolerance can also be included by the use of multi-

ple phases. [144] describes an AC drive with multiple independent phase driving units. For wind turbines, such a multiple phase system with nine phases constructed with classical three phase converters was described in [145].

#### VII. PROMISING RESEARCH DIRECTIONS

The previous sections have reviewed some methods that aim to increase the availability of wind turbine generator systems by the design for component reliability, the active control for reliability, and the design for fault tolerance approaches. This section highlights those methods that the authors are working on and consider promising directions for investigation.

Converter Design for Reliability - The use of design concepts at a converter level to increase reliability can be applied to commercially available power modules. Even with advancement in power module technology, the failure mechanisms are still driven by thermal and power cycling (the examples being press-pack technology, silver sintering methods etc.). Therefore, with the advances in power module technology, these design concepts will only help boost the reliability of the converter (until other failure mechanisms become the limiting factor in reliability).

A number of avenues for further research exist in this field. First, a comparison of the effects of overrated components and overrated topologies on the lifetime of the converter is required. This will allow the identification of an optimal topology from the point of view of reliability. Further, the use of dynamic switching strategies that distribute the losses based on the temperatures of the semiconductors can be investigated.

Dynamic Thermal Management - Many active control methods use the control of electrical parameters to reduce the amplitude of temperature cycles in the junction of the power semiconductors ( $\Delta\,T_j$ ) and increase the lifetime. The essence of this concept is to increase the losses when the junction temperature is low so that  $\Delta\,T_j$  is reduced. However, the reduction of  $\Delta\,T_j$  can also be achieved by controlling the effectiveness of the thermal circuit. Without the need to increase losses, this method has the potential of improving the lifetime without considerable effect on the efficiency of the converter. The case for the use of dynamic thermal management is further strengthened by the fact that a majority of wind turbine converters already use liquid cooling. Therefore, aspects of this method can be included into the design without major re-engineering.

There are a number of opportunities for research in this field. First, different configurations that are possible need to be identified and evaluated. One possibility is the use of the generator as thermal capacitance by the integration of the converter and generator cooling circuits. This could be used to counter medium term temperature cycles. Another possibility is the use of differential heat production in separate parts of the component for dynamic thermal management i.e. use heat from one place to reduce thermal efficiency at another.

Fault Tolerance with Modularity - Systems, no matter how well designed, can suffer from random failures. This is more so in the case of complex systems like wind turbines. Therefore, the use of fault tolerant design can play an important role in increasing the availability of such systems. Modularity is interesting because it is already used to some extent in large wind turbine generator systems. Furthermore, the use of modularity can benefit other aspects such as maintainability and the installation of generator systems.

This area of research presents a number of opportunities some of which have been listed in [96]. These include: the design of compact physically modular converters that can be replaced by a single worker without heavy lifting equipment, a detailed investigation of physically modular generator topologies for use in wind turbines, and the optimal sizing of generator modules considering electrical, structural, and post fault performance. Further, as the converter has a majority of the failures when compared to the machine winding, it must be investigated if the generator needs to be designed for fault tolerance.

#### VIII. CONCLUSIONS

The increased availability of wind turbine generator systems is based on five pillars - design for component reliability, active control for reliability, design for fault tolerance, prognostics, and design for maintainability. This paper has reviewed methods focusing on the first three pillars and identified a few promising directions for further research. With a holistic approach based on these five design approaches, methods can be adopted at each level such that they result in the required availability with an acceptable increment in the cost.

Further, the following conclusions are made for the wind turbine power electronic converter:

A majority of the failure mechanisms are driven by junction temperature and the amplitude of junction temperature variation. Therefore, the methods described under the design for components reliability and the active control for reliability approaches focus on these issues.

Methods for design for converter reliability are promising because they address reliability at a system level and can be applied with advancing technology as long as temperature is the driving factor in failures.

Dynamic thermal management reduces the amplitude of junction temperature cycles without significantly increasing the electrical losses. Furthermore, a comparison of electrical parameter control and thermal control based on the improvement in the lifetime as well as the electrical performance is required.

Reliability oriented control (or condition based operation) can be used to reduce the maintenance costs by allowing operation of the converter until the next scheduled maintenance visit. Thus, removing the need for unscheduled maintenance visits.

Fault tolerance through modularity is also promising because apart from the advantage of fault tolerance, it can improve the maintainability of the converter.

Also, the following conclusions are made for the wind turbine generator:

Choices in the design of the generator can have a large impact on the reliability of the generator. The examples of this are the use of non-magnetic stator wedges, and the use of brushless excitation.

Bearing relief from the dynamic forces could be an important step in improving the lifetime of generator bearings. However, the real-time identification of the stresses is a challenge that has to be overcome for this.

Dynamic thermal management can be used to reduce temperature cycling stresses on the winding insulation. However, further studies are required to confirm the effect of the temperature cycling stresses on the insulation lifetime in wind turbine applications.

Modularity in the generator system can be used to improve maintainability as well as the ease of installation. However, the trade-off between the maintainability, the electrical performance, and the structural requirements needs analysis.

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## Past, Present and Future Trends of Non-Radiative Wireless Power Transfer

S.Y. Ron Hui

Abstract—Although non-radiative wireless power transfer (WPT) was invented over a century ago, it has regained research and development interests in 1980s. Over the last 15 years, WPT has appeared as an "emerging" technology that has attracted wide-spread attention in both academia and industry. Because of the long history of WPT research and developments, researchers of the modern days often do not know some historical milestones of WPT. This paper aims at providing a brief history of some key concepts and technologies that pave the way for modern WPT research and applications. A few misconceptions of WPT technologies are particularly highlighted so that new researchers entering this research field can avoid such pitfalls. Finally, some discussions on present and future trends of WPT are included.

*Index Terms*—Wireless power transfer, magnetic resonance, inductive power.

#### I. Introduction

THE scientific breakthroughs of the French Scientist André-Marie Ampère (1775-1836) and English scientist Michael Faraday (1791-1867) in early 19<sup>th</sup> century laid down the foundation of electricity and electromagnetism. The Ampere's law, Faraday's law and electromagnetism form the pillars of modern electrical engineering. Their work was further enhanced by Scottish scientist J.C. Maxwell who developed the well-known Maxwell's equations for electromagnetic fields and waves. These scientific principles became the tools for early WPT pioneers, such as Tesla, Hutin and Leblanc [1]-[3], to explore WPT through the use of coupled alternating magnetic field.

Among early WPT pioneers, Nicola Tesla was undoubtedly the most influential scientist/engineer in WPT research. Tesla was recognized as a highly visionary inventor who was well ahead of his time [4], [5]. His many inventions such as a.c. machines, ac power generation and transmission, radio transmitters and receivers, X-ray machines and the world's first remote-controlled technology have been used for over a century. Although some of his inventions have been improved over time with the availability of more advanced technologies, their basic concepts are still being used every day in modern societies.

Between the WPT research of Tesla in late 19<sup>th</sup> century to

mid 1980s, while research in WPT was still active in medical implants, commercial applications of WPT was not wide spread. Tesla pointed out that WPT could take place through magnetic coupling at high frequency and under resonance conditions. To maintain high energy efficiency, WPT requires (i) windings with low resistance at high frequency operation and (ii) a high-frequency power source. While Litz wires have become available since 1950s, high-frequency switching power electronics switches (namely power mosfets) only became commercially available in 1980's. The availability of high-frequency power sources based on power electronics technology certainly makes it easy to realize economically the high-frequency power source in a compact form. Such historical developments of Litz wires and power electronics explain why research in magnetic resonance based WPT took off for medical implants [6], [7] in late 1980s and electric vehicles and inductive power pickups in mid 1990s [8], [9]. The dawn of the mobile phone era in mid 1990s also prompted active research in wireless charging for portable electronics [10]-[15]. Reviews of near-field WPT for a range of applications starting from low-power consumer electronics [16] to relatively high-power inductive power pickup systems in manufacturing industry [17] have been reported.

The publicity of an article by the M.I.T physics team in Science [18] about the use of a 4-coil WPT system to power a light bulb over a distance of 2m in 1997 is an important factor that raises intensive interest in WPT in late 1990s. For high energy efficiency WPT, the authors of [18] claimed the use of magnetic resonance and identified a "strong coupling" regime as:

$$\kappa / \sqrt{\Gamma_1 \Gamma_2} >> 1$$
 (1)

where the symbol  $\kappa$  is related to the mutual coupling

coefficient 
$$k$$
 as  $\kappa = \left(\frac{\omega}{2}\right)k$ ;  $\Gamma_1 = \frac{\omega}{2Q_1}$  and  $\Gamma_2 = \frac{\omega}{2Q_2}$  are the

intrinsic loss rates of the first resonator and the second resonator respectively. Here, k is the mutual coupling coefficient,  $\omega$  is the angular frequency,  $Q_1$  and  $Q_2$  are the quality factors of the two magnetically coupled windings. According to [18], the condition of (1) is "a regime of operation that has not been studied extensively". Equation (1) can be expressed in standard electrical engineering terms as:

$$\frac{\kappa}{\sqrt{\Gamma_1 \Gamma_2}} = \frac{\left(\frac{\omega k}{2}\right)}{\left(\frac{\omega}{2Q_1}\right)\left(\frac{\omega}{2Q_2}\right)} = k\sqrt{Q_1 Q_2} \tag{2}$$

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It can be seen that the term  $\kappa/\sqrt{\Gamma_1\Gamma_2}$  of the coupled mode theory is equal to  $k\sqrt{Q_1Q_2}$  in electric circuit theory. Thus,  $\kappa/\sqrt{\Gamma_1\Gamma_2} >> 1$  simply means  $k\sqrt{Q_1Q_2} >> 1$ . The idea of ach ieving high energy efficiency in WPT through the maximization of the product of the mutual coupling and quality factor (i.e. kQ) has been a well-known concept for many decades. Several research teams have independently studied the WPT equations based on the coupled mode theory and transformed them in standard electric circuit theory [19]-[21]. Their analyses are consistent that the work in [18] can well be explained in standard circuit theory. The idea of achieving high energy efficiency in WPT through the maximization of the kQ product has been a central principle among power electronics researchers for decades. For short-range applications in which magnetic coupling is relatively large (i.e. with a large k), winding with reasonably high Q-factor will lead to high efficiency. For mid-range applications in which k is a small value, a very high O-factor is needed in the magnetically coupled windings.

The fact that such a well-established electrical engineering concept has become a factor to spark off new research interests in WPT is intriguing. One obvious reason is the lack of relevant WPT background among researchers who recently joined this research field. It is the objective of this paper to highlight some historical facts and R&D activities relevant to high-efficiency WPT concept expressed in (2) and explain such well-established idea has been used for decades and is still being used in modern WPT applications [22]. Remarks on the current status and future trends of WPT are also included in this paper.

#### II. THE PAST

## A. Magnetic Resonance was well established in Tesla's works

Since the end of the 19<sup>th</sup> century, "resonance" was a common theme in several aspects of Tesla's such as radio and TV transmitter and receiver circuits. The use of inductive-capacitive (LC) resonant circuits was the basic concept adopted in many of Tesla's high-frequency works. In his 1893 lecture delivered to the Franklin Institute, Philadelphia [23], he experimented with "condenser in series with the self-induction". (Note: condenser is equivalent to capacitor in modern electrical engineering term.). This inductive-capacitive (LC) resonant circuit was fed by a high-frequency alternator. To achieve resonant operation, he remarked that "both capacity and self-inductance were adjusted to suit the dynamo frequency". This means that the inductance and capacitance values of the LC circuit were tuned to suit the frequency of the voltage excitation.

In Tesla's time, high-frequency power generator was not commercially available because high-speed power semiconductor switches had not been invented yet. Historical records show that Tesla developed his high-frequency power source based on generators with a high number of pole pairs. In the article of his high-frequency tests [23], the frequency was set in the range of 5 kHz to 10 kHz. Among various WPT circuits tested by Tesla, two examples are shown in Fig. 1(a) and Fig. 1(b). In Fig. 1(a), a condenser (i.e. a capacitor) is connected across the primary coil (P) to form a parallel resonant circuit, which wirelessly transmit power to the secondary coil (S). The two output terminals of S are labelled at T.

In Fig. 1(b), the high-frequency voltage generator is fed to a transformer, the outputs of which are connected to the transmitter circuit of the system. The transmitter circuit comprises two parallel condensers are connected in series with the primary coil (P). This arrangement forms a primary series resonant tank. In the receiver circuit, each end of the secondary winding (S') is connected to two parallel plates (labelled as t and t') that form a variable capacitor. This arrangement forms a secondary series resonant circuit. In modern terminology, this system setup is equivalent to a magnetically coupled seriesseries resonant WPT system. The equivalent circuit of such series-series resonant WPT system can be described in Fig. 2. The use of a series capacitor in both of the transmitter and receiver circuit serves to reduce or cancel the reactance in the power flow path, i.e.  $\omega L$ -1/( $\omega C$ )=0, if the operating frequency is set at the resonant frequency of the LC resonant tank. How to use or design the resonant capacitor depends on applications. For relative low frequency, e.g. up to a few Mega-Hertz, a discrete capacitor components of low capacitance is needed. But for very high frequency operation, e.g. exceeding a few Mega-Hertz, the parasitic capacitance of the transmitter and receiver coil could form the required resonance capacitor. But the equivalent circuits in both cases are identical in theory.

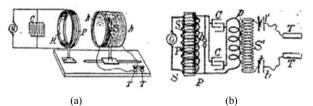


Fig. 1. One WPT setup based on magnetically coupled series-series resonant circuits tested by Tesla [23].

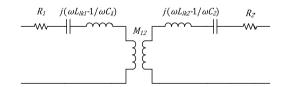


Fig. 2. An equivalent circuit of a magnetically coupled series-series resonant circuit

## B. Use of High Quality Factor and high kQ products in WPT have been well-established concepts

The concept of Quality factor was popularized by K.S. Johnson in 1914 as the ratio of the reactance to the effective resistance in a coil or a condenser according to an article entitled "The story of Q" published in 1955 [24]. The Q

factor for an inductor is:

$$Q = \frac{\omega L}{R} \tag{3}$$

where  $\omega$  is the angular frequency, L is the inductance and R is the winding resistance. It is interesting to note that a very high Q value of 1000 was considered in 1955 [24]. A relative recent investigation into WPT with a Q factor up to 1000 was also considered in a study published in 2006 [25].

Back to Tesla's work reported in 1898 [23], he explained the operation of the system with the emphases on the use of

- (i) high frequency,
- (ii) winding resistance as low as possible;
- (iii) the importance of establishing synchronism between the oscillations in the primary and secondary circuits.

The first two points technically refer to the use of a large  $\omega$  and a small R for equation (2). Therefore, the essence of his descriptions on the operating conditions essentially means the requirements for a high Q factor, although Q factor might not a popular technical term in 1898.

From early 1960s to present, the principles of magnetic resonance and maximization of the kQ product have been central to WPT for medical implants and power electronics applications. In 1961, John Schuder and his team [26] used magnetically coupled resonant circuit for wireless power transfer through the chest wall of an animal to power an artificial heart. The equivalent circuit is shown in Fig. 3. Schuder reported that the power loss was inversely proportional to the product of the mutual coupling coefficient (k) and quality factor (Q) of the receiver coil. Since the power loss is inversely proportional to the energy efficiency ( $\eta$ ), Schuder's discovery led to the important understanding that:

$$\eta \propto kQ$$
 (4)

By 1970, Schuder managed to use series resonant tanks in both of the transmitter and receiver circuits to transfer over 1 kW through animal skin based on similar principle [27]. High Q factor was achieved by using litz wire and an operating frequency of 470k Hz.

The idea of achieving high energy efficiency through maximizing the kQ product has been central to both medical and power electronics research communities for many decades. The transmission distance is inversely proportional to k. Thus, the only way to increase WPT energy efficiency for a given distance is to increase Q. Tesla's suggestions of using high-frequency operation and winding resistance as low as possible in fact pointed to the same principle. This important principle applies to both short-range and midrange WPT applications.

If the quality factors of the two magnetically coupled windings are not identical, E.S. Hochmair in 1984 shows that the kQ product becomes [28]:

$$kQ \text{ product} = k\sqrt{Q_1Q_2}$$
 (5)

where  $Q_1$  and  $Q_2$  are the quality factors of the two windings. The operating frequency was set at 11.7 MHz in [28]. If the two magnetically coupled windings are identical, (5) will converge to (4). A detailed analysis of the energy efficiency of a WPT system with non-identical coupled coils can also be found in [29].

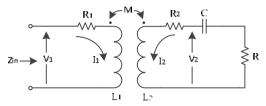


Fig. 3. A magnetically coupled resonant circuit used for WPT in [27].

C. Examples of Magnetic Resonance application in short-range WPT systems

While WPT can in principle be classified as magnetic induction and magnetic resonance, it is important to note that most of the WPT activities over the last century involve primarily magnetic resonance. Magnetic induction is used only in a few applications such as wireless charging stands for electric tooth brushes. Magnetic induction based applications typically share the common features of having high coupling coefficient and the receiver coil fixed in position. These applications essentially treat the magnetically coupled transmitter and receiver coils like a pair of transformer windings.

Among WPT works conducted since 1960s, magnetic resonance and high kQ product have been common knowledge central to WPT research and applications in medical implants, mobile robots, inductive pickups, and Qi-compatible consumer electronic products. In particular, WPT research works published by the power electronics community since 1980s are based on magnetic resonance. The exact operating frequency is usually slightly higher than the actual resonance frequency of the resonant tanks. The reason is to utilize the advantage of magnetic resonance and at the same time achieve soft-switching for the power inverter used in the transmitter circuit. A few examples are listed as follows:

- 1990 A. Ghahary and B. Cho [7] used magnetic resonance technique to transfer 48W in a loosely coupled transcutaneous energy transmission. The coupling coefficient is 0.1 and the operating frequency is 53 kHz. The system energy efficiency was 72%. The power capability was expanded to 150W in 1992 [31].
- 1994 A.W. Green and J. Boys [8] pioneered the inductive power transfer (IPT) systems for the manufacturing industry. Such WPT technique based on magnetic resonance has now become a major industry [31]. The IPT systems are now commonly used in the production lines in clean rooms for the integrated circuit industry. Similar

ideas are being expanded into R&D activities for static and dynamic wireless charging of electric vehicles.

- 1999 S.Y. Hui and S.C. Tang [32] demonstrated that power and signal could be transferred between two planar printed coils based on magnetic resonance without using magnetic core. Such coreless printed-board transformer became the first embeddable electrical isolation transformer in industrial gate-drive circuits for power electronics switches [33]. It was later used for wireless charging of mobile phone [13]. When turned into a multilayer array structure, this concept led to the first wireless charging pad with free-positioning feature for portable consumer electronic devices [34].
- 2000 Y. Jang and M. Jovanovic [12] developed a series-series resonant system to wirelessly charging mobile phones for a wide voltage range. Frequency control technique was used to maintain constant power flow. For 4.5W, a system energy efficiency exceeding 70% was achieved.

#### D. Use of Magnetic Resonance for mid-range WPT

The use of magnetic resonance for mid-range WPT application is not new. A 1937 article [35] explains an experimental setup (Fig. 4) installed in the Franklin Institute, Philadelphia where Tesla had given his WPT lecture. The circuit on the left-hand side of Fig. 4 is the transmitter circuit, which consists of a driving loop and a resonator coil (called antenna in [35]). The receiver circuit is on the righthand side. It can be placed with a variable distance from the transmitter circuit. The receiver circuit consists of a receiver resonator coil which is connected to an adjustable condenser so that the idea of tuning the resonance frequency for optimal power transfer can be demonstrated for different distances between the transmitter and receiver resonant coils. The operating frequency was 100 MHz. The dimensions of the transmitter and receiver resonator coils are 0.75m. This setup was used to demonstrate WPT over a distance up to 3 meters for powering a light bulb. So this is a setup suitable to demonstrate the short-range and mid-range WPT.

The idea of using a driving loop to couple with the transmitter resonator coil is an important concept. In fact, the 4-coil system presented in [18] uses one driving loop coupled to the

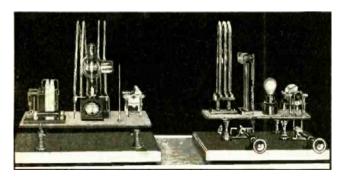


Fig. 4. Mid-range WPT setup in the Franklin Institute, Philadelphia [35].

transmitter resonator coil and a load loop coupled to the receiver resonator coil. But the original idea of coupling the resonator coil with a loop actually came from [35].

#### III. THE PRESENT & FUTURE TRENDS

As mentioned previously, the availabilities of Litz wires and modern power electronics have provided the needed technologies for WPT. The IPT systems have been deployed in manufacturing facilities. Because each manufacturing facility may be different from the others, there is so far no need to form an international standard for IPT systems. However, the situation is quite different for wireless charging of portable consumer electronics. With different mobile phone manufacturers using their own proprietary charging protocols in the 1990s, there was an obvious need from the consumers' point of view that a common charging standard should be adopted. The number of chargers manufactured in 2013 exceeded 2 billion. In an estimation made in 2009 [36], an annual reduction of about 51 000 tons of chargers would be achieved if a common charging protocol was adopted. Standard approaches can be adopted in the both wired charging and wireless charging.

The GSM association has made tremendous efforts in this regard for the wired approach. So far, the majority of the mobile phone manufacturers have agreed to use the mini-USB as the standard wired charging protocol. While this is very good news to the environment, consumers should be aware that there are still major mobile phone manufacturers which not only continue to use their own proprietary charging protocols, but they keep on changing them with new models so that consumers have to keep on buying new chargers. Consumers should exert their power to support manufacturers that adopt sustainable policy in their product designs.

## A. The Evolving "Qi" Standard by Wireless Power Consortium

Founded initially with 8 companies in November 2008 [37], the Wireless Power Consortium (WPC) has grown to include over 220 companies worldwide by October 2016. The WPC launched the world's first wireless charging standard "Qi" (pronounced as Chee) in August 2010. So far, this is the most successful wireless charging standard in commercial terms because over 790 "Qi-certified" products have been registered with WPC by October 2016, let alone many other products claimed to be Qi-compatible, Qi-compliant or Qi-approved.

The expanding applications and power capabilities of wireless charging are reflected from the evolution of the Qi standard. Based on the information from the WPC website [38], the Qi standard has evolved from version 1.0, 1.1 to 1.2. The main features of these three versions of the standard are tabulated in TABLE I. The current version of the Qi specification has version number 1.2.2. The operating frequency range of Qi is within 105 kHz to 205 kHz. This frequency range has been adopted in switched mode power

supplies for over 3 decades. System energy efficiency above 70% can generally be achieved at full load. The Qi standard covers primarily short-range WPT applications. The receiver coils of the loads are placed in close proximity of the transmitter coils. The transmission distance is up to about 4cm. Consequently, the magnetic flux for WPT is essentially enclosed and thus human exposure to electromagnetic radiation is usually not an issue. The recent inclusion of foreign object detection (FoD) is another important step forward in enhancing safety.

## TABLE I SUMARY OF THE KEY FEATURES OF THE VERSIONS OF QI STANDARD [38]

#### Version 1.0

- Qi transmitter delivers 5 Watt power into a Qi phone.
- Choices of transmitter designs include single coil transmitter, coil array transmitter, and moving coil transmitter.
- · High flexibility in design of Qi receivers.
- · Limited flexibility in the design of Qi transmitters.

#### Version 1.1

- Increased design freedom for transmitters. One can now choose between 12 different transmitter specifications.
- Increased sensitivity of "Foreign Object Detection". This prevents heating of metal objects in the neighborhood of an active transmitter.
- The possibility to power a Qi transmitter with a USB charger.

#### Version 1.2

- Fast charging. The possibility for transmitters to deliver up to 15 Watt power and the option for receivers to obtain up to 15 Watt.
- · An improved thermal test for transmitters.
- Improved timing requirements.
- · Changed limits for Foreign Object Detection.
- Optional unique identifier for power receivers (WP-ID).

#### B. Charging Standard by AirFuel Alliance

After the establishment of the WPC, alternative organizations have been formed with the hope of setting up wireless charging standards to cover other forms of WPT applications. Formed in 2012, the Power Matters Alliance (PMA) and the Alliance for Wireless Power (A4WP) were two examples. In 2015, PMA and A4WP merged together to form the AirFuel Alliance [39]. It should be noted that there are overlaps of memberships between the AirFuel Alliance and the WPC.

Different from the WPC which focuses primarily short-range applications, the AirFuel Alliance was set up to develop and maintain the standards for a form of wireless power that allowed additional spatial freedom. The aim was to develop a standard that could simultaneously charge a multiple devices, ranging from low-power bluetooth devices to laptop computers and also covering both short-range and mid-range applications. An illustration of this objective is shown in Fig. 5. Some other important features of the technologies being promoted by the AirFuel Alliance are the choices of 6.78MHz ±15kHz as the operating frequency for power transfer and 2.4 GHz for control and communication signals. In principle, previous WPT technologies developed over the century can be applied to both relatively low frequency operations such as 105 kHz – 205 kHz for WPC

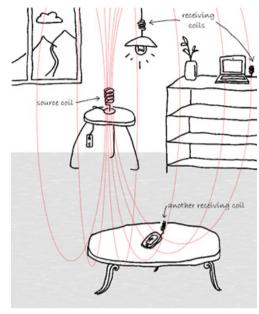


Fig. 5. An illustration of the WPT concept with spatial freedom.

or 6.78 MHz ±15kHz for AirFuel Alliance.

### C. New Health Concern on Human Exposure to Magnetic Field at 7 MHz

Compared with WPC which focuses primarily on short-range WPT applications, AirFuel Alliance chooses a much higher WPT frequency which enables higher compactness of the power and magnetic circuits and a high Q factor. As explained previously, increasing the value of Q allows the mutual coupling to decrease for a given kQ product. A small value of k implies a relatively long transmission distance for WPT, making it possible to increase spatial freedom. However, the idea of increasing spatial freedom (Fig. 5) also implies the requirements of human exposure to ac magnetic field.

The main concern of using 6.78MHz lies not only in the technical performance of the WPT technologies available today, but in the potential health hazards raised recently by quantum biologists about the adverse effects of ac magnetic field at 7 MHz on cell growth. In 2014, new practical evidence was presented in [40] to show that even a weak magnetic field of 10µT at 7 MHz could enhance cell proliferation. Note that an ac magnetic field of 10µT is considered to be weak because the static magnetic field of the earth is about 45 µT. It is suggested in [40] that magnetic field at 7 MHz could influence the electronic spins of cells to form radicals. The authors of [40] criticize the existing safety regulations which only consider the thermal stress on cells based on the specific absorption rate (Watt per kilogram of tissue) as inadequate. They concluded that "In contrast to the spin-pair mechanism, specific absorbed radiation (SAR) measurements of macroscopic tissue heating represent a naïve approach to bio-magnetic RF- interactions because it ignores nanoscale physics and spin chemistry, which can potentially have profound biological effects." Following

up the work in [40], the authors of [41] provide possible explanations for observed changes in growth rates of cancer cells and radical concentration upon exposures to magnetic fields below the ICES and ICNIRP reference levels.

It is therefore important for international regulatory bodies to re-examine existing health and safety regulations in view of the new evidence because 7 MHz is close to the Industrial, Scientific and Medical (ISM) radio band of 6.78 MHz (which happens to be the operating frequency selected by the AirFuel Alliance). The author believes that using 6.78 MHz for short-range applications in which the magnetic flux is enclosed or shielded (like the application framework in the WPC) should not encounter the same potential health issue. The choice of operating frequencies does not affect the validity of many existing WPT technologies in terms of the technical viabilities. Stakeholders in the WPT industry should consider a common standard that addresses both technical performance and health and safety concerns of consumers.

## D. SAE TIR J2954 Guidelines for Wireless Charging of Plug-In Electric Vehicles

SAE International, initially established as the Society of Automotive Engineers, is a professional association and standards developing organization for engineering professionals in various industries. In May 2016, SAE launched SAE TIR J2954 as an industry-wide specification guideline that defines acceptable criteria for interoperability, electromagnetic compatibility, minimum performance, safety and testing for wireless charging of light duty electric and plug-in electric vehicles [42]. The current version addresses unidirectional charging from grid to vehicle. Bidirectional energy transfer is not covered. This guideline calls for a common operating frequency of 85 kHz, which is easily manageable with existing power electronics technology even at 10 kW. It proposes four classes of wireless power transfer: 3.7 kW, 7.7 kW, 11.0 kW, and 22.0 kW. It is intended to be used for stationary applications. Dynamic wireless charging will most likely be considered in future guidelines when dynamic wireless charging technology becomes more mature.

#### E. From Directional to Omni-directional WPT

Existing commercial WPT products are based on directional wireless power flow. One new development of directional WPT is the use of the wireless domino WPT system for powering online monitoring system in power transmission networks. Energy can be harvested from the magnetic field of a high-voltage power cable and transferred to the high-voltage transmission tower to power the online monitoring system (Fig. 6). Coil-resonators can be embedded inside the insulation discs as shown in Fig. 7. The new insulation string structure provides both high-voltage insulation and WPT capabilities [43], [44].

Research into omnidirectional WPT has been reported in [25]. Fig. 8 shows one example of an omnidirectional



Fig. 6. Use of patent-pending insulation string with embedded coil-resonators for WPT [43], [44].



Fig. 7. Novel insulation string" with (i) High-Voltage insulation & (ii) Wireless Power Transfer capabilities [43], [44].

WPT container in which the receiver coil of the load can obtain wireless power regardless of its orientation inside the container. The omnidirectional WPT system in Fig. 8 consists of three orthogonal transmitter coils excited by a patent-pending non-identical current control method. The control principle of this omnidirectional WPT system has been developed [45]. This system can be used for simultaneous charging of a range of portable electronics products, regardless of the orientations

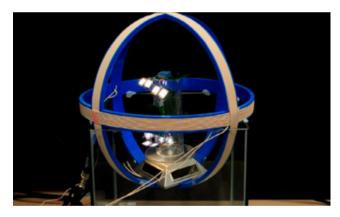


Fig. 8. An omnidirectional WPT system based on three orthogonal transmitter coils and non-identical current-control [45] (Courtesy of the University of Hong Kong).

of the receiver coils. It is suitable for charging a variety of electronics devices (such as smart phones and smart watches) in a highly user-friendly and convenient manner.

#### IV. AVOIDANCE OF SOME PITFALLS IN WPT

Besides understanding the historical developments of WPT, researchers entering this exciting field should equip themselves with some basic understanding so as to avoid certain pitfalls. These issues include the use of the appropriate terminologies, the scientific principles and choices of technologies.

#### A. Understanding the Correct Terminologies

Power electronics (PE) researchers/engineers are usually interested in "power" transfer, while Radio-Frequency (RF) researchers focus on "signal" transfer. They could use similar terms which could have totally different technical meanings. This issue was raised and explained in a critical review [46]. For a RF researcher, the term "impedance matching" often means matching the load impedance with the source impedance. On the contrary, a PE researcher often uses the same term to refer to designing a resonant capacitor so that its negative reactance can cancel the positive reactance in the power flow path. Another example is the term "efficiency". A RF researcher often considers the "power leaving the output terminals" of an ac power source as the "input power" of a RF system. A PE researcher considers the "power entering the input terminals" of an ac power source as the "input power". It is a common practice for a PE researcher to consider the power loss in the power source in the calculation of the overall system energy efficiency.

#### B. Understanding the Correct Operating Principles

As originally pointed out in [46], WPT operations can be classified as under either the Maximum Energy Efficiency (MEE) Principle or the Maximum Power Transfer (MPT) Principle. PE researchers are familiar with the operations of switched mode power supplies that should have minimum

source resistance and switching loss. They tend to adopt the MEE principle because overall system energy efficiency is often a top priority in power transfer. Their designs usually include the considerations of the source resistance that should be as small as possible.

RF researchers tend to consider signal transfer with the equivalent load impedance matching the source impedance in order to meet the maximum power transfer theorem. However such approach, when used for power transfer, suffers an inherent problem that the overall energy efficiency will never be higher than 50%. Even in the ideal case that the source resistance is equal to the load resistance, half of the input power will be dissipated in the source resistance. For WPT applications in which energy efficiency is of top priority, the MEE principle is the preferred option instead of the MPT principle. Therefore, ignoring the source resistance in WPT system design will lead to very low energy efficiency. While the transmission efficiency (without considering the power loss in the power source) in [18] is about 40%, the overall system efficiency including the power loss in the power source is only 15%. So the work in [18] illustrates the problems of ignoring the source resistance and of using the MPT principle in WPT applications of significant power. As different applications require different strategies of designs and operating principles, some general guidelines for choosing the appropriate operating methods have been addressed in [22] and now expanded in TABLE II.

TABLE II
GENERAL GUIDELINES OF CHOOSING THE OPERATING PRINCIPLES

	MEE	MPT
Impedance matching	To design the resonance capacitor to compensate the leakage inductance	To match the input impedance of the WPT system with the source impedance
System efficiency	Can be higher than 50%	≤ 50%
Source resistance	As low as possible (RS $\rightarrow$ 0)	Dependent on the power source
Suitable power level if efficiency is a priority	$\geq 1$ W	< 1 W
Applications	Energy efficiency is a priority	Energy efficiency is not a priority
Feature of a 2-coil system	High efficiency for short-range, but very low efficiency for mid-range applications	Low efficiency for both short- and mid-range applications
Feature of a 3-coil system (including an intermediate relay resonator) [47]	Under some conditions, a 3-coil system can be more efficient than a 2-coil one.	
Feature of a 4-coil system based on two resonators and two coupled coils [18]		Maximized transmission distance at the expense of energy efficiency.
Feature of multi-coil system based on relay resonators [43], [44]	A good compromise between energy efficiency and transmission distance if relay resonators are allowed.	

#### V. Conclusions

Despite the original concept was developed over a century ago, WPT is still a fast growing R&D area with immense application potentials. With the understanding of the historical WPT developments, it is hoped that visionary researchers would take WPT to new heights in the future. International cooperation plays an instrumental role in

setting up wireless charging standards to serve the industrial community and users of wireless power. It is natural that these standards will evolve with time and progress of WPT technology. Wireless power not only provides a wide range of functions for various industrial and domestic applications, it also offers sustainable solutions to reduce tonnes of unnecessary chargers and their associated electronic waste. This point is particularly important to the industry of portable consumer electronics devices. With new evidence

of health concerns presented by quantum biologists about the use of magnetic field at 7 MHz, more research efforts should be devoted to study the effects of magnetic field on cell growth. International health and safety organization should re-examine the coverage of existing standards. So far, WPT has reached commercialization stage in consumer electronics and manufacturing industry. It is envisaged that the next sectors that would benefit from WPT include electric vehicles and medical implants. WPT is no longer a discipline for electrical engineers and scientists only. It has evolved into a multidisciplinary subject involving quantum biologist, biological and biomedical scientists.

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# Design for Reliability of Power Electronics for Grid-Connected Photovoltaic Systems

Yongheng Yang, Ariya Sangwongwanich, Frede Blaabjerg

Abstract—Power electronics is the enabling technology for optimizing energy harvesting from renewable systems like Photovoltaic (PV) and wind power systems, and also for interfacing grid-friendly energy systems. Advancements in the power semiconductor technology (e.g., wide band-gap devices) have pushed the conversion efficiency of power electronics to above 98%, where however the reliability of power electronics is becoming of high concern. Therefore, it is important to design for reliable power electronic systems to lower the risks of many failures during operation; otherwise will increase the cost for maintenance and reputation, thus affecting the cost of PV energy. Today's PV power conversion applications require the power electronic systems with low failure rates during a service life of 20 years or even more. To achieve so, it is vital to know the main life-limiting factors of power electronic systems as well as to design for high reliability at an early stage. Knowhow of the loading in power electronics in harsh operating environments (e.g., fluctuating ambient temperature and solar irradiance) is important for life-time prediction, as the prerequisite of Design for Reliability (DfR). Hence, in this paper, the technological challenges in DfR of power electronics for grid-connected PV systems will be addressed, where how the power converters are stressed considering real-field mission profiles. Furthermore, the DfR technology will be systematically exemplified on practical power electronic systems (i.e., gridconnected PV systems).

Index Terms—Reliability, design for reliability, power electronics, physics of failure, mission profiles, thermal loading, degradation, Monte Carlo method, photovoltaic systems.

#### I. Introduction

A ccessibility and sustainability are of high concern in energy sectors across the globe. Shortage of conventional coalor oil-fired energy and its impact on climate changes have been the main driving forces to develop and advance the renewable energy technology. As of the end of 2015, the total renewable energy installed worldwide is approaching 2000 GW [1], and the capacity is expected to be

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even higher in the future [2]. Fig. 1 shows the historical data of the energy paradigm shift to renewables, where it can be observed that the hydropower is always leading in terms of total installed capacity, followed by wind and solar energy. Hydroelectric power systems are deemed as a relatively matured technology that uses released water to spin a turbine for electricity generation. Power electronics is the link of this energy conversion chain. Along with the demand of environmental-friendly energy systems and the decrease of manufacturing cost in wind turbines and solar Photovoltaic (PV) panels, power generation based on wind turbine and PV technologies is becoming increasingly important in national strategical plans, as indicated in Fig. 1. For instance, in Denmark, a goal of completely being independent from fossil fuels by 2050 has been set up [3]. Although there are several state-of-the-art wind turbine technologies (e.g., the Doubly-Fed Induction Generator - DFIG wind power systems), power electronics converters are normally heavily involved [2],[4],[5]. A thriving penetration of power electronics has also been acknowledged in PV applications, either in small-scale stand-alone units or in large-scale ongrid systems [6],[7]. In a word, power electronics is essential in the power conditioning of renewable energies, and it is also developing with new and emerging power devices coming out on market [8]-[10].

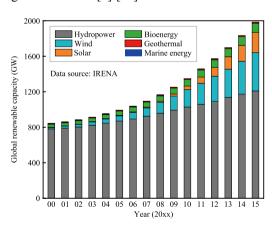


Fig. 1. Annual evolution of the global installed renewable capacity (2000-2015), where hydropower also includes pumped storage and mixed plants and marine energy covers tide, wave, and ocean energy [1].

To accomplish those objectives, two main challenges have to be addressed: increasing the energy conversion efficiency and reducing the cost in installation and maintenance, which are closely related to the Levelized Cost of Energy (LCOE) [5], [11], [12] as indicated by

$$LCOE = \frac{C_{Int} + C_{Cap} + C_{O\&M}}{E_{Annual}}$$
 (1)

with  $C_{\text{Int}}$  being the initial development cost,  $C_{\text{Cap}}$  representing the capital cost,  $C_{0\&M}$  indicating the operational and maintenance cost, and  $E_{Annual}$  is the average annual energy production in the lifetime cycle of the system. Only when the LCOE for renewable energies reaches a comparably low level (i.e., making solar energy cost-competitive), a complete phasing-out of conventional fossil-based energy resources can possibly be realized. This can also be concluded from the SunShot Initiative [13] to lower PV cost by 2030, which is presented in Fig. 2. It can be observed in Fig. 2 that a significant reduction by more than 50% in the cost of PV systems has been achieved in the past 7 years. More important, the reduction needs to continue. Nevertheless, reflected by (1), the two aforementioned factors affect the LCOE. Namely, increasing the efficiency will contribute to more energy yield, and improving the reliability will lower the cost in maintenance, leading to a lower LCOE. As the power electronics is the core of renewable power generation, highly efficient and highly reliable power electronics converters are thus demanded.

Efficiency improvements can be attained mainly by two means: topological developments and power semiconductor advancements. From the topological point view, reducing the number of conversion stages in PV applications can contribute to an increased efficiency. Transformerless PV inverters are typical representatives in terms of high efficiency, where namely bulky transformers have been removed [7], [14]-[17]. However, topological simplification also brings side-effects like a lack of galvanic isolation, and thus dedicated control strategies are required. Alternatively, latest advancements in power electronics semiconductor technologies (e.g., wide-band gap power devices like Silicon-Carbide - SiC and Gallium-Nitride -GaN transistors), featuring with high-temperature and highswitching-frequency operation capabilities but low power losses, bring much space to improve the efficiency of PV power converters [9], [17]-[21]. As reported, highpower PV converters employing wide-band gap devices have achieved an efficiency approaching 99% [22], [23]. With this impressive performance, commercial PV inverters (e.g., from GE and SMA) are available on market. In addition, applying the soft switching techniques can also bring down the power losses due to fast switching, and thus in return the overall efficiency can further be improved.

Nevertheless, higher efficiencies of PV converters are relatively achievable, and thus it enables an efficient energy conversion from solar PV panels, especially with the successful applications of wide band-gap devices. However, the power electronics converter itself also becomes one of the most fragile parts in PV systems, leading to many downtimes. According to a survey [24], the unscheduled maintenance events due to power electronics accounts for 37% of the total events, as it is shown in Fig. 3. Those

downtime events require human intervention (system repairing or maintenance), thus affecting the overall production and also increasing the maintenance costs, which can be observed in Fig. 3. In the end, the LCOE of PV energy according to (1) will go up drastically due to the high failure rate of power inverters in PV systems. Hence, as aforementioned, high reliability of power electronics is in urgent need on top of efficiency.

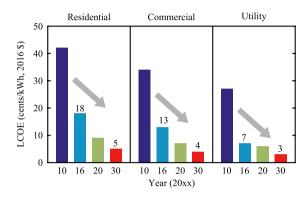


Fig. 2. Progress and goals of the SunShot Initiative to lower the cost of PV systems in residential, commercial, and utility applications [12], [13]. Figure adapted from the National Renewable Energy Laboratory (NREL).

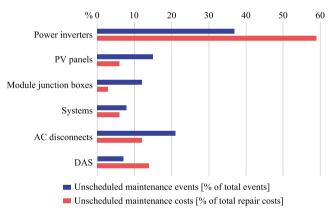


Fig. 3. Five year of real-field experience in failures of an utility-scale PV power plants [24], where DAS stands for Data Acquisition Systems.

In regards to enhancing reliability, more challenging issues have to be addressed [25]-[35]. It is very important to predict the lifetime, and thus Design for Reliability (DfR) can be incorporated in the design phase of the PV inverter system considering key life-limiting aspects [36], [37]. Previous research in lifetime prediction of power electronics (converters) has been mainly focused on statistic analysis. During this period, a handbook – MIL-HDBK-217 F [38] has been widely adopted to predict the lifetime of electronics equipment [32], [37], [39]-[43]. Basically, the lifetime predication can be achieved in a statistic way, where the reliability models (typically, constant failure rates) of subsystems are defined. Various analysis approaches like fault tree analysis [44], [45], Markov analysis [32], [46]-[49], failure mode and effect analysis [50], [51], and reliability block diagram analysis [52] can then be employed to determine the reliability from a systemlevel viewpoint.

However, the models with constant failure rates in this handbook are out of date, which have not been updated since 1995, leading to the revocation of this handbook. Another reason for the termination is that the predicted lifetime or reliability has no direct or high guiding value for planning and design of the entire PV systems [39]. That is, it is difficult to use the predicted reliability data to design new products or systems with higher reliability.

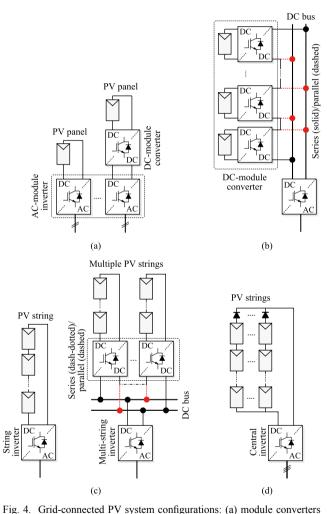
Hence, a transition to the Physics-of-Failure (PoF) based reliability analysis is undergoing [25], [26], [30], [33], [53], where identifying the root-causes of failures in power electronics is one of the attempts. In addition, for the PoF reliability analysis, different failure mechanisms from the points of view of physical structure, internal material characteristic, and operational environment/condition in power electronics are studied in prior-art research [35], [53]-[66]. Among those investigations, it has been observed that the thermo-mechanical stress is one major inducers of failures (mainly die-attach solder crack and bond-wire damage). The thermal stress is reflected as temperature cycling in the power electronics devices, including mean junction temperatures and junction temperature swings. Therefore, many attempts have been made to estimate the junction temperature in real-time [67]-[69] and develop schemes to manage/control the junction temperature for higher reliability [70]-[72]. In practice, the temperature variations are closely related to the operating conditions and environments, which are referred to as mission profiles [73]-[76]. Hence, the reliability analysis of power electronics in PV applications should also involve the acknowledge of mission profiles (i.e., ambient temperature and solar irradiance), which are time-varying inputs. In all, it calls for a systematic reliability analysis and design approach for power electronics in PV applications. It should be pointed out that enhancing the redundancy of PV power converters may also contribute to a high reliability at the cost of complexity.

In light of the above concerns, this paper briefly discusses the mainstream power electronics converters for gridconnected PV systems in § II. More important, reliability analysis in grid-connected PV inverters has been performed, where the DfR approach has been demonstrated in § III. A case study on a 6-kW single-phase grid-connected PV inverter system has been provided in § IV to better illustrate the DfR approach considering mission profiles, where the Monte-Carlo based simulation has also been performed so that a systemlevel reliability analysis can be achieved. It is demonstrated that the mission profile is an important factor which should be taken into account in the design phase of power electronics converters. Fortunately, the presented DfR approach offers a systematical design. Finally, § V gives concluding remarks and also discusses future research trends in the reliability of power electronics.

#### II. POWER CONVERTERS FOR PV SYSTEMS

Power electronics converters are the link between solar

PV energy and the grid, and thus have to perform various rigorous functions [5]. Harvesting and then transferring the solar PV energy to an ac grid considering the inherent characteristic of intermittency are the basic requirements. Also, other specifications are imposed to make gridconnected PV systems more resilient and grid-friendly: 1) reliable or secure the power supply, 2) flexible control of active and reactive power, 3) dynamic grid support per demands, 4) system condition monitoring, protection and communication, and 5) high efficiency and reliability, low cost, and small volume. Practically, there are mainly four structures for grid-connected PV systems, as it is shown in Fig. 4. It is clearly observed in Fig. 4 that the intermediate unit-power electronics converters is of essence to the energy conversion, in which the above functions should be implemented.



rig. 4. Grid-connected PV system configurations: (a) module converters typically applied in single-phase small systems of hundred watts, (b) demodule converters connected to a common dc-bus (forming a dc-grid), which can be connected to grid as single- or three-phase systems of several kW in small or residential applications, (c) string and multi-string converter applied in single- or three-phase systems (residential and commercial applications), and (d) center inverters for commercial or utility scale applications (high power, e.g., hundred kW).

Depending on the applications and power ratings, a PV system can be configured according to Fig. 4. For instance,

modular PV converters (Fig. 4(a) and (b)) are commonly adopted in small energy conversion systems, where volume and scalability are important. However, in order to connect modular PV converters to the grid through an inverter, high conversion ratio dc-dc converters may be required or a dcgrid is necessary. Comparing to this, string, multi-string or central inverters can directly feed power into the grid, as demonstrated in Fig. 4(c) and (d). In fact, the PV utilization is still at a residential level but tends to be large-scale with increased power ratings. Hence, string and multi-string inverters are dominate on market, and the single-phase connection is more often to see [7], [77]. Fig. 5 exemplifies a single-phase grid-connected PV system with an LCL filter, where a full-bridge inverter has been employed. Additionally, to have a higher efficiency, transformerless PV inverters are favorable, as shown in Fig. 5. However, the removal of isolation transformers can generate leakage currents in the system, which may be addressed by specifically designing the modulation schemes [5], [14].

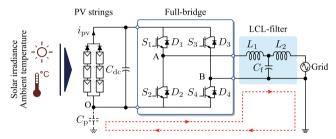


Fig. 5. Single-phase single-stage transformerless full-bridge string inverter with an LCL filter, where ipv represents the PV output current and  $C_{\rm p}$  is the parasitic capacitor between the PV panels (strings) and the ground. The red dashed line indicates possible leakage currents circulating through the parasitic capacitor  $C_{\rm p}$ .

Although single-phase grid-connections are more commonly seen in PV applications, increasing demands in power push the rating of PV systems higher. In that case, three-phase PV systems with central inverters become feasible, which is also promoted by industrial companies like SMA, ABB, and Kaco. For high-power utility-scale PV systems, the power electronics converters can be traditional full-bridge converters, as shown in Fig. 6. Notably, the cables and power devices may have to bear large currents. Disconnecting a large amount of dc currents is also challenging. As an alternative, (modular) multilevel converters might be a promising solution [78]-

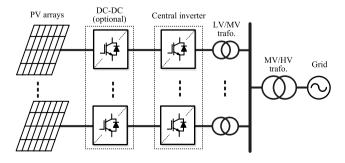


Fig. 6. Connecting large-scale PV plants to the grid through center inverters, where the dc-dc converters are optional.

[80]. Nevertheless, the role of power electronics converters remains in high-power applications.

## III. DESIGN FOR RELIABILITY OF POWER CONVERTERS FOR PV SYSTEMS

As discussed in § II, PV panels and power converters are essential components, but all have to be considered in the design phase in order to further break down the cost of PV energy. Fig. 7 shows the cash-flow in the design and operation phases of grid-connected PV systems, where it can be observed that many factors affect the cost of PV systems. Furthermore, it is implied that the unexpected failures during operation incur high costs in maintenance [36]. This is because the reliability is not specifically included in the design, but reflected as slow and expensive feedbacks or iterations.

Hence, in order to lower the unscheduled maintenance cost, potential failures should be anticipated as early as possible and input in the design. This initiates a more promising solution to improving the reliability of PV systems, as it is shown in Fig. 8. The inclusion of the DfR enables a quick identification of design flaws or weakness, and thus feeds back to the design for corrections (e.g., re-selection of components). After a few iterations, the reliability demands can be fulfilled before the system construction. Consequently, it contributes to significant cost reduction in the design phase and shorter development cycle for the PV system targeting for higher reliability. Furthermore, the failures or downtimes of the PV systems are predictable.

Notably, the DfR approach is relying on the lifetime or reliability prediction, which involves in multiple disciplines from the PoF point of view. Fig. 9 depicts the detailed reliability evaluation process of the DfR approach. It can be seen that the reliability analysis has three major tasks: 1) failure identification, 2) stress analysis and strength modeling, and 3) reliability mapping. More specific, the critical components and the major failure mechanisms in the PV power converter system are identified through physics analysis and real-field experience. Accordingly, the corresponding stresses and the ability of power electronics components to withstand the stresses are tested and modeled. Finally, counting algorithms and statistical distributions are adopted to map the stress and strength information of the power electronics components to the reliability metrics of the entire PV power converter. Notably, the reliability indicators can be direct performances like  $B_x$  lifetime, robustness, and failure probability, etc., or indirect performances like maximum thermal stress [36].

For a specific application (e.g., the PV inverter installed in Denmark), the DfR approach included in the design phase of Fig. 8 and detailed in Fig. 9 enables analyzing the power converter candidates in terms of reliability. Here, the failure mechanisms have to be identified first. As it has been discussed previously, for power electronics converters, the major failures are related to the temperature in power

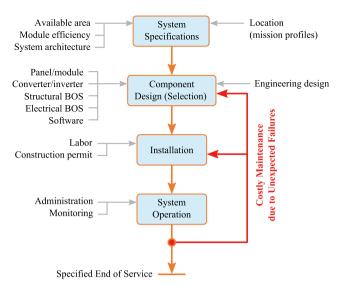


Fig. 7. Cash-flow in the conventional design and operation phases of gridconnected PV systems (BOS – Balance of System).

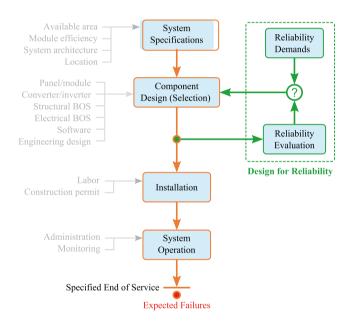


Fig. 8. Cash-flow in the design and operation phases of grid-connected PV systems, where the design for reliability of power electronics has been incorporated in the design phase.

devices. This can also be validated through accelerated tests, where power cycling and thermal cycling should be performed. Nevertheless, on condition that the failure mechanisms are identified, it is possible to directly translate mission profiles specified by customers into thermal loading on the power electronics components of the selected candidates according to Fig. 9. As a result, the reliability is obtained from a system point view, and the process is summarized as:

- Mission profile translation to thermal loading
- Thermal cycling interpretation
- Lifetime (degradation) model of power devices
- · Monte Carlo reliability assessment
- System-level reliability analysis

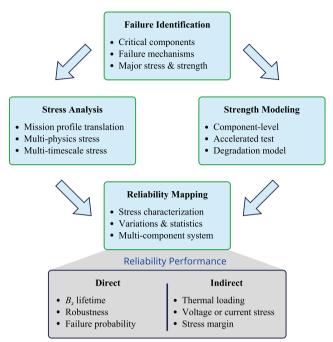


Fig. 9. Design for Reliability (DfR) structure for power electronics converters, which can be used to evaluate the reliability of candidate power converters considering various factors (e.g., mission profiles). In this approach,  $B_x$  lifetime indicates the time by which x percent of a population of the evaluated system will have failed.

which will be discussed in details as following.

#### A. Mission Profile Translation to Thermal Loading

In the DfR approach, the knowledge of the power converter operating conditions during the entire operation is essential [25], [73], [75]. In this respect, a mission profile of the power converters, which represents the operating condition of the system, is needed. The mission profile of the PV system can be obtained from the solar irradiance and ambient temperature profiles at the installation sites, as these two parameters have a strong impact on the PV power production [76]. Then, the mission profiles have to be translated into thermal loading of power converters (e.g., junction temperature variations of the devices), since it is usually a life-limiting factor in power electronic applications (e.g., resulting in a bond wire lift-off) [60]. There are intermediate steps to obtain the thermal loading of the power converters, as it is illustrated in Fig. 10.

From the solar irradiance and ambient temperature profiles, the PV power production  $P_{\rm pv}$  can be estimated from the PV panels electrical characteristic model [81]. Then, by taking the MPPT algorithm efficiency  $\eta_{\rm MPPT}$  and the PV inverter electrical characteristic (e.g., conduction and switching behaviors of power devices) into account, the power losses dissipated in the power devices  $P_{\rm loss}$  can be estimated. Notably, this loss calculation is usually implemented with a Look-Up Table (LUT), in order to assist the long-term simulation (e.g., an annual mission profile). In that case, the power losses are calculated for a certain set of operating conditions (e.g., the input power from 0% to

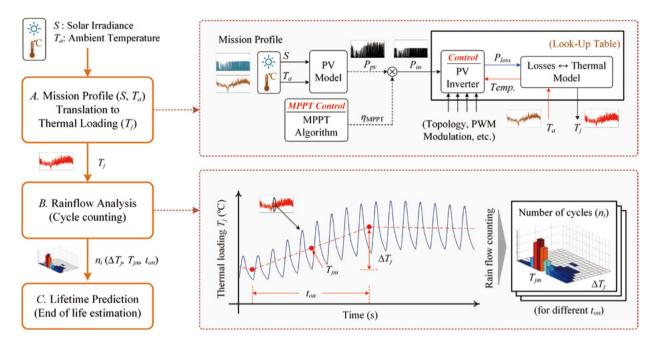


Fig. 10. Flowchart of the lifetime evaluation or predication considering mission profiles of the power electronics systems [76].

100% of the rated power, and the ambient temperature from -25 °C to 50 °C), and the power losses under other operating conditions can be interpolated from the constructed LUT. Then, the thermal model of the power devices in the power converter is needed in order to obtain the device junction temperature variation due to the dissipated power losses in the power devices.

#### B. Thermal Cycling Interpretation

By applying the previous process, the junction temperature of the power device  $T_j$  under a specific mission profile can be obtained. However, the device junction temperature is usually an irregular loading profile, due to the dynamics of mission profiles (i.e., solar irradiance and ambient temperature for gridconnected PV systems). Thus, a cycle counting algorithm such as a rainflow analysis is usually employed, in order to divide the irregular thermal loading cycle into several regular thermal loading cycles [82]. By doing so, the information such as the mean junction temperature  $T_{jm}$ , the cycle amplitude  $\Delta T_j$ , and the cycle period  $t_{on}$  can be obtained, which can be then applied to the lifetime (degradation) model of the power electronics devices of the converter candidates.

#### C. Lifetime (Degradation) Model of Power Devices

There are several components in the PV inverter (e.g., capacitors and IGBTs) that can cause failure of the system. In that regards, it leads to a complex analysis, as the components in the inverter systems may have a cross effect of the reliability on each other. In this study, only the temperature-related failure mechanisms of the power device are considered in order to simplify the reliability analysis. In fact, the power device has been reported as one of the most

critical components in the power converter, which cause failures of the whole system [27]. Hence, there are many temperature-related lifetime models reported in literature [61], [83]. According to [61], a lifetime model of an IGBT power device can be given as

$$N_f = A \times (\Delta T_j)^{\alpha} \times (ar)^{\beta_1 \Delta T_j + \beta_0} \times \left[ \frac{C + (t_{on})^{\gamma}}{C + 1} \right] \times \exp\left(\frac{E_a}{k_b \times T_{im}}\right) \times f_d$$
 (2)

where  $N_f$  is the number of cycles to failure [61]. Notably, the inputs of this lifetime model are: the mean junction temperature  $T_{jm}$ , cycle amplitude  $\Delta T_j$ , and cycle period  $t_{on}$ , which can be obtained from the cycle counting process, while the other parameters are given in TABLE I. Normally, the lifetime of the power device is expressed by considering the Life Consumption (LC), which indicates how much life of the device has been consumed (or damaged) during operations. The LC is calculated by using the Miner's rule as [82]

$$LC = \sum_{i} \frac{n_i}{N_{fi}} \tag{3}$$

PARAMETERS OF THE LIFETIME MODEL OF AN IGBT MODULE [61].

Parameter	Value	Experimental condition
A	3.4368×10 <sup>14</sup>	
$\alpha$	-4.923	$64 \text{ K} \leq \Delta T_i \leq 113 \text{ K}$
$oldsymbol{eta}_1$	-9.012×10 <sup>-3</sup>	,
$oldsymbol{eta}_0$	1.942	$0.149 \leqslant ar \leqslant 0.42$
C	1.434	
γ	-1.208	$0.07 \text{ s} \leqslant t_{on} \leqslant 63 \text{ s}$
$f_d$	0.6204	
$E_a$	0.06606 eV	$32.5 ^{\circ}\text{C} \leqslant T_j \leqslant 122 ^{\circ}\text{C}$
$k_{\scriptscriptstyle B}$	8.6173324×10 <sup>-5</sup> eV/K	

where  $n_i$  is the number of cycles (obtained from the thermal cycling interpretation, e.g., a rainflow analysis) for a certain  $T_{jm}$ ,  $\Delta T_j$ , and  $t_{on}$ , and  $N_{fi}$  is the number of cycles to failure calculated from (2) at that specific stress condition. For instance, if the number of cycles  $n_i$  is counted from a oneyear mission profile, the LC calculated in (3) will represent a yearly LC of the power device. When the LC accumulates to unity (i.e., 100%), the power electronics device is considered to reach its end of life, and the lifetime can be predicted.

#### D. Monte Carlo Reliability Assessment

Actually, the lifetime prediction of the power device obtained from (3) can be considered as an ideal case, where all the power devices fail at the same rate (under a certain mission profile). In reality, there are uncertainties in the time-to-failure of the power devices, which are mainly introduced by variations in the lifetime model parameters as well as variations in the stresses. Therefore, it is more common to express to lifetime prediction in terms of statistical value (e.g., by using probability of failure), rather than the fixed value. In order to do so, the Monte Carlo analysis needs to be performed. The idea of the Monte Carlo method is to introduce variations in the system parameters, and simulate the result with a large number of samples. With the large enough number of samples, the results will converge to the expected value.

This approach can be employed for estimating the power devices lifetime [62], [84], [85], as it is shown in Fig. 11. In this method, all the parameters in the lifetime model in (2) have to be modeled by a distribution function (e.g., normal distribution) with a certain range of variations. Then, following the Monte Carlo simulation approach, a certain number of samples from each parameter distribution are randomly taken for calculating the lifetime of the power device. By doing so, a set results of lifetime prediction is obtained, which can then be represented with a certain distribution function (e.g., Weibull distribution) [86]. The Probability Density Function (PDF) of this lifetime prediction result is usually referred to as a lifetime distribution (failure distribution) f(x), while its Cumulative Distribution Function (CDF) is considered as an unreliability function F(x). The  $B_x$  lifetime, which is the time when x%of the populations are failed, can be obtained from the unreliability function of the power device, as it is shown in Fig. 11.

#### E. System-Level Reliability Analysis

In most cases, the power converters consist of several power devices, where each device has its own unreliability function F(x). In order to perform the system-level reliability assessment, the reliability block diagram of the whole system needs to be constructed [28]. The reliability block diagram represents how the reliability of components in the system interact with each other. For the system with n number of components and the system cannot function if

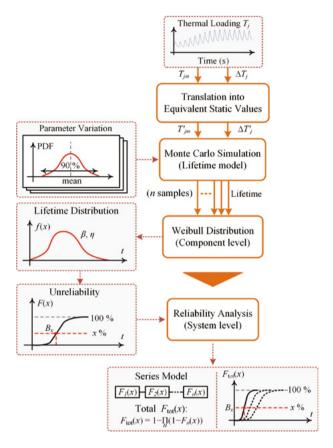


Fig. 11. Flow diagram of Monte Carlo-based system-level reliability assessment of PV inverters with reliability block diagram.

any of the component fails, the total unreliability of system  $F_{tot}(x)$  can be calculated as:

$$F_{\text{tot}}(x) = 1 - \prod_{n} (1 - F_n(x))$$
 (4)

where  $F_n(x)$  is the unreliability function of the  $n^{th}$  component. Once the total unreliability function of the inverter system  $F_{tot}(x)$  is obtained, the  $B_x$  lifetime of the entire PV inverter can be estimated in the similar way as it has been done for a single power electronics component.

It should be pointed out that this approach can be applied to any power electronic system. For different converter topologies, the reliability block diagram of the system may be different, depending on the number of power devices and their operational principle.

#### IV. CASE STUDY

In this section, a case study of 6 kW single-phase PV inverters will be presented. The DfR approach discussed in § III will be applied to the mission profile of the inverter installed in Denmark. The lifetime evaluation and the reliability assessment will be carried out in the following.

#### A. Mission Profiles of the Case Study

The yearly solar irradiance and ambient temperature profiles recorded from the installation site in Denmark are shown in Fig. 12. It can be seen from Fig. 12(a) that the solar irradiance level varies considerably through the whole year. The average solar irradiance level is relatively high from June through August, while it is relatively low through November to February. This variation in the solar irradiance during the year will have a direct impact on the PV power production, which will in return contribute to the long-term thermal loading of the power devices in the PV inverter.

Similarly, the ambient temperature in Denmark also varies in a wide range during the year. For instance, the highest temperature reaches around 34 °C in summer (i.e., at the end of May), while the lowest ambient temperature can be around -18 °C in winter (i.e., at the beginning of February). This ambient temperature variation will have a strong influence on the mean junction temperature, but also contribute indirectly to the thermal loading of the PV inverter through the life-cycle PV power production.

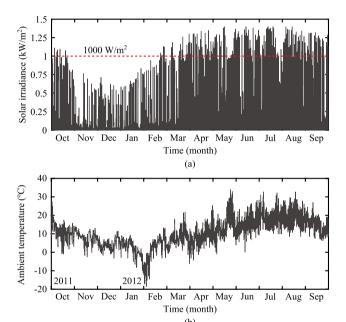


Fig. 12. Yearly mission profiles (i.e., irradiance and ambient temperature with a sampling rate of 5 mins per sample) in Denmark: (a) solar irradiance level and (b) ambient temperature.

#### B. Translated Thermal Loading

By using mission profile translation process presented in § III.A, the junction temperature of the power device can be obtained. The power device junction temperature of the PV inverter installed in Denmark (with the mission profile in Fig. 12) is presented in Fig. 13. It can be seen that the cycle amplitude of the junction temperature in Fig. 13(a) has similar variations as the solar irradiance profile in Fig. 12(a), with the maximum cycle amplitude of 25 °C. The mean junction temperature of the power device is shown in Fig. 13(b), which has a similar tendency as the ambient temperature profile. The mean junction temperature reaches its highest value at 78 °C, while its minimum value is -18 °C in winter (i.e., at the beginning of February).

#### C. Lifetime Evaluation

The rainflow analysis is then applied to the junction temperature loading profile shown in Fig. 13, and the results are used to determine the LC from the lifetime model in (2). By doing so, the resultant LC for a single device of the PV inverter can be calculated as 0.0073/year, which indicates that the individual power semiconductor device will reach its end of life after 137 years of operation.

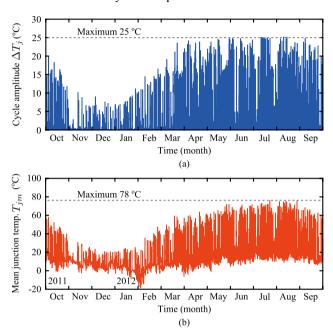


Fig. 13. Thermal loading of an individual power device in the singlephase full-bridge PV inverter under a yearly mission profile in Denmark (see Fig. 12): (a) cycle amplitude of the junction temperature variation  $\Delta T_j$  and (b) mean junction temperature  $T_{jm}$  of the power device.

Considering parameter variations of the lifetime model, the Monte Carlo method is applied to the lifetime evaluation. In this case, the parameters of the lifetime model in (2) are modeled by using a normal distribution with 5% parameter variation. Similarly, the parameter variation also needs to be introduced to the stress parameters  $(T_{jm}, \Delta T_j, \text{ and } t_{on})$ , which are the inputs of the lifetime model. In this case, it is necessary to determine the equivalent static value of these dynamic parameters (which dynamically changes during operations, i.e., mission profile). Basically, the equivalent static value of the stress parameters  $(T'_{jm}, \Delta T'_j, \text{ and } t'_{on})$  are the representative values of the stresses obtained from mission profile, which results in the same LC.

In fact, there are several combinations of equivalent static values that can be applied to the lifetime model and result in the same LC. For simplification, only the line frequency (i.e., 50 Hz) thermal cycling is considered, meaning that, $t'_{on}$  is selected to be 0.01 s (heating period is half of the total cycle period), and the number of cycles per year  $n'_i$  is  $(365 \times 24 \times 60 \times 60) \times 50$  cycles. Regarding the junction temperature variations, the equivalent mean junction temperature  $T'_{jm}$  can be obtained by averaging the yearly profile of the mean junction temperature in Fig. 13(b).

Afterward, the equivalent cycle amplitude  $\Delta T_j$  can be calculated by solving the equation (2). The equivalent static values from the mission profile of the PV inverter installed in Denmark is summarized in TABLE II. Once the equivalent static values are determined, they are also modeled with a normal distribution function, as it has been done previously with the lifetime model parameters.

The Monte Carlo simulation is then carried out with a population of 10000 samples, where the LC and the corresponding lifetime for 10000 samples can be obtained and fitted with a Weibull distribution. Notably, the lifetime distribution of the power device, f(x), usually follows the Weibull distribution [53], [86], whose PDF can be expressed as

$$f(x) = \frac{\beta}{n^{\beta}} x^{\beta - 1} \exp\left[-\left(\frac{x}{n}\right)^{\beta}\right]$$
 (5)

where  $\beta$  is the shape parameter and  $\eta$  is the scale parameter. In general, the value of  $\beta$  represents a failure mode (i.e., same failure modes will result in a similar  $\beta$  value), while the value of  $\eta$  is corresponding to the time when 63.2% of population will have failed [53]. The lifetime distribution f(x), Weibull PDF, of the power device obtained from the Monte Carlo simulation is shown in Fig. 14(a), and the unreliability function (Weibull CDF) is shown in Fig. 14(b). From the Weibull CDF in Fig. 14(b), the Bx lifetime of one singledevice power device considering parameter variations can be obtained. For instance, the B<sub>10</sub> and B1 lifetime of the power device are 74 and 42 year, respectively. This implies that 10% of the population is expected to fail after 74 years of operation, and 1% of the populations is expected to fail after 42 years.

TABLE II
EQUIVALENT STATIC VALUES OF THE STRESS PARAMETERS.

Parameters	Value
Mean junction temperature $T'_{im}$	13.45°C
Cycle amplitude $\Delta T'_{j}$	5.69°C
Cycle period $t'_{on}$	0.01 s
Number of cycles per year $n'_i$	(365×24×60×60)×50
Yearly LC	0.0073
Lifetime prediction	137 years

#### D. System-Level Reliability Analysis

From the component-level unreliability function F(x) obtained from the Monte Carlo method, the system-level reliability assessment can be performed by using the reliability block diagram. The full-bridge inverter topology in Fig. 5 consists of four power devices and the inverter cannot function if any of the devices fail. Thus, the total unreliability of system  $F_{tot}(x)$  can be calculated as:

$$F_{\text{tot}}(x) = 1 - \prod_{n=1}^{4} (1 - F_n(x))$$
 (6)

where  $F_n(x)$  is the unreliability function of the  $n^{th}$  power

device in the system. In the case of full-bridge topology (with bipolar pulse width modulation technique), the loading of each power device is equal, meaning that, it has the same unreliability function:  $F(x) = F_1(x) = F_2(x) = F_3(x) = F_4(x)$ . Therefore, the system-level unreliability function can be simplified as

$$F_{\text{tot}}(x) = 1 - (1 - F(x))^4 \tag{7}$$

The total unreliability of the full-bridge inverter is presented in Fig. 14(b), and the corresponding system-level  $B_x$  lifetime is also shown in the same figure. The  $B_{10}$  and  $B_1$  lifetime of the full-bridge inverter (i.e., system-level reliability) is 53 and 30 years, respectively, which is 21 and 12 years lower than the component-level  $B_{10}$  and  $B_1$  lifetime.

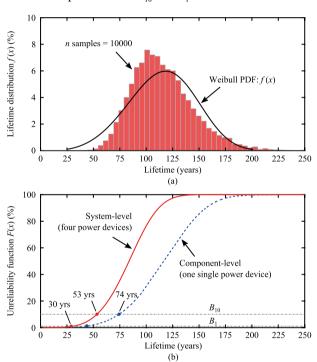


Fig. 14. Results from the Monte Carlo simulation with 10000 samples: (a) lifetime distribution of one single power device (i.e., the Weibull PDF function) and (b) unreliability function (i.e., the Weibull CDF function) of one single power device (component-level) and full-bridge inverter with four power devices (system-level).

#### V. Conclusions

In this paper, it has been illustrated that the developments and requirements for the power electronics technology in the grid-connected PV systems are increasing drastically, where the importance of reliability performance should be especially focused. State-of-the-art in power electronics converters for grid-connected PV power generation systems has been briefly presented, where the role of power electronics converters is highlighted. Then, the Design for Reliability (DfR) approach has been introduced in details. A case study on a gridconnected PV system has also been performed to demonstrate the DfR approach.

It is concluded that as the continuously fast development

of the grid-connected PV technology, the reliability performance of the power electronics in such applications is getting more and more critical. There are many emerging challenges as well as technology opportunities to achieve more reliable power electronics, in such a way that the LCOE in solar PV systems can be further reduced. It is worth to mention that, right now the reliability calculation and analysis for power electronics including PV power converters are undergoing revolutionary advancements, many other issues beside power semiconductors and thermal loading are also important factors to be taken into consideration in the final product.

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He has received 18 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He was nominated in 2014, 2015 and 2016 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.

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China Power Supply Society (CPSS) founded in 1983 is a nonprofit, non-governmental academic and professional organization of scientists and engineers in the power supply & power electronics fields. CPSS is dedicated to achieving scientific and technological progress of power supply and the advancement of the power supply industry. CPSS website is www.cpss.org.cn.

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