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Abstract

In this paper, the gate voltage oscillations occurring under short-circuit conditions in Insulated-Gate Bipolar Transistors are investigated, together with their dependency with respect to stray inductance variations. By using AnSYS Q3D Extractor, electromagnetic simulations are conducted to extract the self and mutual inductances of three different layouts, which are also experimentally tested. Finite-element device simulations on a planar IGBT cell have been carried out to provide a better understanding of the internal physical mechanisms and thus demonstrate by a sensitivity analysis which layout parameters must be minimized. This study is important to reach conclusions on the package design requirements for optimum performance under short-circuit operations, revealing the compromises between switching speed and short-circuit performance. Finally, an optimized layout solution for mitigating possible IGBT short-circuit instabilities, such as oscillations, is proposed.

1. Introduction

For decades, the ever-increasing demand for fast switching devices has continuously challenged the full performance of power semiconductor devices. The main reason is the rapid improvement of the semiconductor device industry, as each device generation is faster and more efficient than the previous one, in contrast, the lower rate of development in terms of packaging and integration methods [1]. For instance, the most prevalent packaging in modularization and integration on power electronic systems is nowadays the Insulated-Gate Bipolar Transistor (IGBT) module. And yet, novel designs are constantly needed in order to construct a lower inductance module.

High reliability performance is another crucial factor to move towards low-inductive designs. In practical applications, many failures in power semiconductor devices are caused by parasitic effects [2, 3]. For example, if the layout is not effectively optimized, the voltage spikes during the IGBT turn-off under normal and abnormal operations can exceed the maximum voltage rating of the IGBT (i.e., the breakdown voltage of the device). This means that an IGBT chip with higher voltage rating must be selected with an additional cost. On the other hand, reducing the inductance is not always desirable, particularly when several devices have to be connected in parallel in order to achieve a higher current capability. By reducing the emitter inductance, the device switching speed will become much faster and therefore more difficult to synchronize the turn-on/turn-off transients among the paralleled devices.

In the past, the stray inductance influence on the normal IGBT switching behaviour has been discussed in terms of switching loss reduction and switching oscillations, leading to very robust technologies [4]. Nevertheless, the expected IGBT module robustness during short-circuit operations may be constrained due to instability mechanisms involving the external circuit network, such as high-frequency oscillations [5]. Short circuit oscillations have previously been presented in the literature and its mitigation has been deeply investigated from the circuit design perspective: (a) increasing the gate resistance [6], (b) minimizing the gate-emitter inductance [7], and (c) proposing stability criteria to avoid the unstable regions [8]. Even though the prior-art research has discussed the oscillation trends depending on the RLC circuit variations, another type of oscillation has been found in [9] and therefore its dependency on the stray inductance variations is not known. The purpose of this investigation is to gain a better understanding of the possible stray inductance variations and their effects on the short-circuit oscillations with the help of experiments and FEM simulations.

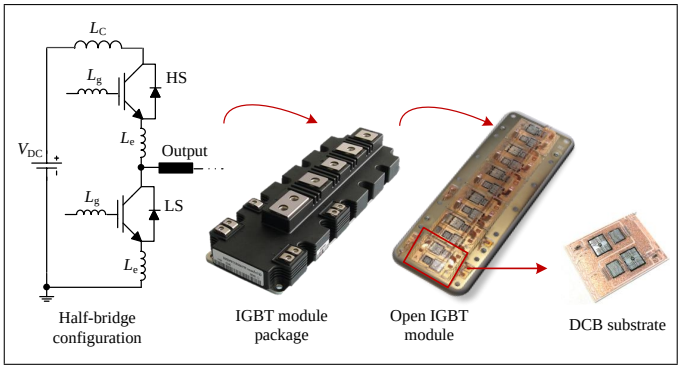

Fig. 1: The 1.7-kV/ 1-kA IGBT module showing its internal layout. HS: High Side, and LS: Low Side.

2. Selected Layout Designs

In commercial IGBT power modules, such as the 1.7-kV/ 1-kA IGBT module in Fig. 1 , IGBTs and diodes are commonly arranged in parallel-connected DCB (Direct Copper Bonded) substrates. Each DCB substrate contains two IGBT chips and two freewheeling diodes, which are configured as a half-bridge. In general, when paralleling IGBTs, the stray inductance of the emitter bond wires shares a common path between the gate and the power loop. In this way, the IGBT switching speed can be slowed down for ensuring balanced current sharing among paralleled DCBs. Nevertheless, this shared inductance on the emitter side seems to be crucial in case of a short-circuit condition. In the following, a comparison between three different layouts with special focus on the stray inductances will be given using the Finite-Element-Method AnSYS Q3D Extractor. The geometries have been drawn in SolidWorks and then exported to Q3D. The DCB dimension is 39 x 59 mm^2, the IGBT size is 13.58 x 12.58 mm^2 and the diode size is 9.58 x 9.58 mm^2. The bond wire diameter is 0.25 mm and the material used is aluminium.

2.1. Layout 1

To make the study more meaningful with the industry standard package, the layout outline of a commercial 1.7-kV/ 1-kA IGBT module was selected. The following study will be focused on the short-circuit performance of a single IGBT mounted on one DCB substrate, that is one of the six sections of the whole module, as highlighted in Fig. 1. A better view of the geometry can be observed in Fig. 2a. The ANSYS Q3D Extractor is used to perform electromagnetic simulations and extract the AC self- and

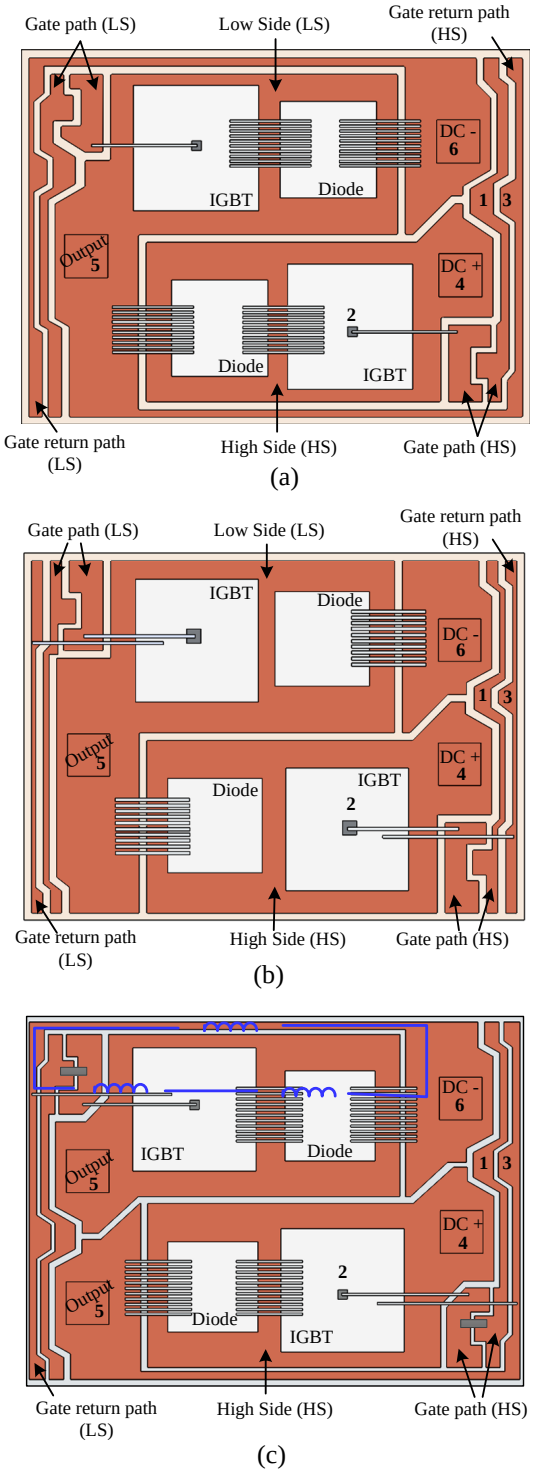

Fig. 2: Layout comparison of a single DCB design section of the IGBT power module: (a) Layout 1, (b) Layout 2, and (c) Layout 3.

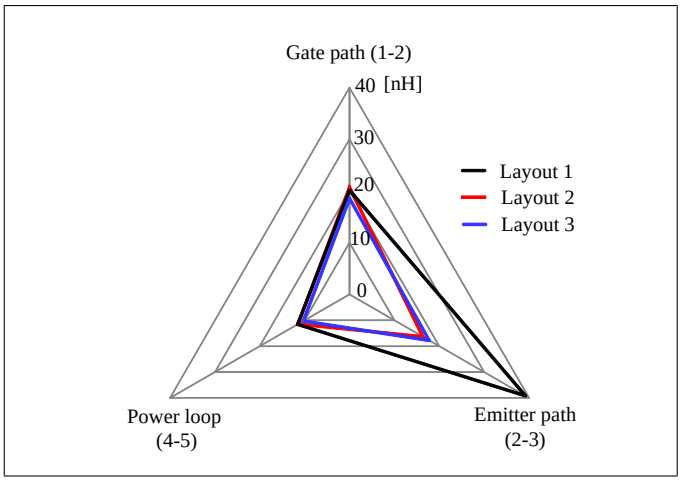

Fig. 3: Extracted stray inductances of the three layouts by Q3D at 100 kHz including self and mutual inductance.

mutual inductances at 100 kHz. Referring to Fig. 2, the paths from points 1-2 and 2-3 which can be found in the figure are the gate and gate-return loops of the high side, respectively. The path from points 4-5 is the main circuit loop from the positive to the output terminal. Since the high side IGBT will be tested later under short-circuit, only the simulation results from the high side are presented in Fig. 3.

2.2. Layout 2

Fig. 2b shows the Layout 2. With reference to Layout 1 (Fig. 2a), the inductance of the emitter bond wires and DCB trace, which constitutes the power loop path, shares fractions with the gate return path. This shared inductance, L_σ, prevents fast current changes by voltage feedback on the gate loop. The aim of Layout 2 is to reduce the emitter inductance by decoupling the gate loop from the power loop with an additional bond wire from the IGBT emitter to the gate return trace (see Fig. 2b). The cancellation of the parasitic shared inductance leads to faster switching transients and therefore higher turn-off over voltages, which could be compensated with increased gate resistance. The extracted AC inductances at 100 kHz can be observed in Fig. 3. From this graph, it is clear that layout 2 gives a more optimum solution in terms of stray emitter inductance reduction.The effect of L_e on the short-circuit performance will be demonstrated in the next section.

2.3. Layout 3

Layout 2 demonstrated that the best solution for minimizing the gate-return path inductance is by separating the gate path from the power loop path. In case that is not feasible to do that, i.e., excessive voltage spikes or too fast commutations, the Layout 3 presented in Fig. 2c can be adopted instead. This configuration has an additional bond wire from the emitter IGBT to the gate return trace forming a loop, which can be analysed as a triangle of inductances, as it is observed in Fig. 2c: 1) from the IGBT emitter to the gate-return path emitter, 2) from the IGBT emitter, through the bond wires to the output phase terminal, and 3) from the output phase terminal to the gate return bond wire. The resulting AC extracted stray inductances at 100 kHz can be compared with the other layouts in Fig. 3, the major difference is observed for the emitter inductance value.

3. Short-Circuit Experimental Results

The three layout configurations evaluated in the previous section have been tested under short-circuit conditions. The testing facility used to perform repetitive short-circuit tests on the DCB substrates is the 2.4-kV/ 10-kA Non-Destructive Tester at CORPE, Center Of Reliable Power Electronics, Aalborg University, Denmark [10]. In the following, it will be demonstrated that single IGBT chips show an instability mechanism occurring under short-circuit type 1, which causes oscillations clearly seen on the gate voltage waveform. The short-circuit sequence has been done by increasing the short-circuit pulse in steps of 1 μs and varying the DC-link voltage. Such oscillations are more prone to occur under low DC-link voltages as previously investigated in [9], hence, the short-circuit experimental waveforms presented in the following will be shown for low DC-link voltages.

Fig. 4 shows the experimental short-circuit results performed on the high-side IGBTs of the three DCB layouts. The influence of the emitter inductance in reducing the commutating di/dt is clearly observed in Fig. 4 , where Layout 1 has the highest emitter inductance and Layout 2 has the lowest. The effect of the emitter inductance leads to an overshoot on the

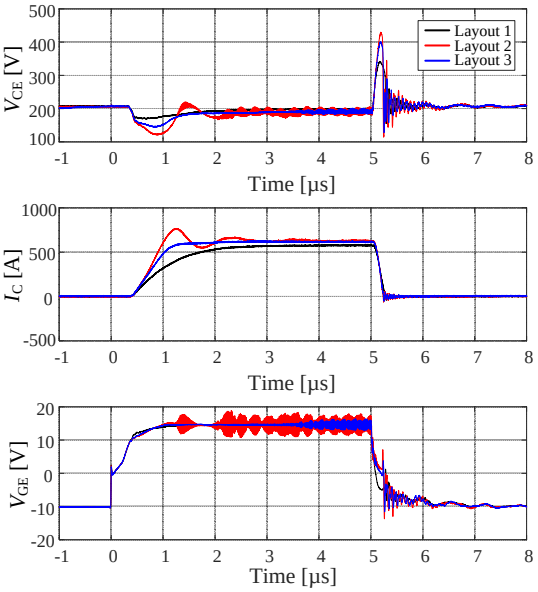

Fig. 4: Emitter inductance effect on the short-circuit oscillations of a single IGBT for three different DCB solutions. Testing conditions: V_{GE} = 15 V, V_{CE} = 200 V, T = 25 °C.

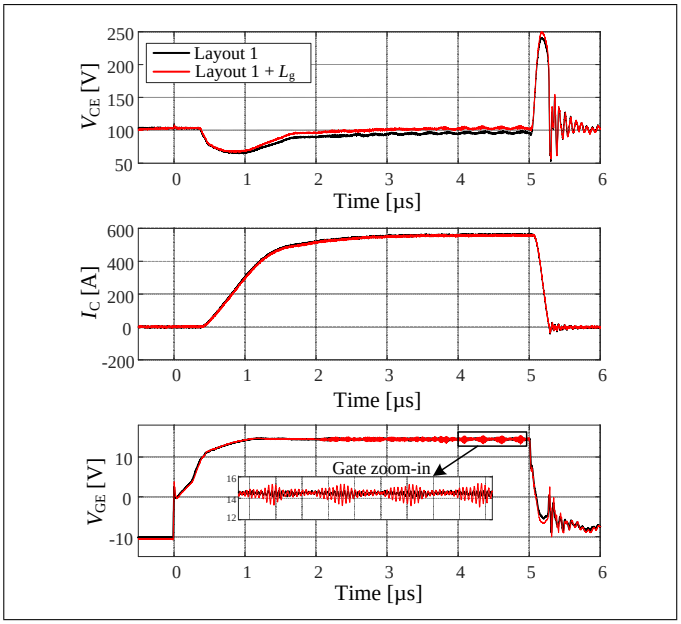

Fig. 5: Gate inductance effect on the short-circuit oscillations for Layout 1. Testing conditions: V_{GE} = 15 V, V_{CE} = 100 V, T = 25 °C.

collector current I_C coinciding at the same time with the highest voltage drop at the collector-emitter voltage V_{CE}. The combination of high collector current and low collector-emitter voltage seems to be correlated with the occurrence of gate-voltage oscillations under the short-circuit event. Here, one of the strategies for achieving higher short-circuit robustness can be derived - the lower di/dt, the better. Overall, if the emitter inductance value is correctly selected, packaging designers can gain three main features: (a) it minimizes the risk of unsynchronized switching in case that many chips are arranged in parallel, (b) it reduces possible electromagnetic interferences and (c) it helps to mitigate the oscillatory behaviour under short-circuit events.

The short-circuit experiments in Fig. 4 point out that Layout 1 performs quite well under short-circuit conditions without showing critical oscillations. However, the original module has 6 DCB sections connected in parallel, having the external gate terminal positioned at the edge of the package. This means, that the furthest DCB section from the external gate terminal has a higher gate inductance compared with the nearest one. To investigate the effect of higher gate inductance keeping a given geometry, Layout 1 has been tested with a larger gate wiring cable. The result can be seen in Fig. 5, where a higher amplification on the gate waveform is appreciated with higher gate inductance designs.

4. Short-Circuit Device Simulation Results

Using the Sentaurus TCAD device simulation tool [11], mixed-mode simulations have been performed to investigate the short-circuit operation of the IGBT. The short-circuit oscillations in IGBTs have been reproduced through simulations making this analysis possible. By looking at the IGBT internal physic quantities in Fig. 6, it has been found that during short-circuit the mobile carriers strongly influence the charge distribution in the n-base of the IGBT, and therefore play a major role in determining the shape of the electric field. In Fig. 6, the evolution of the IGBT from its blocking state to the short-circuit condition in terms of electric field and electron density can be observed. Here, it can be noted that the electric field peak transfers from the emitter side (blocking state) to the collector side (short-circuit condition), similarly to the Kirk Effect commonly observed in BJTs. This, in turn, leads to a charge storage effect at the surface of the IGBT, as pointed out in Fig. 6. The observed Kirk Effect

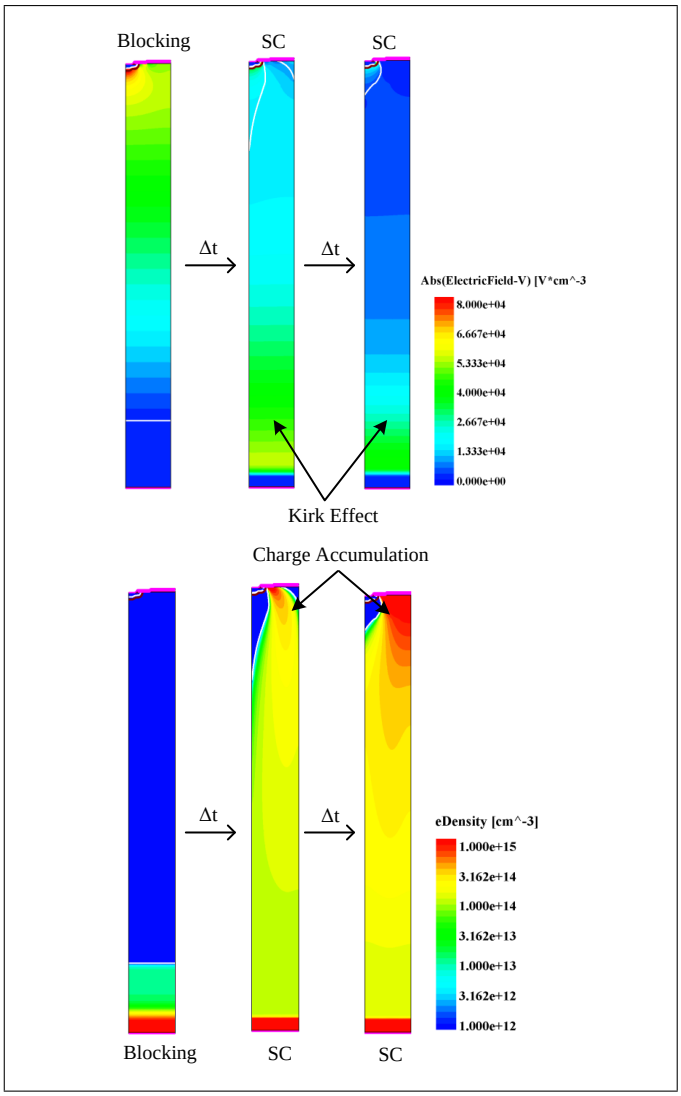

Fig. 6: Simulated IGBT showing the electric field and electron density distributions from blocking to short circuit (SC).

phenomenon is in agreement with the experimental results in Fig. 4, since the oscillations are easily triggered at high collector current values in combination with low collector-emitter voltages.

To demonstrate the oscillation dependency as a function of the stray inductance variations, i.e., collector inductance L_C, gate inductance L_g and emitter inductance L_e, device simulations have been done with one parameter varied at a time, keeping the rest of the parameters at their reference values. In Fig. 7 the simulated gate voltage oscillations are compared as a function of stray inductance variations, demonstrating that it is beneficial to design layouts with low gate inductance, low collector in-

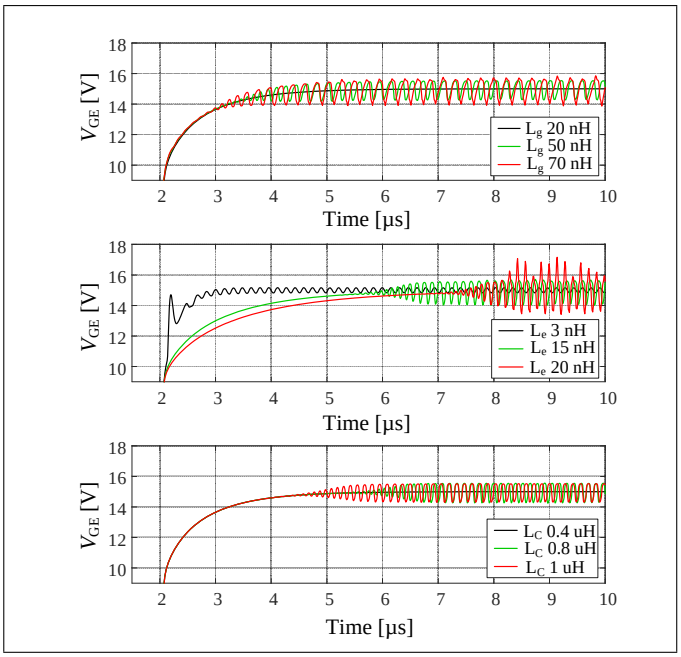

Fig. 7: Short-circuit simulation of a 3.3-kV IGBT half-cell at 1000 V illustrating the oscillation dependency as a function of stray inductance variations.

ductance and high emitter inductance. Additionally, the simulation results are in agreement with the experimental ones, in which Layout 2 having the smallest emitter inductance, shows oscillations occurring earlier in time, similarly to the simulation results when the emitter inductance has been set to the smallest value of 3 nH. Another important observation made from the simulated results is that a large gate inductance contributes to a higher amplification, which it is again in agreement with the experimental results.

5. Proposed Layout for higher Short-Circuit Robustness

With the aim of improving the short-circuit ruggedness against short-circuit oscillations, the layout presented in Fig.8a is proposed. The most important requirement for achieving higher ruggedness is to ensure minimum inductance on the collector L_C and the gate L_g, and slow switching transients. The previous layout solutions are based on the traditional anti-parallel phase-leg inverters, which means that the high side IGBT and diode are connected closer to each other and therefore the power loop length is relatively large. As discussed in [12], P-cells and

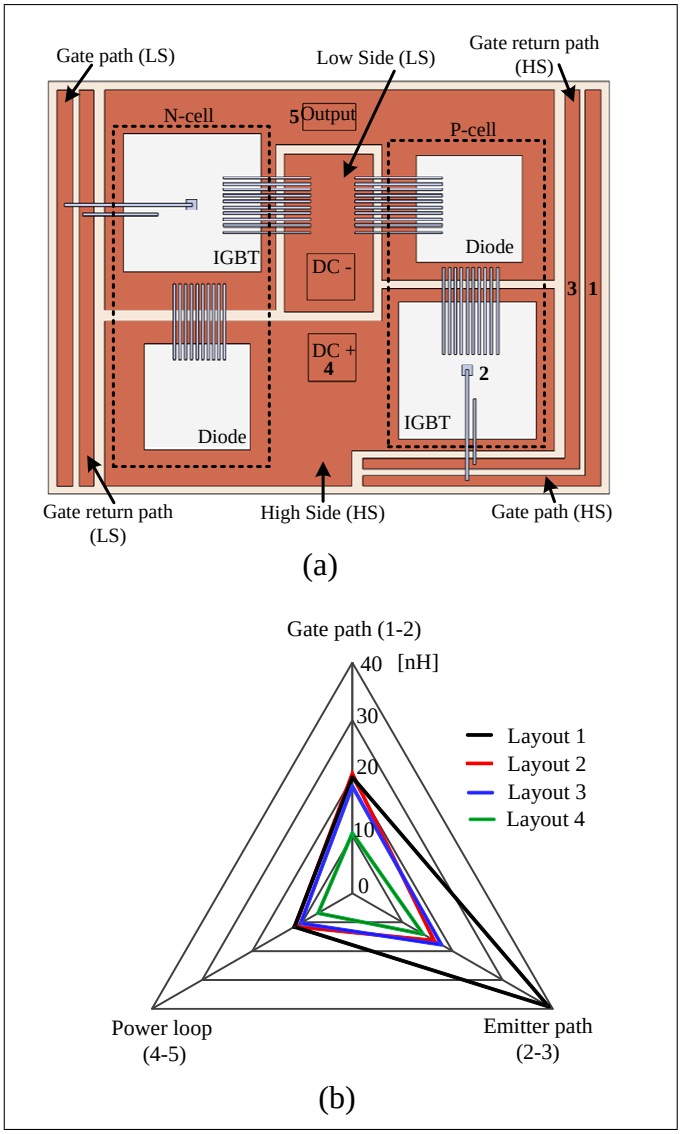

Fig. 8: Optimized layout in terms of stray inductance reduction to mitigate short-circuit instabilities: (a) Layout 4, (b) extracted inductance by Q3D.

N-cells bring the benefit of minimizing the power loop inductance, so this layout concept is adopted here. In Fig. 8b, a comparison between the four layouts is given in terms of stray inductances, which have been extracted from Q3D simulations. It is clear that Layout 4 gives a more optimum solution by minimizing the inductance for both power and gate loops. One may notice that the emitter inductance of Layout 4 is quite small, and therefore not suitable for normal switching or short-circuit requirements [9]. However, the switching speed can be controlled with an additional gate resistance in order to obtain the desired switching speed under normal conditions and thus smoother short-circuit waveforms, mitigating short-circuit instabilities. Many other layouts are possible, but one has to fulfil with the requirements coming from manufacturability aspects, for example perpendicular bond wires are not allowed on the same chip.

6. Conclusion

The short-circuit oscillation behaviour which is typically seen in IGBTs has been investigated with respect to external stray inductance variations. In order to understand the parasitic effects on the short-circuit behaviour, different layout concepts have been proposed and compared through layout design, stray inductance extraction, device simulation and experimental measurement. The results demonstrate that short-circuit oscillations are less critical with low-inductive designs and at the same time ensuring slow di/dt transients. The short-circuit experiments together with finite-element device simulations indicate which strategies should be followed for achieving higher short-circuit robustness. On this basis, Layout 4 is the best candidate. Although the origin of such oscillations is due to capacitive time-varying effects coming from the unstable Kirk Effect mode and the charge storage accumulation at the surface of the IGBT, the amplification behaviour can be mitigated if proper layout solutions are adopted.

Acknowledgement

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