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Advanced Accelerated Power Cycling Test for Reliability Investigation of Power Device Modules

Ui-Min Choi, *Student Member, IEEE*, Søren Jørgensen, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—This paper presents an apparatus and methodology for an advanced accelerated power cycling test of insulated-gate bipolar transistor (IGBT) modules. In this test, the accelerated power cycling test can be performed under more realistic electrical operating conditions with online wear-out monitoring of tested power IGBT module. The various realistic electrical operating conditions close to real three-phase converter applications can be achieved by the simple control method. Further, by the proposed concept of applying the temperature stress, it is possible to apply various magnitudes of temperature swing in a short cycle period and to change the temperature cycle period easily. Thanks to a short temperature cycle period, test results can be obtained in a reasonable test time. A detailed explanation of apparatus such as configuration and control methods for the different functions of accelerated power cycling test setup is given. Then, an improved *in situ* junction temperature estimation method using on-state collector–emitter voltage $V_{\mathrm{CE_ON}}$ and load current is proposed. In addition, a procedure of advanced accelerated power cycling test and test results with 600 V, 30 A transfer molded IGBT modules are presented in order to verify the validity and effectiveness of the proposed apparatus and methodology. Finally, physics-of-failure analysis of tested IGBT modules is provided.**

***Index Terms*—Failure mechanism, insulated-gate bipolar transistor module, lifetime model, power cycling test, physics-of-failure, reliability.**

I. Introduction

POWER electronic systems play an important role in a wide range of applications for power generation, distribution, and consumption in order to achieve high efficiency and also achieve high performance of the systems [1], [2]. As power electronic systems have gradually gained an important status in the power infrastructure, reliability improvement and lifetime prediction of power electronics are two important research topics [3]–[5].

The power electronic systems consist of various components. Among them, power devices are one of the reliability-critical components [6]–[8] and thus play a key role in the robustness and reliability of overall power electronic systems. In [3], the critical stressors for different components in power electronic systems have been summarized. It can be noted that the temperature cycling and the steady-state temperature greatly influence a failure of power devices. Therefore, much research has been done on reliability of power device modules regarding temperature stresses such as analysis of failure mechanisms, lifetime modeling, and lifetime estimation of power devices under various operating conditions of different applications [9]–[14].

The accelerated power cycling test is an important test to investigate the reliability performance of power device modules regarding temperature stresses [14]–[18]. By performing the power cycling test, failure mechanisms due to temperature stresses can be studied [16]. Further, new device packaging materials and designs can be evaluated [17], [18]. Also, lifetime models can be developed based on the power cycling test results [19] which can be used for lifetime estimation of power device modules under given mission profiles [20].

Most power cycling tests have been performed with simple designed test setup, where the load pulse with constant DC current source is applied to the power device modules under test. The temperature of the tested module is increased by the conduction losses. When the temperature increases to a desired maximum temperature, the applied power is disconnected and the temperature is decreased by an external cooling system. This period is defined as cycle period and it is repeated until the tested module fails. The duration and amplitude of current pulse are changed in order to obtain the specific junction temperature swing ΔT_j and mean junction temperature T_{jmean} [14]. However, in this test, the tested module is not operated under realistic electrical conditions. There are no switching loss, high DC-link voltage, etc. Further, an overload current may be required for high temperature swing in a short period, because the junction temperature is increased by only the conduction losses. In addition, there is a lack of study on the effect of the operating conditions of the power modules on the test results and thus this effect is still an open question [21]–[23]. Therefore, the power cycling test under more realistic electrical operating conditions is needed in order to minimize the uncertainty which may be able to come from other parameters or test conditions and to affect test results.

Several accelerated reliability tests have been performed at product level with real loads such as a motor [23]–[25]. However, the power cycling test with real load is not cost-effective because the real load generates large power losses during tests. Further, it requires a long test period. In addition, in the case of power cycling test with only small load inductors, there are limitations to emulate the various operating conditions such as power factor, modulation index, etc.

In [16], the ac power cycling test based on the circuit proposed in [33] has been performed. This circuit allows

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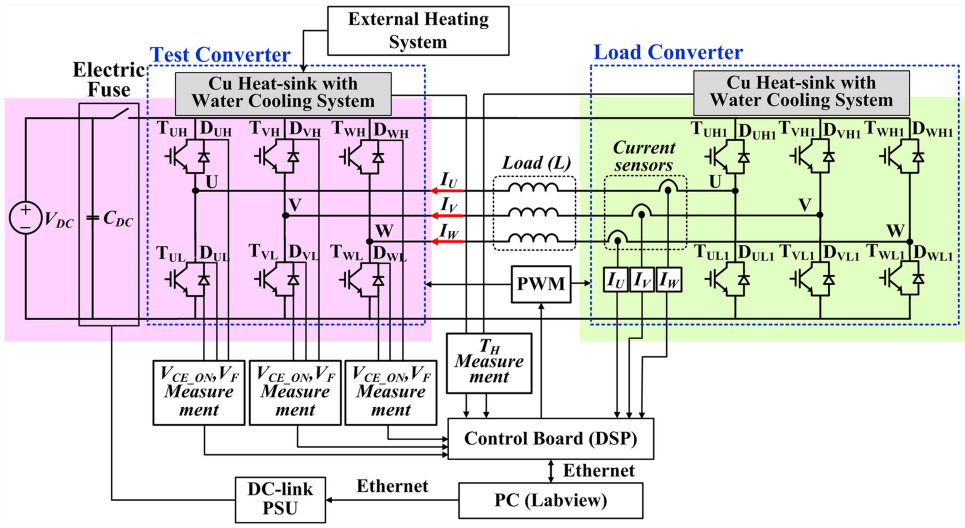

Fig. 1. Configuration of the power cycling test setup.

performing the power cycling test under more realistic converter operation compared with conventional DC test with small power losses. However, in this setup, some features such as online monitoring system are required for more advanced power cycling test. Further, some detailed information for the test such as configuration and control method of the test setup and test procedure are still needed. There is a still lack of quantitative study on the ac power cycling test in the existing test activities.

In this paper, an apparatus and methodology for an advanced accelerated power cycling test dedicated to power device module degradation are presented. The test setup is developed based on the concept of circuit in [33] with more advanced features such as online on-state collector emitter voltage circuit and DC fuse for the protection. The advantages of this setup are the following. First, the accelerated power cycling tests can be performed under more realistic operating conditions with online wear-out monitoring of tested modules. Second, by the proposed concept of applying temperature stress, it is possible to generate various magnitudes of temperature swing in a short cycle period and to change the temperature cycle period easily. Thanks to a short temperature cycle period, test results can be obtained in a reasonable test time. Finally, the power losses during the power cycling test can be kept low and thus it is cost-effective solution. This is an important factor for accelerated power cycling test because power cycling test may last for a long period until the test module reaches a certain degradation level or failure.

In the first section of this paper, the explanation of test setup such as configuration and control methods for different functions of advanced accelerated power cycling test is given in detail based on [37]. Then, an improved *in situ* junction temperature estimation method using on-state collector–emitter voltage $V_{\mathrm{CE_ON}}$ and load current is proposed. Finally, a procedure of advanced accelerated test and experimental results with physics-of-failure analysis are presented.

II. Advanced Accelerated Power Cycling Test Setup

A. Configuration of Accelerated Power Cycling Test Setup

Fig. 1 shows a configuration of an advanced accelerated power cycling test setup. Two three-phase converters are connected through load inductors (L). One is a test converter and the other one is a load converter. An insulated-gate bipolar transistor (IGBT) module that will be tested is used for the test converter. In the load converter, an IGBT module which has a higher rated power than a tested module is used in order to reduce the effect of the thermal stresses on the load IGBT module during accelerated power cycling tests. By using the higher rated power module for the load converter, the load converter can run for a long time even though the tested IGBT modules are changed after a certain number of power cycling tests. These two converters are connected with a DC source (V_{DC}) via an electric fuse (see Fig. 1). If there is short-circuit current during the power cycling test due to abnormal conditions, the electric fuse disconnects the two converters from the DC source in order to protect the overall system. The detailed information for the electric fuse can be obtained in [34].

The on-state collector–emitter voltages $V_{\mathrm{CE_ON}}$ of the IGBTs and forward voltages V_F of the diodes are measured in real time by an online $V_{\mathrm{CE_ON}}$ measurement circuit to monitor the wear-out condition of the IGBT module under the test [26]. $V_{\mathrm{CE_ON}}$ is a good indicator to determine the wear-out level of the power device module regarding bond-wire lift-off, delamination of the solder joints and chip metallization degradation [27], [28]. Further, the junction temperature of the IGBT and diode can also be estimated by $V_{\mathrm{CE_ON}}$ and V_F, respectively, because it is one of temperature-sensitive electrical parameters in the IGBT module [29], [30].

The two converters are controlled by a digital signal processor (DSP) and Labview interface communicates with the DSP to manage and monitor the overall system. A water cooling system and external temperature controllable heating system are used

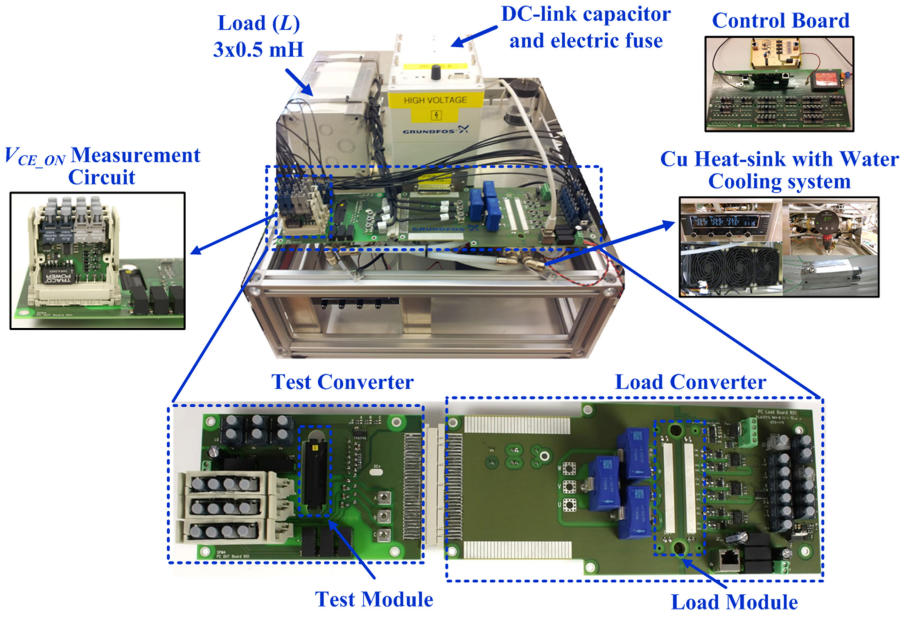

Fig. 2. Prototype of the advanced accelerated power cycling test setup.

to change the heat-sink temperature according to the desired test conditions and to keep the heat-sink temperature as a constant during the power cycling test.

Fig. 2 shows a prototype of the advanced accelerated power cycling test setup. A power circuit board consists of three parts: test converter board, load converter board, and $V_{\mathrm{CE_ON}}$ measurement board. In this system, a 600 V, 30 A, three-phase transfer molded intelligent power IGBT module is used for the test converter and a 1200 V, 75 A, three-phase IGBT module is used for the load converter.

The IGBT module under test is replaced with a new one after the power cycling test and the test converter board is also changed sometimes to a new one if the board is worn out. Therefore, the power circuit board has been designed by applying the plug-and-play concept. The boards can be separated from each other easily and components, which are put on the test converter board, are minimized to avoid the unnecessary replacement of components. In this topology, there are only power losses by the tested and load IGBT modules, which are the switching and conduction losses and the loss from load inductors. Further, only a small value of inductors is needed for the loads in order to get an acceptable low ripple current. Therefore, although the rated output currents are generated, the power losses by the test setup can be kept low.

B. Operating Principle of Power Cycling Test Setup

Output of each test converter leg and output of corresponding load converter leg are connected through each load inductor and the load inductors are not connected to each other as shown in Fig. 1. Therefore, this system is controlled like three single-phase half-bridge converters. For example phase-U, the test converter generates the output voltage ($V_{U_\mathrm{ref_test}}$) that fulfills required test conditions like magnitude, output frequency with a determined switching frequency and the load converter produces the output voltage in order to generate the current with desired magnitude, frequency, and power factor. The output phase current of the converter (I_U) is considered as the current in the *d*-axis in the stationary frame when it is controlled. The *q*-axis current in the stationary frame can be made by shifting the *d*-axis current in the stationary frame by 90° using an all-pass filter as shown in Fig. 3. The *d*- and *q*-axis currents in the stationary frame are converted to the currents in the synchronous frame with a phase angle. The real power is aligned to the *d*-axis and the imaginary power is aligned to the *q*-axis in the synchronous frame. Then, they become the input to proportional-integral current controllers, separately. The output of each current controller becomes the reference output voltages ($V_{\mathrm{de_ref}}$ and $V_{\mathrm{qe_ref}}$) in the synchronous frame. By inverse transformation, the output reference voltages $V_{\mathrm{de_ref}}$ and $V_{\mathrm{qe_ref}}$ are converted to voltages in the stationary frame ($V_{\mathrm{ds_ref}}$ and $V_{\mathrm{qs_ref}}$), where the *d*-axis reference voltage $V_{\mathrm{ds_ref}}$ becomes the reference voltage of the load converter ($V_{U_\mathrm{ref_load}}$).

The output current (I_U) is generated by the difference of the output voltages (V_L) between the test and load converters, which is applied to the inductor as shown in Fig. 4. It means that the voltage is applied across the inductor during a short period. Therefore, small value inductors are enough as loads of the converter in this test setup in order to obtain an acceptable low current ripple. In this specific system, 0.5 mH inductors are used. The power factor of output currents can be varied by changing the magnitude and polarity of the *d*-axis and *q*-axis currents. By changing the power factor, the focused device for the power cycling test can be chosen. For example, under PF $= 1$ which is inverting mode, the losses in the IGBTs are dominant and thus they have the larger thermal stresses than diodes. On the contrast, under PF $= -1$, the diodes have the larger thermal stresses than IGBTs like converter and rectifier.

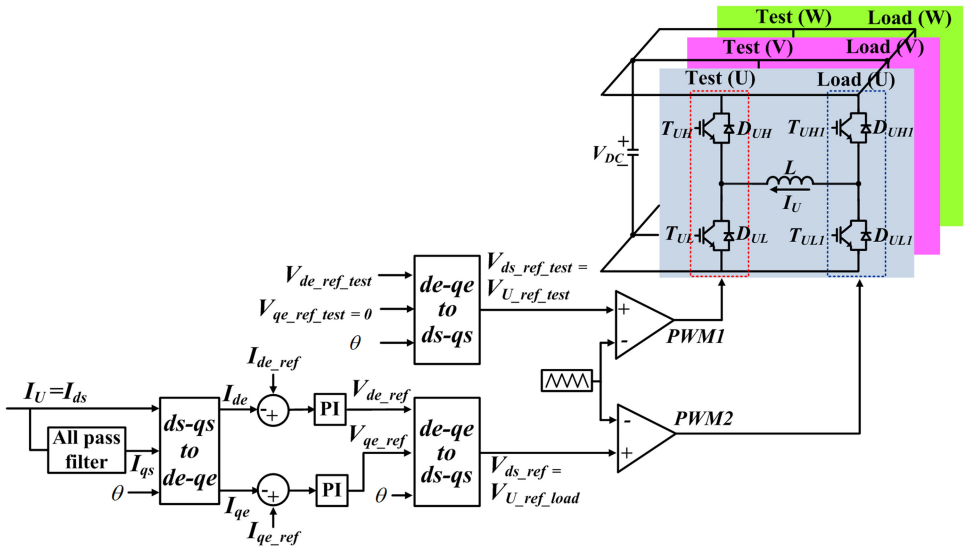

Fig. 3. Control block diagram of the converter for the accelerated power cycling test.

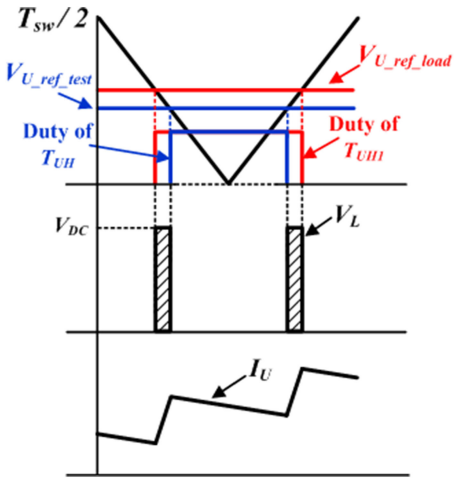

Fig. 4. Reference voltages for load and test converters and corresponding inductor voltage and output current.

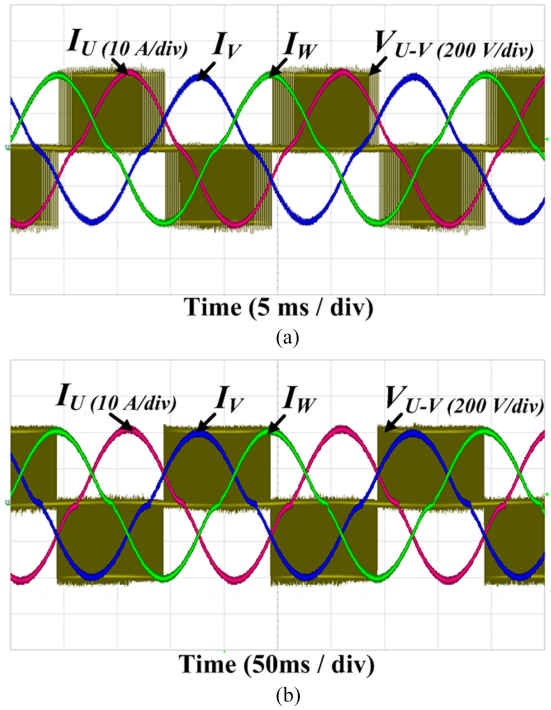

Fig. 5. Output of the test setup under various operating conditions when $I_{\rm ref} = 20$ A, $V_{\rm DC} = 400$ V. (a) $f_{\rm OUT} = 50$ Hz, PF $= 1$ (inverting mode), (b) $f_{\rm OUT} = 5$ Hz, PF $= -1$ (converting mode).

The controls for the other phases are the same as explained earlier but there are only 120° and 240° shifting in phase angle, respectively, to simulate a three-phase converter system. The parameters like output frequency, modulation index, magnitude of the output current and voltage, power factor, switching frequency can be set to apply various thermal stresses on the test module and emulate the various operating conditions of the test converter.

Fig. 5 shows the outputs of the test setup under different operating conditions.

C. Online $V_{\rm CE_ON}$ and V_F Measurements

The on-state collector–emitter voltage $V_{\rm CE_ON}$ of an IGBT and forward voltage V_F of a diode are good indicators for determining the wear-out condition of power device modules regarding bond-wire degradation, delamination of the solder joints and chip metallization degradation. By measuring $V_{\rm CE_ON}$ and V_F, the degradation level of the tested module can be monitored during the accelerated power cycling test. Usually, 5–20% increase of $V_{\rm CE_ON}$ and V_F from its initial values is considered as wear-out failure of the power device modules [14]. Further, the junction temperature of the tested module can be estimated by measuring $V_{\rm CE_ON}$ and V_F.

Fig. 6 shows the schematic of $V_{\rm CE_ON}$ and V_F measurement circuit, described in [26] in detail.

Two diodes D_1 and D_2 are connected in series and these diodes are forward-biased by the current source (I_D) when the

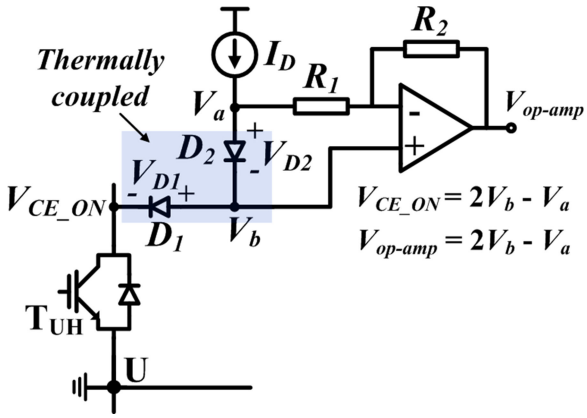

Fig. 6. Schematic of the online $V_{\mathrm{CE_ON}}$ and V_F measurement circuit.

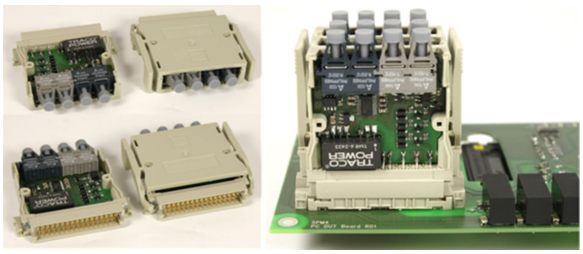

Fig. 7. Prototype of $V_{\mathrm{CE_ON}}$ and V_F measurement circuit for the power cycling test.

transistor (T_{UH}) is turned on. If T_{UH} is turned off, D_1 blocks the high V_{CE} voltage, which comes from the DC-link to protect the measurement circuitry. Assuming diodes D_1 and D_2 have the same characteristics, the forward voltage of D_1 and D_2 can be represented as follows:

$$V_{D1} = V_{D2} = V_a - V_b. \tag{1}$$

For example, T_{UH}, the $V_{\mathrm{CE_ON}}$ can be expressed by the difference between the voltage potential V_b and V_{D1} as follows:

$$V_{\mathrm{CE_ON}} = V_b - V_{D1} = V_b - (V_a - V_b) = 2V_b - V_a. \tag{2}$$

The aforementioned result can be realized by choosing properly the gain of the amplifier. If $R_1 = R_2$, the output of amplifier can be expressed as

$$\begin{aligned} V_{\mathrm{op-amp}} &= V_b - ((V_a - V_b) \cdot R_2/R_1) \\ &= 2V_b - V_a = V_{\mathrm{CE_ON}}. \end{aligned} \tag{3}$$

The output of the amplifier is the same with $V_{\mathrm{CE_ON}}$ as described earlier. $V_{\mathrm{CE_ON}}$ of the IGBT is measured during the negative current and V_F of the diode can be measured during the positive current, where the current from load converter to the test converter is positive.

Fig. 7 shows a prototype of $V_{\mathrm{CE_ON}}$ measurement circuit. To improve the resolution of the measured data, an external 14-bit analog-to-digital converter is used. It is designed compactly and it can easily be separated from the power cycling test board.

Fig. 8 shows the measured $V_{\mathrm{CE_ON}}$ and V_F of IGBTs and diodes of phase-U according to the current under the inverter operation.

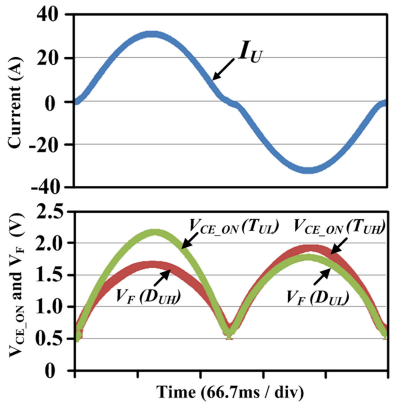

Fig. 8. $V_{\mathrm{CE_ON}}$ and V_F measurement of phase-U under the inverter operation when I_{peak} : 30 A, f_{OUT} : 3 Hz.

III. Junction Temperature Estimation

It is important to know the applied temperature stresses like junction temperature swing (ΔT_j), mean junction temperature ($T_{j\mathrm{mean}}$) when the power cycling test is performed. They are important factors when the lifetime models for power device modules are developed. Further, they are also needed when the tested modules are investigated physically to study the failure mode and the effect of the different thermal stresses on the power device modules degradation.

A simple and correct method is to use an infrared (IR) camera but it is an expensive solution as well as the module needs to be opened. In this paper, the IR camera (FLIR X8400sc), which has high accuracy of ± 1 °C or $\pm 1\%$ and therefore produces sensitive thermal images, is used to measure directly the applied temperature stresses and validate the applied methods. Using open module covered by black paint, the junction temperature is measured under certain operating conditions. Then, the same electrical operating conditions are applied to the tested power modules, which are the normal modules. However, even though the applied thermal stresses for power cycling test are known by the IR camera, it is also important to know the junction temperature variation as the tested module is worn-out in order to investigate the degradation effect of power device modules and in order to identify the failure mechanism. Therefore, the estimated junction temperature is the important parameter to be monitored. In this section, an improved junction temperature estimation method using $V_{\mathrm{CE_ON}}$ and the load current is described based on [36].

A. Preliminary I–V Characterization

A preliminary calibration is necessary to estimate the junction temperature from $V_{\mathrm{CE_ON}}$ and V_F. The purpose is to obtain the dependence of temperature on the $V_{\mathrm{CE_ON}}$ and V_F for the IGBTs and diodes, under a given current level. From the simple switching sequences with online $V_{\mathrm{CE_ON}}$ measurement, the *I–V* characterization curves for the junction temperature estimation can be obtained. The heat-sink temperature T_H is controlled by the external temperature controllable heating system. After a while, once the thermal steady-state condition is reached, the

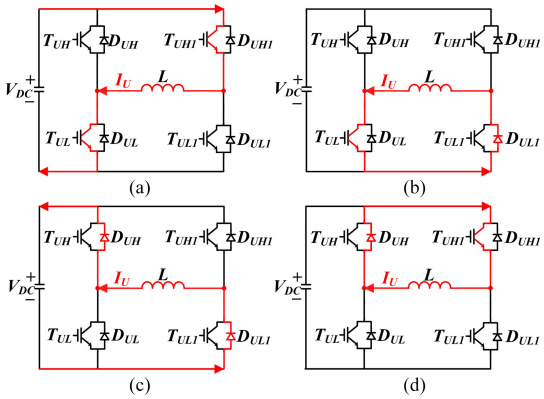

Fig. 9. Switching sequence for *I–V* characterization (a) switching for I_U increase, (b) switching for freewheeling of I_U through $T_{\rm UL}$, (c) switching for I_U decrease, and (d) switching for freewheeling of I_U through $D_{\rm UH}$.

junction temperature becomes equal to T_H, and then $T_{\rm UL}$ and $T_{\rm UH1}$ are turned on as shown in Fig. 9(a). The current level can be changed by varying the dwell time of turn-on state of $T_{\rm UL}$ and $T_{\rm UH1}$. Then, $T_{\rm UH1}$ is turned off so that the current flows through $T_{\rm UL}$ and D_{UL1} as shown in Fig. 9(b). $V_{\rm CE_ON}$ of $T_{\rm UL}$ and the current (I_U) are measured at this point. After $V_{\rm CE_ON}$ and I_U are measured, $T_{\rm UL}$ is turned off and I_U is reduced to zero as shown in Fig. 9(c). In the case of measurement for $D_{\rm UH}$, $T_{\rm UL}$ is turned off. I_U flows through $D_{\rm UH}$ and $T_{\rm UH1}$ as shown in Fig. 9(d). The forward voltage V_F of $D_{\rm UH}$ and the current are measured at this point and then $T_{\rm UH1}$ is turned off to make the current zero. This switching sequence is performed by changing the current level from the minimum value to the rated current value under the same temperature and then it is performed again at different temperature levels. Each switching sequence is performed in a short period (less than three switching periods). During this period, thermal impedance and the losses of the device are very small. Therefore, the increase of junction temperature during the switching sequence is negligible. Fig. 10 shows the output current corresponding to the switching sequences for the *I–V* characterization. Fig. 11 shows the *I–V* characterization curves for the low-side IGBT of the phase-V ($T_{\rm VL}$) at different temperatures. *I–V* characterization curves for the other components can be obtained from the similar switching principle.

B. Junction Temperature Estimation From I–V Characterization Curves

1) Conventional Estimation Method: It is needed to derive $V_{\rm CE_ON}$ as a function of temperature at a given current level in order to estimate the junction temperature T_j from the obtained *I–V* characteristic curves in Section III-A. To derive the relation between $V_{\rm CE_ON}$ and T_j, $V_{\rm CE_ON}$ should be formularized as a function of current. This can be achieved by the polynomial fitting method. Then, T_j can be represented as a function of $V_{\rm CE_ON}$ at a given current. These relations can be represented by a slope factor (K) as shown in Fig. 12.

From the previous relations, T_j can be estimated from the measured current and the $V_{\rm CE_ON}$ as follows:

$$T_{j_\rm est} = K_{(I)} \cdot (V_{\rm CE_M} - V_{\rm CE_B(I)}) + T_B \qquad (4)$$

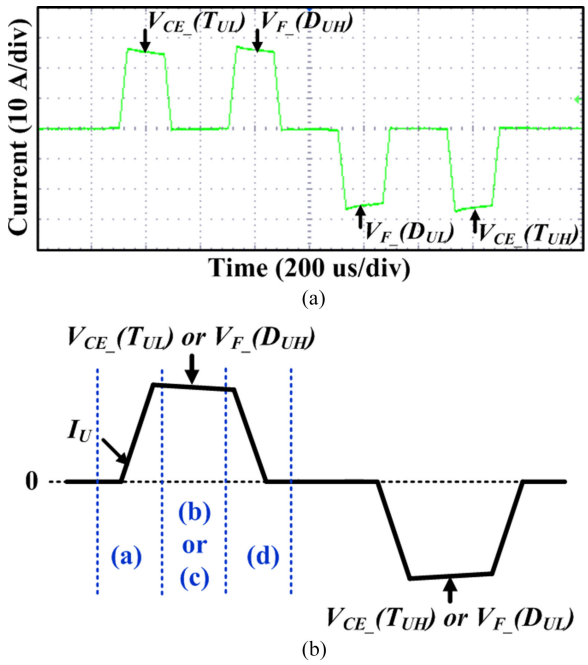

Fig. 10. Output current under switching sequence for *I–V* characterization. (a) Output current corresponding to the switching sequence. (b) Experimental result.

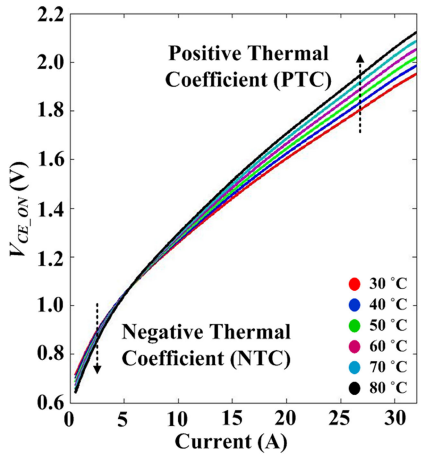

Fig. 11. *I–V* characteristic curves of $T_{\rm VL}$.

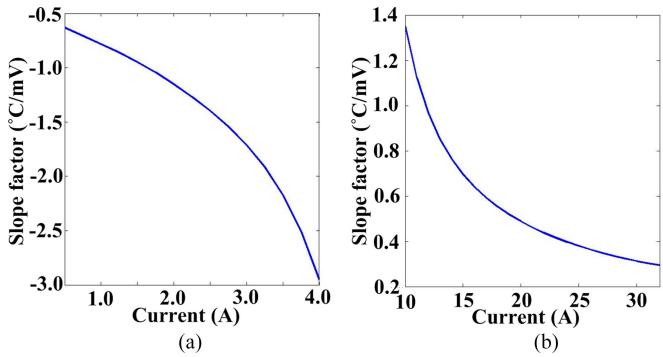

Fig. 12. Slope factors (K) as a function of current. (a) NTC region. (b) PTC region.

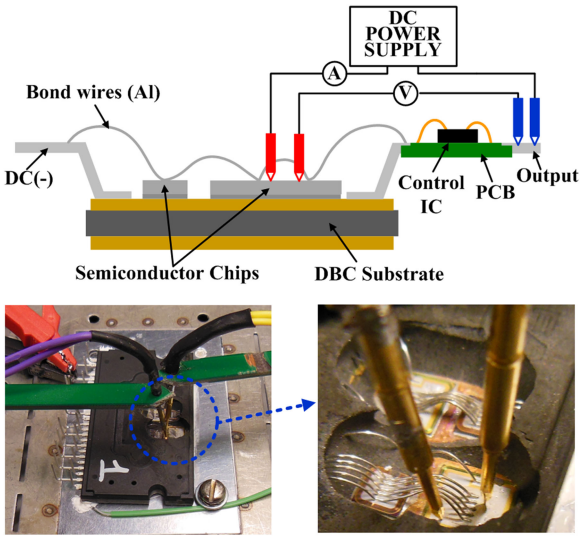

Fig. 13. Four-point probing method for the interconnection resistance measurement in an open module.

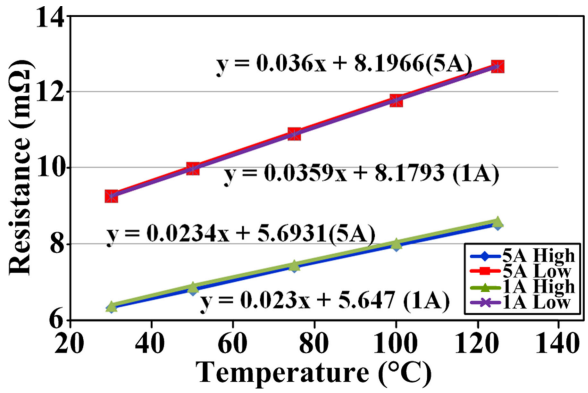

Fig. 14. Measured parasitic package resistances of high- and low-side IGBTs in the open module as a function of temperature.

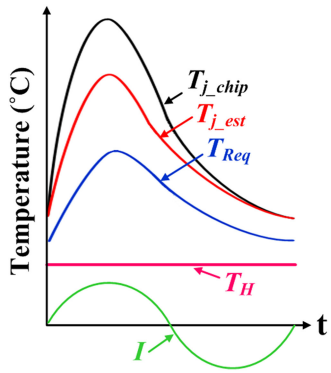

Fig. 15. Simplified temperatures in the power module corresponding to an ac current.

where T_{j_est} is the estimated temperature, $K_{(I)}$ is the slope factor as a function of current, V_{CE_M} is the measured on-state V_{CE} in real time, $V_{\mathrm{CE}_B(I)}$ is the base $V_{\mathrm{CE}_\mathrm{ON}}$ as a function of current which can be chosen among the characterization curves. T_B is the base temperature corresponding to the base $V_{\mathrm{CE}_\mathrm{ON}}$.

However, it is worth to note that packaged devices do not permit solely to measure $V_{\mathrm{CE}_\mathrm{ON}}$. In fact, each device is connected to the output pins through a series of interconnections, like bond-wire and traces. Therefore, the measured $V_{\mathrm{CE}_\mathrm{ON}}$ definitely includes the voltage drops on various interconnection elements as follows:

$$V_{\mathrm{CE}_M} = V_{\mathrm{CE}_\mathrm{Chip}} + R_{\mathrm{eq}} \cdot I_C \tag{5}$$

where $V_{\mathrm{CE}_\mathrm{Chip}}$ is the real on-state collector–emitter voltage of the chip, R_{eq} is the equivalent resistance of the interconnection elements, and I_C is the collector current.

2) Resistance Variation in an IGBT Module According to Temperature: To investigate the effect of temperature variation on the resistance in the IGBT module, resistances of the interconnection materials in the IGBT module is measured using the four-point probing approach. An open module is used to contact the probe to the emitter and collector of the device.

Fig. 13 shows the four-point probing method to measure the interconnection resistance. The resistances from the negative DC-link input pin to emitter and collector to output pin of low side IGBT and from positive DC-link input pin to collector and emitter to output pin of high side IGBT are measured by applying a DC current. Two different DC currents (1 and 5 A) have been used to check the effect of self-heating during the measurement. Moreover, two IGBT modules have been used for measurements. Fig. 14 shows the total parasitic package resistance values of high- and low-side IGBTs. No big differences are observed in the resistances between the cases of 1 and 5 A and between the two different modules. From the results, it can be concluded that the self-heating effect by the applied DC current is negligible. Further, the resistance variation factor (*RVF*) according to temperature can be obtained. Measurements of Fig. 14 yield *RVFs* 0.036 and 0.0234 mΩ/°C for low-side and high-side IGBTs, respectively.

3) Compensation for the Effect of Interconnection Resistance: As analyzed earlier, the interconnection resistances are significantly changed by the temperature and this change affects the measured voltage drop.

Fig. 15 shows the simplified temperatures in the power module corresponding to an ac current, where T_{j_chip} is the real junction temperature of the device which means the average of temperature distribution on the chip surface, T_{j_est} is the estimated junction temperature, and $T_{_\mathrm{Req}}$ is the average temperature of the interconnection materials in the module. The interconnection materials are represented by one equivalent resistor with an average temperature. If $T_{_\mathrm{Req}}$ is the same as T_{j_chip}, T_{j_est} would be the same as T_{j_chip}. However, $T_{_\mathrm{Req}}$ is not the same as T_{j_chip} under the converter operation and it leads to a lower $V_{\mathrm{CE}_\mathrm{ON}}$ measurement than the one under the characterization condition, even though, the junction temperatures are the same. Consequently, the estimated junction temperature by $V_{\mathrm{CE}_\mathrm{ON}}$ with the current is smaller than the real one. Therefore, it is necessary to compensate for the voltage drop caused by the different temperature of the interconnection materials. However, it is challenging to know the temperature of each part of interconnection materials during real operations. There is reasonable assumption, which has been further supported by

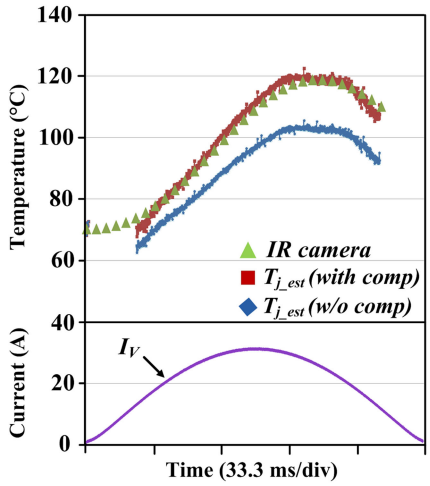

Fig. 16. Comparison of the junction temperature between IR camera and estimation using $V_{\mathrm{CE_ON}}$ with and without compensation ($f_{\mathrm{OUT}} = 3$ Hz).

the experimental validation that the temperature difference between T_{j_chip} and $T_{_\mathrm{Req}}$ during one fundamental period of the output current has the similar trend with the temperatures as shown in Fig. 15. Therefore, it can be expressed as (6) and the resistance variation can be represented as given in (7). Finally, the on-state voltage compensation $V_{\mathrm{CE_comp}}$ can be expressed as (8)

$$T_{j_\mathrm{chip}} - T_{\mathrm{Req}} = \alpha \cdot (T_{j_\mathrm{est}} - T_H) \tag{6}$$

$$\Delta R_{\mathrm{int}} = \alpha \cdot (T_{j_\mathrm{est}} - T_H) \cdot RVF \tag{7}$$

$$V_{\mathrm{CE_comp}} = \Delta R_{\mathrm{int}} \cdot I = \alpha \cdot (T_{j_\mathrm{est}} - T_H) \cdot RVF \cdot I \tag{8}$$

where T_H is the heat-sink temperature, α is the scaling factor, *RVF* is the resistance variation factor (determined in advance), and *I* is the output current.

Finally, the junction temperature estimation can be corrected as

$$T_{j_\mathrm{est_comp}} = K_{(I)} \cdot (V_{\mathrm{CE_}M} - V_{\mathrm{CE_}B(I)} + V_{\mathrm{CE_comp}}) + T_B. \tag{9}$$

To find the scaling factor (α) of a tested module, an IR camera (FLIR 8400sc) and a black-painted open module have been used. By comparing the measured junction temperature by IR camera with the estimated one, the scaling factor α can be found. α and *RVF* factors are different according to the types of modules, because they have different resistances and structures. For this reason, it is difficult to generalize both factors for all modules. Therefore, efforts to find α and *RVF* are still needed but by using the proposed approach, junction temperature can be estimated more precisely under the converter operation. In addition, $V_{\mathrm{CE_}B(I)}$ and $K_{(I)}$ need to be updated repeatedly as $V_{\mathrm{CE_ON}}$ of tested module increases during the power cycling test in order to exclude the effect of $V_{\mathrm{CE_ON}}$ increase due to the electrical degradation on the junction temperature estimation.

Fig. 16 shows a comparison of the junction temperatures measured by IR camera and estimated by $V_{\mathrm{CE_ON}}$ and load current with and without compensation. The comparison has been performed under the operating Condition 1 which is listed in Table I.

TABLE I
OPERATING CONDITIONS FOR JUNCTION TEMPERATURE ESTIMATION IN IGBT MODULE

Parameters	Condition 1	Condition 2	Condition 3	Condition 4
DC-link voltage (V_{DC})	400 V	400 V	400 V	400 V
Output current (I_{peak})	30 A	30 A	25 A	25 A
Output reference voltage (V_{ref})	140 V	140 V	140 V	140 V
Switching frequency (f_{SW})	10 kHz	10 kHz	10 kHz	10 kHz
Output frequency (f_{out})	3 Hz	1 Hz	0.5 Hz	5 Hz
Power factor (*PF*)	1	1	1	1
Heat-sink temperature (T_{H})	50 °C	48 °C	53 °C	50 °C

The maximum T_{j_IR} measured by the IR camera is about 118.8 °C and the minimum is about 70 °C. The maximum estimated junction temperature T_{j_est} before the compensation is about 103 °C and the estimation error is about 15.8 °C. After the compensation, the maximum T_{j_est} is about 120.2 °C, yielding an error of less than 1.5 °C with respect to the measured temperature by the IR camera. The estimated temperature agrees well with the measured value.

The junction temperature estimations are also performed under different operating Conditions 2–4 are given in Table I. Fig. 17 shows T_{j_IR} and T_{j_est} with compensation under the operating Condition 2. The maximum T_{j_est} is 140.2 °C and the maximum T_{j_IR} is about 142.3 °C. The temperature error between them is about 2 °C. The junction temperatures under the operating Condition 3 are shown in Fig. 18. In this case, the temperature difference between maximum T_{j_est} and T_{j_est} is about 2.3 °C. The estimated temperature is about 139.7 °C and measured one is 142 °C. Under the operating Condition 4, the maximum T_{j_est} is about 96. 5 °C and T_{j_IR} is about 97 °C as shown in Fig. 19.

As shown in the previous results, the estimated junction temperatures by the proposed method are in good agreement with the measured temperatures by the IR camera at various operating conditions.

It is worth to point out uncertainties that come also from the IR measurement technique. The measured temperatures by the IR camera are the average ones along the chip surface. For this reason, according to the area that is considered for mean temperature, the measured value can be slightly changed. Furthermore, the black paint and shading effect of the bondwire can also affect a little the measured temperature value. Therefore, the error between estimation and measurement could be changed a bit but it is not significant.

It can be concluded from the results that the accuracy of the junction temperature estimation using $V_{\mathrm{CE_ON}}$ and the load current is significantly improved by the proposed method.

IV. ADVANCED ACCELERATED POWER CYCLING TEST

A. IGBT Power Module Under Test

In order to demonstrate the capabilities of the test system, a 600 V, 30 A, transfer molded three-phase intelligent power module (IPM) has been used for power cycling test. The IPM

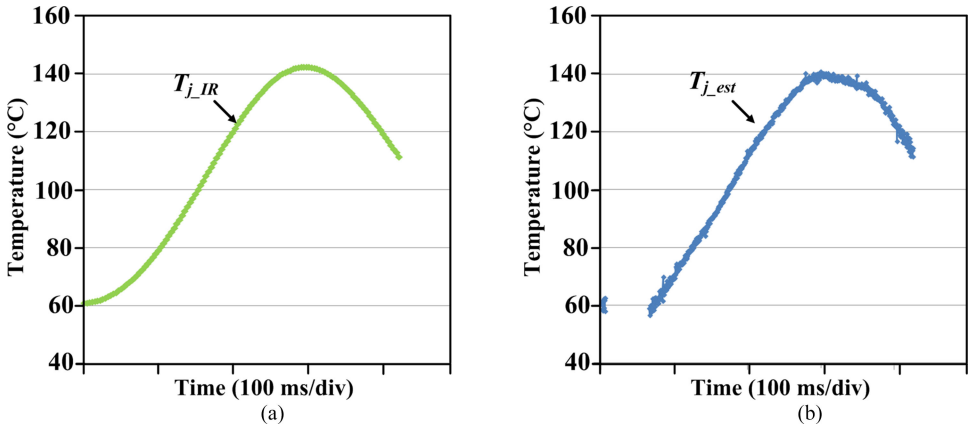

Fig. 17. Junction temperatures under the operating Condition 2 (see Table I). (a) IR camera measurement. (b) Estimation by the proposed method.

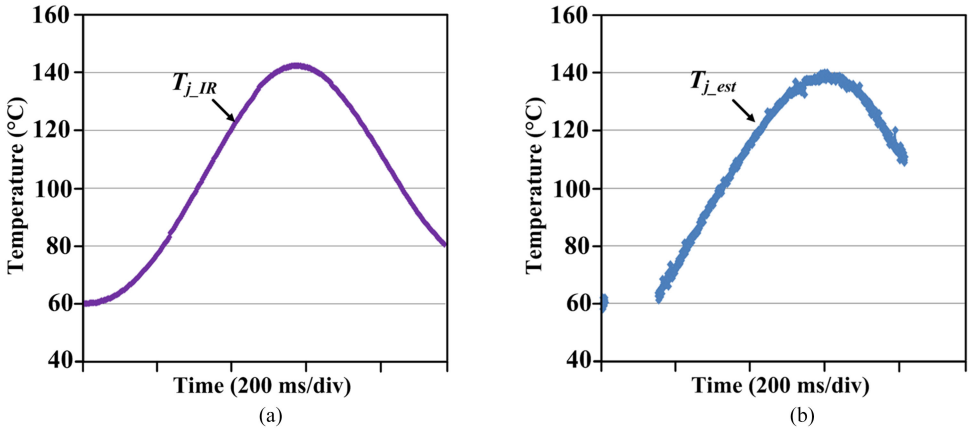

Fig. 18. Junction temperatures under the operating Condition 3 (see Table I). (a) IR camera measurement. (b) Estimation by the proposed method.

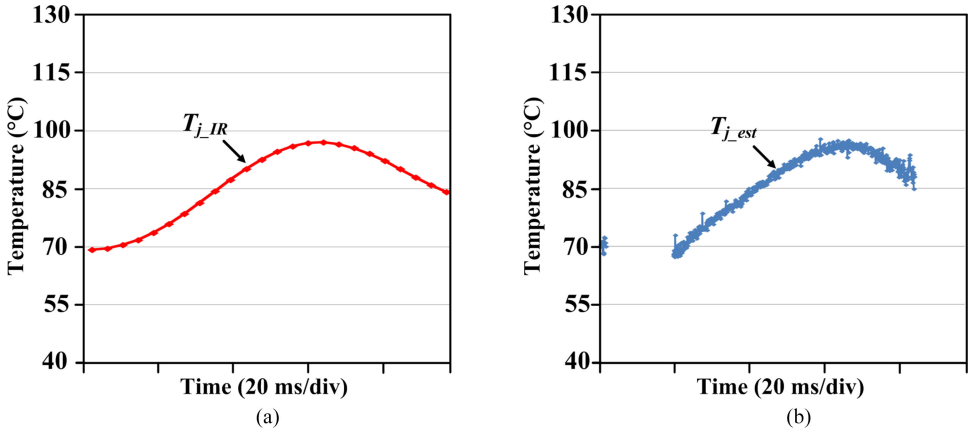

Fig. 19. Junction temperatures under the operating Condition 4 (see Table I). (a) IR camera measurement. (b) Estimation by the proposed method.

consists of six IGBTs and six diodes and they are mounted on a direct bonded copper (DBC) substrate with aluminum wire interconnection. The lead frame is connected to the DBC substrate by soldering and a copper surface of the DBC substrate is exposed to be contacted with an external heat-sink. Further, the integrated circuits (control ICs) with printed circuit board are embedded inside the module too. This module is covered by epoxy molding compound (EMC) instead of gel and there is no base-plate. Therefore, the wear-out failure mainly occurs in bond-wire and chip solder joint due to thermomechanical stresses.

Fig. 20 shows the vertical structure and configuration of the transfer molded IPM. Due to the asymmetric layout of the module, each device has different thermal resistances as shown in Fig. 21 and the difference of the thermal resistance becomes larger as the transient time increases. Since this module is

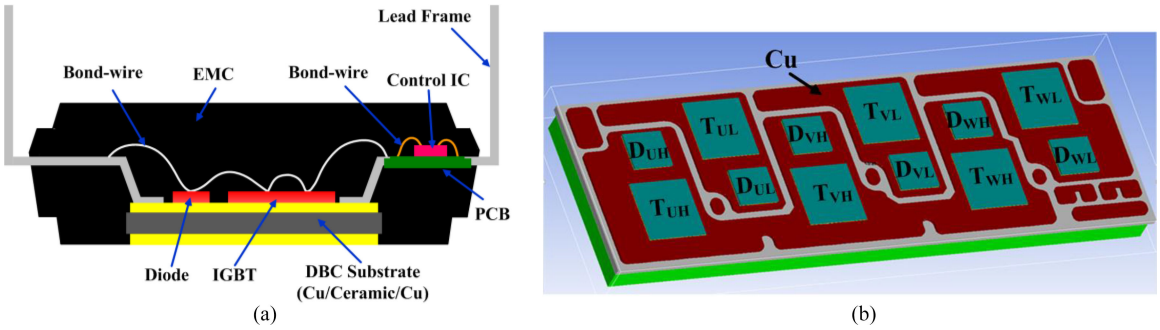

Fig. 20. Transfer molded IPM for the test. (a) Vertical structure. (b) Configuration.

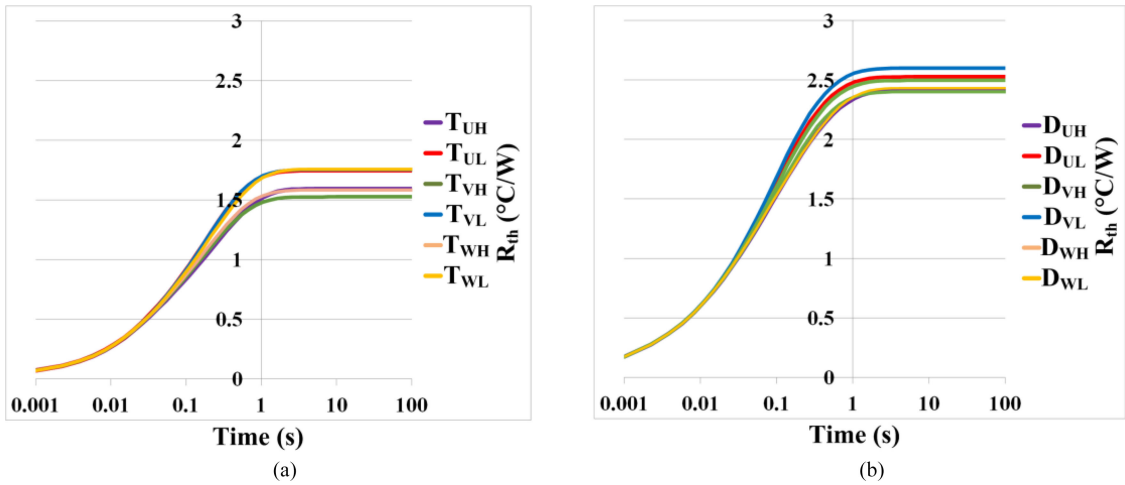

Fig. 21. Thermal impedances of chips in transfer molded IPM by finite-element method simulation. (a) IGBTs. (b) Diodes.

TABLE II
POWER CYCLING TEST CONDITIONS FOR THE IGBT POWER MODULE

Parameters	Condition 1	Condition 2
DC-link voltage (V_{DC})	400 V	400 V
Output current (I_{peak})	30 A	21 A
Output reference voltage (V_{ref})	140 V	113 V
Switching frequency (f_{SW})	10 kHz	10 kHz
Output frequency (f_{OUT})	1 Hz	0.1 Hz
Power factor (PF)	1	1
Heat-sink temperature (T_H)	48 °C	59 °C
Junction temperature swing (ΔT_j)	81.6 °C	80.8 °C
Mean junction temperature (T_{jmean})	101.5 °C	102.3 °C

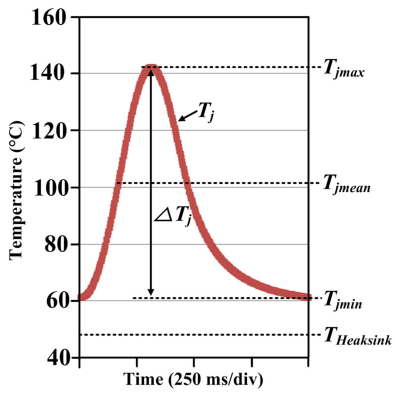

Fig. 22. Temperature profile measured by IR camera under Condition 1 in Table II.

designed for inverter applications, the IGBT chip size is bigger than diode chip size as also shown in Fig. 20(b). Therefore, the diodes have higher thermal impedance than that of IGBTs. However, in this test, the tested IGBT module is operated under inverter mode with high power factor and thus losses in IGBTs are dominant. Therefore, it leads to higher junction temperature and larger junction temperature variation than diodes.

Besides the difference between the IGBTs and diodes, each IGBT and diode have also different thermal impedances. For example, IGBTs, the copper surface area around each IGBT is different as shown in Fig. 20(b). In this module, the copper surface areas around the high-side IGBTs are wider than the copper surface areas around low-side IGBTs. A wider surface area means a smaller thermal resistance. Therefore, the low-side IGBTs have larger thermal resistance than high side IGBTs as shown in Fig. 21(a) and its difference between high- and low-sides IGBT is bigger as the transient time is longer. From this result, it can be expected that the low-side IGBTs have the highest thermal stress during power cycling test and

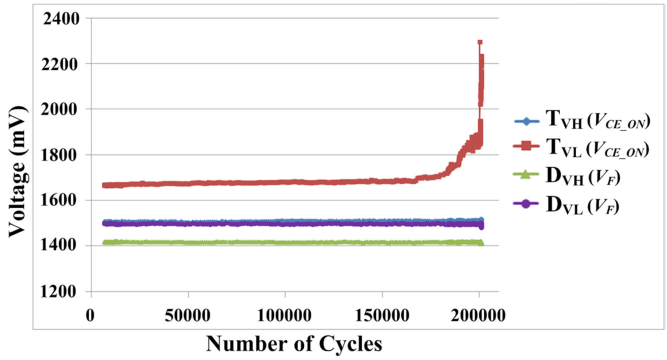

Fig. 23. Measured $V_{\mathrm{CE_ON}}$ and V_F of the IGBTs and diodes in phase-V during power cycling test under Condition 1 given in Table II.

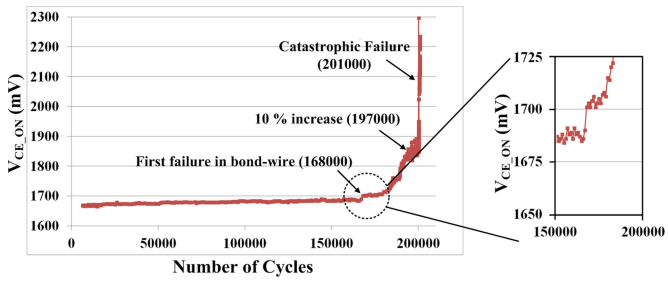

Fig. 24. $V_{\mathrm{CE_ON}}$ of low-side IGBT of phase-V in detail from Fig. 23.

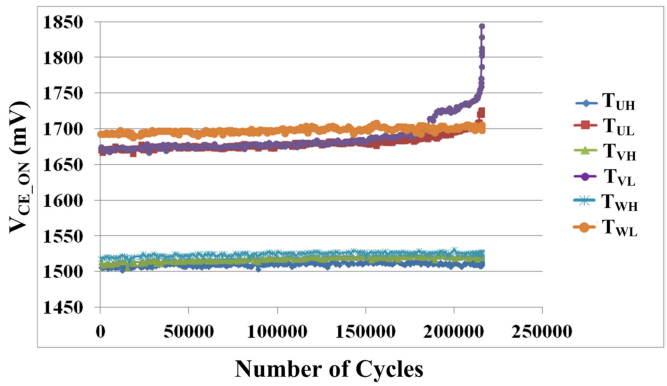

Fig. 25. Result of the advanced accelerated power cycling test under the operating Condition 1 specified in Table II.

the failure may be expected to occur among low-side IGBTs first.

B. Accelerated Power Cycling Tests

One of the important factors for accelerated power cycling test is a test time. To get the results in a reasonable test time, a proper temperature stress and temperature swing cycle period ($t_{\Delta Tj}$) should be chosen. Furthermore, $t_{\Delta Tj}$ is related to the failure mechanisms in the IGBT modules. Typically, short $t_{\Delta Tj}$ leads to the failures in bond-wire, emitter metallization and chip solder joint while relatively long $t_{\Delta Tj}$ (more than a few minutes) also provokes the failure in base-plate solder joint [15]. As mentioned earlier, the target module in this test does not have the base-plate. In addition, it is possible to generate large

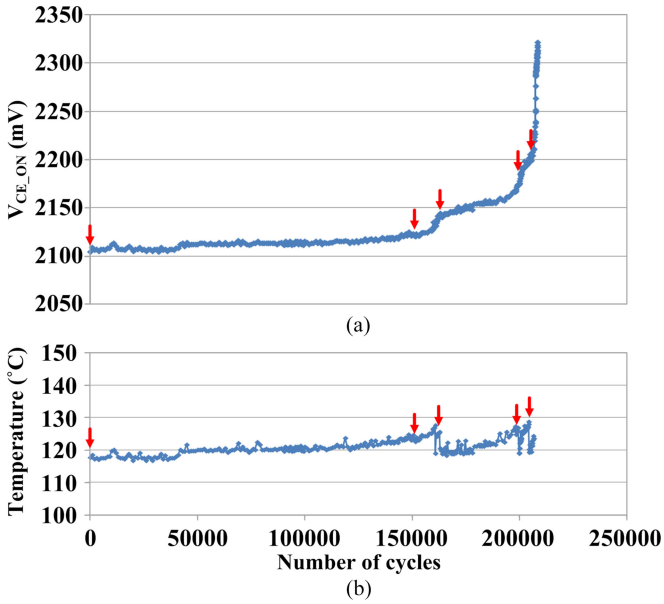

Fig. 26. Power cycling test results with junction temperature monitoring under Condition 1. (a) On-state collector–emitter voltage ($V_{\mathrm{CE_ON}}$). (b) Estimated junction temperature at 29 A.

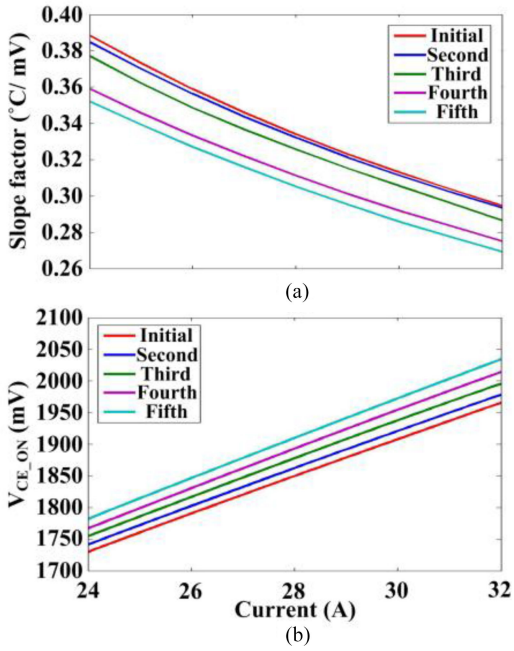

Fig. 27. Change of parameters for junction temperature estimation during power cycling test. (a) Slope factor. (b) Base $V_{\mathrm{CE_ON}}$ as a function of current ($V_{\mathrm{CE_B(I)}}$) at 30 °C (see (9)).

temperature swing in a short period in this test setup. Therefore, in this test, the power cycling period is in the range from several hundred milliseconds to a few tens of seconds and it can be achieved by changing the output frequency f_{OUT}.

Further, the powerr cycling test with different control strategies lead to different number of cycles to failure. In [31], conventional DC power cycling tests are performed with different four control strategies and results are compared. As the tested module is degraded during the test, the temperature swing and

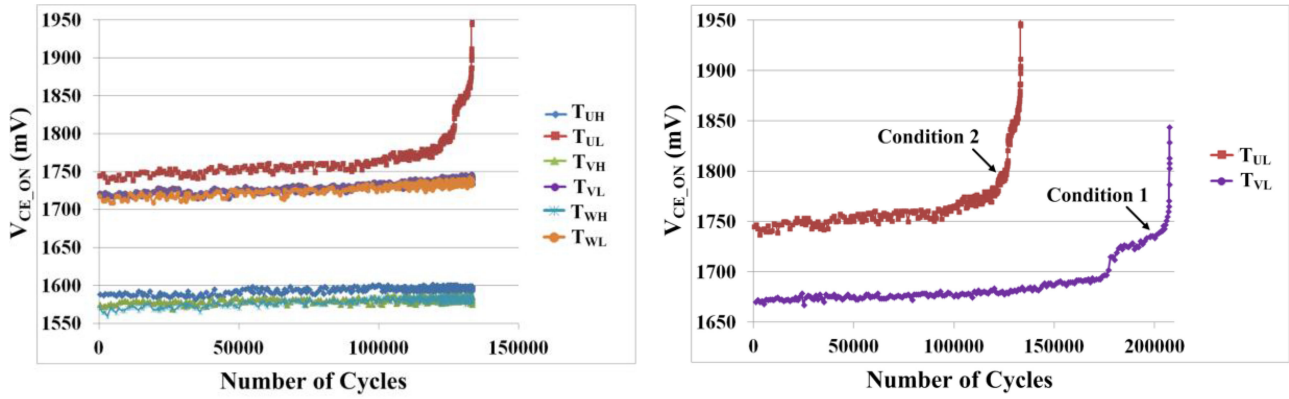

Fig. 28. Result of the advanced accelerated power cycling test: (a) under the operating Condition 2 and (b) comparison of the number of cycles to failure between Condition 1 and Condition 2.

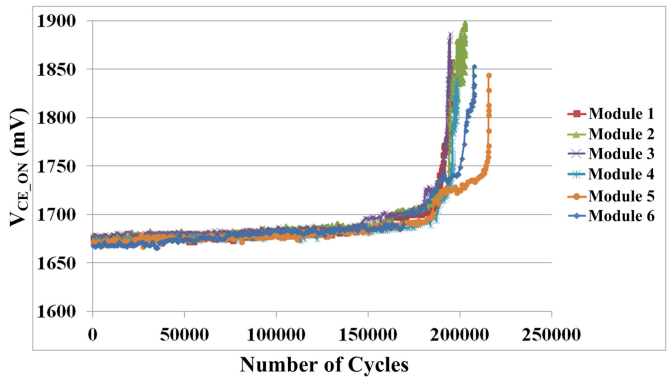

Fig. 29. Power cycling test results of six modules under Condition 1.

TABLE III
NUMBER OF CYCLES TO FAILURE FOR SIX TEST MODULES UNDER CONDITION 1

Condition	Number of cycles to failure
Module 1	190 700
Module 2	194 200
Module 3	191 000
Module 4	195 650
Module 5	207 425
Module 6	201 200

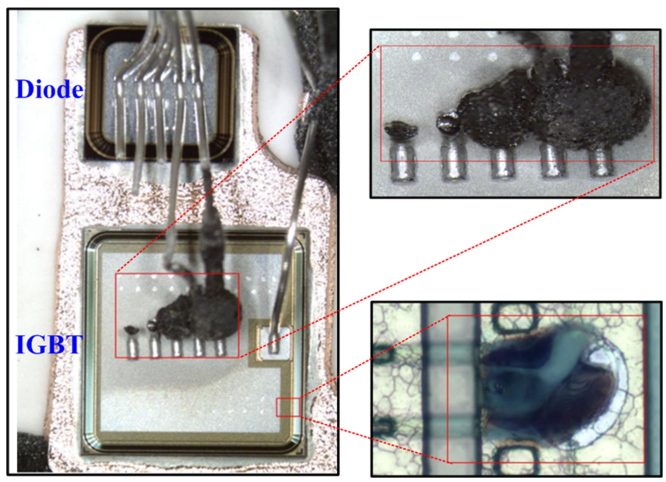

Fig. 30. Failure analysis of the tested module corresponding to Fig. 23 under the operating Condition 1 given in Table II.

power losses could be changed and it leads to higher thermal stresses. The test strategies with constant temperature swing and constant power losses compensate degradation effects and deliver three times longer lifetime than the power cycling test strategy without compensations. Finally, it concludes that the test strategies with constant temperature swing and constant power losses are not suitable for the power cycling test from a real application point of view. Therefore, in this test methodology, the electric test conditions such as current, DC-link voltage, switching frequency, modulation index and gate voltage are kept without any compensations for degradation of the tested module during power cycling tests. Further, test conditions should be in the safe-operating area (SOA) of the test device to prevent the other failure mechanisms that could come from the operation outside of SOA.

The power cycling test has been performed under the operating Condition 1 as listed in Table II. Fig. 22 shows the temperature profile under Condition1 where $T_{j\mathrm{mean}} = (T_{j\max} + T_{j\min})/2$. The power cycling test conditions are chosen based on the temperature of T_{VL}.

Fig. 23 shows the measured $V_{\mathrm{CE_ON}}$ and V_F of the IGBTs and diodes in phase-V during the power cycling test. As expected, the failure occurs in low-side IGBT first. Fig. 24 shows $V_{\mathrm{CE_ON}}$ of the low-side IGBT of phase-V in detail. It seems that the first failure occurs in the bond-wire at about 168 K cycles, because there is a sudden increase of $V_{\mathrm{CE_ON}}$. After 197 K cycles, $V_{\mathrm{CE_ON}}$ increases by 10% from its initial value and a catastrophic failure occurs after 201 K cycles.

Fig. 25 showsr the power cycling results of another module under the same operating condition. $V_{\mathrm{CE_ON}}$ is measured at 20 $\mathrm{A_{peak}}$ for all power devices. If $V_{\mathrm{CE_ON}}$ increases more than 10–15% of its initial value, the test is stopped to protect the tested module against catastrophic failure. The failure occurs in T_{VL} first. After 176 k cycles, there is a sudden increase in $V_{\mathrm{CE_ON}}$

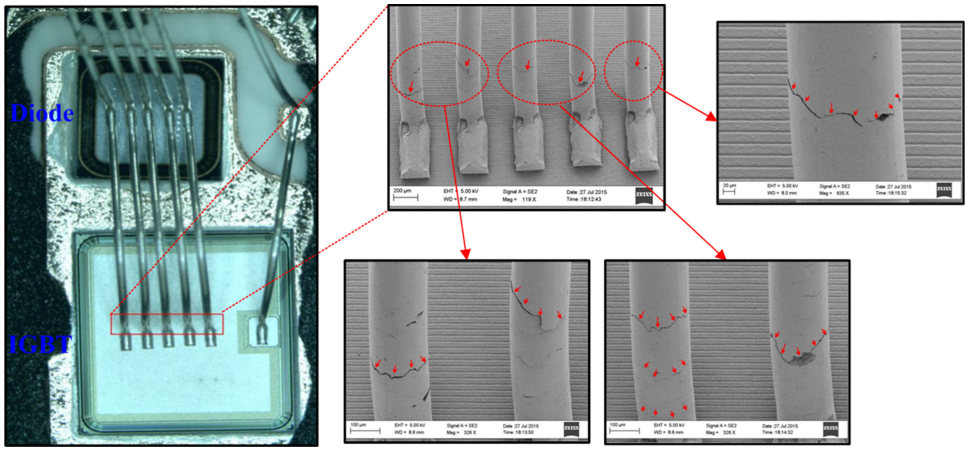

Fig. 31. Failure analysis of the tested module corresponding to Fig. 25 under the operating Condition 1 in Table II where the power cycling test has been stopped before catastrophic failure occurs (cracked bond-wires—Red arrow).

of T_{VL} and then it is increased by 10% after 216 k cycles. This test takes about 60 h until it is finished. Even though the test is stopped after the $V_{\mathrm{CE_ON}}$ of T_{VL} increases to above the set point, it can be expected that the T_{UL} will fail next, because there is a sudden increase in $V_{\mathrm{CE_ON}}$ just before the test is finished. This result also reflects well the previous analysis that the low-side IGBTs have a higher thermal stress compared to the high-side IGBTs due to different thermal impedance caused by asymmetric layout.

Fig. 26 shows the power cycling test result with online junction temperature monitoring under Condition 1 where red arrow indicates the recharacterization points. In this test, $V_{\mathrm{CE_ON}}$ is measured at 29 A and the junction temperature is estimated at this point. The *I–V* characterization is performed at initial stage and the estimated temperature is about 118 °C. If the estimated junction temperature T_j increases by a certain level due to $V_{\mathrm{CE_ON}}$ increase, the *I–V* characterization needs to be performed again to eliminate the effect of electrical degradation on T_j estimation and to determine $V_{\mathrm{CE_ON}}$ increase either due to bond-wire fatigue or due to solder joint fatigue. This point can be set properly within end-of-life criteria, for example, 20% increases of thermal impedance, and can be checked in real time. As $V_{\mathrm{CE_ON}}$ increases during the test, the estimated T_j also increases as shown in Fig. 26. At 150 000 and 163 883 cycles where $V_{\mathrm{CE_ON}}$ increases by about 25 and 40 mV, respectively, the *I–V* recharacterization is performed and the estimated T_j decreases by its initial value. The *I–V* characterization is performed two times again at 199 422 and 205 238 cycles, separately until $V_{\mathrm{CE_ON}}$ increases by 5% and the estimated T_j decreases after recharacterization. It means that there is no thermal resistance increases during the test. Therefore, it can be expected that the main cause of $V_{\mathrm{CE_ON}}$ increases is not due to the solder joint fatigue but due to the bond-wire fatigue in this test condition. Fig. 27 shows the change of parameters for the junction temperature estimation during the power cycling test.

The power cycling test has been performed under Condition 2 as given in Table II to investigate the effect of ΔT_j duration on lifetime of the IGBT module. In this condition, the temperature stresses ΔT_j and $T_{j\mathrm{mean}}$ are almost the same with Condition 1, but f_{OUT} is changed from 1 to 0.1 Hz. This test is continued for about 370 h. In this case, T_{UL} fails first as shown in Fig. 28(a). After 133 K cycles, $V_{\mathrm{CE_ON}}$ of T_{UL} increases by more than 10% from its initial value and the power cycling test is stopped. As shown in Fig. 28(b), there is a significant difference in the number of cycles to failure between Condition 1 and Condition 2. This result shows that the cycle period is also one of the important factors to affect the lifetime and it should be considered when the power cycling test is performed and a lifetime model is developed from the test results [32].

Furthermore, in the lifetime modeling, the statistical data analysis is an essential in order to deal with uncertainty because the reliability, typically represented by probability of survival and failure rate, is influenced by variability such as variations in manufacturing process, environments and any other varying factors. Therefore, the power cycling test should be performed with a number of samples per test condition in order to get statistic results.

Fig. 29 shows the six power cycling test results under the test Condition 1 and the number of cycles to failure when 5% of $V_{\mathrm{CE_ON}}$ increase is considered as the end-of-life is represented in >Table III. It can be seen that each sample has the different number of cycle to failure even though they are tested under the same operating condition. Therefore, the statistical data analysis should be considered when the lifetime model is developed. The Weibull analysis is one of popular methods in reliability engineering for analyzing life data [35]. Further, when the lifetime model is developed with statistical data analysis, the end-of-life criteria, specific lifetime definition of a lifetime model and confidence level of a specific lifetime model should be provided because parameters of the lifetime model are varied according to different definitions.

C. *Physics-of-Failure Analysis of the Tested Modules*

The tested modules are decapsulated by heated fuming nitric acid to investigateo inside of the module since the target module

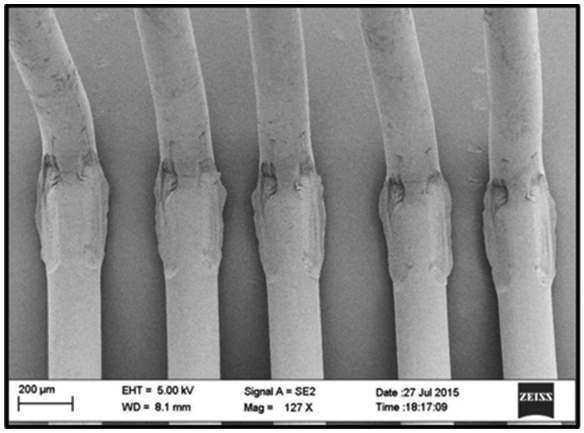

Fig. 32. SEM image of the diode D_{VL} of tested module under the operating Condition 1 in Table II.

is covered by EMC. The physical analysis has been done by optical/scanning electron microscope (SEM) inspection.

Fig. 30 shows the analysis result of the tested module shown in Fig. 23. Abnormal high current flows at the end of the test due to the catastrophic failure and thus metal, silicon and emitter bond-wires of low side IGBT of phase-V (T_{VL}) are fused. Under this condition, it is impossible to investigate the failure mechanism correctly and therefore it is important to stop the power cycling test before a catastrophic failure occurs which is possible by the online V_{CE} measurement.

The physics-of-failure analysis of the second tested module under the same operating condition has been performed. In this case, the power cycling test is stopped when $V_{\mathrm{CE_ON}}$ increases by 10–15% from its initial value as shown in Fig. 25. Fig. 31 shows the analysis results. The bond-wire cracks are observed in all five bond wires of T_{VL}. This is the reason that $V_{\mathrm{CE_ON}}$ increases as shown in the power cycling test results.

There is no visible degradation in the diode D_{VL} as shown in Fig. 32. These results agree well with power cycling test results that $V_{\mathrm{CE_ON}}$ of T_{VL} increases due to degradation. Under the test Condition 2, the bond-wire cracks are also observed in T_{UL}.

Fig. 33(a), (b) and (c) shows the SEM images of the cross-sectioned IGBT module before and after the power cycling tests under Conditions 1 and 2, respectively. After the power cycling test under the Condition 1, there are no visible degradation in chip solder joint in comparison with new one and no bond-wire lift-off as shown in Fig. 33(b). In the case of the tested module under the Condition 2, there are also no degradation in chip solder joint compared with new one and no fracture in the interface between chip and bond-wire as shown in Fig. 33(c). It is worth to note that the black spots in the solder and bond-wire shown in Fig. 33 are not the degradation due to power cycling test but remained material from the IGBT module.

It can be seen from the physics-of-failure analysis results that the bond-wire degradation is the predominant failure mechanism of this module. However, the power cycling tests under more various temperature stress conditions with a number of samples per condition are still needed in order to investigate the effect of temperature stress conditions on the failure mechanisms with statistic results.

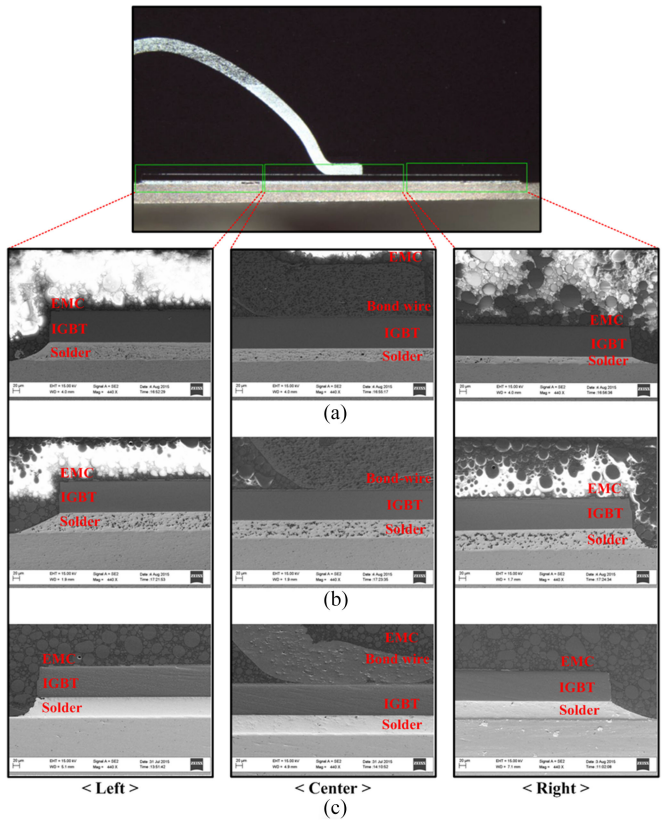

Fig. 33. SEM images of cross-sectioned IGBT for failure analysis: (a) before and (b) after the power cycling test under Condition 1 and (c) after the power cycling test under Condition 2.

V. Conclusion

This paper has presented a methodology and apparatus for an advanced accelerated power cycling test of power device modules. The detailed explanations of configuration, features, and control methods for different functions of advanced accelerated power cycling test setup have been presented. An online $V_{\mathrm{CE_ON}}$ measurement concept also has been discussed. By applying the online $V_{\mathrm{CE_ON}}$ measurement circuit, the degradation of the tested power module can be monitored in real time which gives a convenience to perform the test.

An improved junction temperature estimation method has been proposed using $V_{\mathrm{CE_ON}}$ and load current. *I–V* characterization curves for the tested devices are obtained by the proposed simple switching sequence with online $V_{\mathrm{CE_ON}}$ measurement. By means of the proposed method, the estimation error which comes from the different temperatures of the interconnection materials in the module is compensated and it leads to satisfactory estimated results. Further, it can be used for power cycling test to determine the failure mechanism between bond-wire and solder joint fatigues.

In addition, accelerated power cycling tests with 600 V, 30 A intelligent power IGBT modules have been performed under two different test conditions in order to verify the validity and effectiveness of the proposed power cycling test concept. By the proposed concept of applying temperature stress, it is possible to generate various magnitudes of the temperature swing in a short

cycle period. Owing to this, the tests have been finished in 3 and 16 days, respectively. Further, the dominant failure mechanism between bond-wire and solder joint is identified by monitoring the junction temperature during the test. It can also be seen from the six test results under the same test condition that the statistical data analysis is essential in the lifetime modeling of IGBT module. The effect of ΔT_j duration on lifetime of the IGBT module has also been investigated and the results show that it has the significant effect on the lifetime of the IGBT module.

Finally, the physics-of-failure analysis has been performed to investigate the failure mechanism of the tested device modules. The bond-wire cracks are observed in all tested modules and there are no visible degradation in the chip solder joint. Therefore, the bond-wire is the predominant failure mechanism in the tested modules under these conditions. However, the power cycling tests under more various temperature stress conditions with a number of samples per condition are still needed in order to investigate the effect of temperature stress conditions on the failure mechanisms and to develop a lifetime model with statistic results.

The proposed accelerated power cycling test concept is expected to be useful for developing lifetime models as well as investigating the reliability performance of power device modules under more realistic electrical operating conditions.

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