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# Analysis and Design of the Quasi-Z-Source Inverter for Wide Range of Operation

Ahmed Abdelhakim[1], Pooya Davari[2], Frede Blaabjerg[2], and Paolo Mattavelli[1]
[1]Dept. of Management and Engineering, University of Padova, Vicenza, Italy
[2]Dept. of Energy Technology, Aalborg University, Aalborg, Denmark
Email: ahmed.a.abdelrazek@ieee.org, pda@et.aau.dk, fbl@et.aau.dk, paolo.mattavelli@unipd.it

***Abstract*—Impedance source inverters are experiencing a solid evolution since the first release of the traditional Z-source inverter (ZSI) in 2003, and among the abundant structures, quasi-ZSI (qZSI) is commonly studied for many applications due to its simple structure and having a continuous input current. Despite such attractive performance of the qZSI in various applications, it suffers from an inferior performance during partial-load operation, resulting in a limited range of operation. Hence, this paper introduces a conceptual study of the qZSI partial-load operation, demonstrating two important aspects in order to maintain the highest possible performance within the desired operating range. Firstly, a design aspect concerning the proper sizing of the impedance network inductance using linear and non-linear chokes is introduced. Secondly, a control aspect is proposed based on utilizing higher effective switching frequency through switching among different modulation schemes. Finally, a *3 kVA* qZSI prototype is utilized in order to experimentally validate the reported analysis and discussions.**

***Index Terms*—Continuous conduction mode (CCM), discontinuous conduction mode (DCM), impedance source inverter, partial-load, quasi-Z-source inverter (qZSI), shoot-through, space vector modulation, Z-source inverter (ZSI).**

## I. Introduction

Impedance source inverters with buck and boost capabilities in a single-stage operation are interesting and relevant alternatives to the traditional two-stage architecture, in which a boost converter-fed voltage source inverter (VSI), which is shown in Fig. 1, is commonly used [1]–[4]. This family of power converters, i.e. the impedance source inverters, is experiencing a fast evolution since the first release of the Z-source inverter (ZSI) in 2003, where many different structures have been developed since then [1], [5], [6]. Despite this evolution, all of these different structures, except for the split-source inverter (SSI) [4], [7], are utilizing the same basic principle of operation, which is inherited from the original ZSI [1]. Such principle of operation implies the use of an additional switching state, called shoot-through (ST) state, under which the inverter bridge acts as a short circuit, and this is permissible due to the utilization of an impedance network between the dc source ($V_{in}$) and the inverter bridge [1], [8].

Among the abundant structures of the impedance source inverters, the three-phase quasi-ZSI (qZSI), which is shown in Fig. 2, is commonly used due to its simple structure and continuous input current [9]–[11]. This qZSI has been studied

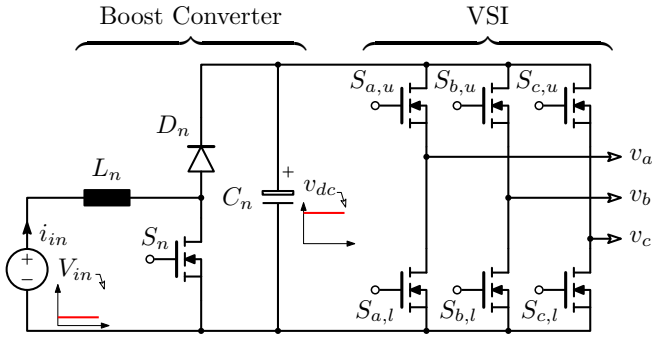


Fig. 1. Traditional two-stage dc-ac architecture using a boost converter-fed three-phase voltage source inverter (VSI).

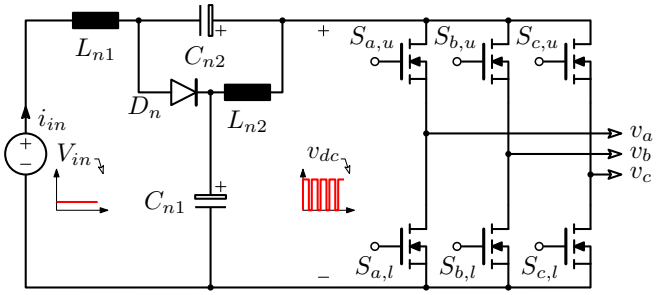


Fig. 2. Three-phase quasi-Z-source inverter (qZSI).

for many applications, such as photovoltaic (PV) systems [12], [13], energy storage [14], and electric vehicles [15].

Despite this attractive exploitation of the qZSI in many applications, it suffers from an inferior performance at partial-load operation, which is mandatory for many applications. This inferior performance arises from the variation of the dc-link voltage ($v_{dc}$) between three voltage levels, unlike the normal operation, under which $v_{dc}$ pulsates between two voltage levels only. Those two voltage levels are as follows: the zero-voltage level, i.e. $v_{dc} = 0$, which occurs during the ST state, while the other one is the peak-voltage level, i.e. $v_{dc} = \hat{v}_{dc}$, being $\hat{v}_{dc}$ is the peak value of $v_{dc}$, which occurs during the non-ST states. On the other hand, under partial-load condition and during the non-ST states, $v_{dc}$ varies between two different voltage levels. Note that this operation is similar to the discontinuous conduction mode (DCM).

In the literature, the different modes of operation of the ZSI and the qZSI have been investigated in [16]–[18]. The authors in [16] have investigated the different modes of operations that the ZSI might go through under a small impedance network inductance or a low power factor. Moreover, the critical value of the impedance network inductance in order to avoid the unwanted abnormal modes of operation is mentioned in [16] for the ZSI. On the other hand, the qZSI abnormal modes of operation have been discussed in [17], [18], in which the critical value of the impedance network inductance is introduced in order to ensure a proper operation.

Although the prior studies, the only introduced solution in order to eliminate these unwanted modes of operation and ensure a proper operation of the converter is the replacement of the impedance network diode with an active switch. Furthermore, the wide range of operation, which is mandatory for many applications, has never been discussed before for these family of power converters. Accordingly, this paper starts first by introducing a conceptual study of the qZSI partial-load operation, demonstrating the proper sizing of the impedance network inductance using linear and non-linear chokes, which has some merits compared to the linear one, in order to maintain the highest possible performance within the desired operating range. Moreover, this paper discusses the possibility of switching among the different modulation schemes at partial-load in order to obtain a higher effective switching frequency for the impedance network, and utilize the smallest possible impedance network inductance with wider range of operation as a consequence.

The rest of this paper is organized as follows: Section II reviews the operation and modulation of the three-phase qZSI. Then, the partial-load operation of the qZSI and the proper sizing of its impedance network inductance for a desired range of operation are studied in Section III. Furthermore, this section discusses the effect of switching among the different modulation schemes for the qZSI in order to achieve a wide range of operation with minimal inductance requirements. In order to verify the reported analysis and modulation scheme, the experimental results using a *3 kVA* three-phase qZSI are presented in Section IV. Finally, conclusions are reported in Section V.

## II. Review of the qZSI Operation and Modulation

The traditional three-phase VSI shown in Fig. 1 utilizes eight different switching states in order to modulate the B6-bridge and to achieve the inversion operation. These eight states comprises six active states and two zero states. In addition to these different eight switching states, the three-phase qZSI shown in Fig. 2 can utilize an additional switching state, which is not permissible in the traditional VSIs, in order to embrace the boosting capability within the inversion operation. This additional switching state, which is called ST state, is permissible in the impedance source inverters due to the utilization of an impedance network between the dc source and the B6-bridge as depicted in Fig. 2 for the qZSI.

During the ST state, the inverter bridge is equivalent to a short-circuit and the dc-link voltage ($v_{dc}$) is equal to zero as shown in Fig. 3. This can be achieved by simultaneously turning ON each pair of switches in one, two, or three-phase legs, which corresponds to seven different possible combinations. On the other hand, during the non-ST states, i.e. the conventional active and zero states, the inverter bridge acts as a current source and $v_{dc}$ is equal to a constant value, i.e. $v_{dc} = \hat{v}_{dc}$, as depicted in Fig. 3 assuming negligible capacitor voltage ripple. Note that the impedance network inductors ($L_{n1}$ and $L_{n2}$) are charged during the ST state, while the impedance network capacitors ($C_{n1}$ and $C_{n2}$) are charged during the non-ST states.

In order to fulfill such operation, many modulation schemes can be utilized, where these different schemes have been reviewed and compared in [19], [20]. According to [9], [20], the simple-boost modified space vector (SBMSV) modulation scheme, whose reference signals are depicted in Fig. 4, achieves high performance. Under this modulation scheme, the three-phase qZSI shown in Fig. 2 is modulated as follows: for phase $a$, $S_{a,u}$ is turned ON when $v_a^*$ is larger than the carrier signal or larger than $v_b^*$ and $v_c^*$, while $S_{a,l}$ is turned ON when $v_a^*$ is smaller than the carrier signal. Similarly, phase-legs $b$ and $c$ can be modulated in the same way.

Then, according to [9], the value of the impedance network inductors, using the SBMSV modulation scheme, can be calculated by

$$L_{n1} = L_{n2} = L_n \geq \frac{M \cdot (1-M) \cdot V_{in}}{(2M-1) \cdot f_s \cdot \Delta I_L}, \tag{1}$$

where $M$ is the modulation index defined in Fig. 4, $V_{in}$ is the input dc voltage, $f_s$ is the switching frequency, and $\Delta I_L$ is the peak-to-peak inductor current ripple. Hence, assuming that the input power is equal to the output power, $L_n$ can be calculated for the rated output power ($P_o$) from

$$L_n \geq \frac{M \cdot (1-M) \cdot P_o}{(2M-1) \cdot f_s \cdot \Delta I_L \cdot I_{in}}, \tag{2}$$

where $I_{in}$ is the average input current. Thus, considering a certain desired peak-to-peak inductor current ripple ($\Delta I_L$) at full-load, the required impedance network inductance ($L_n$) can be calculated from (2).

## III. Partial-Load Operation of the qZSI

### A. Conceptual Study of the qZSI Partial-Load Operation

The qZSI can have several modes of operations like the ZSI, where the authors in [16] have mentioned that some of these unwanted operating modes occur at low power factor or when a small impedance network inductance is utilized. Meanwhile, if the impedance network inductance is properly selected, these unwanted modes of operation can be avoided as discussed in [17], [18].

The qZSI normal operation implies that the dc-link voltage ($v_{dc}$) pulsates between two voltage levels, where the first one is the zero voltage level, which occurs during the ST state, while the other one is the peak voltage level, which occurs

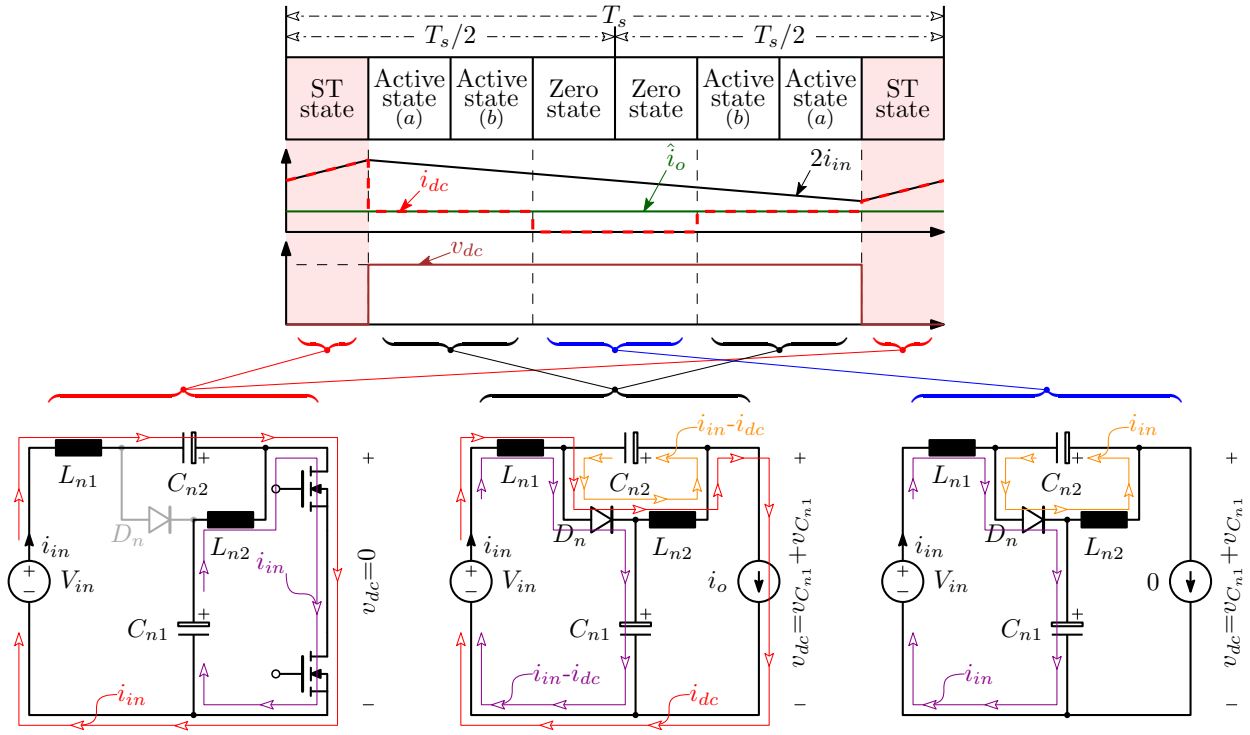


Fig. 3. Equivalent circuits of the three-phase qZSI during the different switching states under its normal operation, showing the dc-link voltage ($v_{dc}$) and current ($i_{dc}$) during one switching state, where $T_s$ is the switching time. Note that $i_{in}$ is the input current, which is equal to the sum of the inductor currents, $v_{C_{n1}}$ and $v_{C_{n2}}$ are the voltages across $C_{n1}$ and $C_{n2}$ respectively, and $\hat{i}_o$ is the peak value of the output phase current ($i_o$). The shown switching pattern is for the simple-boost modified space vector (SBMSV) modulation scheme, which is proposed in [9].

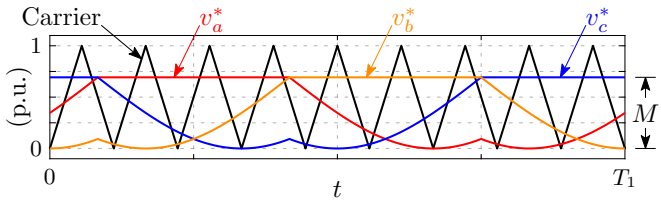


Fig. 4. Reference and carrier signals of the simple-boost modified space vector (SBMSV) modulation scheme for one fundamental cycle, where $T_1$ is the fundamental period and $M$ is the modulation index [9]. Note that the modulation-to-fundamental frequency ratio ($M_f$) is set to be 9, which is low and it is for illustrative purposes.

during the non-ST states as shown in Fig 3. Meanwhile, under partial-load condition, the peak voltage level is divided into two regions with different voltage levels as shown in Fig 5, which results in an inferior operation in terms of increasing the voltage stresses across the switches and also increasing the distortion in the output ac voltage.

Such partial-load operation can be clarified as follows: as long as the impedance network diode ($D_n$) is ON, which must occur during the non-ST states, the dc-link voltage ($v_{dc}$) is equal to the sum of $v_{C_{n1}}$ and $v_{C_{n2}}$, i.e. ($v_{dc} = v_{C_{n1}} + v_{C_{n2}}$), which is similar to the normal operation. Meanwhile, if $D_n$ is OFF during the non-ST states, $v_{dc}$ is equal to $v_{C_{n1}}$ which is equal to ($V_{in} + v_{C_{n2}}$), assuming negligible current ripple is $L_{n1}$ and $L_{n2}$. The later scenario or mode of operation occurs when the peak value of the output phase current ($\hat{i}_o$) is equal to ($2 \cdot i_{in}$), being $i_{in}$ is the input current which is equal to the current through $L_{n1}$ and $L_{n2}$. Then, ($2 \cdot i_{in}$) remains equal to $\hat{i}_o$ as shown in Fig 5. Note that a negligible load current ripple is assumed, which results in negligible voltages across $L_{n1}$ and $L_{n2}$ when $D_n$ is OFF during the non-ST states. Hence, if the load current ripple is not negligible, $v_{dc}$ is equal to ($v_{C_{n1}} + v_{L_{n1}}$), which is also equal to ($V_{in} + v_{C_{n2}} + v_{L_{n2}}$).

### B. Classical Approaches for Wide Range of Operation

*1) Active Approach:* A conventional approach that is usually used in order to avoid any of the qZSI unwanted modes of operation is the replacement of the impedance network diode ($D_n$) with an active switch ($S_n$), where this switch is turned ON during the non-ST states [16], [21]. Thus, the dc-link voltage ($v_{dc}$) is forced to be equal to the sum of $v_{C_{n1}}$ and $v_{C_{n2}}$ during the entire non-ST period as shown in Fig. 6. It is worth to note that such utilization of a controlled switch allows a bidirectional power flow capability. Meanwhile, two demerits arise as a consequence: the first demerit is the generation of an additional control signal, while the second one is the mandatory need of generating a dead-time between the gate signal of $S_n$ and the ST-state as shown in Fig. 6 in order to avoid any short circuit across the impedance network capacitors.

*2) Passive Approach:* On the other hand, considering a minimum output power level ($P_{o,min}$), $L_n$ must be estimated

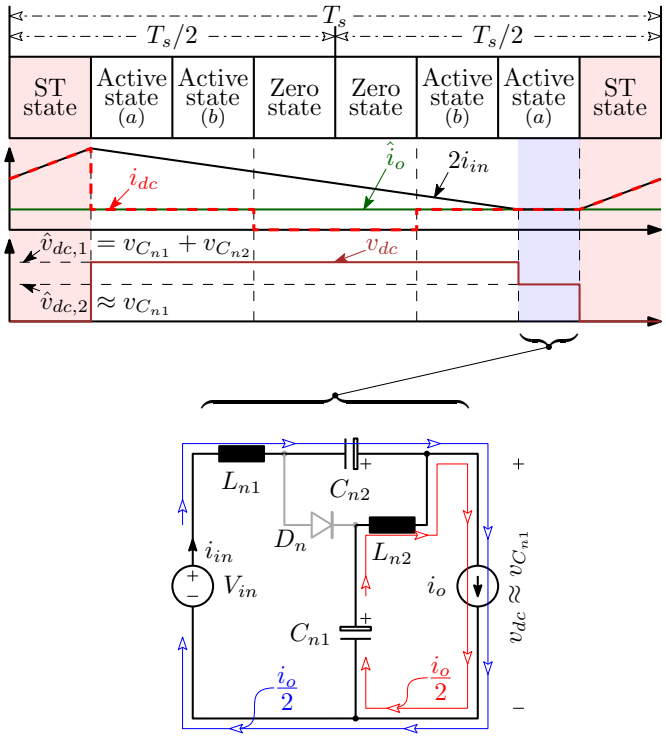


Fig. 5. Equivalent circuit of the three-phase qZSI when $\hat{i}_o$ is equal to $(2 \cdot i_{in})$, where this scenario occurs during partial-load operation.

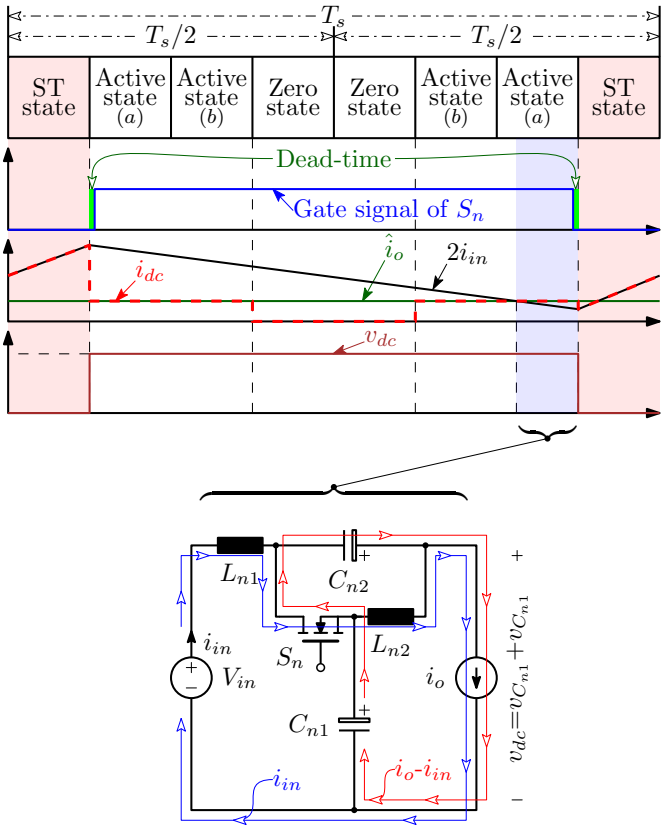


Fig. 6. Equivalent circuit of the three-phase qZSI when $\hat{i}_o$ is larger than $(2 \cdot i_{in})$ under partial-load condition using an active switch $(S_n)$ instead of the impedance network diode $(D_n)$. Note that $S_n$ is turned ON during the non-ST states and turned OFF during the ST state in order to avoid short circuiting the impedance network capacitors.

from

$$L_n \geq \frac{M \cdot (1-M) \cdot V_{in}}{(4M-2) \cdot f_s \cdot P_{o,min} \cdot (\frac{1}{V_{in}} - \frac{1}{3\sqrt{2}V_\varphi \cdot cos(\varphi)})}, \quad (3)$$

where $V_\varphi$ is the fundamental output RMS phase voltage and $cos(\varphi)$ is the load power factor.

An interesting and relevant passive solution that can be used in order to extend the operating range of the qZSI is the utilization of a non-linear choke, such as Magnetics Inc Kool M$\mu$ [22]. As it is well known, this non-linear choke is characterized by its variable inductance versus the dc bias variation as shown in Fig. 7 for the Kool M$\mu$ 77109A7 toroid core with 75 turns. Fig. 7 shows that for lower dc bias levels, the non-linear choke has a high inductance, while the choke inductance is lower at higher dc bias levels. Hence, it is possible to design a non-linear choke in order to have a certain value of the inductance at the desired partial-load power.

In order to design the non-linear choke for an intended operating range, the required inductance value at full load is calculated using (2), while the desired one at partial-load is calculated using (3). Then, the non-linear choke must ensure that the inductance is higher than the prior calculated values at full and partial-loads. Finally, it is worth to note that the efficiency of a non-linear choke is higher than the efficiency of a linear choke of the same inductance value [23].

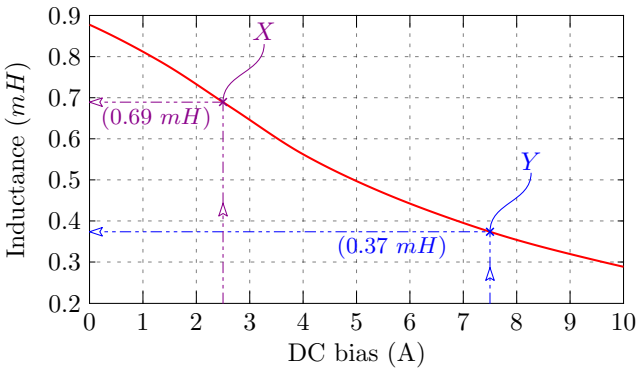


Fig. 7. Estimated inductance variation of a Kool M$\mu$ 77083A7 toroid core from Magnetics Inc with 75 turns. Note that $Y$ represents the desired linear choke value at full load conditions, while $X$ represents the desired linear choke value in order to ensure an intended operating range for the *3 kVA* system, whose parameters are listed in Table I.

### C. Modulation-Based Approach for Wide Range of Operation

One of the simple approaches that can be used in order to extend the qZSI operation is to increase the effective switching frequency of the impedance network ($f_{n,eff}$) at light load condition in order to minimize the inductors peak-to-peak current ripples. Thus, the peak value of the output phase

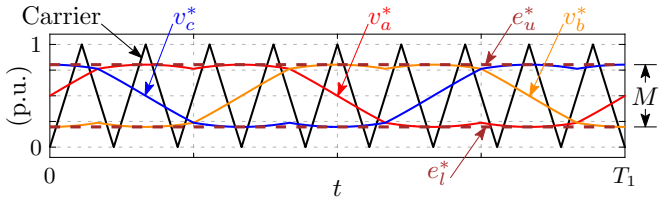


Fig. 8. Reference and carrier signals of the simple-boost space vector (SBSV) modulation scheme for one fundamental cycle [9]. Note that $e_u^*$ and $e_l^*$ are used in order to generate the ST state by comparing them with the carrier signal.

TABLE I
PARAMETERS OF THE 3 $kVA$ THREE-PHASE QZSI PROTOTYPE

| | | | | | |
|---|---|---|---|---|---|
| $V_{in}$ | 400 $V$ | $V_{\varphi}$ | 220 $V$ | $M$ | 0.7951 |
| $f_s$ | 60 $kHz$ | $L_{n1,2}$ | 0.37 $mH$ | $C_{n1,2}$ | 20 $\mu F$ |
| $f_1$ | 50 $Hz$ | $L_{f,abc}$ | 1.0 $mH$ | $C_{f,abc}$ | 4.7 $\mu F$ |

current ($\hat{i}_o$) stays smaller than twice the minimum value of the inductor current.

Such increase in $f_{n,eff}$ can be achieved using two approaches. The first approach, which is a straight forward one, is to increase the carrier frequency itself. Meanwhile, the second approach keeps the same carrier frequency but changes the used modulation scheme to another one, where $f_{n,eff}$ is much higher.

An example for the second approach is changing the used SBMSV modulation scheme, whose reference signals are as shown in Fig. 4 and $f_{n,eff} = f_s$, to the simple-boost space vector (SBSV) modulation scheme, whose reference signals are shown in Fig. 8 and $f_{n,eff} = 2f_s$ [9].

It is worth to note that the authors in [19], [20] have introduced a comprehensive review of the different modulation schemes used for the three-phase impedance source inverters. This comprehensive review includes a detailed comparison among these schemes demonstrating the effective switching frequency of the impedance network under each modulation scheme.

## IV. EXPERIMENTAL RESULTS

In order to verify the prior analysis and discussions, a 3 $kVA$ three-phase qZSI prototype, whose parameters are listed in Table I, is utilized. Note that Table I shows the desired impedance network inductance at full load, which is designed using (1) in order to have a peak-to-peak current ripple ($\Delta I_L$) of $0.7I_{in}$ at full load, i.e. $\Delta I_L = 5.25$ $A$.

This three-phase qZSI is desired to be operated at a partial-load of 1 $kW$ as minimum power level with a unity power factor. Thus, according to (3), the desired inductance must be increased to be 0.65 $mH$. Hence, it is not recommended to use the prior designed impedance network inductance value, i.e. 0.37 $mH$, at 1 $kW$ as it results in an inferior performance as shown in Fig. 9. Fig. 9(a) shows the dc-link voltage ($v_{dc}$), the voltage across $C_{n1}$ ($v_{C_{n1}}$), and the current through $L_{n1}$ ($i_{in}$) at full load, while the same results are shown again in Fig. 9(b) at partial-load, where the output power is equal

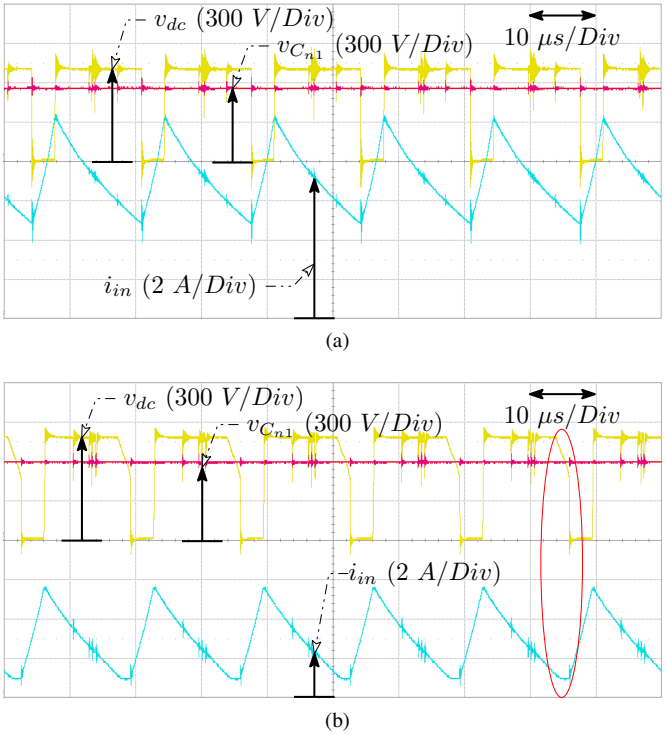


Fig. 9. Experimental results of the 3 $kVA$ qZSI at the maximum and minimum desired output power levels using the SBMSV modulation scheme shown in Fig. 4, where the used parameters are listed in Table. I. (a) Full load operation and the output power is equal to 3 $kW$; and (b) partial-load operation and the output power is equal to 1 $kW$, i.e. 30% of the rated power. Note that in both results the dc-link voltage ($v_{dc}$), the voltage across $C_{n1}$ ($v_{C_{n1}}$), and the current through $L_{n1}$ ($i_{in}$) are shown.

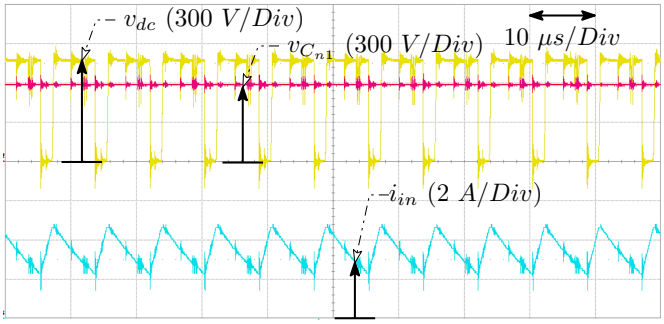


Fig. 10. Partial load results of the 3 $kVA$ qZSI using an increased effective switching frequency of the impedance network under the SBSV modulation scheme shown in Fig. 8. In this result, the dc-link voltage ($v_{dc}$), the voltage across $C_{n1}$ ($v_{C_{n1}}$), and the current through $L_{n1}$ ($i_{in}$) are shown. Note that the output power is equal to 1 $kW$, i.e. 30% of the rated power, and the effective switching frequency is equal to 120 $kHz$.

to 1 $kW$. Comparing Fig. 9(a) and Fig. 9(b) confirms the prior discussion about the inferior performance of the qZSI under partial-load condition. Note that the prior shown results in Fig. 9 are based on the SBMSV modulation scheme shown in Fig. 4.

In order to overcome such poor performance, the prior mentioned approaches can be utilized. Fig. 10 shows the same prior partial-load results using an increased effective switching

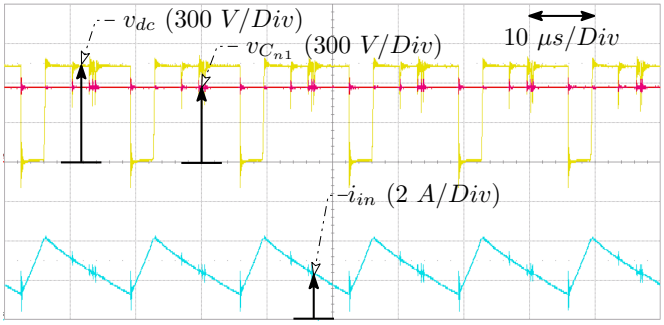


Fig. 11. Partial load results of the 3 $kVA$ qZSI using a non-linear choke. In this result, the dc-link voltage ($v_{dc}$), the voltage across $C_{n1}$ ($v_{C_{n1}}$), and the current through $L_{n1}$ ($i_{in}$) are shown. Note that the output power is equal to 1 $kW$ and the used non-linear choke is a Kool M$\mu$ 77109A7 toroid core from Magnetics Inc with 75 turns, where Fig. 7 shows its inductance variation versus the dc bias.

frequency of the impedance network ($f_{n,eff}$) under the SBSV modulation scheme shown in Fig. 8, where $f_{n,eff} = 120\,kHz$. Meanwhile, Fig. 11 considers the non-linear choke solution, where a Kool M$\mu$ 77109A7 toroid core from Magnetics Inc with 75 turns. Note that this core has been selected and designed with this number of turns in order to ensure a proper operation for the qZSI within the desired range, i.e. 1 to 3 $kW$, where the minimum and the maximum operating points are highlighted in Fig 7.

These results confirm the introduced analysis in this paper and verify the importance of the proposed solutions in order to improve the performance of the qZSI for a wide range of operation.

## V. Conclusion

The quasi-Z-source inverter partial-load operation has been investigated in this paper, where its normal and abnormal operations have been discussed. Moreover, the sizing of the impedance network inductors has been introduced in order to ensure a proper operation within the desired operating range. In addition, different active and passive solutions have been discussed for the sake of extending the operating range without increasing the inductance requirements.

Finally, experimental results using a 3 $kVA$ three-phase qZSI have been introduced in order to verify the introduced analysis, discussions, and solutions, where these solutions have demonstrated effective enhancement in the qZSI performance at partial-load.

## Acknowledgement

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