Aalborg Universitet

A ZVS PWM control strategy with balanced capacitor current for half-bridge three-level DC/DC converter

Liu, Dong; Deng, Fujin; Chen, Zhe

Published in:
Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)

DOI (link to publication from Publisher):
10.1109/APEC.2017.7930710

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Liu, D., Deng, F., & Chen, Z. (2017). A ZVS PWM control strategy with balanced capacitor current for half-bridge three-level DC/DC converter. In *Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)* (pp. 307-314). Article 7930710 IEEE Press. https://doi.org/10.1109/APEC.2017.7930710

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

Take down policy
If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

A ZVS PWM Control Strategy with Balanced Capacitor Current for Half-Bridge Three-Level DC/DC Converter

Dong Liu, Fujin Deng, Zhe Chen
Department of Energy Technology
Aalborg University
Aalborg, Denmark
dli@et.aau.dk, fde@et.aau.dk, zch@et.aau.dk

***Abstract*— The capacitor current would be imbalanced under the conventional control strategy in the half-bridge three-level (HBTL) DC/DC converter due to the effect of the output inductance of the power supply and the input line inductance, which would affect the converter's reliability. This paper proposes a pulse-wide modulation (PWM) strategy composed of two operation modes for the HBTL DC/DC converter, which can realize the zero-voltage switching (ZVS) for the efficiency improvement. In addition, a capacitor current balancing control is proposed by alternating the two operation modes of the proposed ZVS PWM strategy, which can eliminate the current imbalance among the two input capacitors. Therefore, the proposed control strategy can improve the converter's performance and reliability in: 1) reducing the switching losses and noises of the power switches; 2) balancing the thermal stresses and lifetimes among the two input capacitors. Finally, the simulation and experimental results are presented to verify the proposed control strategy.**

Keywords—Capacitor current balance; DC/DC three-level converter; zero-voltage-switching (ZVS).

I. INTRODUCTION

More and more researches focus on the high voltage DC/DC converter with high performance and high reliability. The three-level (TL) DC/DC converter is one of most attractive choices for the DC distribution systems with the high DC bus voltage [1-3] because the power switches in the TL converter only have to withstand half of the input voltage. The TL circuit structure was first applied into the DC/DC converter in [4], [5]. So far, many studies have been done based on the conventional TL circuit structure [6-9]. Reference [10] proposed a novel four-switch half-bridge three-level (HBTL) DC/DC converter with zero-voltage-switching (ZVS) control strategy as shown in Fig. 1(a). In comparison with the conventional TL DC/DC converter, the four-switch HBTL converter only adds one DC-blocking capacitor but removes two clamped diodes. Therefore, the four-switch HBTL converter features with lower cost and more compact circuit structure, which makes it more suitable for the industrial applications. Due to these advantages, many studies have been done based on the four-switch HBTL converter [11-14]. In [10], the currents through the two input capacitors in the four-switch HBTL converter are analyzed with the assumption that the input power supply is regarded as an ideal voltage source, which means that the input current can change abruptly in the switching period. However, in the real applications, there exist the output inductance of the input power supply and the inductance of the input line, which would avoid the abrupt changes of the input current in the switching period and thus result in the current imbalance among the two input capacitors in the four-switch HBTL converter. The capacitor current imbalance issue would affect the reliability of the converter in aspects of the imbalance of the thermal stresses and lifetimes among the two input capacitors.

In this paper, a ZVS PWM strategy and a capacitor current balance control are proposed for the four-switch HBTL DC/DC converter. The proposed ZVS PWM strategy is composed of two operation modes with the same output performance, which can effectively achieve the ZVS for improving the converter's efficiency. What is more, a capacitor current balancing control is proposed by alternating the two operation modes of the proposed ZVS PWM strategy to eliminate the current imbalance among the two input capacitors. Therefore, the proposed control strategy can reduce the switching losses and noises, balance the thermal stresses and lifetimes among the two input capacitors, and thus greatly improve the performance and reliability of the converter. Finally, the simulation and experimental results are presented to validate the proposed control strategy.

The organization of this paper is as follows. Section II analyzes the capacitor current imbalance under the conventional control strategy. Section III presents the operation principles of the proposed ZVS PWM strategy and capacitor current balancing control. Section IV analyzes the characteristics and performances of the HBTL DC/DC converter under the proposed control strategy. Section V shows the simulation and experimental results to validate the proposed control strategy. Finally, Section VI summarizes the main contributions of this paper.

II. Analysis of Capacitor Current Imbalance

Fig. 1 shows the circuit structure of the four-switch HBTL DC/DC converter and main operation waveforms under the conventional control strategy [10]. In the primary side, two input capacitors C_1 and C_2 are used to split the input voltage V_{in} into two voltages V_1 and V_2; S_1 - S_4 and D_1 - D_4 are power switches and diodes; T_r is the high frequency transformer (HFT); L_r is the leakage inductance of T_r; C_{s1} - C_{s4} are the parasitic capacitors of S_1 - S_4; C_b is the DC-blocking capacitor. In the secondary side, there are four rectifier diodes D_{r1} - D_{r4}, one output filter inductor L_o, and one output filter capacitor C_o. In Fig. 1(a), i_{in} is the input current; i_{c1} and i_{c2} are the currents flowing through C_1 and C_2, respectively; i_p is the current of the transformer T_r; i_{Lo} is the current through L_o; V_{cb} is the voltage on C_b; i_o and V_o are the output current and output voltage; V_{ab} is the voltage between point a and b; n is the turns ratio of the transformer T_r.

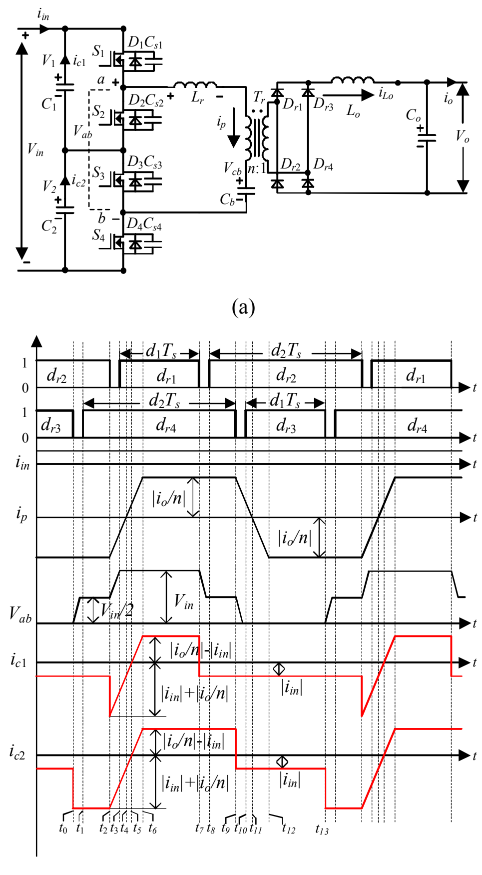


Fig. 1. (a) Circuit structure. (b) Conventional control strategy in [10].

Before discussing about the currents on the two input capacitors in the four-switch HBTL DC/DC converter, some assumptions are made as below: 1) the output filter inductor L_o is large enough to be considered as the current source; 2) the switches S_1 - S_4 and diodes D_1 - D_4 are ideal; 3) the input current i_{in} is considered as a constant in the switching period due to the output inductance of the input power supply combined with the inductance of the input line.

According to Fig. 1(b), i_{c1} and i_{c2} in one switching period namely T_s can be expressed as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \le t < t_2 \\ i_p - i_{in} & t_2 \le t < t_7 \\ -i_{in} & t_7 \le t < t_{13} \end{cases} \tag{1}$$

$$i_{c2} = \begin{cases} i_p - i_{in} & t_0 \le t < t_9 \\ -i_{in} & t_9 \le t < t_{13} \end{cases} \tag{2}$$

According to Fig. 1(b), the primary current i_p in one switching period T_s can be described as

$$i_p = \begin{cases} -\dfrac{i_o}{n} & t_0 \le t < t_2 \\ -\dfrac{i_o}{n} + \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & t_2 \le t < t_6 \\ \dfrac{i_o}{n} & t_6 \le t < t_9 \\ \dfrac{i_o}{n} - \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_9) & t_9 \le t < t_{12} \\ -\dfrac{i_o}{n} & t_{12} \le t < t_{13} \end{cases} \tag{3}$$

Substituting (3) into (1) and (2), i_{c1} and i_{c2} in one switching period can be rewritten as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \le t < t_2 \\ \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \dfrac{i_o}{n} - i_{in} & t_2 \le t < t_6 \\ \dfrac{i_o}{n} - i_{in} & t_6 \le t < t_7 \\ -i_{in} & t_7 \le t < t_{13} \end{cases} \tag{4}$$

$$i_{c2} = \begin{cases} -\dfrac{i_o}{n} - i_{in} & t_0 \le t < t_2 \\ \dfrac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \dfrac{i_o}{n} - i_{in} & t_2 \le t < t_6 \\ \dfrac{i_o}{n} - i_{in} & t_6 \le t < t_9 \\ -i_{in} & t_9 \le t < t_{13} \end{cases} \tag{5}$$

In the steady-state situation, the time intervals [t_2 - t_6] and [t_9 - t_{12}] are the same as shown in Fig. 1(b), which can be calculated by

$$t_6 - t_2 = t_{12} - t_9 = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}} \tag{6}$$

According to (4) - (6), the root-mean-square (RMS) values of i_{c1} and i_{c2} under the conventional control strategy namely $i_{c1\_rms\_c}$ and $i_{c2\_rms\_c}$ can be calculated by (7) and (8).

$$i_{c1\_rms\_c} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{7}$$

$$i_{c2\_rms\_c} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_2}{n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{8}$$

From (7) and (8), it can be observed that $i_{c1\_rms\_c}$ and $i_{c2\_rms\_c}$ are different and $i_{c2\_rms\_c}$ is bigger than $i_{c1\_rms\_c}$ because d_2 is bigger than d_1 as shown in Fig. 1(b). This current imbalance among the two input capacitors could result in the different thermal stresses and lifetimes between the two input capacitors, which would affect the converter's reliability.

III. Proposed Capacitor Current Balance Control

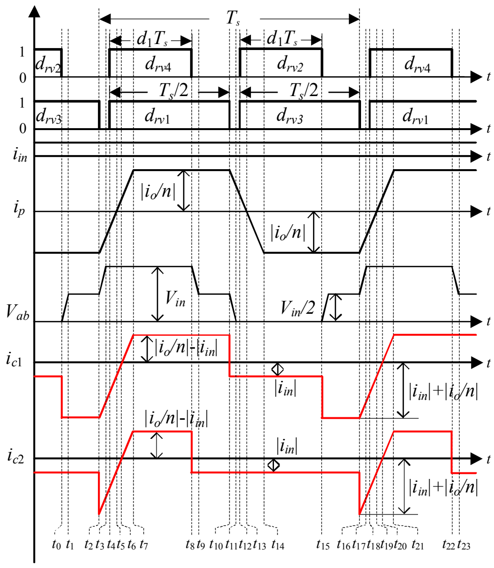
In this section, a capacitor current balancing control is proposed, which can not only achieve ZVS for the power switches but also eliminate the current imbalance among the two input capacitors.

A. Proposed ZVS PWM Strategy

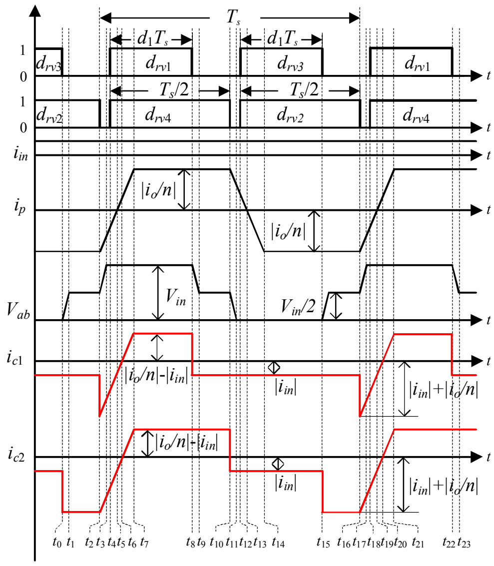
Fig. 2 shows the proposed ZVS PWM strategy including two operation modes with same output characteristics, in which d_{rv1} - d_{rv4} are four driving signals of the power switches S_1 - S_4 and d_1 is the duty ratio in one switching period. In the operation mode I, the duty ratios of d_{rv1} and d_{rv3} are 0.5 and duty ratios of d_{rv4} and d_{rv2} are d_1. On the contrary, the duty ratios of d_{rv2} and d_{rv4} are 0.5 and duty ratios of d_{rv1} and d_{rv3} are d_1 in the operation mode II.

Fig. 3 shows equivalent circuits to explain the operation principle of the operation mode I shown in Fig. 2(a).

Stage 0 [before t_0] During this stage, both S_2 and S_3 are on-state, therefore the current i_p flows through S_2, S_3, and C_b, the voltage V_{ab} is 0 V. The power from C_b is transferred to the output through T_r, D_{r2}, and D_{r3}.



(a)



(b)

Fig. 2. Proposed ZVS PWM strategy. (a) Operation mode I. (b) Operation mode II.

Stage 1 [t_0-t_1] At t_0, the switch S_2 is turned off. The capacitor C_{s2} starts to charge, and the capacitor C_{s1} begins to discharge. This stage finishes until V_{cs2} increases $V_{in}/2$ and V_{cs1} decreases 0 V.

Stage 2 [t_1-t_2] At t_1, the voltage on C_{s2} becomes zero and the diode D_1 begins to conduct. The circuit operates in a free-wheeling mode with the current i_p flowing through L_r, D_1, C_1, S_3, C_b, and T_r. During this stage, the current i_p is kept at i_o/n.

Stage 3 [t_2-t_3] At t_2, the switch S_3 is turned off. The capacitor C_{s3} starts to charge, and the capacitor C_{s4} begins to discharge. This stage finishes until V_{cs3} increases to $V_{in}/2$ and V_{cs4} decreases 0 V. The current i_p starts to increase.

Stage 4 [t_3-t_4] At t_3, the voltage on C_{s4} becomes zero and the diode D_4 begins to conduct. The circuit operates in a free-wheeling mode with the current i_p flowing through L_r, D_1, C_1, C_2, D_4, C_b, and T_r.

Stage 5 [t_4-t_5] At t_4, the switches S_1 and S_4 are turned on at zero voltage. The current i_p flows through L_r, S_1, C_1, C_2, S_4, C_b, and T_r.

Stage 6 [t_5-t_6] At t_5, the current i_p increases to 0 A and continues to increase linearly, which means the direction of i_p begins to change.

Stage 7 [t_6-t_7] At t_6, the currents i_{c1} and i_{c2} increases to 0 A, which means the directions of i_{c1} and i_{c2} begin to change.

Stage 8 [t_7-t_8] At t_7, the current i_p increases to i_o/n, then the input power V_{in} begins to be transferred to the output through T_{r1}, D_{r1}, and D_{r4}. During this stage, i_p is kept at i_o/n.

Stage 9 [t_8-t_9] At t_8, the switch S_4 is turned off. The capacitor C_{s4} starts to charge, and the capacitor C_{s3} begins to discharge. This stage finishes until V_{cs4} increases to $V_{in}/2$ and V_{cs3} decreases to 0 V.

Stage 10 [t_9-t_{10}] At t_9, V_{cs2} decreases to 0 V and diode D_3 begins to conduct. The circuit operates in a free-wheeling mode with the current i_p flowing through D_3, C_1, S_1, L_r, T_r, and C_b.

Stage 11 [t_{10}-t_{11}] At t_{10}, the switch S_1 is turned off. The capacitorC_{s1} starts to charge, and the capacitor C_{s2} begins to discharge. This stage finishes when V_{cs1} increases to $V_{in}/2$ and V_{cs2} decreases to 0 V. The current i_p starts to decrease, and the current i_{c1} decreases to -i_{in}.

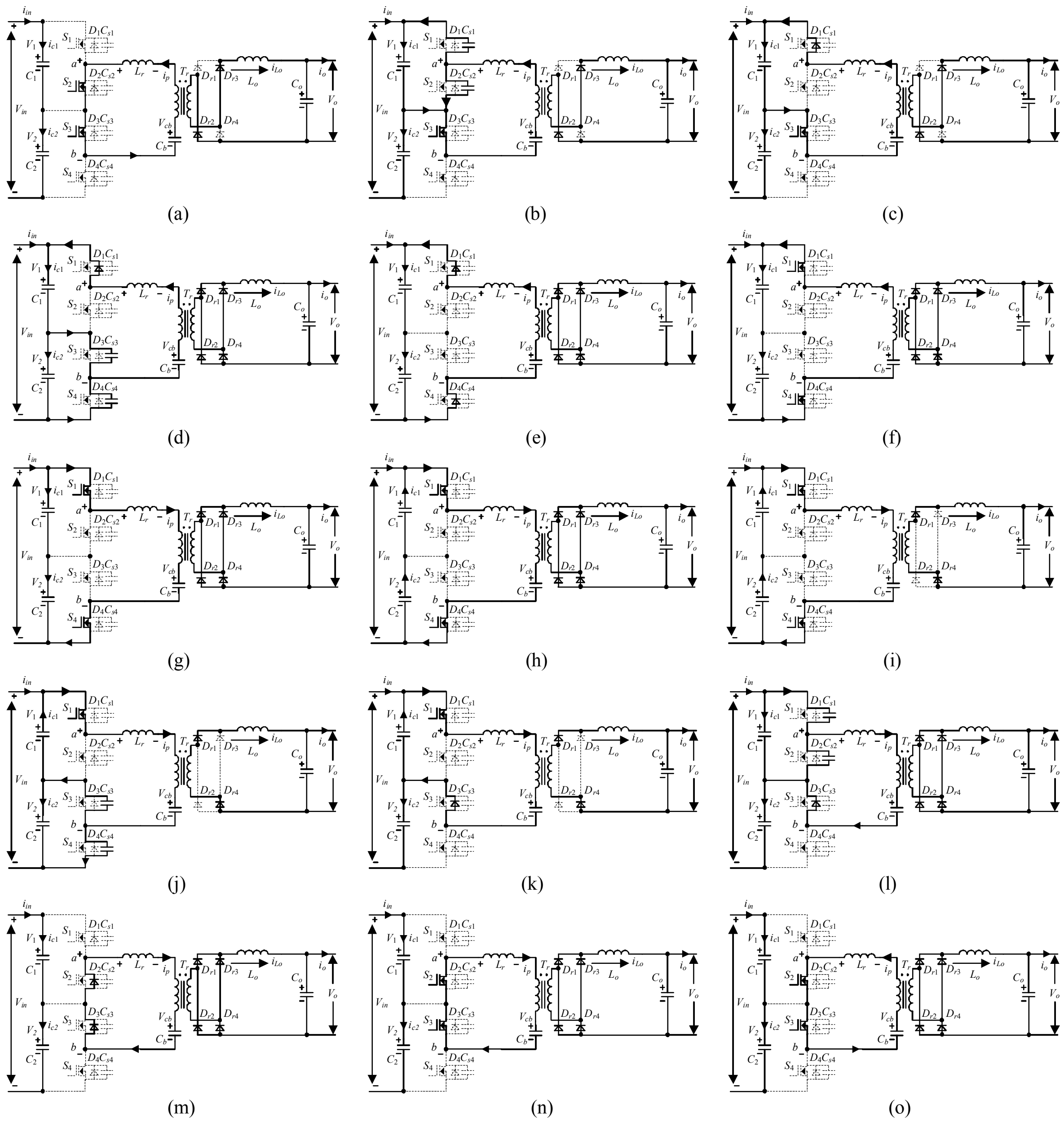
Stage 12 [t_{11}-t_{12}] At t_{11}, the voltage on C_{s2} becomes zero and diode D_2 begins to conduct. The circuit operates in a free-wheeling mode with the current i_p flowing through D_3, D_2, L_r, T_r, and C_b. Both current i_{c1} and i_{c2} are -i_{in}.

Stage 13 [t_{12}-t_{13}] At t_{12}, the switches S_2 and S_3 are turned on at zero voltage. The current i_p would flow through S_3, S_2, L_r, T_r, and C_b.

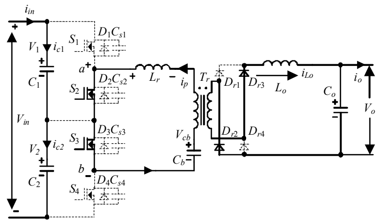
Stage 14 [t_{13}-t_{14}] At t_{13}, the current i_p decreases to 0 A and continues to decrease linearly, which means the direction of i_p begins to change.

Stage 15 [t_{14}-t_{15}] At t_{14}, the current i_p decreases to -i_o/n, then the power is transferred from C_b to the output through T_r, D_{r2}, and D_{r3}. During this stage, the current i_p is kept at -i_o/n.

At t_{15}, the following work operation in the next cycle starts, which is same as the first switching period. The analysis of the operation mode II is similar as that of the operation mode I, which is not repeated here.



(a) (b) (c) (d) (e) (f) (g) (h) (i) (j) (k) (l) (m) (n) (o)



(p)

Fig. 3. Equivalent circuits under the operation mode I. (a) [before t_0]. (b) [t_0 - t_1]. (c) [t_1 - t_2]. (d) [t_2 - t_3]. (e) [t_3 - t_4]. (f) [t_4 - t_5]. (g) [t_5 - t_6]. (h) [t_6 - t_7]. (i) [t_7 - t_8]. (j) [t_8 - t_9]. (k) [t_9 - t_{10}]. (l) [t_{10} - t_{11}]. (m) [t_{11} - t_{12}]. (n) [t_{12} - t_{13}]. (o) [t_{13} - t_{14}]. (p) [t_{14} - t_{15}].

B. Proposed Capacitor Current Balance Control

Based on the above analysis, the main difference between the operation mode I and II is that the RMS value of i_{c1} is bigger than that of i_{c2} in the operation mode I but the RMS value of i_{c1} is smaller than that of i_{c2} in the operation mode II. In order to balance these two currents i_{c1} and i_{c2}, a capacitor current balance control is proposed by alternating the two operation modes. Fig. 4 shows the proposed control for balancing the currents on the two input capacitors, in which d_{rv1} - d_{rv4} are four driving signals of the power switches S_1 - S_4 and d_1 is duty ratio in one switching period. In the proposed capacitor current balancing control, the operation mode I is used for the first switching period and the operation mode II is used for the second switching period, which makes the currents on the two input capacitors are the same in every two switching periods as shown in Fig. 4.

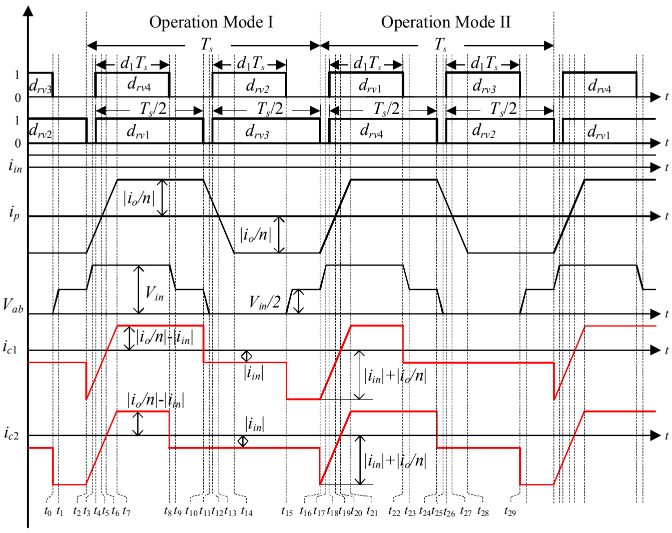


Fig. 4. Proposed capacitor current balancing control.

IV. Characteristics and Performances under the Proposed Control Strategy

A. Output Characteristic

If neglecting the duty ratio loss, the average output voltage V_o is

$$V_o = \frac{1}{n} \cdot \left[(V_{in} - V_{cb}) \cdot d_1 + V_{cb} \cdot d_1 \right] \tag{9}$$

Assuming that the DC-blocking capacitor is large enough to be considered as a voltage source, the voltage on the DC-blocking capacitor is

$$V_{cb} = \frac{V_{in}}{2} \tag{10}$$

Substituting (10) into (9), then the output voltage can be expressed by

$$V_o = \frac{V_{in}}{n} \cdot d_1 \tag{11}$$

The duty cycle loss in one switching period as shown in Fig. 4 can be given by

$$d_{loss} = 2 \cdot (\frac{t_7 - t_2}{T_s}) = \frac{8 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \tag{12}$$

where d_{loss} is the duty cycle loss.

After considering the effect of duty cycle loss, the output voltage can be calculated by

$$V_o = \frac{V_{in}}{n} \cdot (d_1 - \frac{d_{loss}}{2}) = \frac{V_{in}}{n} \cdot (d_1 - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}) \tag{13}$$

B. ZVS Achievement Conditions

Before discussing the ZVS achievement conditions under the proposed control strategy, one assumption is made that the parasitic capacitors of S_1 - S_4 are the same namely C_s.

In the operation mode I, the energy E_1 calculated by (14) is needed to ensure the switches S_1 and S_3 realizing zero-voltage switch-on. The energy to achieve zero-voltage switch-on for S_1 and S_3 is provided by both the output filter inductance and the leakage inductance.

$$E_1 = \frac{1}{2} \cdot C_{s4} \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_{s3} \cdot (\frac{V_{in}}{2})^2 = \frac{1}{4} \cdot C_s \cdot V_{in}^2 \tag{14}$$

The energy of the leakage inductance of the transformer is used to achieve zero-voltage switch-on of switches S_2 and S_4. Therefore, in order to achieve the zero-voltage switch-on of switches S_2 and S_4, (15) should be satisfied.

$$\frac{1}{2} \cdot L_r \cdot \left(\frac{I_o}{n} \right)^2 \geq \frac{1}{2} \cdot C_{s1} \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_{s2} \cdot (\frac{V_{in}}{2})^2 = \frac{1}{4} \cdot C_s \cdot V_{in}^2 \tag{15}$$

In the operation mode II, the analysis of the ZVS achievement conditions is similar to that in the operation mode I as above, which is not repeated here.

The proposed capacitor current balance control operates by alternating the operation mode I and II, therefore the ZVS achievement conditions of the proposed capacitor current balance control is the combination of the ZVS achievement conditions of the operation mode I and II. In the first switching period, the energy from both the output filter inductance and leakage inductance of the transformer is provided for S_1, S_3 to realize the zero-voltage switch-on and the energy from the leakage inductance is provided for S_2, S_4 to achieve the zero-voltage switch-on. In the second switching period, the ZVS achievement conditions are just contrary to that in the first switching period, which means the energy from both the output filter inductance and leakage inductance of the transformer is provided for S_2, S_4 to realize the zero-voltage switch-on and the energy from the leakage inductance is provided for S_1, S_3 to achieve the zero-voltage switch-on.

C. Analysis of Input Capacitor Currents

According to Fig. 4, the expressions of i_{c1} and i_{c2} in two switching periods can be given by

$$i_{c1}=\begin{cases}-i_{in} & [t_0-t_2]\\ i_p-i_{in} & [t_2-t_{10}]\\ -i_{in} & [t_{10}-t_{15}]\\ i_p-i_{in} & [t_{15}-t_{22}]\\ -i_{in} & [t_{22}-t_{29}]\end{cases} \tag{16}$$

$$i_{c2}=\begin{cases}i_p-i_{in} & [t_0-t_8]\\ -i_{in} & [t_8-t_{16}]\\ i_p-i_{in} & [t_{16}-t_{24}]\\ -i_{in} & [t_{24}-t_{29}]\end{cases} \tag{17}$$

Because the frequency of the primary current i_p is same as the switching frequency, i_p in one switching period as shown in Fig. 4 can be given by.

$$i_p=\begin{cases}-\dfrac{i_o}{n} & [t_0-t_2]\\ -\dfrac{i_o}{n}+\dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2) & [t_2-t_7]\\ \dfrac{i_o}{n} & [t_7-t_{10}]\\ \dfrac{i_o}{n}-\dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2) & [t_{10}-t_{14}]\\ -\dfrac{i_o}{n} & [t_{14}-t_{15}]\end{cases} \tag{18}$$

Substituting (18) into (16) and (17), i_{c1} and i_{c2} can be expressed by

$$i_{c1}=\begin{cases}-i_{in} & [t_0-t_2]\\ \dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\dfrac{i_o}{n}-i_{in} & [t_2-t_7]\\ \dfrac{i_o}{n}-i_{in} & [t_7-t_{10}]\\ -i_{in} & [t_{10}-t_{15}]\\ -\dfrac{i_o}{n}-i_{in} & [t_{15}-t_{16}]\\ \dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\dfrac{i_o}{n}-i_{in} & [t_{16}-t_{21}]\\ \dfrac{i_o}{n}-i_{in} & [t_{21}-t_{22}]\\ -i_{in} & [t_{22}-t_{29}]\end{cases} \tag{19}$$

$$i_{c2}=\begin{cases}-\dfrac{i_o}{n}-i_{in} & [t_0-t_2]\\ \dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\dfrac{i_o}{n}-i_{in} & [t_2-t_7]\\ \dfrac{i_o}{n}-i_{in} & [t_7-t_8]\\ -i_{in} & [t_8-t_{16}]\\ \dfrac{V_{in}}{2\cdot L_r}\cdot(t-t_2)-\dfrac{i_o}{n}-i_{in} & [t_{16}-t_{21}]\\ \dfrac{i_o}{n}-i_{in} & [t_{21}-t_{24}]\\ -i_{in} & [t_{24}-t_{29}]\end{cases} \tag{20}$$

The time intervals [t_2 - t_7], [t_{10} - t_{14}], [t_{16} - t_{21}], and [t_{24} - t_{28}] as shown in Fig. 4 can be described as

$$t_7-t_2=t_{14}-t_{10}=t_{21}-t_{16}=t_{28}-t_{24}=\frac{4\cdot L_r\cdot i_o}{n\cdot V_{in}} \tag{21}$$

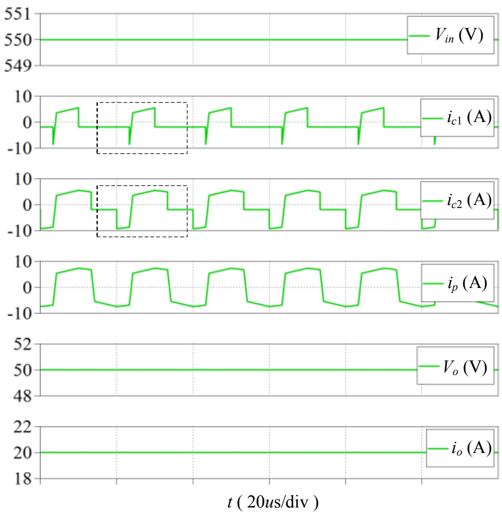
According to (19), (20) and (21), the RMS values of i_{c1} and i_{c2} under the proposed control namely $i_{c1\_rms\_p}$ and $i_{c2\_rms\_p}$ can be calculated as (22).

$$i_{c1\_rms\_p}=i_{c2\_rms\_p}=\sqrt{\begin{aligned}&i_{in}^2+\frac{i_o^2}{2\cdot n^2}+\frac{8\cdot L_r\cdot i_{in}\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}\ldots\\&-\frac{2\cdot i_{in}\cdot i_o\cdot D_1}{n}-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}\end{aligned}} \tag{22}$$

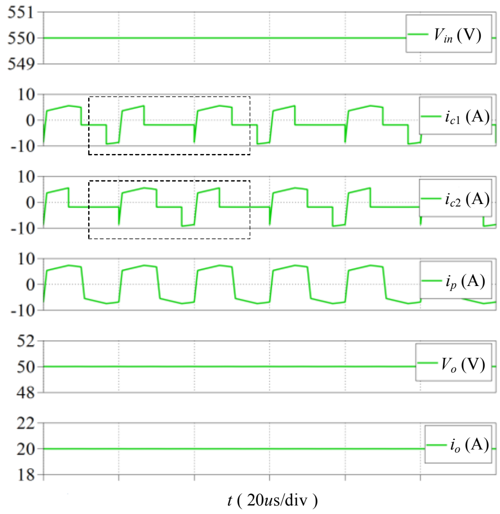
V. Simulation and Experimental Verification

A. Simulation Verification

In order to verify the proposed control strategy, a simulation model is built, whose parameters are listed in Appendix. In the simulation, the input voltage V_{in} is 550 V, the output voltage V_o is 50 V, and the output power namely P_o is 1-kW. Figs. 5(a) and (b) show simulation results under the conventional control strategy and the proposed control strategy, respectively.



(a)



(b)

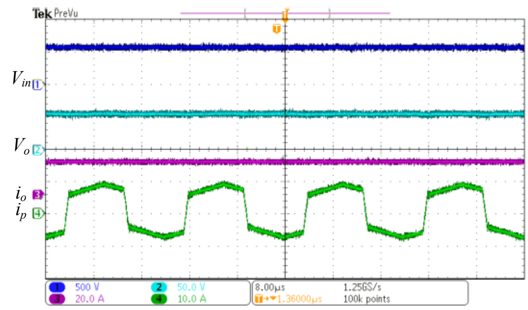
Fig. 5. Simulation results including V_{in}, i_{c1}, i_{c2}, i_p, V_o, and i_o. (a) Conventional control strategy. (b) Proposed control strategy.

Fig. 5(a) shows that i_{c1} and i_{c2} are different under the conventional control strategy, whose RMS values are 3.05 A and 5.11 A respectively. Under the proposed control strategy, the frequencies of i_{c1} and i_{c2} are twice of the switching frequency, i_{c1} and i_{c2} are the same, whose RMS values are both 4.2 A, as shown in Fig. 5(b). In summary, the simulation results verify that the current imbalance among the two input capacitors C_1 and C_2 are effectively eliminated by utilizing the proposed control strategy.

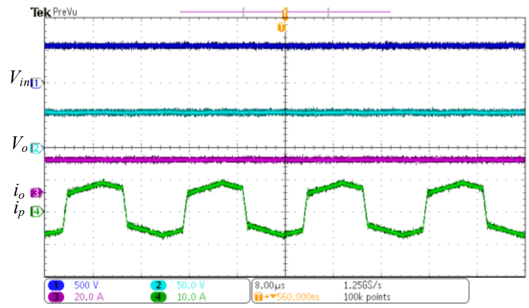
B. Experimental Verification

A 1-kW 50 kHz prototype is built to verify the above theoretical analysis. The specifications of the built prototype are listed in Appendix. In the experiments, the output voltage V_o is 50 V, and the input voltage is 450 V - 550 V. The turns ratio of the transformer T_r is 25:8. SPW47N60C3 is adopted as the primary power switches. MBR40250TG is selected for the output rectifier diodes. The performances of the established prototype are shown in Figs. 6 and 7 under the working conditions that the input voltage V_{in} is 550 V and the output power P_o is 1-kW.

Figs. 6(a) and (b) show the currents i_p, i_o and voltages V_{in}, V_o under the conventional and proposed control strategy, respectively. It can be seen that the primary currents i_p are almost the same under the two control strategies. The frequencies of i_{c1} and i_{c2} under the proposed control strategy are twice of that under the conventional control strategy as marked in Fig. 7, which is consistent with the theoretical analysis. In addition, i_{c1} and i_{c2} are different under the conventional control strategy, whose RMS values are 3.16 A and 5.18 A respectively, as shown in Fig. 7(a). Therefore, the difference between $i_{c1\_rms\_c}$ and $i_{c2\_rms\_c}$ are 2.02 A. After using the proposed control strategy, i_{c1} and i_{c2} are almost the same and their RMS values are 4.36 A and 4.39 A, respectively, as shown in Fig. 7(b).

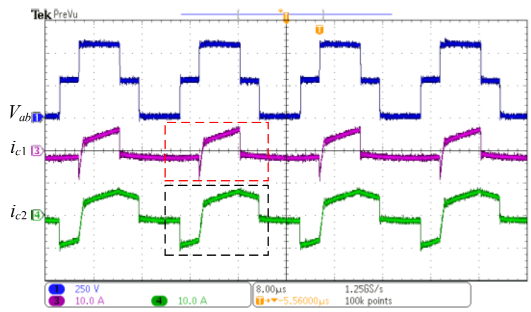


(a)

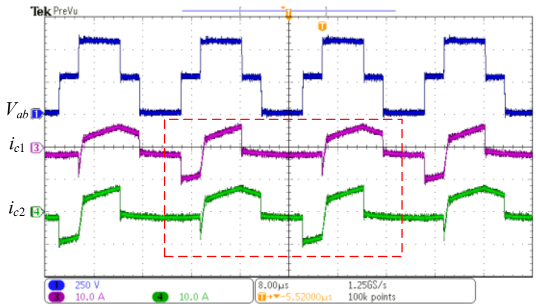


(b)

Fig. 6. Experimental results including V_{in}, V_o, i_o, and i_p at V_{in} = 550 V and P_o = 1-kW. (a) Conventional control strategy. (b) Proposed control strategy.



(a)



(b)

Fig. 7. Experimental results including V_{ab}, i_{c1}, and i_{c2} at V_{in} = 550 V and P_o = 1-kW. (a) Conventional control strategy. (b) Proposed control strategy.

VI. CONCLUSIONS

In this paper, a ZVS PWM strategy and a capacitor current balancing control is proposed for the four-switch HBTL DC/DC converter. The proposed ZVS PWM strategy composed of two operation modes can achieve the ZVS for the efficiency improvement. In addition, a capacitor current balance control is proposed by alternating the two operation modes of the proposed ZVS PWM strategy to eliminate the current imbalance among the two input capacitors. Therefore, the proposed control strategy can reduce the switching losses and noises, balance the thermal stresses and lifetimes among the two input capacitors, and thus improve the performance and reliability of the converter. Finally, the simulation and experimental results verify the proposed control strategy.

APPENDIX

TABLE I. PARAMETERS OF THE SIMULATION MODEL AND EXPERIMENTAL PROTOTYPE

Description	Parameter
Turns Ratio of Transformer T_r	25:8
Leakage Inductances L_r (uH)	20.7
Output Filter Capacitor C_o (uF)	470
Output Filter Inductors L_o (uH)	140
Input Capacitors C_1 and C_2 (uF)	14.4
DC-blocking Capacitors C_b (uF)	12
Switching Frequency (kHz)	50
Dead Time (ns)	400

REFERENCES

[1] B. M. Grainger, A. R. Sparacino, R. J. Kerestes, and M. J. Korytowski, "Advancements in medium voltage DC architecture development with applications for powering electric vehicle charging stations," in *Energytech, 2012 IEEE*, 2012, pp. 1–8.

[2] M. Saeedifard, M. Graovac, R. F. Dias, and R. Iravani, "DC power systems: Challenges and opportunities," in *Proc. IEEE Power Energy Soc. Gen. Meet*., 2010, pp. 1–7.

[3] X. Ruan, B. Li, Q. Chen, S. C. Tan, and C.K. Tse, "Fundamental considerations of three-level dc-dc converters: Topologies, analyses, and control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3733–3743, Dec. 2008.

[4] J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter—A new concept in high-voltage DC-to-DC conversion," in *Proc. IEEE Int. Conf. Ind. Electron. Control Instrum. Autom*., 1992, pp. 173–178.

[5] J. R. Pinheiro and I. Barbi, "The three-level ZVS-PWM DC-to-DC converter," *IEEE Trans. Power Electron*., vol. 8, no. 4, pp. 486–492, Jul. 1993.

[6] F. Canales, P. Barbosa, and F. C. Lee, "A zero-voltage and zero-current switching three-level dc/dc converter," *IEEE Trans. Power Electron*., vol. 17, no. 6, pp. 898–904, Nov. 2002.

[7] Z. Guo, K. Sun, and D. Sha, " Improved ZVS three-level dc-dc converter with reduced circulating loss," *IEEE Trans. Power Electron*., vol. 31, no. 9, pp. 6394–6404, Sep. 2016.

[8] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Power Electron*., vol. 20, no. 2, pp. 395–404, Mar. 2005.

[9] Z. Zhang and X. Ruan, "ZVS PWM full-bridge three-level converter," in *Proc. 4th Int. Power Electron. Motion Control Conf*., 2004, pp. 1085–1090.

[10] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC/DC converter: Four switches $V_{pk} = V_{in}$ /2, capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron*., vol. 19, no. 4, pp. 918–927, Jul. 2004.

[11] Y. Shi, and X. Yang, "Wide-range soft-switching PWM three-level combined DC–DC converter without added primary clamping devices," *IEEE Trans. Power Electron*., vol. 29, no. 10, pp. 5157–5171, Oct. 2014.

[12] W. Li, S. Zong, F. Liu, H. Yang, X. He, and B. Wu, "Secondary-side phase-shift-controlled ZVS DC/DC converter with wide voltage gain for high input voltage applications," *IEEE Trans. Power Electron*., vol. 28, no. 11, pp. 5128–5139, Nov. 2013.

[13] T. T. Sun, H. S. H. Chung, and A. Ioinovici, "A high-voltage DC-DC converter with Vin /3—Voltage stress on the primary switches," *IEEE Trans. Power Electron*., vol. 22, no. 6, pp. 2124–2137, Nov. 2007.

[14] X. Yu, K. Jin, and Z. Liu, "Capacitor voltage control strategy for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron*., vol. 29, no. 4, pp. 1557–1561, Apr. 2014.