A Dual-Bridge Hybrid DC Circuit Breaker

Zhang, Hanwen; Li, Gen; Wang, Yanbo; Liu, Chuang; Chen, Zhe

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A Dual-Bridge Hybrid DC Circuit Breaker

Hanwen Zhang
AAU Eenergy
Aalborg University
Aalborg, Denmark
hzha@et.aau.dk

Gen Li
School of Engineering
Cardiff University
Cardiff, UK
LiG9@cardiff.ac.uk

Yanbo Wang
AAU Eenergy
Aalborg University
Aalborg, Denmark
ywa@et.aau.dk

Chuang Liu
School of Electrical Engineering
Northeast Electric Power University
Jilin, China
victorliuchuang@163.com

Zhe Chen
AAU Eenergy
Aalborg University
Aalborg, Denmark
zch@et.aau.dk

***Abstract*— Various DC circuit breakers (DCCBs) have been widely proposed for the DC fault protection of high-voltage direct-current (HVDC) grids. In recent years, hybrid DCCBs (HCBs) have been paid significant attentions due to their features of low power losses and fast dynamic response. However, several aspects regarding the design of HCB should be further addressed. For instance, the requirement of deploying a large surge arrester to dissipate the large fault current energy should be further addressed and the strategy to perform zero-voltage switching (ZVS) of semiconductor devices during the post-fault restoration processes should be investigated. In this paper, a dual-bridge hybrid DC circuit breaker (DB-HCB) with freewheeling diode branches is proposed to address the above issues. The operation principle of the proposed DB-HCB for pole-to-ground and pole-to-pole faults is presented. Compared with other HCBs, the capacity of the surge arrester is obviously reduced, so that the capital cost and volume of the proposed DB-HCB is decreased. Moreover, the ZVS is implemented during the post-fault restoration processes. Simulation results in PSCAD/EMTDC are given to validate the effectiveness of the proposed DB-HCB.**

Keywords—DC circuit breaker, DC protection, DC fault current, DC grid, HVDC, MTDC, fault protection, surge arrester.

I. INTRODUCTION

Renewable energy sources (RES), such as wind power and solar power, etc. are playing significant roles in achieving sustainable and low-carbon development [1]-[3]. Due to the remote geographical location of large-scale RES, high-voltage direct-current (HVDC) transmission system has been widely utilized for renewable energy integration [4]-[5]. Nowadays, the voltage source converter (VSC)-based HVDC technology has been increasingly adopted in HVDC transmission system compared with the line-commutated-converter-(LCC) based HVDC system [6]-[9].

DC circuit breaker (DCCB) is one of critical components in VSC-HVDC systems, which is able to provide a fast and reliable DC fault protection for multi-terminal HVDC (MTDC) grids [10]-[12]. The interruption of DC fault current is difficult due to the lack of the natural current zero-crossing and its high rising-rate [13]. Therefore, the DCCBs have been paid the increasing concerns from academia and industry.

DCCBs consist of mechanical circuit breakers (MCBs), solid-state circuit breakers (SSCBs) as well as hybrid circuit breakers (HCBs) [14]. MCB has low on-state losses and high reliability. However, the fault current interruption time of the MCB can be delayed to tens milliseconds or longer due to long-term operation of mechanical switch, which reduces the safety for MTDC grid protection [15]. In SSCBs, power electronic devices are adopted to improve the current interruption speed [16]. However, the on-state power losses of SSCBs are high due to the internal resistance of power electronic devices. Moreover, cooling systems for the normal operating branch are required, which also increases the system complexity and volume [10]. Compared with the MCB and SSCB, HCB combines the advantages of the two solutions. The HCB exhibits the fast interrupting speed as well as the low on-state power losses [17]-[19]. However, the high capital cost and large volume commonly limit the practical application of HCBs in MTDC systems.

In recent years, the intensive research regarding HCB has been performed. The HCB is originally proposed for HVDC application by ABB company in 2012, which uses front-to-front connected insulated gate bipolar transistors (IGBTs) in the load commutation switch (LCS) and main breaker (MB) to achieve bidirectional operation [10], [20]. In normal condition, the load current flows through the branch of the ultra-fast disconnector (UFD) and the LCS, which exhibits the merit of the low power losses. In fault condition, the fault current will be commutated to the MB under the arc voltage by turning off the LCS. The UFD can be opened under zero current once the current in this branch fully commutates to the MB. Then, the fault current will be forced to the surge arrester by blocking the MB, so that the energy will be dissipated.

The deployment of the IGBT-based MB implements the excellent current breaking capability and arc extinction capacity. Therefore, the interruption speed of DCCB is significantly improved. However, the VSCs are always connect to the fault point during the fault current interrupting and energy dissipating processes. Therefore, it fails to isolate the converter from the faulted line until the fault current completely diminished. Additionally, the surge arrester needs to absorb a large amount

of fault current energy within a short period which may lead to overheating and a large reverse-voltage. Therefore, the requirements for the capacity of the surge arrester and the insulation of the DCCB will be high. Another issue of the HCB is that the IGBTs fail to achieve the zero voltage switching (ZVS) during the post-fault restoration process. Further, it is difficult to perform the dynamic voltage balancing of IGBTs [21].

A full-bridge submodule (FB-SM)-based HCB is proposed and applied in Zhoushan five-terminal VSC-HVDC project [22]-[23]. Due to the employment of the SM capacitor, the issue of the dynamic voltage balancing of the IGBT modules in the above HCB has been addressed. It can be seen that a number of semiconductor devices and capacitors are required, so that the capital cost and power losses are increased.

In order to reduce the number of IGBTs, a diode FB-SM - based HCB is proposed and applied in the Zhangbei 500 kV four-terminal DC grid project [24]. The capital cost is reduced compared with the circuit used in Zhoushan project. However, the stray inductance of the series-connected diodes may prolong the current conduction time. Hence, the magnitude of the interruption current is higher than the above topologies. In [25], a thyristor-capacitor-based HCB is proposed to mitigate the use of IGBT, which needs the parallel auxiliary branch to limit fault current. In this case, the magnitude of the interrupted fault current can be increased.

The surge arresters of the abovementioned DCCBs are required to absorb energy of fault current. In [26], a surge-arrester-less SSCB is proposed to address the above issues. However, this surge-arrester-less SSCB has the evident drawbacks such as unidirectional current interrupting and high on-state power losses.

To address the above issues, this paper presents a dual-bridge HCB (DB-HCB) with the additional freewheeling diode branches, which is able to reduce the capacity and volume of the surge arrester as well as maintain the energy dissipating capability. The strategy of the fault current interruption and the post-fault restoration is developed for both pole-to-ground and pole-to-pole faults. The fault interruption process consists of two stages, including the current commuting stage and the energy dissipating stage. The proposed DB-HCB can rapidly isolate the VSCs from the faulted circuit after the current commuting stage. The fault current energy will then be gradually dissipated by the surge arresters in the freewheeling diode branches. Moreover, the ZVS can be implemented in the post-fault restoration process, which improves the safety and the lifetime of the DB-HCB. The effectiveness of the proposed DB-HCB is verified by time-domain simulations in PSCAD/EMTDC.

II. Topology of the Proposed DB-HCB

Fig. 1 shows the circuit configuration of the proposed DB-HCB. It can be seen that the terminal A and C are connected to DC source and DC transmission line, respectively. Terminal B is connected to the ground. The DB-HCB consists of dual symmetrical bridges, where each bridge consists of four parts.

a) Disconnector. The disconnector is a UFD which is able to isolate the converter from the faulted circuit when the fault current is interrupted.

b) Normal current carrying branch (NCCB). The NCCB consists of a UFD and an IGBT-based bidirectional LCS, which provides the path for normal current in steady-state.

c) Fault current breaking branch - main breaker (MB). The MB consists of a number of unidirectional series-connected IGBT modules. The IGBTs in two MBs form a front-to-front connection. The circuit with a capacitor C_Q and a resistor R_Q is deployed in paralleled with each IGBT module.

d) Energy dissipating branch (EDB). In the EDB, the freewheeling diodes are connected in series with a surge arrester. Snubber resistor R_D is paralleled with each diode.

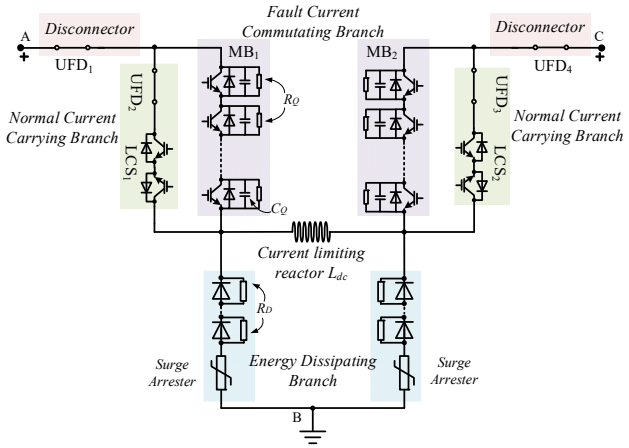


Fig. 1. The circuit configuration of the proposed DB-HCB.

III. Operating Principle of the DB-HCB

A. Fault current interruption

It is assumed that the terminal A is connected to a converter and the terminal C is connected to the DC line, and a DC fault occurs in the DC line. The fault current interrupting principles of the proposed DB-HCB are illustrated in Fig. 2 and explained as follows.

1) The normal current i_N passes through the two NCCBs and the current limiting reactor L during normal operation, as shown in Fig. 2(a). The two MBs are operated in the off-state.

2) The current i_F will start to increase in case of a DC line fault. The current path of the fault current i_F is shown in Fig. 2(b) before it reaches the specified protection threshold.

3) The LCSs in the two NCCBs will be terminated once the magnitude of i_F reaches the specified thresholds. In order to speed up the current commutation process, the IGBTs in MB_1 and MB_2 can be triggered earlier before blocking the LCS. The fault current will commutate to the MBs.. Fig. 2(c) shows the fault current path at this stage.

4) The UFDs in the two NCCBs will be opened at zero current once the fault current fully commutates to the MBs. This process may take 1 to 2 ms. Then, MBs can be blocked and i_F will charge the capacitor C_Q in MB_1. The voltage of each mode in MB_1 can be balanced due to the capacitor C_Q. Fig. 2(d) shows the fault current path at this stage.

5) The fault current i_F will reach the maximum value once the voltage of C_Q in MB_1 is equal to the voltage of terminal A. Then, the freewheeling diodes in EDB provide the path for the residual fault current so as to dissipate the energy stored in the current limiting reactor. At this moment, the converter has been isolated from the faulted circuit by opening the UFD_1 under zero current. In this way, the converter is safely isolated from the faulted circuit. Then, the fault current is dissipated through the surge arrester and the freewheeling diodes in the EDB and MB_2. The fault current path at this stage is shown in Fig. 2(e). Then, the residual current will decay to zero.

6) The UFD_4 is activated when the residual current decay to zero. Then, the fault circuit is fully isolated. The energy stored in the C_Q is fully dissipated by R_Q over a certain time period. The last stage is shown in Fig.2(f).

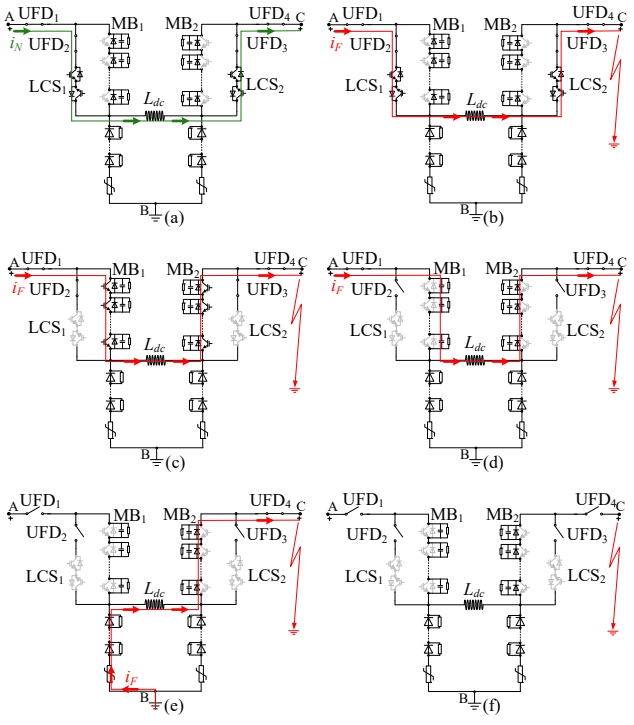


Fig. 2. Fault current interrupting processes of the proposed DB-HCB.

B. Fault current interruption Post Fault Restoration

After the fault current is interrupted, there exists a deionization period to extinguish the residual arc, and the faulted line is under low voltage. The following steps will be executed once the DB-HCB receives a reclosing order from the high-level control system.

1) The first step is to close the UFD_1 and UFD_4.

2) Turn on the IGBTs in the two MBs once the UFD_1 and UFD_4 are fully closed.

3) After the above operations, the load current flows through the DB-HCB and charge the DC line naturally.

4) Close the UFD_2 and UFD_3, and turn on the LCS_1 and LCS_2 in the two NCCBs. Then, the current will commutate to the two NCCBs.

5) Turn off the IGBTs in the two MBs. The switching process of the IGBTs implement the ZVS.

IV. Desgin of the Surge Arrester

Compared with other HCBs, one of the advantages of proposed DB-HCB is reduced capacity of the MB surge arrester, so that the volume and capital cost is reduced. A comparative analysis between the proposed DB-HCB and the ABB HCB is given in Table I.

TABLE I

THE COMPARISON OF THE ABB HCB AND THE PROPOSED DB-HCB

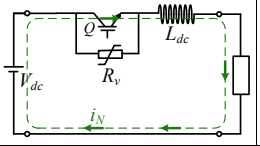
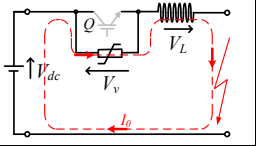
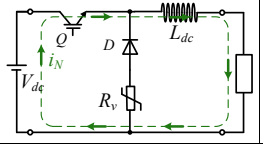
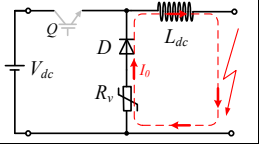
Items	In normal condition	In fault condition
ABB HCB		
DB HCB		

Table I shows the equivalent circuits and operation principles of the ABB HCB and the proposed DB-HCB. The voltage source V_{dc} supplies the resistive load. The inductor L_{dc} represents the overall inductance of the DCCB and DC transmission line. Q is a solid-state power switch that represents the IGBTs in the MB. R_v represents the variable resistance of the surge arrester.

A. ABB HCB

In normal condition, the load current i_N flows to the load through Q. Q will be turned off immediately if a fault is detected. It is assumed that I_0 is the instantaneous current at the moment of turning off Q, and it will be commutated to R_v. The voltage stress of Q equals the clamping voltage of R_v. It is assumed that the clamping voltage of the arrester is V_v. Then, it can be presented as (1)

$$V_v = V_{dc} + V_L \tag{1}$$

where V_L is the voltage of L_{dc} when Q is turned off (t=0). Therefore, the current in L_{dc} can be represented as (2).

$$i_L(t) = I_0 - \frac{V_L}{L_{dc}} t \cdot \tag{2}$$

Then, the fault energy is dissipated by the arrester, and the fault current is decreased to zero gradually. The time that the current i_L is decreased to zero can be represented as (3).

$$T_{open} = \frac{L_{dc}}{V_L} I_0 \tag{3}$$

The fault energy W_R absorbed by the arrester during the energy dissipating period until time instant T_{open} can be represented as (4).

$$W_R = \int_0^{T_{open}} (V_{dc} + V_L) i_R dt \tag{4}$$

where i_R is the current flowing by R_v. and the i_R is equal to i_L during the energy dissipating period. Then, the following equation can be obtained as (5) by combining (1)-(4).

$$W_R = \left(\frac{V_{dc}}{V_L} + 1 \right) \frac{1}{2} L_{dc} I_0^{\,2} \tag{5}$$

The V_L is much lower than V_{dc} at the moment of turning off Q. Thus, the energy W_R absorbed by the arrester is much higher than the energy stored ($L_{dc}I_0^2/2$) in L_{dc} at $t = 0$. In design of the surge arrestor, the high energy can be dissipated quickly without causing overheating and overvoltage. Moreover, the DC source is still in fault current path during the de-energizing process.

B. DB-HCB

The design guideline of the proposed DB-HCB is explained by the equivalent model as shown in Table I. During steady-state operation, the load current i_N flows through the switch Q to the load. Q is switched off once the value of the fault current reaches the specified threshold. Then, the fault current will commutate to the diode D and the nonlinear resistor R_V. Meanwhile, the DC source is isolated from the faulted circuit.

The residual energy stored in L_{dc} is exhausted by R_v. The energy absorbed by R_V can be calculated as (6).

$$W_R = \frac{1}{2} L_{dc} I_0^{\,2} . \tag{6}$$

It can be seen from (5)-(6) that WR of the proposed DB-HCB is lower than ABB's HCB. Therefore, the capacity and volume of the surge arrester can be dramatically reduced, which is an evident advantage for the proposed DB-HCB. Moreover, the front-to-front connected IGBTs in the MB of ABB's HCB are equally deployed in the two bridges (MBs) of the proposed DB-HCB. Therefore, the proposed DB-HCB has the same number of IGBTs in the MB compared with ABB's HCB. Also, the MBs in the proposed DB-HCB can be replaced by different MBs with preserving the advantages of the proposed topology.

V. Simulation Verification

To validate the effectiveness of fault current interruption and post-fault restoration capability of the proposed DB-HCB, a model of the proposed DB-HCB with 650 MW and ± 320 kV is developed in PSCAD/EMTDC, where both pole-to-ground and pole-to-pole faults are tested. The parameters for the simulation case are given in Table II.

TABLE II

CIRCUIT PARAMETERS IN SIMULATION CASE

Items	Values
Power rating	640 MW
Nominal DC line voltage	320 kV
Load impendence	160 Ω
Number of each main breaker IGBTs	120
Nominal voltage of R_V	20 kV
Current limiting reactor L_{dc}	100 mH
R_D	470 kΩ
R_Q	1 kΩ
C_Q	4 μF

A. Pole-to-ground fault

Fig. 3 shows the test circuit of a pole-to-ground fault. The system rated load current i_N is 2 kA. The mechanical breaker S_{fault} is placed to produce the short-circuit. The opening time of UFDs (S_1 and S_2) is set as 2 ms with the consideration of practical condition. The UFD can only switch under zero current. IGBTs (T_2) in the MBs are in off-state during the normal operation. The specified protection threshold of the LCS (T_1) is 2 times of the rated load current.

For the post-fault reclosing of the DB-HCB, it is assumed that the fault detection and discrimination have been successfully conducted by the protection system. The proposed DB-HCB is reclosed when the fault is fully cleared and the fault energy is safely dissipated.

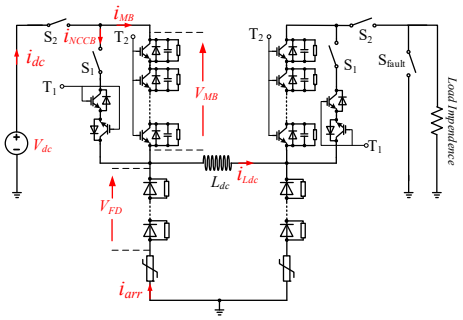


Fig. 3. The simulation circuit of the proposed DB-HCB.

In normal condition, the load current flows through NCCBs and L_{dc}. During this period, it can be seen from Fig. 4 that i_{NCCB} equals to i_{dc} whose value is 2 kA. The pole-to-ground fault happens at the time of 0.01s by closing the S_{fault}. It shows that i_{dc} starts to increase at $t = 0.01$ s.

As mentioned above, the turn-off signal of T_1 is 4 kA. To prevent the failure of fault current commutation, T_2 will turn on in advance at the time when i_{NCCB} equals to 3 kA. The fault current reaches to 4 kA at the time of 0.0106s as shown in Fig. 4. Then, the current i_{NCCB} becomes zero and the fault current is commutated to the MB naturally once T_1 is turned off.

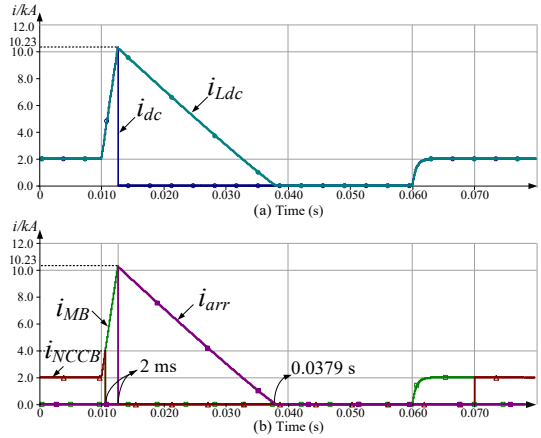


Fig. 4. Current waveforms during a pole-to-ground fault.

The S_1 opens in 2ms, where the current i_{MB} is increased to 10.23 kA. S_1 opens at the time of 0.0126 s. The fault current is blocked after turning off the T_2 in the MBs as shown in Fig. 4, where i_{dc} drops to zero. From 0.0126 s to 0.0379 s, the currents i_{Ldc} and i_{arr} are reduced to zero gradually. In other words, the energy in L_{dc} is gradually exhausted by the arrester. At t = 0.0379s, the residual energy in L_{dc} is totally consumed. Hereafter, the DC source is isolated from the faulted circuit once the two S_2 are opened.

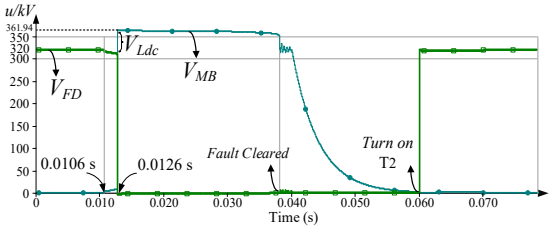


Fig. 5. Voltage waveforms during a pole-to-ground fault.

Fig. 5 shows the voltage waveforms during the fault blocking process. At t = 0.0126s, the voltage of freewheeling diodes group V_{FD} drops to zero. V_{MB} equals to the sum of DC voltage and the voltage of L_{dc} (361.94 kV). After tripping S_2, the energy stored in C_Q will then be exhausted by R_Q gradually.

The post-fault restoration begins at t = 0.05 s. At the time of 0.06s, the S_2 is firstly closed. The T_2 will be turned on once S_2 is fully closed. Then, the currents i_{Ldc} and i_{MB} are recovered to 2 kA as shown in Fig. 4. Meanwhile, V_{FD} is almost recovered to DC voltage because of R_Q<<R_D. Note that the switching of T_2 implements the ZVS and the switching of S_2 implements the zero current switching (ZCS). The triggering signal of S_1 is given at the time of 0.07 s. As the load current is flowing through the MBs, S_1 can be turned on under the ZCS as well. After two milliseconds, the load current will flow through NCCB by turning on T_1.

B. *Pole-to-pole fault*

Compared with the pole-to-ground fault, the pole-to-pole fault is relative severe. The pole-to-pole fault protection can be implemented by installing two DB-HCBs in the positive and negative lines, as shown in Fig. 6. Note that the directions of the diodes in EBD and the IGBTs in MB of the two DB-HCBs are opposite due to the opposite current directions.

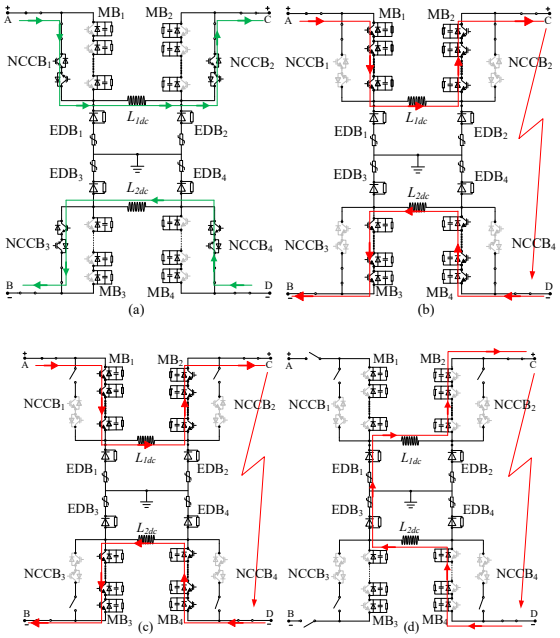


Fig. 6. Topology and interruption principles of protecting a pole-to-pole fault.

Fig. 6(a) shows the load current paths under system normal operation. Two arms are activated simultaneously once a pole-to-pole fault is detected. The operational sequences of the pole-to-pole protection are similar with the pole-to-ground fault protection, as shown in Fig. 6(b)-(d). The fault current will be exhausted by the surge arresters.

The pole-to-pole fault occurs at t = 0.01 s. The fault current is increased to 4 kA from 0.010 s to 0.0106 s. At the time of 0.0106 s, the fault current is commutated from the NCCB to the MB, as shown in Fig. 6(b). After two milliseconds, as shown in Fig. 6(c), the UFDs in NCCBs are fully opened. Hereafter, the fault energy is exhausted by arresters by turning off MBs, as shown in Fig. 6(d).

Fig. 7 shows the currents in MB_1 and MB_4. It can be seen that there always exist the fault current in MB_4 until the fault is fully eliminated. However, the fault current in MB_1 is immediately interrupted after the IGBTs in MB_1 are switched off. At the time of 0.0126s, the current flows through the EDB_1 and EDB_3 once the IGBTs in MB_1 and MB_4 are turned off. Fig. 8 shows the voltage transition stages of MB_3 and the freewheeling diode group in EBD_3. It can be seen that the fault is eliminated at the time of 0.0379s.

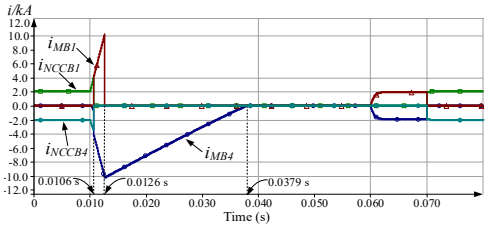


Fig. 7. Current waveforms during a pole-to-pole fault.

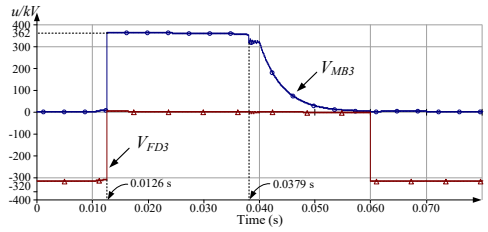


Fig. 8. Voltage waveforms during a pole-to-pole fault.

VI. Conclusions

This paper proposes a dual-bridge hybrid DC circuit breaker for the protection of MTDC girds. The operation principle of the proposed DB-HCB for protecting both pole-to-ground and pole-to-pole faults is presented. Simulation verification is performed in PSCAD/EMTDC to validate the effectiveness of the proposed DB-HCB. The studies show that the proposed DB-HCB can obviously reduce the capacity and volume of the surge arrester as well as maintain the energy dissipating capability. Therefore, the capital cost and volume of the proposed DB-HCB can be significantly reduced. Moreover, the DB-HCB is able to quickly isolate the converter from the faulted circuit in the help of the series-connected freewheeling diodes. ZVS can be implemented during the post-fault restoration processes and therefore, so that the operation safety and efficiency of the DB-HCB can be improved and result in a long lifetime. In addition, different MBs can be applied in the proposed DB-HCB with preserving its advantages, so as to increase the flexibility of the proposed topology.

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