Aalborg Universitet

AALBORG UNIVERSITY
DENMARK

Elastic Half-Space Theory-Based Distributed-Press-Pack Packaging Technology for Power Module with Balanced Thermal Stress

Chang, Yao; Li, Chengmin; Luo, Haoze; Li, Wuhua; Iannuzzo, Francesco; He, Xiangning

Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.2990208

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Chang, Y., Li, C., Luo, H., Li, W., Iannuzzo, F., & He, X. (2021). Elastic Half-Space Theory-Based Distributed-Press-Pack Packaging Technology for Power Module with Balanced Thermal Stress. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *9*(4), 3892-3903. Article 9078066. https://doi.org/10.1109/JESTPE.2020.2990208

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

Take down policy
If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

Elastic Half-Space Theory based Distributed-Press-Pack Packaging Technology for Power Module with Balanced Thermal Stress

Yao Chang, Chengmin Li, *Student Member*, *IEEE*, Haoze Luo, *Member*, *IEEE*, Wuhua Li, *Member*, *IEEE*, Francesco Iannuzzo, *Senior Member*, *IEEE*, Xiangning He, *Fellow*, *IEEE*

***Abstract* – In this paper, the distributed-press-pack (DPP) packaging technology is developed to achieve balanced thermal stress on the chips. Under the current lumped-press-pack (LPP) style, the mechanical stress distribution on the chips, which is inherently uneven and coupled with thermal stress distribution, can be described with elastic half-space theoretical model. By decentralizing the lumped pressing load and positioning the loads evenly, a matrix of clamping array is formulated and the mechanical stress distribution is compared under different clamping ways. Then, a 3*3 clamping method that meets the trade-off between balanced stress distribution and the packaging cost is chosen. Meanwhile, the busbar and heatsinks are integrated to improve the power density of the power module. Finally, a DPP prototype is implemented. By varying the pressure around the chips and heating them, the thermal distribution between parallel chips inside the prototype is compared and the effect of proposed elastic half-space theory based DPP packaging technology on the thermal stress balance is verified.**

I. Introduction

The press-pack packaging technology is configured with double-sided cooling structure and direct pressure contact between semiconductor chips and material electrodes, which enables more efficient thermal dissipation performance and avoids failure modes such as bonding wire lift-off and solder joint crack [1-4]. Hence the press-pack power modules are featured by higher operation reliability and thermal cycling capability, which makes them more competitive in high power applications such as high-voltage direct current (HVDC) transmission system [5-8].

Currently, commercial press-pack power modules are categorized into two kinds of packaging styles: the cuboid StakPak module [9] and cylinder modules such as press-pack IGBT from Westcode or IEGT from Toshiba [10-11]. Both kinds of press-pack power modules are clamped with the lumped-press-pack (LPP) packaging technology.

From the mechanical point of view, the state-of-the-art LPP power stack is composed of pressing components and pressed module stack as shown in [12, Page 5] and [13, Page 1]. The pressing component includes the insulator board that acts as force spreader and the pressing load that is usually made up of disc springs or pressing plate. The way of clamping force is ensured to be perpendicular to the module stack which is made up of the sandwich-like pressed heatsinks and modules. The gate driver is connected at the stack lateral side to control the power module. Meanwhile the rods and nuts are fastened around the stack to maintain the pressure.

However, the lumped pressure contact will lead to uneven pressure distribution among the chips. In [14, Fig. 15] and [15, Fig. 17], the pressure distribution inside StakPak and cylinder press-pack modules was analyzed and measured with Prescale film. It is concluded that the pressed chips on the edge of the power module tend to bear less stress compared with the chips close to the center. Furthermore, with the decrease of the pressure on the chip, the thermal contact resistance rises up [16-17]. It was reported that the junction temperature of the chips located at the edge or corner of the module is higher than those close to the center and the temperature gap is more than 10 degrees [18]. Therefore, with the increase of the power rating of the high power module, the influence of LPP packaging structure on the thermal distribution inside the power modules can be severe.

To address the unbalanced thermal distribution inside the LPP power module, the mechanical stress on the chips needs to be analyzed accurately and balanced. The elastic half-space theory [19] can be applied to describe the mechanical stress distribution on the contact surface of the power module. Then a distributed-press-pack (DPP) packaging technology is proposed. The DPP power module enables pressing loads to be positioned around the pressed chips evenly. Moreover, the integration level is enhanced because pressing components, heatsinks and busbar are integrated into the packaging structure. Since different clamping methods are generated by distributing pressing components according to different arrays around the pressed chips, a matrix of clamping method is formulated and the performance of the various clamping

This work is sponsored by the National Nature Science Foundations of China (51925702, 51677166) and the National Key Research and Development Program of China (2017YFE0112400) (*Corresponding author: Haoze Luo*).

Yao Chang, Chengmin Li, Wuhua Li, and Xiangning He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: cy_pe@zju.edu.cn, lichengmin@zju.edu.cn, woohualee@zju.edu.cn and hxn@zju.edu.cn).

Haoze Luo is with the College of Electrical Engineering, and also with the ZJU-Hangzhou Global Scientific and Technological Innovation Center, Hangzhou, Zhejiang University, China (e-mail: haozeluo@zju.edu.cn).

Francesco Iannuzzo is with the Department of Energy Technology, Aalborg University, 9220 Aalborg East, Denmark (e-mail: fia@et.aau.dk).

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

methods is compared by calculating the maximum and minimum mechanical stress on the contact surface. An optimal clamping solution is offered to obtain a uniform mechanical and thermal stress distribution.

This paper is organized as follows. In Section II, the limit of LPP power module is investigated and the unbalanced stress distribution under LPP packaging technology is analyzed. In Section III, the DPP packaging solution is proposed and the performance of various DPP-based clamping methods is compared. Section IV presents the case study based on the DPP packaging technology and a SiC full-bridge prototype is assembled. The thermal experiments are conducted to verify the feasibility of DPP packaging technology in Section V. Finally, Section VI draws the conclusion.

II. Configuration of LPP Packaging Technology

A. Challenges to mechanical structure of LPP power stack

According to [20], the diameter of the force spreader should be equal to that of power device and the thickness of the force spreader should be half of its diameter. With the increase of diameter and thickness, the fastening rods have to be placed further away from the center of power devices and the fastening nuts have to be assembled higher than the power devices. Hence, the uniform stress distribution on the device surface becomes more difficult to achieve since it is hard to adjust the position and torque of fastening rods and nuts. And the whole mechanical structure design is inevitably bulky and complex. Moreover, the inherent distortion inside the bulky mechanical structure could be amplified during the long-term thermal cycling process, leading to inhomogeneous pressure distribution.

For other kinds of pressure contact styles, the size of disc spring, force spreader and heatsinks is small and can not meet the demand of mounting instructions [12-13, 20]. The surface of heatsinks is not flat hence the contact between heatsinks and power modules is not tight and effective. The warpage of contact electrodes of the press-pack IGBT module is produced and also leads to the uneven pressure distribution among parallel chips [21-22] which is different from the configuration in [14-15]. However, as the typical and common method to clamp the press-pack power modules in high power converter applications, the LPP packaging technology is chosen and the mechanical stress distribution is investigated in this paper.

B. Unbalanced stress distribution with lumped pressing load

Without losing generality, the Westcode press-pack IGBT module T2960BB45E is chosen as a study target. The typical dimensions (diameter * thickness) are around 170 mm * 26 mm and the force mounted by disc springs needs to be at least 75 kN [23]. The press-pack power stack with this IGBT module is designed according to [13] and presented in Fig. 1.

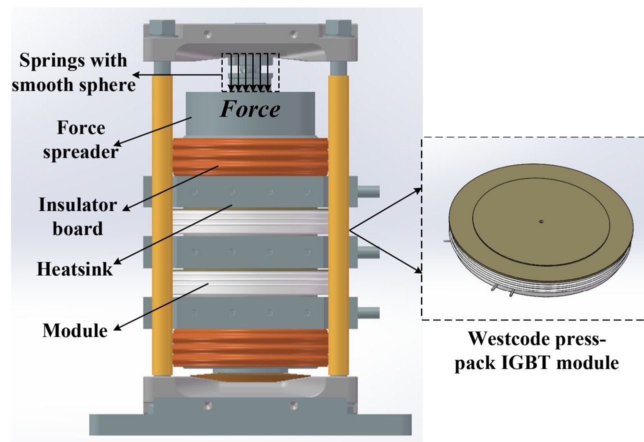
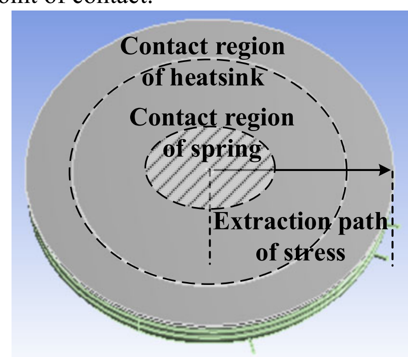


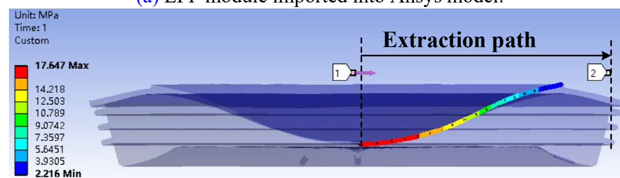
Fig. 1. Typical press-pack power stack.

The diameter of the disc springs is set to be 50 mm and the thickness of the force spreader is half of the diameter of the power module which is 85 mm. The insulator board is nearly the same size of power module while size of heatsink is 200 mm * 200 mm * 30 mm. With LPP packaging technology, the tight and effective pressure contact enables an isotropic structure with a flat contact plane. The clamping force F is mounted through the pressing disc whose size is usually much smaller than the module stack and the way of force is perpendicular due to the smooth sphere.

To analyze the mechanical stress distribution on the power module, the 3D power stack is imported into Ansys model and is simulated with finite element method (FEM). The simulation result when the force is set as 75 kN is displayed in Fig. 2. The contact region of heatsink acts as boundary condition and the contact region of spring corresponds to the force of spring in Fig. 1. It is exhibited the contact stress within the pressed solid is highly concentrated close to the contact region and decay sharply in magnitude with distance from the point of contact.



(a) LPP module imported into Ansys model.



(b) Stress extracted along the path.

Fig. 2. Unbalanced Stress distribution on LPP module.

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

C. Stress distribution model with elastic half-space theory

The elastic half-space theory is applied when a pressing load is exerted on the surface of the elastic solid which is isotropic. Since the pressed solid is elastic and semi-infinite, it behaves like the elastic half-space and the corresponding approach is called as elastic half-space theory. It is utilized to describe the contact stress distribution below the contact surface of the pressed half-space.

Since the modular unit, which includes the pressing load, force spreader, insulator board, heatsink and power module of LPP power stack, is elastic and isotropic. The pressed spring is rather small and the modular unit is seen as semi-infinite. Within the LPP power stack, the needed pressure on the press-pack power module is in the range of 10~20 MPa [24] and is much less than the yield strength of materials in the stack such as Si, Cu, Al alloys and carbon steel. In this way, the stress on the power modules or heatsinks will be under a reasonable limit and the plastic strain is minimized. Therefore, the strain is considered as pure elastic strain and the elastic half-space theory can be applied to explain the contact stress distribution below the contact surface. By the means of analytical equations with contact mechanics, the mathematical relationship between different configurations of the pressing load and the stress map is reflected in detail. Moreover, the trade-off between accuracy and computing speed is improved.

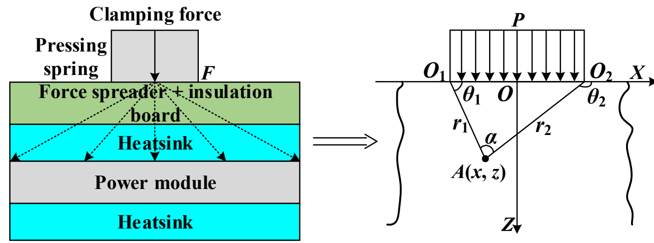


Fig. 3. Configuration of mechanical stress analyzed with elastic half-space theory.

The modular stack to be analyzed with elastic half-space theory is drawn in Fig. 3 where the contact surface is set to be *x-y* plane and the middle point of pressing spring is set as origin. The pressing load is configured as the line loading. According to the elastic half-space theory, the clamping force has two components under the line loading: the normally distributed force $p(x)$ and tangentially distributed force $q(x)$. However, the clamping force F is uniformly exerted through the pressing disc. And the housing and heatsink should be polished, cleaned and then covered with a thin film of silicone oil [20]. Hence the clamping force has only the normal component P.

The boundary of the clamping force is located at $O_{1,2}$ whose coordinates are $(\pm a, 0)$. At a random point A (x, z), the mechanical stress can be expressed in (1).

$$\begin{cases} \sigma_x = -\dfrac{P}{2\pi}[2(\theta_2-\theta_1)-(\sin 2\theta_2-\sin 2\theta_1)] & (a) \\ \sigma_z = -\dfrac{P}{2\pi}[2(\theta_2-\theta_1)+(\sin 2\theta_2-\sin 2\theta_1)] & (b) \\ \tau_{xz} = -\dfrac{P}{2\pi}(\cos 2\theta_2-\cos 2\theta_1) & (c) \end{cases} \quad (1)$$

$$\text{where } \tan\theta_{1,2} = \frac{z}{x \pm a}$$

The distance between A and $O_{1,2}$ is marked as $r_{1,2}$ while the angle $\angle AO_{1,2}X_+$ is $\theta_{1,2}$. The angle $\angle O_1AO_2$ is noted as α and it is equal to the absolute value of θ_1-θ_2. And σ_x and σ_z mean the normal stress in x and z axis respectively while τ_{xz} notes the tangential stress in y axis (which is perpendicular to *x-z* plane).

The mechanical stress is composed of normal stress and tangential stress. When the tangential stress is zero and normal stress reaches its maximum or minimum value which is called the principal stress. The principle stress of point A is expressed by (2), where σ_1 and σ_2 mean minimum and maximum direct stress respectively.

$$\sigma_{1,2} = -\frac{P}{\pi}(\alpha \mp \sin\alpha) \quad (2)$$

Therefore, mechanical stress distribution on the extraction path in Fig. 2 can be fitted with (2) and figured in Fig. 4. Furthermore, the mechanical distribution on the all contact surface can be obtained by rotating the curve in Fig. 4 along the *Z*-axis, which is shown in Fig. 5.

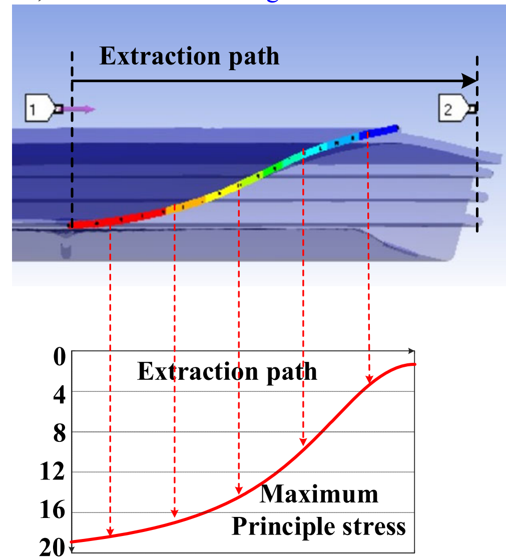


Fig. 4. Fitting curve of principal stress σ_2 with distance x on contact surface of power module.

In Fig. 5, the contact plane acts as the *x-y* plane in the 3-D coordinate system and the *Z*-axis stands for the maximum principal stress distributed on the contact surface. It is seen that the ratio of maximum value to minimum value is more than 7 and it does not change along with the value of force.

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

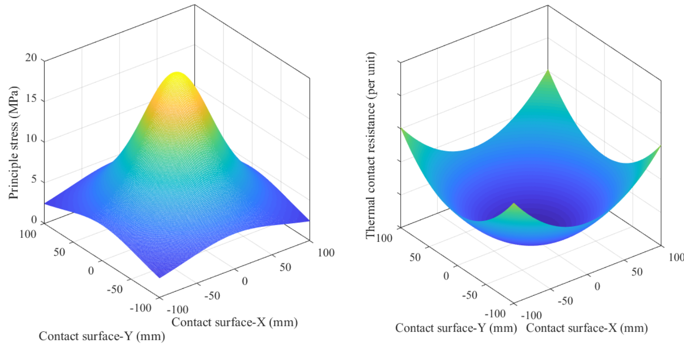


Fig. 5. Distribution of maximum principal stress σ on the contact plane.

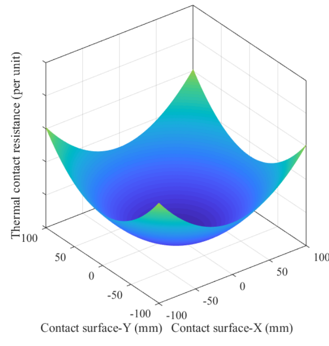


Fig. 6. Per-unit model of distribution of thermal contact resistance.

Additionally, the relationship between thermal contact resistance $R_{\text{ther_con}}$ and the principal stress, i.e. the contact pressure of the joint σ is described in (3) [25], where k_s notes the mean thermal conductivity of pressed joint, m is absolute slope of the interface, ε is the effective root mean square of surface roughness, H stands for the hardness of the softer material and A means the contact area.

$$R_{\text{ther_con}} = \frac{1}{0.125 k_s \frac{m}{\varepsilon}\left(\frac{\sigma}{H}\right)^{0.95} A} \tag{3}$$

Since the parameters k_s, m, ε, H, and A are directly determined by the contact material, the thermal contact resistance can be viewed as the function of stress σ inside the uniformly elastic solid. Hence, the per-unit model of the 3-D distribution of $R_{\text{ther_con}}$ on the contact plane inside the power stack is fitted in Fig. 6.

The distribution of thermal contact resistance is displayed in Fig. 6. Inside the LPP power stack, the maximum thermal resistance occurs at the edge of the pressed power module and is more than 10 times than the minimum thermal resistance at the center.

III. Proposed DPP Packaging Technology

A. Decentralization of pressing loads under distributed clamping method

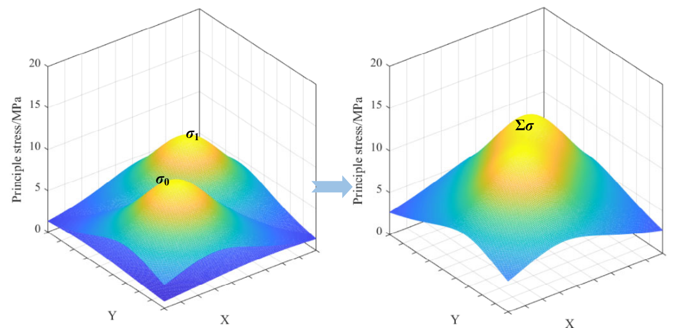
The root reason of the uneven thermal distribution inside the power module is the unbalanced mechanical stress introduced by lumped pressure contact. To this end, a novel packaging technology is proposed by decentralizing the pressing load and placing it at symmetrical locations of the contact surface. The pressure needed on the load is reduced and the requirement on the size of the load is also relieved. The distribution model obtained in Fig. 4 and Fig. 5 by traditional lumped contact method can be noted as the clamping case (1*1), which acts as the base of reconstruction of press-pack packaging technology. The function to describe the stress and the location is denoted as σ_0 (x, y, z) and it is derived in (4). Assume that the peak value of the stress is 20 MPa to ensure that the stress is within the limit.

$$\begin{gathered}
\text{In } xyz \text{ coordinate system, } \sigma = -\frac{P}{\pi}(\alpha + \sin\alpha) \\
\text{In } xy \text{ plane, let } r = \sqrt{x^2 + y^2} \\
\text{In (4), } \alpha = \arctan\left(\frac{z}{r-a}\right) - \arctan\left(\frac{z}{r+a}\right) \\
\text{substitute } r \text{ with } x \text{ and } y, \text{ yield } \sigma \triangleq \sigma_0(x,y,z)
\end{gathered} \tag{4}$$

The clamping case (1*2) is achieved by applying two pressing loads while the magnitude of the pressure drops by 2 times. Assume the center of one pressing load is applied at the original point (0, 0, 0) and the other load is applied at the point (Δx_1, Δy_1, 0). The corresponding stress generated by the load is denoted as σ_0 (x, y, z_0) and σ_1 (x_1, y_1, z_0) respectively. (x, y, z_0) and (x_1, y_1, z_0) mean the random points under the contact surface while z_0 is a constant and stands for the distance between pressing load and contact surface on the power module. The latter σ_1 (x_1, y_1, z_0) is yielded by multiplying the original function σ_0 (x, y, z_0) and the transformation matrix T. The transformation process is expressed and the transformation matrix is obtained in (5).

$$\begin{gathered}
\text{For any point } (x_1, y_1) \text{ in } \sigma_1, \text{ it satisfies} \\
\begin{bmatrix} x_1 \\ y_1 \\ 1 \end{bmatrix} = \begin{bmatrix} x + \Delta x_1 \\ y + \Delta y_1 \\ 1 \end{bmatrix} = \left(m \cdot \begin{bmatrix} 1 & 0 & \Delta x_1 \\ 0 & 1 & \Delta y_1 \\ 0 & 0 & 1 \end{bmatrix} \right) \times \begin{bmatrix} x \\ y \\ 1 \end{bmatrix} \\
\text{Let } T = m \cdot \begin{bmatrix} 1 & 0 & \Delta x_1 \\ 0 & 1 & \Delta y_1 \\ 0 & 0 & 1 \end{bmatrix} \\
\Longrightarrow \sigma_1(x_1, y_1, z_0) = T \times \sigma_0(x, y, z_0)
\end{gathered} \tag{5}$$

In (5), Δx_1 and Δy_1 denote the distance between the original pressing load and another pressing load along the X-axis and Y-axis. Meanwhile m is the magnification what is equal to $|\sigma_1|$ divided by $|\sigma_0|$. When applying the clamping case (1*2), the ratio m is set to be 0.5 and the resultant stress $\Sigma\sigma$ is the sum of two stress components, which means the $\Sigma\sigma$ (x, y, z) is the superposition of function σ_1 and σ_0 in the unified x-y-z coordinates system. Since the value of Z-coordinate is constant and marked as z_0, $\Sigma\sigma$ (x, y, z) can be simplified as $\Sigma\sigma$ (x, y).



(a) Discrete stress components (b) Resultant stress after superposition

Fig. 7. Configuration of distributed clamping case (1*2).

The stress components before superposition are presented in Fig. 7(a) and the resultant stress is shown in Fig. 7(b). It can be seen that despite the two pressing loads are applied, the

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

unbalanced distribution has not been improved a lot. The minimum value is still about 5 times less than the maximum value. To improve the distribution of resultant stress, the clamping array can be extended. Different clamping arrays form the different clamping cases and they can be distinguished by the matrices denoting the clamping arrays. Under the same contact surface which acts as *XY*-plane in Fig. 5, the different configurations of clamping cases are illustrated in Fig. 8.

To make the most use of the area at the contact region and save the number of the pressing loads at the same time, the clamping cases 2*2, 3*3, 4*4 are configured of which the pressing loads are located at the corner, edge and the center of the contact region. In addition, the clamping force under these clamping cases keeps unchanged and for every clamping case the clamping force is shared uniformly by the pressing loads.

The clamping case (2*2) and the corresponding transformation process is expressed as (6).

$$\begin{gathered}
\sigma_{2*2}=\sum_{i=0}^{3}\sigma_i(x,y)=\sum_{i=0}^{3}T_i\times\sigma_0(x,y) \\
T_i=m_i\cdot\begin{bmatrix}1&0&\Delta x_i\\0&1&\Delta y_i\\0&0&1\end{bmatrix} \\
m_i=\frac{1}{4}(i=0,1,2,3) \\
\Delta x_0=\Delta y_0=0,\ \Delta x_1=\Delta y_1=\delta_{2*2} \\
\Delta x_2=0,\ \Delta y_3=\delta_{2*2},\ \Delta x_4=\delta_{2*2},\ \Delta y_4=0
\end{gathered} \tag{6}$$

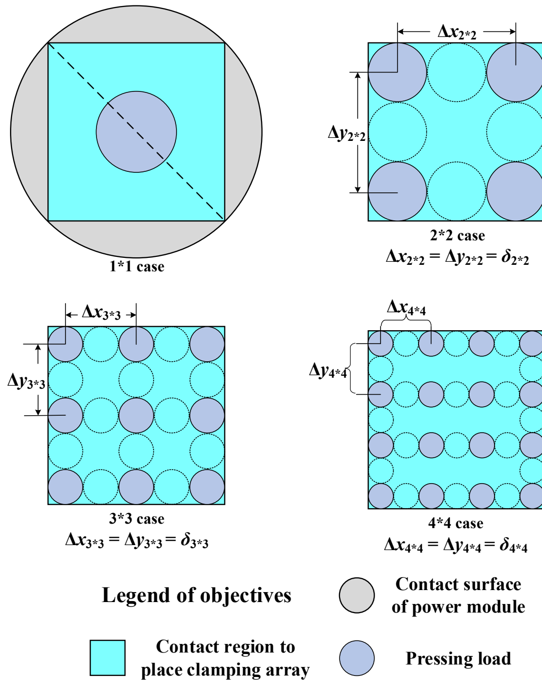
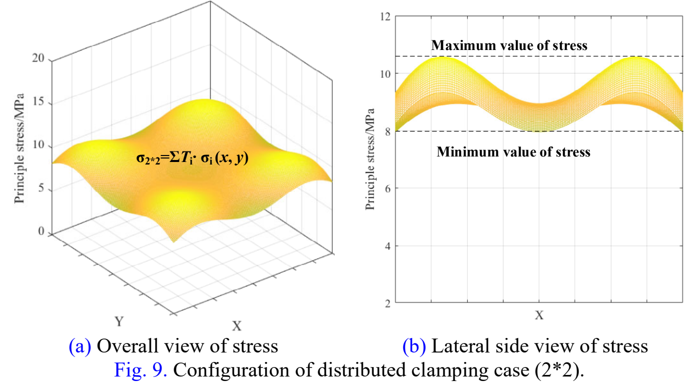


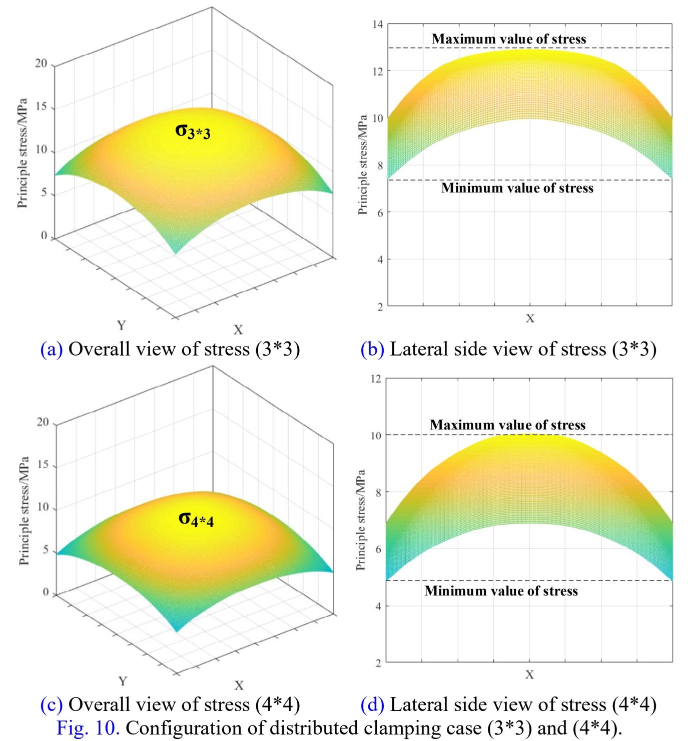
Fig. 8. Geometry configuration of different clamping cases.

Let m_i (i=0, 1, 2, 3) be 0.25 and $|\Delta x_i| = |\Delta y_i| = \delta_{2*2}$. In this way, the resultant stress after applying the clamping case (2*2) is displayed as Fig. 9.

Due to the increase in the number and the symmetrical layout of pressing loads, mechanical stress becomes more uniform. The maximum value is about 1.3 times larger than the minimum value which indicates that the unbalance degree of mechanical stress distribution is reduced.



(a) Overall view of stress (b) Lateral side view of stress
Fig. 9. Configuration of distributed clamping case (2*2).



(a) Overall view of stress (3*3) (b) Lateral side view of stress (3*3)
(c) Overall view of stress (4*4) (d) Lateral side view of stress (4*4)
Fig. 10. Configuration of distributed clamping case (3*3) and (4*4).

The resultant stress of clamping cases (3*3, 4*4) are given in Fig. 10 respectively. In Fig. 10 it is observed that the gap between the minimum value and the maximum value is optimized compared with that in Fig. 5 and Fig. 7. As for the clamping case (3*3), the maximum value is about 1.6 times higher than the minimum. Moreover, the effects of balancing the stress distribution by clamping case (4*4) are not much better than the clamping case (3*3). The maximum stress by clamping case (4*4) is more than 2 times higher than the minimum.

In Table I, the performance of different clamping cases (*X***Y*) is compared. The ratio of maximum stress to minimum stress is listed. It indicates that under the same total pressure

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

and the same contact surface, the mechanical stress distribution becomes more even with the increase of distributed pressing loads. However, despite clamping case (4*4) utilizes more pressing loads, the balanced degree is not as good as the clamping case (3*3), which indicates that the effect of distributed clamping methods on the balanced mechanical distribution is approaching saturation. Under the same clamping force in total, the clamping case 3*3 rather than clamping case 2*2 can meet the requirement of tight and optimal contact in the range of 10 MPa and 20 MPa [24]. It is exhibited that the clamping case (3*3) is the best solution among them which can not only meet the demand of clamping pressure but also ensure balanced stress distribution. Besides, the number and the cost of the pressing loads are within a reasonable range.

TABLE I. Comparison of performance of different clamping case (*X***Y*).

Clamping case (X*Y)	Ratio of maximum stress to minimum stress $\sigma_{max}/\sigma_{min}$
(1*1)	7.5
(2*2)	1.3
(3*3)	1.6
(4*4)	2.0

B. Integration of distributed pressing loads and busbar

The clamping case (3*3) utilizes 9 pressing loads of which the total clamping force is equal to that in the clamping case (1*1). Despite the number of pressing loads increases, the size of the pressing loads is reduced and the loads are relatively easy to control compared with clamping case (4*4) or more. The structure of the power stack with distributed pressing loads based on Fig. 3 is reconstructed in Fig. 11.

Despite the distributed pressing loads are able to achieve even mechanical stress among parallel chips inside the power module, the sandwich-like structure of the press-pack power stack still results in complex design. To save the cost and volume of the press-pack power stack, the distributed pressing loads are integrated inside the stack and maintain the clamping force by fastening them. Hence the force spreader can be removed and the reconstructed power stack is given in Fig. 12.

The configuration in Fig. 12 promises a high power density packaging design with uniform stress on the parallel chips because the structure of pressing components is simplified by removing the pressing shaft and disc springs and using fastening bolts or screws to maintain the pressure. A torque spanner can be used to control the fastening torque on each fastening bolt. On each bolt, the torque can be applied according to the mechanical requirement and guarantee the balanced pressure.

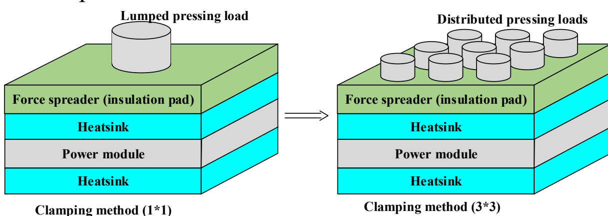


Fig. 11. Reconstruction of clamping method with distributed pressing loads.

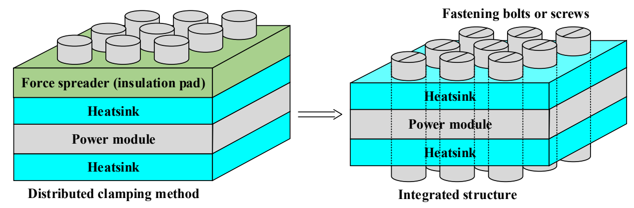


Fig. 12. Distributed pressing loads integrated inside power stack.

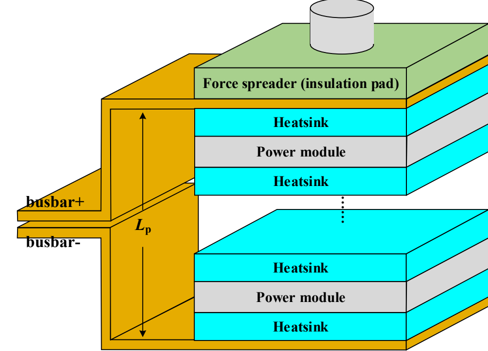


Fig. 13. Configuration of busbar connection to lumped-press-pack power stack.

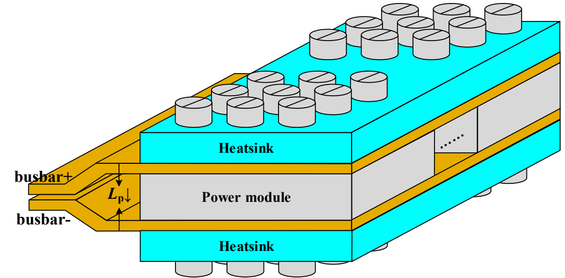


Fig. 14. Integration of pressing components and busbar in proposed distributed-press-pack power stack.

What is more, the busbar connection between the power stack and DC-link capacitors has to be adjusted to adapt the distributed-press-pack packaging design. For the lumped-press-pack power stack as drawn in Fig. 13, the positive and negative electrodes of the busbar are connected to the top and bottom side of the power stack and the parasitic inductance of busbar reaches inevitably up to 200~500 nH [26-27].

To reduce the voltage overshoot in conjunction with the switching losses caused by high parasitic inductance, a 3D inductor-integrated concept [28-30] is adopted to realize low-inductive structure design. In stead of lumped-press-pack power stack, the busbar are integrated into the distributed-press-pack power stack as the positive and the negative side of the busbar are inserted between the heatsinks and power module in Fig. 14, which makes it easier to apply a laminated busbar. With the increase of stacked chips in parallel, the distance between positive and negative electrodes remains the same whilst the width of busbar becomes higher. Therefore, the parasitic inductance of the busbar gets lower. The integration design with the distributed pressing components and the busbar forms the DPP packaging method.

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

IV. A CASE STUDY

Without losing generality, the SiC diode chip (VS-H2257H12A6x) is chosen as the pressed chip. Since the shape of the chip is square, the contact region is set to be square. Due to the geometric similarity, the clamping cases in Fig. 8 can be applied in the square contact region whose size is smaller. In this way around the chip the distributed clamping method (3*3) is applied. The pressing loads are realized by the bolts which are placed evenly around the chip. The bolts will get through the heatsinks and the copper pads that act as the busbar. The basic part composed of pressed chip and the surrounding bolts in Fig. 15 is configured as the chip unit. By applying and controlling the torque on the bolts, the heatsinks and Cu pads are fastened to press the chip tightly. In this way, a more compact sandwiched press-pack structure is formed and the contact mechanics theory is still suitable in this structure.

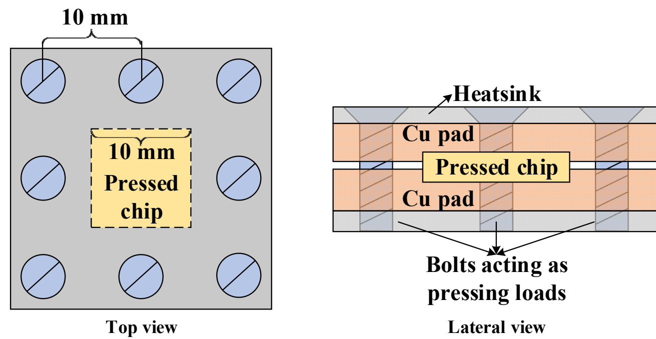
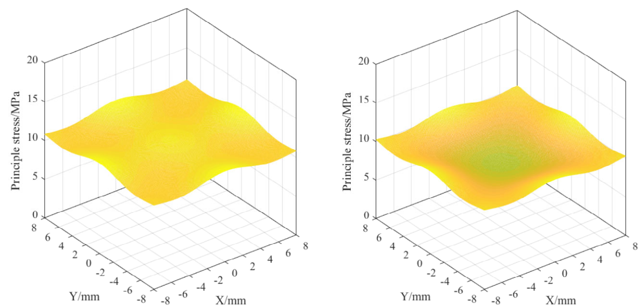


Fig. 15. Configuration of chip unit with distributed clamping method.



(a) Stress distribution of customized clamping method (3*3) with 9 bolts

(b) Stress distribution of customized clamping method with 8 bolts

Fig. 16. Comparison of stress distribution between clamping method (3*3) with 9 bolts and 8 bolts.

However, since the size of the pressed chip is small and the bolts need to be customized and pass through the heatsinks and Cu pads, the bolt in the center of the 3*3 array when applying the distributed clamping method has to be removed. The comparison of the stress distribution produced by the original clamping method (3*3) and customized clamping configuration in Fig. 15 is given in Fig. 16, in which the size parameters of the pressed chip are taken into account. The thickness of heatsinks and Cu pads are set to be 4 mm and 1 mm respectively and the bolts are configured as M5. In Fig. 16 it can be found that despite the middle pressing load is eliminated, the stress distribution is not much affected. Therefore, the modified clamping method (3*3) with 8 bolts can be applied in the structure of the chip unit.

Based on the modified clamping method, the DPP power module can be implemented with the chip units in parallel. The two parallel chip units clamped with 13 bolts are shown in Fig. 17. The stress distribution on the two pressed chips is given in Fig. 18. It can be seen that not only the stress distribution on the one pressed chip is balanced but the two pressed chips in parallel share the even stress distribution. Even if the number of parallel chips becomes higher, the stress distribution among the pressed chips will still remain uniform.

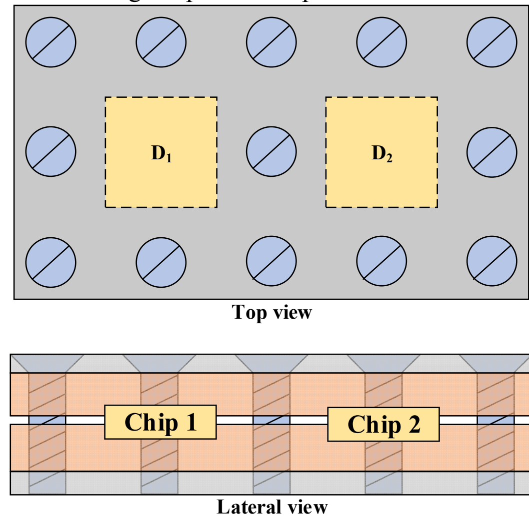
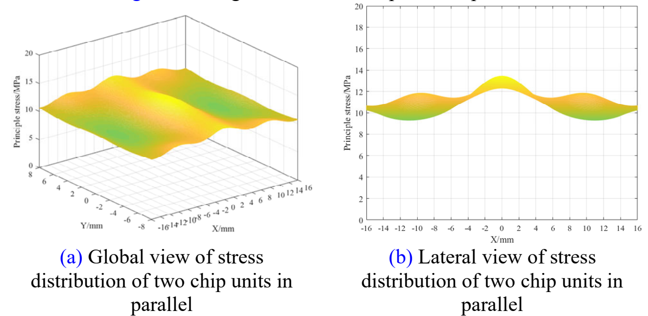


Fig. 17. Configuration of two chip units in parallel.



(a) Global view of stress distribution of two chip units in parallel

(b) Lateral view of stress distribution of two chip units in parallel

Fig. 18. Stress distribution of two parallel chip units.

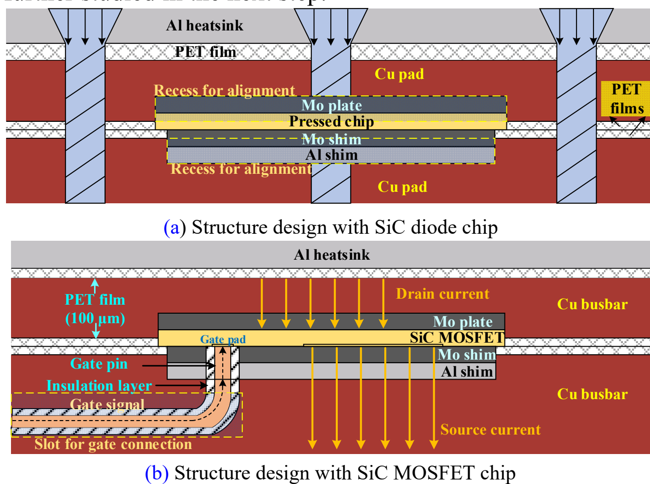
More in detail, the profile of the distributed-press-pack chip unit is displayed in Fig. 19. To ensure the tight pressure contact, the pressed chip is in contact with other metal layers such as molybdenum (Mo) plate and aluminum (Al) shim, which are helpful to match the coefficient of thermal expansion (CTE) between Cu pads and the semiconductor chip. The flat 100-micrometer-thick polyethylene terephthalate (PET) layer provided by Mylar® of DuPont Teijin Films which is thermally stable [31] is filled inside the space between different Cu pads. On the contacting surface of the Cu pads and the chip unit, the recess is made for the alignment of the chip unit. The copper pads which are directly clamped with the chips and conduct the current act as the DC busbar and AC terminals.

As for three terminals' SiC MOSFET chip, the structure design with gate connection is illustrated in Fig. 19(b) (SiC

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

MOSFET CPM2-1200-0080B is taken as an example). The gate pad is close to the source pad and they are on the same surface of the chip, while the drain pad is on the back surface. To connect the gate pad and avoid the short-circuit between gate and source pad, a slot is made inside the busbar and the insulation layer is covered on the surface of the slot. A gate pin made up of copper can be configure as the route to the gate pad with the copper inside the slot. To embed the gate slot inside the busbar and make sure the gate pin correctly contacts the gate pad, a higher demand is put forward on the fabrication technology of busbar with gate connection. The printed contact solution that prints and curves a gate trace on the busbar may be applied [32], but it makes the mechanical structure more expensive to assemble. Since this study mainly focuses on the power module with cost-effective and thermally balanced packaging technology, the gate connection structure which is shown in Fig. 19(b) and does not affect the related positions of pressed components which include Mo plate, chip, Mo shim, Al shim and Cu busbar inside proposed packaging style and only increases the cost and difficulty of the assembly, the SiC diode chips are used to achieve a simple prototype to verify the feasibility of proposed packaging technology and the prototype with SiC MOSFET will be further studied in the next step.



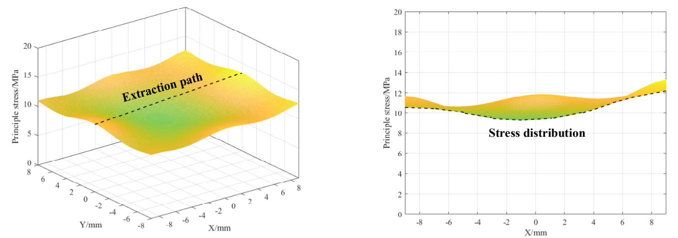
(a) Structure design with SiC diode chip

(b) Structure design with SiC MOSFET chip

Fig. 19. Detailed profile of distributed-press-pack chip unit.

Since the size of chip in high press-pack power module is usually large, the diode chip VS-H2257H12A6x (10 mm * 10 mm) whose size is as large as possible is chosen. However, to balance the pressure on the chips in parallel, the bolts have to placed around the chips. Hence the power density of the power module is inevitably sacrificed to ensure the stress uniformity. To reach a good trade-off between the size and the pressure distribution, the bolt which are made up of polyether-ether-ketone (PEEK) is customized. PEEK bolt has high enough isolation capability to withstand the high voltage for the press-pack power module. The compressive strength of PEEK is also much higher than the needed pressure on the chip [25, 33].

The stress distributed on the single chip is analyzed as exhibited in Fig. 20. Despite the stress on the edge of a single chip is higher than that in the center, the stress ratio extracted through the path is within 1.5. Hence, if the size of fastening parts is customized and close to the size of pressed chip, the stress distribution on the single chip can also be balanced. This is helpful to analyze the pressure distribution on other kinds of press-pack chip.



(a) Global view of stress distribution on single chip

(b) Lateral view of stress distribution on single chip

Fig. 20. Stress distribution on single chip.

Combine 4 chip units together and the full-bridge power module is formed. The prototype of the full-bridge power module with distributed-press-pack packaging technology is implemented based on the process flow in Fig. 21, which is stated as follows:

Step 1: Clean the surfaces of PET film, copper bars and heatsinks with ethanol at the beginning. Cut the PET film and put the PET film under the Al heatsink.

Step 2: Mount the DC- busbar and align the chip units on the recesses of the busbar.

Step 3: Add another PET layer and put the two AC terminals. Mount the chips and other shims on the recesses.

Step 4: Mount the DC+ busbar and another heatsink.

Step 5: Apply the bolts made up of polyether-ether-ketone (PEEK).

Step 6: Fasten the bolts and the prototype is finished.

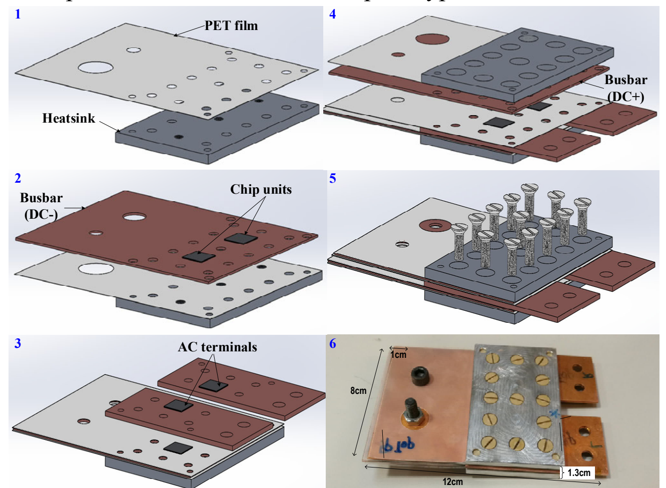


Fig. 21. Assembly process of distributed-press-pack power module.

Compared to the lumped-press-pack power stack, the 13 PEEK bolts inside the distributed-press-pack power module enables the balanced stress distributed on the two parallel half-bridge units, and the outer pressing components are removed to simplify the mechanical design. Meanwhile, the heatsinks and busbars have been integrated together as part of the power

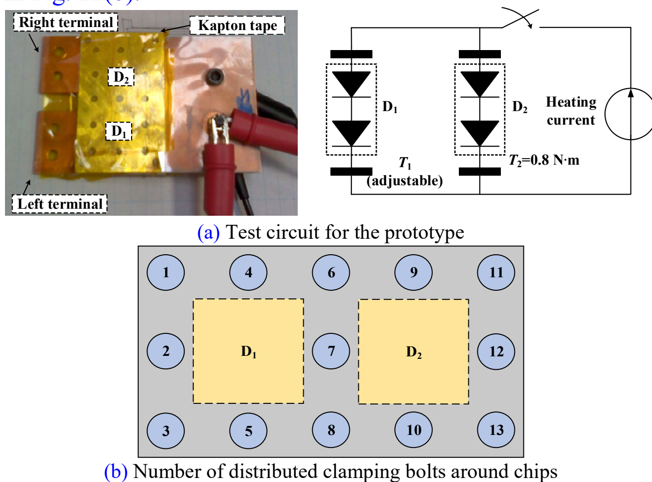
2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

module, which inherently reduces the parasitic inductance of the whole power loop and thermal impedance from the junction of the chip to the ambient. And the feature of double-sided cooling structure in the lumped-press-pack power stack is still maintained, which inherently improves the thermal dissipation capability of the prototype together with the integrated heatsink structure. Since the proposed DPP packaging technology is aimed at balancing the mechanical and thermal stress distribution among pressed chips, the Al cooling plate is chosen as the heatsink to realize passive cooling by natural air cooling condition.

V. EXPERIMENTAL EVALUATION OF DPP PACKAGING TECHNOLOGY

Despite the pressure analysis with Fuji Prescale film can be conducted to study the mechanical stress distribution, the film can only reflect the variation trend but not the exact parameters. Because the thermal stress distribution is negatively correlated with the mechanical stress distribution according to [16-18, 25] and the thermal behavior is easier to be measured accurately inside a highly integrated power module than the mechanical behavior, the thermal stress distribution which has the main effect on the reliability of the power module is measured. To investigate the effects of different pressure on the thermal performance of the power module and validate the balanced mechanical and thermal distribution of parallel chips, the steady-state thermal tests are conducted by adjusting the torque value of the bolts. The configuration of the prototype under the test is photographed in Fig. 22(a) and the equivalent test circuit is displayed. Besides, the bolts of the prototype are numbered and marked in Fig. 22(b).



(a) Test circuit for the prototype

(b) Number of distributed clamping bolts around chips

Fig. 22. Prototype under steady-state thermal test of pressure imbalance.

The thermal distribution of the prototype is monitored by the IR camera. To avoid insufficient emission of metal materials, the Kapton tape provided by DuPont is covered smoothly and uniformly on the surface of the heatsinks and the Cu terminals to obtain the correct measurement results by the IR camera. The Kapton tape is thermally stable and can withstand temperature as high as 260 °C. On the surfaces of heatsinks and Cu terminals, the tape is covered uniformly and smoothly. As a result, the thermal resistance of heatsink's surface to the ambient which includes the thermal resistance of the Kapton layer is evenly distributed on the heatsink's surface. With the other factors controlled equally, the thermal stress comparison between pressed chips in parallel is only affected by the mechanical pressure contact of every chip. Hence the thermal resistance of the Kapton layer is not considered in this paper and the thermal stress distribution of parallel chips determined by mechanical pressure contact is the main issue.

The diodes are pressed between the DC busbar and AC terminals, so the temperature of diodes is not easy to observe directly. Both the temperature of DC busbar and AC terminals can be measured with an IR camera. However, the heatsink and PET film covering the DC busbar cause some inconvenience to the measurement. Besides, the DC busbar has to be connected to the DC-link capacitor as Fig. 24 shows while the length beyond the heatsink is inevitably large, leading to some potential errors of measurement. Since the length of the AC terminal beyond heatsink is not much and the temperature of that is easy to measure, the junction temperature of the chips can be viewed as equal to the temperature of the corresponding terminals.

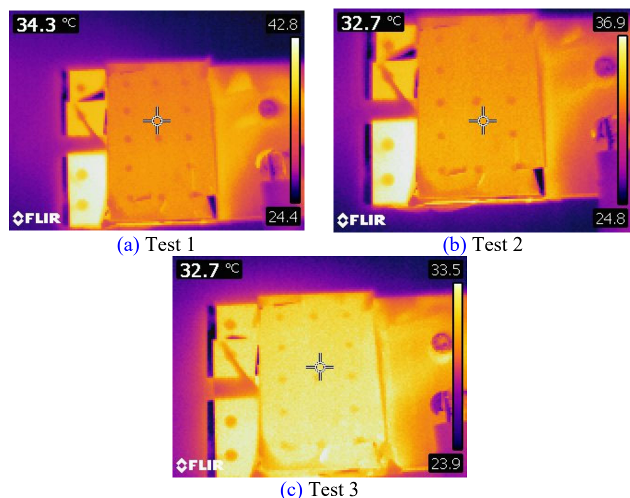
In Fig. 22(a), it is noted that the temperature of the left terminal and right terminal is viewed as the junction temperature of D_1 and D_2 respectively. The two electrodes of the busbar are connected to the DC current source to heat the whole prototype. The torque of the bolts can be adjusted to cause the pressure imbalance. According to [35], the maximum torsional value of M5 PEEK bolt is 1.28 N·m. To ensure a safe and tight press, the torque on bolts from 1 to 7 in Fig. 22(b) is fixed as 0.8 N·m while the torque on bolts from 8 to 13 is set as 0 initially, which means these bolts are not clamped at the beginning. By changing the torque value of the bolts from 8 to 13, different kinds of test configuration can be realized and the parameters of test configuration are listed in Table II. The prototype is located where the ambient temperature is controlled at 25 °C and there are no cooling fans around, making sure the cooling condition has no effect on the thermal distribution between the chips. The temperature distribution is photographed by the IR camera and the results of the three test configurations are presented in Fig. 23. The temperature difference of the three test configurations is compared in Fig. 24.

TABLE II. Parameters for different test configurations.

Test configuration	Test 1	Test 2	Test 3
Total heating power	15 W		
Thermal dissipation condition	Natural air cooling without cooling fans around		
Initial temperature	25 °C		
Ambient temperature	25 °C		
Torque of bolts around D_1 (1~7)	0.0 N·m	0.4 N·m	0.8 N·m
Torque of bolts around D_2 (8~13)	0.8 N·m		

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics



(a) Test 1 (b) Test 2

(c) Test 3

Fig. 23. Thermal distribution of prototype under different pressure configuration.

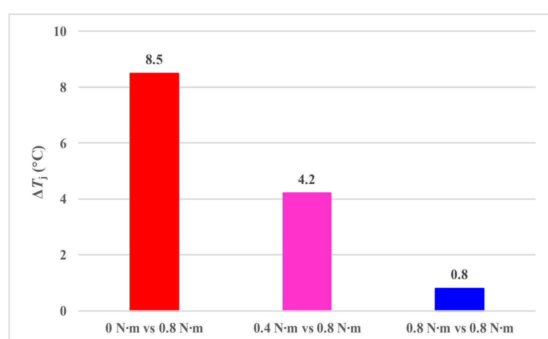


Fig. 24. Temperature difference between D_1 and D_2 under different test conditions.

It can be inferred that with the increase of pressure on the chip, the temperature rise will drop. When the bolts around the chip unit D_1 get loose, the temperature of the left terminal, which is equally viewed as the junction temperature of chip unit D_1 will rise up to become the maximum temperature in the IR camera. When the torque of the bolts around the D_1 is 0 and the temperature gap between D_1 is D_2 is about 8.5 °C. Then the temperature gap decreases to 4.2 °C when the value of torque is adjusted to 0.4 N·m. Despite the PEEK bolts have a CTE of 46.8 ppm and the expansion would be 61 μm under a 100 °C temperature swing, the temperature distribution of the prototype will be still uniform if all the bolts are produced with standard manufacturing process and clamped with the same torque. The balanced mechanical and thermal stress configuration demonstrates that DPP packaging technology can improve the thermal stress balance of the parallel chips.

The thermal tests have compared the temperature difference caused by stress imbalance under a thermal steady state, which have validated the effects of mechanical stress on the thermal performance of pressed chips, as well as the feasibility of proposed DPP packaging technology which can balance the mechanical and thermal stress distribution to optimize the reliability of power modules.

VI. Conclusion

In this paper, a distributed-press-pack (DPP) packaging concept was proposed and explored. By decentralizing the pressing loads of lumped-press-pack power stack, the clamping methods were optimized to balance the mechanical stress distribution among parallel chips. Different configurations of clamping methods were compared and the optimal configuration was chosen to achieve a balanced and cost-effective packaging solution. By removing the springs and inserting the pressing bolts around the SiC chips evenly and integrating busbar and heatsinks, a distributed-press-pack structure with high integration level was realized. The proposed approach did not only adopt the advantage of ABB's and Westcode's press-pack power module but also synergized balanced mechanical and temperature distribution among chips with an improved power density level of the power module. The full-bridge prototype was implemented based on DPP packaging technology. Then the thermal experiments were conducted with three kinds of test configurations. By adjusting the torque around the chip units, the pressure imbalance was induced. Then the temperature distribution of the SiC power module was measured by IR camera. It has demonstrated that the effects of unbalanced pressure of chips on the thermal stress distribution and revealed the positive correlation between thermal resistance and mechanical stress. Furthermore, a thermally balanced press-pack packaging technology by balancing the mechanical configuration has been verified to overcome the challenge of uneven thermal distribution among current available multi-chip press-pack power modules.

Due to the limit of manufacturing techniques, the number of parallel chips can not be raised in a short period. However, the effects of proposed packaging design methodology on the stress balance has been validated by the experimental investigations and comparisons, which makes it possible to offer an alternative approach to extend the application of press-pack packaging technology. In the future the power module with more chips which takes manufacturing factors into considerations will be developed and the time-stress changing profile which is related to reliability issue in the long term will be further investigated.

References

[1] E. Deng, Z. Zhao, Q. Xin, J. Zhang, Y. Huang, "Analysis on the difference of the characteristic between high power IGBT modules and press pack IGBTs", *Microelectron. Reliab.*, vol. 78, pp. 25-37, Nov 2017.

[2] J. Feng, Y. Mei, X. Li, G. Lu, "Characterizations of a Proposed 3300-V Press-Pack IGBT Module Using Nanosilver Paste for High-Voltage Applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2245-2253, Dec. 2018.

[3] S. Kicin, M. Laitinen, C. Haederli, J. Sikanen, R. Grinberg, and et al., "Low-Voltage AC Drive Based on Double-Sided Cooled IGBT Press-Pack Modules," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2140-2146, Nov.-Dec. 2012.

[4] H. Chen, W. Cao, P. Bordignon, R. Yi, H. Zhang, and et al, "Design and testing of the World's first single-level press-pack IGBT based

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2990208, IEEE Journal of Emerging and Selected Topics in Power Electronics

submodule for MMC VSC HVDC applications," *in Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, 2015, pp. 3359-3366.

[5] R. Simpson, A. Plumpton, M. Varley, C. Tonner, P. Taylor, and et al, "Press-pack IGBTs for HVDC and FACTs," *CSEE J. Power Energy Syst.*, vol. 3, no. 3, pp. 302-310, Sept. 2017.

[6] Y. Luo, F. Xiao, B. Liu, Y. Huang, "A Physics-based Transient Electro-Thermal Model of High-Voltage Press-Pack IGBTs under HVDC Interruption," *IEEE Trans. Power Electron.*, Early Access.

[7] L. Feng, R. Gou, F. Zhuo, X. Yang, F. Zhang, "Development of a 10kV solid-state DC circuit breaker based on press-pack IGBT for VSC-HVDC system," *in Proc. IEEE 8th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Hefei, 2016, pp. 2371-2377.

[8] A. Hassanpoor, J. Häfner, B. Jacobson, "Technical Assessment of Load Commutation Switch in Hybrid HVDC Breaker," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5393-5400, Oct. 2015.

[9] M. Chen, E. Tsyplokov, R. Schnell, P. Hong, H. Wang, and et al, Power Devices for GW VSC-HVDC Application Development trend and status with StakPak. ABB Semiconductor Products Inc., Switzerland, 2016.

[10] F. Wakeman, J. Pitman, S. Steinhoff, "Long term short-circuit stability in Press-pack IGBTs," *in Proc. 18th Eur. Conf. Power Electron. Appl. (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

[11] R. Kotani, T. Nitta, N. Tsukamoto, H. Kitazawa, M. Kitagawa, and et al, "4.5 kV Rupture Resistant Press Pack IEGT," *in Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy and Energy Manage. (PCIM Europe 2018)*, Nuremberg, Germany, 2018, pp. 1-4.

[12] M. Chen, H. Wang, P. Hong, High power semiconductors for T&D and industry application StakPak & IGCT introduction. ABB Semiconductor Products Inc., Switzerland, 2014.

[13] *Power Semiconductor Assemblies, Components and Custom Solutions*, Westcode Semiconductors Ltd, [Online]. Available: http://www.westcode.com/publicity/prod_lit/pub2.pdf.

[14] T. Wei, Z. Yu, Z. Chen, X. Zhang, W. Wen, Y. Huang, and et al., "Design and test of the bidirectional solid-state switch for an 160kV/9kA hybrid DC circuit breaker," *in Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018, pp. 141-148.

[15] M. Varley, A. Plumpton, R. Simpson and C. Tonner, "Thermo-Mechanical Optimisation of Press-Pack IGBT Packaging Using Finite Element Method Simulation," *in Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy and Energy Manage. (PCIM Europe 2017)*, Nuremberg, Germany, 2017, pp. 1-8.

[16] T. Poller, S. D'Arco, M. Hernes, A. Rygg Ardal, J. Lutz, "Influence of the clamping pressure on the electrical, thermal and mechanical behaviour of press-pack IGBTs," *Microelectron. Reliab.*, vol. 53, pp. 1755-1759, 2013.

[17] E. Deng, Z. Zhao, P. Zhang, X. Luo, J. Li, and et al, "Study on the Method to Measure Thermal Contact Resistance Within Press Pack IGBTs," *IEEE Trans. Power Electron.*, vol. 34, no.2, pp. 1509-1517, Feb. 2019.

[18] W. Lai, H. Li, M. Chen, S. Kang, H. Ren, R. Yao, and et al, "Investigation on the Effects of Unbalanced Clamping Force on Multi-chip Press Pack IGBT Modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2314-2322, Dec. 2019.

[19] J. K. Langstreth, "Line loading of an elastic halfspace," in *Contact Mechanics*, Cambridge, New York, Cambridge University Press, 1985, pp. 11-44.

[20] Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors, [Online]. Available: https://www.5scomponents.com/pdf/clamping_of_press_mechanical_clamping.pdf.

[21] T. Poller, T. Basler, M. Hernes, S. D'Arco, J. Lutz, "Mechanical analysis of press-pack IGBTs", *Microelectron. Reliab.*, vol. 52, pp. 2397-2402, Sep.-Oct. 2012.

[22] E. Deng, Z. Zhao, P. Zhang, Y. Huang, Z. Lin, "Clamping Force Distribution within Press Pack IGBTs", *Trans. China Electro-tech. Soc.*, vol. 32, no. 6, pp. 201-208, March 2017.

[23] Insulated Gate Bi-Polar Transistor Type T2960BB45E, [Online]. Available: http://www.westcode.com/t2960.pdf.

[24] J. Lutz, H. Schlangenotto, U. Scheuermann, Rik De Doncker, "Packaging and Reliability of Power Devices," in *Semiconductor Power Devices - Physics, Characteristics, Reliability*, Springer-Verlag Berlin Heidelberg 2011, pp. 343-348.

[25] M. M. Yovanovich, "Four Decades of Research on Thermal Contact, Gap, and Joint Resistance in Microelectronics," *IEEE Trans. Compon. Packag. Technol.*, vol. 28, no. 2, pp. 182-206, June 2005.

[26] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Power Capability Investigation Based on Electrothermal Models of Press-Pack IGBT Three-Level NPC and ANPC VSCs for Multimegawatt Wind Turbines," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3195-3206, July 2012.

[27] H. Chen, F. Wakeman, J. Pitman, G. Li, "Design, analysis, and testing of PP-IGBT-based submodule stack for the MMC VSC HVDC with 3000 A DC bus current," *J. Eng.*, vol. 2019, no. 16, pp. 917-923, 2019.

[28] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and et al, "Flexible PCB-Based 3-D Integrated SiC Half-Bridge Power Module with Three-Sided Cooling Using Ultralow Inductive Hybrid Packaging Structure," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5579-5593, June 2019.

[29] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and et al, "An SiC-Based Half-Bridge Module with an Improved Hybrid Packaging Method for High Power Density Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8980-8991, Nov. 2017.

[30] L. Wang, W. Liu, D. Malcom, Y. Liu, "An Integrated Power Module Based on the Power-System-In-Inductor Structure," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7904-7915, Sept. 2018.

[31] DuPont Teijin Films. [Online]. Available: http://europe.dupontteijinfilms.com/media/2431/info-mylar-a-electrical-properties.pdf.

[32] X. Lan, X. Lu, M. Y. Chen, D. Scherrer, T. Chung and et al, "Direct On-Chip 3-D Aerosol Jet Printing with High Reliability," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 7, no. 8, pp. 1369-1376, Aug. 2017.

[33] H. Wang, Z. Zhao, P. Fu, J. Li, P. Zhang, "Insulation Performance of Polyetheretherketone Frame inside Press-pack Insulated Gate Bipolar Transistors," *in Proc. IEEE Int. Power Electron. Appl. Conf. Expo. (IEEE PEAC)*, Shenzhen, China, 2018, pp. 915-918.

[34] https://www.kaptontape.com/1_Mil_Kapton_Tapes_Datasheet.php.

[35] http://www.sarltsf.com/products/chemis/peek.html.

2168-6777 (c) 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Aalborg Universitetsbibliotek. Downloaded on May 01,2020 at 06:25:13 UTC from IEEE Xplore. Restrictions apply.