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Impact of Grid Topology on Pole-to-ground Fault Current in Bipolar DC Grids: Mechanism and Evaluation

Yingmin Zhang, Wenxin Zhang, Qiao Peng, Baohong Li, Yan Tao, Min Zhang, Tianqi Liu, and Frede Blaabjerg

***Abstract*—The fault current level analysis is important for bipolar direct current (DC) grids, which determines the operation and protection requirements. The DC grid topology significantly impacts the current path and then the fault current level of the grid, which makes it possible to limit the fault current by optimizing the grid topology. However, the corresponding discussion in the literature is indigent. Aiming at this point, the impact of grid topology, i.e., the connecting scheme of converters, on the pole-to-ground fault current in bipolar DC grids, is investigated in this paper, and the ground-return-based and metallic-return-based grounding schemes are considered, respectively. Firstly, the decoupled equivalent model in frequency domain for fault current analysis is obtained. Then, the impacts of converters with different distances to the fault point on the fault current can be analyzed according to the high-frequency impedance characteristics. Based on the analysis results, a simplified fault current index (SFCI) is proposed to realize the fast evaluation of impact of grid topology on the fault current level. The SFCI is then applied to evaluate the relative fault current level. Finally, the simulation results validate the model, the analysis method, and the SFCI, which can effectively evaluate the relative fault current level in a direct and fast manner.**

***Index Terms*—Bipolar DC grid, pole-to-ground fault, grid topology, fault current evaluation, simplified fault current index.**

I. Introduction

THE modular multilevel converter (MMC) with high voltage and large capacity has become the primary choice in practical high-voltage direct current (HVDC) projects [1], [2], including point-to-point DC systems and DC grids. In the MMC-based DC grids, the DC fault analysis should be specially addressed, as the insulated gate bipolar transistors (IGBTs) in the MMCs are vulnerable and sensitive to DC fault current [3], [4]. Thus, the DC fault current should be evaluated and limited for the stability and safety of the DC grids.

Conventionally, symmetric monopole configuration is more popular for the DC grids due to simplicity and relatively low cost. Thus, the analysis, calculation, and limitation of fault current in symmetric monopole DC grids are widely discussed in the literature. For example, an approximated analytical model for pole-to-ground fault calculation in symmetrical monopole DC grids is presented in [5], and the fault protection strategies are proposed in [6], [7]. Moreover, the DC fault characteristics of medium-voltage DC systems [8] and distribution systems [9] are investigated, which mainly concentrate on the fault detection and ride through methods [10], [11].

With the ascending demand for reliability and flexibility, the bipolar configuration of DC grids emerges [12]. Compared with the symmetric monopole DC grids, the bipolar ones are more complicated with more components, which makes the fault current analysis more challenging. To explore the fault current characteristics of bipolar DC grids, lots of attempts have been made in the literature. Specifically, a pole-to-pole fault current calculation method based on the differential equations is proposed in [13], and the key components impacting the fault current are discussed. However, the high-order differential equations for fault current calculation introduce cumbersome computation, limiting the application in the large-scale DC grids. To solve the computation issue, a state space model to calculate the pole-to-pole fault current of bipolar DC grids with multiple converters is proposed in [14]. Although the analytical fault current expression cannot be directly obtained in such a method, its numerical solution can be resolved with high accuracy and efficiency. With the state space model, the impact of the converter control strategy on the fault current is further investigated [15].

Notably, most of the discussion on fault current in bipolar DC grids focuses on the pole-to-pole fault. Although the pole-to-pole fault is usually the most severe for bipolar DC

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grids, the most frequent fault is pole-to-ground fault. It could also sharply increase the instantaneous current and should be carefully addressed for the DC grid security [16]. Nevertheless, the analysis on the pole-to-ground fault in bipolar DC grids is indigent, where only a few explore the calculation of the pole-to-ground fault current based on the state space model [17], [18]. Moreover, most of the research on the pole-to-ground fault current is realized in symmetric monopole DC grids, as mentioned above. Thus, it is urgent to explore the pole-to-ground fault current characteristics in bipolar DC grids.

In addition to the fault current calculation, the fault current limitation measurements in bipolar DC grids are also important. Accordingly, the thyristor-based DC fault current limiter with inductor inserting-bypassing capability [19], thyristor-based bridge-type fault current limiter [20], and DC circuit breaker with fault current limitation capability [21] have been investigated. However, most of the measurements require additional hardware or components, which inevitably increases the cost of the DC grids. A more economical solution for fault current limitation is to design the DC grid topology, as the capacitor and inductance of converter affect the fault current through the DC lines. It is addressed in [22] that the fault current level of symmetric monopole DC grid could be effectively reduced by optimizing the DC grid topology. This fault current limitation method is independent of additional hardware, and the cost of the DC grid may even decrease. However, as the configurations, topologies, and grounding schemes are different between the symmetrical monopole and the bipolar DC grids, the results obtained in [22] cannot be directly applied to the bipolar DC grids, which should be further explored.

In light of the above, this paper will discuss the impact of grid topology on the pole-to-ground fault current in bipolar DC grids. More specifically, the mechanism of the impact and the simplified evaluation method of grid fault current level will be addressed. The rest of the paper is organized as follows. Firstly, the impact of the grid topology on the fault current in bipolar DC grids with ground returns is investigated in Section II, and the simplified index for relative fault current evaluation is proposed. Then, the impact of the grid topology on the fault current in bipolar DC grids with metallic returns is addressed in Section III with the simplified index to evaluate the relative fault current level. Section IV validates the analysis methods and the proposed evaluation indices through simulation. Finally, concluding remarks are given in Section V.

II. Impact of Grid Topology on Fault Current in Bipolar DC Grids with Ground Returns

For a DC pole-to-ground fault, the path of the fault current is from the grounding point to the fault point. Thus, the grounding schemes of DC grids significantly affect the pole-to-ground fault currents. The grounding schemes of DC grids consist of ground-return-based and metallic-return-based grounding schemes. When the DC grid is with metallic returns, the grounding points of all the converters are connected by the metallic wires, and only one grounding point is required. As for the ground-return-based grounding scheme, there is no metallic wire to connect all the converters. Thus, each converter should have an independent grounding point.

As the grounding schemes impact the fault current in different ways, the topology impact mechanism will be discussed separately with respect to different grounding schemes. Notably, topology in this paper represents the connection of converters on the DC side, i.e., the distribution of DC lines. The DC grids with ground returns will be focused in this section, while the DC grids with metallic returns will be addressed in Section III.

A. Pole-to-ground Fault Current Analysis Based on Decoupled Equivalent Model

The configuration of a bipolar DC grid with ground returns is shown in Fig. 1, where L_n is the neutral line reactance; L_d is the inductance of the DC reactor; R_0 and L_0 are the DC line resistance and inductance, respectively; R_m and L_m are the arm resistance and inductance, respectively; N is the number of submodules (SMs); and MMCp and MMCn represent the positive and negative MMCs, respectively.

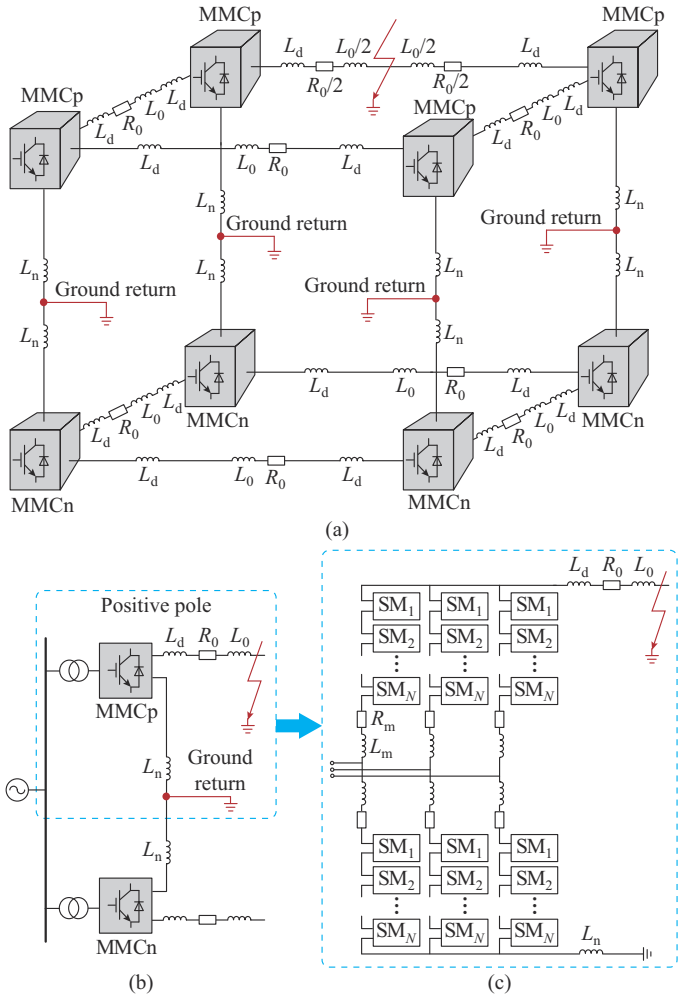

Fig. 1. Configuration of bipolar DC grid with ground returns. (a) Ground-return-based grounding scheme in four-terminal DC grid. (b) Typical bipolar MMC and DC line with pole-to-ground fault. (c) MMCp and DC line with pole-to-ground fault.

The configuration of the ground-return-based grounding scheme in a four-terminal DC grid is shown in Fig. 1(a). The typical bipolar MMC with DC line with a pole-to-ground fault is shown in Fig. 1(b), where the MMC is configured with a ground return for asymmetrical operations [23]. Due to the ideal grounding point at the midpoint between the positive and negative poles of each converter, all the converters are equipotential at the grounding points. It is equivalent to connecting the neutral points of converters by ideal wires, which isolates two poles in the pole-to-ground fault. Thus, the analysis of pole-to-ground faults can be realized by focusing on a single pole. In this paper, the positive pole is focused to illustrate the modeling and analysis. The configuration of MMCp and DC line with pole-to-ground fault is shown in Fig. 1(c).

After a pole-to-ground fault, the fault DC line should be isolated by DC circuit breakers within several milliseconds (1-3 ms in current projects, and 3 ms is considered in this paper) to guarantee the global security. During this short period, the fault current is mainly contributed by the discharge of the capacitors in the SMs [24], and the AC current feeding can be ignored due to large counter electromotive force on the arm reactors [14]. The fault current in this stage can be calculated by the decoupled equivalent resistance-inductance-capacitor (RLC) model of the MMC and the faulty DC line [22], [25], as shown in Fig. 2.

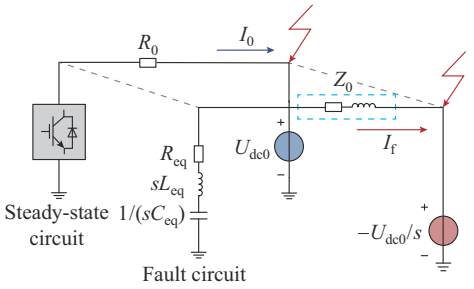

Fig. 2. Decoupled equivalent RLC model of MMC and faulty DC line for pole-to-ground fault analysis.

The fault current is formed by two components, i. e., steady-state component and fault component (I_0 and I_f in Fig. 2, respectively), which can be calculated by the steady-state and fault circuits. More specifically, the steady-state component of the fault current is decided by the power flow, which is determined by the circuit parameters as well as control strategies. When calculating the fault component of the fault current, the transient dynamics of the inductors and capacitors should be considered. To achieve this, the fault component can be calculated by the fault circuit in frequency domain, as shown in Fig. 2, where U_{dc0} is the steady-state DC voltage; $-U_{dc0}/s$ is the instantaneous step signal feeding to the fault point at the fault moment [26]; R_{eq}, L_{eq}, and C_{eq} are the equivalent resistance, inductance, and capacitance of the MMC and DC line, respectively; and Z_0 is the equivalent line impedance. The equivalent parameters are obtained as:

$$\begin{cases} R_{eq} = \dfrac{2}{3} R_m \\ L_{eq} = \dfrac{2}{3} L_m + L_n \\ C_{eq} = \dfrac{3}{2N} C_m \end{cases} \tag{1}$$

$$Z_0 = R_0 + s\left(L_0 + L_d\right) \tag{2}$$

where C_m, L_m, and R_m are the capacitance, reactance, and resistance of an SM, respectively.

Notably, as mentioned above, the steady-state component of the fault current is largely impacted by the control strategies and parameters. Nevertheless, the fault component is barely affected by the controllers, of which the response time is generally above dozens of milliseconds, e.g., the voltage controller, the phase-locked loop (PLL), and the current controller. Thus, the impact of different control strategies and parameters on the fault current is not considered in this paper. As for the valve or SM controllers, they may significantly vary the fault current path, and then the fault current may be impacted, which is, however, out of the scope of this paper.

Based on the decoupled equivalent model, the steady-state and fault components of the fault current can be analyzed independently. Then, the fault component is focused in the current and following subsections. Moreover, unless specified, the fault current in this paper indicates the fault component.

B. Impact Analysis of Grid Topology on Fault Current Based on High-frequency Equivalent Impedance

As indicated in [27], the DC grid topology impacts the fault current mainly through the equivalent impedance. Thus, the impact of the grid topology on the fault current can be investigated by analyzing the grid equivalent impedance. Before that, the impact of different converters on the fault current should be addressed. Based on the decoupled equivalent model shown in Fig. 2, a chained DC grid for analysis of the impact of grid topology on the fault current is constructed, as shown in Fig. 3, where Z_{eq1}, Z_{eq2}, …, Z_{eqn} are the converter equivalent impedances obtained from (1); and Z_{10}, Z_{12}, …, $Z_{(n-1)n}$ are the equivalent impedances of the lines connecting two converters. Notably, the meshed grid can also be represented by such a structure by breaking up the loops according to [26], while the chained DC grid is adopted here for the simplicity of analysis.

The fault current varies when the equivalent impedance from the sources to the fault point changes. Thus, the converters can be classified according to their location with respect to the fault point. In this paper, we define the converters directly connected to the fault point as adjacent converters (e.g., Converter 1 in Fig. 3), and the converters directly connected to the adjacent converters as sub-adjacent converters (e.g., Converter 2 in Fig. 3). The rest converters are defined as distant converters (e.g., Converters 3 and 4 in Fig. 3). The equivalent sum impedances corresponding to different converter connection schemes, i.e., Z_{t1}, Z_{t2}, …, Z_{tn} in Fig. 3, can be obtained as:

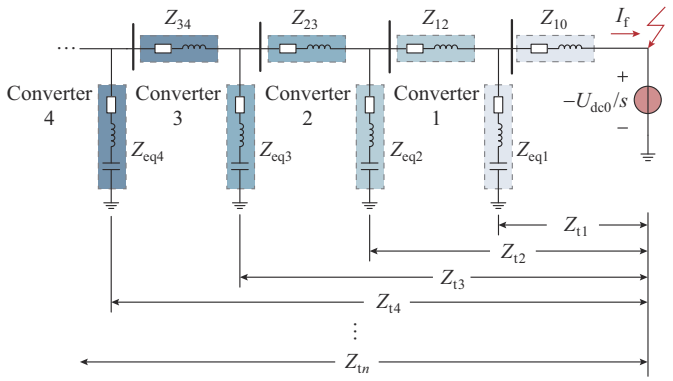

Fig. 3. Chained DC grid for analysis of impact of grid topology on fault current.

$$Z_{tn}=\ldots\left(\left(Z_{eqn}+Z_{n-1,n}\right)//Z_{eq(n-1)}+Z_{n-2,n-1}\right)//Z_{eq(n-2)}+\ldots \quad (3)$$

where the symbol "//" denotes the paralleling of impedance.

To theoretically investigate the impact, the high-frequency equivalent impedance analysis method is applied [26], [28]. Specifically, the fault current in the first several milliseconds (e.g., 3 ms) after faults are mainly decided by the high-frequency characteristic of the equivalent impedance of the fault circuit, as the high-frequency zone in the frequency domain corresponds to the early dynamic after faults in the time domain. According to [29], the region above 100 Hz in the frequency domain significantly affects the fault current value in the first few milliseconds. Thus, the fault current characteristics can be analyzed by investigating the high-frequency equivalent impedance above 100 Hz.

To compare the equivalent impedances of the sets consisting of different types of converters, a case study is conducted in the DC grid, as shown in Fig. 3, and the system parameters are given in Table I, where C_{SM} is the equivalent total capacitance of all the SMs, i.e., $C_{SM}=NC_m$. Notably, the DC lines are overhead lines, of which the traveling-wave process is not considered, as the main objective of this paper is to investigate the impact of the DC grid topology on the fault current level. In the case study, it is considered that the MMC will not be blocked within 3 ms after faults, and the DC lines between converters are of the same length. Moreover, the master-slave control strategy is adopted (Converter 1 is the DC voltage control terminal and the rest is to control the active power).

TABLE I
SYSTEM PARAMETERS OF DC GRID

L_m (mH)	R_m (Ω)	C_{SM} (mF)	L_n (mH)	L_d (mH)	R_0 (Ω)	L_0 (mH)	N	U_{dc} (kV)
50	0.27	15	300	150	1.98	164	200	±400

Based on (3), the equivalent sum impedance of DC grids in Fig. 3 with ground returns and different numbers of converters are calculated, as shown in Fig. 4. It can be observed in Fig. 4 that Z_{t2} (equivalent sum impedance of only adjacent and sub-adjacent converters) and Z_{t4} (equivalent sum impedance of all the converters) are remarkably close to each other (the error is less than 3% at 100 Hz with the reference as Z_{t4}). Thus, it can be inferred that the adjacent and sub-adjacent converters can almost represent all the converters with respect to the contribution to the pole-to-ground fault current in bipolar DC grids with ground returns. Then, it is reasonable to consider only the adjacent and sub-adjacent converters in the fault current evaluation. Moreover, when the impact of grid topology on fault current is considered, the DC grid with more adjacent and sub-adjacent converters with respect to the fault point will have higher fault current level.

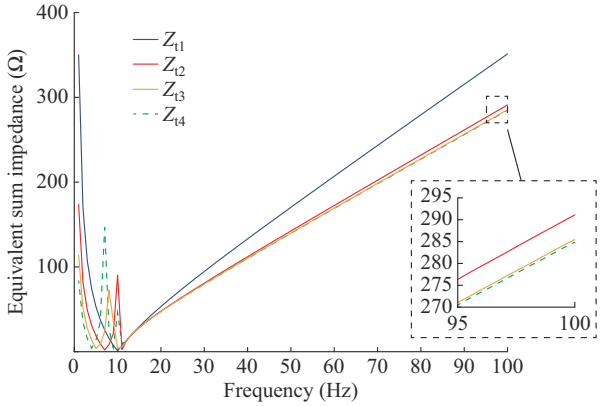

Fig. 4. Equivalent sum impedance of DC grids in Fig. 3 with ground returns and different numbers of converters.

It should be noted that the DC lines contribute to the equivalent sum impedance of the system as well, as shown in Fig. 3. Thus, the DC lines also impact the fault current level of the DC grid. However, the DC line inductance is usually much smaller than the inductance of the neutral line and the DC reactor. Hence, the impact of the converters on the fault current is more significant than the DC lines. Then, the impact of the DC lines on the fault current can be represented by the converters in the above analysis. When the DC line inductance is greater than that shown in Table I, which is a relatively large value for the current DC grid projects, the impact of the DC lines on the fault current should be specifically addressed.

C. Simplified Fault Current Index for Fast Fault Current Level Evaluation in DC Grid with Ground Returns

Although the fault current can be analytically calculated based on the state space model, the calculation requires burdensome computation, especially when the number of converters increases. Thus, the state space model is not cost-effective and computation-efficient to be adopted for the analysis of the impact of grid topology on the fault current level, i.e., the maximum fault current value of the DC grid. To tackle this issue, a simplified index that can evaluate the relative fault current levels of different DC grids in a simple and fast way is required. According to the previous analysis, the pole-to-ground fault current in the DC grid with ground returns is mainly impacted by the adjacent and sub-adjacent converters. Then, the distant converters and connecting lines can be ignored in such a case, as shown in Fig. 5, where i and j denote the adjacent converters, and x, y, p, q, m, n denote the sub-adjacent converters.

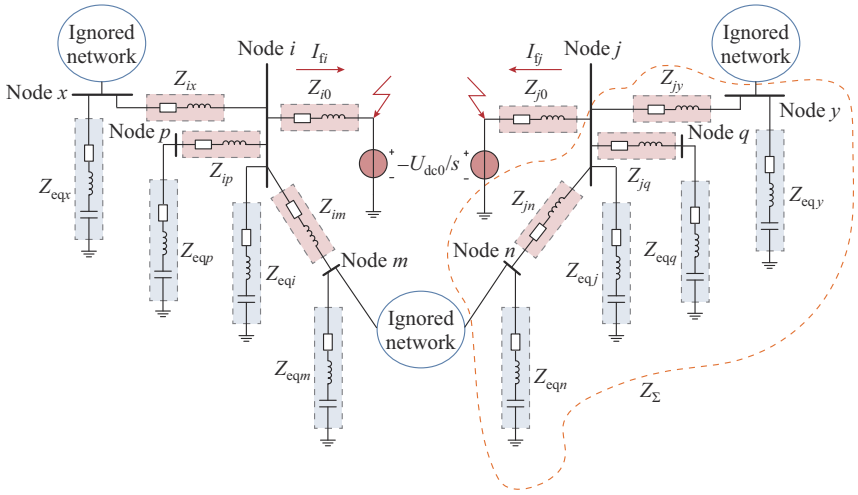

Fig. 5. Simplified equivalent model of a DC grid considering only adjacent and sub-adjacent converters and corresponding DC lines for pole-to-ground fault analysis.

When a pole-to-ground fault occurs on line *ij*, the equivalent impedance from the fault point to node *i*, defined as Z_{fij}, can be obtained from Fig. 5 as:

$$Z_{fij}=\frac{1}{\dfrac{1}{Z_{im}+Z_{eqm}}+\dfrac{1}{Z_{ip}+Z_{eqp}}+\dfrac{1}{Z_{ix}+Z_{eqx}}+\dfrac{1}{Z_{eqi}}}+Z_{i0} \tag{4}$$

where Z_{i0} is the impedance from node *i* to the fault point; Z_{ix} is the equivalent impedance of the line connecting nodes *i* and *x*; and the rest parameters are defined in the same manner.

Note that the inductance impedance is usually much higher than the resistance and capacitance impedances in high-frequency domain, as shown in Fig. 6.

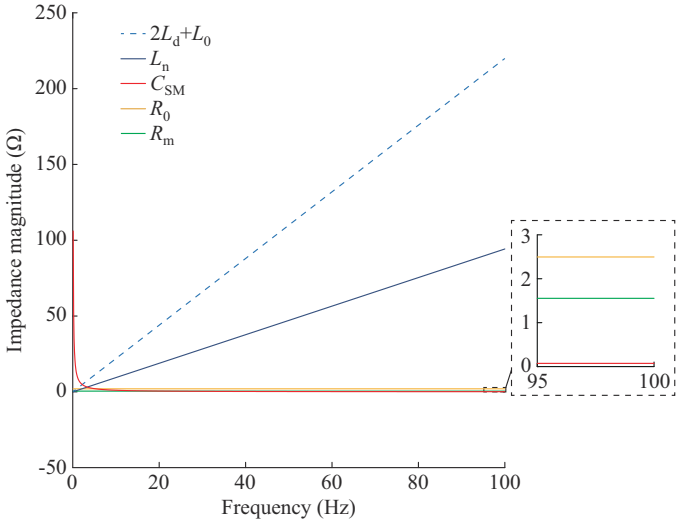

Fig. 6. Magnitudes of resistance, inductance, and capacitance impedances in frequency domain.

Thus, the impedances in (4) can be replaced by the inductances for simplification, which obtains the fault current in time domain as:

$$I_{fj}(t)=L^{-1}\left(\frac{U_{dc0}/s}{s\left(L_d+L_{\Sigma}\right)}\right)=\frac{U_{dc0}}{L_d+L_{\Sigma}}t \tag{5}$$

where L_{Σ} is the parallel equivalent inductance of the adjacent converters and the sub-adjacent converters as well as the connecting lines. It should be noted that (5) is obtained by considering only the adjacent and sub-adjacent converters in the fault current analysis, which is viable according to previous analysis. In such a case, L_{Σ} in (5) consists of only the arm inductance of the adjacent and sub-adjacent converters and the line inductances between the two types of converters. Thus, L_{Σ} can be used for the fault current analysis in the early fault stage, e.g., within 3 ms after the fault. In the early stage, the fault current rising trend is approximately linear. Moreover, the closer the concerned time point is to the fault time, the more accurate the fault current characteristics are according to (5).

Considering that the fault current is conversely proportional to the impedance, the relative fault current levels of different DC grids can be evaluated by comparing their equivalent sum impedances. As the maximum fault current usually appears at the converter terminal on a DC line, L_d in (5) can be ignored.

Then, the simplified fault current index (SFCI) of DC grid with ground returns (SFCI-G) is defined as:

$$SFCI\text{-}G_{ij}=\frac{U_{dc0}}{L_{\Sigma}} \tag{6}$$

For a DC grid with *m* lines, a total of 2*m* SFCI-G values should be calculated to obtain the maximum fault current with this topology. Then, the maximum SFCI-G (indicated as $SFCI\text{-}G^{max}$) can be used to represent the fault current level of this topology, which can be further used for DC grid topology design and optimization in terms of fault current limitation. Notably, SFCI-G is not the numerical fault current. Instead, it is used to evaluate the possible maximum fault current for a DC grid with certain topology and certain fault point.

It can be observed in (6) that only the topology of the DC grid, steady-state parameters, and the fault point location should be given in the calculation of SFCI, where the iterative calculation is avoided.

III. Impact of Grid Topology on Fault Current of Bipolar DC Grid with Metallic Returns

A. Equivalent Model Transformation for Pole-to-ground Fault Analysis

The metallic return scheme is another basic grounding scheme for bipolar DC grid. A typical four-terminal bipolar DC grid with metallic returns is shown in Fig. 7, where R_g and L_g are the grounding resistance and inductance of the metallic returns, respectively. The neutral points of all the converters are connected by metallic wires with impedance, and all the converters share a common grounding point.

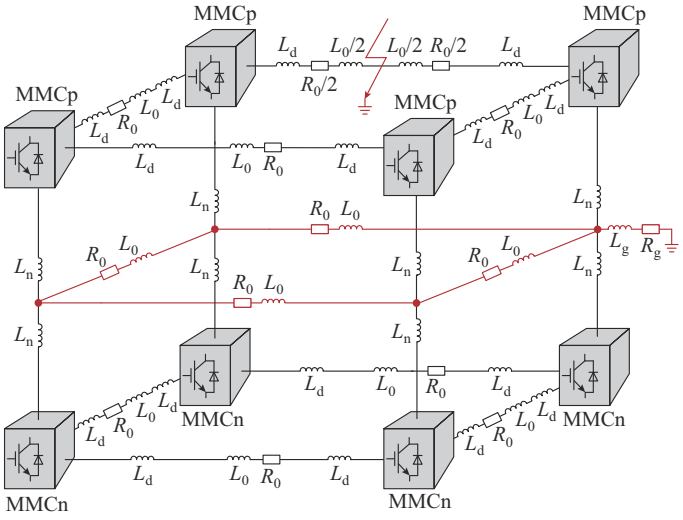

Fig. 7. Typical four-terminal bipolar DC grid with metallic returns.

Different from the DC grid with ground returns, the DC grid with metallic returns cannot be analyzed by directly aggregating the equivalent impedances of converters, as they are not physically in parallel due to the impedances of the metallic wires. Instead, the DC grid equivalent model should be transformed before the fault current analysis. Specifically, three transformation processes are required, which will be exemplified in a four-terminal DC grid as shown in Fig. 8.

1) Transformation 1: Ignoring Healthy Pole

In a DC grid with metallic returns, the impedances of the metallic wires are much smaller than the sum of the healthy pole converters. As a result, there is almost no fault current flows through the healthy pole. Then, the fault current is almost provided by the fault pole converter, while the healthy pole converter does not contribute to the fault current. Additionally, although in a pole-to-ground fault, the healthy pole will be disturbed by the fault current, the amplitude of the disturbance current is negligible, and the sum of the disturbance current is zero. Thus, the healthy pole does not affect the fault pole in turn. Without consideration of the impact of the healthy pole, the model of the DC grid with metallic returns shown in Fig. 8(a) can be transformed to the model as shown in Fig. 8(b).

2) Transformation 2: Transforming Meshed Metallic Returns to Radial Configuration

To analyze the fault current more efficiently, the meshed grid shown in Fig. 8(b) should be transformed to the radial grid, and then, the impedance characteristics can be generally investigated. To achieve so, the transfer impedance algorithm of passive grid can be applied. After the transformation, the general radial model of the DC grid can be obtained, as shown in Fig. 8(c), where R'_{gi} and L'_{gi} are the transfer resistance and inductance from the i^{th} converter to the grounding point, respectively.

3) Transformation 3: Decoupling Common Grounding Point

When focusing on the fault currents flow through the converters to the grounding point, the common grounding point can be decoupled. Then, the grounding path of each converter becomes an independent loop from the converter to the decoupled grounding point via an equivalent impedance, as shown in Fig. 8(d). The main concept is to split the grounding resistance and inductance according to the currents injected from converters. When calculating the equivalent inductance, the sharing factor of each converter is obtained as:

$$h_{Li}=\sum_{k=1}^{n}\frac{L_{Fi}}{L_{Fk}} \tag{7}$$

$$L_{Fi}=L'_{gi}+L_{eqi} \tag{8}$$

Then, the inductance L_{eqgi} from the i^{th} converter to the grounding point in Fig. 8(d) can be obtained as:

$$L_{eqgi}=h_{Li}L_g+L'_{gi}+L_{eqi} \tag{9}$$

Notably, R_{eqg} and L_{eqg} consist of the arm resistance and arm inductance, respectively, while the converters in Fig. 8(d) are presented for illustration only. The equivalent resistance R_{eqgi} in Fig. 8(d) can be obtained in a similar way. More details about the transformations and derivations can be found in Appendix A.

B. Topology Impact Analysis of DC Grid with Metallic Returns Based on High-frequency Equivalent Impedance

Based on the transformed model, as shown in Fig. 8(d), the previous topology impact analysis method in Section II can now be used for DC grid with metallic returns. With the same converter parameters in Table I, the high-frequency equivalent impedances of the DC grids with metallic returns and different numbers of converters shown in Fig. 3 are calculated, as shown in Fig. 9. It can be observed in Fig. 9 that the equivalent sum impedances in high-frequency domain vary a lot with each other. Thus, it can be referred that the pole-to-ground fault current in the DC grids with metallic returns is impacted by all the converters and lines. This is different from the DC grid with grounding returns, of which the fault current is mainly contributed by the adjacent and sub-adjacent converters. Thus, all the converters and DC lines should be considered when analyzing the pole-to-ground fault in the DC grids with metallic returns. The reason is that the metallic returns will introduce additional impedance into the DC grid, including the impedances of the grounding wire and the metallic wires. In such a case, the equivalent impedance from the converter to the grounding point will change compared with Fig. 2, as show in Fig. 8(d).

Then, the additional equivalent impedances distinguish the equivalent sum impedances corresponding to different converter connection schemes.

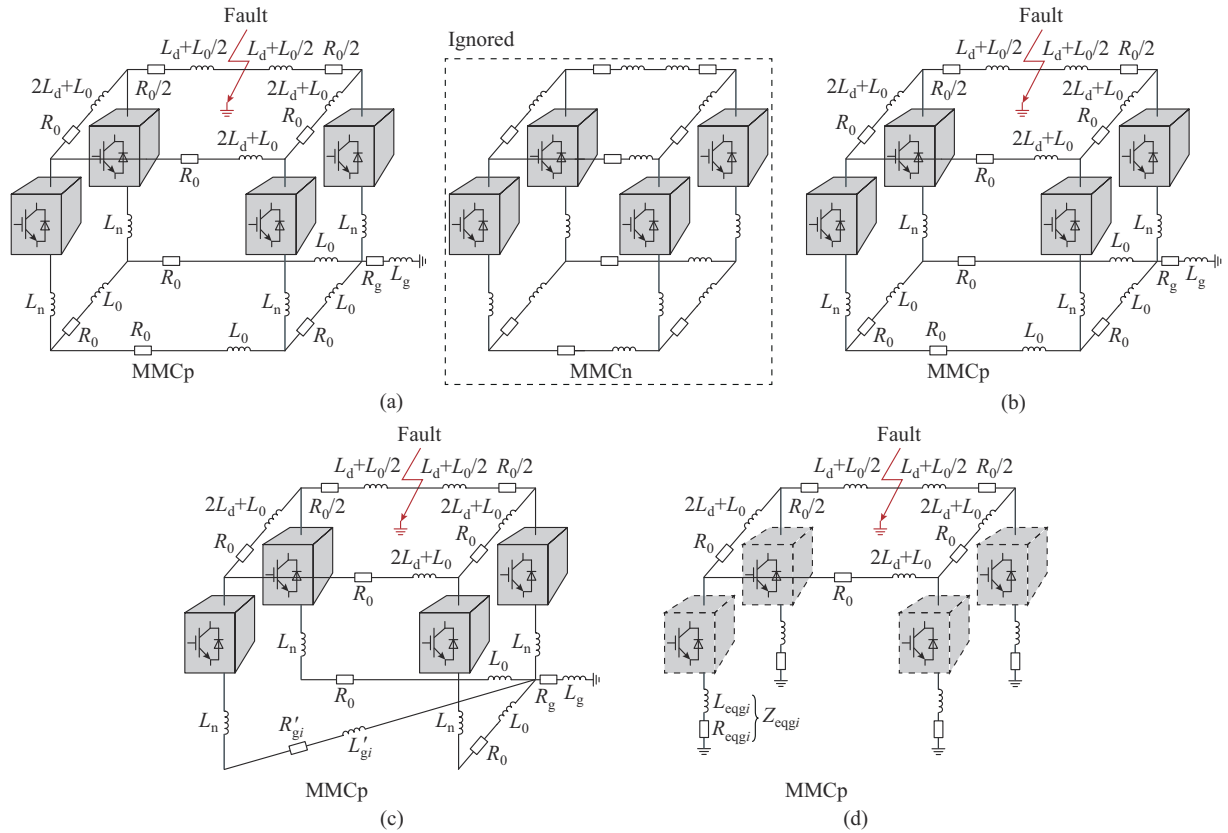

Fig. 8. Model transformation of bipolar DC grid with metallic returns. (a) Full model with two poles. (b) Model ignoring healthy pole. (c) Model in general radial configuration. (d) Model after decoupling common grounding point.

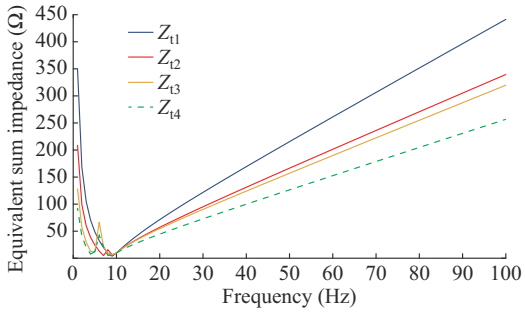

Fig. 9. Equivalent sum impedances of DC grids in Fig. 3 with metallic returns and different numbers of converters.

C. Simplified Fault Current Index for Fast Fault Current Level Evaluation in DC Grid with Metallic Returns

According to the transformed model shown in Fig. 8(d), an MMC with metallic return can be analyzed in the same way as the MMC with ground return, while the equivalent sum impedance is increased. Thus, similar to Section II-C, the SFCI for the DC grids with metallic returns (SFCI-M) can be developed to evaluate the relative fault current levels. Referring to Fig. 5 and (4), the sum equivalent impedance of the DC grid with metallic returns can be obtained as:

$$Z'_{fij} = Z'_{\Sigma} + Z_{j0} \tag{10}$$

where Z'_{Σ} is the parallel equivalent impedance of all the converters in the transformed model.

Then, the fault current in the time domain can be obtained as:

$$I_{fj}(t) = \frac{U_{dc0}}{Z'_{fij}} t \tag{11}$$

Ignoring the resistance and considering that the maximum fault current usually appears at the converter terminal on a DC line, SFCI-M can be defined as:

$$SFCI\text{-}M_{ij} = \frac{U_{dc0}}{\dfrac{1}{L'_{\Sigma m}} + \dfrac{1}{L'_{\Sigma p}} + \dfrac{1}{L'_{\Sigma x}} + \ldots + \dfrac{1}{L'_{eqi}}} \tag{12}$$

The maximum SFCI-M, i.e., $SFCI\text{-}M^{max}$, can be used to represent the relative fault current level of this topology, which can be further used for DC grid topology design and optimization. Similar to SFCI-G, $2m$ SFCI-M values should be calculated to obtain the maximum fault current of a DC grid consisting of m lines with a certain topology.

IV. Simulation Results

A. Validation of High-frequency Impedance-based Fault Current Analysis Method

The high-frequency impedance-based fault current analysis method is validated at first. A meshed five-terminal DC grid, whose topology is shown in Fig. 10, is adopted as the test system, of which the parameters are shown in Table I. The pole-to-ground fault point is set at the midpoint of Converters 1 and 5. The calculation results according to (5) and

(11) are obtained in Fig. 11 with the PSCAD/EMTDC simulation results, where the results of the DC grids with ground returns and metallic returns are given. It can be observed in Fig. 11 that within the first 3 ms after fault, the calculation results of the fault current match well with the simulation results, where the errors are within 3%. Thus, the high-frequency impedance-based fault current analysis and the DC grid topology impact analysis are reasonable and viable.

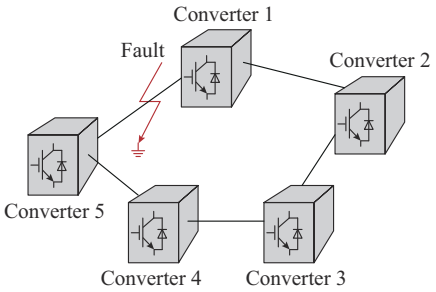

Fig. 10. Topology of a meshed five-terminal DC grid.

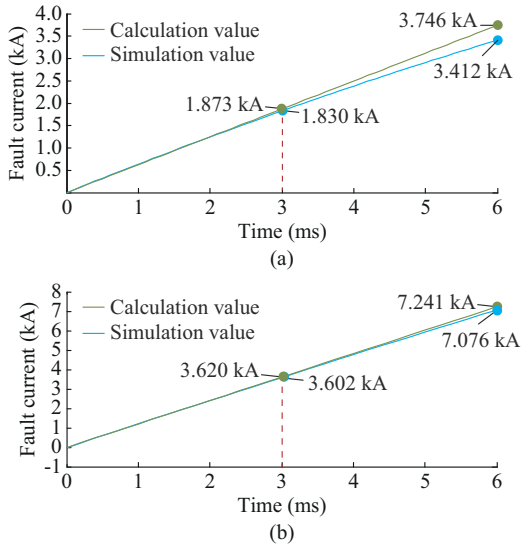

Fig. 11. Calculation and simulation results of fault current when DC grid is with ground or metallic returns. (a) Ground returns. (b) Metallic returns.

B. Validation of Topology Impact Analysis Results

To verify the analysis results about the impact of grid topology on the fault current characteristic, a chained DC grid is tested in PSCAD/EMTDC, as shown in Fig. 12. It should be mentioned that Fig. 12 is a schematic diagram of the DC grid to display the connection of converters. Thus, the DC lines are not presented. The system parameters are the same, as shown in Table I.

First, only two of the converters are connected (Converters 1 and 2), referring to Case 1. Then, one more converter (Converter 3) is connected to Converter 2, referring to Case 2. The fourth converter (Converter 4) is then connected to Converter 3 in Case 3. Finally, the fifth converter (Converter 5) is connected to Converter 4 in Case 4. A pole-to-ground fault is triggered at the midpoint of the DC line connecting Converters 1 and 2 at $t=2$ s. The fault currents that last for 3 ms in the DC grid with different topology cases are shown in Fig. 13, where the DC grid is with ground and metallic returns, respectively.

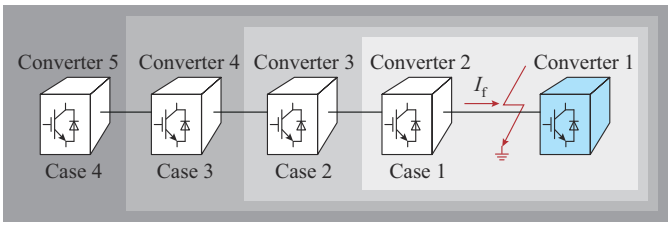

Fig. 12. Schematic diagram of chained DC grid for topology impact mechanism verification.

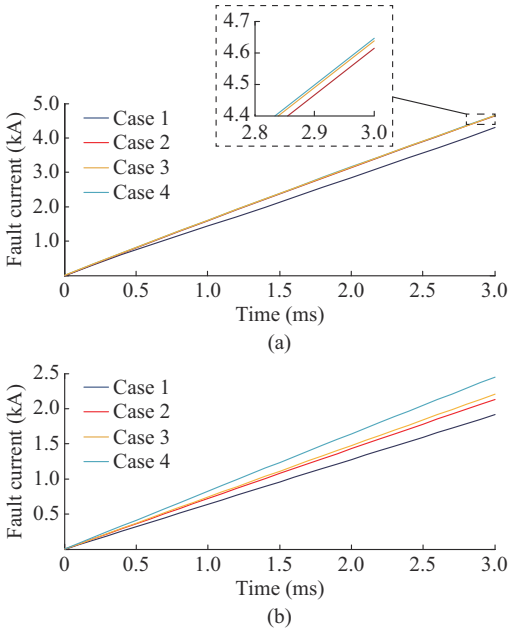

Fig. 13. Fault currents in DC grid with different topology cases. (a) Ground returns. (b) Metallic returns.

It can be observed in Fig. 13(a) that the fault current that lasts for 3 ms of Case 2 is 4.54 kA, while the fault current of Case 4 is 4.63 kA. It indicates that the error caused by the ignorance of Converters 3 and 4 is smaller than 2%. Thus, the adjacent converters and sub-adjacent converters contribute the most to the pole-to-ground fault current (more than 98%), while the contribution of the distant converters is less than 2% when the DC grid is with ground returns. Different results can be observed in Fig. 13(b), where the fault currents in the DC grids with metallic returns are presented. In Fig. 13(b), the more converters are added, the larger fault current is generated, indicating that all the converters impact the fault current rather than the adjacent or sub-adjacent ones. The simulation results match well with the analysis results.

To further validate the analysis results, a case study in the five-terminal DC grid, as shown in Fig. 10, is conducted. The pole-to-ground fault is also applied on the line connecting Converters 1 and 5. In the case study, the DC voltage is focused to evaluate the discharging level of converter, where a larger DC voltage deviation indicates a higher discharging level, corresponding to larger contribution to fault current. The simulation results are shown in Fig. 14, which presents the DC voltages of converters in the five-terminal DC grid

with ground and metallic returns, respectively. It can be observed in Fig. 14 that when the DC grid is with ground returns, the DC voltages of Converters 1 and 5 are reduced most significantly, followed by those of Converters 2 and 4, and the DC voltage of Converter 3 barely deviates from the initial value. Thus, Converters 1 and 5, as the adjacent converters, impact more on the fault current. The impact of the sub-adjacent converters, i.e., Converters 2 and 4, is less than the adjacent converters. Moreover, the distant converter, i.e., Converter 3, hardly contributes to the fault current. As for the DC grid with metallic returns, it can be observed from Fig. 14(b) that the DC voltages of all the converters are reduced to a relatively large extent. That is to say, all of the adjacent, sub-adjacent, and distant converters contribute to the pole-to-ground fault current at an approximately average level. The results validate the theoretical analysis again.

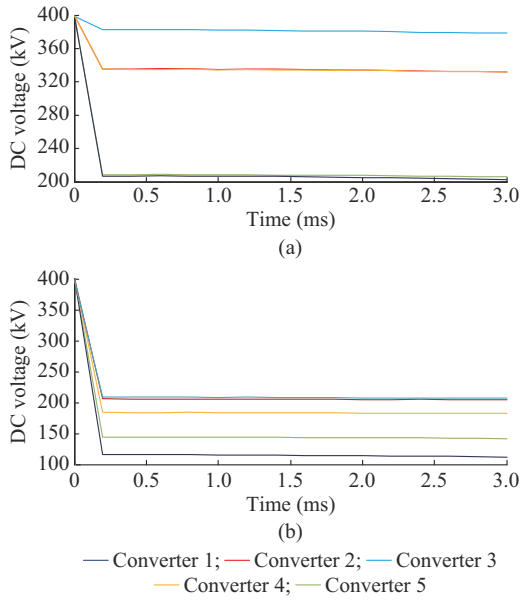

Fig. 14. DC voltages of converters in five-terminal DC grid with ground or metallic returns. (a) Ground returns. (b) Metallic returns.

According to the analysis results, from the perspective of pole-to-ground fault current limitation, the metallic return-based grounding scheme is preferable for the DC grid with less converters, which can effectively increase the equivalent impedance of the DC grid to suppress the fault current. However, when DC grid is expanded to a relatively large extent with more converters, the ground-return-based grounding scheme may be more proper, where the distant converters will scarcely contribute to the fault current.

C. Validation of Simplified Fault Current Indices

The validation of the proposed SFCI, including SFCI-G and SFCI-M, is then carried out. The simulation is also conducted in the five-terminal DC grid as shown in Fig. 10. The pole-to-ground fault at the midpoint of each DC line is successively triggered. Pole-to-ground fault current simulation results compared with calculated SFCI when the DC grid is with ground or metallic returns are shown in Fig. 15, respectively. It should be mentioned that the SFCI-G and SFCI-M are without dimensions, which are used to evaluate the relative fault current levels of DC grids rapidly and directly. In Fig. 15, I_{12} and I_{21} are the fault currents fed from Converters 1 and 2, respectively, to the fault point when the fault appears at the midpoint of line 12, which is the most severe for Converters 1 and 2.

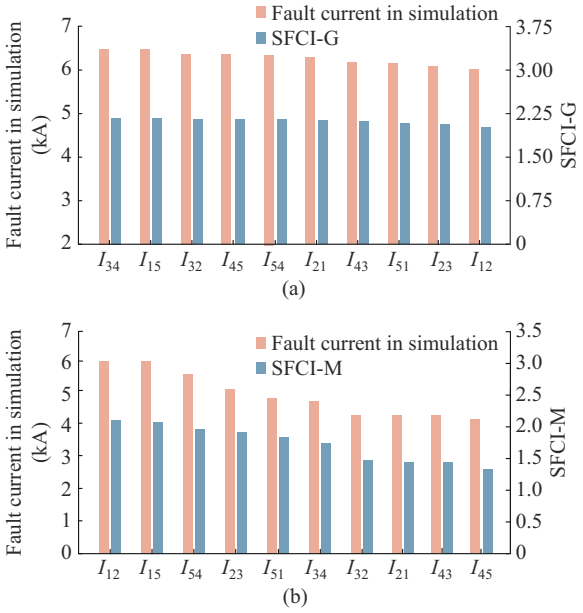

Fig. 15. Pole-to-ground fault current simulation results compared with calculated SFCI when DC grid is with ground or metallic returns. (a) Ground returns. (b) Metallic returns.

As can be observed from Fig. 15, the SFCI results effectively evaluate the relative fault current of the DC grids with different fault points and different grounding schemes. For instance, as shown in Fig 15(a), the largest fault current in the simulation results is 6.642 kA, corresponding to I_{34}, of which the SFCI-G is also the largest in the SFCI-G results, i.e., 2.193 kA. The results show that the proposed SFCI can effectively evaluate the relative fault current level. Based on the SFCI, the worse fault point for a DC grid with certain topology can be identified. For example, it can be observed in Fig. 15(a) that $SFCI\text{-}G^{max}$ corresponds to I_{34}, indicating that the worse fault current is the one from node 3 to node 4 when the fault appears on line 34. The simulation results validate that I_{34} is the maximum fault current with the current DC grid topology.

D. Fault Current Level Evaluation Based on Proposed Simplified Indices

The simplified indices are further applied to screen the DC grid topologies in terms of fault current level evaluation, where the grounding and metallic return schemes are considered, respectively. The fault current level of the DC grid is defined as the highest fault current value that the system can reach, i.e., the fault current of the worst fault point. In this case study, the midpoints of DC lines are selected as the fault points to observe the fault current characteristics. The fault point (one of the midpoints of the DC lines) with the largest fault current is identified as the worst fault point.

It should be mentioned that the pre-fault condition of the DC grid is that the power output of all the converters is set

to be zero, i.e., there is no power flow in the DC grid in steady state. This precondition has been proven to be reasonable for fault current analysis in [30]. Specifically, the fault current is formed by steady-state component and fault component, where the latter is provided by the capacitors in SMs. The pre-fault component and the fault component are almost linearly composited to form the fault current. The steady-state component is mainly determined by the power references of converters, and the fault component is basically determined by the grid topology, which is the focus of this paper. Moreover, the pre-fault component is relatively small compared with the fault component. Thus, the zero-power flow is realized in the case study of this paper to focus on the fault component of the fault current.

The simulation is conducted in a five-terminal DC grid, and several typical topologies for fault current level evaluation are shown in Fig. 16, which will be assessed and compared with ground return and metallic return schemes, respectively. To evaluate the fault current level, the pole-to-ground fault is successively applied on all the lines for each topology. The pole-to-ground fault current simulation results are presented in Fig. 17, which are compared with the calculated SFCI when DC grids of different topologies are with ground or metallic returns. The results corresponding to the DC grids with ground returns are shown in Fig. 17(a), where the SFCI values and simulation results agree well with each other. The lines with the highest fault current at 3 ms after fault are marked in Fig. 16, as indicated by the fault symbols. It can be observed in Fig. 17 that the fault current level of the loop topology 1 is the lowest, while the fault current level of the radial topology 5 is the highest.

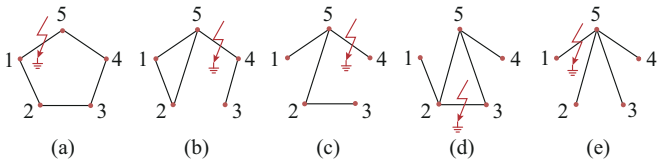

Fig. 16. Several typical topologies for fault current level evaluation. (a) Topology 1. (b) Topology 2. (c) Topology 3. (d) Topology 4. (e) Topology 5.

The results corresponding to the DC grids with metallic returns shown in Fig. 17(b) also present a significant agreement between the simulation results and SFCI. It can be observed in Fig. 17(b) that the fault current levels of the loop topology 1 and radial topology 5 are still the lowest and the highest, respectively. However, the ranking of fault current levels for other topologies is different from the results of the DC grids with ground returns, which indicates different impact mechanisms of grid topology on the fault current in these two cases.

V. Conclusion

The impact of grid topology on pole-to-ground fault current and its fast evaluation method in bipolar DC grids are addressed in this paper, where the ground-return-based and metallic-return-based grounding schemes are considered, respectively. The conclusion of this paper is summarized as follows.

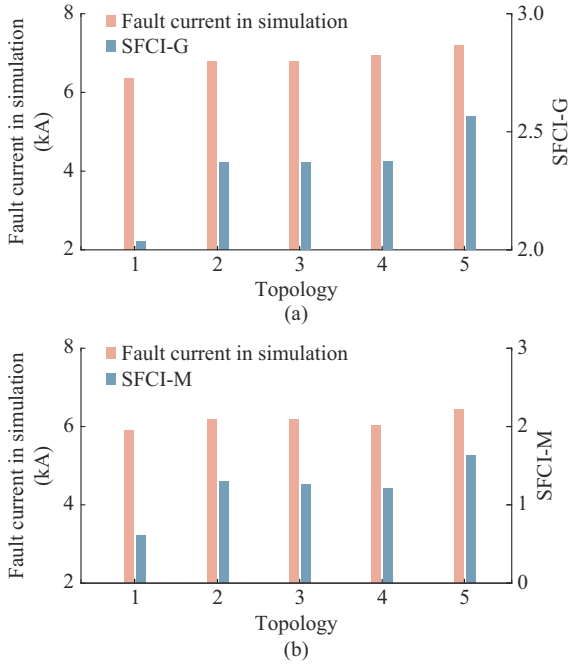

Fig. 17. Pole-to-ground fault current simulation results compared with calculated SFCI when DC grids of different topologies are with ground or metallic returns. (a) Ground returns. (b) Metallic returns.

1) The proposed high-frequency impedance-based fault current analysis method is accurate, especially when it is used to calculate the current that lasts for 3 ms after fault. Moreover, the SFCI can effectively evaluate the relative fault current levels of DC grids with different topologies. The cumbersome computation is avoided in such an evaluation method, based on which the fault current level can be assessed directly and rapidly.

2) The DC grid topology largely impacts the pole-to-ground fault current, while the impact mechanisms of the DC grids with ground and metallic returns are different. In the DC grid with ground returns, the fault current is mainly affected by the adjacent and sub-adjacent converters. In the DC grid with metallic returns, all the converters, including the distant converters, contribute to the fault current at an approximately average level.

3) Based on the proposed SFCI, it has been found that the loop topology is usually with the lowest fault current level, while the radial topology obtains the highest. In the future, the proposed analysis method and simplified indices will be used to optimize the DC grid topology with respect to fault current limitation.

Appendix A

The details of Transformation 2 in Fig. 8 and derivation of (9) are given as follows.

A four-node DC grid before transformation is shown in Fig. A1(a), where Z_{ij} is the real impedance between nodes i and j; and Z'_{nm} is the transfer impedance from nodes n to m.

The transfer impedance from node 1 to node 2, i.e., Z'_{12}, can be obtained as:

$$Z'_{12} = Z_{12} // \left(Z_{14} + Z_{23} + Z_{34} \right) \tag{A1}$$

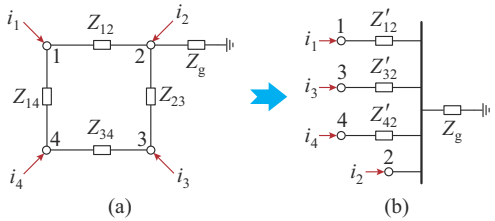

Fig. A1. Equivalent model of metallic returns of four-node DC grid. (a) Before transformation. (b) After transformation.

The rest can be done in the same manner, yielding:

$$Z'_{32}=Z_{23}//\left(Z_{14}+Z_{12}+Z_{34}\right) \tag{A2}$$

$$Z'_{42}=\left(Z_{12}+Z_{14}\right)//\left(Z_{23}+Z_{34}\right) \tag{A3}$$

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