Multidisciplinary Modelling Tools for Power Electronic Circuits

with Focus on High Power Modules

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Multidisciplinary Modelling Tools for Power Electronic Circuits

with Focus on High Power Modules

by

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Center of Reliable Power Electronics (CORPE)

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(With Focus on High Power Modules)

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CV

Amir Sajjad Bahman received the B.Sc. degree from Iran University of Technology, Tehran, Iran, in 2008, and the M.Sc. degree from Chalmers University of Technology, Gothenburg, Sweden, in 2011, both in electrical engineering. He joined the Center of Reliable Power Electronics (CORPE) at Aalborg University in 2012. He is currently pursuing toward the Ph.D. degree in the Department of Energy Technology, Aalborg University. His current research interests include reliability, thermal management, power module packaging, and power electronics applications in renewable energy systems.

Preface

This thesis is a summary of the PhD project entitled “Multidisciplinary Modelling Tools for Power Electronic Circuits (With Focus on High Power Modules)”. This work has been made possible by the Center of Reliable Power Electronics (CORPE) at the Department of Energy Technology, Aalborg University, Denmark. Acknowledgements are given to the above-mentioned institution that financially supported me through my PhD study.

This research project was done under supervision of Prof. Frede Blaabjerg, Prof. Francesco Iannuzzo, and Assistant Prof. Ke Ma from the Department of Energy Technology in Aalborg University. First and foremost, I would like to express my deepest gratitude to my supervisor, Prof. Frede Blaabjerg, for his for setting me on this journey through such a wide range of material and his leadership throughout the project. Dr. Ke Ma has mentored me step by step through several meetings helping to dispel uncertainty and promote understanding. Prof. Francesco Iannuzzo also mentored me throughout this project and spent many hours working out problems with me very friendly. Prof. Poh Chiang Loh also supervised me throughout the beginning of this project learning the control strategies for power electronic circuits. Dr. Huai Wang also mentored me from the beginning of this project to get insight into design for reliability approach. Furthermore, thanks to Pramod Ghimire for significant assistance with experimental works and discussions on numerous topics.

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The industry advisory board of this institute has provided me many insights into what is truly needed to improve the engineering of power electronics. Klaus Olesen at Danfoss Silicon Power GmbH provided key information on the thermal design process of power modules and many interesting discussions during my internship. Additionally, I would like to thank specialists at ANSYS, Inc., Jens Uwe Friemann and Vinayak Kamat, for significant assistance with solving problems in FEM simulations.

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Finally, I wish to express my most sincere gratitude to my family for their exceptional love, support, concern, understanding and encouragement through my life.

Niels Bohr, a Danish physicist, ever said, “Every great and deep difficulty bears in itself its own solution. It forces us to change our thinking in order to find it”. After this three-year Ph.D. study, I found out that most of the important things in the world have been accomplished by people who have kept on trying when there seemed to be no hope at all. I do my best to be as brave as to make a wonderful life with what I have learnt from all of you. Wish the best for all of us.

Amir Sajjad Bahman

October 2015, Aalborg

Abstract

This thesis presents multidisciplinary modelling techniques in a Design For Reliability (DFR) approach for power electronic circuits. With increasing penetration of renewable energy systems, the demand for reliable power conversion systems is becoming critical. Since a large part of electricity is processed through power electronics, highly efficient, sustainable, reliable and cost-effective power electronic devices are needed. Reliability of a product is defined as the ability to perform within its predefined functions under given conditions in a specific time. Because power electronic devices are applied in a wide range of loads and frequencies, the reliability of a power device may face to challenges to perform within the product specification in different application where high electrical/thermal stresses are experienced. Moreover, with the integration of power electronic devices in a compact package, e.g. power module, DFR approach meets trade-offs in electrical, thermal and mechanical design of the device.

Today, virtual prototyping of power electronic circuits using advanced simulation tools is becoming attractive due to cost/time saving in building potential designs. With simulations, the designer can test new concepts and optimize design layouts before the physical components and systems are built up. Moreover, if a failure occurs, there will be no destruction, but valuable data is obtained to modify and to optimize the product as part of an iterative design process. A key requirement to this process is to quickly generate compact and simple models describing the electrical and thermal performance of a potential design. Even though, numerical tools based on Finite Element Analysis (FEA) are powerful in studying the physical behavior of power devices, they are time consuming and demand for expensive computation facilities in DFR approach. Therefore, in this thesis focus is placed on the generation of accurate, simple and generic models to study and assess thermal and electrical behavior of power electronic circuits (especially power modules).

In this thesis, different power electronic converter topologies and control strategies are investigated with focus on reducing the number of active components and increasing the efficiency of converter. Several power converter topologies are discussed and compared with alternative solutions from power dissipation and efficiency point of view. By understanding the methods gain to identify power dissipation in the power modules, FEM simulations are utilized to investigate thermal behavior of power module in normal (e.g. power cycling) as well as abnormal (e.g. short-circuit) conditions. By knowing the challenges and shortcomings in FEM simulation in reliability assessment of power modules, a three-dimensional lumped thermal network is proposed to be used for fast, accurate and detailed temperature estimation of power module in dynamic operation and different boundary conditions.

Since an important issue in the reliability of power electronics is the thermal management of power devices, efficient cooling system design will be aimed in the following. Due to better performance of direct liquid cooling systems compared to forced air cooling systems, they will be utilized to cool down the power module. A design tool is presented with a user friendly

environment to be used for optimization of cooling system layout with respect to thermal resistance and pressure drop reductions.

Finally extraction of electrical parasitics in the multi-chip power modules will be investigated. As the switching frequency of power devices increases, the size of passive components are reduced considerably that leads to increase of power density and cost reduction. However, electrical parasitics become more challenging with increasing the switching frequency and paralleled chips in the integrated and denser packages. Therefore, electrical parasitic models are analyzed based on micro-strip structures and partial inductances to predict parasitic parameters according to varied layouts.

Some of the presented models in this thesis are verified by FEM simulations and experimental results in real world applications. The power losses, thermal and electrical parasitic models are generic and valid to be used in circuit simulators or any programing software. These models are important building blocks for the reliable design process or performance assessment of power electronic circuits. The models can save time and cost in power electronics packaging and power converter to evaluate new designs and to assess products in normal, abnormal, and harsh environments.

Dansk Abstrakt

I denne afhandling præsenteres en række multi-disciplinære modelleringsteknikker indenfor ”Design For Reliability (DFR)” – design som er målrettet med pålidelighed indenfor effektelektronik. Med en stigende vækst i udnyttelsen af vedvarende energi følger også et øget behov for pålidelige effektomformnings-systemer. Da effektelektronik er involveret i størstedelen omformningen af elektrisk energi er der specielt behov for effektelektronik-teknologier, der har høj effektivitet, er bæredygtige, pålidelige og billige. Et givet produkts pålidelighed defineres ved dets evne til at opretholde sin funktion indenfor dets arbejdsområde i et givet tidsrum under veldefinerede betingelser. Da effektelektronik anvendes indenfor en række varierende belastninger, kan dette give udfordringer, hvis produktet anvendes i andre områder, hvor det udsættes for en stor elektrisk og termiske belastning. Derudover skal det tages i betragtning, at hvis effektelektroniske komponenter integreres i kompakte enheder, såsom i effektmoduler, kan man i DFR tilgangen tage nødvendige afvejninger imellem elektrisk, termisk, og mekanisk design-hensyn.

Brugen af virtuelle prototyper til effektelektroniske kredsløb ved hjælp af avancerede simulerings værktøjer er attraktivt, da det er en tids- og omkostningseffektiv måde at udvikle nye, potentielle designs på. Ved hjælp af simuleringer kan designeren teste nye koncepter og optimere design layouts inden de virkelige systemer realiseres. Endvidere, hvis et design skulle vise sig at lede til fejlhændelser, er der ingen reelle destruktive hændelser i virtuelle prototyper, men derimod mulighed for at få vigtig information, der kan bruges til yderligere justeringer og optimeringer i en iterativ design proces. I den forbindelse er det afgørende at kunne udvikle simple og kompakte modeller, der kan beskrive den elektriske og termiske studere opførslen af et givet design. Selvom numeriske metoder såsom Finite Element Method (FEM) er særdeles velegnet til at undersøge fysikken i effektelektronik, så er de tidskrævende og kræver omfattende computerberegninger, når de skal anvendes til DFR. Derfor er der i denne afhandling fokus på at udvikle nøjagtige, simple og bredt anvendelige modeller, der kan anvendes til at undersøge og vurdere den termiske og elektriske opførsel i effektelektroniske kredsløb (specielt høj-effekt moduler)

I afhandlingen undersøgelses forskellige effektelektroniske kredsløbs topologier, hvor der fokuseres på at reducere antallet af aktive komponenter og øge effektiviteten af topologien. Adskillige effektelektroniske omformer topologier diskuteres og sammenlignes med alternative løsninger i forhold til energitab og effektivitet. Baseret på erfaringerne med udfordringerne og begrænsningerne, som er forbundet med FEM simuleringer til at estimere pålidelighed, foreslås en model, som er baseret på et 3-dimensionelt simpelt termisk netværk, der kan anvendes til en hurtig, nøjagtig og detaljeret estimering af temperature i effekt moduler under forskellige testbetingelser. Da køling er specielt vigtigt for effektelektronik, behandles dernæst design af effektive kølesystemer. Køling ved hjælp af direkte kontakt med kølevæsker er mere effektivt end luftbaserede kølesystemer og de anvendes i til afhandlingen køling af effektmoduler.

Som det sidste emne præsenteres undersøgelser af parasitiske komponenter i effekt moduler med adskillige effektelektroniske komponenter. Ved at øge switch-frekvensen, kan størrelsen af de passive komponenter i omformerne reduceres, hvilket muliggør en øget effekttæthed og en lavere pris. Men dette leder samtidigt til en øget udfordring for de kompakte kredsløb med mange komponenter i forhold til de parasitiske komponenter, der bliver betydningsfulde ved højere frekvenser. For at imødegå dette er der udviklet modeller der ud fra micro-strip strukturerer kan bestemme de parasitiske parametre i forskellige layouts og som derved kan optimeres i forhold til dette hensyn.

En række af de modeller, der er præsenteret i afhandlingen, er blevet testet og verificeret i forhold til numeriske FEM simuleringer og eksperimentelle resultater udviklede. Modeller for energitab, termiske køling og de parasitiske elektriske parametre er bredt anvendelige og kan anvendes i kredsløbssimulerings-programmer eller andre programmeringsværktøjer. Modellerne er vigtige elementer i designprocesser målrettet med bedre pålidelighed eller forøgelse af virkningsgraden i effektelektronik. De kan spare tid og penge i udviklingen af nye designs til fremstilling af effektelektroniske enheder og kan bruges til at vurdere produkterne under typiske, atypiske og sågar ekstreme anvendelser

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Chapter 1
Introduction

This chapter presents the background, motivation and organization of the work presented in this thesis. The state of the art approaches in reliable design of power electronics are discussed and future trends and requirements for design tools will be explained. Finally, the objectives and structure of this thesis are outlined.

1.1 Introduction and background

1.1.1 Reliability of power electronics

The increasing demand for electrical energy, exhausting fossil energy reserves and the increase in energy prices have necessitated the use of current energy resources in a more efficient way. Power electronic converters are finding increased use as the essential equipment to convert and control electrical power in the wide power range from milliwatts to gigawatts with the help of power semiconductor devices [1].

Today, more than 70% of all electricity is processed through power electronics; therefore, highly efficient, sustainable, reliable and cost-effective power electronic systems are needed to reduce the waste of energy, to improve power quality and also to reduce costs in power generation, power transmission/distribution and end-user application [2]. As the power densities are increasing, the challenges for the reliability of power electronic systems have been more significant. For example, in one project [3], 290 cases of failures of wind turbines produced by different manufacturers were studied. In this study, 31,500 downtime events showed the second most significant contribution of 12% was caused by power electronics.

Thermal management, exposure to moisture, vibration, dust, chemicals, high voltage and deformation caused by temperature are important parameters since power electronic converters are often applied in harsh environments. The mission profiles for the converters exposed to these stressors should be known and taken into account during the design process to predict the lifetime of the converter. Today industries may use standard handbook calculation for each component in order to design the power

electronic system and with a low risk of failure rating, which may overrate the system in a costly way. However, standard handbooks do not show the root cause of failures in the optimization process of the products [4]-[9]. To solve these problems, design tools based on physics of failure methods should be developed in order to promote the industries enhancing the reliability of their power electronics converters.

In recent years, the reliability of power electronic systems has attracted more attention. The development of power electronics demands higher efficiency, stability and reliability. On the other hand, it demands also less weight, volume and cost (Fig. 1.1). In applications such as smart grid or renewable energy systems, the reliability of power electronic systems is very important, since the power system is always in operation and the power electronic converter plays a vital rule to produce the power to the grid. Moreover, in application such as powertrains, traction systems or other harsh environments, the life time of power electronic devices and circuits is a major performance factor considered in the design process [5].

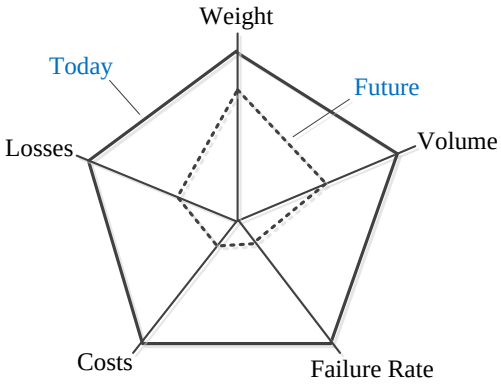

Fig. 1.1. Important performance indexes of power electronic systems and future design requirements .

1.1.2 **Concept of design for reliability**

Today, power electronics is experiencing the development of reliability from classic handbook-based reliability prediction and qualification testing to a systematical Design for Reliability (DFR) approach [10]. The related research works have been directed in analyzing various reliability aspects [11]-[15]. In order to analyze the reliability of power electronic systems, mathematical models to predict reliability are needed. Many

efforts have been directed to develop mathematical and simulation models at component-level for studying electrical, electro-thermal and thermo-mechanical behaviors [16], [17]. Besides, many significant methodologies have been proposed to develop system-level models in order to achieve a predictable lifetime models for power electronic systems [18]-[19].

However, the design tools used for improving the reliability of power electronic systems are not at an acceptable level for the following reasons [4]:

I. The DFR approach is not considered in state-of-the-art cases. Power electronic systems have a wide range of specific failure mechanisms as well as complicated mission profiles, and the design tools are not customized for power electronics.

II. The bathtub curve [4], which shows the failure rate of a device or system as a function of time, divides the life time of a device or system into three periods: Burn-in, Useful Life, and Wear-out (Fig. 1.2). The limitations of the curves are that: 1) the assumption of constant failure rate during useful life is not valid for many application cases, and 2) the wear out of power electronic components could start since the beginning of the operation.

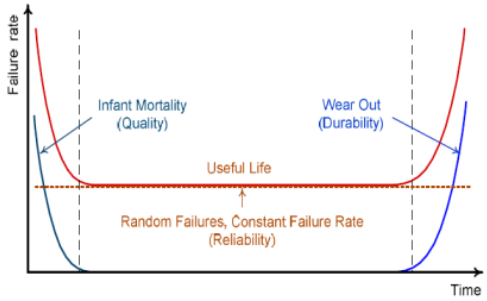

Fig. 1.2. Typical failure rate curve as a function of time (bathtub curve).

III. Most industries use models based on reliability handbooks to design their products and predict the failure rates in power electronic systems. However, handbooks do not consider temperature cycling, combined environments, failure rate changes with material and the quality or technology, which is used in the product. Moreover, the models addressed in handbooks do not indicate the root causes of a failure to improve the reliability of the device or the system.

When a product is used, the performance of the product will wear out over time (Fig. 1.3) [4]. Only the performance improvement will be obtained by assigning optimal values to the parameters in the design stage. In other words, the reliability of a system can be enhanced by comprehensive multi-objective optimization of the system [5]. A diagram for optimization process in a power electronic system design is shown in (Fig. 1.4).

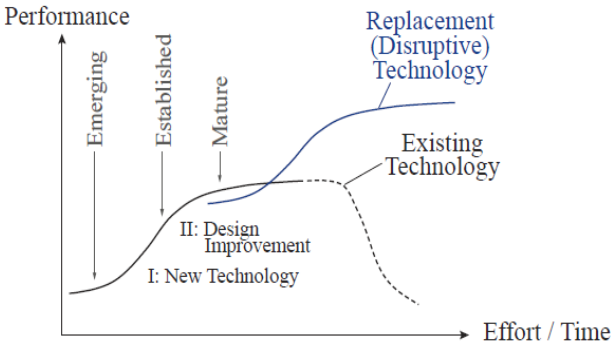

Fig. 1.3. Product performance as a function of time.

1.1.3 **Design tools for power electronics**

In order to optimize the system reliability of a power electronic circuit, first a comprehensive mathematical model must be established. This model can be a design tool, which includes thermal, electrical and mechanical models of the system. This tool could be based on component and circuit equations, on numerical simulations or both of them. Equation-based models can provide fast analysis of the system. These equation-based models are easy to use and time-efficient, but the accuracy of the final result is highly dependent on the accuracy of the component-level models, which is a great challenge. This is particularly true when using new power electronic devices, topologies or e.g. modulation techniques. Furthermore, simulation-based models are completely flexible, but may need strong computational efforts.

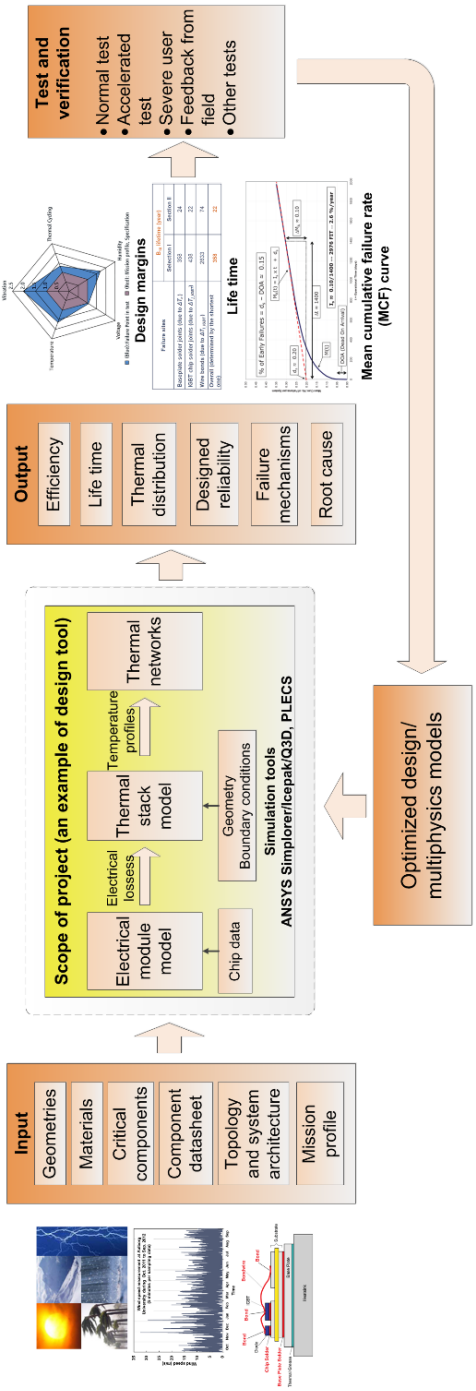

Fig. 1.4. A diagram illustrating a reliability-driven design process of a power electronic converter.

The behavior of the power electronic system could be predicted by applying the design tool. This tool can include junction temperature of components, thermo-mechanical stresses, and electrical parasitics in the circuit as well as the life-time of the power electronic circuit. In addition, this tool enables the reduction in time and cost of the system development, since the design tool can be implemented in software models instead of hardware. Besides, the failure mechanisms caused by component temperatures and mechanical stresses could be identified in the early design stage for various mission profiles such as overvoltage, overload, short-circuit, wind speed, solar irradiance, etc. without building complicated and expensive prototypes for the applications such as renewable energy systems, hybrid or electric vehicles.

Furthermore, using a design tool enables the design engineers to study the effect of parameter variations on the whole converter system. In this way, the variation could be held by multiple objectives, e.g. increase the efficiency together with power density in the state of keeping the costs as low as possible. Moreover, different converter topologies could be compared and the performance limitations of various topologies identified. The circuit models developed in the design tools have to be accurate and reliable for a wide range of operating conditions, such as temperature or load. In addition, the design models must be easy to be uses for design engineers to set up and to parameterize.

Power electronic devices and systems are affected by various stressors, such as temperature, overvoltage, overload, vibration, Electro-Magnetic Interference (EMI), humidity, etc. Therefore, the design process must include electrical, thermal, mechanical, fluid and control concerns within a multidisciplinary system. The design tool is a dynamic approach for the reliability problem and the design challenge. In this process, a simulation tool can be used, which incorporates multiple and integrated physics. The design tool will be developed by using electrical and thermal models based on a multiphysics simulation environment based on Finite Element Method (FEM).

One possible solution for multiphysics simulation at circuit level is ANSYS [20]. This software platform allows the analysis of all aspects of large-scale systems in a

single simulation design environment. Various controllable electrical, thermal, fluid and mechanical components are integrated into the simulation environment to develop power electronic system. This software ensures that the components in the system will operate like a real-world environment. Furthermore, for component models requiring the highest level of accuracy, ANSYS can enable power electronic designers to incorporate detailed physics-based models and to design complex systems by integration with other softwares such as ANSYS Icepack®, ANSYS Q3D Extractor®, ANSYS Simplorer®, ANSYS Mechanical®, etc. Moreover, professional programs such as MATLAB SIMULINK, PLECS, SolidWorks, etc. can be incorporated into ANSYS, where their benefits are used. This feature allows the designer to use customized codes and existing control or feedback methods without time consuming model translation.

1.1.4 **Design of high power modules**

One of the most important issues that must be considered in the design process of power electronics is the characterization of devices including Insulated Gate Bipolar Transistor (IGBT) power modules. A power module is a physical package containing several power semiconductor devices that are typically soldered or sintered on a power electronic substrate. In the present work, the focus is placed on high power modules. Today, high power modules are widely used in wind turbines, motor drives, electric ships and trains [3]. For cost reduction reasons, manufacturers attempt to fabricate power modules with less silicon area, which leads to higher power density. Besides, the device manufacturers try to integrate power semiconductors in a common substrate with bond-wire connectors to increase the power density of circuit. These technologies introduce several stressors to the entire power module which may seriously affect the reliability of the device. For example, adverse thermal/power cycling may cause fatigues like bond-wire lift-off or solder cracking due to Coefficient of Thermal Expansion (CTE) mismatch [21]. So, an accurate prediction of the chip temperature in normal/abnormal operations and optimized cooling system are necessary in order to ensure a reliable and cost-effective converter design. Moreover, in practical applications, electrical parasitics cause many failures in the power module. The stray

inductances exist in the power module: from the IGBT chip collector and emitter to the busbars. The parasitic inductance accumulates energy, when the current flows through the commutation paths inside the power module. When the switch is turned off, this energy is released as a voltage spike, which may lead to device failure if no external snubber capacitor exists in the current path. The parasitics eventually affect the Electro-Magnetic Interference (EMI), and efficiency of the circuit [22]. Therefore, reduction of electrical parasitics is important in the power module layout design, especially in high frequency, high power applications of power electronics.

In the conventional design of power modules, it is intended to place multiple chips in a package to reduce the electrical parasitics in the conductors. However, by integration of the chips and making a compact layout design, thermal management of the power module becomes a critical issue since higher temperature is produced. In simple words in order to reduce the parasitic effects the connector lengths which semiconductor chips are placed on them should designed smaller and chips should be place closer to each other, but this will increase the heat generated in the power module due to thermal coupling effects among the chips [23].

Conventionally power module manufacturers follow a predefined layout design process based on the circuit topology, required electrical rating and geometrical constraints. The geometrical constraints include minimum chip size and conductor area/thickness and thus the minimum isolation layer required to mount the conductors [23]. When an initial layout is designed, the electrical parasitic parameters and the power module temperature can be extracted by simple mathematical models or Finite Element based tools. Finally, to obtain an optimized solution, an iterative process is done to find the layout with minimum electrical parasitics as well as minimum temperature. However, iterations demand for time-consuming calculations that may not be efficient for a fast analysis of the design. Therefore, simple modelling tool is required to iterate the electrical parasitics and thermal analyses of different layout designs towards an optimized solution.

1.2 Hypothesis and objectives

Thermal analysis and electrical parastics extraction are important in the design process for reliable performance. In the conventional design process, thermal analysis is performed by FEM tools such as ANSYS Icepak, SolidWorks, Pro/ENGINEER, etc. Electrical parasitic extraction, on the other hand, is performed by electromagnetic field FEM solvers such as ANSYS Q3D. The computation cost needed in the mentioned tools seriously affect the designing time. Especially in the cases when power modules are loaded in long-term thermal cycling or abnormal operations such as short-circuit which demands for very short time steps to capture short electrical/thermal stresses. On the other hand, circuit simulators are convenient tools which can model the power electronic circuit behaviors by using equivalent electrical elements. So, the objectives of the present work are:

- How to apply different circuit simulators in order to model various converter topologies and to investigate different control strategies in order to increase the efficiency of the power electronic system.
- How to employ multiphysics FEM tools in order to study the physical behavior of high power modules and to understand better the reliability of power modules in real operating conditions.
- How to simplify modelling of high power modules and cooling system inside the FEM environment in order to increase the efficiency of simulations and develop simple models to be used for reliability study.
- How to develop methods to extract electrical parasitics in the multi-chip power modules.

By applying the developed models in an optimization system design tool, shorter design cycle, cost reduction and improved power electronic system can be obtained.

1.3 Thesis outline

Chapter 1 presents the introduction and motivation of the thesis, where the background, motivation and objectives of the thesis are addressed.

Chapter 2 studies several circuit topologies for high power applications to analyze different control strategies and circuit configurations in respect to the efficiency of the

converters and loading of individual devices. It consists of two parts; first different topologies of multi-level inverters will be analyzed and efficiency of the inverters will be compared. In this part manufacturer datasheets will be used to calculate the power dissipation. In the second part, reduced switch converters will be studied and the efficiency of converters will be compared in different energy conversion conditions using generic power dissipation models.

Chapter 3 explains the FEM modelling of power modules in both normal and abnormal operating conditions. The advantages and drawbacks of FEM simulations are first addressed. The concept of thermal coupling effect in power modules will be investigated and thermal design tools will be introduced for allocating power semiconductor chips. Finally, FEM simulations will be used to estimate the mechanical stress/strain in aged power module devices and short-circuit conditions

In chapter 4, an extensive study is devoted to develop simplified thermal model for high power modules. For this reason, 3D thermal network is constructed inside the power module in which critical temperature points are identified and assigned as nodes and lumped RC networks are constructed between the temperature points as branches. The main contribution of this 3D thermal network is identification of thermal coupling effects between chips and sublayers. In addition, the effect of boundary conditions on thermal modelling will be analyzed and modelled based on high power modules. Finally, the thermal model will be verified by FEM simulation and experimental testing.

In chapter 5, as another important factor in thermal management, cooling systems for power modules will be analyzed by means of FEM simulations. A design tool will be introduced to be applied for optimization of direct liquid cooling systems.

In chapter 6, the focus of the work is dedicated to electrical parasitics extraction of high power modules. The micro-strip transmission line method is employed to extract parasitic inductances in the multi-chip power modules. Also, a simplified index is presented to evaluate the parasitic inductances in different power module layouts. As a case study, parasitic parameters are extracted for a commercial SiC power module by means of mentioned method and the results are compared with FEM simulation results. Then by using parasitic reduction techniques, a reduced parastic power module is

designed and fabricated. The parasitic parameters of the optimized layout will be compared with parameters from a commercial power module.

In chapter 7, the conclusions and contributions of the thesis as well as potential suggestions for the future work will be given.

1.4 List of publications

The list of publications extracted from the work presented in this thesis is in the following:

Journal papers:

[P1] A.S. Bahman, K. Ma, P. Ghimire and F. Blaabjerg, "A Lumped Thermal Model Including Thermal Coupling and Thermal Boundary Conditions for High Power IGBT Modules," *IEEE Trans. Ind. Electron*, accepted with major revision.

[P2] A.S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A 3D Lumped Thermal Network Model for Long-term Load Profiles Analysis in High Power IGBT Modules," *IEEE J. Emerg. Sel. Topics. Power Electron*, to be published.

[P3] K. Ma, A. S. Bahman, S. Beczkowski, and F. Blaabjerg, "Complete Loss and Thermal Model of Power Semiconductors Including Device Rating Information," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2556-2569, May 2015.

[P4] Z. Qin, P. C. Loh, A. S. Bahman, and F. Blaabjerg, "Evaluation of current stresses in nine-switch energy conversion systems," *IET Power Electron.*, Vol. 7, No. 11, pp. 2877-2886, October 2014.

Conference proceedings:

[P5] A. S. Bahman, F. Iannuzzo, C. Uhrenfeldt, F. Blaabjerg and S. Munk-Nielsen "Prediction of Short-Circuit-Related Thermo-Mechanical Stress in Aged IGBT Modules," submitted to *ECCE 2016*.

[P6] A. S. Bahman and F. Blaabjerg, "Optimization Tool for Direct Liquid Cooling System of High Power Modules," submitted to *EPE 2016*.

[P7] A.S. Bahman, K. Ma, and F. Blaabjerg, "General 3D Lumped Thermal Model with Various Boundary Conditions for High Power IGBT Modules," accepted, *proc. of APEC 2016*.

[P8] A. S. Bahman, F. Blaabjerg, A. Dutta, and A. Mantooth, "Electrical Parasitics and Thermal Modeling for Optimized Layout Design of High Power SiC Modules," accepted, *proc. of APEC 2016*.

[P9] A.S. Bahman, K. Ma, and F. Blaabjerg, "A Novel 3D Thermal Impedance Model for High Power Modules Considering Multi-layer Thermal Coupling and Different Heating/Cooling Conditions," *in Proc. APEC 2015*, pp. 1209-1215, 2015.

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[P15] A. S. Bahman, and F. Blaabjerg, "Comparison between 9-level hybrid asymmetric and conventional multi-level inverters for medium voltage application," *in Proc. ISIE 2013*, pp. 1-7, 2013.

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Chapter 2

Power module applications in high power converters

As technology has evolved, industry has constantly been looking for methods to reduce the size and cost of power converters and also improving their reliability. This leads to the development of many new power converters and to invent new modulation methods, which so far, has focused on improving a few topological or performance features. This chapter deals with the application of alternative topologies and control strategies to increase the efficiency and reliability of power electronic converters. First alternative topologies and semiconductors will be used in multi-level inverters to increase the efficiency and then new topologies with reduced number of switches will be used to increase the efficiency in back to back converters.

2.1 Application of power modules in multi-level inverters

There is an increasing demand for multi-level inverter systems capable of providing high output voltage, good spectral performance and easy control. Examples of such systems are medium voltage drives, FACTS devices, HVDC transmission, and active power filters [1], [2]. Currently, medium voltage drives cover a power range from 0.2 MW to 100 MW at voltage levels from 2.3 kV up to 13.8 kV [2].

Nevertheless, the design of medium voltage drives encounters a number of challenges related to the topologies and control of the grid side converter (e.g. power quality, resonance, and power factor) and motor side converter (e.g. dv/dt, torque ripples, motor derating caused by generated harmonics and traveling wave reflections), as well as power semiconductor devices (semiconductor losses) [1]. Essential requirements for medium voltage drives are high efficiency, high reliability, low cost, low volume, and in some applications, high dynamic performance and regeneration capability [1].

Due to limitations in semiconductor voltage and current rating, it is difficult to connect a single semiconductor device directly to a medium voltage network. To overcome this problem, a family of multi-level inverters hav been introduced for medium voltage levels [3].

Multi-level inverters consist of power semiconductor devices and capacitors which generate voltages with stepped waveforms in the output. The DC-link in the input of multi-level inverters comprises of a capacitor, or a bank of capacitors. The switching schemes of semiconductor switch devices allow the inverter to generate higher stepped voltages by using more capacitors in the DC-link. However, most semiconductor devices cannot withstand high level of voltages to several kVs.

The large number of semiconductors in multi-level inverters has negative impact on the reliability and overall efficiency. However, using inverters with a low number of semiconductors requires large and expensive LC-filters to limit insulation stress on the motor windings, or can only be used in applications with motors that can withstand this stress [4]. As a result, there is significant effort to develop multi-level inverters with the same performance and less power devices.

Best known multi-level topologies include: the cascaded H-bridge, diode clamped and flying-capacitor multi-level inverters [5]-[7]. These classical solutions are called symmetric multi-level inverters, because they have the same voltage on each of the intermediate-circuit capacitors, and all the power semiconductors have to be capable to block the same voltage in their ‘off’ state. An asymmetric multi-level inverter has exactly the same circuit topology as the symmetric multi-level inverter – it differs only in the capacitor voltages. However, the properties of asymmetric multi-level inverters are quite different. Specifically, the number of output-voltage levels can be dramatically increased [8], [9]. Since the different cells of asymmetric inverters work with different DC-link voltages and different switching frequencies, it is more efficient to select various semiconductor devices that are appropriate for the conditions of each cell and thereby optimize the performance of the converter. These inverters are called “hybrid multi-level inverters” [10].

In this section, hybrid asymmetric multi-level inverter will be compared with conventional symmetric multi-level inverters in terms of harmonic distortion, power

losses and efficiency for the same output voltage rating. This section is organized into the following sub-sections: First, the structure of the multi-level inverter topologies is briefly described. Then, the inverter specifications, modulation techniques and performance indexes are investigated. Finally, the investigated topologies are compared and simulation results are presented.

2.1.1 **Multi-level inverter topologies**

- **Cascaded H-bridge multi-level inverter (CHB MI)**

A single phase 9-level cascaded H-bridge multi-level (9-L CHB ML) inverter is shown in Fig. 2.1. In this topology, the power cells are in series and the number of phase voltage levels that can be obtained at the converter terminals is proportional to the number of cells. Simply, the number of phase voltage levels at the converter terminals is *2N+1*, where *N* is the number of cells [3]. This topology has excellent input current and output voltage waveforms. The output voltage has smooth steps, so an output filter is usually not needed or in the case of need, it can be very small.

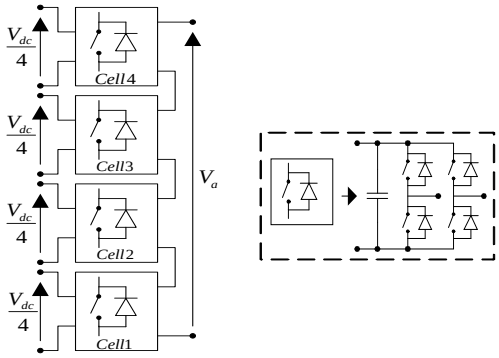


Fig. 2.1. 9-level Cascaded H-bridge multi-level inverter (9-L CHB MI) circuit.

- **Diode Clamped Multi-Level Inverter (DC MI)**

Fig. 2.2 shows a single phase of a 3-level diode-clamped multi-level inverter (3-L DC MI). In this topology, the semiconductor devices are connected in series and the dc-link is divided by smaller capacitors and connects to the switches by clamping diodes [11]. The clamp diode connections are necessary to block the current and their numbers in each leg are selected in such a way to have the same blocking voltage like the

switches. This topology has a simple circuit topology, but generates high and steep voltage steps, which may impact the life time of the motor windings as the dv/dt can be high. An additional filtering stage is therefore needed to reduce the ripple in the inverter output voltage.

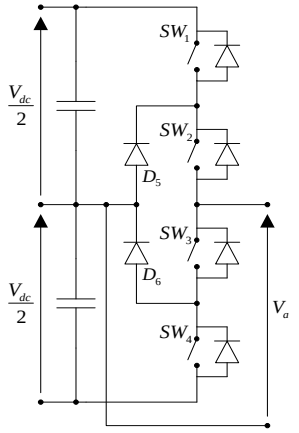


Fig. 2.2. 3-level Diode-clamped multi-level inverter (3-L DC MI) circuit.

- **Hybrid Asymmetric Multi-Level Inverter (HA MI)**

Fig. 2.3 shows the single phase circuit diagram of an asymmetric cascaded two-cell 9-level inverter (9-L HA MI), where the dc voltages for the H-bridge cells are not equal [12]. In the asymmetric topology, a High-Voltage (HV) cell, which has a higher voltage rating and operates at low switching frequency, is ideal for GTO/IGCT switches. GTO and IGCT are reliable devices providing a high blocking voltage [13], [14]. On the other hand, the Low-Voltage (LV) cell, which has a lower voltage rating and operates at high switching frequency, is ideal for IGBTs. IGBTs allow higher switching frequencies together with good performance at lower voltages [15]. By combining IGBT and GTO/IGCT in an asymmetric multi-level inverter, a hybrid inverter could be obtained by utilizing the benefits of two device technologies.

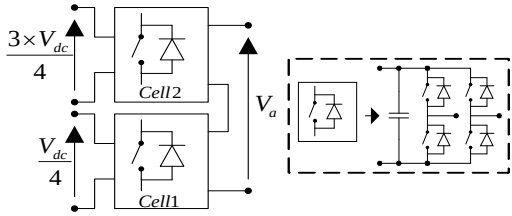


Fig. 2.3. 9-level Hybrid asymmetric multi-level inverter (9-L HA MI) circuit.

2.1.2 **Inverter specifications**

In this section both the inverter rating and specifications are chosen close to that of what is commercially available for medium voltage applications [16], [17]. Some commercial medium voltage drives, their power and voltage ratings and converter topologies with the semiconductor switches applied to them are summarized in Table 2.1.

Table 2.1. Commercial available medium voltage drives

Manufacturer	**Drive Model**	**Power (MVA)**	**Voltage (kV)**	**Topology**	**Semi-conductor**
Robicon	Perfect Harmony	0.3 – 0.31	2.3 – 13.8	CHB MI	LV IGBT
Allen Bradley	Power Flex 7000	0.15 – 6.7	2.3, 3.3, 4.16, 6.6	CSI	IGCT
Siemens	Masterdrive MV	0.66 – 9.1	2.2, 3.3, 4.16, 6.6	3-L Diode Clamped	HV IGBT
	Masterdrive ML2	0.66 – 9.1	3.3	3-L Diode Clamped	IGCT
ABB	ACS 1000	0.3 – 5	2.3, 3.3, 4	3-L Diode Clamped	IGCT
	ACS 5000	5.2 – 2.4	4.16, 6, 6.6, 6.9	Cascaded H-Bridge	IGCT
	ACS 6000	3 – 27	3, 3.3	3-L Diode Clamped	IGCT
Alstom	VDM 5000	1.4 – 7.2	2.3, 3.3, 4.2	2-L VSI	IGBT
	VDM 6000	0.3 – 8	2.3, 3.3, 4.2	3-L Flying Capacitor	IGBT
	VDM 7000	7 – 9.5	3.3	3-L Diode Clamped	GTO
General Electric	Dura-Bilt5 MV	0.3 – 2.4	4.16	3-L Diode Clamped	IGBT
	MV-GP Type H	0.45 – 7.5	3.3, 4.16	Cascaded H-Bridge	IGBT

The drive system under study is designed to supply an induction motor with line-to-line voltage of 4.16 kV, Nominal power of 500 kVA, output frequency of 50 Hz and power factor of 0.85. Table 2.2 summarizes the basic inverter data for the design of the main power part components.

Table 2.2. The basic specifications of inverter and induction motor for comparison

Inverter line-to-line voltage (RMS)	4.16 kV
Phase current	60 A
Nominal inverter output power	500 kVA
Power factor of motor	0.85
Nominal dc-link voltage	6353 V
Modulation technique	Optimized PD-PWM
Switching frequency	450 - 1050 Hz
Maximum junction temperature (IGBT, IGCT, diode)	125^{o}C

2.1.2.1 Modulation technique

The modulation technique employed in this system is Phase Disposition PWM (PD-PWM). The PD-PWM method is one of the carrier-based PWM methods, and the implementation is based on a comparison of a reference waveform with vertically shifted carrier waveforms [18]-[21]. This method uses *N-1* carrier signals to generate the *N*-level inverter output voltage. The injection of a 3rd harmonic into the reference waveforms will achieve a 15% increase in modulation index compared to sinusoidal PWM before over-modulation nonlinearities occur. This is simply because of the reduced height of the three-phase reference envelope that is achieved by 3rd harmonic injection [22]. In this technique, the 3rd harmonic is cancelled out in a three-phase system. This modulation technique is called Switching Frequency Optimized PD-PWM (SFO-PD-PWM) and it is shown in Fig. 2.4.

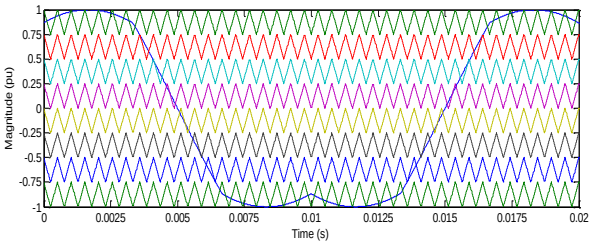


Fig. 2.4. Switching Frequency Optimized PD-PWM (SFO-PD-PWM) technique, reference and carrier signals.

2.1.2.2 DC-link voltage

The minimum dc-link voltage to achieve an output line-to-line voltage of 4.16 kV using SFO-PWM can be calculated by

$$\boldsymbol{V_{dc,min} = \sqrt{2} \, . \, V_{ll,rms} = \sqrt{2} \, . \, 4,16 \, kV = 5883 \, V} \tag{2.1}$$

where $V_{dc,min}$ is the minimum dc-link voltage and $V_{ll,1,rms}$ is the RMS value of the output line-to-line voltage. To determine the nominal dc-link voltage of the inverter, a voltage reserve of 8% is assumed (for the imperfections of the real system, control reserve, device voltage drops, etc.)

$$\boldsymbol{V_{dc,n} = 1,08 \, . \, V_{dc,min} = 1,08 \, . \, 5883 = 6353 \, V} \tag{2.2}$$

where $V_{dc,n}$ is the nominal dc-link voltage.

2.1.2.3 Power semiconductors selection

Table 2.3 and Table 2.4 summarize the design of the power semiconductors for the 4.16 kV inverter, assuming a switching frequency of 600 Hz in all topologies. The voltage V_{com} describes the commutation voltage of the corresponding commutation cells. $V_{com@100FIT}$ is an index for the maximum voltage that the semiconductor switch can withstand and is defined by the nominal voltage of the semiconductor for which it has a cosmic ray withstand capability of 100 FIT (one FIT is equivalent to one failure in 10^9 operation hours). The ratio of $V_{com}/V_{com@100FIT}$ represents a measure of the device voltage utilization for different topologies [23].

Table 2.3. Inverter voltage and semiconductor specifications in the conventional multi-level topologies

Topology	3L-DC MI	9L-CHB MI
Power devices	6.5 kV / 200 A FZ200R65KF2 INFINEON	1.7 kV / 200 A BSM200GB170DLC EUPEC
Nominal dc-link voltage	6353 V	794 V
Rated device voltage	6.5 kV IGBT	1.7 kV IGBT
Commutation voltage	3176 V	794 V
$\boldsymbol{V_{com@100FIT}}$	3600 V	900 V
$\boldsymbol{V_{com}}$ / $\boldsymbol{V_{com@100FIT}}$	0.88	0.88

Table 2.4. Inverter voltage and semiconductor specifications in the hybrid asymmetric topology

Topology	**9L-HA MI**	
	Main Inverter (IGCT)	Sub Inverter (IGBT)
Power devices	4.5 kV / 340 A 5SHX04D4502 /5SDF03D4502 ABB	1.7 kV / 200 A BSM200GB170DLC EUPEC
Nominal dc-link voltage	2382 V	794 V
Rated device voltage	4.5 kV IGCT	1.7 kV IGCT
Commutation voltage	2382 V	794 V
$V_{com@100FIT}$	2700 V	900 V
V_{com} / $V_{com@100FIT}$	0.88	0.88

2.1.3 **Performance indexes**

The performance indexes used in the comparison are: Total Harmonic Distortion (THD), First-order Distortion Factor (DF1), semiconductor power losses (conduction and switching losses) and the efficiency.

a. THD

The THD of the inverter can be calculated as:

$$\boldsymbol{THD}\% = \frac{\boldsymbol{100}}{\boldsymbol{V_1}} \sqrt{\sum_{\boldsymbol{h=2,3,\ldots}}^{\infty} \boldsymbol{V_h^2}} \tag{2.3}$$

where V_1 is the fundamental harmonic of the signal analyzed, h is the harmonic order, and V_h is the harmonic amount of order h.

2.1.3.1 DF1

In AC motor drive applications, the first-order Distortion Factor (DF1) which is the Weighted Total Harmonic Distortion (WTHD) is another considerable index. DF1 is defined by:

$$\boldsymbol{DF1}\% = \frac{\boldsymbol{100}}{\boldsymbol{V_1}} \sqrt{\sum_{\boldsymbol{h=2,3,\ldots}}^{\infty} (\frac{\boldsymbol{V_h}}{\boldsymbol{h}})^{\boldsymbol{2}}} \tag{2.4}$$

The output phase and line voltage waveforms and their harmonic spectrum for the 9-level hybrid asymmetric multi-level inverter are shown in Fig. 2.5. It can be seen that

the harmonic content, especially in the low level orders are decreased compared to two-level inverters because of the increase in the number of output voltage levels.

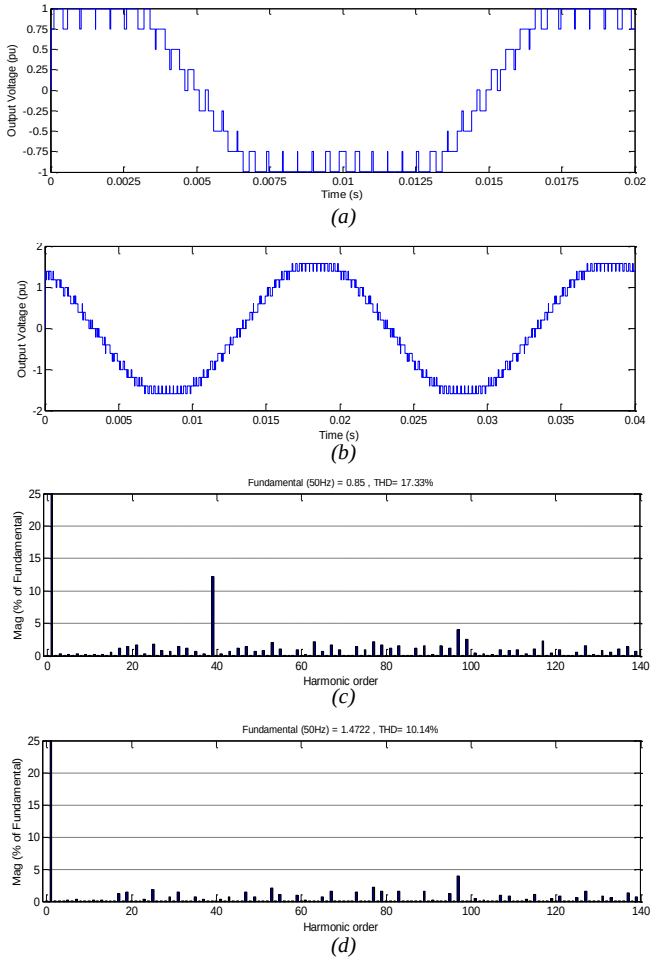


Fig. 2.5. Output voltage waveforms and harmonic spectrum for fundamental frequency 50 Hz: a) Output phase voltage, b) Output line voltage, c) Harmonic spectrum of output phase voltage, d) Harmonic spectrum of output line voltage.

2.1.3.2 Semiconductors power losses

The semiconductor power losses can be calculated from the curves ($v_{sat\times}\ I_{load}$) and ($E_{\times}\ I_{load}$), given in the datasheet of each device. In these curves the parameters are defined as: v_{sat}: The on-state saturation voltage (v_{ce} for the IGBT, v_T for the IGCT and v_F for the diode); E: The switching energy losses in one commutation (E_{on} for a turn-on

commutation, E_{off} for a turn-off commutation and E_{rec} for reverse recovery process); I_{load}: The load current. These curves are used in MATLAB to calculate the power losses. MATLAB uses the mathematical models that represent the functions $v_{sat}(i_{load})$ and $E(i_{load})$ for semiconductors. These models are obtained by extrapolation of curves extracted from datasheets and using the curve-fitting toolbox (*cftool*). Based on these mathematical models, the conduction and switching losses are calculated in each semiconductor device. The sum of switching and conduction power losses gives the total power losses.

- **Conduction losses**

The conduction power losses are calculated by (2.5) in the main switch and by (2.6) in the diode:

$$P_{cond_{SW}} = \frac{1}{T_{SW}} \int_0^{T_{SW}} v_{sat}(t) \,.\, i_{load}(t) . v_{cmd_{SWx}}(t) \,.\, dt \tag{2.5}$$

$$P_{cond_D} = \frac{1}{T_{SW}} \int_0^{T_{SW}} v_F(t) \,.\, i_{load}(t) . v_{cmd_{SWx}}(t) \,.\, dt \tag{2.6}$$

where T_{sw} is the switching cycle and v_{cmd} is the command signal of switch that can be 1 or 0. The total conduction power losses are calculated by (2.7):

$$\boldsymbol{P_{cond_{TOTAL}} = P_{cond_{IGBT/IGCT}} + P_{cond_D}} \tag{2.7}$$

- **Switching losses**

The turn on and the turn off power losses in the main switch are given by (2.8) and (2.9) and the reverse recovery power losses in the diode is calculated by (2.10) – for a given gate voltage:

$$P_{on} = \frac{1}{T} \sum E_{on}\big(i_{load}(t)\big) \,.\, f_{SW} \tag{2.8}$$

$$P_{off} = \frac{1}{T} \sum E_{off}\big(i_{load}(t)\big) \,.\, f_{SW} \tag{2.9}$$

$$P_{rec} = \frac{1}{T} \sum E_{rec}\big(i_{load}(t)\big) \,.\, f_{SW} \tag{2.10}$$

The total switching power losses are calculated by (2.11):

$$\boldsymbol{P_{SW_{TOTAL}} = P_{on} + P_{off} + P_{rec}} \tag{2.11}$$

Finally, the total power losses are the sum of all conduction and switching power losses and computed by (2.12):

$$\boldsymbol{P_{loss} = P_{cond_{TOTAL}} + P_{SW_{TOTAL}}} \quad (2.12)$$

Based on these mathematical models, the conduction and switching losses are calculated in each semiconductor device. The sum of the switching and the conduction power losses gives the total power losses.

2.1.4 **Comparison of different multi-level inverter topologies**

The comparison for the drive system explained in the previous section will be implemented in two ways: constant switching frequency and constant efficiency.

- **Comparison in the state of constant switching frequency (600 Hz)**

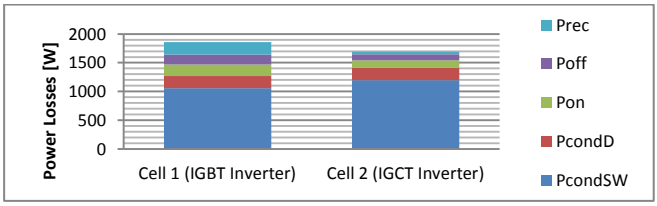
A switching frequency range of 450-1050 Hz is typical for available industrial medium voltage drives [17]. The switching frequency is assumed to be 600 Hz for the various topologies in this study. The performance indexes are listed in Table 2.5 and the power losses distributions for each topology are shown in Fig. 2.6.

According to Table 2.5, both the hybrid asymmetric and cascaded H-bridge inverters have the same THD for current and voltage, since they generate the same voltage levels. Compared with the other two topologies, the THD for the diode clamped inverter is about 3 times higher for the current and 3.8 times higher for the voltage. The THD of the voltage is higher than the current since the load is inductive and behaves as a filter. Similarly, the DF1 for the diode clamped is larger than the DF1 for the hybrid asymmetric and cascaded H-bridge inverters. This means that at a constant switching frequency, the harmonics of the output voltage appears at higher frequencies which are more damped by an inductive load. Moreover, power losses in the hybrid asymmetric topologies are lower, compared with both the cascaded H-bridge and the diode clamped inverters.

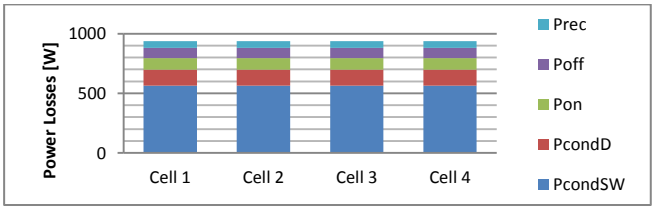
Considering the power rating of inverters, the hybrid asymmetric topology seems to show better performance in saving energy compared to other conventional topologies. As it can be seen in Fig. 2.6 (a), in the hybrid asymmetric inverter, the IGBT cell has the largest portion of power losses, as this cell operates at a higher switching frequency than IGCT cell, and therefore the switching losses increases. In

both of the cells the conduction power losses represent the most significant portion of the total losses. This is due to the fact that the switching frequency is low and all the switching devices commutate at a low switching frequency. Moreover, the RMS currents over the switches in the IGCT and IGBT inverters are 78 A and 72 A respectively – and consequently IGCT inverter has higher conduction losses than the other one.

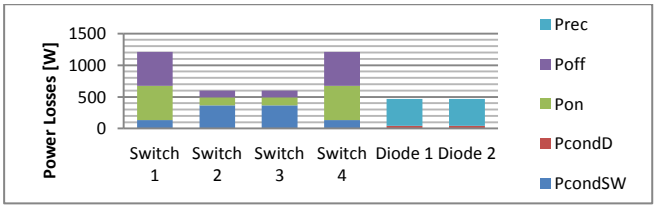
Fig. 2.6 (b) shows the power losses distribution in cascaded H-bridge inverter. In this topology, all the cells operate with the same switching frequency and dc-link voltages. Therefore, all cells show approximately the same semiconductor power losses. In the diode clamped inverter, Fig. 2.6 (c), the power losses are concentrated in switch 1 and switch 4. This occurs because switch 2 in the positive and switch 3 in the negative half cycles do not commutate to generate the zero voltage level. So, the conduction losses are the major of power losses in these switches. In diodes, most of power losses are related to switching losses, since these diodes block the current in all the switches commutations as well as conducting functions.



(a)



(b)



(c)

Fig. 2.6. Power loss distribution at constant frequency (600 Hz) with the test conditions given in Table 2.3 and Table 2.4 (a) Hybrid asymmetric 9-level inverter (b) Cascaded H-bridge 9-level inverter (c) Diode clamped 3-level inverter.

Table 2.5. Comparison of Multi-Level Inverter Topologies at Constant switching Frequency

Comparison	**Constant Switching Frequency (600 Hz)**		
Topologies	**Hybrid Asymmetric 9-Level**	**Cascaded H-bridge 9-Level**	**Diode-Clamped 3-Level**
Total number of devices/phase	4 IGBT Modules + 4 IGCT/Diodes	16 LV-IGBT Modules	4 HV-IGBT Modules + 2 Diodes
Number of phase-voltage levels	9	9	3
Number of line-voltage levels	17	17	5
THD of phase-current [%]	5.09	5.21	15.36
THD of line-voltage [%]	7.51	7.52	31.6
DF1 of line-voltage [%]	0.47	0.48	10.21
Total power losses [W]	3552	3893	4544
Inverter Efficiency [%]	99.29	99.22	99.09

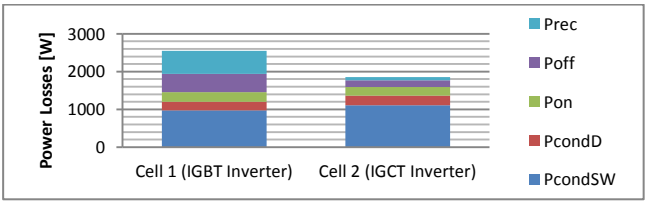
- **Comparison in the state of constant efficiency (99%)**

To evaluate the three designed topologies for different applications with a demanded efficiency, it is assumed that the inverter efficiencies for all of topologies are about 99% at a constant inverter power of 500 kVA. This efficiency is typical for state-of-the-art medium voltage drives [12]. Since the conduction losses of the switches are dependent to the average values of voltage and current of switches, by controlling the switching frequencies, the efficiency of 99% can be obtained. The performance indexes for this comparison are listed in Table 2.6 and the power losses distributions are shown in Fig. 2.7.

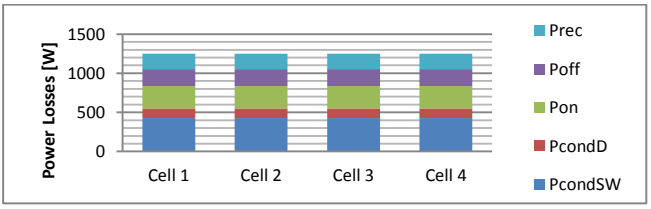
Compared to the constant frequency state, with an increase in the switching frequencies, the THD values of the current and voltage do not change significantly. This fact is due to the topologies and the output voltage levels are remaining unchanged. Instead, since the frequency of the first harmonic band directly affects the DF1, the first distortion factor is decreased. This can be seen especially in the hybrid asymmetric topology that by increasing the switching frequency to 5400 Hz, DF1 is reduced by 93%. In the cascaded H-bridge with the switching frequency of 800 Hz and diode-

clamped with the switching frequency of 1150 Hz, the reductions of DF1 are approximately 79% and 48%. These values of DF1 indicate that the output filter of the diode-clamped and cascaded H-bridge inverters will have greater volume, weight, and cost than the filter used in the hybrid asymmetric inverter to obtain the same line voltage distortion.

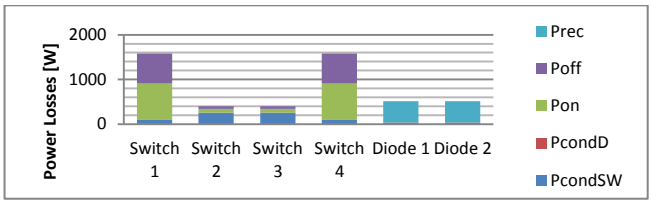
On the other hand, considering the power losses distribution in the hybrid asymmetric topology, the switching losses are the major part of the power losses in cell 1 (IGBT inverter). This increase of switching losses comparing to the previous case (switching frequency of 600 Hz) shows that in the hybrid asymmetric topology the switching frequency affects the IGBT inverter switching losses more than the IGCT inverter, since it works with higher switching frequency. In addition, in the state of operation at the same efficiency in the three topologies, the frequency of carrier signals in the hybrid asymmetric topology is about 6.2 times of cascaded H-bridge and 4.7 times of diode-clamped topology. It shows more relevance of this topology compared to the switching frequency that in practice limits the increase of switching frequency up to 1000 Hz.



(a)



(b)



(c)

Fig. 2.7. Power loss distribution in equal efficiency (99%)) with the test conditions given in Table 2.3 and Table 2.4 (a) Hybrid asymmetric 9-level inverter (b) Cascaded H-bridge 9-level inverter (c) Diode clamped 3-level inverter.

Table 2.6. Comparison of Multi-Level Inverter Topologies at Equal Efficiency

Comparison	**Equal Efficiency (99%)**		
Topologies	**Hybrid Asymmetric 9-Level**	**Cascaded H-bridge 9-Level**	**Diode-Clamped 3-Level**
Total number of devices/phase	4 IGBT Modules + 4 IGCT/Diodes	16 LV-IGBT Modules	4 HV-IGBT Modules + 2 Diodes
Number of phase-voltage levels	9	9	3
Number of line-voltage levels	17	17	5
Switching frequency [Hz]	5400	860	1150
THD of phase-current [%]	1.73	5.02	15.84
THD of line-voltage [%]	6.6	6.78	32.3
DF1 of line-voltage [%]	0.037	0.102	5.338
Total power losses [W]	4897	4999	4982
Inverter Efficiency [%]	99.01	99.01	99.01

2.2 Application of power modules in reduced switch converters

Besides to development of more efficient multi-level inverter topologies, one of the popularly pursued features is to reduce the number of components needed in the converters. For passive components, the commonly mentioned example will probably be the ac-ac matrix converters, where no bulky dc-link capacitors are needed [24]. Matrix converters are thus referred to as “all-semiconductor” even though a clamping capacitor is still needed in practice. The development in matrix converters has subsequently been progressed to the indirect type [25], where a fictitious dc-link has been introduced, but no large dc-link capacitor is used. This progress allows active switches to be reduced, leading to sparse matrix converters to be proposed in [26].

Indeed, reducing of the active switches is helpful since it also removes some accompanying gate circuits, and hence minimizes the chances of short-circuit and open-circuit failures caused by electromagnetic interferences. Many more reduced-switch converters are thus proposed over the years with most having the voltage-source characteristics. A common example is the B4 converter [27], which uses four switches to form two phase-legs. The third phase-leg is then drawn out from the middle of a split dc-link capacitor. The B4 converter thus saves two switches compared to the standard six-switch converter. The same reduction of switches can be performed when two six-switch bridges are connected back-to-back to form an ac-dc-ac converter. An example, which saves two switches, is discussed in [28], where the five-leg converter is proposed. Based on slightly different topological principles, a more recent example can be found almost simultaneously in [27] and [29], where the nine-switch converter is proposed to save three switches. The nine-switch converter has since then been tested for single and dual motor drives [28], [30], uninterruptable power supplies [29] and unified power quality conditioners [31] with its performance noted to be not always satisfactory for some of them [30]. This is no doubt linked to the performance constraints introduced by its reduced switch count, which are also experienced by other reduced-switch topologies. It is hence important to study the nine-switch converter with more details before appropriate application areas can be identified for it to benefit from its reduced switch feature, while not being burdened by its performance constraints. For that, the loss generation of the nine-switch converter is now compared with its twelve-switch back-to-back equivalence.

2.2.1 **Operational principle of nine-switch converter**

As seen in Fig. 2.8, the nine-switch converter is formed by three phase-legs with three switches each. It therefore saves three switches (or 25% depending on how many phase-legs are required), as compared to its twelve-switch equivalence as shown in Fig. 2.9.

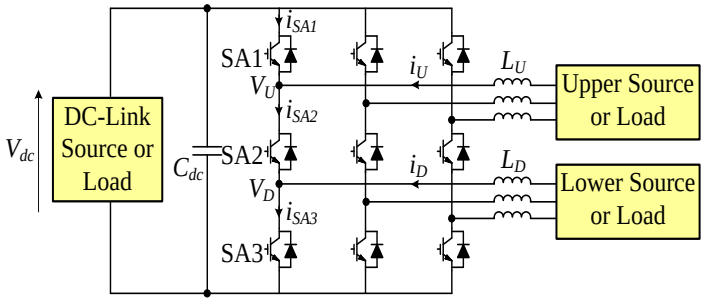


Fig. 2.8. Nine-switch converter with two three-phase loads.

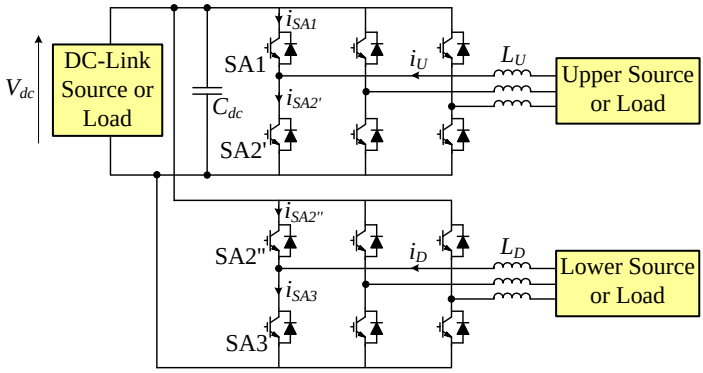


Fig. 2.9. Twelve-switch back-to-back converter with two three-phase loads.

However, using fewer switches introduces a constraint to the nine-switch converter, as demonstrated in Table 2.7, where the fourth state of $V_{A\_UP} = 0$ and $V_{A\_DN} = V_{dc}$ cannot be generated. In terms of modulation, it means the sinusoidal reference used for the upper terminal must always be placed above that of the lower terminal, as illustrated in Fig. 2.10. Moreover, the instantaneous current expressions for half a carrier period are shown in Fig. 2.11. Phase-shift between the two references is therefore limited if they have the same frequency and their amplitudes summed to be greater than that of the triangular carrier. On the other hand, if their frequencies are different, their total amplitude must always be smaller than the carrier amplitude. These constraints simply mean that the application of the nine-switch converter should be studied carefully, before real saving can be concluded to be gained from its fewer switches.

Table 2.7. Operating States of Nine-Switch Converter

Switch State	Voltage
S_{A1} = S_{A2} = ON and S_{A3} = OFF	$V_{A\_UP} = V_{dc}$ and $V_{A\_DN} = V_{dc}$
S_{A1} = S_{A3} = ON and S_{A2} = OFF	$V_{A\_UP} = V_{dc}$ and $V_{A\_DN} = 0$
S_{A2} = S_{A3} = ON and S_{A1} = OFF	$V_{A\_UP} = 0$ and $V_{A\_DN} = 0$
Fourth combination of $V_{A\_UP} = 0$ and $V_{A\_DN} = V_{dc}$ cannot be realized.	

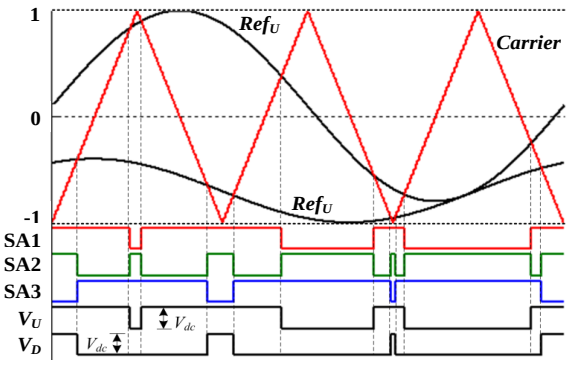


Fig. 2.10. Modulation of nine-switch converter with two output phases.

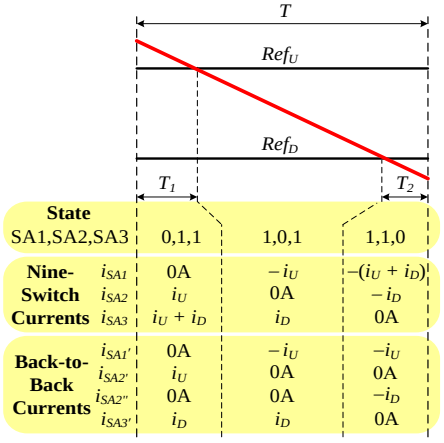


Fig. 2.11. Instantaneous switch current expressions.

2.2.2 **Loss modelling and computation**

Losses in the switches include conduction and switching losses, which can be computed using models describing specific switches or the generic model found in [32].

Since the aim here is to show the relative merits between the two converters without biasing of specific switches, the generic model is deemed as appropriate. The loss expressions are given as follows.

- **Conduction losses**

Conduction losses produced by switch SA1 in a phase-leg of the nine-switch converter can be computed using (2.20) based on the current notations used in Fig. 2.8 and Fig. 2.11. The same computation can be repeated for the other two switches and two phases. The other expressions can be found in [33].

$$\boldsymbol{P_{Con_{SA1}}} = \sum_{\epsilon=1\rightarrow f_{SW}} \left\{ 2\left(\begin{pmatrix} \boldsymbol{k_1 V_{Tran_{On}}} \\ \boldsymbol{+(1-k_1) V_{Diode_{On}}} \end{pmatrix} |\boldsymbol{i_U}| (\boldsymbol{T - T_1 - T_2}) + \begin{pmatrix} \boldsymbol{k_3 V_{Tran_{On}}} \\ \boldsymbol{+(1-k_3) V_{Diode_{On}}} \end{pmatrix} |\boldsymbol{i_U + i_D}| \boldsymbol{T_2} \right) \right\}_{\epsilon} \tag{2.20}$$

$$\boldsymbol{k_1} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_U \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_U > 0} \end{cases}, \boldsymbol{k_2} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_D \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_D > 0} \end{cases}, \boldsymbol{k_3} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_U + i_D \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_U + i_D > 0} \end{cases}$$

where $P_{Con_{SA1}}$ is conduction losses produced by SA1, V_{Tran_On} and V_{Diode_On} are respectively the on-state voltages of the transistor and diode in a switch, T, T_1 and T_2 are time intervals shown in Fig. 2. 11, i_U and i_D are currents flowing through the upper and lower terminals.

The corresponding expression for switch SA1′ of the equivalent twelve-switch converter can also be written as (2.21) based on the notations used in Fig. 2.9 and the current expressions shown in Fig. 2.11. The same computation can be repeated for the other two switches and two phases in the nine-switch converter.

$$\boldsymbol{P_{Con'_{SA1}}} = \sum_{\epsilon=1\rightarrow f_{SW}} \left\{ 2\left(\begin{pmatrix} \boldsymbol{k_1 V_{Tran_{On}}} \\ \boldsymbol{+(1-k_1) V_{Diode_{On}}} \end{pmatrix} |\boldsymbol{i_U}| (\boldsymbol{T - T'_1}) \right) \right\}_{\epsilon}$$
$$\boldsymbol{k_1} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_U \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_U > 0} \end{cases} \tag{2.21}$$

where $P_{Con_{SA1}}$ is conduction losses produced by SA1′ and T'_1 is the equivalent time interval to T_1 in twelve-switch converter.

- **Switching losses**

The switching losses of the nine-switch converter can be computed using (2.22). Assuming that the switching frequency is high and the current values in a switching period are nearly constant, the expressions for computing switching losses of the equivalent twelve-switch converter is given in (2.23).

$$P_{SW_{SA1}} = \sum_{\epsilon=1\rightarrow f_{SW}} \left\{ \frac{1}{2} V_{dc} |i_U| \begin{pmatrix} k_1\left(t_{Tran_R} + t_{Tran_F}\right) + \\ (1-k_1) t_{Diode_F} \end{pmatrix} \right\}_{\epsilon} \tag{2.22}$$

$$k_1 = \begin{cases} 1, & i_U \leq 0 \\ 0, & i_U > 0 \end{cases}$$

$$P_{SW\_SA1'} \approx \frac{V'_{dc}}{V_{dc}} P_{SW\_SA1}, \tag{2.23}$$

Where V_{dc} and V'_{dc} are the dc-link voltages for the nine-switch and twelve-switch converters respectively, t_{Tran_R} and t_{Tran_F} are the rise-time fall-time of the switch in commutation respectively and t_{Diode_F} is the fall-time of the free-wheeling diode in commutation.

- **Difference in losses**

To simplify the expressions for an easier understanding, the switching instants of the two converters are assumed to be the same. That means $T_1 \approx T'_1$ and $T_2 \approx T'_2$, which are approximately the case at high nominal modulation conditions. Differences in conduction losses for the two converters can hence be written as (2.24).

$$\begin{aligned} \Delta \boldsymbol{P_{Con\_SA1}} &= \boldsymbol{P_{Con\_SA1}} - \boldsymbol{P_{Con\_SA1'}} \\ &\approx \sum_{\epsilon=1\rightarrow f_{SW}} \left\{ 2\boldsymbol{T_2} \left(\begin{pmatrix} {}_3\boldsymbol{V_{Tran_{On}}} \\ +(\boldsymbol{1}-\boldsymbol{k_3})\boldsymbol{V_{Diode_{On}}} \end{pmatrix} |\boldsymbol{i_U} + \boldsymbol{i_D}| \right. \right. \\ &\quad \left. \left. - \begin{pmatrix} \boldsymbol{k_1 V_{Tran_{On}}} \\ +(\boldsymbol{1}-\boldsymbol{k_1})\boldsymbol{V_{Diode_{On}}} \end{pmatrix} |\boldsymbol{i_U}| \right) \right\}_{\epsilon} \end{aligned} \tag{2.24}$$

$$\boldsymbol{k_1} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_U \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_U > 0} \end{cases}, \boldsymbol{k_2} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_D \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_D > 0} \end{cases}, \boldsymbol{k_3} = \begin{cases} \boldsymbol{1}, & \boldsymbol{i_U + i_D \leq 0} \\ \boldsymbol{0}, & \boldsymbol{i_U + i_D > 0} \end{cases}$$

where ΔP_{Con_SA1} is the difference in conduction losses of SA1 for the two converters.

Although this is certainly not the case in practice, but for simplifying the analysis further, V_{Tran_On} and V_{Diode_On} are assumed to be equal ($= V_{On}$). Equation (2.24) then becomes (2.25).

$$\Delta \boldsymbol{P_{Con\_SA1}} \approx \sum_{\epsilon=1\rightarrow f_{SW}} \{\boldsymbol{2V_{On}T_2}(|\boldsymbol{i_U}+\boldsymbol{i_D}|-|\boldsymbol{i_U}|)\}_{\epsilon} \tag{2.25}$$

It is thus clear that the differences in conduction losses between the two converters are solely dependent on their relative current magnitudes and time durations (T_1 and T_2) in each switching period. The corresponding differences in the switching losses can also be determined as (2.26), from which it can be seen that the differences in losses can be minimized by lowering the dc-link voltage of the nine-switch converter, whenever possible.

$$\Delta \boldsymbol{P_{SW\_SA1}} = \boldsymbol{P_{SW\_SA1}} - \boldsymbol{P_{SW\_SA1'}} \approx \left(\boldsymbol{1}-\frac{\boldsymbol{V'_{dc}}}{\boldsymbol{V_{dc}}}\right)\boldsymbol{P_{SW\_SA1}} \tag{2.26}$$

where ΔP_{SW_SA1} is the difference in switching losses of SA1 for the two converters.

Equations (2.25) and (2.26) can subsequently be used for analyzing energy conversion systems and these are discussed next.

2.2.3 **Same frequency operation (AC-AC and DC-DC)**

The same frequency operation includes both ac-ac and dc-dc energy conversion systems with the latter being a simplified case of the former at zero frequency. The modulating references used for operating them can hence be summarized as:

$$\begin{aligned} \boldsymbol{Ref_U} &= \boldsymbol{M_U cos(\omega t)} + \boldsymbol{M_{oU}} + \boldsymbol{M_{Tri\_U}}, \\ \boldsymbol{Ref_D} &= \boldsymbol{M_D cos(\omega t + \varphi)} - \boldsymbol{M_{oD}} + \boldsymbol{M_{Tri\_D}} \end{aligned} \tag{2.27}$$

where Ref_U and Ref_D are modulating references for upper and lower terminals respectively, $0 \le M_U \le 1$ and $0 \le M_D \le 1$ are the modulation ratios, M_{Tri_U} and M_{Tri_D} are triplen offsets added to gain a 15% extension of the linear modulation range in a three phase system, and M_{oU} and M_{oD} are constant offsets added to ensure that Ref_U is always above Ref_D. Applying the expression of (2.25) to this operating mode then shows that a reduction in conduction losses can always be achieved by the nine-switch converter if (2.28) is satisfied, regardless of the values of T_1 and T_2.

$$|\boldsymbol{i_U}+\boldsymbol{i_D}| \le |\boldsymbol{i_U}| \quad \text{and} \quad |\boldsymbol{i_U}+\boldsymbol{i_D}| \le |\boldsymbol{i_D}| \tag{2.28}$$

For the case of the converter supplying sinusoidal currents at the fundamental frequency, (2.28) can further be expressed as (2.29).

$$\begin{cases} \boldsymbol{I_U^2}+\boldsymbol{I_D^2}-\boldsymbol{2I_DI_Ucos(180^\circ-\theta)} \le \boldsymbol{I_D^2} & \boldsymbol{if\ I_D \le I_U} \\ \boldsymbol{I_U^2}+\boldsymbol{I_D^2}-\boldsymbol{2I_DI_Ucos(180^\circ-\theta)} \le \boldsymbol{I_U^2} & \boldsymbol{if\ I_U \le I_D} \end{cases} \tag{2.29}$$

where $\boldsymbol{i_U = I_U cos(\omega t + \theta_U)}$ and $\boldsymbol{i_D = I_D cos(\omega t + \theta_D)}$

$$\Rightarrow \begin{cases} |\boldsymbol{I_U/I_D}| \leq \boldsymbol{2cos(180° - \theta)} & \boldsymbol{if\ I_D \leq I_U} \\ |\boldsymbol{I_D/I_U}| \leq \boldsymbol{2co(180° - \theta)} & \boldsymbol{if\ I_U \leq I_D} \end{cases}, \boldsymbol{\theta = \theta_U - \theta_D}$$

where θ_U and θ_D are the phase current angle of upper and lower terminals.

For the ideal case of $\theta = 180°$ and $|i_U| = |i_D|$ (*one terminal absorbing and the other supplying power*), currents through SA1 and SA3 of the nine-switch converter will be cancelled, hence generating zero conduction losses during T_1 and T_2. The switching losses of the nine-switch converter are also not increased under same frequency operation, since its dc-link voltage can remain the same as its twelve-switch equivalence. This can clearly be seen from (2.26) after setting $V_{dc} = V'_{dc}$.

2.2.4 **Different frequency operation (AC-DC, DC-AC and AC-AC)**

Different frequency operation includes ac-dc, dc-ac and ac-ac conversion, which will be analyzed sequentially as follows.

- **AC-DC conversion**

Modulating references used for ac-dc conversion are summarized in (2.30), from which the expressions for T_1 and T_2 are also derived. Also included in (2.30) are the ac and dc currents that are assumed to flow into the converter.

$$\begin{gathered} \boldsymbol{Ref_U = M_U cos(\omega t) + M_{oU} + M_{Tri\_U}, Ref_D = -M_{oD},} \\ \boldsymbol{T_1 = 0.5T(1 - Ref_U), T_2 = 0.5T(1 + Ref_D)} \\ \boldsymbol{i_U = I_U cos(\omega t + \theta_U),\ \ i_D = I_D} \end{gathered} \tag{2.30}$$

Clearly, T_1 is time-varying, while T_2 is fixed and should be kept small to keep V_{dc} of the nine-switch converter closer to V'_{dc} of the twelve-switch converter in order to minimize the switching loss differences in (2.26) [34]. From (2.25), the sum of conduction loss differences for the nine-switch converter can then be written as (2.31), where the second and third terms are noted to have only a single variable for summation. They are hence "uncontrollable". Unlike such situations, the first term in (2.31) can be lowered on average by making the maximum value of $(T_1 + T_2)$ coinciding with the minimum value of $|i_U + I_D|$, and vice versa (anti-phase). Ideally,

that can be ensured by having Ref_U in phase with i_U and $I_U \approx I_D$ (*both terminals supplying or absorbing power*).

$$\begin{aligned}\Delta \boldsymbol{P_{Con_{SA}}} &= \sum_{\boldsymbol{X=1,2,3}} \Delta \boldsymbol{P_{Con_{SAX}}} \\ &\approx \boldsymbol{2V_{On}}\left[\sum_{\boldsymbol{\epsilon=1\rightarrow f_{SW}}} \{(\boldsymbol{T_1}+\boldsymbol{T_2})|\boldsymbol{i_U}+\boldsymbol{I_D}|\}_{\epsilon} - \boldsymbol{I_D}\sum_{\boldsymbol{\epsilon=1\rightarrow f_{SW}}} \{\boldsymbol{T_1}\}_{\epsilon}\right. \\ &\left. - \boldsymbol{T_2}\sum_{\boldsymbol{\epsilon=1\rightarrow f_{SW}}} \{|\boldsymbol{i_U}|\}_{\epsilon}\right]\end{aligned} \tag{2.31}$$

- **DC-AC conversion**

The recommended operating conditions for dc-ac conversion are different from those for ac-dc conversion, although it sounds like a simple interchange in ac-dc conversion. The modulating reference for dc-ac conversion as well as currents flowing into the converter are summarized in (2.32) with the same expression for T_1 and T_2 like in (2.30). Here, T_2 is time-varying and T_1 is fixed and should be kept small in order to minimize the switching loss differences in (2.26).

$$\begin{aligned}\boldsymbol{Ref_U} = \boldsymbol{M_{oU}}, \boldsymbol{Ref_D} = \boldsymbol{M_D cos(\omega t)} - \boldsymbol{M_{oU}} + \boldsymbol{M_{Tri\_D}}, \\ \boldsymbol{i} \quad = \boldsymbol{I_U}, \boldsymbol{i_D} = \boldsymbol{I_D\, cos(\omega t + \theta_D)}\end{aligned} \tag{2.32}$$

Similarly to ac-dc conversion, the sum of conduction loss differences for the nine-switch converter for dc-ac conversion can be written as (2.33).

$$\begin{aligned}\Delta \boldsymbol{P_{Con_{SA}}} &= \sum_{\boldsymbol{X=1,2,3}} \Delta \boldsymbol{P_{Con_{SAX}}} \\ &\approx \boldsymbol{2V_{On}}\left[\sum_{\boldsymbol{\epsilon=1\rightarrow f_{SW}}} \{(\boldsymbol{T_1}+\boldsymbol{T_2})|\boldsymbol{I_U}+\boldsymbol{i_D}|\}_{\epsilon}\right. \\ &\left. - \boldsymbol{I_U}\sum_{\boldsymbol{\epsilon=1\rightarrow f_{SW}}} \{\boldsymbol{T_2}\}_{\epsilon} - \boldsymbol{T_1}\sum_{\boldsymbol{\epsilon=1\rightarrow f_{SW}}} \{|\boldsymbol{i_D}|\}_{\epsilon}\right]\end{aligned} \tag{2.33}$$

Assuming the upper terminal in the nine-switch converter is drawing dc power with $i_U = I_U > 0$ and the lower terminal is supplying ac power with i_D phase shifted with Ref_D by 180°. With $i_D > 0$ averaging the first term in (2.33) leads to an increase for a shorter T_2, since Ref_D is closer to a triangular wave. In contrary, when $i_U < 0$,

averaging of the first term in (2.33) leads to a decrease for a longer T_2, since Ref_D has more distance to a triangular wave. Therefore, since the second and third terms in (2.33) are uncontrollable, the minimization of the conduction power loss can be achieved by choosing i_U as positive and i_D as negative or vice versa with the peak of $|i_D| \approx |i_U|$. This means one terminal must be supplying power, while the other must be absorbing power.

- **AC-AC conversion**

For ac-ac conversion, one can assume that the upper terminal current frequency is much higher than the lower terminal, $\omega_U \gg \omega_D$. The lower terminal current can be approximated as dc in upper fundamental frequency. Hence, like to section V.B, the average conduction loss can be minimized by Ref_U in phase with i_U, positive i_D and $I_U \approx I_D$. However, the average conduction loss will be increased when i_D becomes negative. Consequently, the earlier loss minimization will be cancelled leading to no distinguished advantage for nine-switch converter in ac-ac conversion. Therefore, it is recommended to keep $I_U \approx I_D$.

2.2.5 **Simulation results**

For verification, the understanding and prediction tools developed were applied to identify conditions during which the nine-switch converter will have an advantage over its twelve-switch equivalence. The conditions chosen for testing are listed in Table 2.8. The results obtained for the individual switch power losses are shown in Fig. 2.12. It is observed for all cases, the switching loss difference is negligible by setting of $V_{dc} \approx V'_{dc}$. In ac-ac conversion with same frequency and dc-dc conversion, it is clear in Fig 2.12a and 2.12d that eq. (2.28) is met and the reduction in conduction loss is achieved for both conversion systems. For ac-dc conversion, both terminals should absorb or supply power, and the minus sign for currents in Table 2.8 means both terminals absorb power. Hence, the power saving is achieved as shown in Fig 2.12b. In dc-ac conversion, in nine-switch converter one terminal supplies power and the other terminal draws power. Hence, the advantage in reduction of the conduction loss can be verified in Fig. 2.12c.

Table 2.8. Parameters used for testing (‘+’ means absorbing and ‘ –‘ means supplying current by the converter)

☐☐pe	Nine-Switch Converter	Twelve-Switch Converter
AC-AC	$I_U = +11.27$ A, $I_D = -10.75$ A, $\theta = 5°$ $M_U = 0.82$, $M_{oU} = 0.1$ $M_D = 0.8$, $M_{oD} = -0.15$, $\theta_{RefU} - \theta_{RefD} = 12.6°$	$I_U = +10.49$ A, $I_D = -10.35$ A, $\theta = 5°$ $M_U = 0.82$, $M_{oU} = 0.1$ $M_D = 0.8$, $M_{oD} = -0.15$, $\theta_{RefU} - \theta_{RefD} = 12.6°$
AC-DC	$I_U = -10.92$ A, $I_D = -13.82$ A, $M_U = 0.9$, $M_{oU} = 0.1$, $M_D = -0.85$	$I_U = -10.25$ A, $I_D = -13.82$ A, $M_U = 0.9$, $M_{oU} = 0.1$, $M_D = -0.85$
DC-AC	$I_U = +13.96$ A, $I_D = -13.07$ A, $M_U = 0.85$, $M_D = 0.9$, $M_{oD} = -0.08$	$I_U = +13.96$ A, $I_D = -13.12$ A, $M_U = 0.85$, $M_D = 0.9$, $M_{oD} = -0.08$
DC-DC	$I_U = -10.24$ A, $I_D = +11.16$ A, $M_U = 0.1$, $M_D = -0.5$	$I_U = -10.76$ A, $I_D = +11.48$ A, $M_U = 0.1$, $M_D = -0.5$
DC link	佴□欐ȣĤ	300 V
Switching frequncy	10 kHz	10 kHz
Nominal power	1.5 kW	1.5 kHz

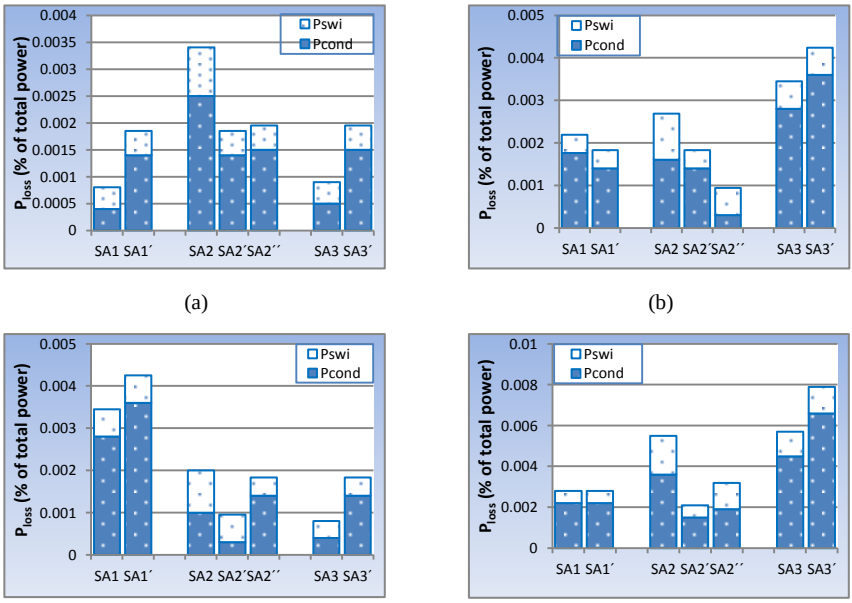


Fig. 2.12. Individual switch power losses of different nine-switch and twelve-switch energy conversion system: AC-AC (a), AC-DC (b), DC-AC (c), DC-DC (d).

To be more precise, Fig. 2.13 shows the total losses obtained for the different energy conversion systems in the nine-switch and back-to-back converters. It uniformly shows that the nine-switch converter, despite using fewer switches, can still maintain a performance advantage so long as it is used in the appropriate conditions.

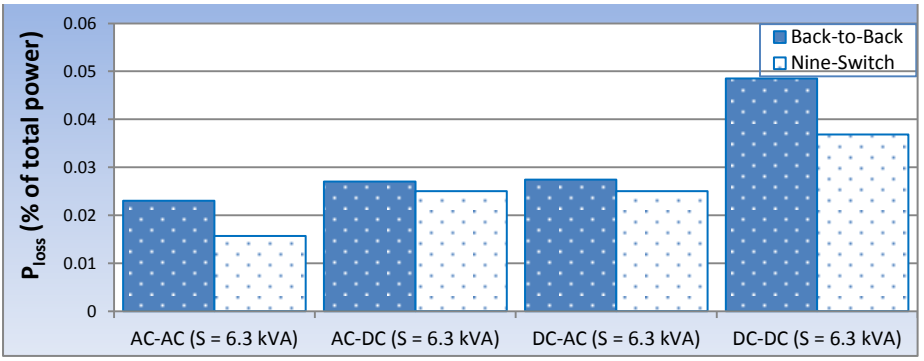


Fig. 2.13. Total power losses of different energy systems.

2.3 Conclusions

In this chapter, a comparison between the 9-level cascaded H-bridge, the 3-level diode clamped, which are the most conventional topologies in the industry, and 9-level hybrid asymmetric has been carried out. The simulation results show that the hybrid asymmetric topology has better performance in both conditions than the conventional multi-level inverters in all the performance indexes, which can lead to energy saving and improvement of power quality and a reduction in size, weight and volume of the LC filter. Besides, loss generation of the nine-switch converter has been compared with its twelve-switch equivalence for different types of energy conversion systems. It has been identified that the nine-switch converter will have an advantage when used for ac-ac, dc-ac and dc-dc energy conversion, if appropriate operating conditions are met. Test results done by other project members in CORPE verify the application criteria [35]. Converter selection and power loss identification is a part of design tool to be able to assess complete system as shown in Fig. 1.4.

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Chapter 3

Thermal modelling of high power IGBT modules

IGBT modules as the key devices have an important role in reliability of high power electronic converters [1], [2]. Extreme thermal cycling or thermal loading may trigger the reliability problems like thermo-mechanical stresses, which lead to progressive wear out of the device and fatigues inside the device package, e.g. bond-wire lift-off or solder cracking [3]-[5]. There are mathematical models, which relate the lifetime of IGBT modules to the thermal cycling [6], [7]. Besides, the semiconductor chip may lead to breakdown if the maximum junction temperature given by manufacturer is violated [6]. Therefore, a precise calculation of temperature inside the device package is important to ensure an accurate life time estimation and cost-effective converter design.

In common operating conditions each silicon chip generates heat that flows through multiple layers inside the package until it is dissipated in the heatsink. Besides, operation of multiple chips on the same substrate generates cross coupling heat flows between the chips [8], [9]. The cross coupling heat flows also occur between different sub-layers in the IGBT module. The cross coupling heat flows are not fully considered in the design process and this chapter investigates this behavior inside the IGBT module package by using Finite Element Method (FEM). The structure of the high power IGBT module and the materials used in different layers is explained. The concept of thermal cross coupling effect is described and the importance of this behavior is shown in the accurate temperature estimation of an IGBT module in dynamic operation. Finally, the cross coupling thermal resistances between chips will be extracted as a function of distance between chips and the position of the chips on the DCB.

3.1 Structure of IGBT module and conditions for analysis

The high power IGBT module for the analysis is composed of 6 IGBT/diode chip sections connected in parallel, and can handle load currents up to 1 kA with a blocking

voltage of 1.7 kV. All silicon chips are placed on a DCB layer and copper baseplate respectively via solder layers. In the case study for the thermal modelling, the IGBT module contains of 6 half-bridge converters connected in parallel, leading to totally 12 transistors and 12 diode chips. The IGBT module is simulated using FEM-based tool, which is the ANSYS Icepak, to extract the temperature profiles. A graphical view of the IGBT module in the FEM simulation is shown in Fig. 3.1. The IGBT module is assumed adiabatic from the top and to the lateral sides; so the heat propagates from the junction area through sub-layers and dissipates into the heat exchanger. Therefore, bond-wires are removed due to their minimum influence on the thermal impedance identification for simplification and also for reduction of the simulation time.

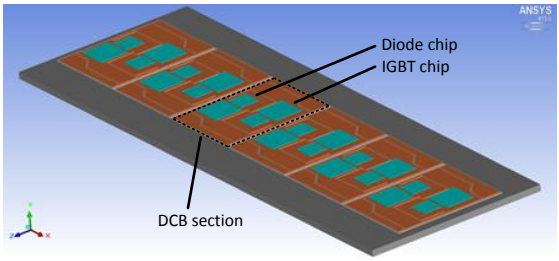


Fig. 3.1. Graphical view of high power IGBT module modelled in ANSYS Icepak.

The definition of different layer materials in the IGBT module is shown in Fig. 3.2. The DCB layer material is chosen as Aluminum Oxide (Al_2O_3). However, other DCB materials such as AlN or Si_3N_4 are also of interest, which can be studied as alternative cases. The thermal characteristics of all materials used in the IGBT module are given in Table 3.1. It is noted that the conductivity of some materials is set to be temperature dependent based on [10] especially silicon and copper, which show considerably lower thermal conductivity at higher temperatures.

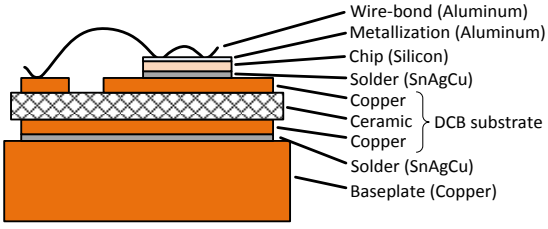


Fig. 3.2. Cross-section layers of IGBT module.

Table 3.1. IGBT module material thermal properties

Material	Density kg/m^3	Specific heat $J/(kg \cdot K)$	Conductivity $W/(m \cdot K)$	
			Temp. (°C)	Conductivity
Silicon	2330	705	0.0	168
			100.0	112
			200.0	82
Copper	8954	384	0	401
			100	391
			200	389
Al_2O_3	3890	880	35	
SnAgCu	7370	220	57	

As an initial demonstration and reference for analysis, the FEM simulations are conducted based on the given specifications of IGBT module. It is assumed that the baseplate is mounted on a plate with fixed temperature set to 80°C in order to decrease the simulation time and to avoid the uncertain physical properties in the thermal grease and heat sink. This is a typical design target of the cooling system for the chosen IGBT modules [11]. Heatsink behaves as a boundary condition beneath the IGBT module and the effect of boundary condition on thermal behavior of IGBT module is not focused in this section. Also, the ambient temperature of the simulations is fixed to 20°C. To achieve the highest accuracy in the simulation results and least simulation time, a multi-level meshing is applied in the FEM tool. Multi-level meshing means to apply a finer mesh with much more elements in the critical layers such as junction and solder layers rather than the thicker layers such as the baseplate and DCB. The FEM simulations are done in transient mode for 0.5 seconds, which is a sufficient time to ensure the temperatures inside the IGBT module has obtained the steady-state.

3.2 Thermal coupling effects

The conventional thermal models calculate the junction temperature excursions for self-heating of the devices caused by single operational semiconductor chips, but they do not explain any coupling of the thermal paths between the chips [12]. Therefore, the elevating temperature effect from one chip to another is not considered in such simple models, which might give an underestimation of the junction temperatures. Indeed any chip, which dissipates power to the heat exchanger, will result in temperature increase in all remaining chips because any heat flow will transfer through the whole IGBT

module. So, an accurate thermal model is needed, which accounts for this phenomenon. To study the thermal coupling effects, first, the average losses in chips are derived by simulation a half-bridge topology using PLECS. The converter specifications are shown in Table 3.2 and the calculated power losses (calculated by the IGBT module datasheet information using PLECS) are shown in Fig. 3.3.

Table. 3.2. Parameters of the converter simulated in PLECS

DC bus voltage V_{dc}	450 V
Rated load current I_{load}	ä¾ 嚬 A (peak)
Fundamental frequency f_o	50 Hz
Switching frequency f_{sw}	2.5 KHz
Filter inductor L_1	350 µH
IGBT module	1700V/1000A

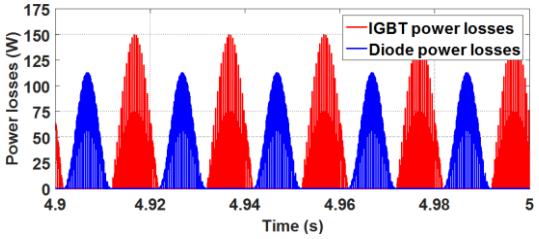


Fig. 3.3. Power losses for the IGBT module under study.

The surface temperature distribution of the IGBT module is shown in Fig. 3.4. As it is highlighted, the IGBT module under study consists of 6 cells, each cell contains a half-bridge converter including two pairs of IGBTs and freewheeling diodes, which are named as *T1*/*D1* and *T2*/*D2*.

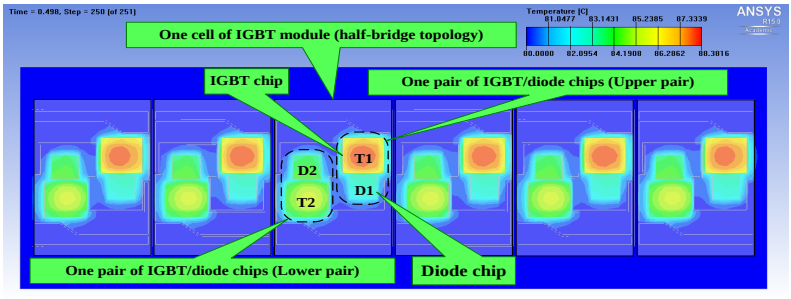


Fig. 3.4. Temperature distribution in a six cell-IGBT module in the test conditions stated in Table 3.2.

The coupling effect from other chips is related to the distance of heat sources and the magnitude of the power generated at heat sources [13]. It can be observed from Fig. 3.4 that in each half-bridge cell (totally 6 half-bridge cells), the thermal-coupling effects among the cells are negligible because they are mounted 1 mm far from each other for mechanical reasons. As a result the study can be focused on one individual half-bridge cell, which is composed of four closely located chips (Transistors *T1*, *T2*, and freewheeling diodes *D1*, *D2*). Besides, for simplicity, the thermal coupling study is focused on one pair of IGBT/diode (*T1* and *D1*) due to the symmetrical position to the next pair (*T2* and *D2*). It should be mentioned that the thermal coupling is not only among the chips, but also among the sub-level layers beneath the chips. Fig. 3.5 shows the cross-section view of temperature distribution in the IGBT module. It is seen that high thermal-couplings exist between different sub-layers. In addition, a noticeable amount of heat is flowing through the solder layers, which can lead to reliability problem as discussed detailed in [5].

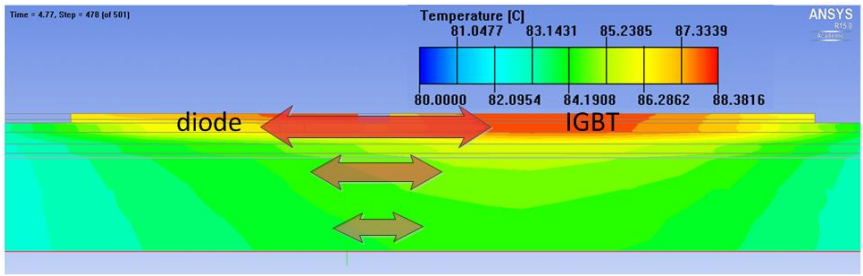


Fig. 3.5. Cross section view of temperature distribution in one cell of IGBT module and thermal coupling effects in the test conditions stated in Table 3.2.

The temperatures at the corner of chips are critical information for solder cracks, since solder delamination initiates from sides [5]. Therefore, nine equally spaced monitoring points are considered on each IGBT/diode chip to study the self heating and thermal coupling effects from the other chips. These monitoring points are shown in Fig. 3.6. Other monitoring points are considered under the chips in the chip solder and baseplate solder layers and they are labeled as s_1 and s_2 respectively.

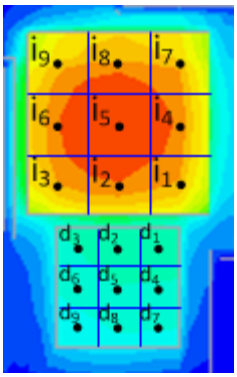


Fig. 3.6. Temperature monitoring points in one pair of IGBT/diode chip in the test conditions stated in Table 3.2.

3.2.1 **Thermal coupling effects on dynamic operation of IGBT module**

With reference to Fig. 3.4 to Fig. 3.6, in order to model the self heating and thermal coupling effects in dynamic operation, the FEM simulations are conducted in three cases: 1. when only the IGBT chip (*T1*) is conducting; 2. when only the freewheeling diode chip (*D1*) chip is conducting and 3. when the *T1* and the *D1* are conducting alternatively. For this purpose, a power loss profile from a grid-connected converter is given to the whole volume of IGBT and diode chips. The results for i_2, i_5 and i_8 monitoring points on the IGBT chip and d_2, d_5 and d_8 on the diode chip are shown in Fig. 3.7. As it is seen in Fig. 3.7 (a), (b) and (c), the transient temperature on the selected monitoring points of IGBT chip are shown. The IGBT chip gets minor thermal coupling impact from the diode chip. On the contrary, in Fig. 3.7 (d), (e) and (f), the diode chip is prone to more considerable thermal coupling impact from the IGBT chip, especially for the monitoring point d_2 which is more closer to the IGBT chip, as illustrated in Fig. 3.6. This asymmetrical thermal coupling between IGBT chips and diode chips is mainly due to the smaller size of the diode chip and higher losses in the IGBT chip in this operating condition. Since, the power losses depends on the power factor, in a case of reverse power flow, as in grid-connected inverters, the dioses will dissipate the largest part of power losses. So, it can be concluded that, the thermal coupling effects are not equal among the chips, depending on the operation mode of the

converter. Thermal calculations based on datasheet's thermal impedance curves risk to be tremendously wrong in such circumstances, due to thermal coupling effects between thermal paths.

3.2.2 **Thermal coupling effect variation by chip positions**

Commonly, IGBT module manufacturers demand for package design which is compact in size and can withstand higher temperatures and also adverse thermal cycling. This design can increase the power density and reliability of power module. On the other hand, there are some constraints in the design of the power module packaging. Electrical parasitics, e.g. stray inductances, is one of the constraints which limit the designer to place the chips far from each other. In addition, the chips cannot be placed much far from each other in order to decrease the thermal cross-coupling

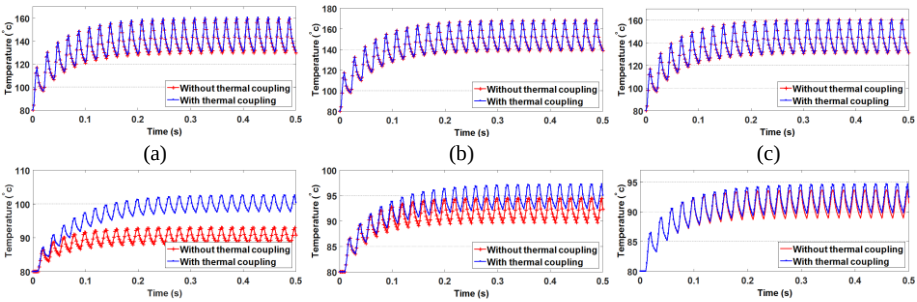


Fig. 3.7. Transient temperature on selected monitoring points with and without considering the thermal coupling effect: i_2 (a), i_5 (b), i_8 (c), d_2 (d), d_5 (e), d_8 (f).

effects, because it is difficult to obtain a compact design of the power module. Therefore, defining the thermal coupling variations with the chip positions can be useful for power module package designers. To quantify thermal coupling effects, the term, coupling thermal resistance is defined as the following:

$$\boldsymbol{R_{th(coupl)} = \frac{\Delta T_{IGBT-diode}}{P_{loss\ (opposite\ chip)}}} \tag{3.1}$$

where $R_{th(coupl)}$ is the coupling thermal resistance, $\Delta T_{IGBT-diode}$ is the diffrence of average temperatures in the chip which is the monitroing point is located and the chip where the power loss is injected and $P_{loss\ (opposite\ chip)}$ is the pulsed power loss injected to the opposite chip to the monitored chip.

In the first simulation, a pulsed power loss (50 W) is injected to whole volume of *T1* and the coupling thermal resistance is calculated between *D1* and *T1*. *T2* and *D2* are not conducting to identify the thermal coupling effect between *T1* and *D1*. *D1* is moved vertically and horizontally as it is shown in Fig. 3.8a. '*dx*' stands for moving *D1* horizontally, so *dx* equal to zero means *D1* and *T1* are in line. '*dz*' stands for moving *D1* vertically and represents the distance between *D1* and *T1*, so *dz* equal to zero means *D1* and *T1* are tangent to each other. The thermal resistance results are shown in Fig. 3.8b and Fig. 3.8c. The results show that thermal coupling is higher when both chips are in line and closer to each other.

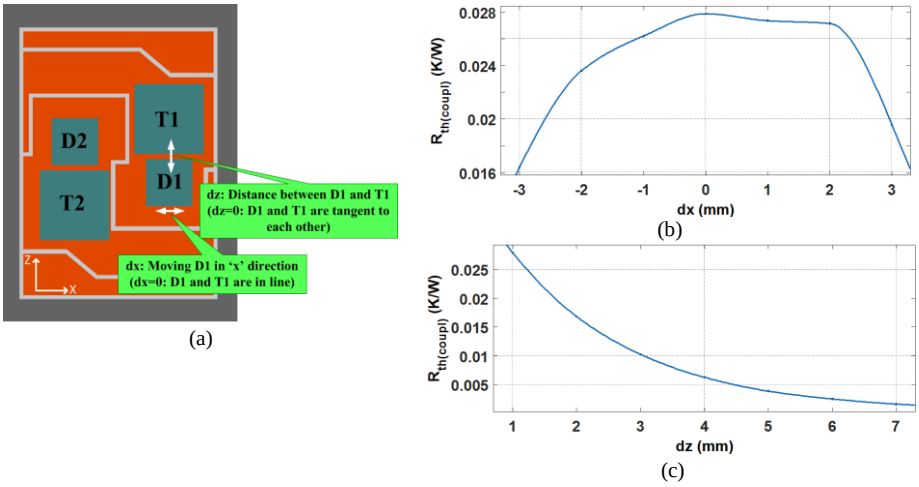


Fig. 3.8. Coupling thermal resistance between *D1* and *T1*: schematic view (a), moving *D1* in 'x' direction (b) moving *D1* in 'z' direction (c).

Similarly, the simulation is repeated for *T1* and *D2*. As it is shown in Fig. 3.9a, *D2* is moved vertically and horizontally to find the coupling thermal resistance between *D2* and *T1*. '*dx*' in this figure means the distance between *D2* and *T1*, so *dx* equal to zero means *D2* and *T1* are tangent to each other and $dx < 0$ means D2 is moved in $-x$ direction. '*dz*' stands for moving *D2* vertically, so *dz* equal to zero means *D2* and *T1* are in a line. The pulsed power is injected to *T1* and the coupling thermal resistance is calculated from *D2* to *T1*. The results are shown in Fig. 3.9b and Fig. 3.9c. As it can be seen, the maximum thermal resistance when *D2* and *T1* are in a line is much less than in the case when *D1* and *T1* are in a line.

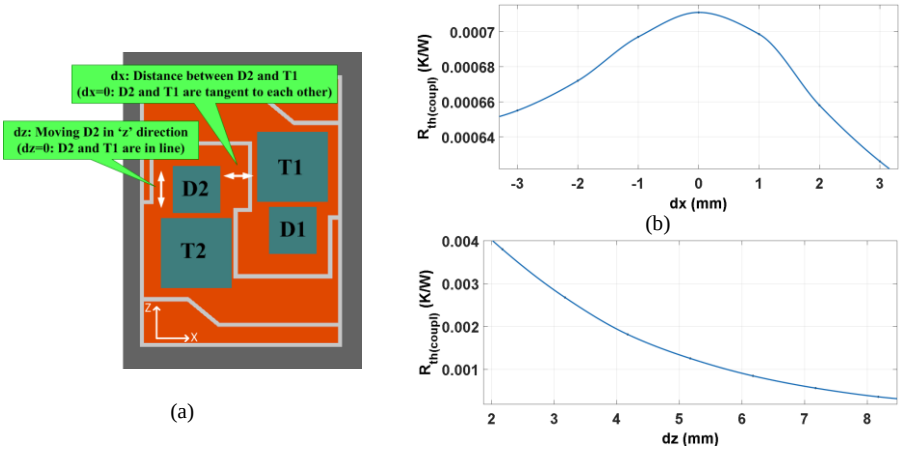


Fig. 3.9. Coupling thermal resistance between *D2* and *T1*: schematic view (a), moving *D2* in 'x' direction (b), moving *D2* in 'z' direction (c).

The last simulation is done to find the coupling thermal resistance between *T2* and *T1*. This case is shown in Fig. 3.10. '*dx*' and '*dz*' stand for moving *T2* horizontally and vertically, respectively. The simulation results are shown in Fig. 3.10b and Fig. 3.10c. As it is seen from this figure, the coupling thermal resistance for *T2*-*T1* is much less than two other cases.

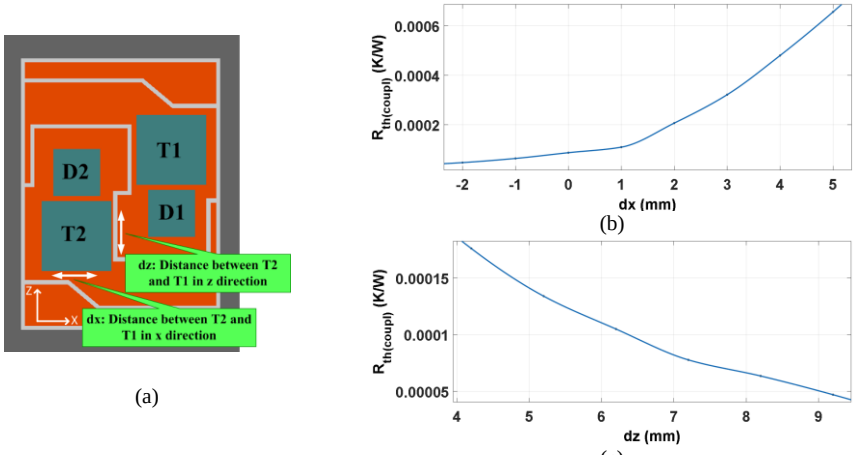


Fig. 3.10. Coupling thermal resistance between *T2* and *T1*: schematic view (a), moving *T2* in 'x' direction (b), moving *T2* in 'z' direction.

3.3 FEM modelling of power modules in abnormal operation

In the current research works, the lifetime of high power IGBT modules are mostly investigated under normal operating conditions such as thermal cycling and power cycling [14], [15]. However, abnormal operations such as short circuit or overloads are also critical and should be considered if a confident lifetime prediction is targeted. In short-circuit operation, the device withstands high voltage and high current at the same time and even if the device does not fail, a high thermo-mechanical stress on the entire module package can reduce the life-time significantly. The problem becomes more drastic in the presence of an aged part such as delaminated solder [16]. Therefore for a design for reliability approach, mixed failure mechanisms should be taken into account from the very beginning [17]. In this section thermal stress generated in short-circuit condition on bond-wires of aged MW-scale IGBT modules is investigated. FEM is applied to extract the temperature profiles at the surface of the IGBT chip for different die-attach delamination depths. The most thermal stressed bond-wires are identified and the thermo-mechanical stresses on them are estimated, which are caused by thermal expansion mismatch in silicon/aluminium interface.

3.3.1 Operation of IGBT module in short-circuit condition

In the short-circuit condition, thermal stresses are expected to occur in the range of tens of microsecond; therefore the chip are expected to peak up to very high temperatures in a short time. For this reason, it is more important to consider temperature-dependent thermal properties for the materials used in the IGBT module. As boundary conditions in the FEM simulation, the IGBT module is assumed to be adiabatic from the upper and lateral surfaces and a heat exchanger is taken into account at the bottom of the baseplate with a heat transfer coefficient of 5000 W/m^2. This value reflects the effective convection parameter for the cooling system and is highly dependent to the cooling system flow rate and geometry. So, by the change of these parameters the temperature response in the IGBT module can be changed accordingly. The heat source is taken into account as a volumetric heating block with 30 µm thickness and 10 µm below the chip surface, whose dimensions have been taken from the internal electric field curve during the short-circuit at the considered voltage. A

simple half-bridge model has been developed in Pspice for power loss calculations. In this study, the input voltage of the circuit is set to a fixed DC voltage source.

The most critical short-circuit condition occurs when one IGBT switch is conducting and the other one is switched on. If a protection circuit is not present in the circuit, the short circuit can destroy the IGBT module immediately. However, modern gate drivers effectively detect such a condition by monitoring the V_{CE} and turning off the device before 10 μs from the short-circuit occurrence. In the short-circuit condition, though, the high voltage which is present on the device together with a current up to 10x higher than the nominal one produces a huge switching loss which is several hundred times higher than the normal switching cycle. For the electrical simulation and to get power losses in short-circuit, the IGBT module described in 3.1 is short circuited in a half-bridge circuit. The measured short-circuit current, collector voltage and dissipated power are shown in Fig. 3.11 which is a typical situation in the IGBT module under study. The short-circuit power increases to 5.4 MW for about 10 μs. It is assumed that this power is evenly distributed in 6 DCB sections, which means 0.9 MW on each IGBT chip.

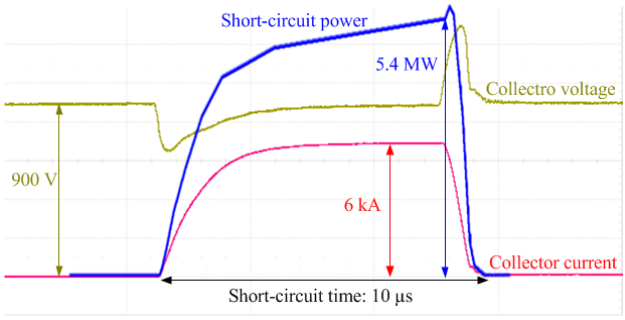


Fig. 3.11. Typical short-circuit operation of the high power IGBT module.

3.3.2 **Ageing (delamination) effects**

The prominent aging mechanisms in the IGBT power modules are solder fatigue, bond wire fatigue, and reconstruction of Al metallization [16]. Solder cracks propagate due to visco-plastic deformation amplitude per cycle and the solder layer tends to

accumulate plastic strains on the edges; hence the delamination initiates from these areas [16]. An sketch of this phenomenon is shown in Fig. 3.12.

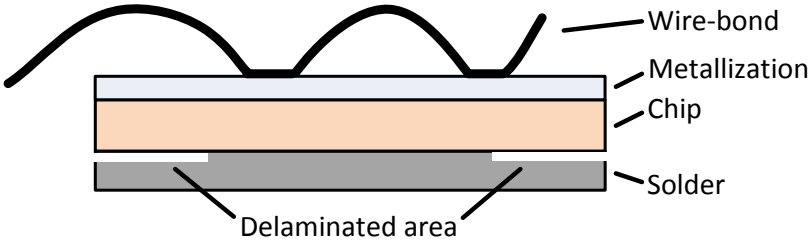
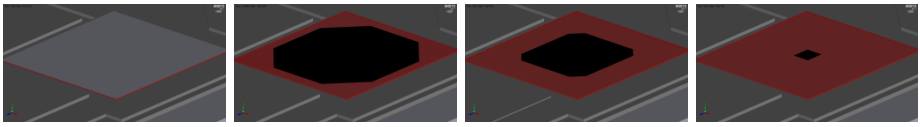


Fig. 3.12. A sketch of solder delamination in a chip of IGBT module.

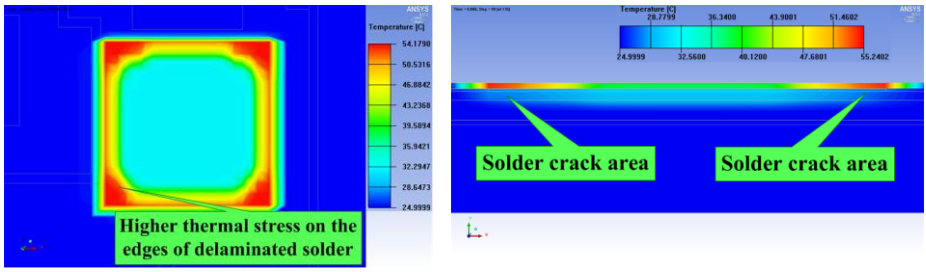
As explained in [16], the delamination area propagates by the number of thermal cycling from the edges inwards until a significant part of the solder material vanishes (end of life). So, several delamination depths have been simulated with steps of 1 mm. The models for the fresh solder, beginning of solder delamination, hard solder delamination and end life of the solder is shown in Fig. 3.13.



(a) (b) (c) (d)

Fig. 3.13. Geometry of IGBT chip and solder developed in ANSYS Icepak: fresh solder (a), beginning of solder delamination (b), hard solder delamination (c), end life of the solder (d).

The FEM simulations (in ANSYS Icepak) are carried out from 0 to 0.1 ms and the short-circuit power is injected to the IGBT chip in 5 μs for 10 μs duration. To understand the effects of aging on the chip surface, die-attach (chip solder) delamination is modelled as an octagon region with 1 μm thickness surrounded by air in the upper area of solder. A very fine mesh is generated in the delaminated area with at least 3 elements in the vertical direction. Fig. 3.14 illustrates the model. It is seen that the outmost corners are the most stressed ones. Moreover, it is clearly seen that the temperature changes sharply at the crack interface.



(a) (b)

Fig. 3.14. Temperature profile of the IGBT chip with aged solder: top view (a), cross-sectional view (b).

3.3.3 **Thermal stress on wire-bond attach locations**

By incrementing the aging of the solder layer, the junction-to-case thermal resistance of the IGBT module increases due to less heat spreading from the chip to the lower layers. The higher thermal resistance leads to higher temperatures on the surface of the chip. As discussed in 3.3.2, solder delamination induce an inhomogeneous temperature field, which causes an increased stress in regions above the delaminated area (including the chip surface). There are ten wire-bonds, which connect the chips to the collector trace in addition to one wire-bond in the center of the chip to connect the gate to the gate busbar. In solder delamination conditions, different wire-bonds experience different temperatures depending on the location they are attached. For this reason, several temperature monitoring points are used for comparison of local temperature and thermo-mechanical stress in different delamination levels. Such monitoring points are shown in Fig. 3.15.

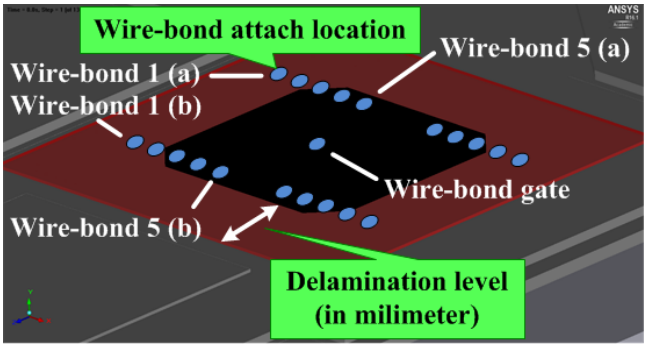


Fig. 3.15. Temperature monitoring points on the IGBT chip.

As an example, the temperature in short-circuit condition is shown for different delamination levels (fresh, beginning, aged, and end of life) in three wire-bond attach locations: *1a*, *1b* and *gate*. In this case study, fresh means brand new solder, beginning means solder delaminated 1 mm from corners, aged means solder delaminated 5 mm from edges, and end of life means solder is totally delaminated. Short-circuit occurs at 5 µs for 10 µs. The results are shown in Fig. 3.16. As it is observed, the peak temperature is the same for all cases, since the heat up is almost adiabatically due to the time frame of the power loss. Afterwards, the generated heat propagates to lower layers. As indicated in Fig. 3. 16, the temperature is seen to drop to initial temperature in 0.1 s. In the 'end of the life' condition, both wire-bond heel locations in *1a* and *gate* show higher temperature response due to uniform thermal distribution (due to higher thermal resistance of the IGBT module). For all other cases the temperature in the gate location shows almost the same response. The reason originates from the delamination propagating from corners, hence the last remaining solder material is under the center of the IGBT chip.

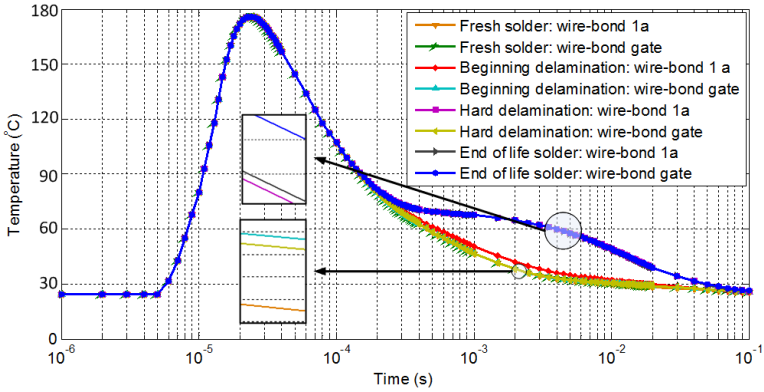


Fig. 3.16. Temperature profiles for different solder delamination levels on wire-bond heel *1a* and *gate* in the short circuit condition.

Fig. 3.17 shows the temperature profiles for 5 samples of wire-bond attach locations in middle solder delamination level (4 mm delaminated from sides). It is observed that the wire-bond attach closer to corners experience slower cooling than the middle wire-bonds and the gate wire-bond. The reason is that, the corners have no physical contact to the underneath layers and therefore, they do not have cooling sides, lead to higher

temperatures. In addition, since each wire-bond is attached in two places on the chip with different distances to the sides of the chip, they show different temperatures in relation to the distance to the sides. In this example '*a*' are closer to the corners of the chip and therefore they experience slower cooling rather than '*b*', which are closer to the center of the IGBT chip.

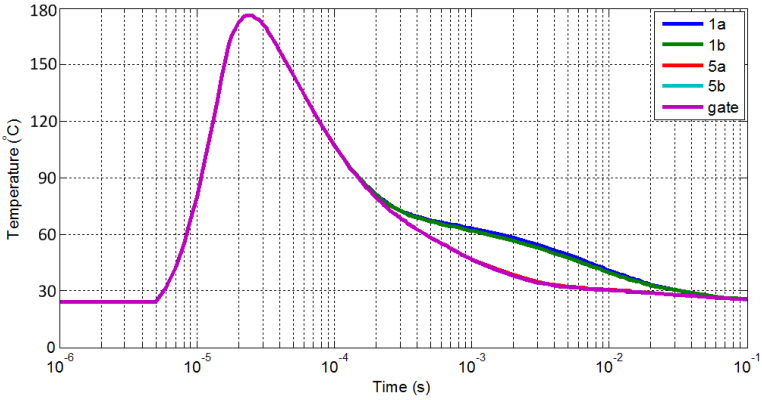


Fig. 3.17. Temperature profiles for bond-wire heel locations in middle delamination level (4 mm delaminated from sides) in the short-circuit condition.

3.3.4 **2D analytical strain model of wire-bonds**

Thanks to cooperation with Kristian Bonderup Pedersen from the Department of Physics and Nanotechnology at Aalborg University, a thermos-mechanical model has been established for the bond-wires. During heat-up, the Aluminum wire expands according to the Coefficient of Thermal expansion (CTE) between Silicon and Aluminum. This creates a strain due to CTE mismatch. Similarly, at the bond heel wire flexure induce local strain from pure Aluminum expansion. The former is derived directly from the expansion coefficients:

$$\varepsilon_{CTE} = \Delta\alpha\Delta T \tag{3.2}$$

where $\Delta\alpha$ is the CTE difference between Si and Al and ΔT is the temperature difference between two materials. The strain induced by wire flexure, however, is more complicated. In principle one needs the temperature field across the wire and carry out 3D simulations. However, if it is assumed homogenous temperature throughout the

wire (T_W) and instantaneous heating of the wire curve (T_W=T_{Si}). Then an analytical approximation of the homogeneous strain near the bond heel can be derived as:

$$\varepsilon_{XX} = \left(\sin(\phi) + \frac{2l_c}{d}\cos(\phi) \right) \varepsilon_{th} \qquad \text{ëâU3)}$$

$$\varepsilon_{YY} = \left(\cos(\phi) - \frac{2l_c}{d}\sin(\phi) \right) \varepsilon_{th} \qquad (3.4)$$

where $\varepsilon_{th} = \alpha_{Al}\Delta T$, ϕ is the wire angle, l_c is the wire heel length, d is the wire diameter, and the wire is assumed isotropic. The approximation displays results similar to finite element based simulations with limited divergence under constant temperature. From (3.3) and (3.4) the volumetric strain near the bond heel can be calculated as:

$$\varepsilon_V = \varepsilon_{XX} + \varepsilon_{YY} + \varepsilon_{XX}\varepsilon_{YY} \qquad (3.5)$$

Fig. 3.18 illustrates the volumetric strains on wire-bonds. As it is observed, the strains are higher in more aged conditions and for bond-wire closer to the edge of the chip. It should be mentioned that the plotted strain is assumed purely elastic, which is the reason it is fully reversible. However, the plastic strain is the main cause to failure on the wire-bonds which has not been focused in this thesis.

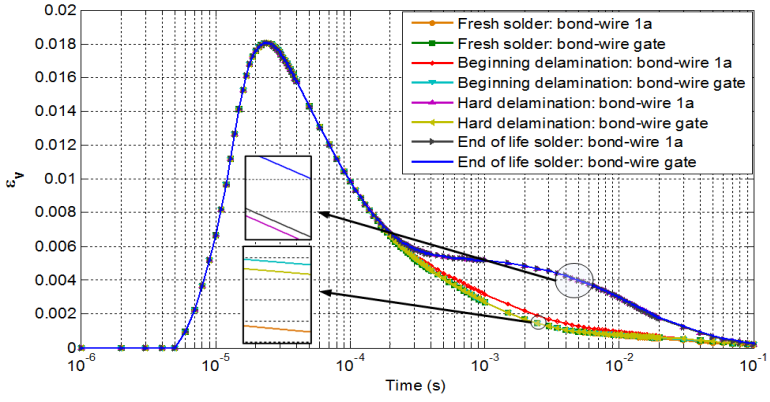


Fig. 3.18. Strain of wire-bonds *1a* and *gate* (see Fig. 3.15) for different solder delamination levels in the short-circuit condition.

3.4 Conclusions

In this chapter, application of FEM simulations in thermal study of IGBT module has been investigated. The thermal coupling effects and their importance in calculation of temperatures in high power modules have been discussed. In addition, the dependency of thermal coupling effects to the distance between the chips has been studied for different distances and design maps suggested for coupling thermal resistances in respect to the distance between the chips. Besides to normal operation of IGBT module, abnormal operation is important to be investigated. So FEM has been applied to study the thermal behavior of IGBT module in the short-circuit condition. The thermo-mechanical stress on wire-bonds of the IGBT module in short-circuit operation has been investigated. The effect of solder delamination on temperature distribution on the chip surface has been studied and thermal profiles have been presented for different wire-bond attach locations. Based on a 2D analytical strain model, the volumetric strain near bond heels was calculated for different delamination depths. It was concluded that higher strains are induced to the wire-bonds in higher solder delamination depths specially the wire-bonds closer to the edges of the chip.

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Chapter 4

3D thermal network for high power IGBT modules

In chapter 3, FEM studies have been focused on short-term load profiles (milliseconds to seconds), however many other factors may have impacts on the loading of high power IGBT modules in long-term applications (real mission profiles). Some of the factors are shown in Fig. 4.1. These factors include variable wind speeds and temperatures, harsh environments, grid disturbances, etc.

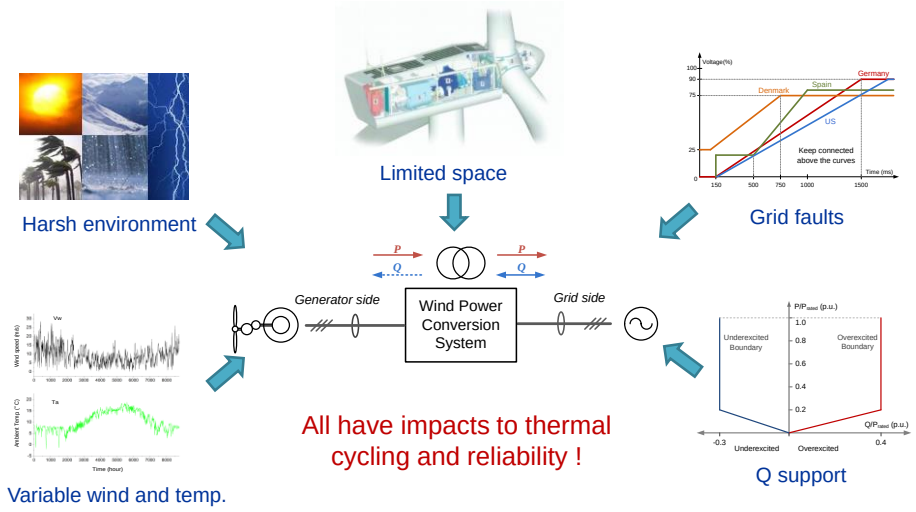


Fig. 4.1. Long-term factors affecting the reliability of IGBT modules.

FEM simulations are conventionally used for steady-state simulations or transient simulations in the range of seconds. For long-term load profiles FEM is time-consuming and demands huge amount of computation time, which is practically not feasible. Therefore, much faster methods are required to estimate temperatures for load profiles under multi-time scales and to study life-time of the IGBT module. Meanwhile, the accuracy about the thermal coupling and temperature distribution inside the IGBT module need to be maintained at same level.

Currently, the correct estimation of the temperature in high power semiconductor is still a challenging task. A group of methods are based on indirect estimation of the

temperature, using thermal models composed of RC lumps given by the manufacturer's datasheets, as described detailed in [1]-[8]. In these methods, the temperature of IGBT module is mathematically solved by the information of loss dissipation in the IGBT/diode chips as well as the thermal impedances in the form of 1D RC lumps. However, these thermal models have their limits to represent the temperatures in different layers of the IGBT module. In addition, they can only address an average temperature of the chip area without considering the thermal coupling between the chips or accurate temperature distribution on different layers of the materials. On the other hand, many researches have been carried out to simplify and speed up the pure FEM simulation tools, such as the ones mentioned in [12]-[20]. Nevertheless, these methods are quite difficult to be connected to the loading behavior of the device under certain converter mission profiles, and some of them may significantly decrease the level of accuracy in the temperature computation.

In this chapter a novel 3D RC lumped-based thermal model is proposed for high power IGBT modules. In this thermal model, the structure geometry and material information of the devices are taken into account. The obtained model is suitable to be integrated into a circuit simulator [21], where the simulation is much faster than the FEM simulation with a comparable accuracy. This model includes thermal coupling effects between the chips as well as sub-layers under the chips. Moreover, critical boundary conditions which affect the thermal behavior of the IGBT module are considered in the model. One key outcome is that the detailed temperature distribution inside the IGBT module can be obtained both vertically and horizontally in a circuit simulator with acceptable simulation speed. This feature is very important for the reliability analysis of the power electronics [22]. In reliability studies, maximum temperatures as well as temperature cycles on chip surface, where the wires are bonded and critical layers such as solders, where fatigues occur are important to be identified. A schematic of the IGBT module highlighted with critical locations is shown in Fig. 4.2. The presented thermal model provides fast and accurate thermal information in the IGBT module for long load profiles where FEM simulations are impossible to be used.

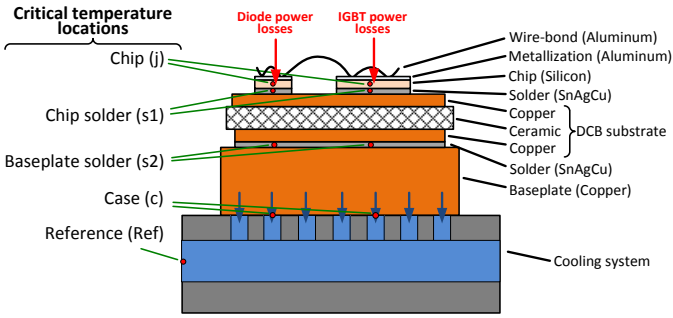


Fig. 4.2. Schematic of IGBT module with critical temperature locations.

The chapter is structured as follows: the modelling environment and operating conditions of the considered IGBT module are introduced first, where the modelling challenges and limits of the existing thermal models are explained. Then, the proposed method to extract the 3D lumped thermal network is described. Self-heating and thermal coupling effects inside the IGBT module are carefully included in the modelling process. Then, the boundary condition effects on the thermal model are discussed. Finally, the obtained thermal network is validated both by FEM simulation and experimental measurement under the real field operating conditions in a grid-connected wind power converter.

4.1 Proposed structure of 3D thermal model

In order to correctly represent the thermal-coupling impact, a thermal model is needed which estimates the self-heating as well as thermal coupling effects from other chips in critical layers. Indeed, this model should make a superposition of self-heating and thermal-coupling effects. For this purpose, the self-heating effects are modelled as conventional lumped RC networks from the chip to reference point (e.g. cooling temperature) for each intended locations on the chips. On the other hand, thermal coupling effects are modelled as voltage sources between every two adjacent temperature nodes. These voltage sources are controlled by power losses in the neighboring chips, which cause to thermal coupling.

FEM is executed for two trials in which the temperatures are monitored on nine equal distanced positions on chips and solder. The number of points is selected to

monitor more thermal coupling effects. So, if there is a high thermal coupling between the chips, temperature variation on the surface of the chips will be higher; therefore, the number of points can be increased to 16, 25, etc. Finally a 3D thermal lumped network is obtained, which is shown in Fig. 4.3. For simplicity, only the thermal branches for i_2 and d_2 monitoring points are shown; the other points follow the same instructions. The thermal branches are drawn for the critical monitoring points from chip surface to chip solder $Z_{th}(j\text{-}s1)$, chip solder to baseplate solder $Z_{th}(s1\text{-}s2)$, baseplate solder to case $Z_{th}(s2\text{-}C)$ and case to reference $Z_{th}(s2\text{-}C)$. Z_{th} is the thermal impedance of each branch, which will be described later in this chapter. The thermal coupling effects are shown as controlled voltage sources, which are coupled to the main thermal branches.

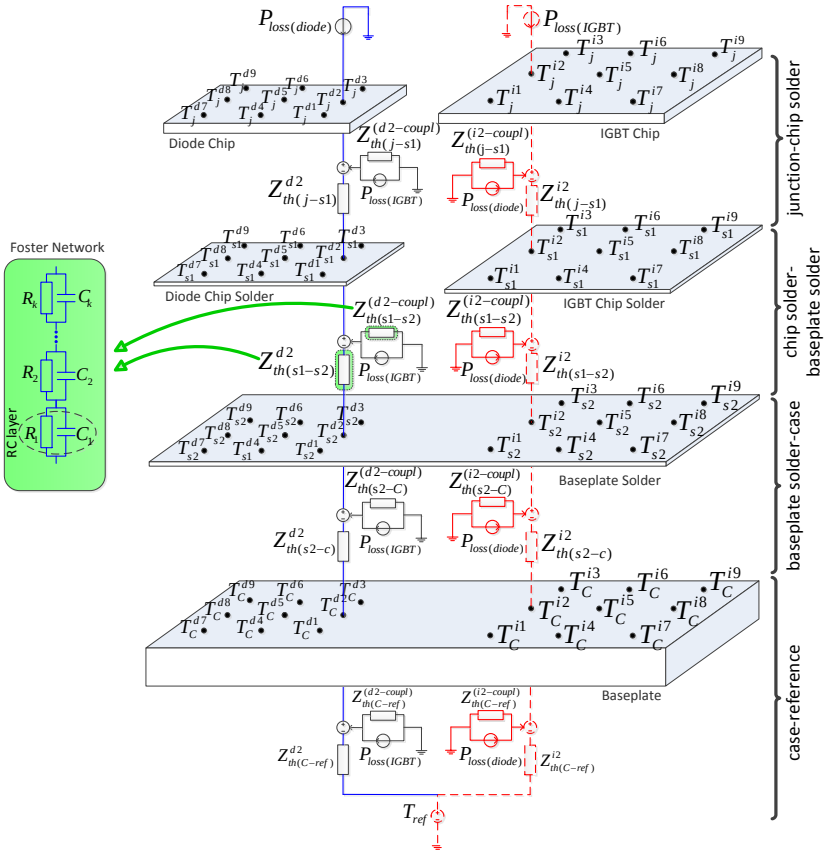


Fig. 4.3. 3D thermal impedance network for a pair of IGBT/diode chips (Thermal network is shown for $\boldsymbol{i_2}$ and $\boldsymbol{d_2}$; all other monitoring points share the same thermal network configuration).

4.2 Extraction of 3D thermal network

In general terms, the temperature rise across the IGBT module is proportional to the power dissipation in both transient and steady-state [18]. The temperature rise in steady-state can be calculated applying thermal resistance, R_{th}, between the target point and a reference temperature point. Similarly, the temperature in the dynamic state is calculated using the transient thermal impedance curve, $Z_{th}(t)$, between the two mentioned points. The thermal resistance and thermal impedance equations are given by eq. 4.1 and eq. 4.2.

$$\boldsymbol{R_{th(a-b)} = \frac{T_a - T_b}{P_a}} \tag{4.1}$$

$$\boldsymbol{Z_{th(a-b)}(t) = \frac{T_a(t) - T_b(t)}{P_a}} \tag{4.2}$$

where T_a and T_b are temperatures in two adjacent points and P is the power losses which is generated in the first point. Typically, the device power losses is not constant and also time dependent, so the temperature rise (ΔT) of the device can be calculated as eq. 4.3 [23].

$$\boldsymbol{\Delta T(t) = \int_0^t P(\tau).dZ_{th}\,(t-\tau).d\tau} \tag{4.3}$$

But in order to study the thermal coupling impact on the chips and to find the temperature rise in critical points such as solder layers, more detailed thermal impedances are needed. This information is essential for the optimized design of IGBT modules. To consider self-heating and thermal coupling impacts, eq.4.3 can be rewritten as 4.4.

$$\begin{bmatrix} T_1 \\ T_2 \\ \cdots \\ T_m \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2n} \\ \cdots & \cdots & & \cdots \\ Z_{m1} & Z_{m2} & \cdots & Z_{mn} \end{bmatrix} . \begin{bmatrix} P_1 \\ P_2 \\ \cdots \\ P_n \end{bmatrix} + \begin{bmatrix} T_{ref} \\ T_{ref} \\ \cdots \\ T_{ref} \end{bmatrix} \tag{4.4}$$

where, T_m is the monitoring point temperature, P_n is the power losses on each chip, T_{ref} is the reference temperature to the monitoring point, Z_{mm} is the self-heating and Z_{mn} is the coupling thermal impedance between the monitoring point and the reference point.

As an example the thermal branch for i_2 (highlighted in red in Fig. 4.3) can be written as the following

$$\begin{aligned} \boldsymbol{T_j^{i2}} = \boldsymbol{P_{loss(IGBT)}}\cdot\left(\boldsymbol{Z_{th(j-s1)}^{i2}} + \boldsymbol{Z_{th(s1-s2)}^{i2}} + \boldsymbol{Z_{th(s2-c)}^{i2}} + \boldsymbol{Z_{th(c-ref)}^{i2}}\right) \\ + \boldsymbol{P_{loss(diode)}}\cdot\left(\boldsymbol{Z_{th(j-s1)}^{(i2-coupl)}} + \boldsymbol{Z_{th(s1-s2)}^{(i2-coupl)}} + \boldsymbol{Z_{th(s2-ref)}^{(i2-coupl)}}\right. \\ \left. + \boldsymbol{Z_{th(c-ref)}^{(i2-coupl)}}\right) + \boldsymbol{T_{ref}} \end{aligned} \quad (4.5)$$

where $T_j i2$ is the temperature on chip i_2, $P_{loss}(IGBT)$ is the IGBT chip power losses, $P_{loss}(diode)$ is the diode power losses, $Z_{th(m\text{-}n)}i2$ is the thermal impedance between adjacent critical points, $Z_{th(m\text{-}n)}(i2\text{-}coupl)$ is the coupling thermal impedances between adjacent critical points and T_{ref} is the reference temperature in the cooling system. The method used in this work, is to extract thermal impedance values, which are based on extraction of thermal impedance curves from FEM analysis and transformation of these curves into an equivalent thermal RC networks by using step responses. The RC networks can then be used in any circuit simulators like PSpice or PLECS to calculate temperatures. This will accelerate the simulation time with acceptable accuracy compared to the time-consuming FEM analysis.

To extract the responses, a pulsed power loss is injected to each chip (IGBT and diode) separately and the temperature responses from the intended monitoring points are drawn. If only the self-heating of the monitoring point is intended to be calculated, the step-response analysis can be applied to extract the equivalent thermal RC network. If the thermal coupling effect is also needed to be taken into account, the overall thermal impedance for one node can be extracted by using the superposition principle as the summation of self-heated thermal impedance and coupling thermal impedances from the other chips (as another heat source). The methodology to find the thermal response of the IGBT module is detailed in the following:

1. The IGBT module geometry is drawn in FEM environment.
2. Step response analysis is performed for all chips – by applying the pulsed power loss input to one single chip in a trial and then to monitor the temperature responses on the same chip and all other intended points on the other chip. The results are a series of curves, which are transient temperature responses. This process is illustrated in Fig. 4.4.

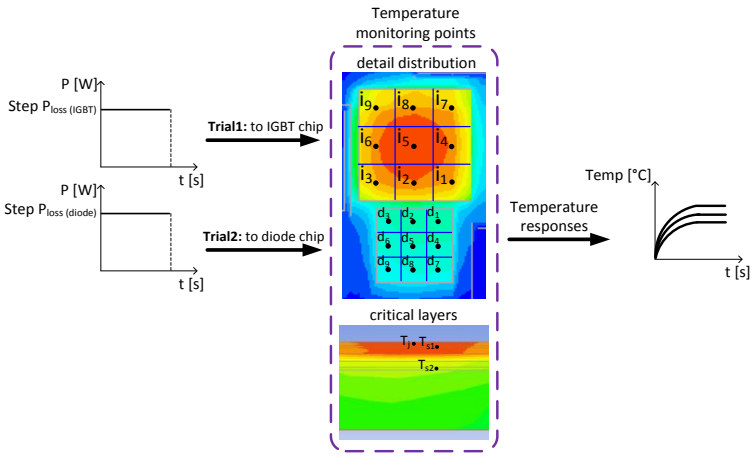


Fig. 4.4. Temperature responses to step in power losses injected to the IGBT chip and diode chip and they are monitored in critical locations and layers of the IGBT module.

3. In order to obtain self-heating thermal impedance curves between the vertical monitoring points, i.e. *j* to *s1*, *s1* to *s2*, *s2* to *C*, and *C* to *ref*, the extracted temperature curves in each monitoring point is subtracted from the adjacent vertical point and divided to the same chip power losses. As an example the equation to obtain the self-heating thermal impedance between *j* and *s1* can be calculated as

$$\boldsymbol{Z_{th(j-s1)}^{im}} = \frac{\boldsymbol{T_j^{im} - T_{s1}^{im}}}{\boldsymbol{P_{loss(IGBT)}}} \tag{4.6}$$

where *im* is the monitoring point on the IGBT chip in the monitoring layer and $P_{loss}(IGBT)$ is the power losses of the IGBT chip.

For identification of the coupling thermal impedance curves, the temperature difference between two adjacent layers on each monitoring point of a chip is divided to the pulsed power losses injected to the other chip. For example the coupling thermal impedance between *j* and *s1* can be calculated as the following

$$\boldsymbol{Z_{th(j-s1)}^{im-coupl}} = \frac{\boldsymbol{T_j^{im} - T_{s1}^{im}}}{\boldsymbol{P_{loss(diode)}}} \tag{4.7}$$

4. In order to apply the thermal impedance curves in the circuit simulator for temperature estimation, the thermal impedance curves in each scenario are curve-

fitted mathematically using a sum of exponential functions as shown in (4.8) in order to obtain an equivalent thermal network to the thermal impedance curve.

$$\boldsymbol{Z_{th}(t) = \sum_{i} R_{th_i} . (1 - e^{-t/R_{th_i}C_{th_i}})} \tag{4.8}$$

where R_{thi} is the equivalent thermal resistance and C_{thi} is the equivalent thermal capacitance.

The equivalent RC network, which is used in this thesis, is a Foster network that is shown in Fig. 4.3. The number of RC layers in the Foster network is dependent on the accuracy of the fitted curve to $Z_{th}(t)$ to the real curve. The R and C values in the Foster network are mathematically calculated using a curve-fitting tool in MATLAB. For this purpose, first the time values and thermal impedance values in the thermal impedance curve are entered as two matrices. The number matrix arrays should be as much that the thermal impedance curves get to the steady-state. Also for better fitting operation, it is advised that in transient behavior, more resolution of thermal impedance values being selected rather than the steady-state. The time steps selected for this work are shown in Fig. 4.5, which are 0.05, 0.1 and 1 seconds. The curve-fitting tool creates an interpolation fit to the data based on the eq. 4.8. MATLAB Curve-fitting tool uses nonlinear least-squares formulation to fit the nonlinear model to the data extracted from the thermal impedance curve. The whole curve-fitting process can be found in [24].

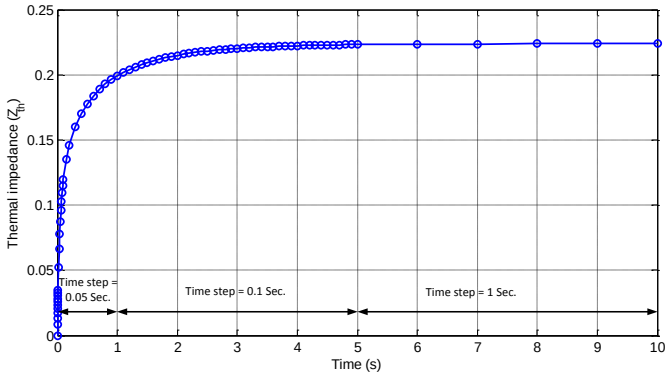


Fig. 4.5. Time step values which has been selected for curve fitting of transient thermal impedance curves.

4.3 Characterization of boundary conditions in 3D thermal network

Although the presented 3D thermal model gives detailed thermal information in the IGBT module, variation of boundary conditions, which is inevitable on the thermal analysis of IGBT modules, is neglected. The boundary conditions in term means a set of conditions that is required to be satisfied at all or one part of the boundary of a design geometry in which a set of differential equations is to be solved [25]. In an IGBT module, boundary conditions consist of heat sources i.e. power dissipation in the semiconductor chips and heat sink i.e. cooling system. In order to understand the importance of the boundary condition effects in thermal impedance of IGBT module, first the cooling system variations and power loss variations are modelled by FEM simulations and temperature responses are extracted in the corresponding points in the 3D thermal network.

4.3.1 FEM modelling with variation of heatsink

In this section thermal impedances for different cooling system are examined including fluid cooling system and fixed case temperatures. In all cases a 50 W square pulsed power is injected into the IGBT chip to fix the heat source boundary conditions and conditions for heatsinks are varied. To represent the capability of fluid cooling systems, different cooling mechanisms are considered in the heatsink. For each cooling mechanism, the equivalent heat transfer coefficient, *htc*, of the cooling system is extracted and modelled as a thick plate beneath the base plate of the IGBT module. The equivalent heat transfer coefficient is a measure, which stands for the amount of heat, which is transferred by convection between a solid and a fluid [26]. The thermal resistance between the IGBT module and heatsink, R_{th}, can be defined based on the definition of heat transfer coefficient

$$\boldsymbol{R_{th} = \frac{1}{htc.A}\ (K/W)} \tag{4.9}$$

where *A* is defined as the effective area for heat dissipation of the heatsink. As listed in [26], the equivalent heat transfer coefficients can vary from *10 W/m^2·K* for natural

convection systems to 10^5 $W/m^2 \cdot K$ for phase change cooling systems. With the method described in section 4.2, the transient thermal impedance curves are extracted for different *htcs*. The *htcs* with in the ranges of $3000<htc<100000$ $W/m^2 \cdot K$ are used, which represents reasonable cooling conditions for the IGBT module. The transient thermal impedances under different *htcs* are shown in Fig. 4.6. As it is shown, the most influenced thermal impedance is the section from case to reference (cooling fluid temperature) due to its closer distance to the heat sink.

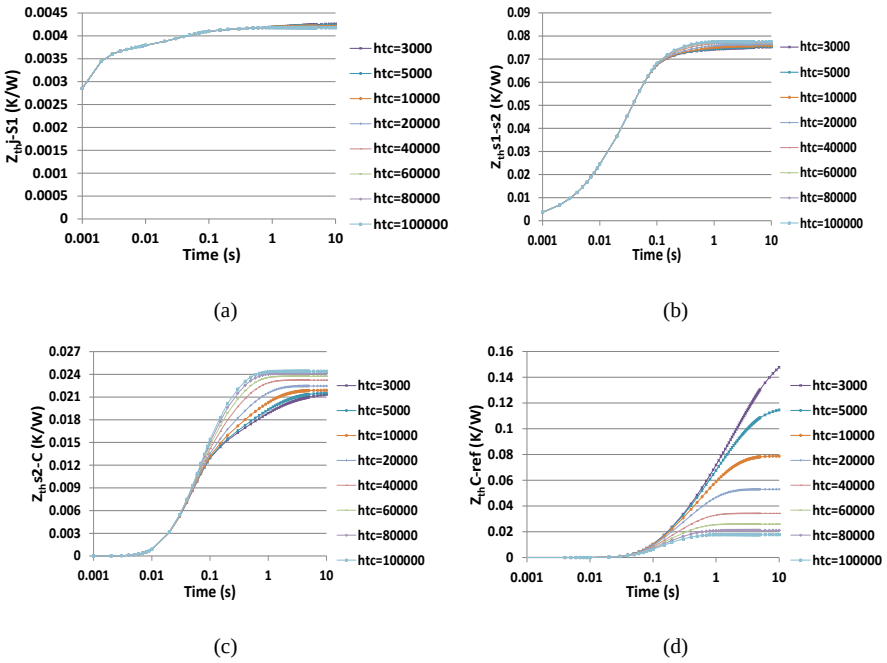
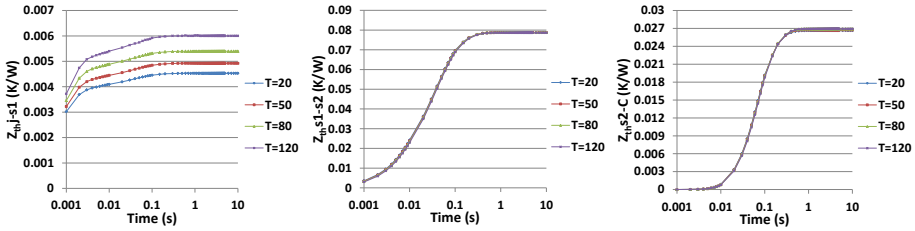


Fig. 4.6. Transient thermal impedances for different **cooling systems (*htc* in W/m^2·K)** in different layers: junction to chip solder (a), chip solder to baseplate solder (b), baseplate solder to case (c)), case to reference (d).

On the other hand, the effect of hotplate temperature variation beneath the baseplate on thermal impedance of IGBT module is studied. To model the fixed case temperature, in FEM environment, a thick wall is placed under the baseplate and boundary condition between the baseplate and wall is set to a very high *htc* (close to infinite). In this study, the case temperature is varied in the range of 20°C to 120°C. The results are shown in Fig. 4.7. As it is seen the most effected section is junction to

chip solder. The reason originates from thermal blocking behavior of the case surface of the device, which prevents the heat to be dissipated in the heat sink. So, the heat generated in the chip does not propagate to the lower layers and tends to be remained in the upper layers.



(a) (b) (c)

Fig. 4.7. Transient thermal impedances for different **hotplates (*T* in °C)** in different layers: junction to chip solder (a), chip solder to baseplate solder (b), baseplate solder to case (c).

4.3.2 **FEM modelling with variation of heat source (power losses)**

To study the effect of heat sources on thermal impedance of IGBT module, the heat sink is fixed to *htc* which is equal to *5000 W/m^2·K* and different power losses are examined in the IGBT chip. The thermal impedance at different power losses are shown in Fig. 4.8. As it can be seen, the most influenced thermal impedance is the section from junction to chip solder. The reason is that in such a short time (<10s) the heat does not have enough time to propagate from the chip to the sub-layers, and since the insulation layer has a high thermal capacitance, it slows down the heat dissipation to the heat sink. This phenomenon makes a bigger temperature difference between the upper and lower layers of the IGBT module, which increases the thermal impedance.

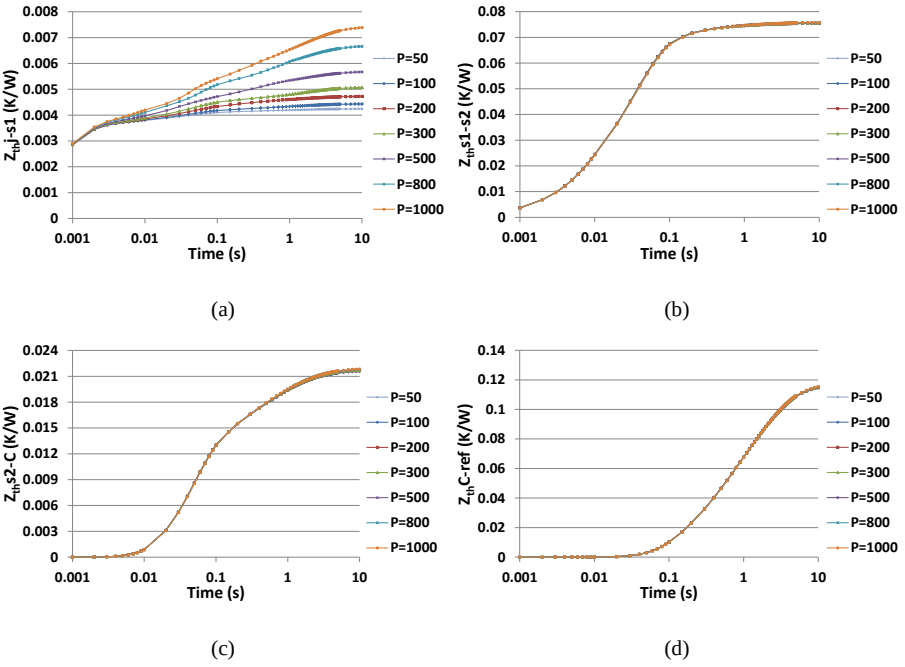


Fig. 4.8. Transient thermal impedances for different **power losses (*P* in W)** in different layers: junction to chip solder (a), chip solder to baseplate solder (b), baseplate solder to case (c)), case to reference (d).

4.3.3 **Transformation of boundary conditions from FEM to lumped RC thermal network**

In circuit simulators it is very hard to model the effect of boundary conditions in the compact thermal model. The boundary conditions need to be translated from FEM to circuit simulator in order to develop a more general thermal model. This is possible to implement by using step response analysis for different boundary conditions in FEM as described in section 4.2. For simplicity of modelling of boundary conditions, in the curve-fitting process, one RC layer is used. The RC element values in respect to the different cooling systems (*htcs*) are shown in Fig. 4.9. As proved in section 4.3.1, the highly effected regions are from baseplate solder to case and from case to reference. The variation is mathematically curve fitted to find the generic model for various cooling mechanisms. In the given curves, the horizontal axis shows different *htcs* (different cooling conditions) and the vertical axis shows the respected thermal

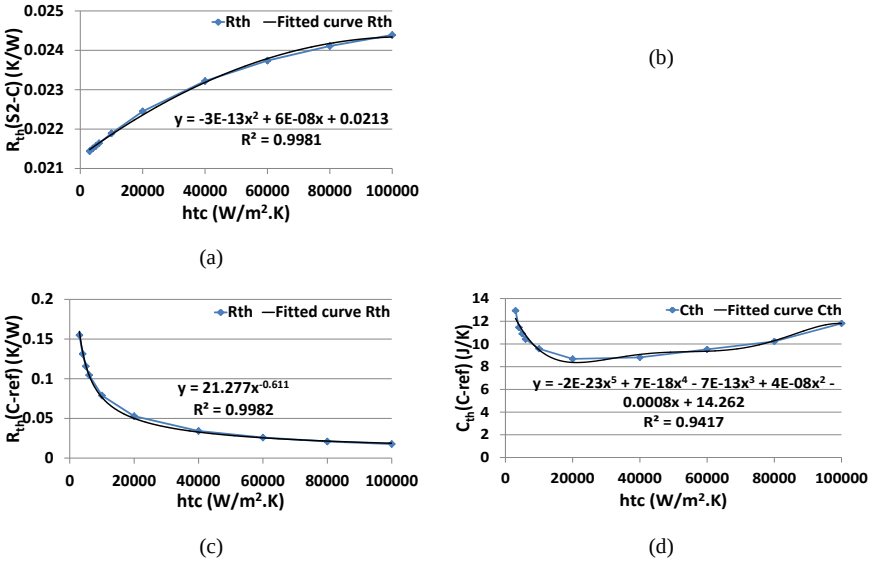
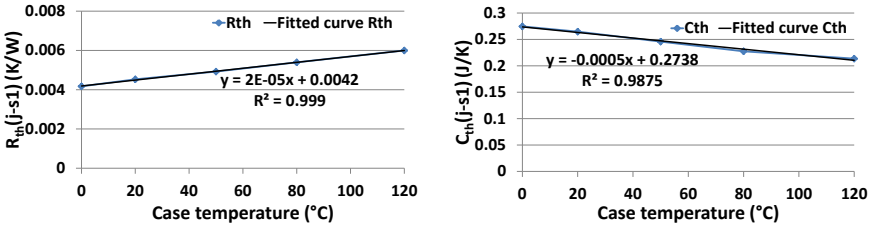


Fig. 4.9. Curve fitted thermal resistance and thermal capacitance for different cooling systems: baseplate solder to case thermal resistance (a), baseplate solder to case thermal capacitance (b), case to reference thermal resistance (c), case to reference thermal capacitance (d).

resistance and thermal capacitance values. The mathematical models representing the thermal and resistance curves based on the least squares fitting method are also shown in the figures. For all cases, the R-squared values are at least 0.9 for a better accuracy of the curve-fitting [24]. The generic thermal models for variation of hotplates and power losses are shown in Fig. 4.10 and Fig. 4.11.

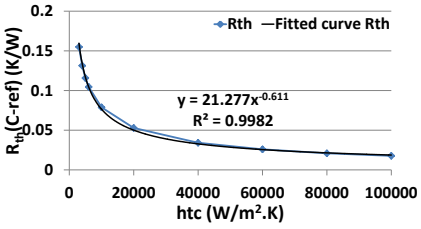
The schematic of one branch of 3D thermal network (highlighted in red in Fig. 4.3) with a variation of different boundary conditions are also shown in Fig. 4.12. As it is seen, the RC elements in the regions which are not varied by boundary conditions are shown as constant values. By variation of the RC elements in the 3D thermal network, a flexible thermal network is developed, in which RC elements are dependent on the boundary conditions. In other words, by the presented approach, thermal model of IGBT module can get feedback from the power losses and cooling system in transient operation, and calculate accurately the temperatures in different locations with very high simulation speed. A flowchart is shown in Fig. 4.13 to describe the extraction of 3D thermal network. In this figure, block 1 represents the parameters to calculate the

heat transfer coefficient of cooling system; blocks 2 to 4 represent the boundary conditions needed to adjust the thermal RC elements; block 5 represents the step response analysis in the FEM environment to calculate transient thermal impedance curves in block 6; block 7 represents the thermal RC elements calculated by curve-fitting of transient thermal impedance curves and block 8 represents the adjusted thermal RC elements using information from block 1 to 4. Applying the converter specifications, power loss on the chips are calculated in block 9. Finally, using the power losses, reference temperature and thermal RC elements, 3D thermal network is constructed in block 10 and temperatures in the monitoring points are exported.



(a) (b)

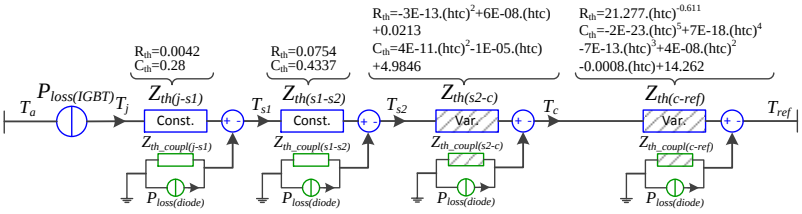
Fig. 4.10. Curve fitted thermal resistance and thermal capacitance for different **hotplates**: junction to chip solder thermal resistance (a), junction to chip solder thermal capacitance (b).



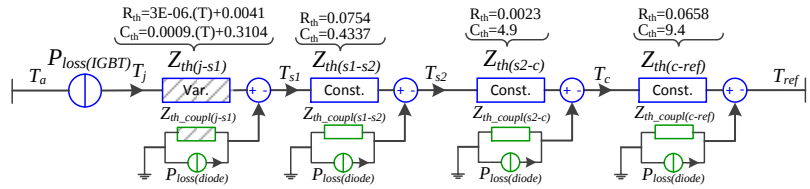
(b)

(a)

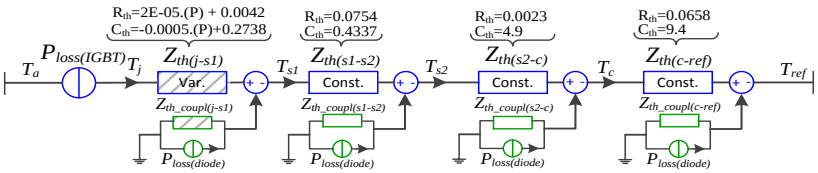
Fig. 4.11. Curve fitted thermal resistance and thermal capacitance for different **power losses**: junction to chip solder thermal resistance (a), junction to chip solder thermal capacitance (b).



(a)



(b)



(c)

Fig. 4.12. schematic of a 3D thermal network branch (highlighted in red in Fig. 4.3) with different boundary conditions: variation of fluid cooling system (a), variation of hotplate (b), variation of power losses (c).

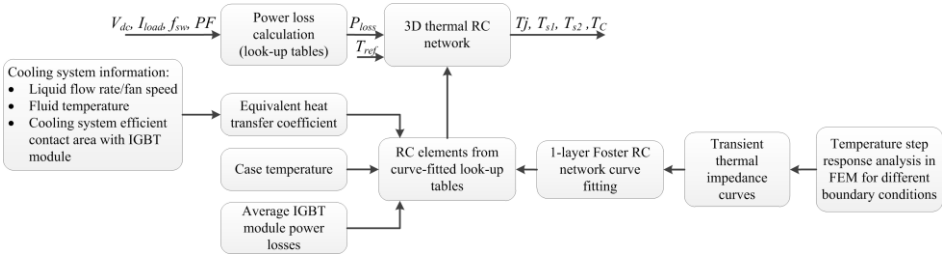


Fig. 4.13. Flowchart of the proposed boundary-dependent 3D thermal model for fast simulations.

4.4 3D thermal model verifications

To validate the 3D thermal model, first the thermal network is established in a circuit simulator environment (e.g. PLECS) and temperature responses are compared with FEM simulations (e.g. ANSYS Icepak). In order to find the power loss profile, the IGBT module is loaded with a three-phase DC-AC Two-Level Voltage Source Converter (2L-VSC). The schematic of the converter is shown in Fig. 4.14.

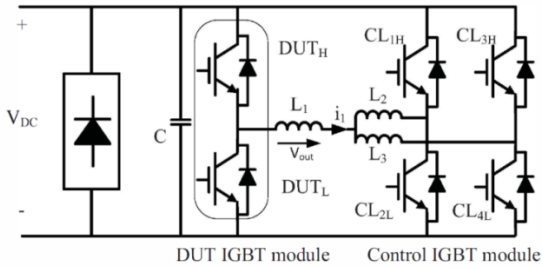


Fig. 4.14. Schematic of two-level voltage source DC-AC converter (2L-VSC).

4.4.1 **Solder temperature estimation**

The converter specifications where the IGBT module is tested are listed in Table 4.1. The IGBT, diode and other components are selected as typical values, which are typically used in grid-side inverters for wind power applications.

Table 4.1. Parameters of converter (shown in Fig. 4.14) to validate The 3D thermal model in calculation of solder temperatures.

킼口 ted output active power P_o	250 kW
Output power factor P_F	close to 1.0
DC bus voltage V_{dc}	1050 V_{DC}
Rated load current I_{load}	209 A rms
Fundamental frequency f_o	50 Hz
Switching frequency f_c	2 kHz
Filter inductance L_f	Ũ 瘐 Ãज 瘐 à□嗿 0.2 p.u.)
IGBT module	1700V/1000A

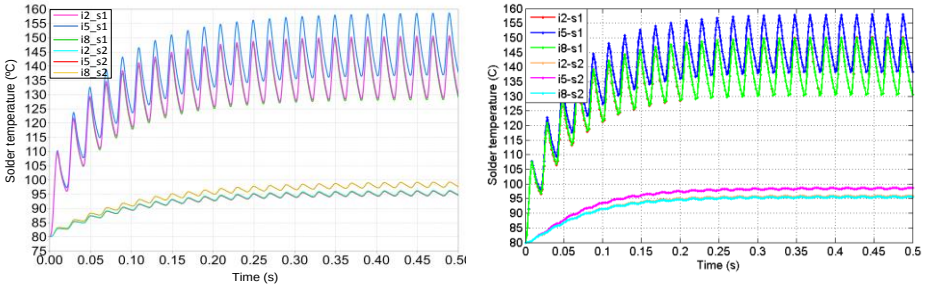
The converter conditions presented in Fig. 4.14 and Table 4.1 are used to obtain the power losses for the heat sources for the IGBT/diode chips. The loss calculations are detailed in [27]. The loss profile is injected to the network as P_{loss}*(IGBT)* and P_{loss}*(diode)* and the case temperature T_C is fixed to 80 °C. Table.4.2 shows the computer specifications and computational time needed for simulating the presented model and also the FEM model. It can be seen that the simulation time for the presented thermal network is significantly faster than the FEM analysis. However, one could believe that the time needed to extract the thermal network and implementation in the circuit simulator is longer than FEM model setup. It should be clarified that for the presented thermal model, FEM simulation is only run for two simple trials with

pulsed power loss as the inputs and the model can be used for other long-term load profiles without any more FEM simulation. Calculation of multi-layer temperature under the chips is one of the contributions of 3D thermal network, which is not possible to be calculated by manufacturer datasheet or experimental measurements due to inaccessible sub-layers. Therefore, the advantage of fast simulation is significant when a very long load profile exists (e.g. a year load profile) and fast life-time estimation is needed based on temperature cycles in the junction and the sub-layers in the module.

Table 4.2. Computational time and computer specifications for a real simulation of 0.5 s

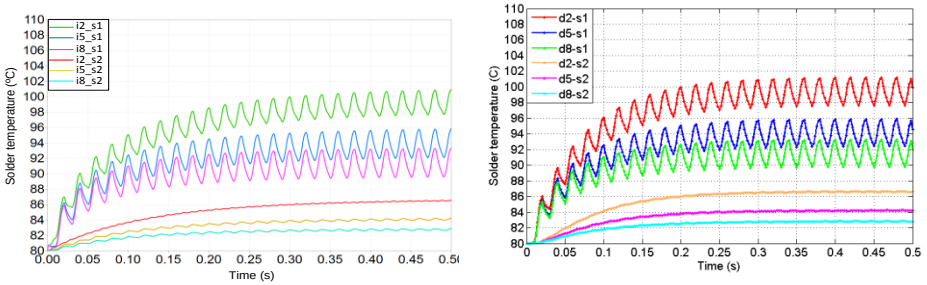
	Presented 3D thermal model simulated in PLECS	**FEM model simulated in ANSYS Icepak**
Computation time	15 seconds	12 minutes
Computer specifications	Laptop: Intel i7 3740QM, RAM 8GB	Work Station: Intel E5-2650 v2, 2.60GHz, RAM 32GB

The temperature responses on i_2, i_5 and i_8 on the IGBT chip (as previously described on Fig. 4.3) are shown in Fig. 4.15. It can be seen that the presented method and the FEM results track well each other. The highest error between the two results is 1.3 % for $i_2(s2)$ monitoring point. It is observed that the temperatures on i_2 and i_8 are very close to each other which demonstrate that no significant thermal coupling effect is seen from the diode chip. The temperature responses on d_2, d_5 and d_8 on the diode chip are given in Fig. 4.16. It is clear that d_2 point is the hottest point – even higher temperature than d_5 – which shows high thermal coupling effect not only from its IGBT chip, but also from other chips on the DCB.



(a) (b)

Fig. 4.15. IGBT chip and baseplate solder temperatures in the monitoring points i_2, i_5, and i_8 for the converter specified in Table 4.1: Simulated thermal model (a), Simulated FEM model (b).



(a) (b)

Fig. 4.16. Diode chip and baseplate solder temperatures in the monitoring points d_2, d_5, and d_8 for the converter specified in Table 4.1: Simulated thermal model (a), Simulated FEM model (b).

To compare the results of the presented 3D thermal network model in PLECS with the FEM model in ANSYS Icepak, the errors are given in percent for the average temperature differences between two models on selected monitoring points in Table 4.3. As it can be seen the highest error is for d_8 monitoring point (2.36%).

Tabel 4.3. Steady state errors of temperature difference between the presented the thermal model in PLECS and FEM model

Temperatures	**Error between PLECS and FEM results (%)**					
IGBT chip junction temp.	$\boldsymbol{i_2}$	0.84	$\boldsymbol{i_5}$	0.67	$\boldsymbol{i_8}$	0.17
IGBT chip solder1 temp.		1.08		0.4		0.36
IGBT chip solder2 temp.		1.32		0.94		0.81
Diode chip junction temp.	$\boldsymbol{d_2}$	1.39	$\boldsymbol{d_5}$	1.75	$\boldsymbol{d_8}$	2.36
Diode chip		0.97		1.29		2.07

solder1 temp.						
Diode chip solder2 temp.		0.1		0.04		0.07

4.4.2 **Boundary condition effects**

In order to verify the model in different operating points, other converter specifications are selected as the Table 4.4. First, the validity of one-layer RC Foster network comparing to a four-layer RC network (see fig. 4.3) is tested. The curve-fitting process is implemented for both cases and the extracted RC values are placed in the 3D thermal network. The conditions for the test are set as: I_{load} *= 450 A (peak),* T_{ref} *= 30 °C* and *htc = 5000 W/m*^{2}*·K*. As it is shown in Fig. 4.17, one RC layer can estimate the temperature with high accuracy comparing to multi-layer RC network. So, one-layer curve-fitting can be used for the 3D thermal network.

Table 4.4. Parameters of converter (shown in Fig. 4.13) to validate the 3D thermal model in different boundary conditions

DC bus voltage V_{dc}	450 V_{DC}
Rated load current I_{load}	variable up to 900 A (peak)
Fundamental frequency f_o	6 Hz
Switching frequency f_c	2.5 kHz
Filter inductance L_f	350 µH
Output power factor P_F	₸close to 1.0
IGBT module	1700V/1000A

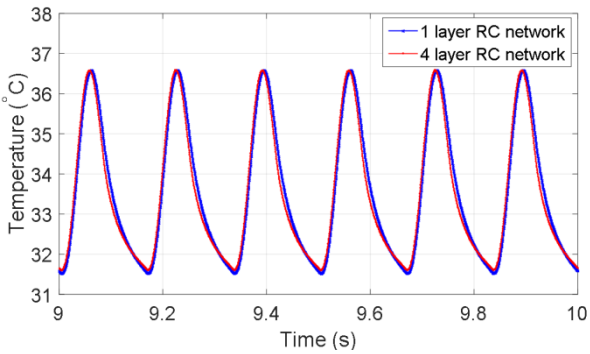
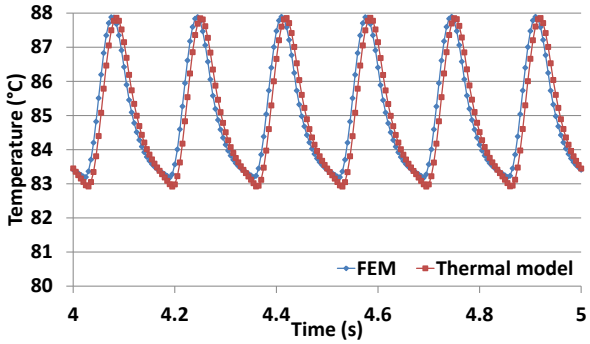


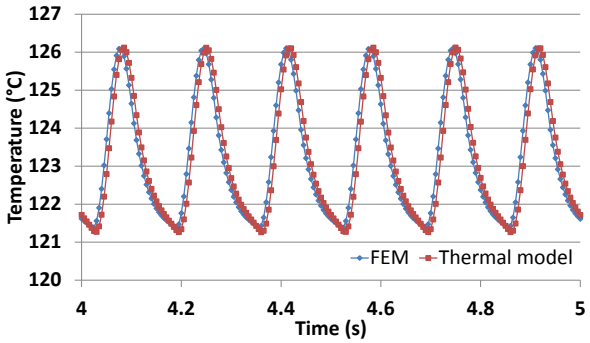
Fig. 4.17. Temperature results calculated by **1-layer** RC network comparing to **4-layer** RC network.

The junction temperature results for a selected point on the IGBT chip (i_2 in Fig. 4.3) are shown for the cases of *htc=20000 W/m*^{2}*·K,* T_C*= 120 °C,* and P_{loss}*=100 W*. As it

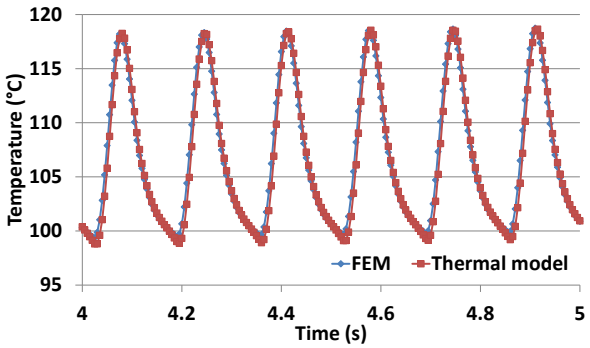
is clear in Fig. 4.18, the thermal model is consistent with the FEM simulation. The errors between the thermal model and FEM simulations for all cases are less than 1%.



(a)



(b)



(c)

Fig. 4.18. Junction temperatures from simulated 3D thermal model and comparing to FEM model in different boundary conditions: *htc=20000 W/m²·K* (a), T_C*= 120 °C* (b), P_{loss}*=100 W* (c).

4.4.3 **Experimental verification**

In this section, the simulated temperatures extracted from the 3D thermal model are compared with the measurements from the experimental setup. For this purpose, a test circuit is set with the specifications given in Table. 4.4. The fundamental frequency of the converter is set to 6 Hz, which is usual in reliability power cycling tests [28]. A test setup featured with an Infra-Red (IR) camera is shown in Fig. 4.19. A black painted and opened IGBT module is being tested in a full bridge test circuit which is shown in Fig. 4.14. The upper chip pairs in the IGBT module under the test are shown as DUT_H and the lower chip pairs are shown as DUT_L. An online temperature measurement is performed by the IR thermal camera at every five minutes in normal operating conditions to prevent oversized data collection.

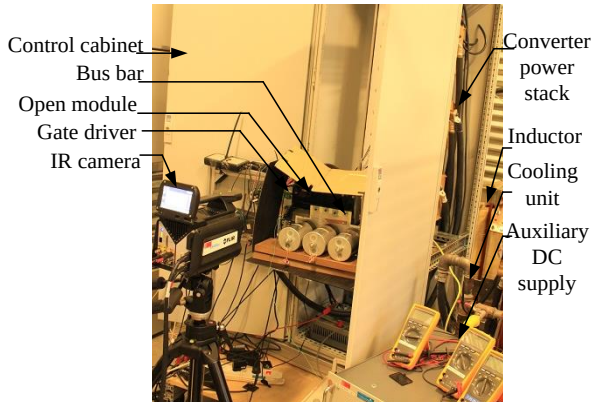


Fig. 4.19. Test set up featured with IR camera for validation of model.

In the first test, the IGBT module is mounted on a hotplate with the temperature fixed to 88°C±0.5°C throughout the test. The infrared thermal image of one DCB section of the IGBT module is shown in Fig. 4.20. To validate the 3D thermal model, same-located points as the 3D thermal networks are taken on the surface of the IGBT chip and the diode chip. The monitoring points should be considered between the wire-bonds and be on the surface of the chips to prevent false temperature monitoring of wire-bonds.

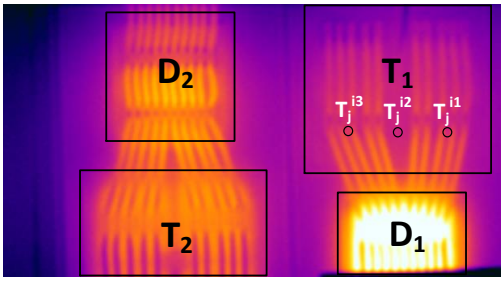


Fig. 4.20. Infrared thermal image of one DCB section of IGBT module.

In the 3D thermal network, average power losses of the chips are calculated according to datasheet information. The average power losses, which are generated in each IGBT chip and diode chip are shown in Fig. 4.21. The power losses are calculated using the methods mentioned in [27], where the temperature feedbacks to the loss calculation are considered.

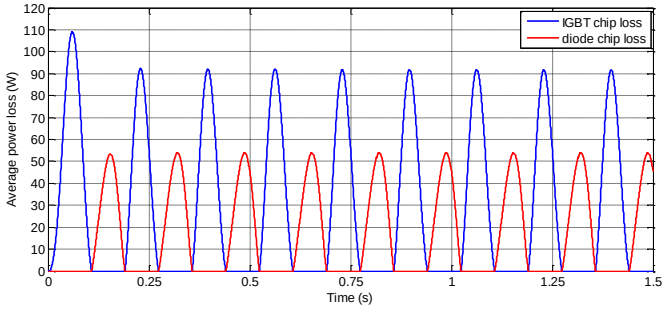


Fig. 4.21. Average power losses generated in the IGBT chip and diode chip in the experiment.

Since the hotplate is not an efficient cooling system, in the FEM, it is considered as a thick plate with very high *htc* and very low thermal resistance in the boundary of the IGBT module and the heatsink. The baseplate temperature, which is measured in the experimental setup during the test is shown in Fig. 4.22. The temperature is fluctuating around 88°C with a slight increasing slope. So, in the FEM simulation the equivalent *htc* is considered as 100000 W/m^2.K. With this *htc*, FEM simulations show the same slope in the increase of baseplate temperature. Assigning these boundary conditions, the FEM simulations are performed to extract the 3D thermal network RC elements.

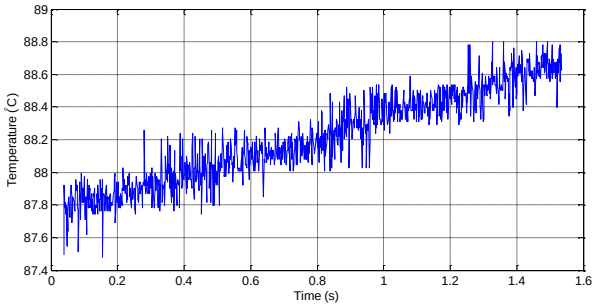
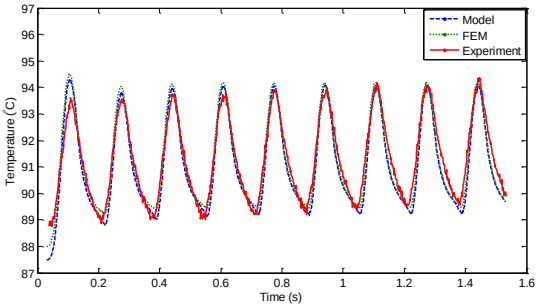
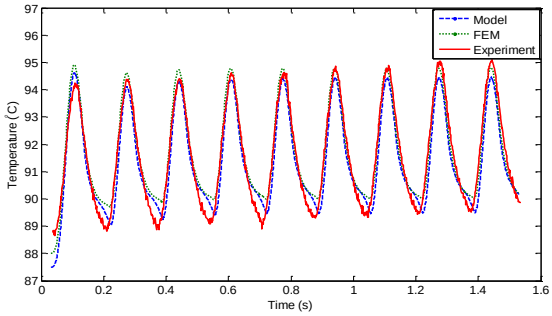


Fig. 4.22. Baseplate temperature measured in the experiment.

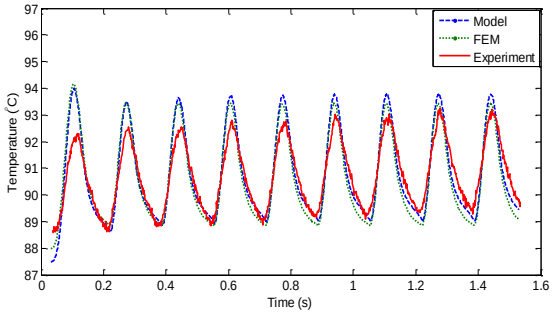
The temperature curves for three monitoring points on the IGBT chip including i_1, i_2 and i_3 are shown in Fig. 4.23. These monitoring points are selected since they are closer to the diode chip and suitable to validate the model in the case of a high thermal coupling effect. The temperature curves are compared with the proposed 3d thermal model, FEM simulations and measurements. The amount of peak-to-peak temperature error between the results by the simulated model and the tests are 3 %, 6 % and 8 % for i_1, i_2 and i_3 respectively. But the simulated model results are consistent with the FEM simulation results with errors less than 1 %. Therefore the 3D thermal network results show satisfactory performance compared to the FEM analysis and experimental results.



(a)



(b)



(c)

Fig. 4.23. IGBT chip surface temperatures by 3D thermal model, FEM analysis and experimental measurements, i_1 (a), i_2 (b), and i_3 (c).

In order to validate the 3D thermal model in different loads, which lead to different power losses, the IGBT module is mounted on a direct liquid cooling system as shown in Fig. 4.24, where the liquid temperature and flow rate can be controlled for each experiment and cool down the IGBT module homogenously [29]. The infrared thermal image of one DCB section of IGBT module is shown in Fig. 4.25. In this test the temperature monitoring points are selected as i_2, i_5 and i_8.

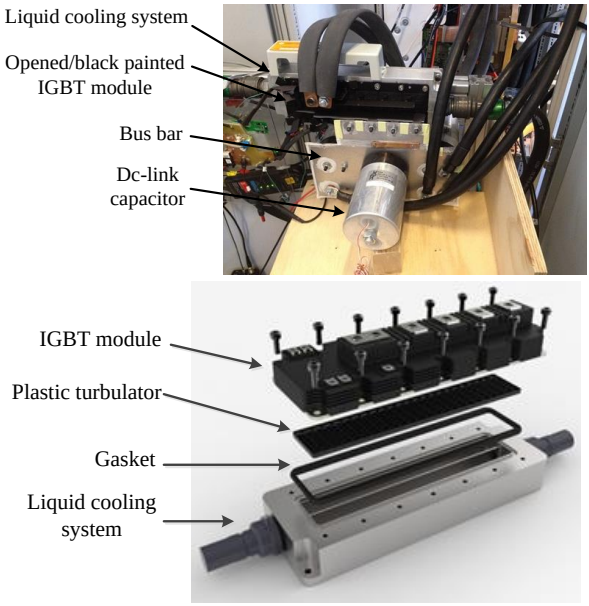


Fig. 4.24. IGBT module mounted on cooling system.

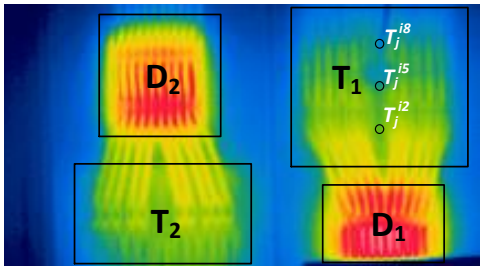
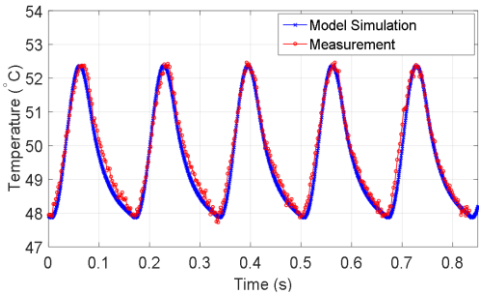


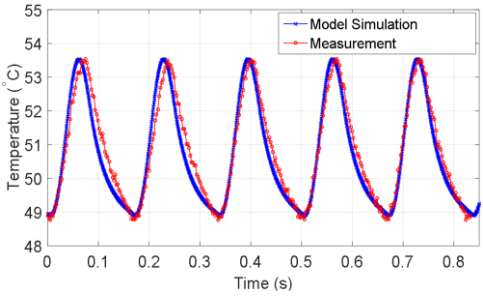
Fig. 4.25. Thermography of one DCB section at the surface of IGBT module.

In the first experiment, the peak of the load current, $I_{load(peak)}$, is fixed to 500 A, cooling liquid flow rate, $\dot{V}$, is set to 5 m^3/hr and cooling liquid temperature ,T_{ref}, is set to 45°C. For the cooling system, the equivalent *htc* is set to 7000 W/m^2·K as suggested by the manufacturer of the cooling system for the mentioned flow rate. Since it is difficult to access the accurate power losses in the experimental setup, the power losses used in the 3D thermal model are calculated based on the IGBT module datasheet, and power losses injected to the thermal model are adjusted in such a way to achieve the same case temperature as the experimental setup. However, the loss is only adjusted within ±10%, which is a reasonable range for the loss estimation error by datasheet.

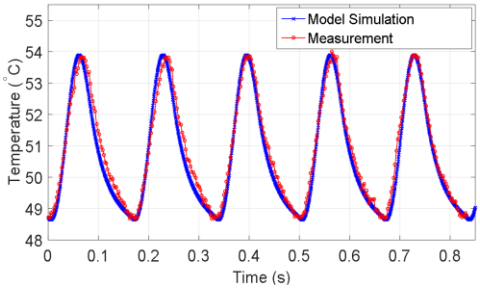
The results are shown in Fig. 4.26. The boundary-dependent 3D thermal model accurately calculates the same junction temperatures as in experimental results. As mentioned earlier in this chapter, the main feature in the presented thermal model is of high accuracy in the calculation of steady-state peak-to-peak temperature, ΔT, and maximum temperature, T_{max}, of junction temperature, which are the main factors in life-time models for IGBT modules [23]. For both parameters, the thermal model shows less than 2% error in steady state compared to experimental results.



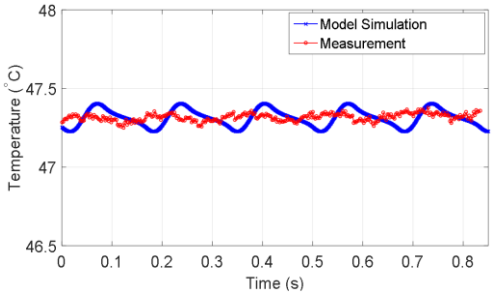
(a)



(b)



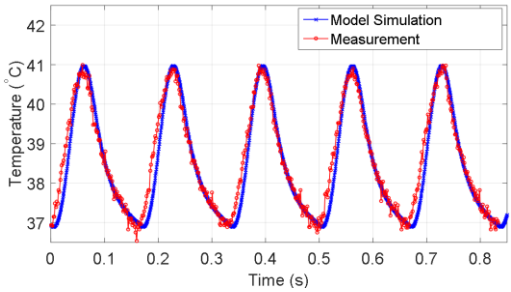
(c)



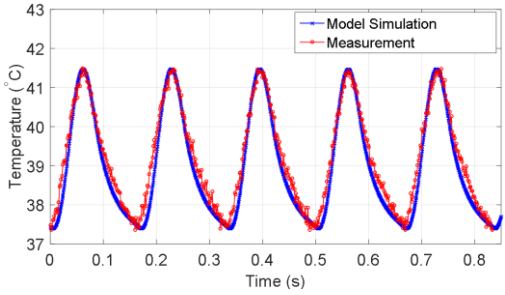
(d)

Fig. 4.26. Junction and case temperature by thermal model simulation and experimental measurement in $\boldsymbol{I_{load(peak)}}$**= 500 A**: i_2 (a), i_5 (b), i_8 (c), case (d).

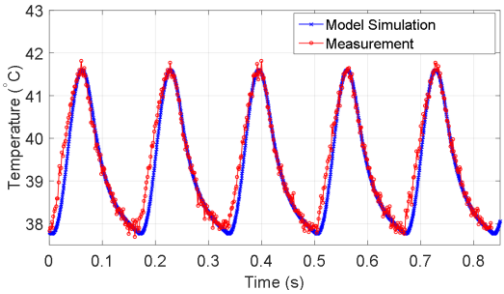
To be ensured about the validity of thermal model on other boundary conditions, the next validations are implemented for these conditions: $I_{load(peak)}$= 400 A, $\dot{V}$= 5 m^3/hr, and $T_{cooling}$=30°C. Results are shown in Fig. 4.27 for temperature monitoring points: i_2, i_5 and i_8. Similarly to the previous case, thermal model results are consistent with the experiment results for both ΔT and T_{max}.



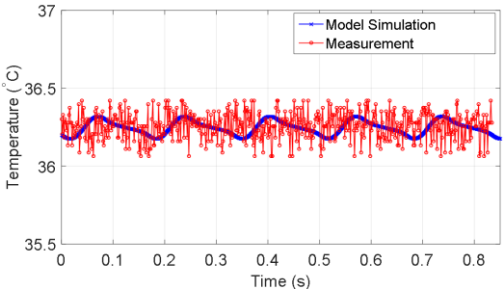
(a)



(b)



(c)



(d)

Fig. 4.27. Junction and case temperature by thermal model simulation and experimental measurement in $\boldsymbol{I_{load(peak)}}$**= 400 A**: i_2 (a), i_5 (b), i_8 (c), case (d).

4.5 Conclusions

In this chapter a detailed 3D thermal model of IGBT modules has been presented. This thermal network contains the self-heating and thermal coupling between the chips as well as multi-locations and multi-layer thermal behaviors of the IGBT module. The lumped RC elements of thermal network have been extracted by step response analysis of FEM model in different loading and cooling conditions. The extracted temperature step responses are modelled as self-heating and heat-coupling Foster thermal networks by accurate curve fitting process. In addition, the influence of different boundary conditions on the transient thermal behavior of the IGBT modules has been investigated. It was shown that with larger heat transfer coefficients, the junction to case thermal impedances are increased due to the less heat spreading inside the IGBT module. The presented thermal model was verified by FEM analysis and experiments. In summary, the model is highly consistent with the FEM model and show low errors

compared to experimental results. The presented thermal model is fast and very easy to be applied in all circuit simulators for long-term dynamic load profiles. Moreover, the 3D thermal network estimates the temperatures in critical layers of IGBT module such as solders which is used by power converter designers for fast life-time estimation of IGBT modules considering real operating conditions and longer time duration assessment. Regarding the limitations, the 3D thermal network is dependent on the physical properties of the IGBT module, so with different geometries and materials, the RC elements inside the thermal network get new values. However, the structure of the thermal model remains the same in all conditions.

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Chapter 5

Design of cooling system for high power IGBT modules

Power electronic devices like the high power IGBT modules generate significant amount of losses which needs to be dissipated to ensure a safe operation. The heat is generated in semiconductor chips due to conduction and switching losses and they can result in large heat dissipation. Moreover, as the devices and packages become more compact, the generated losses lead to extremely large heat fluxes inside the module – typically *300 W/cm*^{2} and more [1]. Therefore, thermal management of power devices – e.g. cooling system design – becomes crucial for a reliable performance of converter. This is more critical when designing a high power module with multi-chips, because thermal coupling effects among chips intensify loading of chips.

Cooling the high power modules with heat dissipations higher than *300 W/cm*^{2} is beyond the capabilities of conventional air cooling systems [1]. On the other hand, liquid cooling systems, surpass the air cooling systems with heat transfer coefficient several order of magnitudes higher and enables much higher power densities of power modules and more compact converter solutions. Today, various liquid cooling solutions have been introduced which generally classified in two groups of indirect and direct liquid cooling [2]-[10]. In indirect cooling, the power module is mounted on a cooler, e.g. cold plate which is fabricated by pressed-in copper tubes in aluminum extrusions or gun drilling holes in aluminum plates. An example of which is shown in Fig. 5.1 [11]. A Thermal Interface Material (TIM) is used between the power module and cold plate for higher heat conduction to the cold plate.

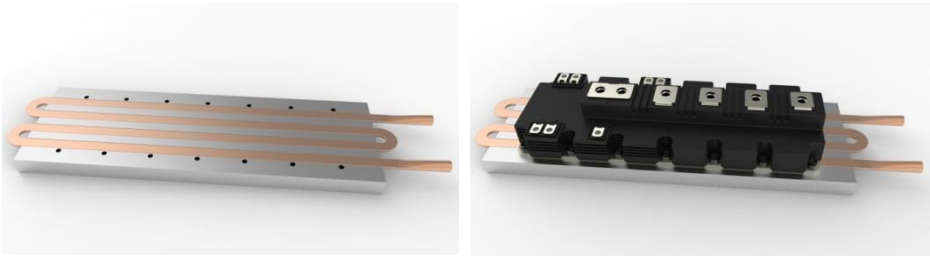

Fig. 5.1. Cold plate for a P3 IGBT module [11].

On the other hand, in direct cooling systems, in which the coolant is directly contacted with the power module without any interfacing layer, the efficiency of cooling system increases by increasing the efficient cooling contact surface and eliminating the TIM layer, thus reducing the junction-to-ambient thermal resistance [10]. Direct liquid cooling systems eliminates TIM that is traditionally needed between the power module and the cold plate. Because, the TIM layer accounts for 30%-50% of the junction to coolant thermal resistance, elimination of TIM results in an improved thermal management for the power module. Since the dominant failure mechanisms are due to thermal stresses, this will also leads to a higher reliability. Direct liquid cooling system is commonly done by various pin fin designs such as the one which is shown in Fig. 5. 2 where a high power IGBT module is equipped with a baseplate with pin fins [11].

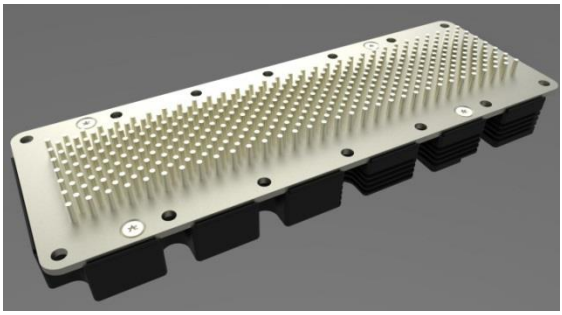

Fig. 5.2. A baseplate with pin fins for a P3 IGBT module [11].

Today, commercial Computational Fluid Dynamic (CFD) simulators such as ANSYS® have facilitated the calculations for cooling system design, thus reduce the time-consuming and costly experimental tests. CFD can predict the liquid flow in fluid

channels of cooling system in order to identify correct heat transfers and pressure drop conditions. Heat transfer rates, in turn, can be used to calculate the junction temperature in dynamic operation of power module. In this chapter, a design tool for optimization of direct liquid cooling system is developed using Computer Aided Design (CAD) software, SOLIDWORKS®. Various physical parameters which influence the performance of cooling system in different applications are studied and applied in the design tool. The design tool is validated by ANSYS® for a given operating condition and performance index.

5.1 ShowerPower® cooling system

One of the concepts of using pin fins for direct liquid cooling is the ShowerPower® developed by Danfoss (see Fig. 5.3) [10]. The main idea for the concept was to solve the classical problem associated with liquid cooling of power modules, i.e.:

- Inhomogeneous cooling due to the calorimetric heating up of the coolant,
- TIM- related quality issues like pump-out and dry-out effects.

Therefore the key features of the ShowerPower® cooling system are:

- Capability to homogeneously cool large baseplate of power modules or stack of power modules, so eliminating temperature gradients and facilitating paralleling of many power semiconductor chips on a common substrate,
- No TIM-related pump-out and dry-out effects.

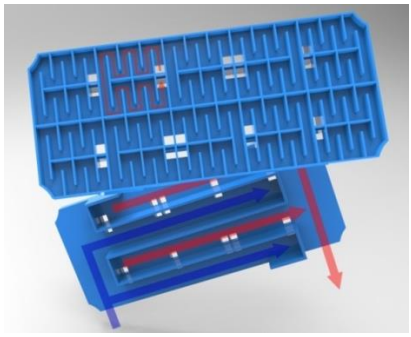

Fig. 5.3. The ShowerPower® turbolator [10].

In ShowerPower®, a plastic turbulator is placed between the cooling bath tub and baseplate of power module as shown in Fig 5.4. The turbulator forces the coolant to flow along the power module baseplate in several isolated channels, thereby supplying a homogenous cooling of large baseplate of high power module. In spite of its name, the turbulator does not produce a turbulent liquid flow, but a laminar flow under normal flow rates of the coolant. The plastic turbulator consists of several cooling cells in the horizontal and vertical directions, which is supplied by a manifold structure on the backside for a uniform liquid temperature in all channels. The cold liquid enters the channels and flows through the channel fins where their heights are less than side walls (see Fig. 5.5). This feature provides the power module a two-step cooling: first the cold liquid enters the channel through the channel inlet and cools down the contact surface of the power module baseplate in top region of the fins and channels. On the other hand, a portion of cold liquid flows through the lower part of the channel. The second cooling step of liquid occurs when the hot and cold liquids meet in the backside of the fins.

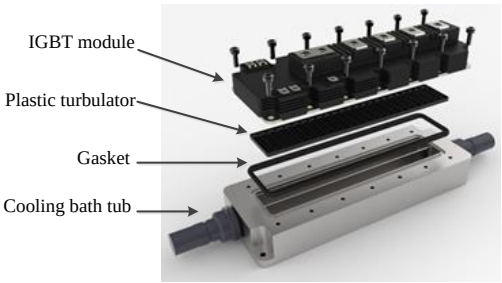

Fig. 5.4. Power module and cooler [11].

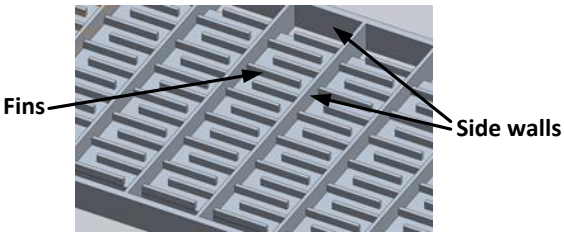

Fig. 5.5. Fins and side walls in ShowerPower®.

5.2 Considerations in the design of cooling system

Simulations (thermal, fluid, mechanical, vibrational etc.) are important in the product development in order to reduce the number of time-consuming and costly tests. The best way to simulate a liquid cooling system is to use CFD simulations. Here the fluid flow is solved numerically so that the correct heat transfer rates and pressure conditions are found and thus the relevant temperatures, e.g. semiconductor junction temperatures are found and can be used for lifetime predictions.

When designing a fluid cooling system in the CFD simulation, several issues should be considered in order to ensure an optimized layout which delivers the performance needed over the required lifetime of the system. The main factors, which influence the thermal performance of the liquid cooling system, are: the contact surface of the coolant, the volumetric flow rate and pressure drop of the coolant, the heat capacitance of the coolant, heat conduction and heat spreading in the heatsink and the coolant temperature [12]. By increasing the contact surface of the coolant with the power module, heat transfer will be improved. In the other words, the complex shape of the liquid cooling system and thus high flow velocity leads to a turbulent flow which considerably reduces the thermal resistance between the coolant and baseplate of power module. Knowing the operating points, thermal resistance can be defined as a function of the volumetric flow rate:

$$R_{th(s-a)2} = R_{th(s-a)1} \cdot \left(\frac{\dot{V}_1}{\dot{V}_2}\right)^K \tag{5.1}$$

where $R_{th(s-a)}$ is the thermal resistance between the baseplate and coolant, $\dot{V}$ is the volumetric flow rate and K is a constant value between 0.3 and 0.5 [12]. In most applications, a pump is utilized to circulate the coolant. The exiting pumping power can be used to provide the required coolant volumetric flow. Pressure drop across the cooling system is a function of squared volumetric flow rate:

$$\Delta P\ [mbar] = M \times \dot{V}^2 \tag{5.2}$$

where ΔP is the pressure drop across the cooling system, $\dot{V}$ is the volumetric flow rate and M is a constant value defined by the geometry of cooling system. Increasing the coolant flow rate decreases the thermal resistance, but the pressure drop across the cooling system increases. Therefore, it is tried to keep both parameters at minimum level as higher thermal resistance increases the junction temperature and higher pressure drop demands for higher power of the pump.

5.3 Optimization design tool for ShowerPower® cooling system

According to section 5.2, in a case of predefined pump power and volumetric flow rate by customer, a trade-off is needed between thermal resistance and pressure drop in the design of cooling system. The turbulator geometric parameters have high influence on cooling system performance. These geometric parameters include width of channel, depth of channel, height of fins, amount of channels per meander and channel cross section area to avoid the risk of blockage (see Fig.5.5 and Fig.5.6). On the other hand, with less order of importance, cooling bathtub geometries also influence the cooling system thermal performance. The effective bathtub geometric parameters are the main inlet/outlet sizes and the main channel widths.

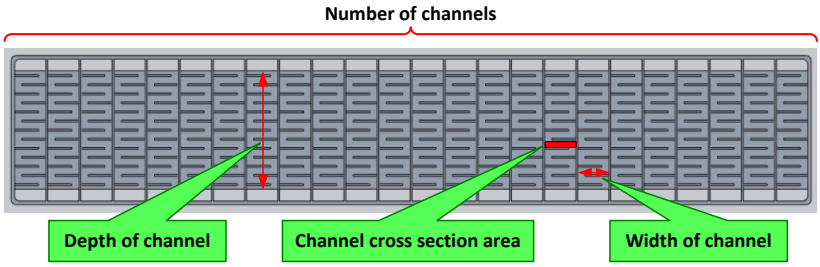

Fig. 5.6. Geometric parameters in the turbulator of ShowerPower®.

In order to create different geometries for the cooling system, a design platform is developed in SOLIDWORKS®. For this reason, first the default geometry of the turbulator is modelled. The turbulator of the cooling system under study is designed to cool the baseplate of a P3 IGBT module. Therefore, the size of the turbulator is the same as the effective heat dissipation area (substrate area) and it will not be changed during the parametrization. The minimum thickness of the side walls and fins are also

kept as fixed values, which can be fabricated by a CNC milling machine. The other mentioned geometric parameters are defined in the window of "Equations, Global Variables, and Dimensions" in SOLIDWORKS®. Since change of one geometric parameter may cause to change in other parameters, parametrization of geometries starts from inner ones, i.e. the parameters inside one channel. In the next stage, number of channels is parametrized with dependent variables to the inner geometries.

Moreover, the geometric parameters are defined for the cooling bathtub. Fig. 5.7 shows a cooling bathtub including the gasket space. To improve the efficiency of the cooling system, the efficient cooling area in the contact surface to the baseplate should be increased. For this reason, some solutions are suggested. It has been observed that the gasket thickness is a parameter, which reduces the efficient contact surface of the cooling system. In addition, there has been a unused distance between the turbulator and the screws, so the effective contact surface has been increased by increasing the size of turbulator and use more efficient contact surface. Finally, the inlet diameter of the cooling bath tub have been made as variable since the inlet size is effective in pressure drop rate of the fluid in the cooling system.

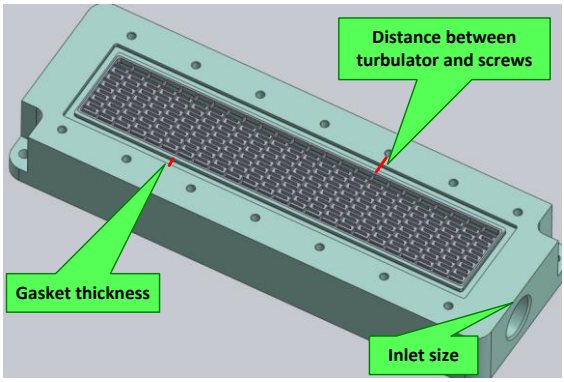

Fig. 5.7. Geometric parameters in the cooling bathtub of ShowerPower®.

By using this design platform, manufacturer can change any effective geometric parameters in both cooling bathtub and plastic turbulator to achieve optimized design according to customer requirements. A view of the developed toolbox in SOLIDWORKS® is shown in Fig. 5.8. "Global Variables" column include the

geometric parameters, “Value/Equation” column include the geometric relative equations and “Evaluates to” column include the calculated values for each parameter. The default turbulator channels are designed in such a way to have at least one turbulator channel for each IGBT/diode pair as shown in Fig. 5.9.

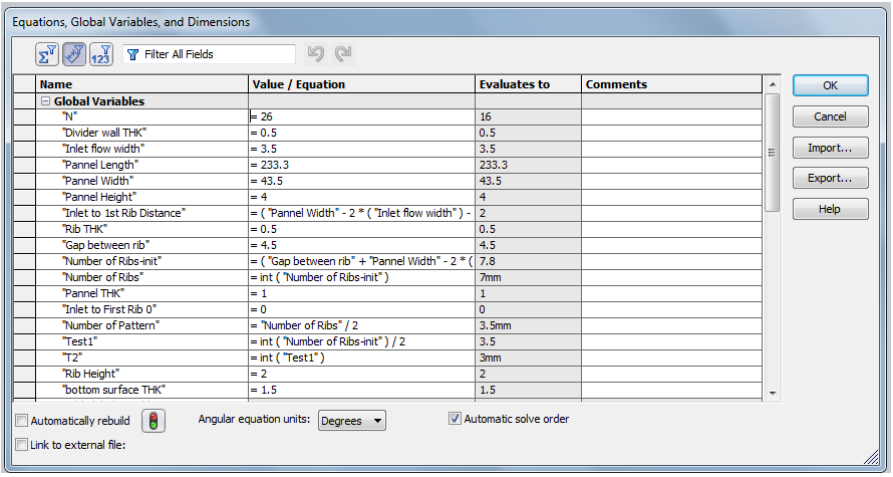

Fig. 5.8. ShowerPower® cooling system design platform developed in SOLIDWORKS®.

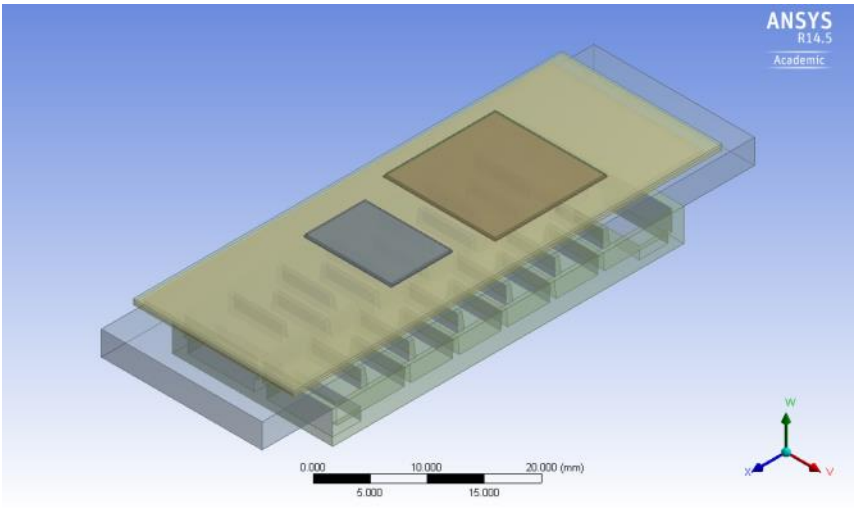

Fig. 5.9. One section of IGBT/diode pair mounted on a cooling channel of ShowerPower® simulated in ANSYS Icepak.

5.4 CFD verification

To assure the functionality of the design platform, the default cooling system is simulated in CFD software (ANSYS Icepak®) to cool down a P3 IGBT module with a certain power losses as shown in Fig. 5.10.

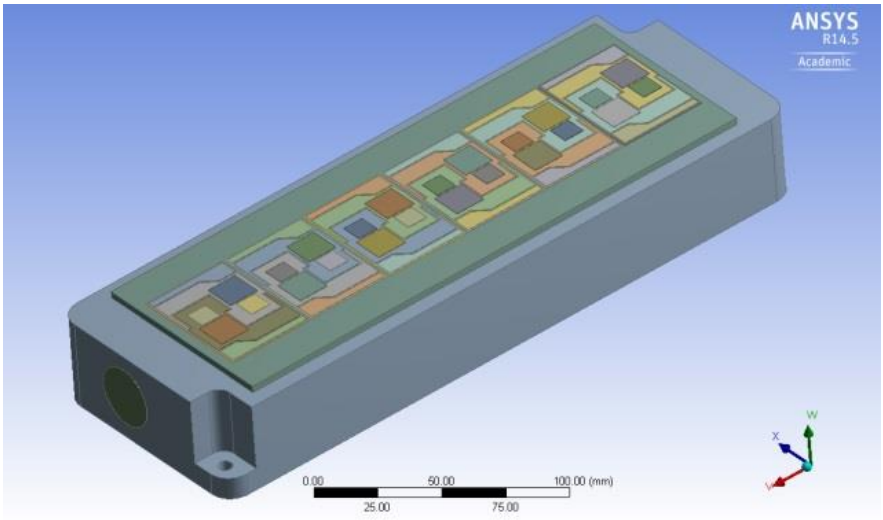

Fig. 5.10. P3 module mounted on ShowerPower® cooling system simulated in ANSYS Icepak®.

The simulation is performed with *50 W* power losses on the IGBT chips and *25 W* power losses on the diode chips. The cooling fluid is selected as glycol 50-water 50, volumetric fluid flow rate is set to *5 l/m*, the inlet fluid temperature is fixed to *20°C* and the output fluid pressure is set to ambient static pressure. Fig. 5.11 shows the fluid flow inside the channels that confirms the correct operation of cooling system. The temperature profile on the surface of the IGBT module is shown in Fig. 5.12.

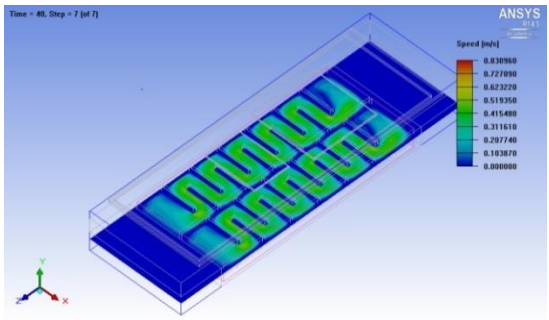

Fig. 5.11. Fluid flow inside the cooling turbulator of ShowerPower®.

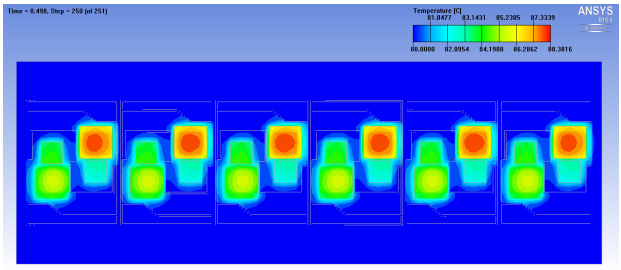

Fig. 5.12. Simulated P3 IGBT module: Temperature profile of the P3 module mounted on ShowerPower® cooling system.

As an example, the number of channels in the tabulator is set as the variable factor. The CFD simulations are implemented for different number of channels from 15 to 40. As it is seen in Fig. 5.13, increase of the channel numbers lead to reduction in the thermal resistance and increase of pressure drop.

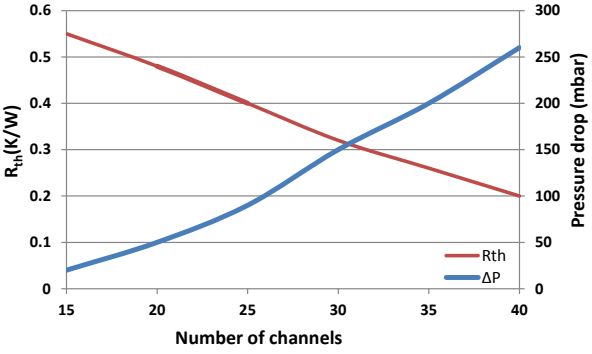

Fig. 5.13. Thermal resistance for a single IGBT chip and pressure drop (ΔP) performance curves vs. number of turbulator channel numbers for ShowerPower® cooling system.

5.5 Conclusions

In this chapter, the concept of cooling system for power modules has been explained. Different types of liquid cooling systems, their pros and cons have been briefly discussed. According to the discussions, the operating principles of ShowerPower® cooling system have been explained, which shows high efficiency in removing the heat homogenously. It has also been shown that depending on the cooling system application, minimum thermal resistance and minimum pressure drop are required to keep the chips junction temperature low along with saving power of cooling system pump. Therefore, a design platform has been developed which can be used to optimize the geometries of the cooling system in respect to the least thermal resistance and pressure drop. Finally, CFD simulation results have been presented to validate the operation of design tool in extraction of optimized cooling system. Using this design platform will enable the cooling system manufacturer to design the cooling system based on the heat generated in the IGBT module and the available pump power. This tool enables to design a cooling system with higher efficiency. The cooling system manufacturer can fabricate the optimized plastic turbulator depending on the application by 3D printing with the least manufacturing costs.

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Chapter 6

Electrical parasitics modelling of power modules

Ideally, it is desired to manufacture power module which is low cost, small in size, very efficient, and highly reliable. Besides, the switching frequency at which the power module is operating, determines how fast the semiconductor switches can modulate to control the power flow. At higher switching frequencies the passive components such as capacitors, inductors and high frequency transformers can be reduced in size that will reduce the cost of the overall system and increases efficiency [1]. However, as the switching frequency is increased, depending on the semiconductor devices, the switching losses of the power module will overcome the efficiency gains. Moreover, in higher switching frequencies, the electrical parasitics become an important issue to decrease the reliability of power electronic system. In this chapter, methods to extract electrical parasitics in power modules are explained and a power module layout is optimized regarding the minimum electrical parasitics.

6.1 Electrical parasitics in power modules

Electrical parasitics in the power modules are the inductances, the resistances, and the capacitances that exist in the copper traces, the terminals, and the bond wires of power modules unintentionally. Electrical parasitics may affect the lifetime of the power module or even casue to catastrophic failures by increasing the switching losses, voltage spikes and Electro-Magnetic- Interference (EMI) issues. However in the power module, by integration of power semiconductor chips and control circuitry in a compact package and thus reducing the conductor path, the electrical parasitics are reduced [2].

Among the electrical parasitics existing in the power modules, stray loop inductances account for the major part. As it is shown in Fig. 6.1(a), stray inductances exist in the current flow path including leads, traces and bond wires. In the commutation time when the devices are turned off, the current decreases and voltage increases on the parasitic inductances. In the case of large stray inductances and high

switching frequency, a large voltage spike appears that may highly stresses the semiconductor devices. In the Fig. 6.1(a) the stray inductances associated with the drain, the source, and the bond wires of a power MOSFET module with two half-bridge topologies have been labeled by L_D, L_S and L_L. The terminals stray inductances have not been shown due to their fixed position in the layout in the design process. Apart from the main loop inductance, the stray inductance in the gate driving path of the switches (Fig. 6.1(b)) can also cause to parasitic effects that lead to ringing effects in the turn-off mode of the switches [3].

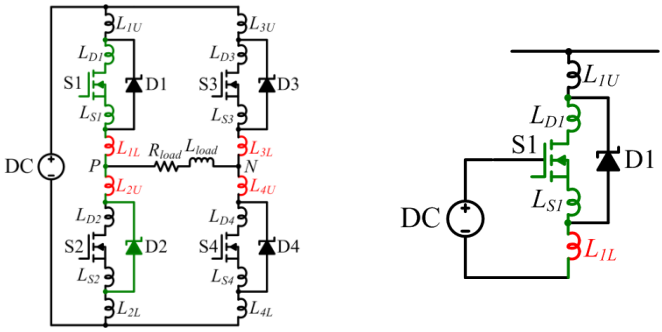


Fig. 6.1. Loop stray inductance in the main switching loop (a), and the gate driving loop (b).

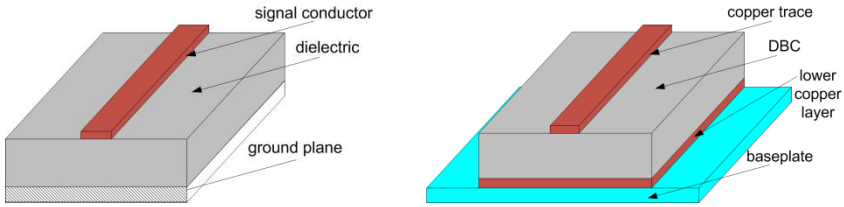
6.2 Extraction of Electrical parasitics

Currently, the layout design of power modules is generally done manually, although some softwares have been developed to facilitate the design process. Most software tools apply the Finite Element Method (FEM) or the Finite Difference Method (FDM), to solve Maxwell's differential equations. However, these numerical methods demand for time-consuming computation facilities. Therefore, faster solutions are needed to extract the electrical parasitics in the power modules [4].

In a layout design process of the power modules based on reduction of the electrical parasitics, geometries including traces, bond wires, and chip positions as well as material properties are varied to obtain the solution. In the following, two methods to extract the electrical parasitics are explained one based on the micro-strip transmission line structure [3], and the other based on a simplified evaluation index.

6.2.1 **Micro-strip transmission line structure**

One of the methods to model the electrical parasitics in the power module is to use micro-strip structure. As it is shown in Fig. 6.2(a), the micro-strip structure consists of a metal layer (signal conductor), an isolation layer (dielectric) and an infinite ground plane. On the other hand, a power module consists of a top metal layer (copper trace), an isolation layer (DBC) and a finite ground plane (baseplate and lower copper layer). The major difference between the micro-strip structure and the power module is the finite ground plane in the former structure and infinite ground plane in the latter structure [3].



(a) (b)

Fig. 6. 2. Comparison between micro-strip transmission line structure (a), and power module (b).

In the case of using a micro-strip structure with infinite ground plane, parasitic inductances are extracted with high error compared to FEM model. This is due to a high effect of ground plane on the parasitic inductance model. So an average model is used between a micro-strip structure with and without ground plane that reduces the error in the inductance model to 10% compared to the FEM model [3]. The simplified equation to calculate the inductance in a micro-strip structure with a ground plane effect can be obtained by [5]

$$L' = l\frac{Z_0}{c}\sqrt{\mu_r \epsilon_{eff}} \ . \tag{6.1}$$

where l is the conductor length, Z_0 is the characteristic impedance, c is the light speed in vacuum, μ_r is the relative magnetic permeability of the dielectric, and ϵ_{eff} is the effective relative permittivity of the dielectric.

In the case of a traces without ground plane effect, simplified closed-form equation for inductance are given by [3]

$$L' = \frac{\mu_0 l}{2\pi}\left[\log\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{2}{9}\left(\frac{w+t}{l}\right)\right]. \tag{6.2}$$

where μ_0 is the vacuum permeability of free space, l is the trace length, w is the trace width, and t is the trace thickness.

Finally a parasitic inductance model for the power module with acceptable accuracy can be obtained by averaging of the inductance model with and without the ground plane effect

$$L = \frac{L' + L''}{2} \tag{6.3}$$

The inductance model based on the micro-strip structure gives equations with geometries and material properties of traces in the power module by breaking into rectangular pieces and can be used in the optimization process [4]. The full list of equations and validation of the model are described in [3].

6.2.2 **Simplified parasitic inductance evaluation index**

Another method to estimate the parasitic inductance in the power modules is based on introducing an evaluation index. For simplification the current loops on the substrate are considered as homogenous conductors with identical thickness which is much smaller compared to the length of traces. In the power module, the main commutation paths are open loops starts with a bus and ends in another bus. However, using the pricinciples of the partial inductances, the stray inductance in the traces is formulated by adding a closing path to the open loop [6]. The self-inductance of a single-turn rectangular current loop is calculated by

$$L = \frac{\mu_0}{\pi}\left[-2(w+h) + 2\sqrt{h^2+w^2} + h\ln\left(\frac{w}{h+\sqrt{h^2+w^2}}\right) + w\ln\left(\frac{h}{w+\sqrt{h^2+w^2}}\right) + h\ln\left(\frac{h}{d}\right) + w\ln\left(\frac{w}{d}\right)\right]\times 10^{-3} \tag{6.4}$$

where w and h are the width and height of the current loop, d is the diameter of the loop cross section ($d<<w,h$), μ_0 is the vacuum permeability, and L is the loop inductance.

The partial self-inductance of a single straight conductor is given by [7]

$$L = \frac{\mu_0 l}{2\pi}\left(\ln\frac{2l}{d} - 1\right)\times 10^{-3} \tag{6.5}$$

where l is the length of the conductor, and d is the diameter of the conductor cross section ($d<<l$), and μ_0 is the vacuum permeability. From (6.4), and assuming $d<<w,h$, the self-inductance of a rectangular loop is approximated by

$$\begin{aligned} L &\approx \frac{\mu_0}{\pi}(w+h)\cdot\ln(w\cdot h)\times 10^{-3} \\ &= \frac{\mu_0}{2\pi}\cdot C\cdot\ln(S)\cdot 10^{-3} \end{aligned} \tag{6.6}$$

where $C=2\cdot(w+h)$ is the perimeter of the loop, and $S=w\cdot h$ is the area of the loop. So the self-inductance of the rectangular loop is linearly proportional to $C\cdot ln(S)$. As derived from (6.4), and assuming $d<<l$, the self-inductance of a single straight trace is approximated by

$$L \approx \frac{\mu_0}{2\pi}\cdot l\cdot\left[\ln(2l) - 1\right]\cdot 10^{-3} \tag{6.7}$$

In order to simplify the inductance model for calculation of the partial inductance of the loop, the shortest path between two ends of the loop is chosen [8]. In this model, the mutual inductance between traces is neglected and only the partial self-inductance is taken into account. Consequently, by subtracting the partial self-impedance from the inductance of the closed loop, the inductance of the open loop between two ends is achieved. So, using (6.6) and (6.7), an index is derived to evaluate the inductance of the commutation loop

$$\alpha = C\cdot\ln(S) - l\cdot\left[\ln(2l) - 1\right] \tag{6.8}$$

In a loop, a large value of the index α illustrates a large stray inductance. So, in the power module layout design, the purpose is to minimize α. However, due to the

adopted approximations, the index α cannot be used for an accurate stray inductance estimation and it is only used as a scale for comparison between the stray inductances of different layout designs.

6.3 Reduced parasitics design example

This section investigates the optimization of a SiC power module by reducing the electrical parasitics using the micro-strip structure and an optimization tool developed at the Mixed Signal Computer Aided Design (MSCAD) Laboratory in the University of Arkansas. The optimization tool implements the Non-Dominated Sorting Genetic Algorithm II (NSGA II) for multi-objective optimization of the power module layout. The case study is a half-bridge inverter module with separate anti-parallel diodes. The addition of anti-parallel diodes outside of the MOSFET chips makes it possible to reduce stray inductance in the package using a technique called P-cell N-cell layout [9]. Conventionally, the anti-parallel diodes are either packaged within the MOSFETS or placed closely in parallel with them as shown in Fig. 6.3(a). The P-cell N-cell layout technique reduces the stray inductance of the main current commutation pathways in a module which cause voltage overshoot and current ringing during switch turn-off and turn-on respectively. This is done by pairing the upper anti-parallel diodes with the lower MOSFETS and vice-versa, as shown in Fig. 6.3(b). The closer these devices are paired together, the lower the parasitic inductance between the devices. This lower inductance reduces the inductive voltage spikes seen across a MOSFET while undergoing a turn-off event and current overshoot during turn-on [9].

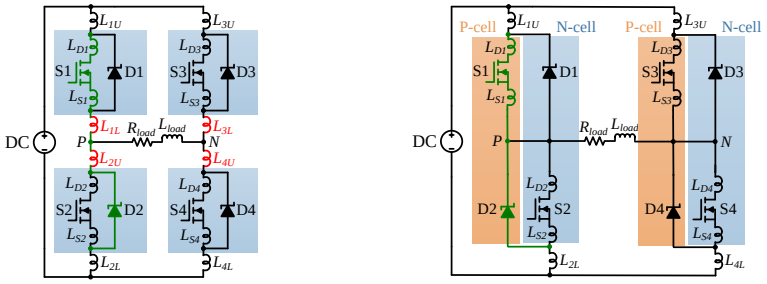


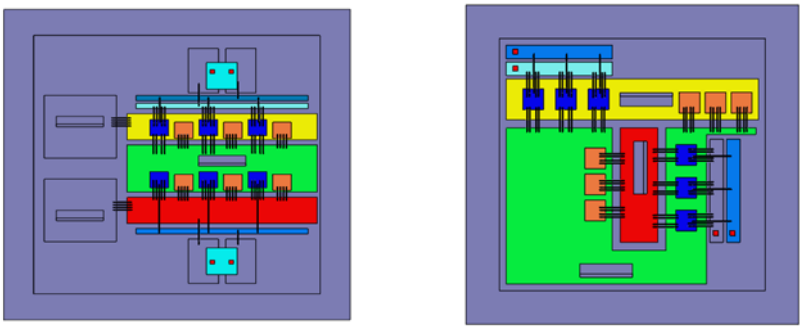
Fig. 6.3. Schematic of full-bridge inverter with parasitic inductance: conventional layout (a), P-cell N-cell paring layout (b).

The optimization objectives for this particular example include the minimization of 3 main parameters: the loop inductance in the path from the positive to negative terminal, gate to source loop inductance of upper and lower switching positions. By minimizing the total loop inductance in the layout from the positive to negative terminals, the inductance of both current commutation paths are simultaneously minimized. This reduces the number of performance measures by one, instead of measuring both paths. Two separate performance measures are created for the gate to source loop inductances. The minimization of the gate loop inductances helps reduce ringing, but they have been shown to be not as important in terms of ringing and switching loss energy as the main loop inductance [10].

There are a total of 6 MOSFETs and 6 anti-parallel diodes included in the design of this module, where 3 MOSFETs are used in each of the upper and lower switching positions. This module is a half-bridge, so only a single inverter phase-leg is implemented. The MOSFETs used in the design are CREE CPMF-1200-S160B and the diodes are CREE CPW4-1200S020B. The module is assumed to be operating at a switching frequency of 50 kHz. The baseplate and substrate dimensions are constrained to a fixed size. The positioning of the devices and trace sizing are allowed to be modified during the optimization process.

6.3.1 **Simulation verification**

Fig. 6.4(a) and Fig. 6.4(b) show the conventional layout which does not consider P-cell N-cell pairing of diodes and MOSFETS. The second is the P-cell N-cell based design. The conventional layout also resides on a larger substrate and baseplate than the P-cell N-cell. Two layouts were modelled in ANSYS Q3D Extractor® for parasitics analysis. Table 6.1 summarizes the results. The P-cell N-cell layout configuration significantly reduces the loop inductance over the conventional layout style.



(a) (b)

Fig. 6.4. Power module layouts: conventional layout (a), P-cell N-cell paring layout (b).

Table 6.1. Layout Performance Results.

Layout Name	Loop Ind. (nH)	Lower Gate Loop Ind. (nH)	Upper Gate Loop Ind. (nH)
Conventional	10.5	9.37	8.08
P-cell N-cell	7.9	5.41	5.62

6.3.2 **Experimental verification**

Moreover to verify the results of parasitic extraction, both power module layouts are fabricated and measured in the laboratory. Fig. 6.5 represents the fabricated P-cell N-cell power module. The loop inductances can be measured trace by trace, but the inductances are too small to have an accurate measurement. In addition, it does not take into account the mutual inductance between traces. In the simulations by the model in ANSYS Q3D Extractor®, the semiconductor chips are set to copper traces to get a conductive switching loop. This has the same effect as the chips being set to conduct and the wires bonded directly to the traces. Therefore, in the measurement, power modules without chips can be fabricated, in which the wires are directly bonded directly to the trace.

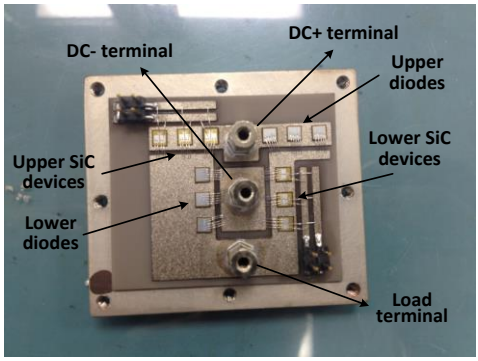
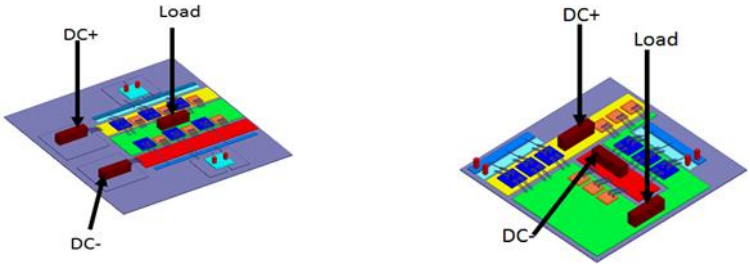


Fig. 6.5. Fabricated P-cell N-cell layout.

Another important issue is the measuring equipment. The principle of measuring stray inductances is to apply a current to the device under the test and measure the voltage (to find impedance). Since the inductance value is too small, high frequency is essential to get a measureable voltage. An Agilent 4294A Precision Impedance Analyzer is used with frequency range of 40 Hz to 110 MHz. Moreover, it is important to use a correct probe fixture in this measurement. The wires in the alligator probes introduce large parsitics that are comparable (and even larger) with the stray inductances in the power module. Therefore, a pin probe is used because the probe fixture is fixed and the parasitics are small and can be compensated through the calibration process. Stray inductances are measured for different switching loops: DC+ to DC-, Load to DC-, and Load to DC+. Two layouts and related terminals are shown in Fig. 6.6.

Fig. 6.7 shows the measurement results of stray inductance for different switching loops in the conventional layout and P-cell N-cell layout. To define the results, the testing frequency is set 10 MHz, in which the impedance of the power module is inductive. The stray inductances of different switching loops are stated in the figures and also listed in Table 6.2 for comparison. As was proven by simulations, P-cell N-cell layout presents lower stray inductances in all switching loops comparing to the conventional layout (the DC+ to DC- parasitic reduced by 43%, the DC- to load parasitic reduced by 37%, and the DC- to load parasitic reduced by 21%).



(a) (b)

Fig. 6.6. Power module layouts load and DC terminals: conventional layout (a), P-cell N-cell paring layout (b).

6.4 Conclusions

In this chapter, electrical parasitic extraction models for power modules have been explained by means of techniques used in micro-strip transmission lines and partial inductances. The inductance model based on the micro-strip structure is geometry/material dependent and it can estimate the loop inductance with about 10% error compared to FEM analysis. However, the method based on the partial inductances gives a simplified evaluation index to be used as a scale for inductance in different power module layout designs. Using the parasitic extraction method based on the micro-strip structure, a reduced parasitic layout for a conventional SiC power module has been proposed based on the P-cell and N-cell concept. The proposed layout reduces the parasitic inductances by reducing the commutation loops using a multi-objective power module design tool. A prototype of the optimized power module has been fabricated and the parasitic inductance estimated by the presented parasitic extraction model has been verified by ANSYS Q3D Extractor® and measurements. The parasitic extraction algorithm can be used as a part of the tool to design reliable power modules with least parasitic parameters.

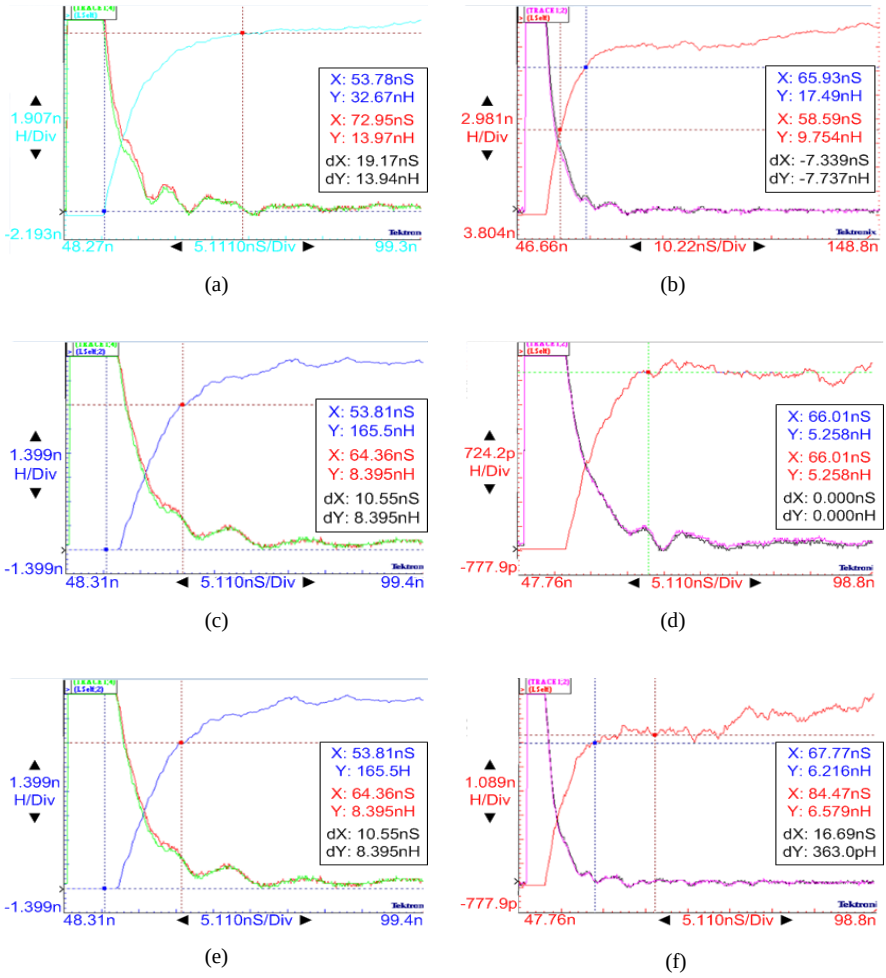


Fig. 6.7. Measured results of stray inductances: The DC+ to DC- parasitic of the conventional module (a), The DC+ to DC- parasitic of the P-Cell and N-Cell module (b), The load to DC- parasitic of the conventional module (c), The load to DC- parasitic of the P-Cell and N-Cell module (d), The load to DC- parasitic of the conventional module (e), The load to DC+ parasitic of the P-Cell and N-Cell module (f).

Table 6.2. Parasitic comparison between the conventional module and P-Cell/N-Cell based modules.

Layout Name	**Loop Ind. (nH)**	**Lower Gate Loop Ind. (nH)**	**Upper Gate Loop Ind. (nH)**
Conventional	13.9	8.3	8.3
P-cell N-cell	9.7	5.2	6.5

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Chapter 7

Conclusions and future works

7.1 Conclusions

In the present thesis work, many issues have been discussed in terms of optimization of power modules in real operations, moving from thermal aspects to electromagnetic ones. It is concluded that, the design for reliability is an improvement approach for the existing devices and development of emerging devices. As most of state of the art design approaches are based on handbooks or application test data, the failure mechanism of devices are neglected. Therefore, simplified thermal and electrical models, which consider physical characteristics of the devices, are included in the models. These models are able to estimate the thermal and electrical behavior of devices in normal and abnormal operations in a time-efficient way. On the other hand, design parameters in the power electronic devices are a series of trade-offs, which should be known and taken into account for an optimized design. A summary of the outcomes in the thesis are detailed in the following:

Topologies for power electronic circuits

One approach in improvements of power electronic circuits is to increase the efficiency by reducing the number of semiconductor devices. In high power drive applications, multi-level inverters are widely used, which are composed of several semiconductor devices. Therefore, the efficiency of the system is highly dependent on the number of switches. In the current thesis work, hybrid asymmetric multi-level topology has been used to take the advantages of appropriate semiconductor devices as well as switching patterns to reduce the number of switches and to increase the total efficiency of the converter. On the other hand, nine-switch converter has been investigated to replace the back-to-back twelve-switch converter for different energy conversion systems. Due to less number of switches, appropriate operating conditions have to be identified, when using nine-switch converter. In this thesis work, using instantaneous switch currents, the appropriate switching conditions have been

identified for different energy conversion systems. Finally, using generic power loss models, the efficiency of the converters have been identified and compared in the nine-switch and twelve-switch topologies.

FEM thermal modelling of power modules

Due to the growing application of high power modules, industries demand for higher power densities and more integrated devices. Therefore, the thermal analysis of power modules in normal operating conditions as well as abnormal operations is needed. FEM softwares are advanced tools, which can be used to estimate temperatures in critical locations of the power modules, where typically most failures occur. It has been found that by using FEM tool, thermal coupling effects between the heat paths inside the power module can be identified. The thermal coupling effect is a phenomenon, which is neglected in most manufacturer datasheets – and hence may lead to wrong calculation of the junction temperature. It is concluded that, FEM simulations can help in reliability-oriented design of power electronic circuits in static or short-term dynamic operations.

Lumped thermal models for power modules

Although FEM tools are advantageous in accurate thermal characterization of the power modules, they are impractical in case of investigating long-term dynamics – e.g. a year operation of a wind turbine. So, a 3D thermal network has been proposed which contribute to the physical characteristics of the device and can be used in circuit simulators with much higher simulation speed. In this thermal network, thermal coupling effects as well as critical temperature locations in the power module have been taken into account. Besides, a generic thermal model has been proposed to translate the boundary conditions from FEM into flexible thermal RC networks in the circuit simulator. It has been observed that boundary conditions – power losses and cooling system – influence the accuracy of thermal network. So, the thermal RC elements are adjusted automatically in the 3D thermal network for different boundary conditions. The 3D thermal network performs satisfactory for different load profiles and boundary conditions compared to FEM simulation and also experimental results.

The 3D thermal network can be used as a fast and accurate tool in different converter topologies for fast life-time estimation with respect to critical locations of the power module.

Cooling system design for high power modules

Apart from temperature estimation in the power modules, cooling system is a key factor, which influences the thermal behavior of the power modules. Direct liquid cooling system is a solution, which increases the efficiency of thermal management with uniform temperature distribution on the cooling surface. However, optimization of the cooling system demands a trade-off between thermal resistance from junction to cooler and pressure drop in the coolant. Therefore, an optimization design tool has been established in order to identify optimized geometries of the cooling system. The optimization tool has been verified by CFD simulations for some geometric parameters.

Electrical parasitics modelling of power modules

Electrical parasitics – including stray inductances, resistances and capacitances – exist everywhere inside the power modules e.g. copper traces and bond wires. As power modules are designed to switch faster and faster, electrical parasitics become more critical. Under large switching currents, the parasitic inductance and capacitance impose voltage spikes across the devices that may lead to failure of the device. Therefore, accurate modelling of electrical parasitics is critical in a reliable layout design of power module. FEM tool is a solution to calculate electrical parasitics, but it is unable to give mathematical models to be applied for parasitic reduction of the device. Two methods based on micro-strip transmission line and partial inductances have been applied to estimate electrical parasitics mathematically. Although the results show inaccuracies in some cases, they show acceptable performance in the case of comparison between different design layouts. The model can be used in the optimization process, when both thermal and electrical behavior of the device should be taken into account. Using the presented parasitic models, an optimized SiC power module layout based on the P-cell N-cell concept has been fabricated. The proposed

layout show better performance in the reduction of stray inductances in the current paths of the power module.

In general, in this thesis, it has been tried to propose simplified models as wells as key methods, in a design for reliability approach, to increase the life-time of the power electronic circuits – specially power modules – and reduce the failure rates/fatigues in the power devices.

7.2 Main contributions

1. Identification of alternative converter topologies to increase efficiency

In respect to increase the efficiency of conventional multi-level inverters, hybrid asymmetric multi-level inverters have been introduced as alternative solution to conventional types. IGCT switches were applied as well as hybrid modulation techniques to increase the efficiency. Moreover, appropriate application areas were identified to apply the nine-switch converter instead of twelve-switch back-to-back converter. Generic power loss models were established based on current evaluation of the switches in ac-ac, ac-dc, dc-ac and dc-dc energy conversion systems.

2. Identification of thermal coupling effects in different layers of power module

Thermal coupling effects between different points on the chips and different layers beneath the chips have identified and characterized for the IGBT power module. Based on chip locations, thermal maps of the coupling between the chips were identified for several chip positions on the substrate. The thermal maps can be used by layout designer in the future to optimize the layout in a trade-off between temperature reduction and electrical parasitics reduction.

3. 3D thermal network

A new three dimensional lumped thermal network has been proposed to be used in circuit simulators for fast and accurate estimation of temperatures in critical temperature locations on the chip surface and solder layers. Geometries, materials, thermal coupling effects and boundary conditions effects are included in the 3D

thermal network. 3D thermal network is an efficient tool to be used in life-time estimation of power modules in real mission profiles.

4. Optimization tool for cooling system of power modules

New user friendly advanced design platform has been established in SolidWorks to parameterize the geometries of cooling system. Several geometric parameters were considered in the design tool which influences the efficiency of cooling system. The design tool can be used for optimization of the cooling system with a trade-off between the thermal resistance and pressure drop depending on the application of power module.

5. Electrical parasitics extraction model

Electrical parasitic models for the power modules have been analyzed using techniques from the micro-strip transmission lines and partial inductances. The presented models can predict electrical parasitics accurately and with high speed compared to existing FEM tools. The electrical parasitics extraction model can be used in an optimization process to come up with the geometric optimized layouts with reduced parasitics.

7.3 Research perspectives

In this thesis several aspects in the modelling of thermal and electrical behavior of power electronic circuits have been documented. However, improvement of the work can be addressed in several directions. Some research topics that could be of high interest for further investigations are listed as the following:

1. Multi-objective design tool for power modules

- Development of a software based on the introduced thermal and electrical models, to design and to optimize layouts of power modules.

- Including the life-time models as a toolbox in the software. Based on the thermal models for different layers inside the power module, more accurate life-time can be estimated by the software.

- Electro-thermal coupling simulation for online temperature estimation calculation with power electronic converter operation.

- Coupling the software to the converter-level design tool to analyze power module behavior in different mission profiles and converter topologies for life-time estimations.

2. Experimental and FEM verifications of the cooling system design tool

- Identification of optimized cooling systems using the developed design tool with respect to a predefined coolant flow rate (CFD simulations).

- Experimental validation of the cooling system design tool using 3D printing to fabricate optimized cooling systems in different applications.

3. Thermo-mechanical modelling of power modules

- Translating the 3D thermal network into mechanical stress/strain models of the power module using FEM mechanical tool.

- Identification of wear-out in the power module with long mission profiles.

- Experimental validation of thermo-mechanical models.

4. Reliability of power module in normal or harsh operations

- Analytical modelling of bond-wire damage with accurate geometric parameters and temperature distribution in the case of solder delamination.

- Accurate life-time models for power module considering short-circuit capability.

- Life-time estimation in the presence of other stressors like humidity.

- Investigation of power module packaging for high temperature applications (e.g. aircraft or automotive) with wide band-gap devices and developing new packaging techniques for reliable operation.