Reliability-Oriented Design and Optimization of Photovoltaic Microinverters

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RELIABILITY-ORIENTED DESIGN AND OPTIMIZATION OF PHOTOVOLTAIC MICROINVERTERS

BY
YANFENG SHEN

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Reliability-Oriented Design and Optimization of Photovoltaic Microinverters

Ph.D. Dissertation

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Abstract

Photovoltaic (PV) energy has become increasingly popular worldwide. As an indispensable part in PV power systems, inverters play a crucial role in reducing volume, enhancing system reliability, and lowering the levelized cost of energy (LCOE). PV inverters can be classified into central, string, and micro- inverters. Notably, the market share of microinverters in residential PV systems has been increasing due to their abilities to achieve the module-level maximum power point tracking (MPPT), and module-level monitoring and troubleshooting. Nevertheless, there are still challenges which should be properly addressed in order to improve the essential performances of PV microinverter systems.

Firstly, the power conversion efficiency of a PV microinverter is still relatively low compared with transformerless string inverters. Particularly, it is challenging for a microinverter to maintain high efficiencies over a wide PV operating range. Therefore, new topologies and control methods are required to improve the efficiency performance of microinverter such that the advantages of PV microinverter systems in energy yields can be strengthened.

Secondly, there is a trend that a PV microinverter will be integrated into a PV module, which implies that the future microinverter should be more compact and of low physical profile. In addition, it is reported that the price per unit of electricity of a PV microinverter is higher than those of string and central inverters. Hence, the volume and cost metrics of PV microinverters need to be upgraded.

Thirdly, the panel-embedded microinverter may be inevitably heated up by the PV panel, accelerating the degradation of components. Also, due to the higher number of components used in the microinverter-based PV power systems, the reliability performance may be deteriorated. Consequently, the reliability evaluation and reliability-oriented design of PV microinverters become paramount.

To tackle those issues and thus enable a compact, low-cost-of-energy and reliable PV microinverter system, this PhD project discusses the corresponding solutions.

Increasing the power conversion efficiency and reducing the power losses

can significantly enhance the energy yield and reliability of a PV microinverter. For a two-stage single-phase PV microinverter, the DC-AC stage implemented with the classic full-bridge inverter topology can achieve a high efficiency, whereas it is challenging for the front-end DC-DC stage to maintain high efficiencies over wide PV voltage and power ranges. Therefore, this PhD thesis proposes a new isolated series resonant DC-DC converter which can cope with a wide input voltage range along with a variable DC-link voltage control. The operation principle and key characteristics of the proposed converter are analyzed. A 1-MHz 250-W PV microinverter prototype has been built and tested to verify the theoretical analysis and the feasibility of the proposed converter. Additionally, a structure-reconfigurable SRC is also discussed for the grid-connected PV microinverter systems with a wide-input voltage range and different grid voltage levels, i.e., 110/120 V and 220/230/240 V.

PV microinverters are typically enclosed in a compound-filled case which prevents the erosion of critical components from humidity. Thus, the temperature cycling is reported as the most significant stressor that affects the reliability of microinverter products. Electro-thermal modeling is crucial to the junction/hotspot temperature prediction and reliability evaluation of devices and systems. In this regard, critical parameters and power loss characteristics are modeled for a series of 650-V GaN enhancement-mode high-electron-mobility transistors (eHEMTs). As another important part in high-power-density power electronic converter, printed circuit board (PCB) vias and pads are also analytically modeled concerning their thermal resistance. An optimal design trajectory and an algorithm are proposed for PCB vias and pads, respectively. Finite element method (FEM) simulations and experimental tests are further conducted to verify the built thermal models.

The three performance metrics of a PV microinver, i.e., cost, volume and reliability, all are concerned by the industry. In this regard, a cost-volume-reliability Pareto optimization method is proposed for a PV microinverter. The modeling process of power loss, thermal impedance, lifetime, cost, and volume of components are conducted. Then the cost-volume-reliability Pareto optimization method is executed, yielding a Pareto front which enables a design trade-off among the three performance metrics.

Furthermore, this PhD thesis exemplifies the procedure and function of a reliability-oriented design method. As a case study, the electro-thermal and lifetime modeling of components is carried out for an impedance-source PV microinverter product. Then, the wear-out performance of the PV microinverter product is analyzed to identify the weakest link which, as a result, is the DC-link capacitor. Accordingly, the previous DC-link capacitor is replaced with a better one, and a variable DC-link voltage control is introduced to the PV microinverter. It turns out that the adopted measures can significantly improve the system reliability.

Dansk Resumé

Solcelle (PV) energi er blevet mere og mere populær over hele verden. Som en uundværlig del af PV-systemer spiller vekselrettere en afgørende rolle i at reducere størrelse, forbedre systemets pålidelighed og sænke Levelized Cost of Energy (LCOE). PV-vekselrettere, også kaldet PV-invertere, kan klassificeres i central-, streng- og mikroinvertere. Markedsandelen af mikroinvertere i residentielle PV-systemer er især stigende på grund af deres evne til at opnå maksimal powerpoint tracking (MPPT), overvågning og fejlfinding på modulniveau. Ikke desto mindre er der stadig udfordringer, som bør adresseres for at forbedre PV-mikroinverter-systemer på en række essentielle områder.

For det første er effektiviteten af en PV-mikroinverter stadig relativt lav sammenlignet med transformerløse strengomformere. Det er især udfordrende for en mikroinverter at opretholde høj effektivitet over et bredt PV-driftsområde. Derfor er der brug for nye topologier og kontrol for at forbedre mikroinverterens effektivitet, således at PV-mikroinverter-systemers fordel med hensyn til energiudbytte kan styrkes.

For det andet er der en tendens til at en PV-mikroinverter integreres i et PV-modul, hvilket indebærer, at den fremtidige mikroinverter skal være mere kompakt og med lille fysisk profil. Derudover er det rapporteret at prisen pr. enhed produceret energi for er højere for en PV-mikroinverter end for streng- og centrale vekselrettere. Derfor skal volumen og omkostningerne for PV-mikroinvertere sænkes.

For det tredje vil den panelindlejrede mikroinverter uundgåeligt opvarmes af PV-panelet og fremskynde nedbrydningen af elektriske komponenter. På grund af det højere antal elektroniske komponenter der anvendes i de mikroinverterbaserede PV-strømsystemer kan pålideligheden forringes. På baggrund af dette bliver pålidelighedsevaluering og pålidelighedsorienteret design af PV-mikroinvertere afgørende.

For at løse disse problemer og dermed muliggøre et kompakt, billigt og pålideligt PV-mikroinvertersystem, diskuterer dette ph.d.-projekt de tilsvarende løsninger.

Forøgelse af effektiviteten og reduktion af effekttabet kan betydeligt øge energiproduktionen og pålideligheden af en PV-mikroinverter. For en to-

trins en-faset PV-mikroinverter kan DC-AC-trinet, implementeret med den klassiske fuldbro-inverter-topologi, opnå en høj effektivitet, mens det er udfordrende for DC-DC-trinet foran at opretholde høj effektivitet over bred vifte af PV spændinger og effektområder. Derfor foreslår denne ph.d.-afhandling en ny isoleret serie-resonans DC-DC-konverter, som kan klare et bredt indgangsspændingsområde sammen med en variabel DC-link spændingskontrol. Operationsprincippet og nøglekarakteristika for den foreslåede konverter analyseres. En 1-MHz 250-W PV mikroinverter prototype er blevet bygget og testet for at verificere den teoretiske analyse og gennemførligheden af den foreslåede konverter. Derudover diskuteres en strukturkonfigurérbar SRC også for de netforbundne PV-mikroinverter-systemer med et bredt indgangsspændingsområde og forskellige netniveauer, dvs. 110/120 V og 220/230/240 V.

PV mikroinvertere er typisk pakket i en beskyttende indstøbning, der forhindrer korrosion af kritiske komponenter på grund af luftfugtighed. Således rapporteres temperatursvingninger som den mest signifikante stressor, der påvirker pålideligheden af mikroinvertere. Nøjagtige elektro-termiske modeller er afgørende for at forudsige junction/hotspot temperatur og pålideligheden af enheder og systemer. I denne henseende modelleres vigtige parametre og effekttabskarakteristik for en serie af 650 V GaN-enhancement-mode høj-elektron-mobilitetstransistorer (eHEMT'er). Som en anden vigtig del i højeffektdensitets-konvertere er printkort (PCB), viaer og pads også analytisk modelleret med hensyn til deres termiske modstand. En optimal designprocedure og en algoritme foreslås for henholdsvis PCB vias og pads. Finite element method (FEM) simuleringer og eksperimentelle tests udføres for at verificere de opbyggede termiske modeller.

De tre præstationskriterier for en PV-mikroinverter, dvs. omkostning, volumen og pålidelighed, er alle vigtige for industrien. I denne henseende foreslås en Pareto-optimeringsmetode for en pris-volumen-pålidelighedsoptimering af en PV-mikroinverter. Modelleringen af effekttab, termisk impedans, levetid, omkostninger og volumen af komponenter udføres. Derefter udføres Pareto-optimeringsmetoden, som giver en pris-volumen-pålidelighed. Dette giver en Pareto-front, der muliggør en afvejning af design blandt de tre præstationskriterier.

Desuden præsenterer denne ph.d.-afhandling et eksempel for proceduren og funktionen af en pålidelighedsorienteret designmetode. Som en caseundersøgelse udføres elektro-termisk- og levetidsmodellering af komponenter for en Impedance-Source PV-mikroinverter. Derefter analyseres wear-out analyse af PV-mikroinverterproduktet for at identificere det svageste led, som vises heraf at være DC-link kondensatoren. På baggrund af dette foreslås en ny variabel DC-spændingskontrol til anvendelse på PV-mikroinverteren, og den tidligere DC-link kondensator erstattes med et nyt design. Det vises at dette kan forbedre systemets pålidelighed betydeligt.

Contents

Thesis Details

Thesis Title:	Reliability-Oriented Design and Optimization of Photovoltaic Microinverters
PhD Student:	Yanfeng Shen
Supervisors:	Prof. Frede Blaabjerg, Aalborg University
	Assoc. Prof. Huai Wang, Aalborg University

The main body of this thesis consists of the following papers:

Publications in Refereed Journals

J1. **Y. Shen**, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-MHz Series Resonant DC-DC Converter With Dual-Mode Rectifier for PV Microinverters," *IEEE Trans. Power Electron.*, 2018, Status: Under Review.

J2. **Y. Shen**, H. Wang, A. Al-Durra, Z. Qin, and F. Blaabjerg, "A Series Resonant DC-DC Converter With Wide-Input and Configurable-Output Voltages," *IEEE Trans. Ind. Appl.*, 2018, Status: Under Review.

J3. **Y. Shen**, H. Wang, and F. Blaabjerg, "Thermal Resistance Modelling and Design Optimization of PCB Vias," *Microelectron. Rel.*, vol. PP, no. 99, pp. 1-6, 2018, Accepted.

J4. **Y. Shen**, S. Song, H. Wang, and F. Blaabjerg, "Cost-Volume-Reliability Pareto Optimization of a Photovoltaic Microinverter," *IEEE Trans. Power Electron.*, 2018, Status: to be Submitted.

J5. **Y. Shen**, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out Failure Analysis of an Impedance-Source PV Microinverter Based on System-Level Electro-Thermal Modeling," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1-14, 2018, Early Access.

Publications in Refereed Conferences

C1. **Y. Shen**, H. Wang, and F. Blaabjerg, "Thermal Modeling and Sizing of PCB Copper Pads," in *Proc. ECCE 2018*, Portland, 2018, pp. 1-7.

This thesis has been submitted for assessment in partial fulfillment of the PhD degree. The thesis is based on the submitted or published scientific papers which are listed above. Parts of the papers are used directly or indirectly in the extended summary of the thesis. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University.

Preface

The work presented in this PhD thesis is a summary of the outcome from the PhD project *Reliability-Oriented Design and Optimization of Photovoltaic Microinverters*, which was carried out at the Department of Energy Technology, Aalborg University, Denmark. This PhD project is supported by China Scholarship Council, Department of Energy Technology, Aalborg University, Otto Mønsteds Fond, Tallinn University of Technology, Ubik Solutions LLC, Hitachi Metals Ltd., and Innovation Fund Denmark through the Advanced Power Electronic Technology and Tools (APETT) project. The author would like to give an acknowledgment to the above-mentioned institutions.

First of all, I would like to sincerely thank my supervisor Prof. Frede Blaabjerg for his patient guidance, continued encouragement, and valuable advice throughout this PhD project. He is such a great mentor, and he has offered plenty of helpful guidance in my PhD research. The thesis could not be finalized without his support. I would also like to deeply thank my co-supervisor Assoc. Prof. Huai Wang who has been supporting me in many aspects of my PhD research, including research planning, paper writing, and experimental testing. It is a wonderful experience to work under his supervision.

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Finally, I would like to express my gratitude to my family and my girlfriend Tik Muk for their endless love and continued support to me. You are the source of my happiness.

Yanfeng Shen
Aalborg University, August 27, 2018

Part I

Report

Chapter 1

Introduction

1.1 Background

The deployment of photovoltaic (PV) is becoming increasingly popular worldwide. The growth in solar PV capacity in 2016 was larger than any other form of generation; since 2010, the costs of new solar PV systems have decreased by 70% [1]. For instance, the past few years have witnessed the rapid growth of the cumulative PV installation capacity in the US, as shown in Fig. 1.1 [2]. Particularly, since 2015, the residential PV system has exceeded the commercial PV systems in the total installation capacity.

Typically, a PV power system consists of modules, inverters, and other balance-of-system (BOS) components (structural and electrical components, e.g., wiring, switches, mounting systems) [2]. As an indispensable part in a PV power system, the PV inverter plays a crucial role in reducing volume, enhancing system reliability and lowering the levelized cost of energy (LCOE) [3]; therefore, the performance optimization of inverters has gained more and more attention from both academia and industry. For instance, the *Little Box Challenge* launched by Google and the institute of electrical and electronics engineers (IEEE) attracted over 2000 teams from the whole world to register for the competition [4].

Generally, PV inverters can be classified into three categories: central inverters, string inverters, and microinverters. For the microinverter-based PV power systems, each module is connected to a microinverter, which allows the module-level maximum power point tracking (MPPT), improved energy yield from module mismatch reduction, and module-level monitoring and troubleshooting [2, 5–7]. Moreover, compared with the cental and string inverters, the microinverter-based power system is the safest solution as there is no high DC voltage [2]. These features make microinverters popular in residential PV power system. Consequently, the market share of microinverters

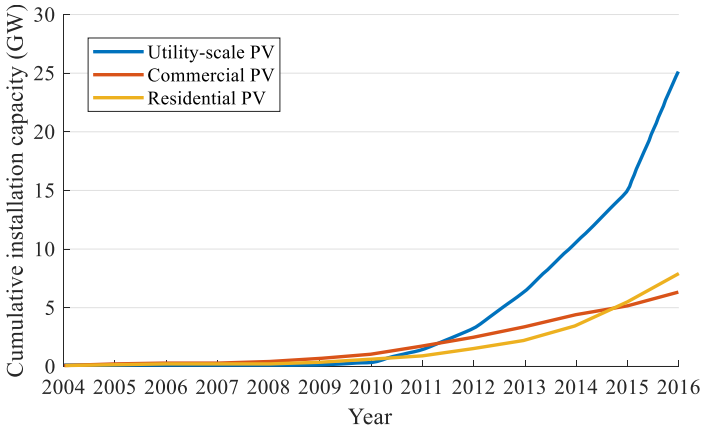

Fig. 1.1: U.S. PV market growth from 2004 to 2016 [2].

in residential systems has been increasing, e.g., from 12% in 2010 to 53% in 2016 California, US [2].

Nevertheless, there are still several issues with PV microinverters:

- PV microinverters are more expensive than string and central inverters [2, 3, 7]. According to the technical report [2], the prices of miroinverters, string inverters and central inverters in the US in 2017 were 0.4 $/Wac, 0.15 $/Wac, and 0.08 $/Wac, respectively. It is a requirement that the cost-of-energy performance of PV microinverters should be lowered.

- The power conversion efficiency of microinverters is still relatively low compared with transformerless string inverters (e.g., a peak efficiency of 99.2% is reported in [8]). Thus, the efficiency performance of microinverters needs to be improved by new topologies and/or control schemes.

- There is a trend that a PV microinverer will be integrated into a PV module [9, 10], which implies that the microinverter should be more compact in the future.

- The panel-embedded microinverter may be inevitably heated up by the PV panel, accelerating the degradation of components [11, 12]. Furthermore, due to the greater number of components used in the microinverter-based PV power systems, the reliability performance may be deteriorated [2]. On the other hand, increasing the microinverter reliability results in a longer lifetime, which helps to lower the LCOE of a PV microinverter system. Therefore, the reliability evaluation and reliability-oriented design of PV microinverters become paramount.

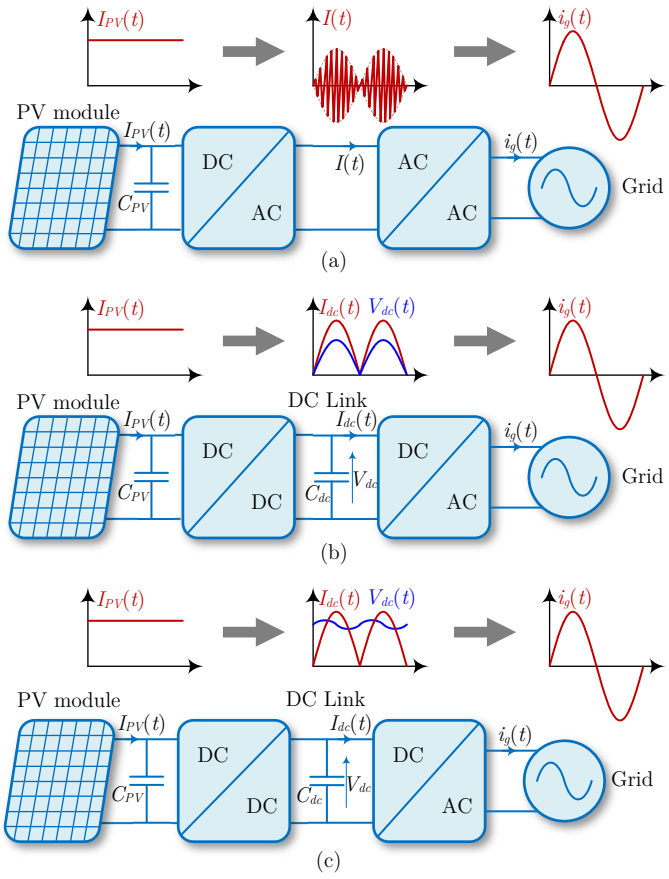

Fig. 1.2: Structures of grid-connected PV microinverter systems [6, 7, 13]: (a) HF-link (single-stage) microinverter, (b) pseudo-DC-link microinverter, (c) DC-link (two-stage) microinverter.

Motivated by the above issues, this PhD project focuses on the topology, electro-thermal modeling, reliability-oriented design, and cost-volume-reliability Pareto optimization of PV microinverters.

1.2 Architectures and Topologies of PV Microinverters

1.2.1 Architectures

In the literature, various microinverter topologies can be found. Based on the structure, these topologies can be categorized into three types [6, 7, 13], i.e.,

high-frequency (HF) link (single-stage) microinverter [14], pseudo-DC-link microinverter [15], and DC-link (two-stage) microinverter [16], as shown in Fig. 1.2.

- **HF-link microinverter** (cf. Fig. 1.2(a)): The output DC current of a PV panel is converted into an HF AC current by a DC-AC converter. Then, the connected AC-AC stage transforms this HF AC current into a low-frequency (LF) sinusoidal grid current $i_g(t)$.
- **Pseudo-DC-link microinverter** (cf. Fig. 1.2(b)): With an HF DC-DC stage, the PV current is modulated to a rectified sinusoidal current at the pseudo-DC-link where the voltage is pulsating as well. The following DC-AC stage operates as an unfolder at line frequency, and inverts the LF pseudo-DC-link current into an LF sinusoidal current $i_g(t)$.
- **DC-link microinverter** (cf. Fig. 1.2(c)): An intermediate DC-link exists between the DC-DC stage and the DC-AC stage. The DC-link voltage is regulated to a constant average value with double line frequency ripples. Both stages are operating at high frequencies.

The output power from a PV module is constant, i.e., DC power, whereas the delivered power to the grid is pulsating at double line frequency. The instantaneous power mismatch between the input and output ports must be decoupled by passive and/or active energy buffers [17].

In the HF-link and pseudo-dc-link microinverters, the energy buffer is normally placed on the low-voltage PV side. Due to the MPPT requirement, the PV voltage ripple should essentially be kept constant, leading to the need for bulky electrolytic capacitors [7, 10]. Thus, the system volume, cost, and reliability may be compromised. By contrast, the DC-link (two-stage) microinverter decouple the power mismatch at the high-voltage DC-link. A significant ripple voltage is tolerable on this capacitor because the DC-AC stage can tolerate an input voltage fluctuation and still can deliver sinusoidal power to the utility [10]. Therefore, low-capacitance high-reliability non-electrolytic capacitors may be used [10]. Moreover, the DC-link solution enables an easier performance optimization for each stage and various grid-support functionalities, e.g., Volt/VAR support [10]. Hence, this solution has been widely adopted [10, 16, 18, 19]. This research project also focuses on the DC-link solution.

Fig. 1.3 shows a typical control scheme for DC-link (two-stage) grid-connected PV microinverters. The front-end DC-DC stage is employed to achieve the MPPT of the PV panel, whereas the DC-AC inverter stage is controlled to regulate the DC-link voltage as well as to feed power to the grid.

In the literature, various single-phase inverter topologies have been proposed, e.g., basic full-bridge inverter [22], H5 inverter [23], HERIC inverter

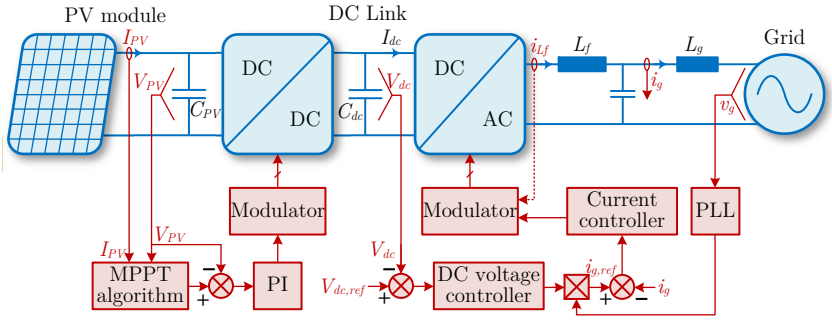

Fig. 1.3: A typical control diagram of DC-link (two-stage) grid-connected PV microinverters [20, 21].

[24], REFU inverter [25], neutral point clamped (NPC) half-bridge inverter [26], T-type half-bridge inverter [16], and other multilevel inverters [27]. Multilevel inverters have advantages of reducing electromagnetic interference (EMI) filter size with improved total harmonic distortion (THD), but also result in increased component count and control complexity [28]. By contrast, the basic full-bridge inverter has the simplest topology structure, and it is able to achieve high power density with low cost and complexity. Moreover, various modulation schemes (e.g., the unipolar modulation, bipolar modulation and hybrid modulation), and flexible control strategies can be applied to the full-bridge inverter to achieve multiple functionalities, e.g., the DC-link voltage regulation, soft-switching of switches, Volt/VAR support to grid and selected harmonics elimination. Therefore, it is the most popular topology among the Google *Little Box Challenge* teams [29]. As for the PV microinverter applications, the reported peak efficiencies of full-bridge inverters have been as high as 98.6% [30] and 98.8% [16]. Therefore, the basic full-bridge inverter topology is selected as the DC-AC stage of the PV microinverters in this PhD research.

1.2.2 DC-DC Converter Topologies for PV Microinverters

Typically, the front-end DC-DC converter is controlled to achieve the MPPT of a PV module. Depending on the module characteristics and the operating conditions, the output voltages of a PV module at the maximum power points vary over a wide range (e.g., 20-40 V). Therefore, the DC-DC converter is expected to be capable of handling a wide input voltage range while maintaining high efficiencies. It is also required that the dc-dc converter should boost the low-voltage (< 50 V [10]) PV module output to a desired high voltage (at the DC link) in order to feed a grid-connected or standalone inverter [40]. Preferably, a high-frequency transformer is inserted into the

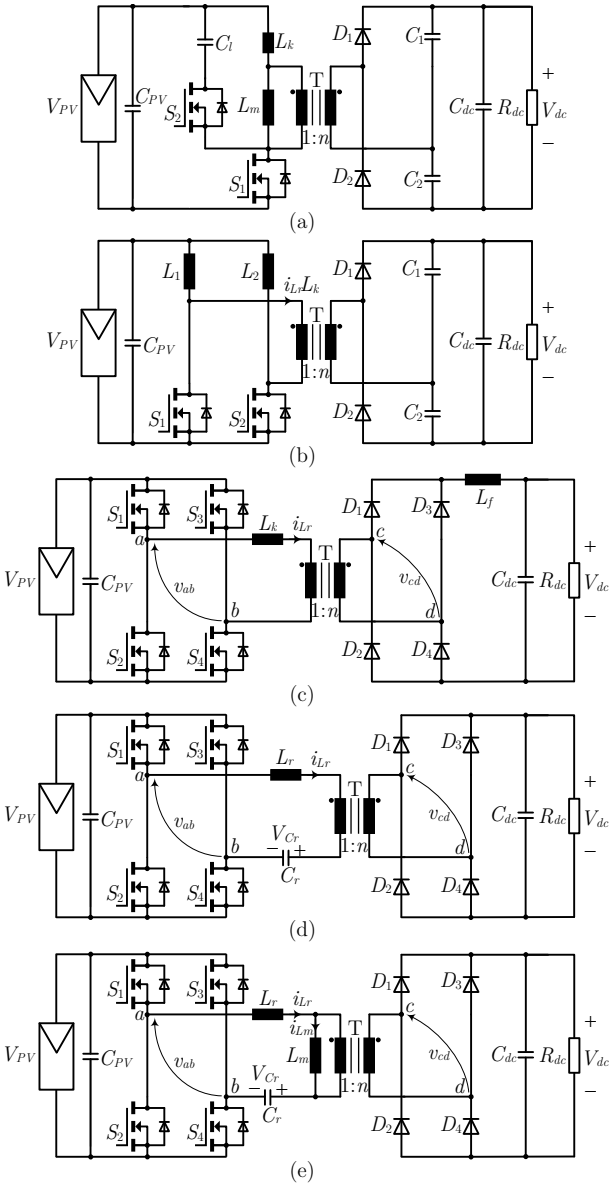

Fig. 1.4: Popular DC-DC converter topologies for two-stage PV microinverter products, evaluation boards and prototypes. (a) Active-clamped Flyback DC-DC converter employed in [31–35], (b) isolated Boost DC-DC converter used in [36], (c) phase-shift full-bridge DC-DC converter adopted in [37], (d) series resonant DC-DC converter used in [13, 38], and (e) *LLC* resonant DC-DC converter employed in [16, 39].

front-end DC-DC stage to achieve galvanic isolation, leakage current elimina-

tion, and a high voltage-boost ratio [13]. Furthermore, in order to reduce the system profile, it is necessary to increase the switching frequency and/or to adopt low-profile passive components (e.g., planar magnetics and low-profile decoupling capacitors).

In contrast to the high power conversion efficiencies achieved in the DC-AC stage, it is challenging for the isolated high-step DC-DC stage to achieve high efficiencies over wide ranges of PV voltage and power [7]. Hence, one of the goals of this PhD research is to develop isolated DC-DC converters which can maintain high efficiencies over a wide operating range. In addition, it has been stated in [7, 18] that improving the power conversion efficiency and reducing power losses can be an effective way to enhance the energy yield and reliability of PV microinverters.

Many popular isolated DC-DC converter topologies can be identified from PV microinverter products, evaluation boards/prototypes and scientific papers [13, 16, 31–39], as shown in Fig. 1.4.

- The Flyback DC-DC converter and its derivatives (e.g., interleaved Flyback converter and active-clamped Flyback converter) are the most popular topologies for PV microinverters because of their simpler structures, fewer components counts and lower costs than other topologies. However, the primary-side switches suffer from high voltage stresses, and the low-voltage low-resistance MOSFETs cannot be used [41]. Furthermore, the Flyback transformer loss is still problematic even using a nanocrystalline core material [7]. Consequently, the efficiency performance of Flyback converters is not satisfactory in PV microinverters.

- Compared with the Flyback converters, the DC-offset current of the transformer can be eliminated in the isolated Boost converter. Thus, its efficiency could be enhanced by the reduced transformer losses. However, the primary switches still operate in the hard-switching conditions, and the voltage stress of switches are high. Therefore, the switching and conduction losses of the primary switches may be problematic.

- The phase-shift full-bridge (PSFB) DC-DC converter has a better efficiency performance due to the soft-switching of switches and zero DC-offset current in the transformer. However, it is challenging for a PSFB converter to operate over a wide load range due to the issues like the hard-switching of the lagging-leg MOSFETs at light loads, large circulating current, high voltage stress over the rectifier diodes, and duty-cycle loss. [15, 42].

- A high power conversion efficiency is easier to achieve for the series resonant converter (SRC) because of the direct power transfer mechanism [40]. However, the main issue with this topology is that the light-load gain range is very narrow even within a wide frequency range [43].

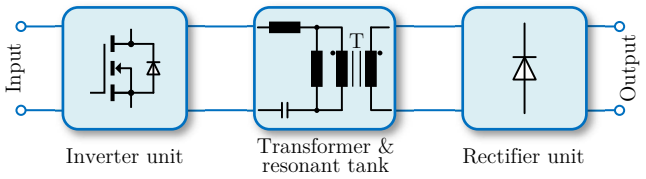

Fig. 1.5: Basic structure of *LLC* resonant converters [46] and their derivatives [40, 47–57].

As a result, this topology cannot effectively accommodate the wide PV voltage and power ranges.

- The last two decades have witnessed an increasing popularity of the *LLC* resonant converters. A high efficiency of 97.6% has been reported even at 1-MHz switching frequency [44]. Compared with the series resonant converter, the *LLC* resonant converter has a wider voltage gain range; and thus, high efficiencies can be achieved over a wider PV voltage range. Nevertheless, its voltage gain range is still not wide enough to cover the PV operating range, especially at high PV power outputs [18, 39, 45]. Therefore, hybrid control schemes (e.g., burst-mode control + variable frequency control, pulse-frequency modulation (PFM) + phase-shift pulse-width modulation (PS-PWM)) have to be applied, leading to increased implementation complexity for PV microinverters.

In order to address the issue of narrow voltage gain range, various modified *LLC* resonant converters have been proposed [40, 47–57]. Fig. 1.5 shows the basic structure of *LLC* resonant converters [46] and their derivatives [40, 47–57]. The topological modifications can be made to the primary-side inverter unit [47, 48, 50, 51, 58], the secondary-side rectifier unit [52–54] and the transformer & resonant tank [55–57].

Instead of the conventional half-bridge or full-bridge structure, a variable frequency multiplier is applied to the *LLC* resonant tank to extend the voltage gain range while maintaining high efficiencies [48]. In [58], the primary-side full-bridge inverter is replaced by a dual-bridge inverter; thus a multi-level AC voltage can be applied to the resonant tank, and a twofold voltage gain range can be achieved; however, the primary-side switches have high turn-off currents, and may suffer from high off-switching losses when operating in high step-up applications (e.g., PV microinverters). By combining a Boost converter with an *LLC* resonant converter, two current-fed LLC resonant converters are proposed in [50, 51]. Nevertheless, the primary-side switches share uneven current stresses, which may lead to high conduction losses as well as high off-switching losses.

To avoid the high off-switching losses on the high-current primary-side

switches, references [52–54] propose secondary-rectifier-modified *LLC* resonant converter topologies. Specifically, in [52] and [53], two diodes in the full-bridge rectifier are replaced with two active switches, yielding a controllable rectifier. In [54], two active switches are adopted to obtain a reconfigurable voltage multiplier rectifier, leading to a squeezed switching frequency range and improved efficiencies over a wide input voltage range; notably, the rectifier components count is high (8 diodes + 2 active switches + 6 capacitors), and thus this topology may not be cost-effective for PV microinverter applications.

Furthermore, references [55–57] modify the transformer and resonant tank to extend the voltage gain range of the *LLC* resonant converter. In [55], an auxiliary transformer, a bidirectional switch (implemented with two MOSFETs in an anti-series connection), and an extra full-bridge rectifier are added to the conventional *LLC* resonant converter. Thus, the equivalent transformer turns ratio and magnetizing inductance can be adaptively changed in order to achieve a wide voltage gain range; however, the components count is high and the transformers utilization ratio is relatively low. To address the issues [55] as well as to maintain high efficiencies over a wide input voltage range, Sun *et al* [57] propose a new *LLC* resonant converter with two split resonant branches; in this way, two operation modes, i.e., the low- and medium-gain modes, are enabled, and the gain range for mode transition is 1.5 times, leading to a smoother efficiency curve over the gain range. In reference [56], a new transformer plus rectifier structure with fractional and reconfigurable effective turns ratios is proposed for a widely varying voltage gain.

1.3 Electro-Thermal Modeling of PCBs and GaN eHEMTs

1.3.1 Thermal Modeling of PCBs

Modern power semiconductor devices are shrinking in size in order to achieve better performance in terms of parasitic inductance, power density, and power losses [59]. Good thermal management must be achieved to ensure the heat generated inside the device is effectively dissipated to the ambient. Otherwise, the high temperature may lead to reliability issues with the semiconductor, solder joint and thermal grease [60–63]. In addition, suitable heat dissipation measures should be considered as early as in the design and development phase, because subsequent modifications are generally more costly and involve increased engineering effort [64].

In medium power applications, a surface-mounted device (SMD) is typically cooled by a heatsink attached to the PCB. In this case, the PCB vias offer an efficient thermal propagation path [65, 66]. In low power scenarios, a PCB

copper pad is used for heat spreading, and thus, a SMD can be cooled by natural convection [67]. Semiconductor device manufacturers have provided many thermal design guidelines [67–71]. However, those reference design schemes are for specific cases only and are not optimized. There is even some discrepancy between the design guidelines, e.g., [69] and [70] give the opposite recommendations for the thermal via diameter. Moreover, the computational fluid dynamics (CFD) simulations are costly and time-consuming despite higher accuracy. Hence, the development of an analytical thermal model, which supports a quick design optimization of PCB vias and pads, is of significance.

References [72–74] employ either experiment or CFD simulation to obtain the thermal resistance of PCB vias. In [65, 75–78], analytical thermal models are built for PCB vias. However, the main issue is that not all parameters are analyzed or considered, and thus, the derived via design is not optimal.

For the heat transfer characteristics of a PCB pad, the heat conduction, convection and radiation all exist, which makes the thermal analysis complicated. Texas Instruments develops an online PCB thermal calculation tool based on CFD thermal resistance data of different package sizes and pad dimensions [79]. However, some important factors (e.g., PCB thickness, number of copper layers, and copper thickness) are not taken into account, and the online tool does not support design optimization. In addition to the CFD simulations, many other numerical calculation methods are developed [80, 81]. The study in [81] deals with a substrate for a ball grid array package, where a belt of densely populated vias and two continuous copper layers are placed; however, the built model is complicated and no CFD or experimental verifications are provided. For electrical engineers, it is more desired to have an analytical thermal model such that the temperature of devices with different designs and cooling methods can be fast predicted [82, 83]. In [67], an analytical thermal resistance model is developed for PCB thermal pads; however, the heat transfer boundary and the convective heat transfer coefficient variation over temperature difference are not included, and as a result, there might be a remarkable error between calculations and measurements.

1.3.2 Characterization and Electro-Thermal Modeling of GaN eHEMTs

GaN power transistors, e.g., enhancement-mode high-electron-mobility transistors (eHEMTs), feature higher power density, higher switching frequency, and lower loss than their silicon counterparts [28, 84]. Accordingly, GaN eHEMTs are becoming increasingly popular in power electronic converters. With the same voltage rating and drain-source on-state resistance, the parasitics of a GaN eHEMT, including the parasitic inductance and capacitance, are significantly smaller than silicon power switches. Thus, fast switching

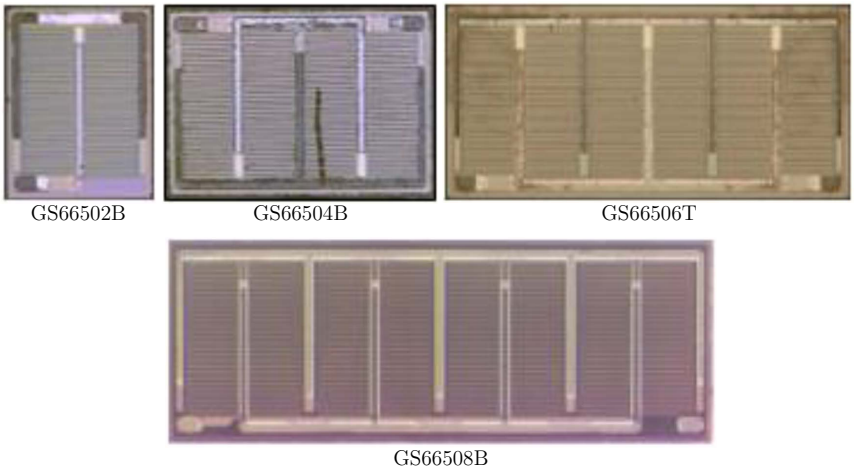

Fig. 1.6: Scanning acoustic microscopy (SAM) images of the 650-V GaN eHEMT dies of GaN Systems^{TM}; The numbers of die units inside GS66502B, GS66504B, GS66506T and GS66508B are 2, 4, 6, and 8, respectively. The total die area of GS66508P (12.3 mm^2 [85]) is almost twice of that of GS66504B (6.1 mm^2 [86]).

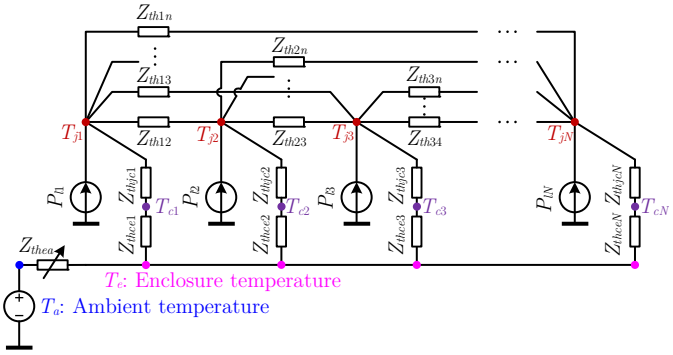

Fig. 1.7: Thermal impedance network of an enclosed converter system, including the self and mutual junction-enclosure thermal impedances. Source: **[J5]**.

and low switching loss are possible for GaN eHEMTs. When the switching frequency is pushing up to megahertz, the side effect of parasitics and the switching loss can still be pronounced. In this PhD project, the employed GaN eHEMTs can achieve the zero-voltage switching (ZVS) turn-on, and the turn-on loss can be negligible. Consequently, only the conduction loss, turn-off loss and soft-switching characteristics of GaN eHEMTs are focused on.

For a series of 650-V GaN eHEMTs from GaN Systems^{TM}, the current rating and on-state drain-source resistance of a transistor are achieved by employing different standard die units in parallel, as shown in Fig. 1.6. The

numbers of die units inside GS66502B, GS66504B, GS66506T, and GS66508B are 2, 4, 6, and 8, respectively.

Detailed information concerning the drain-source resistance, parasitic capacitance, and junction-case thermal impedance of a GaN eHEMT can be found from the datasheet. However, there is still a lack of generic analytical parameter models which can be used for the design optimization of PV microinverters.

For the thermal performance of a GaN eHEMT, it is also determined by the cooling system which may vary significantly with different designs. Most of the PV microinverter products on the market are filled up with high-thermal-conductivity compound [18] in order to improve the cooling performance and protect the converters from humidity erosion. However, the compound reinforces the thermal cross-coupling among the components inside the microinverter enclosure, as illustrated in Fig. 1.7. The heat propagation from the components to the ambient can be divided into three parts, i.e., from the junction/hotspot to the case, from the case to the enclosure, and from the enclosure to the ambient. For the first two heat transfer paths, the heat conduction dominates, whereas the third heat transfer path, i.e., from the converter enclosure to the environment, involves all the three heat transfer approaches, heat conduction, convection, and radiation. The heat transfer rate of convection is determined by the temperature difference between the enclosure surface and the environment, whereas the radiation intensity relates to the absolute temperatures [87]. The participation of convection and radiation makes the whole thermal system strongly nonlinear [18]. Particularly, it is challenging to accurately and quickly calculate the long-term (e.g., 1 year) junction/hotspot temperatures of main components for a complete PV microinverter system operating in the real field.

1.4 Reliability-Oriented Design and Multiobjective Optimization of PV Microinverters

The essential performance metrics of a PV microinverter include efficiency, energy caption, grid integration, cost, volume, reliability, etc. Most early studies and current work focus on the efficiency [7, 14, 16, 18, 32, 35, 39, 40, 43], energy caption [88, 89], grid support function [10, 19], power decoupling [17, 31, 90, 91], and LCOE of PV microinverters [2, 92–94].

Specifically, the most attention has been paid to the power conversion efficiency, which could not only reduce the cost of energy but also improve system reliability [18]. The efficiency improvement of a PV microinverter can be achieved by the innovations on converter topology [35, 40, 43], modulation scheme [14, 16], control strategy [18, 32, 39], and system design (including component selection, PCB design, cooling design, etc.) [7]. The en-

ergy caption enhancement of a PV microinverter system can be realized by adopting a shade-tolerant (global) MPPT algorithm [88] or using a differential power processing architecture [89]. To enable the grid-support functions, e.g., Volt/VAR support and harmonics mitigation, advanced controls are applied to the two-stage microinverters in [10, 19]. A growing number of works have recently focused on both the passive and active power decoupling techniques of PV microinverters to obtain higher reliability or smaller physical size [17, 31, 90, 91]. Furthermore, one of the most popular benchmarking criteria for different PV microinverter techniques is the LCOE, which is widely adopted in industry, academia, and government [2, 92, 93]. The LCOE of a PV microinverter system can be lowered by reducing the system cost and increasing the efficiency and reliability [94].

1.4.1 Reliability Evaluation and Reliability-Oriented Design

The lifetime/warranty of PV modules is about 25 years, but inverters often have to be replaced every 5 to 10 years [95], implying that the reliability of a microinverter needs improvement in order to get along with a PV module. Therefore, the reliability-oriented design of photovoltaic microinverters under a harsh environment becomes more and more important [12, 61].

A failure mode and effects analysis (FMEA) survey for PV module-level power electronics (MLPE) products [96] shows that the loose connection of dc input and ac output connectors, wear-out of dc-link electrolytic capacitors, varistor failure-short from the surge, and degradation of MOSFETs and diodes are the top four failure modes [**J5**]. Due to the compound filled inside microinverter enclosures, the erosion of critical components from humidity is prevented; thus, the temperature cycling is stated as the most significant stressor determining the reliability performance of microinverter products [96].

Recently, increasing effort has been made to the reliability of discrete power electronics components or modules (e.g., IGBT [97], MOSFET [98], and capacitor [99]) [**J5**]. In the literature, only a few works concerning the microinverter reliability can be found, and most of them use the MIL-HDBK-217 handbook [100] to determine the failure rates of microinverters [101, 102]. Unfortunately, the constant failure rates only describe the large-population statistics of random failures, and the wear-out failure is not considered [**J5**]. There are also a few works [103, 104] focusing on the system-level reliability. Moreover, the main issue with previous and current works on the reliability assessment is that the local ambient temperature and the thermal cross-coupling effect among components are not considered; thus, the wear-out performance is usually overestimated [**J5**].

On the other hand, the independent reliability testing and long-term usage data are still missing since the MLPE market is nascent [**J5**]. Neverthe-

less, *Flicker* et al [11] perform long-term accelerated tests for multiple PV microinverter products. As a result, the relative degradation performances of those PV microinverter products in the real-world operation can be predicted. However, the accelerated testing of microinverter products may be time-consuming, e.g., one year as spent in [11].

1.4.2 Multiobjective Optimization

The multiobjective optimization of power electronics enables designers to make the trade-off among multiple performance metrics. During the last decade, the efficiency plus power density Pareto optimizations of a power factor correction (PFC) rectifier, *LC* output filters, inductive power transfer coils, switched capacitor converters have been presented in [105–108], respectively. Recently, another important goal, cost, is also taken into account in the multiobjective Pareto optimization of dual active bridge (DAB) converters [109]. However, a crucial performance criterion, i.e., reliability, is still neglected in the existing multiobjective optimization literature.

On the other hand, only a few papers can be found for the multiobjective optimization of PV microinverters. In [110], a comparative study on different microinverter architectures is conducted to make a trade-off between efficiency and Volt/VAR support capability. Dong *et al* [10] presents a detailed procedure considering multiple performance metrics (e.g., efficiency, cost, and reliability) and compliances (e.g., EMC and safety compliance, and agency compliance); however, only part of the design possibilities are explored, and therefore, the design may not be Pareto optimal.

1.5 Research Questions and Objectives

1.5.1 Research Questions

The final goal of this PhD project is to develop a reliability-oriented design and optimization method for PV microinverters.

The power conversion efficiency does not only determine the energy yield of a PV microinverter, but also affects its reliability due to the power losses [18]. Thus, it is needed to propose new microinverter topologies which are able to maintain high efficiencies over wide PV voltage and power ranges. Since the temperature cycling is the primary cause of the wear-out failure of PV microinverters [96], the electro-thermal modeling of components is of necessity for fast and accurate reliability evaluation. Furthermore, cost and volume are also essential performance metrics determining the competitiveness of a PV microinverter product on the market, and therefore, it is necessary to include the two metrics in the reliability-oriented design.

Based on the above justification, the following research questions are considered:

- Is it possible to develop a new microinverter topology which enables wide ranges of voltage gain and power, while maintaining high efficiencies?
- How to quantify and optimize the thermal resistance and/or power losses of critical components in PV microinverters, e.g., PCB vias, PCB pads, and GaN eHEMTs?
- Is it possible to simultaneously take into account the four performance metrics, i.e., cost, volume, reliability, and energy yield, for the design optimization of a PV microinverter?
- How to evaluate and improve the reliability of a PV microinverter product in the design phase?

1.5.2 Research Objectives

Motivated by those research questions, this PhD project aims to achieve the following objectives:

- **High-efficiency DC-DC converter topologies suitable for PV microinverters:** as mentioned previously, increasing the power conversion efficiency and reducing the power losses can significantly enhance the energy yield and reliability of a PV microinverter. Given that the DC-AC stage implemented with the full-bridge inverter has already achieved high power conversion efficiencies, one of the goals of this PhD project is to propose new wide-voltage-gain DC-DC converters for the two-stage PV microinverters. The operation principle and essential characteristics will be analyzed. Converter prototypes will be built, and the testing results are expected to verify the advantages of the proposed converters in terms of maintaining high efficiencies over wide input-voltage and power ranges.
- **Electro-thermal modeling of components and PV microinverter systems:** accurate electro-thermal models, including the power loss model and the thermal model, are crucial for the junction/hotspot temperature prediction of a device. Notably, for the naturally cooled PV microinverters, the heat conduction, convection and radiation all are involved, which complicates the long-term temperature prediction and online design optimization. Hence, this PhD research attempts to develop analytical power loss models and thermal models for two types of components, GaN eHEMT and PCB. PCB prototypes and a double-pulse test setup will be built to validate the developed models.

- **Cost-volume-reliability Pareto optimization of a PV microinverter:** the three performance metrics, cost, volume and reliability, all are concerned by the industry. However, there is still a lack of design method which can accommodate all the three requirements. In this regard, the PhD project will propose a cost-volume-reliability Pareto optimization method for PV microinverters. A cost-volume-reliability Pareto front is expected to be generated, and thus, a trade-off design/decision can be made among the three performance metrics.
- **Reliability evaluation and improvement of a PV microinverter product:** the last objective of this PhD study is to exemplify the procedure and function of a reliability-oriented design method. As a case study, the wear-out performance of a commercial PV microinverter product will be analyzed to find out the weakest link in terms of reliability. Then, proper measures concerning design and control will be adopted to improve the reliability of the PV microinverter product.

1.6 Thesis Outline

The obtained results of this project are documented in the PhD thesis based on the collection of papers published/submitted during the PhD period. The document consists of the ***Report*** and the ***Selected Publications***, as illustrated in Fig. 1.8. The ***Report*** presents a brief summary of the research outcomes related to the PhD project, whereas the ***Selected Publications*** present the papers derived during the PhD period.

The Report begins with the introduction of this PhD project, where the background, critical issues, challenges, state-of-the-art, and research objectives are discussed. *Chapter 2* mainly focuses on a new wide-voltage-gain DC-DC converter topology for PV microinverters; specifically, the operation principle, characteristics and experimental verifications of the proposed converter are presented in brief. Then the following two chapters (i.e., *Chapters 3 and 4*) deal with the electro-thermal modeling and optimization of GaN eHEMTs and PCBs. The main focus of *Chapters 5 and 6* is on the reliability-oriented analysis and design of PV microinverters. In addition to reliability, the other two performance metrics, cost and volume, are also taken into account in *Chapter 5* for the Pareto optimization of a PV microinverter. In *Chapter 6*, the wear-out performance of a PV microinverter product is analyzed before a new design is implemented to improve the reliability of the product. Finally, Chapter 7 concludes the thesis, summarizes the main contributions of this research, and outlines the future research perspectives.

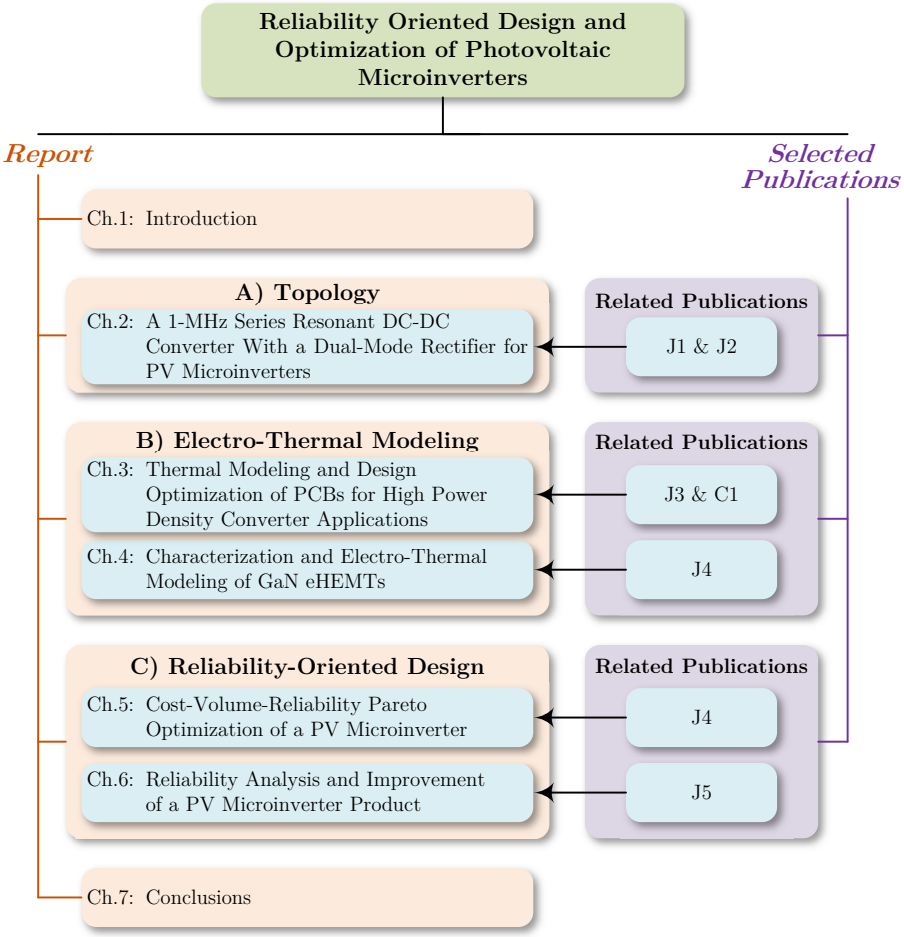

Fig. 1.8: Thesis structure and relationship between the ***Report*** and the ***Selected Publications***.

1.7 List of Publications

The research outcomes during the Ph.D. study have been disseminated in several forms of publications: journal papers, conference publications, book chapters, as listed in the following. Parts of them are used in the Ph.D. thesis as previously listed.

Publications in Refereed Journals

J1. **Y. Shen**, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-MHz Series Resonant DC-DC Converter With Dual-Mode Rectifier for PV Microinverters," *IEEE Trans. Power Electron.*, 2018, Status: Under Review.

J2. **Y. Shen**, H. Wang, A. Al-Durra, Z. Qin, and F. Blaabjerg, "A Series Resonant DC-DC Converter With Wide-Input and Configurable-Output Voltages," *IEEE Trans. Ind. Appl.*, 2018, Status: Under Review.

J3. **Y. Shen**, H. Wang, and F. Blaabjerg, "Thermal Resistance Modelling and Design Optimization of PCB Vias," *Microelectron. Rel.*, vol. PP, no. 99, pp. 1-6, 2018. Accepted.

J4. **Y. Shen**, S. Song, H. Wang, and F. Blaabjerg, "Cost-Volume-Reliability Pareto Optimization of a Photovoltaic Microinverter," *IEEE Trans. Power Electron.*, 2018, Status: to be Submitted.

J5. **Y. Shen**, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out Failure Analysis of an Impedance-Source PV Microinverter Based on System-Level Electro-Thermal Modeling," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1-14, 2018, Early Access.

- **Y. Shen**, H. Wang, A. Al-Durra, Z. Qin, and F. Blaabjerg, "A Bidirectional Resonant DC–DC Converter Suitable for Wide Voltage Gain Range," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2957-2975, Apr. 2018.
- M. Forouzesh, **Y. Shen**, Y. P. Siwakoti, K. Yari., and F. Blaabjerg, "High-Efficiency High Step-Up DC-DC Converter with Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5967-5982, Jul. 2018.
- Z. Qin, **Y. Shen**, P. C. Loh, H. Wang, and F. Blaabjerg, "A Dual Active Bridge Converter with an Extended High-Efficiency Range by DC Blocking Capacitor Voltage Control," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5949-5966, Jul. 2018.
- X. Sun, X. Wu, **Y. Shen**, X. Li, and Z. Lu, "A Current-Fed Isolated Bidirectional DC–DC Converter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6882-6895, Sep. 2017.
- X. Sun, X. Li, **Y. Shen**, B. Wang, and X. Guo, "Dual-Bridge LLC Resonant Converter With Fixed-Frequency PWM Control for Wide Input Applications," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 69-80, Jan. 2017.

Publications in Refereed Conferences

C1. **Y. Shen**, H. Wang, and F. Blaabjerg, "Thermal Modeling and Sizing of PCB Copper Pads," in *Proc. 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, 2018, pp. 1-7.

- **Y. Shen**, H. Wang, Z. Shen, F. Blaabjerg, and Z. Qin, "An Analytical Turn-on Power Loss Model for 650-V GaN eHEMTs," in *Proc. 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 913-918.
- **Y. Shen**, H. Wang, and F. Blaabjerg, "Reliability Oriented Design of a Grid-Connected Photovoltaic Microinverter," in *Proc. 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, 2017, pp. 81-86.
- **Y. Shen**, H. Wang, F. Blaabjerg, X. Sun, and X. Li, "Analytical Model for LLC Resonant Converter With Variable Duty-Cycle Control," in *Proc. 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-7.
- **Y. Shen**, H. Wang, Y. Yang, P. D. Reigosa, and F. Blaabjerg, "Mission Profile Based Sizing of IGBT Chip Area for PV Inverter Applications," in *Proc. 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Vancouver, BC, 2016, pp. 1-8.
- K. Li, **Y. Shen**, Y. Yang, Z. Qin, and F. Blaabjerg, "A transformerless single-phase symmetrical z-source HERIC inverter with reduced leakage currents for PV systems," in *Proc. 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 356-361.
- Z. Shen, H. Wang, **Y. Shen**, Z. Qin, and F. Blaabjerg, "Winding design of series AC inductor for dual active bridge converters," in *Proc. 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 565-570.

Book Chapter

- **Y. Shen**, Z. Qin, and H. Wang, "Modeling and Control of DC-DC Converters," in Control of Power Electronic Converters and Systems, 1st ed., Frede Blaabjerg, Ed.: Elsevier, 2018, ch.3.

Chapter 2

A 1-MHz Series Resonant DC-DC Converter With a Dual-Mode Rectifier for PV Microinverters

2.1 Abstract

The DC-DC stage of a two-stage PV microinverter is required to handle a wide input voltage range while maintaining high efficiencies. This chapter proposes a new isolated series resonant DC-DC converter topology suitable for PV microinverter systems. Compared with the conventional series resonant converter (SRC), a dual-mode rectifier is formed on the secondary side, which enables a twofold voltage gain range for the proposed converters with a fixed-frequency phase-shift modulation scheme. The zero-voltage switching (ZVS) turn-on and zero-current switching (ZCS) turn-off can be achieved for active switches and diodes, respectively, thereby reducing the switching losses. A variable dc-link voltage control scheme is introduced to the studied converter, yielding a remarkable efficiency improvement and input-voltage range extension. The operation principle of the proposed converter is first detailed and then the essential characteristics, i.e., the voltage gain, soft-switching, and root-mean-square (RMS) current, are analyzed. After that, the power loss modeling and design optimization of components are conducted. A 1-MHz 250-W converter prototype with 17 V – 43 V input has been built and tested to verify the theoretical analysis and the feasibility of the proposed converter. Additionally, a structure-reconfigurable SRC is also discussed for

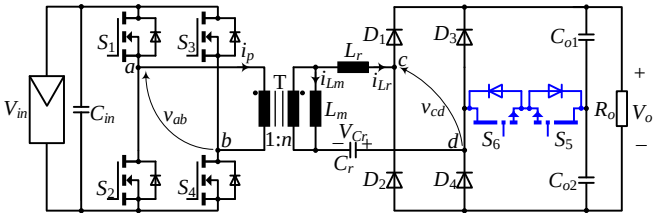

Fig. 2.1: Schematic of the proposed DMR-SRC. Source: [**J1**].

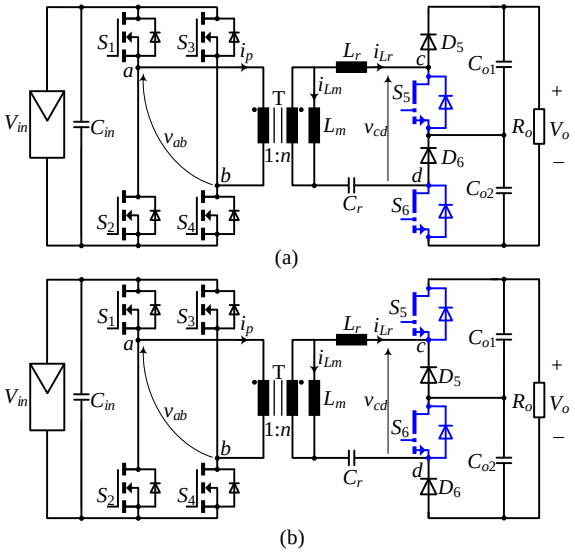

Fig. 2.2: Schematics of the extended DMR-SRC topologies for high-voltage output applications: (a) extended topology *A* and (b) extended topology *B*. Source: [**J1**].

the grid-connected PV microinverter systems with a wide-input voltage range and different grid voltage levels, i.e., 110/120 V and 220/230/240 V.

2.2 Operation Principle of the Proposed Converter

2.2.1 Topology Description

The proposed dual-mode rectifier based series resonant converter (DMR-SRC) is shown in Fig. 2.1 [J1], [111]. It is realized by adding a pair of anti-series transistors ($S_5 - S_6$) between the midpoints of the diode leg ($D_3 - D_4$) and the output capacitor leg (C_{o1} and C_{o2}) [J1], [111]. Thus, a dual-mode rectifier (DMR) can be formed by controlling the anti-series transistors $S_5 - S_6$ [J1], [111].

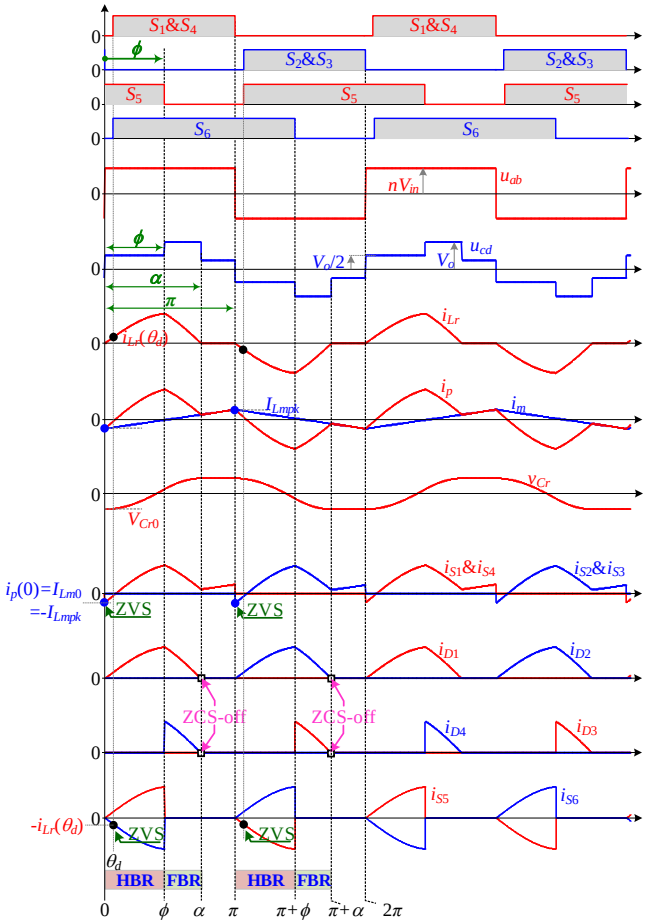

Fig. 2.3: Fixed-frequency phase-shift modulation for the proposed converter shown in Fig. 2.1 and the key operating waveforms. Source: **[J1]**.

- Half-Bridge Rectifier (HBR) mode: when the anti-series transistors $S_5 - S_6$ are triggered on, a half-bridge rectifier (voltage doubler) composed of D_1, D_2, S_5, S_6, C_{o1} and C_{o2} presents on the secondary side [J1], [111];
- Full-Bridge Rectifier (FBR) mode: when $S_5 - S_6$ are disabled, there is a full-bridge rectifier consisting of $D_1 - D_4$ on the secondary side [J1], [111].

Inspired by the dual-mode rectification concept, two extended DMR-SRCs are proposed for high-voltage output applications, as shown in Fig. 2.2. All the secondary diodes and transistors only need to withstand half of the output voltage V_o. By controlling the secondary-side active switches S_5 and S_6,

a dual-mode rectifier can be formed on the secondary side, and as a result, a wide voltage gain can be achieved. Nevertheless, only the basic topology shown in Fig. 2.1 is investigated.

2.2.2 Operation Principle

A fixed-frequency phase-shift modulation is applied to the proposed DMR-SRC, as illustrated in Fig. 2.3. The primary-side diagonal switches are driven synchronously, and the upper and lower switches of each leg are phase-shifted by π. On the secondary side, the turn-on instant of S_5 is synchronized with that of S_2 and S_3, but the turn-off of S_5 is lagged by a phase of with respect to that of S_2 and S_3. The gate signal of S_6 is shifted by a phase of with that of S_5. It is noted that the fixed-frequency phase-shift modulation scheme also holds for the two extended topologies shown in Fig. 2.2(a) and (b).

With this modulation scheme, the voltage across the midpoints of the two primary-side switch legs, i.e., v_{ab}, is an AC square wave (with an amplitude of V_{in}) which applies to the transformer. In addition, the switching frequency f_s is equal to the series resonant frequency of the resonant inductor L_r and capacitor C_r, i.e., $f_s = f_r = 1/(2\pi\sqrt{L_rC_r})$.

The primary-side transformer current i_p is the sum of the magnetizing current i_{Lm} and the resonant current i_{Lr} referred to the primary side, i.e., $i_p = n(i_{Lm} + i_{Lr})$, where n represents the transformer turns ratio.

The waveform of capacitor voltage v_{Cr} has half-wave symmetry, i.e., $v_{Cr}(t) = -v_{Cr}(t + T_s/2)$. Thus, the charge variation of the resonant capacitor over half a switching cycle [0, $T_s/2$] can be obtained as

$$\begin{aligned} q_{hs} &= [v_{Cr}(T_s/2) - v_{Cr}(0)]C_r = -2V_{Cr0}C_r \\ &= \int_0^{T_s/2} i_{Lr}(t)\mathrm{d}t = \int_0^{T_s/2} \frac{i_p(t)}{n}\mathrm{d}t - \int_0^{T_s/2} i_{Lm}(t)\mathrm{d}t \\ &= \int_0^{T_s/2} \frac{i_p(t)}{n}\mathrm{d}t = \frac{T_s}{2nV_{in}} \frac{2}{T_s} \int_0^{T_s/2} [V_{in}i_p(t)]\mathrm{d}t = \frac{P}{2nf_rV_{in}} \end{aligned} \tag{2.1}$$

where V_{Cr0} denotes the initial resonant capacitor voltage at t = 0 (see Fig. 2.3), and P is the transferred power.

The voltage gain of the converter and the inductors ratio of L_m to L_r are defined as $G = V_o/(nV_{in})$, and $m = L_m/L_r$, respectively. The quality factor is denoted as $Q = Z_r/R_o = P/(V_o^2/Z_r)$, in which the characteristic impedance $Z_r = \sqrt{L_r/C_r}$. Thus the quality factor Q is also termed as the normalized power. The initial capacitor voltage V_{Cr0} can be obtained from (2.1) as

$$V_{Cr0} = \frac{P}{4nf_rC_rV_{in}} = -\frac{\pi GQV_o}{2} \tag{2.2}$$

The magnetizing current i_{Lm} can be expressed as

$$i_{Lm}(\theta) = I_{Lm0} + \frac{nV_{in}}{m\omega_rL_r}\theta = I_{Lm0} + \frac{nV_{in}}{mZ_r}\theta \tag{2.3}$$

where $\theta = \omega_r t$ with $\omega_r = 2\pi f_r$ being the resonant angular frequency, and I_{Lm0} represents the initial magnetizing current at $\theta = 0$. The peak magnetizing current I_{Lmpk} is reached at $\theta = \pi$ i.e., $I_{Lmpk} = i_{Lm}(\pi)$. Due to the half-wave symmetry of the magnetizing current i_{Lm}, we have $I_{Lm0} = i_{Lm}(0) = -i_{Lm}(\pi) = -I_{Lmpk}$. Then, the peak and initial magnetizing currents can be obtained as

$$I_{Lmpk} = -I_{Lm0} = \frac{\pi n V_{in}}{2mZ_r} = \frac{\pi V_o}{2mZ_r G} \tag{2.4}$$

Fig. 2.3 shows the operating waveforms of the proposed converter. Neglecting the deadtime, six stages can be identified over one switching cycle [J1], [111]. Due to the symmetry of operation, only stages I-III over the first half switching cycle $[0, \pi]$ are described [J1], [111].

Stage I ($\theta \in [0, \phi]$): Before the time instant 0, S_2, S_3 and S_5 are conducting. At θ = 0, S_2 and S_3 are turned off, the negative magnetizing current I_{Lm0} begins to charge/discharge the output parasitic capacitors $C_{oss1} - C_{oss4}$, such that S_1 and S_4 can achieve the ZVS-on. During this stage, S_5 is turned on and a half-bridge rectifier is formed on the secondary side. The voltage v_{cd} is clamped by half of the output voltage $V_o/2$. The resonant inductor L_r and capacitor C_{r1} resonate, causing the resonant current i_{Lr} to increase from zero. When the parasitic output capacitor of S_6, i.e., C_{oss6}, is fully discharged, the antiparallel diode of S_6 begins to conduct. Thus, the ZVS-on of S_6 can be achieved subsequently by applying the turn-on gate signal. The governing equations of the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = (r_1/Z_r)\sin\theta = A_1 \sin\theta \\ u_{Cr1}(\theta) = -r_1\cos\theta + nV_{in} - V_o/2 \end{cases} \tag{2.5}$$

where $r_1 = nV_{in} - V_o/2 - V_{Cr0}$ and $A_1 = r_1/Z_r$.

Stage II ($\theta \in [\phi, \alpha]$): At $\theta = \phi$, S_5 is turned off, the resonant current is diverted from $S_5 - S_6$ to D_4, and a full-bridge rectifier is presented on the secondary side. Thus, the output AC voltage v_{cd} is equal to the output voltage V_o, causing the resonant current to decrease sinusoidally. The equations in this stage are expressed as

$$\begin{cases} i_{Lr}(\theta) = \frac{r_2}{Z_r}\sin(\theta-\phi) + i_{Lr}(\phi)\cos(\theta-\phi) = A_2\sin(\theta+\delta) \\ v_{Cr1}(\theta) = -r_2\cos(\theta-\phi) + i_{Lr}(\phi)Z_r\sin(\theta-\phi) + nV_{in} - V_o \end{cases} \tag{2.6}$$

where $r_2 = nV_{in} - V_o - v_{Cr}(\phi)$, $A_2 = \sqrt{(r_2/Z_r)^2 + i_{Lr}^2(\phi)}$, and $\delta = -\phi + \arccos[(r_2/Z_r)/A_2]$.

Stage III ($\theta \in [\alpha, \pi]$): When the resonant current i_{Lr} falls to zero, D_1 and D_4 turn off under ZCS. Thus, the resonant tank is prevented from resonance and the resonant current and voltage are kept at 0 and V_{Cr0}, respectively. The output capacitors are discharged to supply the load.

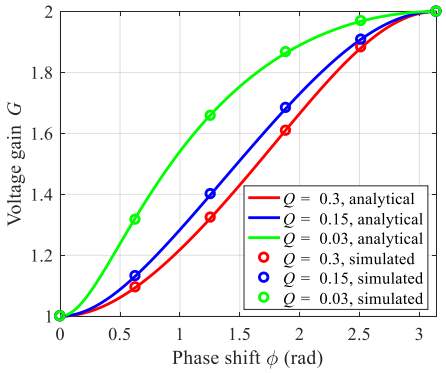

Fig. 2.4: Analytical and simulated results for the normalized voltage gain G with respect to the phase shift ϕ at different quality factors. Source: **[J1]**.

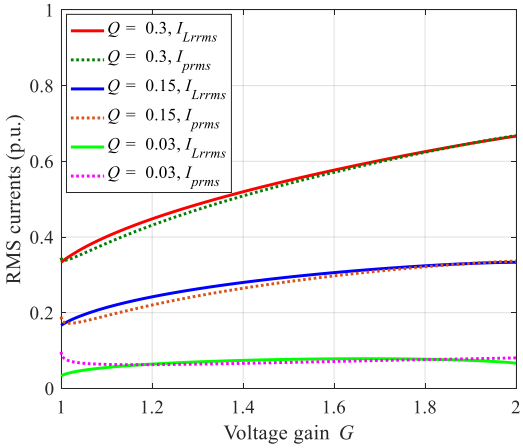

Fig. 2.5: Primary and secondary transformer RMS currents with respect to the voltage gain at $m = L_m / L_r = 6$. Source: **[J1]**.

2.3 Characteristics of the Proposed Converter

2.3.1 Voltage Gain

The voltage gain G and phase angle α can be derived as

$$\begin{cases} G = \dfrac{1}{2\pi Q(3+\cos\phi)} \times \left(K + \dfrac{4\pi Q(4\pi Q+\sin^2\phi)-\cos^3\phi+3\cos\phi-2}{2+4\pi Q-\cos\phi-\cos^2\phi} \right) \\ \alpha = \cos^{-1}\left(\dfrac{4(\sin\phi)^2(1+\cos\phi)-K[3+8\pi Q-2\cos\phi-\cos(2\phi)]}{7+24\pi Q+32\pi^2Q^2-4(1+4\pi Q)\cos\phi-(3+8\pi Q)\cos(2\phi)} \right) \end{cases} \tag{2.7}$$

where $K = \sqrt{8\pi Q(2\pi Q - \cos^2\phi - \cos\phi + 2) + (1-\cos\phi)^2}$.

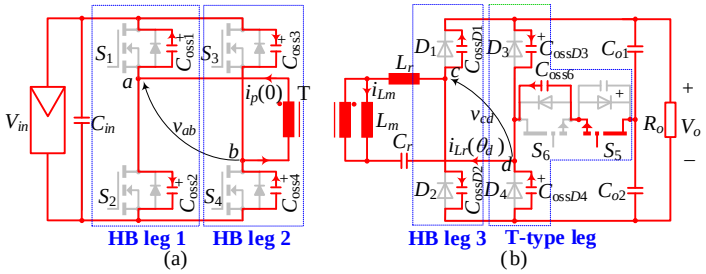

Fig. 2.6: ZVS mechanism of primary and secondary transistors (cf. Fig. 2.3): (a) ZVS turn-on of S_1 and S_4 at $t = 0$, and (b) ZVS turn-on of S_6 at $t = 0$. Source: **[J1]**.

According to (2.7), the voltage gain can be depicted in Fig. 2.4. It can be seen that the range of the normalized voltage gain is always from 1 to 2 irrespective of the quality factor (i.e., the load) [J1], [111]. It should be noted that the inductors ratio $m = L_m/L_r$ has no impact on the voltage gain [J1], [111]. Therefore, the magnetizing inductance can be designed having a large value under the condition of satisfying the ZVS conditions of the primary-side switches [J1], [111]. Circuit simulations of the proposed converter are conducted in PSIM, and the results are also presented in Fig. 6, which validates the obtained analytical gain model (2.7) [J1], [111].

2.3.2 RMS Currents

The secondary and primary transformer RMS currents can be obtained by

$$\begin{cases} I_{Lr,rms} = \sqrt{\frac{1}{\pi}\int_0^{\alpha} i_{Lr}^2(\theta)d\theta} \\ I_{p,rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} \left[i_{Lr}(\theta) + i_{Lm}(\theta)\right]^2 d\theta} \end{cases} \tag{2.8}$$

The final expressions for $I_{Lr,rms}$ and $I_{p,rms}$ are given in **[J1]**. At different quality factors, the RMS currents are shown in Fig. 2.5. It can be seen that at heavy loads, the RMS resonant current $I_{Lr,rms}$ increases with respect to the voltage gain [J1], [111]. However, at light loads, the RMS current firstly increases and then decreases [J1], [111]. For the primary transformer RMS current $I_{p,rms}$, it overall rises as the voltage gain G increases. However, at light loads, $I_{p,rms}$ becomes flat with respect to G [J1], [111]. When comparing the two RMS currents, it is seen that the difference between them is small, which is due to the allowed large inductors ratio $m = L_m/L_r$ in the proposed converter.

2.3.3 Soft-Switching

Ideally, the primary and secondary MOSFETs can achieve the ZVS turn on if $i_p(0)$ and $-i_{Lr}(\theta_d)$ are negative. This ideal ZVS condition always holds,

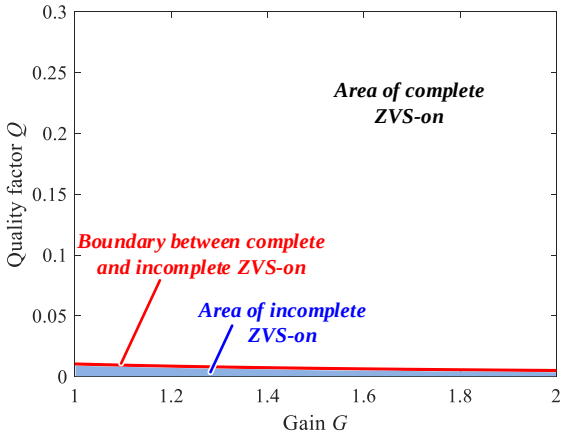

Fig. 2.7: Ranges of complete ZVS-on and incomplete ZVS-on for S_5 and S_6. The shaded area represents the range of incomplete ZVS-on, and the red solid line is the boundary between the complete and incomplete ZVS-on ranges. Source: **[J1]**.

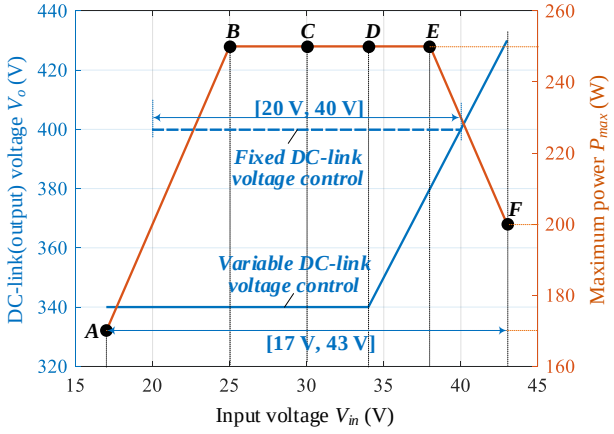

Fig. 2.8: Operation profile of the PV microinverter with fixed and variable DC-link voltage control schemes. The profile of the PV output power P_{PV} is determined by different PV panels as well as the environmental conditions (i.e., the solar irradiance and ambient temperature). Source: **[J1]**.

as analyzed before. In practice, however, there are parasitic output capacitances in parallel with MOSFETs and diodes. Therefore, a certain amount of charge is required during the deadtime interval to fully discharge the output capacitance of the MOSFET, such that its antiparallel diode will firstly conduct before the turn-on signal is applied [112]. Fig. 2.6 illustrates the ZVS mechanism of the primary and secondary transistors. Detailed ZVS analysis

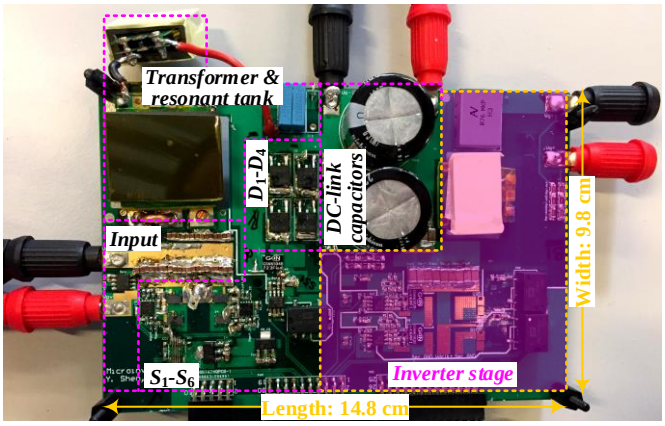

Fig. 2.9: Photo of the PV microinverter prototype. Source: [**J1**].

has been presented in [**J1**].

The practical ZVS conditions of primary-side switches $S_1 - S_4$ can be achieved by decreasing the inductors ratio $m = L_m / L_r$, i.e.,

$$m \leq \min \left\{ \frac{2nt_d V_{in}(2\pi - t_d\omega_r)}{8q_{req,P}Z_r + nV_{in}\omega_r t_d^2[G(\pi GQ - 1) + 2]} \right\} \tag{2.9}$$

where t_d is the deadtime, ω_r is the resonant angular frequency, $q_{req,P}$ is the charge required by the primary-side switches, and Z_r is the characteristic impedance. Then the primary-side switches $S_1 - S_4$ can achieve ZVS over the whole operating range of the proposed converter.

For the secondary switches S_5 and S_6, the complete ZVS-on condition is obtained as

$$A_1(1 - \cos\phi) + A_2[\cos(\delta + \phi) - \cos(\delta + \alpha)] \geq \omega_r q_{req,S} \tag{2.10}$$

where $q_{req,S}$ denotes the charge required by a secondary-side switch. If this equation is not satisfied, S_5 and S_6 will withstand an incomplete ZVS-on. Nevertheless, the drain-source voltage of S_5 and S_6 is low, i.e., $\leq V_o/2$. Therefore, the turn-on losses are not significant even operating under an incomplete ZVS-on condition. Based on (2.10), the areas of complete ZVS-on and incomplete ZVS-on for S_5 and S_6 can be obtained, as shown in Fig. 2.7. It is seen that the incomplete ZVS-on occurs only when the quality factor Q (i.e., the load) is very low.

D) Variable DC-Link Voltage Control: Depending on the PV panel properties and the environmental conditions (i.e., the solar irradiance and ambient temperature), the PV output voltage and power at the maximum power points (MPPs) may change significantly. Fig. 2.8 depicts a typical operation profile,

Table 2.1: Parameters of the built 1-MHz PV microinverter prototype. Source: [**J1**].

Parameters	Values
Input voltage V_{in}	17-43 V
Nominal input voltage V_{inN}	34 V
Output voltage V_o	340-430 V
Rated power P_N	250 W
Transformer turns ratio $N_s : N_p$	10
Resonant inductor L_r	33.4 μH
Resonant capacitor C_r	0.75 nF
Switching frequency f_s	1 MHz
Primary-side switches $S_1 - S_4$	eGaN FET, EPC 2029, $R_{ds,on} = 3.2$ mΩ
Secondary-side switches $S_5 - S_6$	GaN eHEMT, GS66504B, $R_{ds,on}$ = 100 mΩ
Rectifier diodes $D_1 - D_4$	SiC Schottky Diode, C3D02060E
DC-link capacitors C_{o1}&C_{o2}	LGJ2E181MELB15, 180 μF/250 V

i.e., the maximum power with respect to the input voltage, for PV microinverter systems. In this case, the maximum power P_{max} is 250 W when V_{in} is within [25 V, 38 V], but P_{max} declines when V_{in} is out of this range. Six operating points are identified, denoted as A, B, C, D, E, and F.

In a PV microinverter system, the dc-link voltage can be regulated either by the front-end dc-dc stage or by the dc-ac inverter stage. If the MPPT is implemented with the dc-dc stage, then the dc-link voltage will be regulated by the inverter stage, and vice versa. However, it is not necessary always to keep the DC-link voltage constant. Therefore, a variable DC-link voltage control scheme is proposed, as shown in Fig. 2.8. When the input PV voltage V_{in} is lower than 34 V, the dc-link (output) voltage will be always regulated to 340 V; however, when V_{in} is higher than 34 V, then the dc-link (output) voltage reference will rise with the increase of V_{in}. Thus, the input voltage range can be extended from [20 V, 40 V] with the conventional fixed dc-link voltage control to [17 V, 43 V] with the new control. In the meanwhile, the RMS currents under the variable dc-link voltage control are also reduced, which is beneficial to the efficiency improvement.

2.4 Experimental Verifications

A 250-W converter prototype with the dimension of 14.8 cm $\times$ 9.8 cm $\times$ 2 cm has been built up, as shown in Fig. 2.9. Two low-profile aluminum electrolytic capacitors LGJ2E181MELB15 (height: 1.5 cm) are used as C_{o1} and C_{o2}. More detailed parameters are listed in Table 2.1.

The steady-state performance at the six operating points is shown in Fig. 2.10. As can be seen, the steady-state waveforms are in close agreement with

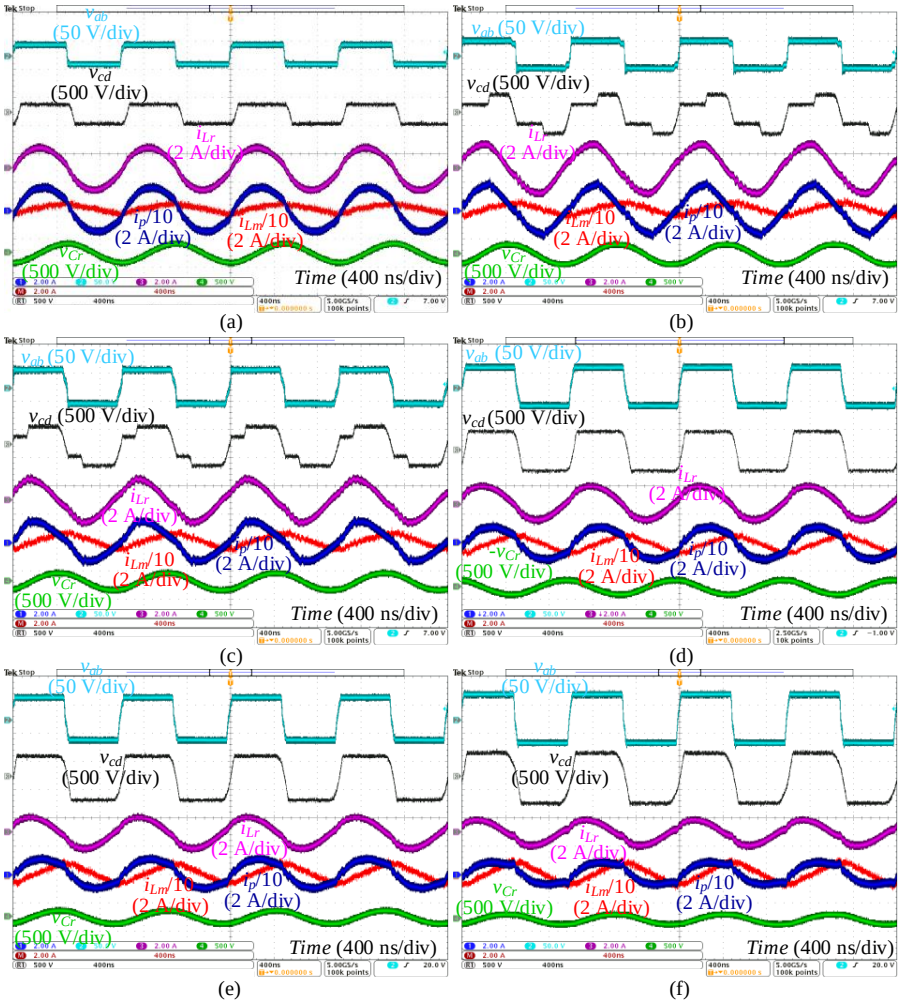

Fig. 2.10: Steady-state performance of the proposed converter under different conditions (cf. Fig. 12 and Table II): (a) operating point A: V_{in} = 17 V, V_o = 340 V, P_o = 170 W; (b) operating point B: V_{in} = 25 V, V_o = 340 V, P_o = 250 W; (c) operating point C: V_{in} = 30 V, V_o = 340 V, P_o = 250 W; (d) operating point D: V_{in} = 34 V, V_o = 340 V, P_o = 250 W; (e) operating point E: V_{in} = 38 V, V_o = 380 V, P_o = 250 W; (f) operating point F: V_{in} = 43 V, V_o = 430 V, P_o = 220 W. Source: [**J1**].

the theoretical analysis.

There are two control options for the dc-dc stage in microinverter applications, i.e., the dc-dc converter can be used either to achieve the MPPT or to regulate the dc-link voltage. Fig. 2.11 presents the dynamic experimental waveforms of the proposed converter with the output voltage closed-loop control. As can be seen, the output voltage V_o can be regulated to the ref-

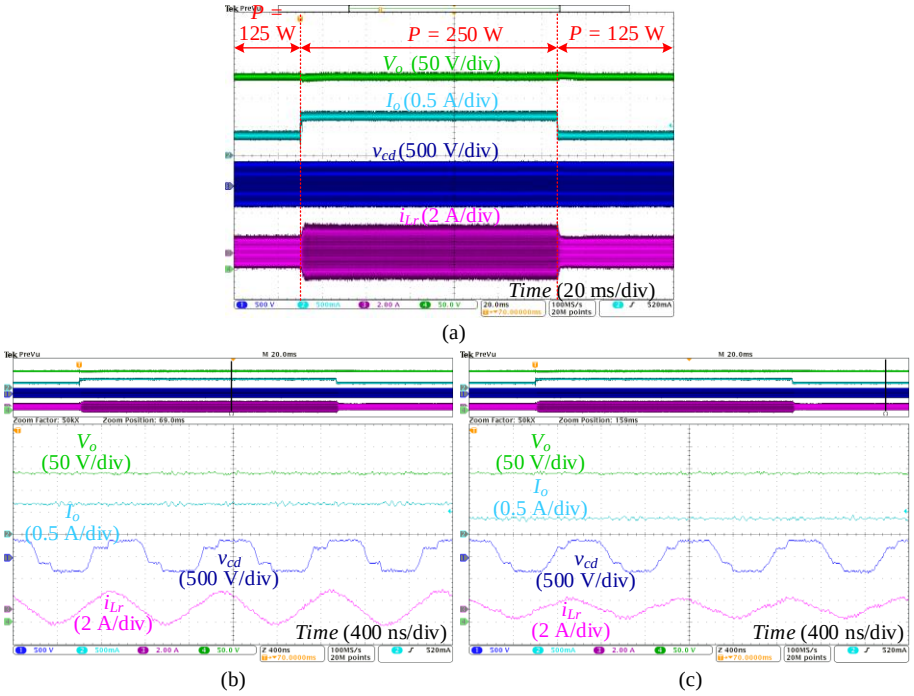

Fig. 2.11: Transient performance of the proposed converter with the output voltage closed-loop control (the input voltage V_{in} = 30 V and the output voltage reference $V_{o,ref}$ = 340 V): (a) transition between P = 250 W and P = 125 W, (b) zoomed-in waveforms at P = 250 W, (c) zoomed-in waveforms at P = 125 W. Source: **[J1]**.

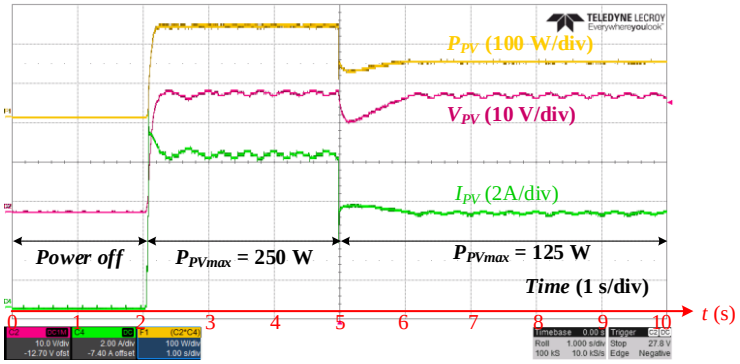

Fig. 2.12: Measured PV MPPT waveforms of the proposed converter powered by a PV simulator. At t = 2 s, the PV simulator is connected with the converter prototype, and the PV simulator operates at its maximum power point being 250 W after a short transition; at t = 5 s, the maximum power of the PV simulator steps to 125 W, and the MPPT controlled converter allows the PV simulator to track its maximum power point at 125 W. Source: **[J1]**.

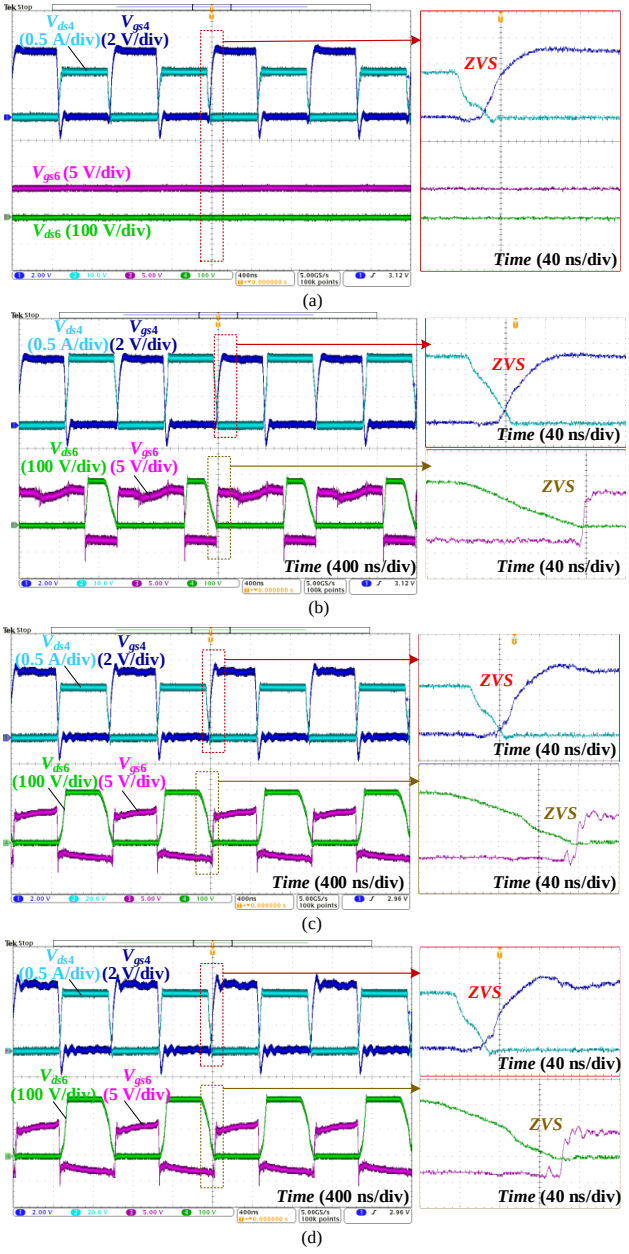

Fig. 2.13: Soft-switching waveforms of the proposed converter at different operating points: (a) operating point A: V_{in} = 17 V, V_o = 340 V, P_o = 170 W; (b) operating point B: V_{in} = 25 V, V_o = 340 V, P_o = 250 W; (c) operating point E: V_{in} = 38 V, V_o = 380 V, P_o = 250 W; (d) operating point F: V_{in} = 43 V, V_o = 430 V, P_o = 200 W. Source: **[J1]**.

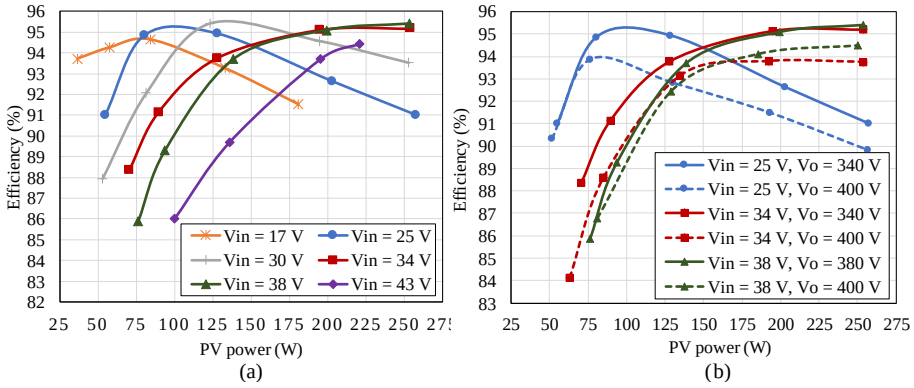

Fig. 2.14: Measured efficiencies of the converter prototype: (a) efficiency curves at different input voltages with the variable dc-link voltage control; (b) efficiency comparison between the variable and fixed dc-link voltage control schemes; solid lines represent the efficiencies with the variable dc-link voltage control and dashed lines are the results with the fixed dc-link voltage control. Source: [**J1**].

erence being 340 V after the load changes. A good dynamic performance is achieved: the transition time is less than 10 ms and the voltage overshoot and undershoot are quite small (< 5 V).

Then the MPPT control is selected for the proposed dc-dc converter, and the experimental dynamic performance is tested, as shown in Fig. 2.12. It can be seen that the proposed converter with the MPPT control enables the PV simulator to track its maximum power points under different conditions.

The soft-switching performance of the proposed converter is tested at different operating points, as shown in Fig. 2.13. Due to the symmetry of the topology and the modulation scheme, only the waveforms of S_4 and S_6 are shown. As can be seen, the drain-source voltage has fallen to zero before the corresponding gate-source voltage rises to its threshold voltage. That is, the antiparallel diode conducts before the gate signal is applied. Thus, the ZVS-on is achieved, leading to a negligible turn-on loss for the switches.

The measured efficiency curves of the proposed converter with the variable dc-link voltage control (cf. Fig. 2.8) at different input voltages are shown in Fig. 2.14(a). As can be seen, peak efficiencies over 95% are achieved for a wide input voltage range, i.e., V_{in} = 25 V, 30 V, 34 V, 38 V and 43 V. The measured full-load (250-W) efficiency increases with respect to the input voltage. This is due to the fact that the RMS currents and conduction losses reduce as the input voltage rises. When the proposed converter is controlled to have a constant dc-link (output) voltage 400 V, the efficiency is measured at different input voltages V_{in} = 25 V, 34 V, and 38 V, as shown in Fig. 2.14(b). It can be seen that the variable dc-link voltage control enables a remarkable efficiency improvement for the proposed converter. Moreover, the proposed variable

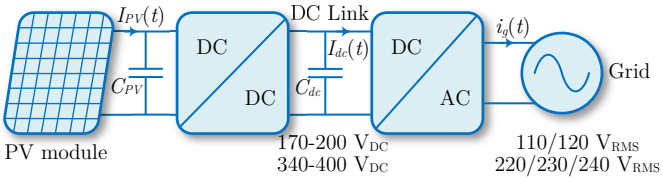

Fig. 2.15: Structures of a grid-connected PV microinverter system with two mains voltage levels 110/220 V and 220/230/240 V [6, 7, 13]. Source: **[J2]**.

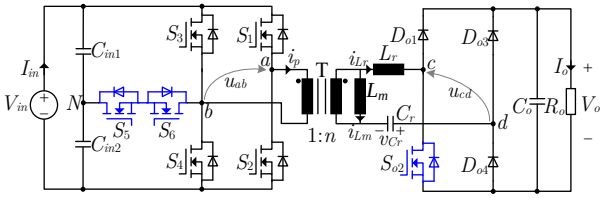

Fig. 2.16: Schematic of the proposed structure-reconfigurable series resonant dc-dc converter. Source: **[J2]**.

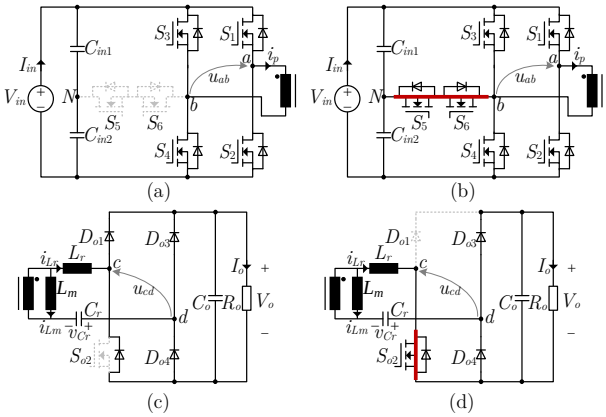

Fig. 2.17: Four structures in the proposed converter: (a) full-bridge inverter unit on the primary side; (b) symmetrical half-bridge inverter unit on the primary side; (c) full-bridge rectifier unit on the secondary side; (d) asymmetrical half-bridge rectifier (voltage doubler) unit on the secondary side. Source: **[J2]**.

dc-link voltage control allows the converter to cope with a more wide input voltage range $V_{in} \in$ [17 V, 43 V] than the conventional fixed dc-link voltage control ($V_{in} \in$[20 V, 40 V]).

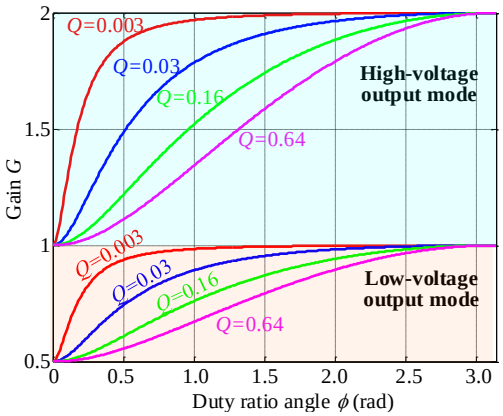

Fig. 2.18: Characteristics of the voltage gain with respect to the duty ratio angle ϕ and the quality factor Q in the low- and high-voltage output modes. Source: **[J2]**.

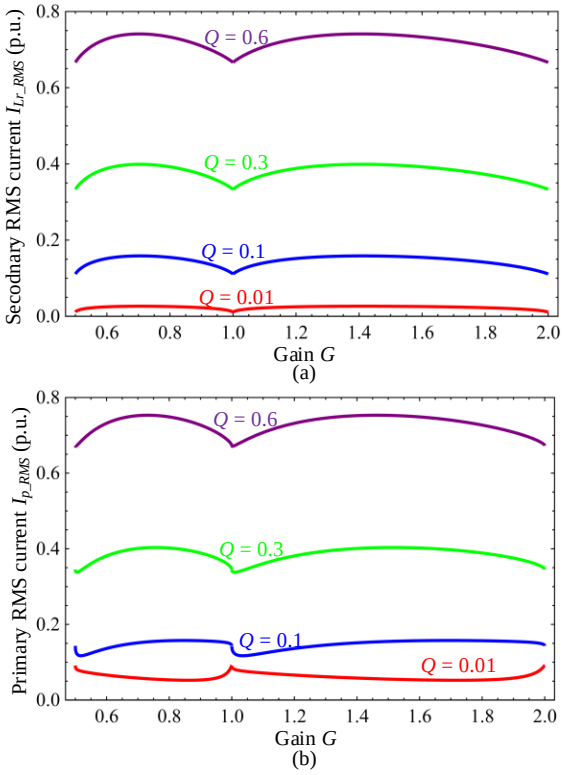

Fig. 2.19: The RMS currents with respect to the voltage gain G and the quality factor Q. (a) Secondary transformer RMS current; (b) Primary transformer RMS current. Source: **[J2]**.

2.5 Topology Extension–a Structure-Reconfigurable SRC

As aforementioned, PV modules feature a wide range of output voltage. Thus, the interfaced dc-dc converter should be capable of maintaining high efficiency over a wide input voltage range. In addition, there are two different mains voltage levels, e.g., 110 V/120 V and 220 V/ 230 V/240 V, in different countries [113]. When connecting to a 220/230/240-V grid, the inverter typically has a dc-link voltage of 340-400 V. However, for a 110/120-V grid, it is preferable that the dc-link voltage is halved, i.e., 170-200 V; this way, the reduced voltage and increased modulation index could help to minimize the switching loss and output current harmonics for the inverter [114, 115]. Hence, it is favorable if the dc-dc converter is also able to flexibly configure its output voltage, e.g., either 340-400 V or 170-200 V, as shown in Fig. 2.15.

In that regard, this chapter proposes a structure-reconfigurable series resonant converter which enables wide-input and configurable-output voltages. The topology is shown in Fig. 2.16. It consists of a dual-bridge structure on the primary side and a configurable half- or full-bridge rectifier on the secondary side, as shown in Fig. 2.17. Thus, four structure combinations can be obtained. The reconfigurability enables the proposed converter with a fixed-frequency pulse-width modulation (PWM) scheme to achieve a fourfold voltage gain range, i.e., from 0.5 to 2, as shown in Fig. 2.18. The primary-side MOSFETs and the secondary-side diode can achieve the ZVS-on and ZCS-off, respectively, leading to low switching losses [**J2**]. Moreover, the RMS currents of the proposed converter are kept low over the fourfold gain range [0.5, 2], as shown in Fig. 2.19. Therefore, the conduction losses are maintained low as well. A 500-W converter prototype has been built and tested, and the experimental results verify the feasibility of the proposed converter. Detailed analysis, design, and experimental verification are presented in [**J2**].

2.6 Summary

This chapter firstly discusses a new DMR-SRC for PV microinverters. The modulation, operation principles, and key characteristics are analyzed. A 1-MHz 250-W converter prototype is tested and the experimental results have verified the theoretical analysis. The proposed converter can cope with a wide input voltage range, e.g., from 17 V to 43 V. The active switches and diodes can achieve ZVS-on and ZCS-off, respectively. Instead of the conventional constant dc-link voltage control, a variable dc-link voltage control is applied, which enables a remarkable efficiency improvement. High power conversion efficiencies (peak efficiency = 95.5 %) can thus be achieved over a

wide input voltage range from 17 V to 43 V, as tested on the 250-W prototype. In addition, a new structure-reconfigurable SRC is also discussed. It suits well for the grid-connected photovoltaic (PV) systems with a wide-input voltage range and different grid voltage levels, i.e., 110/120 V and 220/230/240 V.

Related Publications

J1. **Y. Shen**, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-MHz Series Resonant DC-DC Converter With Dual-Mode Rectifier for PV Microinverters," *IEEE Trans. Power Electron.*, 2018, Status: Under Review.

Main Contribution:
A new dual-mode rectifier-based series resonant DC-DC converter topology is proposed in this paper. The operation principle and characteristics are analyzed before a design optimization is conducted. A 1-MHz 250-W prototype is built and tested, and the measurements verify the theoretical analysis and the feasibility of the proposed converter.

J2. **Y. Shen**, H. Wang, A. Al-Durra, Z. Qin, and F. Blaabjerg, "A Series Resonant DC-DC Converter With Wide-Input and Configurable-Output Voltages," *IEEE Trans. Ind. Appl.*, 2018, Status: Under Review.

Main Contribution:
A structure-reconfigurable series resonant DC-DC converter topology with wide-input and configurable-output voltages is proposed in this paper. The operation principle and characteristics are analyzed. A 100-kHz 500-W converter prototype is built and tested to verify the feasibility of the proposed topology.

Chapter 3

Thermal Modeling of PCB for High-Power-Density Converter Applications

3.1 Abstract

Miniature power semiconductor devices mounted on printed circuit boards (PCBs) are normally cooled by means of PCB vias, copper pads, and/or heatsinks. Various reference PCB thermal designs have been provided by semiconductor manufacturers and researchers. However, the recommendations are not optimal, and there is a discrepancy among them, which may confuse electrical designers. This chapter aims to develop analytical thermal models for PCB vias and pads, and further to obtain the optimal design for thermal resistance minimization. Firstly, the PCB via array is modeled in terms of multiple design parameters; an optimal trajectory for the via diameter is found in different cases. Then an axisymmetric thermal model is developed for PCB pads where the heat conduction, convection and radiation all exist; due to the interdependence of the conductive/radiative heat transfer coefficient and the board temperature, an algorithm is proposed to fast obtain the thermal resistance and to predict the semiconductor junction temperature. Finally, the developed thermal models are verified by computational fluid dynamics (CFD) simulations and experiments.

3.2 Thermal Modeling and Design Optimization of PCB Vias

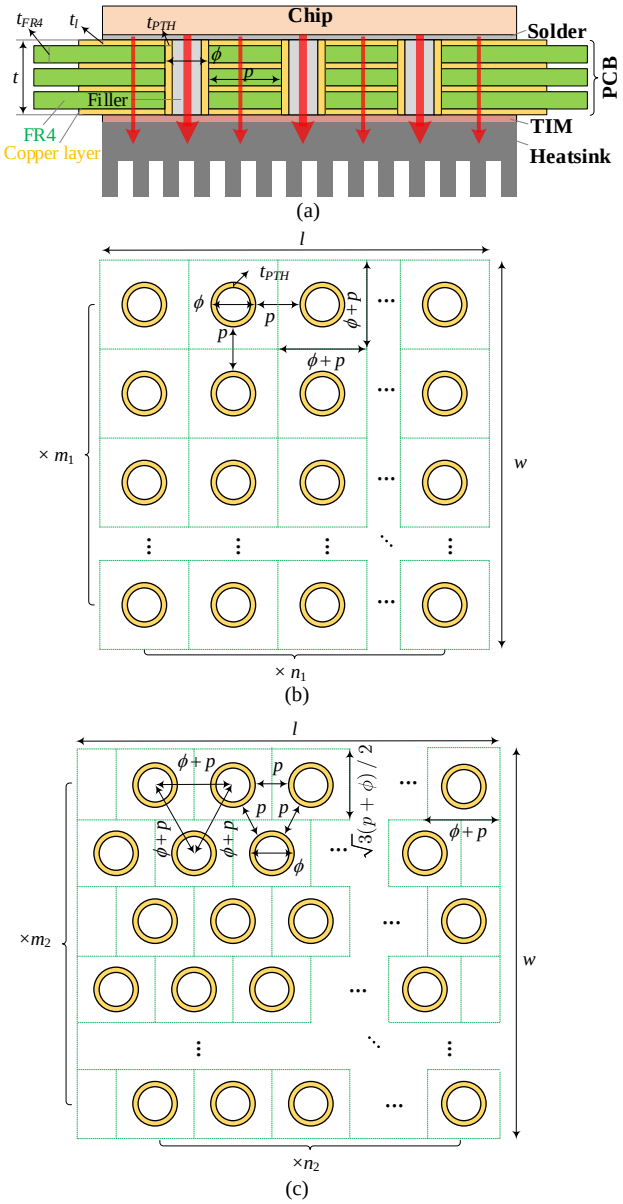

Fig. 3.1: (a) Vertical structure of a multilayer PCB with plated through holes (vias). Top view of a via array in (b) pattern I and (c) pattern II. Source: **[J3]**.

3.2.1 Thermal Modeling of PCB Vias

In medium power applications, a surfaced mounted device (SMD) is normally cooled by a heatsink, and a cluster of small vias are used to transfer

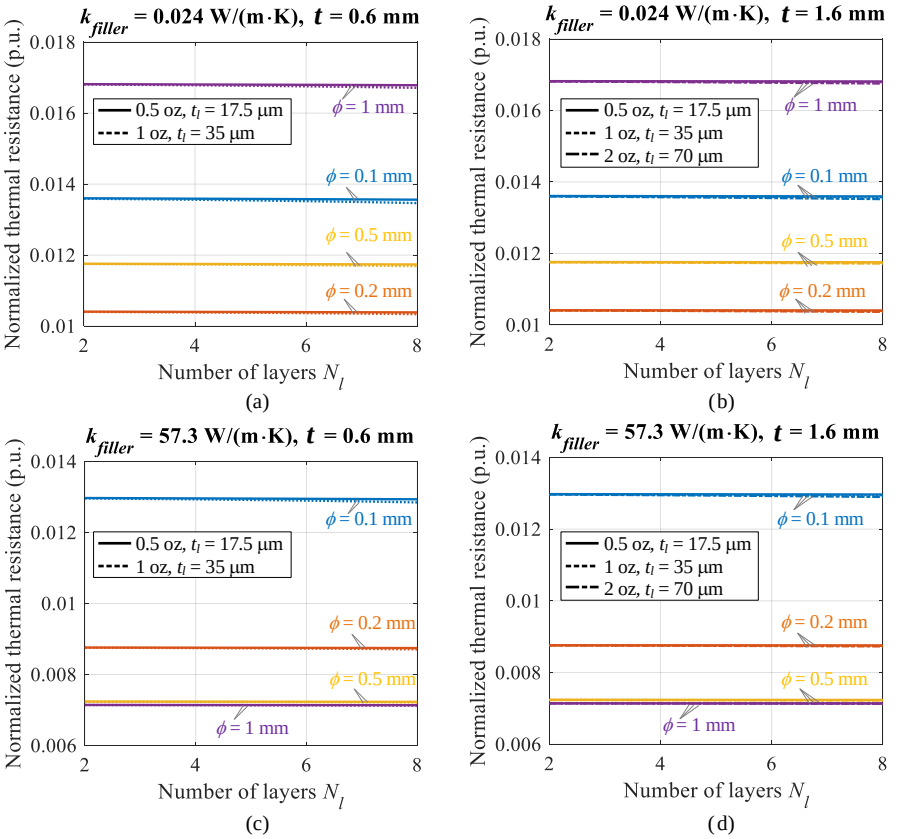

Fig. 3.2: Dependence of the normalized thermal resistance on the number of layers N_l, copper thickness t_l, and PCB thickness t with different filler materials. (a) k_{filler} = 0.024 W/(mK), t = 0.6 mm; (b) k_{filler} = 0.024 W/(mK), t = 1.6 mm; (c) k_{filler} = 57.3 W/(mK), t = 0.6 mm; (d) k_{filler} = 57.3 W/(mK), t = 1.6 mm. The thermal resistances are normalized based on $t/(k_{FR4} \cdot l \cdot w)$, as illustrated in (1). "p.u." represents "per unit", meaning the normalized thermal resistance is unitless. Source: [**J3**].

heat from the SMD to the heatsink [**J3**], as shown in Fig. 3.1(a). Two simple via patterns can be designed for a PCB pad with the dimension of l (length) $\times w$ (width) $\times t$ (height/thickness) [**J3**], as illustrated in Fig. 3.1(b) and (c). The heat flow through the copper barrels of the vias (i.e., plated through holes, PTHs) is much more significant than the heat spreading in the lateral direction, so it is assumed that heat transfers in the vertical direction only [**J3**]. Thus, the via array in patterns 1 and 2 can be divided into $m_1 \times n_1$ and $m_2 \times n_2$ cells, respectively [**J3**]. It can be seen from the horizontal cross-section of the via array that the basic via unit in pattern I is a square of $(\phi + p) \times (\phi + p)$, whereas that in pattern II is rectangular with $[\sqrt{3}(\phi + p)/2] \times (\phi + p)$ [**J3**]. That is, more vias are allowed in pattern II.

For each cell, the one-dimensional (vertical) thermal resistance can be calculated as $\Theta_{cell} = \Theta_{barrel}//\Theta_{filler}//(\Theta_{Cu}+\Theta_{FR4})$ [**J3**]. Then, the normalized thermal resistance of the via array can be obtained as

$$\Theta_{via,n} = \frac{\Theta_{via}}{t/(k_{FR4}lw)} = \begin{cases} \dfrac{4(p+\phi)^2 k_{FR4}}{\left(\underbrace{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH})}_{\text{plated copper in via}} + \underbrace{\pi k_{filler}(\phi - 2t_{PTH})^2}_{\text{via filler}} + \underbrace{\dfrac{t[4p^2+8p\phi+(4-\pi)\phi^2]}{N_{Cu}t_{Cu}/k_{Cu} + (t - N_{Cu}t_{Cu})/k_{FR4}}}_{\text{copper and FR4 layers}} \right)}, & \text{pattern I} \\ \dfrac{2\sqrt{3}(p+\phi)^2 k_{FR4}}{\left(\underbrace{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH})}_{\text{plated copper in via}} + \underbrace{\pi k_{filler}(\phi - 2t_{PTH})^2}_{\text{via filler}} + \underbrace{\dfrac{t[2\sqrt{3}(p+\phi)^2 - \pi\phi^2]}{N_{Cu}t_{Cu}/k_{Cu} + (t - N_{Cu}t_{Cu})/k_{FR4}}}_{\text{copper and FR4 layers}} \right)}, & \text{pattern II} \end{cases} \tag{3.1}$$

IPC-6012 specifies a minimum copper plating thickness of 20 μm for Class 1 PCBs, and 25 μm is a standard via plating thickness [116]. Thus, t_{PTH} = 25 μm is used in the following analysis. Based on (3.1), it is obtained that the normalized via thermal resistance rises when the via spacing p increases. Therefore, p should be designed as small as possible. However, the allowed minimum via spacing depends on the PCB manufacturers, and is generally 8 mil = 0.2 mm in practice.

The dependence of $\Theta_{via,n}$ on the number of layers N_l, copper thickness t_l (i.e., t_{Cu}), and PCB thickness t is shown in Fig. 3.1 [**J3**]. As can be seen, the parameters, N_l (the number of copper layers), t_l (the thickness of a copper layer) and t(PCB thickness), have a negligible impact on the normalized thermal resistance, which implies that the term of the copper and FR4 layers in the denominator of (3.1) have a much higher value compared to the vias (including the plated copper and via filler) [**J3**]. That is, the heat is mainly transferred through the vias. Hence, the term of the copper and FR4 layers in the denominator of (3.1) can be neglected without scarifying accuracy [**J3**], i.e.,

$$\Theta_{via,n} \approx \begin{cases} \dfrac{4(p+\phi)^2 k_{FR4}}{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH}) + \pi k_{filler}(\phi - 2t_{PTH})^2}, & \text{pattern I} \\ \dfrac{2\sqrt{3}(p+\phi)^2 k_{FR4}}{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH}) + \pi k_{filler}(\phi - 2t_{PTH})^2}, & \text{pattern II} \end{cases} \tag{3.2}$$

According to (3.2), the thermal resistance of a via array in pattern II is approximately $\sqrt{3}/2 = 87\%$ of that in pattern I.

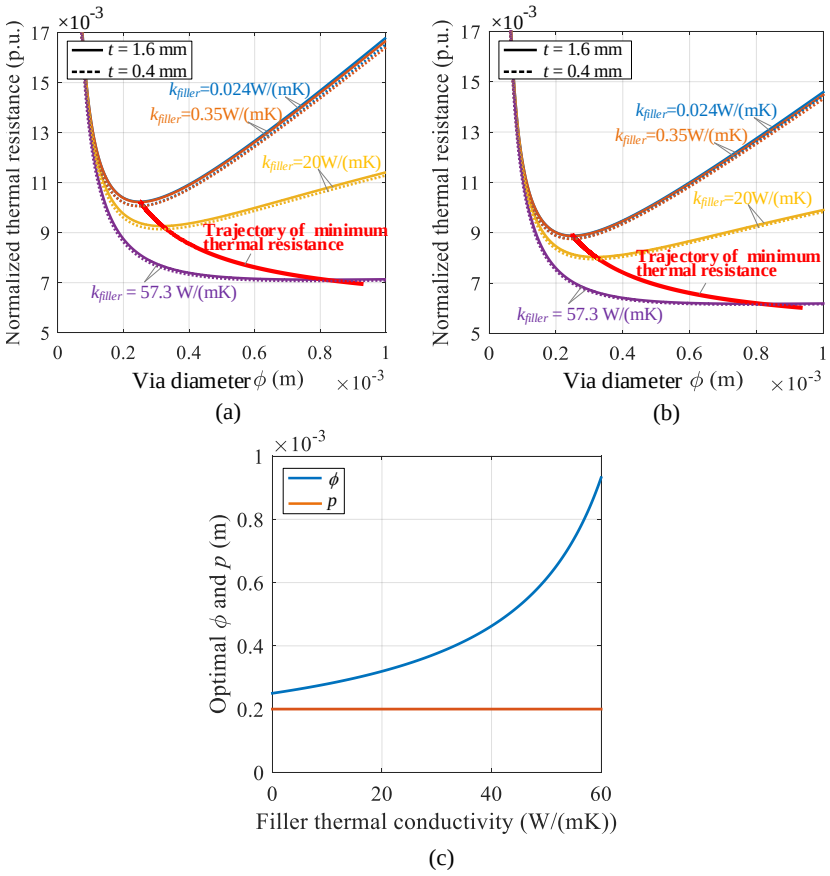

Fig. 3.3: . Dependence of the normalized thermal resistance on the diameter ϕ at different PCB thickness and filler thermal conductivities for (a) pattern I and (b) pattern II. (c) Optimal via diameter and spacing with respect to the filler thermal conductivity: the optimal parameters enable the via array to achieve the minimum thermal resistance. Source: **[J3]**.

3.2.2 Design Optimization of PCB Vias

From (3.2), we can also obtain the optimal via diameter for both patterns, which can achieve the minimum thermal resistance, i.e.,

$$\frac{\mathrm{d}\Theta_{via,n}}{\mathrm{d}\phi} = 0 \Rightarrow \phi_{opt} = \frac{2t_{PTH}(p+2t_{PTH})(k_{Cu}-k_{filler})}{2t_{PTH}(k_{Cu}-k_{filler})-k_{filler}p}, \text{patterns I\&II} \quad (3.3)$$

Fig. 3.3(a) and (b) shows the thermal resistance characteristics of a via array (in patterns I and II) with respect to the via diameter ϕ at different filler materials.

As can be seen, an optimal via diameter can be identified when the filler material is specified. The optimal via diameter contributes the minimum

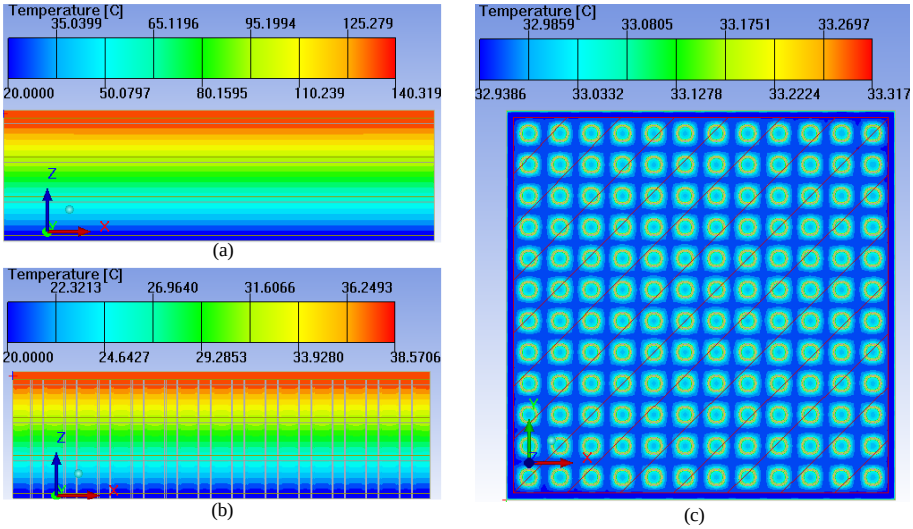

Fig. 3.4: CFD simulation results of different PCBs. (a) vertical cut plane, 4-layer PCB, thickness: 1.6 mm, 2-oz copper on each layer, no via, power P = 1 W; (b) 4-layer PCB, thickness: 1.6 mm, 2-oz copper each layer, via diameter ϕ = 0.25 mm, power, P = 10 W, (c) 4-layer PCB (1.6 mm, 2 oz each layer), ϕ = 0.25 mm, P = 10 W. Source: [**J3**].

thermal resistance for the via array, as shown in Fig. 3.3(a) and (b). Based on (3.3), the optimal via diameter versus the filler thermal conductivity can be plotted, as shown in Fig. 3.3(c). It is seen that as the increase of the thermal conductivity, the optimal via diameter also rises. Fig. 3.3(c) enables designers to select the optimal via diameter for thermal resistance minimization of PCB via arrays.

3.2.3 CFD and Experimental Results

CFD simulations of different PCB via arrays have been performed for the DPAK (TO252) package, as shown in Fig. 3.4. With the help of vias, the thermal resistance of a PCB is remarkably decreased from 120.32 K/W (no via) to 1.86 K/W (with vias, ϕ = 0.25) [**J3**]. Fig. 3.5(a) and (b) shows the calculated and simulated thermal resistances for a PCB via array with different via patterns, diameters and filler materials. It is seen that the simulations coincide with the calculations. Additionally, a proper design of the vias (i.e., pattern, diameter, filler material, etc) enables a remarkable thermal resistance reduction [**J3**].

An experimental setup was built up, as shown in Fig. 3.6(a). The infrared thermal image of the setup in the case of each DPAK diode generating 2.4-W power loss is shown in Fig. 3.6(b). As can be seen, the diode mounted on the

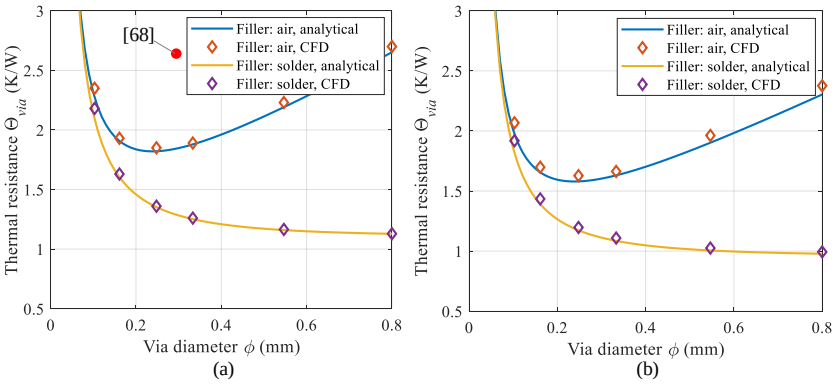

Fig. 3.5: Comparison between the calculated and simulated thermal resistance of vias with different parameters for the DPAK (TO-252): (a) pattern I; (b) pattern II. Source: **[J3]**.

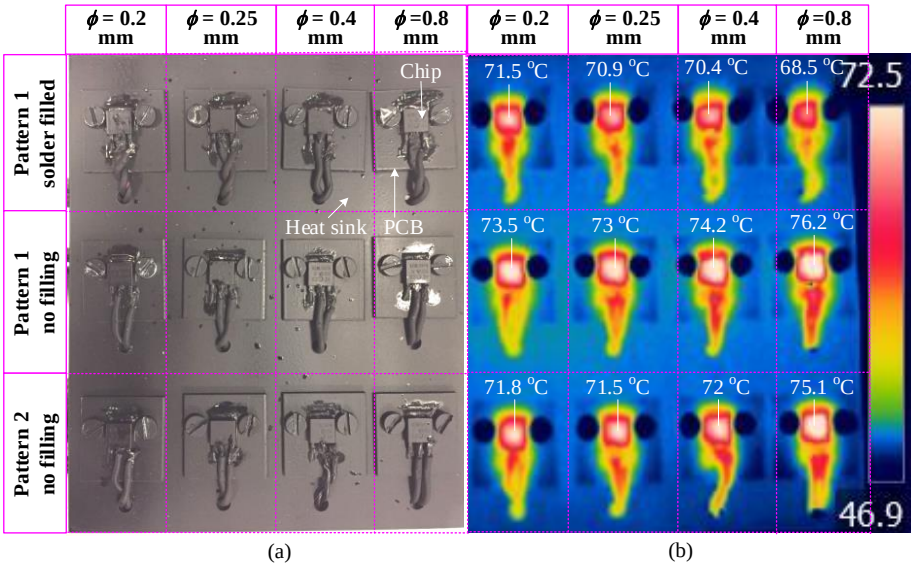

Fig. 3.6: (a) Photo of the experimental setup: each diode (package: TO252) is attached to a PCB and cooled by the heatsink; (b) thermal image of the experimental setup in steady-state when each diode generates 3-W power loss. Source: **[J3]**.

PCB with a via diameter of 0.25 mm has the lowest top-case temperature if the vias are not filled. With solder filled, the via diameter 0.8 mm enables the PCB to achieve the minimum thermal resistance. The trend agrees with the above theoretical analysis **[J3]**.

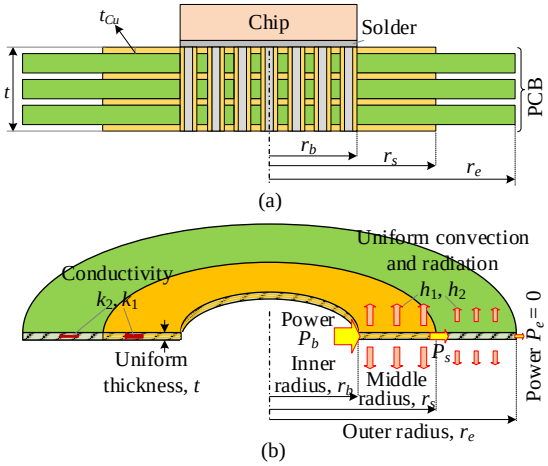

Fig. 3.7: Simplified PCB board. (a) Vertical cut plane of a PCB board; (b) Heat transfer in a circular PCB board: heat conduction in the radial direction, convection and radiation in the axial direction. Source: **[C1]**.

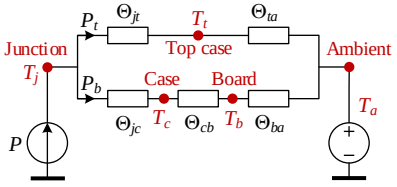

Fig. 3.8: Equivalent thermal resistance diagram for a DPAK package mounted on a PCB. Source: **[C1]**.

3.3 Thermal Modeling and Sizing of PCB Copper Pads

3.3.1 Heat Transfer in a Circular PCB

For the natural convection in the air, the flow remains laminar when the temperature difference involved is less than 100 °C and the characteristic length of the body is less than 0.5 m [117], which is almost always the case in electronic systems. Therefore, the airflow in the following analysis is assumed to be laminar. The natural convection heat transfer coefficient for laminar flow of air at atmospheric pressure, and radiation heat transfer coefficient are given as [117]

$$\begin{cases} h_{conv} = \lambda[(T_x - T_a)/L_c]^{0.25} \\ h_{radi} = \varepsilon\sigma[(T_x + 273)^2 + (T_a + 273)^2] \times [(T_x + 273) + (T_a + 273)] \\ h = h_{conv} + h_{radi} \end{cases} \tag{3.4}$$

where T_x is the PCB surface temperature. The PCB mask is an epoxy-based lacquer, which is an organic material and has a high emissivity of about 0.9 [118]. Fig. 3.7 shows a simplified circular PCB board, where an axisymmetric heat source (package) is located at the inner radius, and the outer edge is assumed to be isothermal. In addition to the heat source, there are two heat transfer zones, i.e., the middle zone (copper zone) within $[r_b,\ r_s]$ and the outer zone (FR4 zone) within $[r_s,\ r_e]$. Heat transfers in both the radial/lateral (conduction) and axial/vertical (convection and radiation) directions. For the lateral heat conduction, the thermal conductivities in the two zones are

$$\begin{cases} k_1 = k_{Cu} N_l t_l / t + k_{FR4}(1 - N_l t_l / t) \\ k_2 = k_{FR4} \end{cases} \tag{3.5}$$

In the vertical direction, it is assumed that the convective and radiative heat transfer coefficients, h_{conv} and h_{radi}, are constant along the radial direction. Then, in the cylindrical coordinate system, the governing equation for the steady-state heat transfer is [119]

$$\begin{cases} \frac{\mathrm{d}^2 T}{\mathrm{d}r^2} + \frac{1}{r}\frac{\mathrm{d}T}{\mathrm{d}r} - \frac{h}{kt}(T - T_a) = 0 \\ P = -2\pi r k t \frac{\mathrm{d}T}{\mathrm{d}r} \end{cases} \tag{3.6}$$

where T represents the temperature at the radius of r. By doing algebraic manipulations, (3.6) can be solved and the solutions are obtained as

$$\begin{cases} \Delta T = a I_0(z) + b K_0(z) \\ P = -2\pi k t z [a I_1(z) + b K_1(z)] \end{cases} \tag{3.7}$$

where $\Delta T = T - T_a$, , I_0 is the modified Bessel function of the first kind and order 0, I_1 is the modified Bessel function of the first kind and order 1, K_0 iss the modified Bessel function of the second kind and order 0, K_1 is the modified Bessel function of the second kind and order 1, and a and b are arbitrary constants. Eliminating a and b, and applying the two-port theory yield

$$\begin{bmatrix} \Delta T_i \\ P_i \end{bmatrix} = \mathbf{T}_{ij} \begin{bmatrix} \Delta T_j \\ P_j \end{bmatrix} = \begin{bmatrix} A_{ij} & B_{ij} \\ C_{ij} & D_{ij} \end{bmatrix} \begin{bmatrix} \Delta T_j \\ P_j \end{bmatrix} \tag{3.8}$$

where the subscript i and j represent the sending and receiving ports at any locations, T_{ij} is the transmission matrix, $z_i = r_i\sqrt{h/(kt)}$, $A_{ij} = z_j[I_1(z_j)K_0(z_i) + I_0(z_i)K_1(z_j)]$, $z_j = r_j\sqrt{h/(kt)}$, $B_{ij} = [I_0(z_j)K_0(z_i) - I_0(z_i)K_0(z_j)]/(2\pi kt)$, $C_{ij} = 2\pi kt z_i z_j [I_1(z_j)K_1(z_i) - I_1(z_i)K_1(z_j)]$, and $D_{ij} = z_i[I_0(z_j)K_1(z_i) + I_1(z_i)K_0(z_j)]$.

The heat transfer from r_s to r_e (including radial conduction and axial convection and radiation) can be illustrated with a two-port system, i.e., the temperature potential ΔT_s and heat flow P_s can be obtained as (3.8). Assume that the outer edge of $r = r_e$ is adiabatic in the horizontal direction, i.e., P_e =

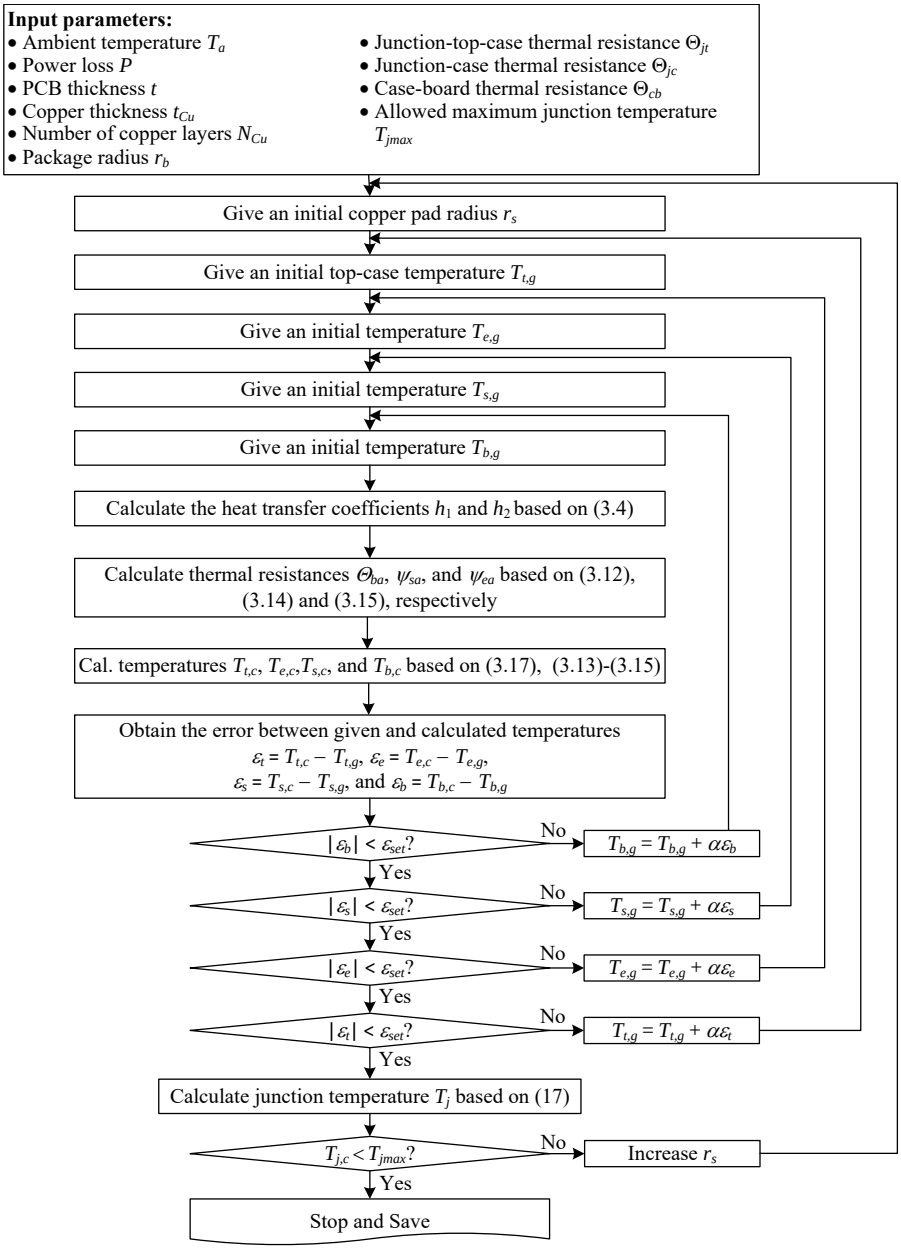

Fig. 3.9: Flowchart for calculating the thermal resistance of a PCB copper pad. Source: **[C1]**.

0, then the thermal resistance from r_s to the ambient, Θ_{sa}, can be derived as

$$\begin{bmatrix} \Delta T_s \\ P_s \end{bmatrix} = \mathbf{T}_{se} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} = \begin{bmatrix} A_{se} & B_{se} \\ C_{se} & D_{se} \end{bmatrix} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} \tag{3.9}$$

$$\Theta_{sa} = \frac{\Delta T_s}{P_s} = \frac{A_{se}}{C_{se}} \tag{3.10}$$

As for the two-port system from r_b to r_s, we have

$$\begin{aligned} \begin{bmatrix} \Delta T_b \\ P_b \end{bmatrix} &= \mathbf{T}_{bs} \begin{bmatrix} \Delta T_s \\ P_s \end{bmatrix} = \begin{bmatrix} A_{bs} & B_{bs} \\ C_{bs} & D_{bs} \end{bmatrix} \begin{bmatrix} \Delta T_s \\ P_s \end{bmatrix} \\ &= \mathbf{T}_{bs}\mathbf{T}_{se} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} = \begin{bmatrix} A_{bs}A_{se} + B_{bs}C_{se} & A_{bs}B_{se} + B_{bs}D_{se} \\ C_{bs}A_{se} + D_{bs}C_{se} & C_{bs}B_{se} + D_{bs}D_{se} \end{bmatrix} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} \end{aligned} \tag{3.11}$$

Then the thermal resistance from r_b to the ambient, and the temperature at r_b can be obtained as

$$\Theta_{ba} = \frac{\Delta T_b}{P_b} = \frac{A_{bs}A_{se} + B_{bs}C_{se}}{C_{bs}A_{se} + D_{bs}C_{se}} \tag{3.12}$$

$$T_b = T_a + P_b\Theta_{ba} \tag{3.13}$$

Manipulating (3.9) and (3.11) yields the equivalent thermal resistance from r_s to the ambient and the thermal resistance from r_e to the ambient when an axisymmetric heat source is located at r_b

$$\psi_{sa} = \frac{\Delta T_s}{P_b} = \frac{A_{se}}{C_{bs}A_{se} + D_{bs}C_{se}} \Rightarrow T_s = T_a + P_b\psi_{sa} \tag{3.14}$$

$$\psi_{ea} = \frac{\Delta T_e}{P_b} = \frac{1}{C_{bs}A_{se} + D_{bs}C_{se}} \Rightarrow T_e = T_a + P_b\psi_{ea} \tag{3.15}$$

It should be noted that ψ_{sa} and ψ_{ea} are defined similarly to the thermal metric ψ_{JT} adopted by the industry (JEDEC Standard: JESD51-2A [120]). They are not true thermal resistances, but could be used to calculate the temperatures at r_s and r_e. The analysis above is carried out by assuming that the heat source, copper pad, and PCB are circular. In practice, the majority of them are rectangular in shape; thus the equivalent radius of a rectangular shape can be approximated by $r_x = \sqrt{a_x b_x/\pi}$ where a_x and b_x are the rectangular side lengths and the subscript 'x' denotes 'b', 's', and 'e'.

3.3.2 Algorithm for Copper Pad Sizing

When an SMD is mounted on a PCB, the heat generated inside the device will be dissipated in two parallel pathways: one is from the junction to the top case, and finally to the ambient; the other is from the junction to the bottom case, then to the board, and finally to the ambient. Fig. 3.8 shows the equivalent thermal resistance diagram for a DPAK package mounted on a PCB. If all the thermal resistances are known, then the top-case and junction temperatures can be predicted by

$$T_t = \frac{P\Theta_{ta}(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})}{\Theta_{jt} + \Theta_{ta} + \Theta_{jc} + \Theta_{cb} + \Theta_{ba}} + T_a \tag{3.16}$$

$$T_j = \frac{P(\Theta_{jt} + \Theta_{ta})(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})}{\Theta_{jt} + \Theta_{ta} + \Theta_{jc} + \Theta_{cb} + \Theta_{ba}} + T_a \tag{3.17}$$

where Θ_{jt}, Θ_{jc}, and Θ_{ta} are package dependent thermal resistances. The junction-top-case and junction-case thermal resistances Θ_{jt} and Θ_{jc} can be regarded as temperature-independent parameters, whereas the top-case-ambient thermal resistance Θ_{ta} relies on temperature. The detailed analysis and derivation of the three parameters are given in [**C1**].

If the top-case temperature T_t and other thermal resistances are determined, then the board-ambient thermal resistance Θ_{ba} can be obtained as

$$\Theta_{ba} = \frac{P\Theta_{ta}(\Theta_{cb} + \Theta_{jc}) - (T_t - T_a)(\Theta_{jc} + \Theta_{cb} + \Theta_{jt} + \Theta_{ta})}{T_t - T_a - P\Theta_{ta}} \tag{3.18}$$

For the heat transfers from the junction to the top-case, from the junction to the bottom-case, and from the case to the board, there is only heat conduction, and therefore the corresponding thermal resistances Θ_{jt}, Θ_{jc}, and Θ_{cb} are constant if neglecting the relatively small material property variation over temperature. However, the heat transfers from the top-case to the ambient and from the board to the ambient involve convection and radiation. Hence, the thermal resistances Θ_{ta} and Θ_{ba} are temperature related. Meanwhile, the total power loss P is divided into two parts P_t and P_b, i.e., $P = P_t + P_b$. Thus, the thermal resistance Θ_{ta} and Θ_{ba} interact with each other as well. Therefore, an algorithm taking into account all the five thermal resistances in Fig. 3.8 is developed to design the copper pad size, as shown in Fig. 3.9.

Before the design, the system parameters, e.g., the ambient temperature T_a, total Power loss P, PCB thickness t, copper thickness t_{Cu}, number of copper layers N_{Cu}, package radius r_b, junction-top-case thermal resistance Θ_{jt}, junction-case thermal resistance Θ_{jt}, case-board thermal resistance Θ_{cb}, allowed maximum junction temperature T_{jmax}, should be determined. Firstly, a small initial value is given to the copper pad radius r_s before the four given temperatures $T_{t,g}$, $T_{e,g}$, $T_{s,g}$, and $T_{b,g}$, are initialized. Then the heat transfer coefficients h_1 and h_2 can be calculated based on (3.4), and the thermal resistances Θ_{ta}, Θ_{ba}, ψ_{sa} and ψ_{ea} can be obtained accordingly. After that, the calculated temperatures $T_{t,c}$, $T_{e,c}$, $T_{s,c}$ and $T_{b,c}$ are compared with the given temperatures $T_{t,g}$, $T_{e,g}$, $T_{s,g}$, and $T_{b,g}$; also the errors can be obtained, i.e., $\epsilon_t = T_{t,c} - T_{t,g}$, $\epsilon_e = T_{e,c} - T_{e,g}$, $\epsilon_s = T_{s,c} - T_{s,g}$, and $\epsilon_b = T_{b,c} - T_{b,g}$. If the absolute error ϵ_x is greater than the preset limit ϵ_{lmt}, then the given temperature $T_{x,g}$ will be updated by adding $\alpha\epsilon_x$ where α is an incremental coefficient and the subscript x represents 't', 'e', 's', or 'b'. If all four temperature errors are smaller than ϵ_{lmt}, then the algorithm proceeds to calculate the junction temperature T_j according to (3.17). If the calculated T_j is higher than the allowed maximum junction temperature, then the copper pad radius r_e will be increased. Otherwise, it implies that the current copper pad radius r_e is

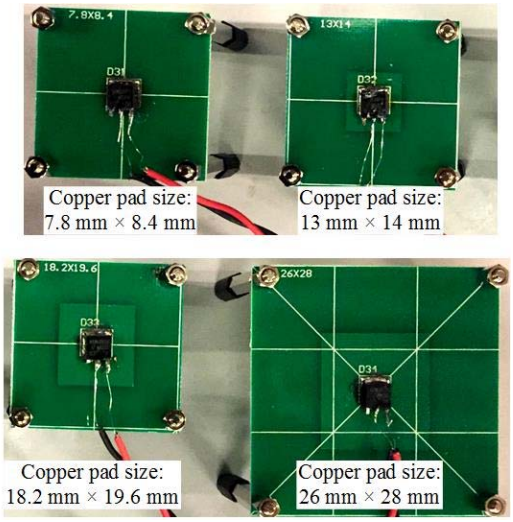

Fig. 3.10: Photo of the built PCBs with different copper pad sizes. Source: [**C1**].

large enough for cooling. In this way, we can find the minimum r_e, which can help to achieve the maximum power density while meeting the thermal specifications.

3.3.3 Experimental Results

Four DPAK diodes VS-6EWL06FN-M3 are mounted on four 2-layer PCBs (70-μm copper thickness for each layer) with different sizes of copper pads, as shown in Fig. 3.10. All diodes are serially connected to a dc power source, and thus the diodes can generate equal power losses, which are further dissipated by the copper pad and natural convection. The steady-state thermal images of the diodes are captured for different sizes of copper pads, as shown in Fig. 3.11. Fig. 3.12 depicts the measured and calculated junction and top-case temperatures when P = 0.5 W. As can be seen, there is a significant top-case temperature difference between the conventional model [67, 121] and the measurements, especially when the copper pad radius is smaller than 15 mm. In contrast, the proposed model can help to predict the top-case temperature with a small error. Therefore, the new model can be used to predict the junction temperature. The maximum operating junction temperature of the selected diode VS-6EWL06FN-M3 is 175 °C. For the sake of high reliability, the maximum junction temperature T_{jmax} should be lower than the limit, e.g., T_{jmax} = 100 °C. Then the minimum copper radius can be found, as illustrated in Fig. 3.12. Based on the proposed model, the minimum copper radius r_e is 3.9 mm, whereas the conventional model gives a minimum copper radius

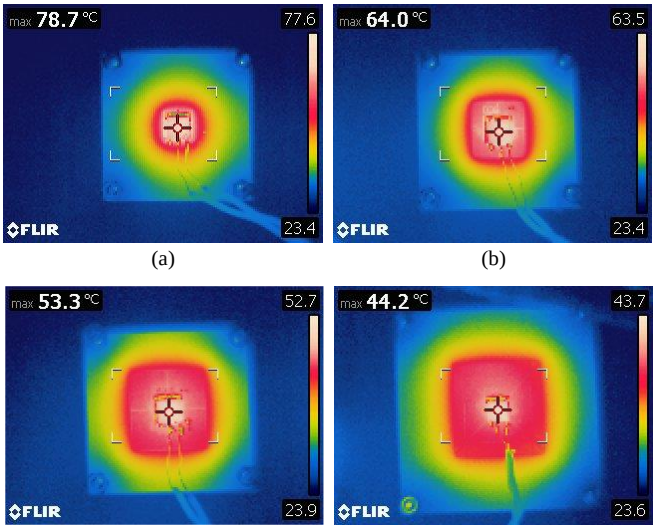

Fig. 3.11: Thermal images of diodes mounted on PCBs with 0.5-W power losses injected and different sizes of copper pads. (a) copper pad size: 7.8 mm × 8.4 mm; (b) copper pad size: 13 mm × 14 mm; (c) copper pad size: 18.2 mm × 19.6 mm; (d) copper pad size: 26 mm × 28 mm. Source: **[C1]**.

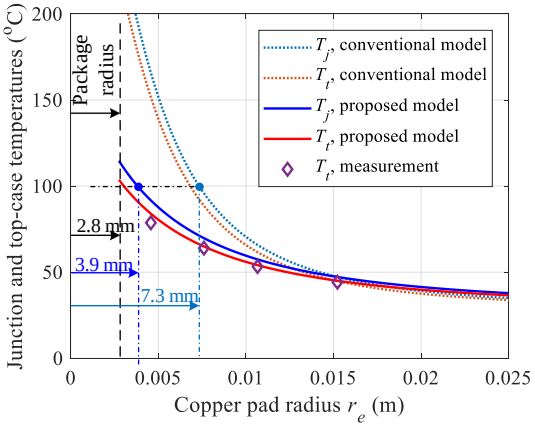

Fig. 3.12: Comparison of the junction and top-case temperatures between measurements and calculations when 0.5-W power losses are generated inside the diode. Source: **[C1]**.

of 7.3 mm, which corresponds to a 250% increase of the copper pad area compared to the design of r_e = 3.9 mm.

3.4 Summary

This chapter develops analytical thermal resistance models for PCB vias and pads. A one-dimensional thermal resistance model is built for two patterns of via arrays; an optimal via design trajectory is then proposed for thermal resistance minimization in different specifications. An axisymmetric thermal resistance model is developed for naturally cooled PCB pads; an algorithm is proposed to find the thermal resistance of PCB pads with different parameters. CFD simulations and experimental measurements agree well with the analytical models. It can be concluded that 1) when the PCB parameters are determined, there exists an optimal via diameter which can achieve the minimum thermal resistance; 2) the layout of pattern 2 and solder filling can help to reduce the thermal resistance of vias; 3) the conventional analytical thermal model for PCB pads overestimates the semiconductor junction temperature, particularly when the copper pad is small in size; by contrast, the proposed thermal model of PCB pads is able to accurately predict the device junction temperature.

Related Publications

J3. **Y. Shen**, H. Wang, and F. Blaabjerg, "Thermal Resistance Modelling and Design Optimization of PCB Vias," *Microelectron. Rel.*, vol. PP, no. 99, pp. 1-6, Aug. 2018.

Main Contribution:
An analytical thermal resistance model is developed for PCB vias, and the optimal design trajectory is identified for thermal resistance minimization.

C1. **Y. Shen**, H. Wang, and F. Blaabjerg, "Thermal Modeling and Sizing of PCB Copper Pads," in *Proc. ECCE 2018*, Portland, 2018, pp. 1-7.

Main Contribution:
An analytical thermal resistance model and sizing algorithm are proposed for PCB pads.

Chapter 4

Characterization and Electro-Thermal Modeling of GaN eHEMTs

4.1 Abstract

In order to better optimize GaN eHEMT based PV microinverters, the critical parameters, i.e., die area, transconductance, drain-source on-state resistance and output capacitance of a series of GaN eHEMTs are characterized, yielding generic parameter models. In addition, the turn-off power loss and junction-case thermal impedance of those GaN eHEMTs are modeled as well.

4.2 Parameter Characterization of GaN eHEMTs

For the series of 650-V GaN eHEMTs from GaN Systems^{TM}, the current rating and on-state drain-source resistance of a transistor are achieved by employing different standard die units in parallel, as shown in Fig. 4.1. The numbers of die units inside GS66502B, GS66504B, GS66506T and GS66508B are 2, 4, 6, and 8, respectively. Thus, their on-state drain-source resistances at 25 °C are inversely proportional to the number of die units N_{unit}, i.e., $R_{ds,on@20C} = 200$ mΩ for GS66502B [123], 100 mΩ for GS66504B [124], 67 mΩ for GS66506T [125], and 50 mΩ for GS66508B [126].

4.2.1 Normalized Drain-Source On-State Resistance

Due to the advanced GaNPX® package, a very low parasitic inductance (0.2 nH) can be achieved for the 650-V GaN eHEMTs [127]. As results, a fast

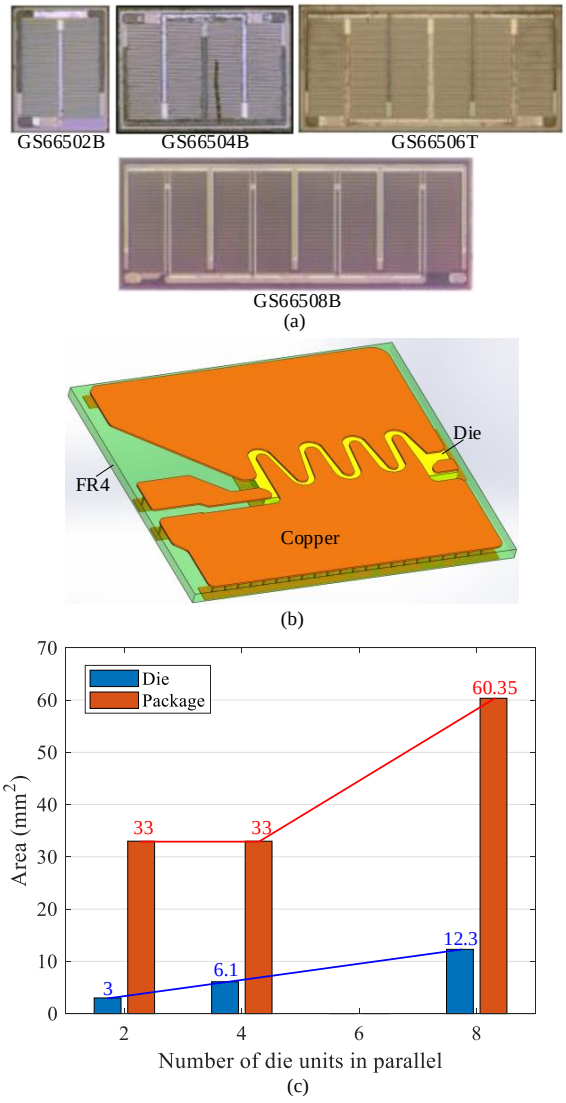

Fig. 4.1: Die and package of the 650-V GaN eHEMTs of GaN Systems^{TM}. (a) Microscopy images of four 650-V GaN dies [122]; The numbers of die units inside GS66502B, GS66504B, GS66506T and GS66508B are 2, 4, 6, and 8, respectively. The total die area of GS66508P (12.3 mm^2 [85]) is almost twice of that of GS66504B (6.1 mm^2 [86]). (b) Package structure of GaN eHEMT GS66508P built up in Solidworks. (c) Die and package areas of the GaN eHEMTs GS66502B, GS66504B, and GS66508B. Source: [**J4**].

turn-on/off is possible, the turn-off loss of a GaN eHEMT can be as low as the energy stored in the parasitic output capacitor, and the drain-source current flowing through the device can be evenly distributed to each die unit. Therefore, the characteristics of a GaN unit are firstly investigated here.

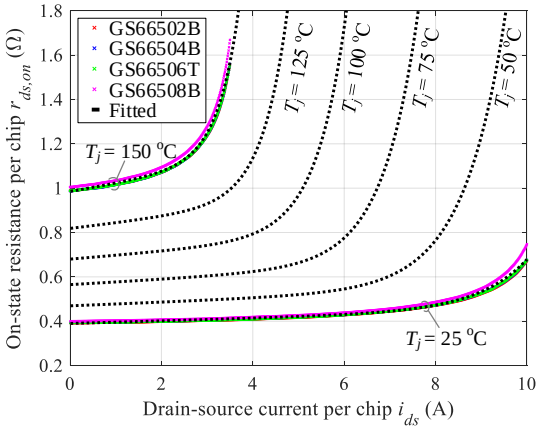

Fig. 4.2: Drain-source on-state resistance per 650-V GaN die unit of GaN Systems. The crosses represent the values from the datasheets [123–126], and the dashed lines are the fitting results. Source: **[J4]**.

Fig. 4.2 presents the dependence of the on-state resistance per unit $r_{ds,on}$ on the drain-source current flowing through a die unit, i_{ds} and the junction temperature T_j. As can be seen, the on-state drain-source resistance per GaN unit increases with respect to the junction temperature T_j and drain-source current i_{ds}. All the four GaN eHEMTs have almost the same performance for the normalized on-state resistance $r_{ds,on}$. Therefore, the on-state drain-source resistance of a GaN device with N_{unit} die units can be fitted as

$$R_{ds,on}(I_{ds}, T_j) = \frac{r_a \exp(r_b I_{ds}/N_{unit}) + r_c \exp(r_d I_{ds}/N_{unit})}{N_{unit}} \tag{4.1}$$

in which $I_{ds} = N_{unit} i_{ds}$ is the total drain-source current flowing through the GaN device, r_a, r_b, r_c, and r_d are junction temperature dependent parameters and can be fitted as $r_a = r_{a1}\exp(r_{a2}T_j)$, $r_b = r_{b1}\exp(r_{b2}T_j)$, $r_c = r_{c1}\exp(r_{c2}T_j)$, and $r_d = r_{d1}\exp(r_{d2}T_j)$, where $r_{a1}, r_{a2}, r_{b1}, r_{b2}, r_{c1}, r_{c2}, r_{d1}$, and r_{d2} are fitted coefficients. More detailed analysis on the parameters characterization of 650-V GaN eHEMTs can be found in **[J4]**.

4.2.2 Normalized Transconductance and Parasitic Capacitance

The switching performance and gate drive loss depend on the transconductance G_{fs} and the parasitic capacitances of a GaN eHEMT, i.e., the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse capacitance C_{rss}. The transconductance is defined as

$$G_{fs} = \frac{I_{ds}}{V_{gs} - V_{th}} \tag{4.2}$$

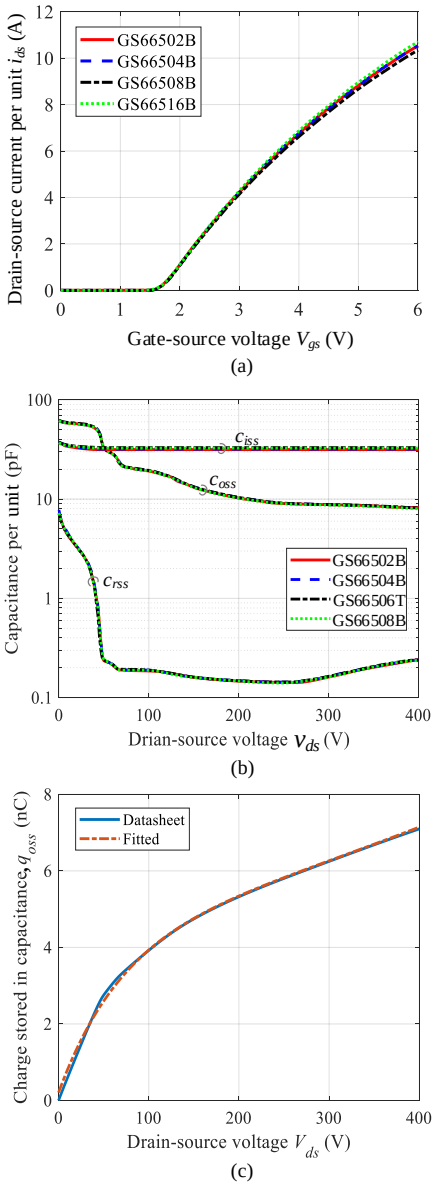

Fig. 4.3: Normalized transconductance, parasitic capacitance and charge per GaN die unit: (a) transconductance characteristics for a series of 650-V eHEMTs from GaN Systems, GS66502B, GS66504B, GS66508B and GS66516B, (b) parasitic output capacitance, reverse capacitance and input capacitance per die unit for GS66502B/04B/06T/08B, (c) fitted charge stored in the output capacitance of a die unit. Source: [**J4**].

where V_{gs} denotes the gate-source voltage, and V_{th} is the gate-source threshold voltage of a GaN eHEMT. Divided by the number of die units inside a

GaN eHEMT, the normalized transfer characteristic $i_{ds} - V_{gs}$ can be obtained from the datasheets [123–126], as shown in Fig. 4.3(a). It is seen that all the GaN eHEMTs share almost the same normalized transfer characteristic, implying that $G_{fs} = N_{unit} g_{fs}$ holds for all the 650-V series of GaN eHEMTs.

The capacitances are proportional to the total die area of a GaN eHEMT. Based on the datasheets [123–126], the capacitance per unit with respect to the drain-source voltage v_{ds} can be obtained, as shown in Fig. 4.3(b). It is seen that all the investigated GaN transistors, i.e., GS66502B, GS66504B, GS66506T, and GS66508B, share the same normalized capacitance for the three capacitors, c_{iss}, c_{oss}, and c_{rss}. Therefore, the actual parasitic capacitance of a GaN eHEMT can be obtained by $C_{iss} = N_{unit} c_{iss}$, $C_{oss} = N_{unit} c_{oss}$, and $C_{rss} = N_{unit} c_{rss}$.

Particularly, the charge stored in the parasitic output capacitor C_{oss}, i.e., Q_{oss}, determines the ZVS realization of a GaN eHEMT. Therefore, the characteristics of the output charge per unit, q_{oss}, with respect to the drain-source voltage v_{ds} are shown in Fig. 4.3(c). The parasitic output charge is governed by

$$q_{oss}(V_{ds}) = \int_0^{V_{ds}} c_{oss}(v_{ds}) dv_{ds} = \int_{V_{ds}}^0 c_{oss}(v_{ds}) dv_{ds} \tag{4.3}$$

where V_{ds} represents the starting or ending drain-source voltage when charging or discharging the parasitic output capacitor c_{oss}. It can be seen that the parasitic output charge of a GaN device is also proportional to the embedded die units inside. Fitting the normalized output charge yields

$$q_{oss}(V_{ds}) = q_a \exp(q_b V_{ds}) + q_c \exp(q_d V_{ds}) \tag{4.4}$$

where q_a, q_b, q_c and q_d are fitted coefficients. Then the actual parasitic output charge Q_{oss} of a GaN eHEMT can be derived by $Q_{oss} = N_{unit} q_{oss}$.

4.3 Turn-off Power Loss of GaN eHEMTs

A double-pulse testing setup has been built up to characterize the power devices. The turn-off waveforms at V_{ds} = 200 V and I_{ds} = 1.43 A are shown in Fig. 4.4(a). When the gate voltage V_{gs} falls to below the threshold voltage, the channel is cut off quickly, but the drain-source voltage V_{ds} has not significantly increased. Therefore, the drain-source current is diverted to the output capacitor of the GaN eHEMT, causing V_{ds} to rise from 0 to 200 V. The measured turn-off energy loss is approximately equal to the energy stored in the output capacitor C_{oss}, as shown in Fig. 4.4(b). It should be noted that the calculated turn-off energy loss E_{off} ($\approxeq E_{oss}$) is not truly dissipated during the turn-off period. If the switch is subsequently turned on under hard switching, then the energy stored in the output capacitor C_{oss}, i.e., E_{oss}, is

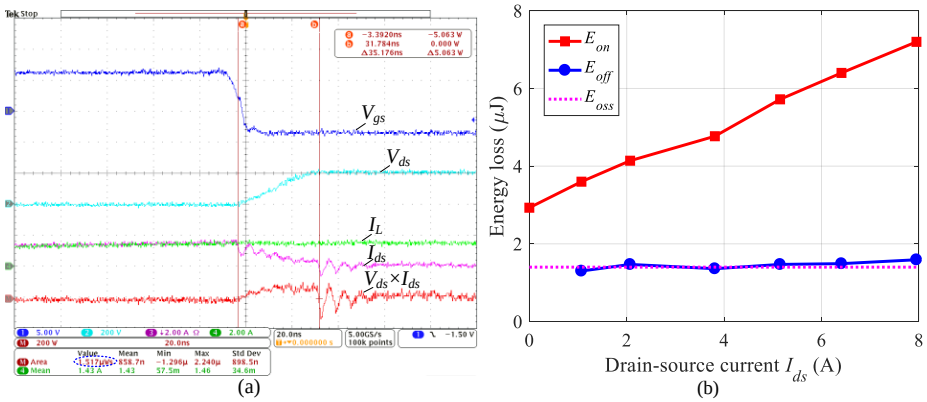

Fig. 4.4: Results of the double-pulse test on a GaN eHEMT GS66504B bridge: (a) measured turn-off waveforms of GS66504B, (b) comparison between the measured turn-off energy loss and the energy stored in the output capacitance of GS66504B at V_{ds} = 200 V. Source: **[J1]**.

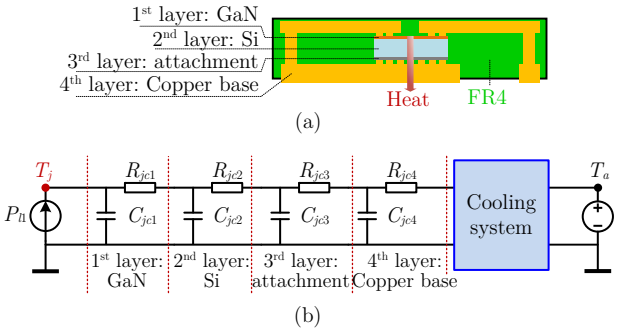

Fig. 4.5: (a) Vertical structure of a bottom-cooled GaN eHEMT with the GaNPX® package; (b) Four-layer Cauer-type junction-case thermal impedance model. Source: **[J4]**.

dissipated on the channel. If the switch can achieve ZVS-on, then the energy stored in the output capacitor will be transferred instead of being dissipated. Therefore, for the converters in which the employed GaN eHEMTs can realize ZVS-on, the GaN eHEMTs can achieve a quasi-lossless turn-off as well **[J2]**.

4.4 Junction-Case Thermal Impedance of GaN eHEMTs

The vertical structure of a bottom-cooled GaN eHEMT with the GaNPX package is shown in Fig. 4.5(a). For the heat transferred from the junction to case, there are four layers involved, i.e., a GaN die layer, a Si layer, an attachment layer, and a copper base layer. Thus, the Cauer-type junction-case thermal model can be illustrated in Fig. 4.5(b), where the Cauer-type *RC* parameters

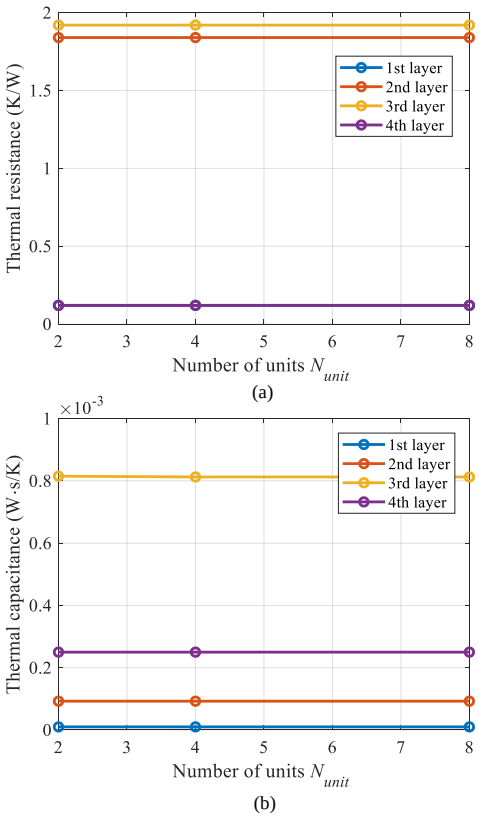

Fig. 4.6: Normalized thermal resistance and capacitance of each layer for the 650-V GaN Systems eHEMTs GS66502B ($N_{unit} = 2$), GS66504B ($N_{unit} = 4$) and GS66508B ($N_{unit} = 8$). (a) thermal resistance per unit; (b) thermal capacitance per unit. Source: **[J4]**.

can be derived based on the geometry dimension and material property of each layer. The thermal resistance can be calculated by $R_{th} = d/(\lambda \cdot A_c)$, where d is the layer thickness, λ is the material thermal conductivity in W/(m-K), and A_c is the chip area. The junction-case thermal capacitance is governed by $C_{th} = c \cdot \rho \cdot d \cdot A_c$, where c is the specific heat in Ws/(g·K), and ρ is the material density in g/m^3.

It is obvious that the junction-thermal resistance is theoretically inversely proportional to the total chip area A_c or the number of die units N_{unit} whereas the thermal capacitance is directly proportional to A_c or N_{unit}. The RC parameters of each layer of the 650-V GaN eHEMTs (GS66502B, GS66504B, GS66508B) are extracted from the datasheets [123, 124, 126]. Then the normalized thermal resistance r_{jcn} and capacitance c_{jcn} (i.e., the thermal resistance and capacitance per die unit) can be obtained by $r_{jcn} = R_{jcn}N_{unit}$ and

$c_{jcn} = C_{jcn}/N_{unit}$, where n represents the layer number. For different numbers of units N_{unit}, the normalized thermal resistance c_{jcn} and capacitance c_{jcn} of each layer are almost the same, as illustrated in Fig. 4.6.

The thermal performance of a GaN eHEMT is also determined by the cooling system which may vary significantly with different designs. Most of the PV microinverter products on the market are filled up with high-thermal-conductivity compound [18] in order to improve the cooling performance and protect the converters from humidity erosion. However, the compound reinforces the thermal cross-coupling among the components inside the microinverter enclosure. The heat propagation from the components to the ambient can be divided into three parts, i.e., from the junction/hotspot to the case, from the case to the enclosure, and from the enclosure to the ambient. For the first two heat transfer paths, heat conduction is the main way, whereas the third heat transfer path, i.e., from the enclosure to the environment, involves all the three heat transfer approaches, heat conduction, convection and radiation. The heat transfer rate of convection is related to the temperature gap between the enclosure surface and the circumstance, whereas the radiation intensity depends on the absolute temperatures [87]. The participation of convection and radiation makes the whole thermal system strongly nonlinear [18].

4.5 Summary

This chapter characterizes the key parameters, i.e., drain-source on-state resistance, transconductance, parasitic capacitance, and models the electro-thermal performance of a series of 650-V GaN eHEMTs. It turns out that an actual GaN eHEMT is achieved by multiple standard die units in parallel, and the normalized characteristics are almost independent of the number of die units inside, which simplifies the design optimization in GaN eHEMT applications.

Related Publications

J4. **Y. Shen**, S. Song, H. Wang, and F. Blaabjerg, "Cost-Volume-Reliability Pareto Optimization of a Photovoltaic Microinverter," *IEEE Trans. Power Electron.*, 2018, Status: to be submitted.

Main Contribution:
Systematic modeling of power loss, thermal impedance, lifetime, cost and volume is developed for the main components. A cost-volume-reliability Pareto optimization method is proposed and executed, which enables a design trade-off among the three performance metrics.

Chapter 5

Cost-Volume-Reliability Pareto Optimization of a PV Microinverter

5.1 Abstract

A multiobjective Pareto optimization routine is proposed in this chapter in order to systematically assess the concepts with respect to the annual degradation, annual energy loss, volume and cost of a PV microinverter. As an important performance criterion, the reliability is included in the multiobjective optimization, which previously has not been discussed in the literature. Thus, a practical trade-off can be made among annual degradation, annual energy yield, volume, and cost for the PV microinverter. Firstly, the operation principle and characteristics of the inverter stage operating in the boundary conduction mode (BCM) are discussed for the waveform modeling. Then, the components parameters are characterized and the electro-thermal models are developed for the microinverter system. After that, the critical performance metrics, reliability, cost, and volume, are modeled before the multiobjective Pareto optimization is conducted.

5.2 Operation Principle and Characteristics of the Proposed PV Microinverter

5.2.1 Topology Description

Fig. 5.1 shows the proposed two-stage PV microinverter topology which consists of a dual-mode-rectifier based series resonant converter (DMR-SRC) as

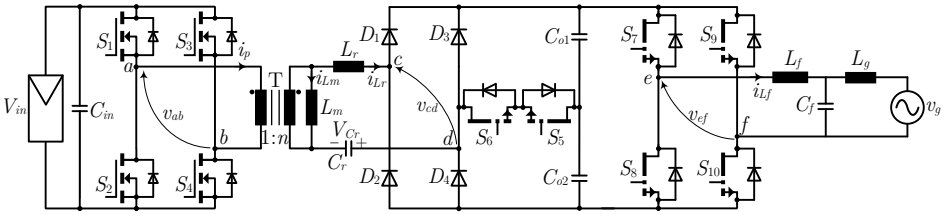

Fig. 5.1: Schematic of the proposed two-stage PV microinverter. Source: **[J4]**.

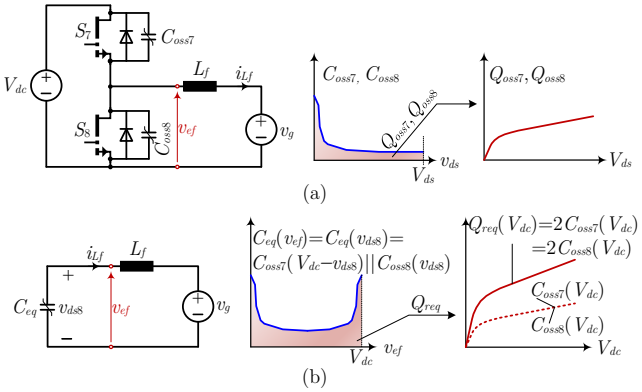

Fig. 5.2: (a) Parasitic output capacitors of GaN transistors in a bridge-leg; (b) Equivalent output capacitor model of the bridge-leg. Source: **[J4]**.

the front-end stage and a full-bridge inverter as the secondary stage. The detailed operation principles, characteristics and experimental verifications of the DMR-SRC have been presented in *Chapter 2* and **[J1]**. A microinverter prototype has been built, as shown in Fig. 2.9. The main focus of this chapter is the design optimization of the inverter stage composed of the active switches $S_7 - S_{10}$, filter inductor L_f and capacitor C_f.

5.2.2 Boundary-Conduction-Mode Operation

The inverter is controlled to operate in the boundary conduction mode (BCM) [30] such that the active switches $S_7 - S_{10}$ can achieve ZVS. The bridge leg $S_7 - S_8$ operates at high frequencies whereas the other bridge leg $S_9 - S_{10}$ is synchronous with the grid voltage v_g. In the positive half line cycle, i.e., $v_g > 0$, S_{10} will be controlled to operate in the on-state and S_9 will be kept in the off-state; when the grid voltage enters into its negative half cycle, i.e., $v_g < 0$, then S_{10} will be turned off, and S_9 will be kept in the on-state. Due to the symmetry of topology and operation, only the positive half line cycle is analyzed.

When $v_g > 0$ and S_{10} are kept on, the inverter can be regarded as a

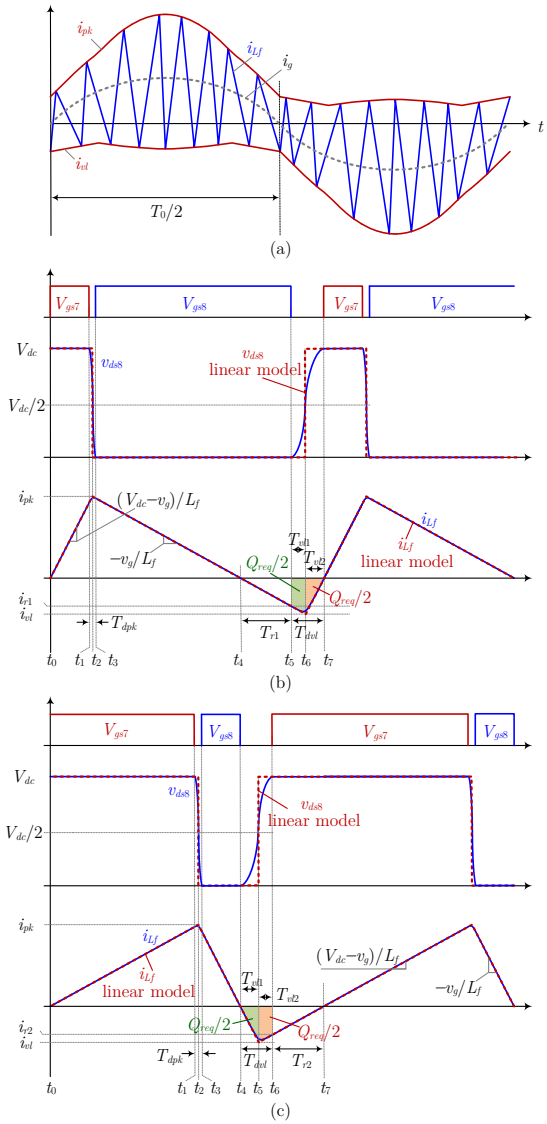

Fig. 5.3: (a) Inductor current over a line cycle; (b) Inductor current and drain-source voltage of S_8, i.e., V_{ds8}, in the case of $v_g < V_{dc}/2$; (c) Inductor current and drain-source voltage of S_8, i.e., V_{ds8}, in the case of $v_g > V_{dc}/2$. Source: **[J4]**.

buck dc-dc converter with a varying output v_g, as shown in Fig. 5.2. The ZVS realization of a switching leg relies on the charging and discharging the parasitic output capacitors of switches. The parasitic output capacitor of a GaN HEMT is highly nonlinear and it varies with respect to its drain-source

voltage v_{ds}, as illustrated in Fig. 5.2(a). For a bridge leg, e.g., $S_7 - S_8$, the two parasitic output capacitors are in parallel in capacitance but in series in the drain-source voltage, i.e., $C_{eq}(v_{ef}) = C_{eq}(v_{ds8}) = C_{oss7}(v_{ds7})||C_{oss8}(v_{ds8}) = C_{oss7}(V_{dc} - v_{ds8})||C_{oss8}(v_{ds8})$. Thus, the equivalent output capacitance of a bridge leg is a bathtub curve with respect to the bridge output voltage v_{ef}. The charge stored in a capacitor, e.g., Q_{oss7}, can be obtained by

$$Q_{oss7}(V_{ds}) = \int_0^{V_{ds}} C_{oss7}(v_{ds})dv_{ds} = \int_{V_{ds}}^0 C_{oss7}(v_{ds})dv_{ds} \tag{5.1}$$

where V_{ds} is the starting or ending voltage when fully discharging or charging a capacitor. For the half-bridge composed with the two parasitic capacitors C_{oss7} and C_{oss8}, the required charge to fully charge or discharge C_{eq} can be calculated by

$$Q_{req}(V_{dc}) = 2Q_{oss7}(V_{dc}) = 2Q_{oss8}(V_{dc}) \tag{5.2}$$

With the BCM modulation, the triangular inductor current i_{Lf} has two bounds, i.e., the upper bound i_{pk} and the lower bound i_{vl}, as shown in Fig. 5.3(a). The average inductor current, i.e., the gray dashed line, equals to the grid current. The lower bound of the triangular inductor current is used to achieve ZVS of S_7 and S_8. In order to minimize the conduction losses, the inductor rms current should be kept possibly low. Therefore, the lower current bound i_{vl} should be maintained small in the absolute value under the condition of ZVS. Thus, when the grid voltage v_g changes over time, the mathematical expression of the lower bound i_{vl} varies and the timing of the gate drive signals change as well. Specifically, in case I ($v_g < V_{dc}/2$), S_8 should be turned off at $i_{Lf} = i_{r1}$ while i_{Lf} is decreasing, and S_7 should be turned on at $i_{Lf} = 0$ while i_{Lf} is increasing; in case II, however, S_8 should be turned off at $i_{Lf} = 0$ while i_{Lf} is decreasing, and S_7 should be turned on at $i_{Lf} = i_{r2}$ while i_{Lf} is increasing. The detailed analysis of the operation process in the two cases can be found in [**J4**].

5.3 Electro-Thermal Modeling

5.3.1 Power Loss Modeling

DC-DC Stage

Since both the dc-dc stage and the inverter stage are integrated into the same PCB, and they will be enclosed by an aluminum case, the power losses of the dc-dc stage will affect the enclosure temperature. Therefore, the power loss characteristic of the dc-dc stage needs to be taken into account. A 60-cell PV module, JinkoSolar JKM300M-60 [128], is assumed to supply the microinverter. The dc-dc stage enables the PV module to operate at maximum power

points (MPPs) irrespective of the solar irradiance S_I and ambient temperature T_a. The measured efficiency of the front-stage dc-dc converter is shown in Fig. 2.14 [43]; then a power loss lookup table can be created with respect to the maximum power point, i.e., the input voltage V_{in} and power P_{in}.

GaN eHEMTs $S_7 - S_{10}$

Since all GaN eHEMTs in the inverter stage, i.e., $S_7 - S_{10}$, can achieve ZVS, their switching loss can be neglected. Thus, only the conduction loss $P_{l,S7}$ is taken into account, and it can be obtained as

$$P_{l,S7} = \frac{1}{T_0}\int_0^{T_0} i_{S7}^2(t) R_{ds,on}(i_{S7}, T_j)dt \approx \frac{1}{T_0}\sum_{m=1}^{M} i_{S7,rms}^2(m\Delta t) R_{ds,on}(i_{S7,rms}, T_j)\Delta t \tag{5.3}$$

where i_{S7} and $i_{S7,rms}$ are the real-time current and rms current flowing through S_7, and $R_{ds,on}$ is the drain-source on-state resistance of S_7. It is noted that $R_{ds,on}$ depends on both the drain-source current i_{S7} and the junction temperature T_j, as illustrated in Fig. 4.2.

Filter Inductor L_f

The planar ER cores have shorter mean turn lengths than EE cores, and therefore provide lower winding resistances for the same core area. The power loss density curve of ferrite material 3C95 is flat concerning the operating temperature [129]. Hence, the four standard 3C95 ER cores, ER18/3.2/10, ER23/3.6/13, ER25/6/15, ER32/6/25, are chosen as the candidate to implement the filter inductor L_f.

The power losses of the filter inductor L_f are composed of the winding loss and the core loss. Since the magnetic cores are excited with nonsinusoidal voltages, and the core loss density can be calculated with the improved generalized Steinmetz equation (iGSE) [130]

Mathematically, the inductor current over a line cycle T_0 can be expressed as a Fourier series. Then, the inductor winding loss $P_{wl,Lf}$ can be obtained by

$$P_{wl,Lf} = \sum_{k=0}^{K} I_{Lf,rms,k}^2 R_{ac,k} \tag{5.4}$$

where k represents the harmonic order, K is the highest harmonic order considered, $I_{Lf,rms,k}$ is the rms value of the kth harmonic of i_{Lf}, and $R_{ac,k}$ is the resistance of a conductor at the frequency of kf_0. The AC resistance of a winding increases dramatically with respect to frequency due to the skin effect and proximity effect, and it can be calculated with the Dowell equation [131, 132].

5.3.2 Thermal Modeling

Most of the PV microinverter products on the market are filled up with high-thermal-conductivity compound in order to improve the cooling performance and protect the converters from humidity erosion. For the proposed microinverter, it is implemented with a four-layer PCB and will be enclosed in an aluminum case with a thickness of 2 mm and a dimension of 150 mm $\times$ 100 mm $\times$ 20 mm by natural cooling. Likewise, the enclosure will be filled up with high-thermal-conductivity (0.7 W/(K·m)) compound [133].

The heat propagation from components to the ambient can be divided into three parts, i.e., from the junction/hotspot to the case, from the case to the enclosure, and from the enclosure to the ambient, as shown in Fig. 5.4(a). The thermal behavior of a system can be modeled by a series of lumps of thermal resistance R and capacitance C. Based on the connection of RC lumps, they can be classified into the Foster and Cauer-type thermal networks. The Cauer RC network enables the series connection of subsystems, and therefore it is considered accurate to predict the temperature of a system [134]. However, the Cauer model parameters are normally hard to derive because the internal geometry, materials, and effective heat path of devices all have to be determined [134].

The Foster RC network is built by fitting the measured temperature dynamics of devices, which means that it is only a behavioral description of a subsystem but no true physical description. Therefore, it is not appropriate to connect multiple Foster-type thermal subsystems; otherwise, there will be a significant error for the temperature prediction [134, 135]. Fortunately, the Foster-type circuit can be transformed into a Cauer circuit which allows for the construction of the thermal models of the complete system [135]. On the other hand, the mathematical representation of the Cauer form is much more complicated than the Foster equation. The Cauer-model parameters cannot be directly used for fast discrete temperature calculation. Therefore, the system-level Cauer model has to be transformed back into a Foster-type circuit for fast discrete temperature calculation.

A system-level thermal modeling method is proposed for the enclosed PV microinverter system, as shown in Fig. 5.5. With the derived thermal impedances, the junction temperature of the kth eHEMT can be obtained by the incremental convolution equations, i.e.,

$$\begin{cases} \Delta T_{jek}(x+1) = \sum\limits_{n=1}^{N} \left[\Delta T_{jek,n}(x) e^{-t/\tau_{k,n}} + P_{lk}(x) R_{k,n} (1 - e^{-t/\tau_{k,n}}) \right] \\ \Delta T_{ea}(x+1) = \Delta T_{ea}(x) e^{-t/\tau_{ea,eq}} + P_{l,tot}(x) R_{ea,eq} (1 - e^{-t/\tau_{ea,eq}}) \\ T_{jk}(x+1) = \Delta T_{jek}(x+1) + \Delta T_{ea}(x+1) + T_a \end{cases} \tag{5.5}$$

where x represents the number of steps in calculation, ΔT_{jek} is the junction-enclosure temperature difference of the kth device, $\Delta T_{jek,n}$ is the junction-

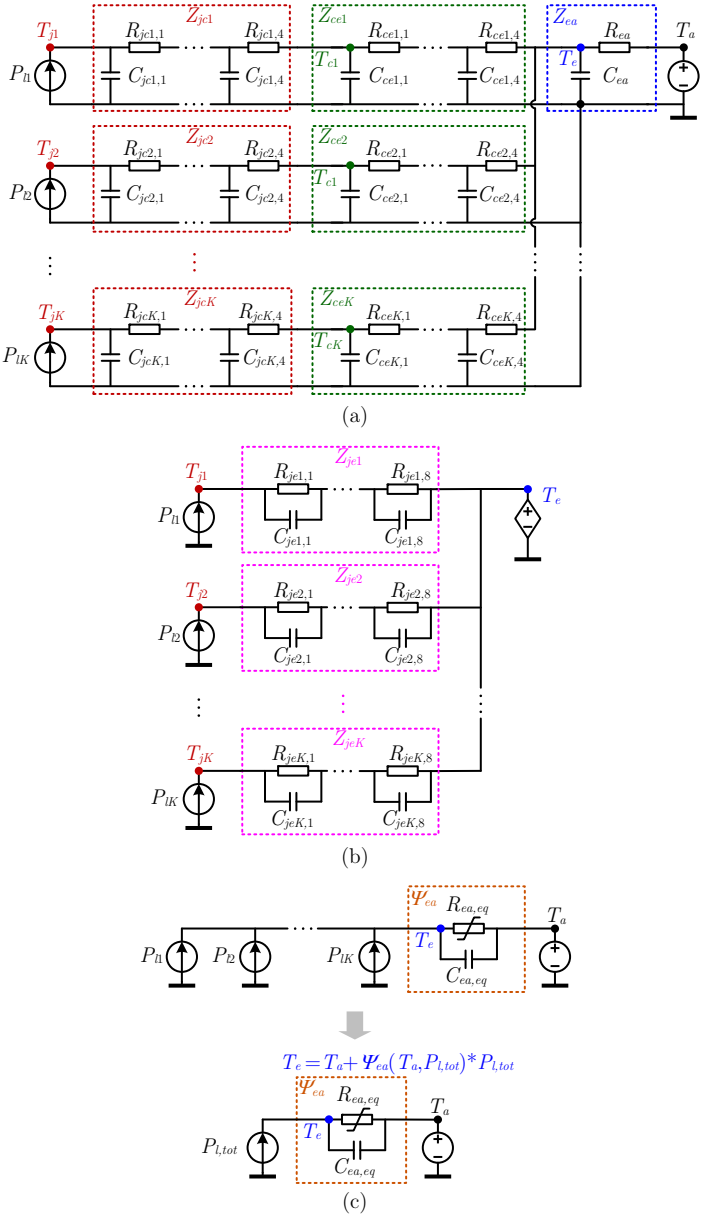

Fig. 5.4: Thermal impedance network of an enclosed converter system. (a) Junction-ambient thermal impedances represented by Cauer thermal models. (b) Junction-enclosure thermal impedances composed of multi-order Foster thermal models. (c) Equivalent enclosure-ambient thermal impedance represented by a multi-order Foster thermal model. Source: **[J4]**.

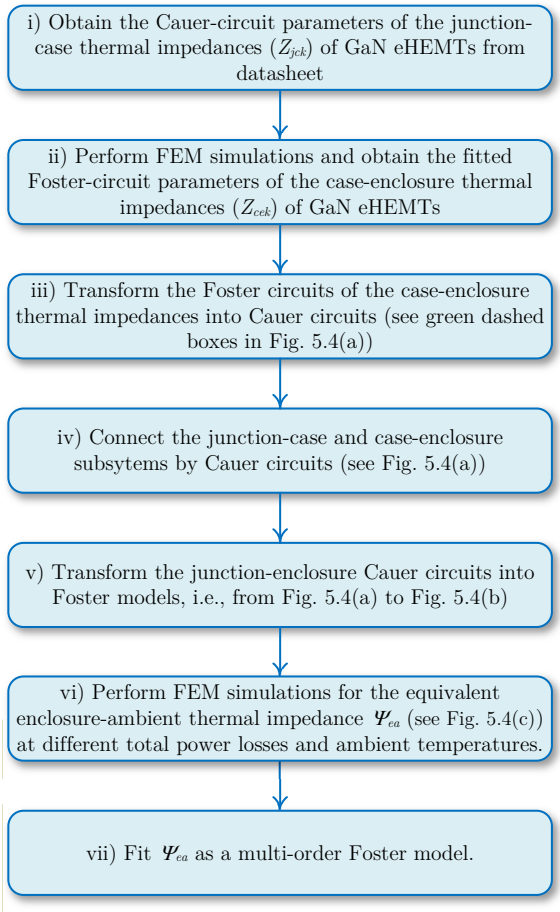

Fig. 5.5: Proposed flowchart of the thermal impedance network derivation for the long-term junction temperature calculation. Source: **[J4]**.

enclosure temperature difference calculated by the nth Foster RC lump (i.e., $R_{k,n}$ and $\tau_{k,n}/R_{k,n}$), P_{lk} is the power loss of the device, ΔT_{ea} is the enclosure-ambient temperature difference, and T_a is the ambient temperature.

The junction-case thermal impedances of GaN eHEMTs have been modeled in *Chapter 4*. The case-enclosure and enclosure-ambient thermal impedances, Z_{ce} and ψ_{ea}, are modeled as follows:

Case-Enclosure and Junction-Enclosure Thermal Impedances–Z_{ce} and Z_{je}

Heat conduction is the primary way for the heat transfered inside the compound-filled enclosure. For the heat transfer from the case to the enclosure, it is quite difficult to perform an analytical characterization because of the irregular ge-

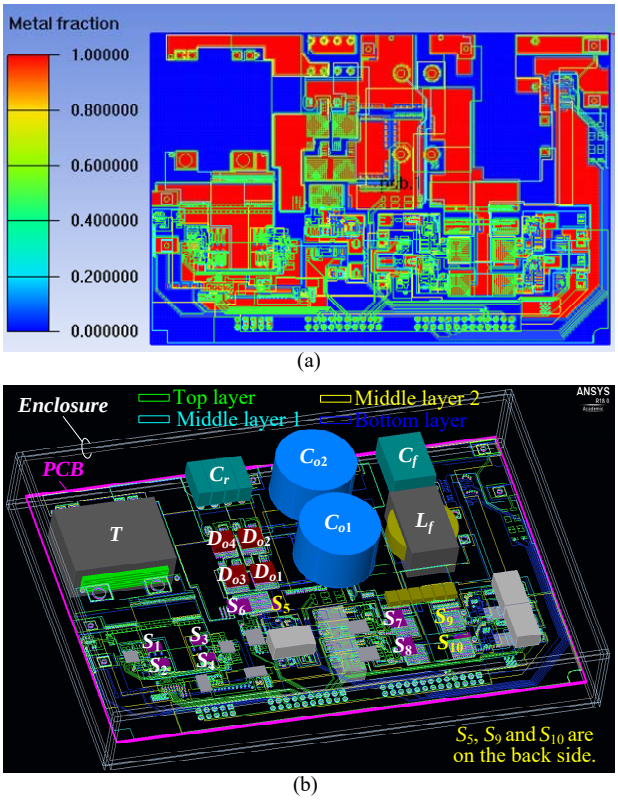

Fig. 5.6: FEM simulation model of the microinverter built in Ansys/Icepak. (a) Percentage of copper on the PCB top layer; (b) Enclosure, PCB (including traces and vias) and main components of the PV microinverter. Source: **[J4]**.

ometry of heat transfer medium. Hence, detailed structure models of all main components, enclosure, and PCB (including traces and vias) are built in ANSYS/Icepak based on real dimensions and material properties, as shown in Fig. 5.6. To extract the case-enclosure thermal impedance of eHEMTs, multiple system-level FEM simulations are conducted for the three cases of $S_7 - S_{10}$ being implemented with GS66502B, GS66504B or GS66508B, as shown in Fig. 5.7(a). Since GS66502B and GS66504B have the same package dimension, their case-enclosure thermal impedances are the same. Meanwhile, it is noticed that the Z_{ce} difference among $S_7 - S_{10}$ is negligible. Therefore, the average Z_{ce} of $S_7 - S_{10}$ is obtained to represent their case-enclosure thermal impedance, as shown in Fig. 5.7.

Then, the average Z_{ce} curves are fitted as multiorder Foster models which are further transformed into Cauer models with the method proposed in [135]. Thus, the junction-case and case-enclosure Cauer-type RC circuits can

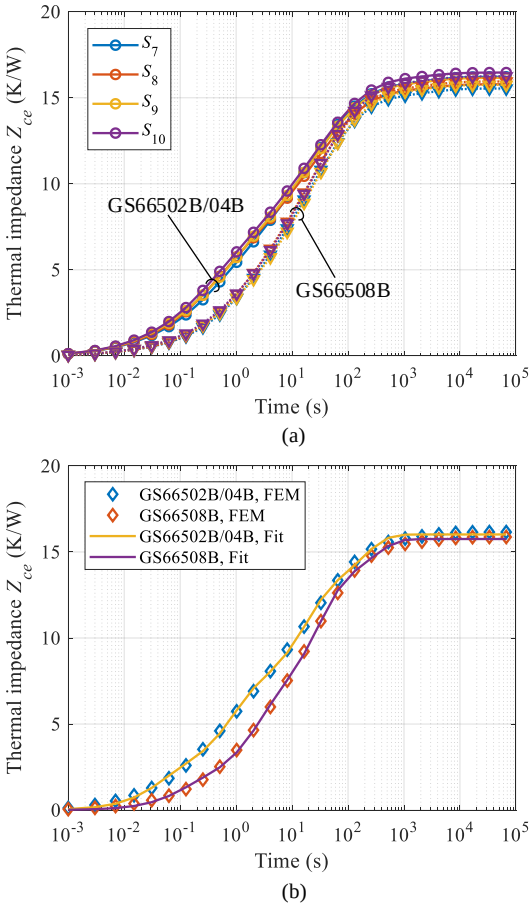

Fig. 5.7: Case-enclosure thermal impedance of $S_7 - S_{10}$ implemented with different GaN eHEMTs (GS66502B, GS66504B and GS66508B): (a) FEM simulations for $S_7 - S_{10}$, (b) fitted case-enclosure thermal impedance. Source: **[J4]**.

be connected in series, as shown in Fig. 5.8. At low and high frequencies, Z_{je} is dominated by Z_{ce} and Z_{jc}, respectively. Finally, the junction-enclosure thermal impedance curves are fitted as multiorder Foster models in order to perform a fast numerical calculation for one-year data.

Enclosure-Ambient Thermal Impedance Z_{ea}

All the three heat transfer ways, i.e., conduction, convection and radiation, are involved in the heat propagation from the enclosure to the ambient. Therefore, its heat transfer coefficient depends on both the enclosure and ambient temperatures. The aluminum enclosure has a high thermal con-

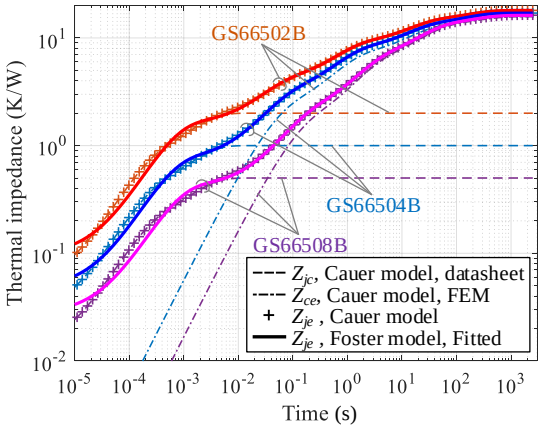

Fig. 5.8: Junction-enclosure thermal impedance of GaN eHEMTs GS66502B, GS66504B and GS66508B. Source: [**J4**].

ductivity, i.e., 205 W/(m·K), and thus, the enclosure is almost isothermal. To obtain the equivalent enclosure-ambient thermal impedance ψ_{ea} (see Fig. 5.4), multiple FEM simulations are conducted at different total power losses and ambient temperatures [**J4**]. Then, the FEM simulation results are fitted as a first-order Foster model

$$\psi_{ea} = R_{ea,eq}\left(1 - e^{-t/(R_{ea,eq}C_{ea,eq})}\right) \tag{5.6}$$

where $C_{ea,eq}$ is found to be constant as 1100 J/K but $R_{ea,eq}$ is a function of the total power loss and ambient temperature, i.e., $R_{ea,eq} = (1.742P_{l,tot}^{-0.114})(1.8 - 7.48 \times 10^{-3}T_a)$.

5.4 Modeling of Lifetime, Cost and Volume

5.4.1 Lifetime Modeling of GaN eHEMT

Failure Mechanism

DC power cycling (PC) tests [136] on the GaN eHEMT GS66508P have been conducted in [127, 137, 138] in order to obtain the degradation characteristic and lifetime model of the 650-V GaN eHEMTs with respect to thermal stresses.

Two failure phenomena of GaN eHEMTs have been observed: thermal conductivity degradation and I_{DSS} failure [127, 137, 138]. For the thermal conductivity degradation of semiconductor devices, it can be explained by the bond wire lift off and solder joint fatigue from thermo-mechanical stresses

[139]. There is no bond wire used in the GaNPX® package; therefore, the solder joint fatigue is the main failure mechanism. The solder joint fatigue of the aged samples is investigated by the scanning acoustic microscope (SAM) analysis.

The second failure mode is the drain-source leakage current I_{DSS} increase. The in-depth analysis on the I_{DSS} failure can be found in [138]. It is confirmed in [138] that the cause of the I_{DSS} failure lies in the GaN semiconductor device, instead of the DUT structure or the GaNPX® package.

Preliminary Lifetime Model

The relationship between the number of cycles to failure N_{ocf} of a GaN HEMT and the applied stresses (mean junction temperature T_{jm} and junction temperature swing ΔT_j) can be modeled by the Coffin-Manson-Arrhenius equation [140]:

$$N_{ocf} = A(\Delta T_j)^{-n} \exp\left(\frac{E_a}{k_b(T_{jm}+273)}\right) \tag{5.7}$$

where the activation energy E_a = 1.8 eV [141], k_b = 8.62 $\times$ 10^{-5} eV/K is the Boltzmann constant, and the two parameters $A = 1.92 \times 10^{11}$ and $n = 15.18$ are obtained from the DC power cycling test results in [127, 137, 138]. It should be noted that the built lifetime for the 650-V GaN eHEMTs is preliminary and needs more comprehensive experimental verifications. Nevertheless, it is used in this research to evaluate the wear-out performance of GaN eHEMTs.

As for the damage accumulation, the commonly used Miner's rule [142], which assumes that the damage accumulates linearly, is employed, i.e.,

$$D_{mg} = \sum_k \frac{N_{oc,k}}{N_{ocf,k}} \tag{5.8}$$

where $N_{ocf,k}$ is the number of cycles to failure under the specific T_{jm} and ΔT_j, and $N_{oc,k}$ is the number of cycles of the same loading stress during the period of operation time under consideration. The device fails when the damage D_{mg} is accumulated to 1.

5.4.2 Cost and Volume Modeling of GaN eHEMT and Inductor

Cost

A survey on the market price of 650-V GaN eHEMTs, 3C95 ER magnetic cores and Litz wires was conducted at Mouser Electronics™ [143], Digi-Key Electronics™ [144] and HSM Wire™ [145] in spring 2018. The minimum ordering quantities (MOQs) are 1000 pieces for the GaN transistors, 500 sets

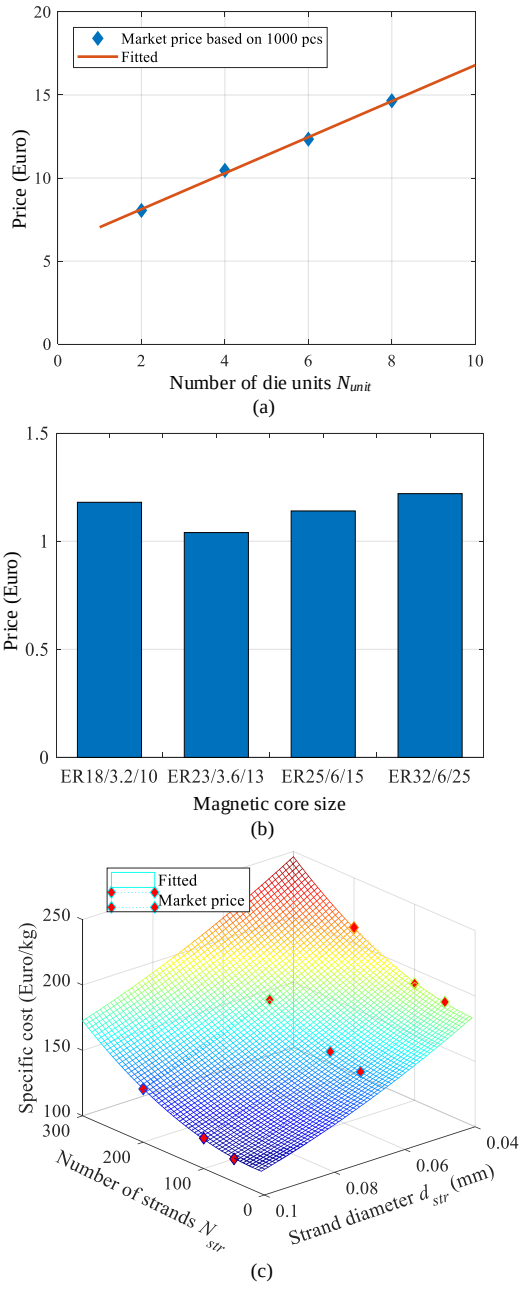

Fig. 5.9: Market prices of (a) GaN Systems 650-V GaN eHEMTs with different number of die units, (b) magnetic cores with different sizes, and (c) Litz wires with different numbers of strands N_{str} and strand diameters d_{str}. Source: **[J4]**.

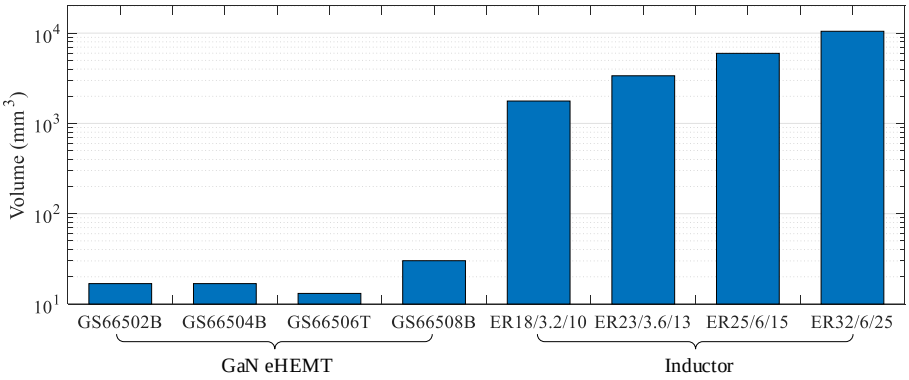

Fig. 5.10: Volume of GaN eHEMTs and inductors. Source: [**J4**].

for the magnetic cores, and 50 kg for the Litz wires. Fig. 5.9(a) shows the market price of GaN eHEMTs with different numbers of die units. As can be seen, the transistor price increases linearly with respect to the number of die units N_{unit} inside the transistor. The price of GaN Systems 650-V eHEMTs can be fitted as [146]

$$C_{ost} = C_{ost,pack} + c_{ost,unit} N_{unit} \tag{5.9}$$

where $c_{ost,unit} = 1.1$ €/unit is the specific price per die unit and $C_{ost,pack} = 6$ € is the package related price.

The prices of 3C95 ER cores from Ferroxcube™ are shown in Fig. 5.9(b). It is seen that the price increases with respect to the core size for the three big cores, ER23/3.6/13, ER25/6/15 and ER32/6/25. For ER18/3.2/10, it has the smallest size and therefore has the least material consumption. However, the small size of ER18/3.2/10 may increase the manufacturing cost. Hence, the smallest size of core, ER18/3.2/10, is not the cheapest. Nevertheless, there is no significant price difference among the four selected cores. The inductor core price only takes about $2\% - 3.8\%$ of that of four GaN eHEMTs. Therefore, the cost of the inverter stage is dominated by the GaN eHEMTs.

For the cost of Litz wire in the inductor L_f, it depends on many factors, e.g., the number of strands N_{str}, the strand diameter d_{str}, the minimum order quantity, and the market copper price [147]. Multiple quotas were made at HSM Wire™ [145] for the Litz wires with different parameters, as shown in Fig. 5.9(c). It is seen that the specific cost of Litz wire increases with respect to the increase of N_{str} and the decrease of d_{str}, and can be fitted as

$$c_{ost,Litz} = c_0 + c_{N1} N_{str} + c_{d1} d_{str} + c_{N2} N_{str}^2 + c_{Nd} N_{str} d_{str} + c_{d2} d_{str}^2 \tag{5.10}$$

where $c_0, c_{N1}, c_{d1}, c_{N2}, c_{Nd}$ and c_{d2} are fitting parameters.

Volume

The volumes of the 650-V GaN eHEMTs and ER cores are calculated based on the datasheets [123–126, 148], as shown in Fig. 5.10. The gate drive circuits are the same for different GaN eHEMTs, i.e., GS66502B/04B/06T/08B. Therefore, the only difference lies in the volumes of GaN eHEMTs. However, the largest size of GaN eHEMT, GS66508B, only accounts for 1.5% of the volume of the smallest inductor ER18/3.2/10. Therefore, the volume of the inverter stage is dominated by the inductor L_f.

5.5 Cost-Volume-Reliability Pareto Optimization of the Proposed Microinverter

5.5.1 Design Process

A cost-volume-reliability Pareto optimization scheme is proposed for the microinverter, as shown in Figs. 5.11 and 5.12. The system specifications, i.e., the dc-link voltage V_{dc}, grid voltage V_g, maximum input power $P_{PV,max}$, and real-field mission profile (solar irradiance S_I and ambient temperature T_a), are predetermined parameters. Regarding the design variables, multiple parameters can be identified, including the power P_{dzn} at which the inductor is optimized, the filter inductance L_f, the number of die units (N_{unit} represents the current rating) inside a GaN eHEMT for $S_7 - S_{10}$, the magnetic core dimension D_{core} and Litz wire gauge G_{Litz} for L_f. The first three design parameters, P_{dzn}, N_{unit}, and L_f, influence the inductor current and switching frequency, whereas D_{core} and G_{Litz} only affect the inductor design optimization. Each design parameter is a vector and its value varies within a range.

First of all, each combination of P_{dzn}, N_{unit}, and L_f is used to generate the real-time inductor current $i_L(\omega_0 t)$, over a line cycle. Together with different magnetic core dimensions D_{core} and Litz wire gauges G_{Litz}, the derived real-time current is then used to optimize the inductor design, yielding the optimal inductor parameters (i.e., the number of turns N_{turn}, the number of strands N_{str}, and the air gap l_g) for the minimum inductor power loss. Thus, a design space $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$ can be obtained and further evaluated with respect to the cost and volume characteristics.

After that, the reliability and annual energy loss of the design space $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$ are assessed, as shown on the right red block of Fig. 5.11 and Fig. 5.12. The real-field mission profile, i.e., the solar irradiance (S_I) and ambient temperature T_a directly determines the electrical and thermal loadings, and thus affects the degradation process of the components inside the PV microinverter. With a PV panel model and an MPPT control algorithm, the long-term mission profile can be translated into

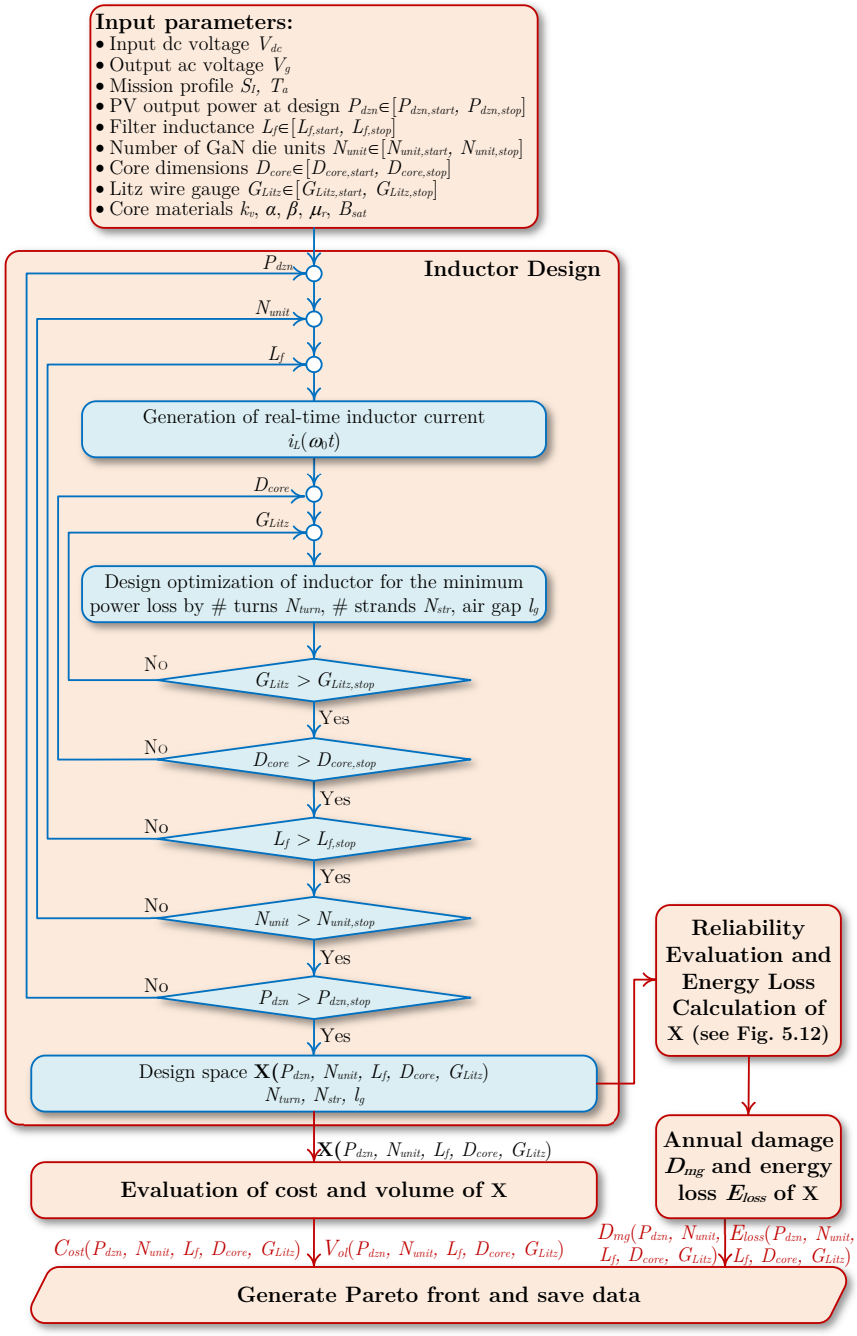

Fig. 5.11: Flowchart of the cost-volume-reliability Pareto optimization of the PV microinverter.

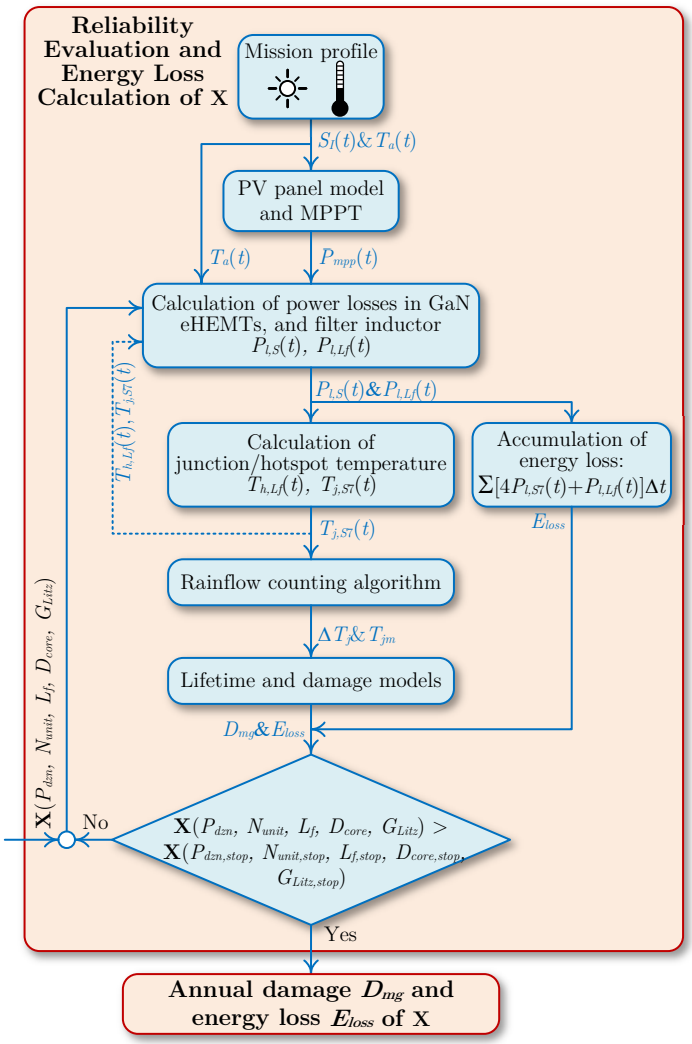

Fig. 5.12: Flowchart of reliability evaluation and energy loss calculation. Source: **[J4]**.

the real-time voltage and power at the maximum power point, $V_{PV,mpp}(t)$ and $P_{PV,mpp}(t)$, which are the input of the microinverter. Then the real-time power $P_{PV,mpp}(t)$ and ambient temperature T_a are used to calculate the power losses of the GaN eHEMTs and the inductor with the design database $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$. The built thermal impedance model is subsequently utilized to calculate the junction temperature of the GaN eHEMTs and the hotspot temperature of the inductor. Due to the interdependence of the power losses and the junction temperature, multiple iterations will be

executed in this stage. The rainflow counting algorithm [149] is employed to extract the number of temperature cycles with different characteristics (e.g., the mean junction temperature T_{jm}, and the temperature swing ΔT_j). After that, the lifetime and damage accumulation models (5.7)-(5.8) can be used to estimate the accumulated damage over a year. Meanwhile, the annual energy loss on the GaN eHEMTs and inductor can also be calculated for each design. As results, the annual damage D_{mg} and energy loss E_{loss} of the whole design database $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$ can be obtained.

Four objectives are selected for the inverter, i.e., the cost of GaN eHEMTs and inductor $\mathbf{C_{ost}}$, the inductor volume $\mathbf{V_{ol}}$, the annual damage of GaN eHEMTs $\mathbf{D_{mg}}$, and the annual energy loss of the inverter stage $\mathbf{E_{l,inv}}$. It is preferable to minimize all these objectives, $\mathbf{C_{ost}}(\mathbf{X})$, $\mathbf{V}_{ol}(\mathbf{X})$, $\mathbf{D_{mg}}(\mathbf{X})$, $\mathbf{E_{l,inv}}(\mathbf{X})$ in the design space $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$. With the multiobjective genetic algorithm [150], the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$-$\mathbf{D_{mg}}$ Pareto-optimal front can be generated, which could help designers make the trade-off among cost, volume, energy loss and reliability.

5.5.2 Cost-Volume-Reliability Pareto Optimization

As a case study, it is assumed that the PV microinverter will be operating in Arizona, US, where the solar irradiance is abundant over the whole year. Fig. 5.13(a) shows its annual solar irradiance S_I and ambient temperature T_a.

A 60-cell PV module, JinkoSolar JKM300M-60, is assumed to supply the microinverter. The dc-dc stage enables the PV module to operate at the maximum power points (MPPs) irrespective of the solar irradiance S_I and ambient temperature T_a. Based on the I-V characteristics of the PV module JinkoSolar JKM300M-60, the annual PV output power at the maximum power point P_{mpp} can be obtained, as shown in Fig. 5.13(a).

Five design variables and constraints have been identified and their ranges are as follows:

- The power on which the design is based, P_{dzn} = 50 W, 100 W, ..., 300 W;
- The number of die units inside the GaN eHEMT, N_{unit} = 2, 4, 8;
- The filter inductance, L_f = 50μH, 75μH, ..., 375μH;
- The core dimension of L_f, D_{core} = ER18/3.2/10, ER23/3.6/13, ER25/6/15, ER32/6/25;
- The Litz wire gauge of L_f, G_{Litz} = AWG38, AWG40, AWG42, AWG44, AWG46.

With the proposed multiobjective design optimization method (see Fig.5.11), a space or database containing 5040 design options can be generated. For each design, the inductor is optimized to achieve the minimum power loss by finely tuned parameters, i.e., the number of turns N_{turn}, the number of strands N_{str} and the length of air gap l_g.

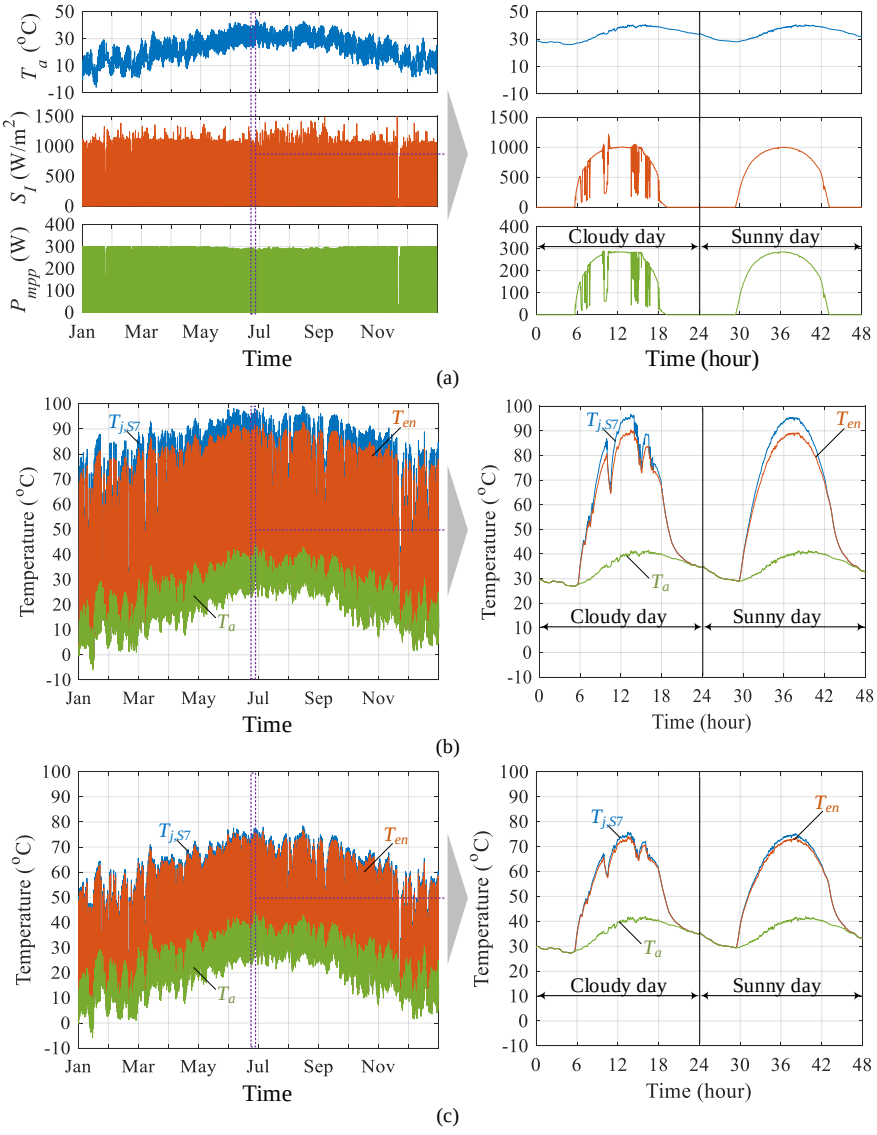

Fig. 5.13: Mission profile and calculated annual temperature profiles of the GaN eHEMT junction and the enclosure when the PV microinverter operates in Arizona, US. (a) Annual mission profile: the ambient temperature T_a, the solar irradiance S_I, and the maximum power P_{mpp} with the 60-cell PV module, JinkoSolar JKM300M-60; (b) Temperature profiles of the microinverter with design parameter set *A*: P_{dzn} = 300 W, $S_7 - S_{10}$ = GS66502B (N_{unit} = 2), L_f = 375 μH, inductor core D_{core} = ER18/3.2/10, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields N_{turn} = 173, N_{str} = 19, and l_g = 0.303 mm. (c) Temperature profiles of the microinverter with design parameter set *B*: P_{dzn} = 250 W, $S_7 - S_{10}$ = GS66508B (N_{unit} = 8), L_f = 125 μH, inductor core D_{core} = ER32/6/25, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields N_{turn} = 20, N_{str} = 481, and l_g = 0.142 mm. Source: **[J4]**.

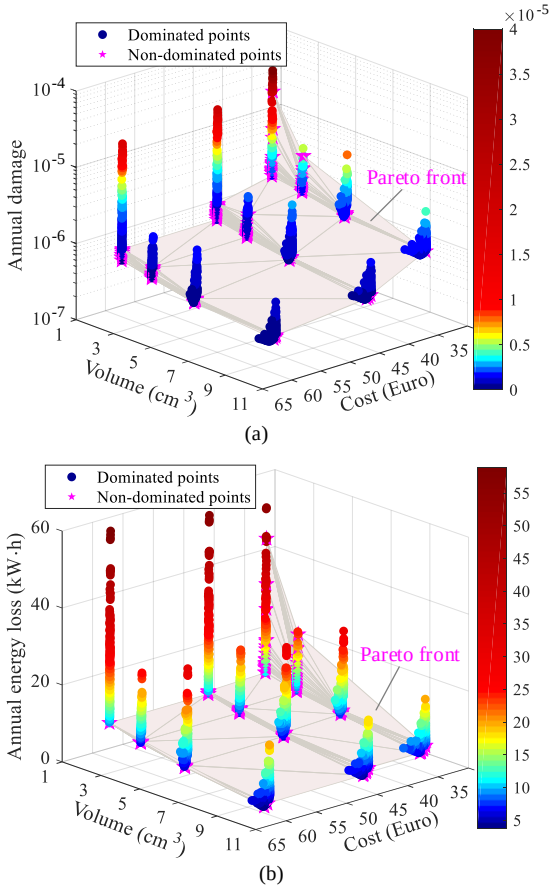

Fig. 5.14: Inverter cost, volume, annual energy loss and annual damage for each design in the space **X**: (a) $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ Pareto-optimal front; (b) $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal front. Source: [**J4**].

Figs. 5.13(b) and (c) show the junction and enclosure temperature profiles of the PV microinverter in two design cases:

Case A: P_{dzn} = 300 W, $S_7 - S_{10}$ = GS66502B (N_{unit} = 2), L_f = 375 μH, inductor core D_{core} = ER18/3.2/10, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields N_{turn} = 173, N_{str} = 19, and l_g = 0.303 mm;

Case B: P_{dzn} = 250 W, $S_7 - S_{10}$ = GS66508B (N_{unit} = 8), L_f = 125 μH, inductor core D_{core} = ER32/6/25, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields N_{turn} = 20, N_{str} = 481, and l_g = 0.142 mm.

As can be seen, the maximum junction temperature of GaN eHEMTs with *Case A* reaches 99 °C, whereas *Case B* enables the maximum $T_{j,S7}$ to fall to

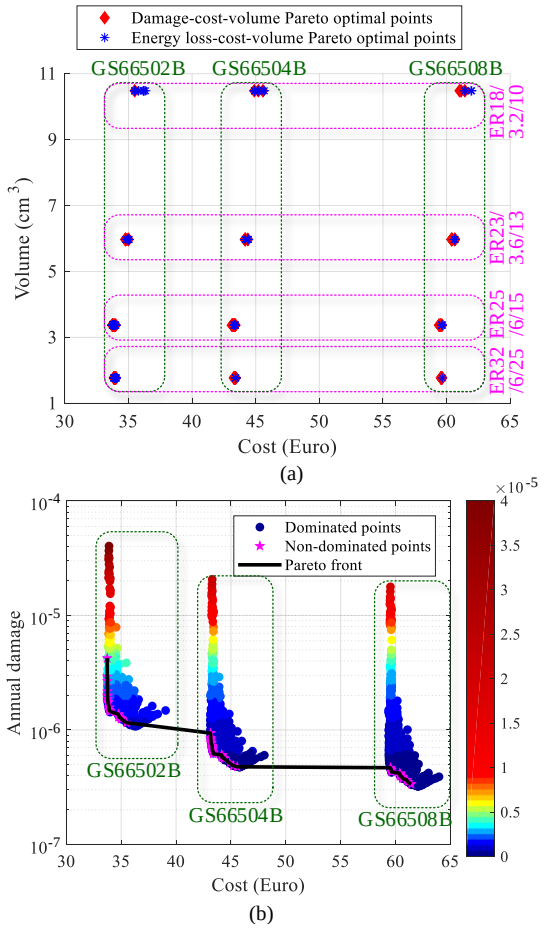

Fig. 5.15: (a) Projection of the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal points on the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$ plane; (b) $\mathbf{C_{ost}}$-$\mathbf{D_{mg}}$ Pareto-optimal front. Source: [**J4**].

78 °C. With a 21-°C decrease for the maximum junction temperature, the annual damage is reduced from 7×10^{-6} to 4×10^{-7}. A two-day mission profile and junction temperature profiles are also given in Fig. 5.13 to make a comparison between the sunny day and cloudy day. When operating on a sunny day, the temperature profiles of the microinverter are smooth due to a smooth solar irradiance. In the cloudy condition, the solar irradiance varies significantly, and thus the temperature profiles change accordingly. However, the temperature changes are not as drastic as S_1 due to the thermal capacitances of materials.

For each design in the space $\mathbf{X}$, the inverter cost, inductor volume, annual inverter energy loss, and annual damage of GaN eHEMTs are evaluated and shown in Fig. 5.14(a) and (b). Then the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-

$\mathbf{E_{l,inv}}$ Pareto-optimal fronts can be identified, as indicated in Fig. 5.14(a) and (b), respectively. The design variables have a significant impact on both the annual inverter energy loss and the annual damage of GaN eHEMTs. The Pareto-front can help to significantly reduce the annual damage and energy loss. Fig. 5.15(a) shows the projection of the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal points on the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$ plane. As can be seen, the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal points almost overlap on the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$ plane, implying that the annual damage is monotone with respect to the annual energy loss. The minimum annual damage of GaN eHEMTs and the minimal annual inverter energy loss can be simultaneously obtained. Fig. 5.15(b) shows the $\mathbf{C_{ost}}$-$\mathbf{D_{mg}}$ Pareto-optimal front of the inverter stage. It is seen that the overall cost is dominated by the employed GaN eHEMTs.

5.6 Summary

This chapter discusses the cost-volume-reliability Pareto optimization of a PV microinverter. The operation principle and characteristics of the inverter are analyzed, and the models of power loss, thermal impedance, lifetime, cost and volume are built for the main components. Finally, a cost-volume-reliability Pareto optimization method is proposed and executed, yield a Pareto front which enables a design trade-off among the three performance metrics. At a similar cost and volume, the proposed design could significantly reduce the annual damage and energy loss for the studied microinverter.

Related Publications

J4. **Y. Shen**, S. Song, H. Wang, and F. Blaabjerg, "Cost-Volume-Reliability Pareto Optimization of a Photovoltaic Microinverter," *IEEE Trans. Power Electron.*, 2018, Status: to be Submitted.

Main Contribution:
Systematic modeling of power loss, thermal impedance, lifetime, cost and volume is developed for the main components. A cost-volume-reliability Pareto optimization method is proposed and executed, which enables a design trade-off among the three performance metrics.

Chapter 6

Reliability Analysis and Improvement of a PV Microinverter Product

6.1 Abstract

This chapter assesses and improves the reliability of a PV microinverter product by applying two different mission profiles and system-level electro-thermal modeling. Instead of GaN transistors, silicon MOSFETs are used in this microinverter product. The system configuration and wear-out analysis process are described in brief before the electro-thermal and lifetime models are developed for reliability-critical components in the microinverter, e.g., semiconductor devices and capacitors. Then the mission profiles of two distinct locations, Arizona, US and Aalborg, Denmark, are applied to the developed microinverter models, yielding the annual junction/hotspot temperature profiles and annually accumulative damages of components. After that, a parameter-sensitivity analysis–Monte Carlo simulation and Weibull analysis are performed to obtain the system wear-out failure probability over time. Finally, an advanced multi-mode control scheme is introduced, and a new long-lifetime electrolytic capacitor is employed in the dc link, leading to a significant reliability improvement for the PV microinverter product.

6.2 System Description and Reliability Evaluation Process

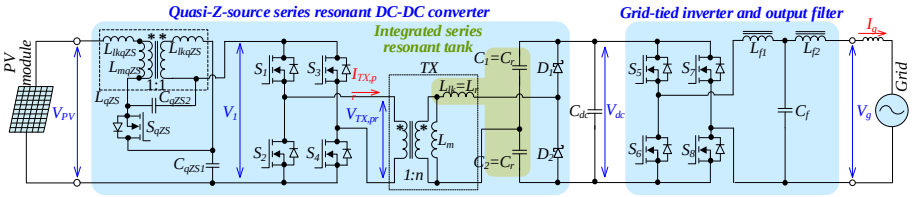

Fig. 6.1: Schematic of the impedance-source PV microinverter product. Source: **[J5]**.

Fig. 6.2: Photo of the PV microinverter product. Source: **[J5]**.

6.2.1 System Description

The topology of the PV microinverter product is shown in Fig. 6.1. As can be seen, it is composed of a synchronous quasi-Z-source series resonant DC-DC converter (qZSSRC) [151] and a grid-tied full-bridge inverter. Depending on the input voltage V_{PV}, three operation modes exist in the qZSSRC, i.e., pass-through mode(PTM), buck mode and boost mode [151]. Thus, the qZSSRC can deal with a wide range of input voltage, e.g., from 10 V to 60 V. The developed 300-W product is shown in Fig. 6.2, and its parameters are listed in Table 6.1. The full-load experimental waveforms and efficiencies of the PV microinverter prototype are shown in Fig. 6.3. As can be seen, the microinverter operates well in all the three modes, and its efficiency can be maintained relatively high over wide input voltage and power ranges.

6.2.2 Reliability Evaluation Process

It is identified in [96] that the temperature cycling is the most critical stress factor affecting the reliability of PV module-level power electronics (MLPE) **[J5]**. Therefore, this chapter takes into account the junction/hotspot temperature cycling and evaluates the wear-out failure probability of reliability-critical devices. The reliability evaluation flowchart is shown in Fig. 6.4.

A real-field mission profile, including the ambient temperature and solar irradiance, is first translated into the microinverter input, i.e., the PV output voltage at maximum power points V_{mpp} and PV output power at maximum power points P_{mpp}. Then the power loss P_l and junction/hotspot tempera-

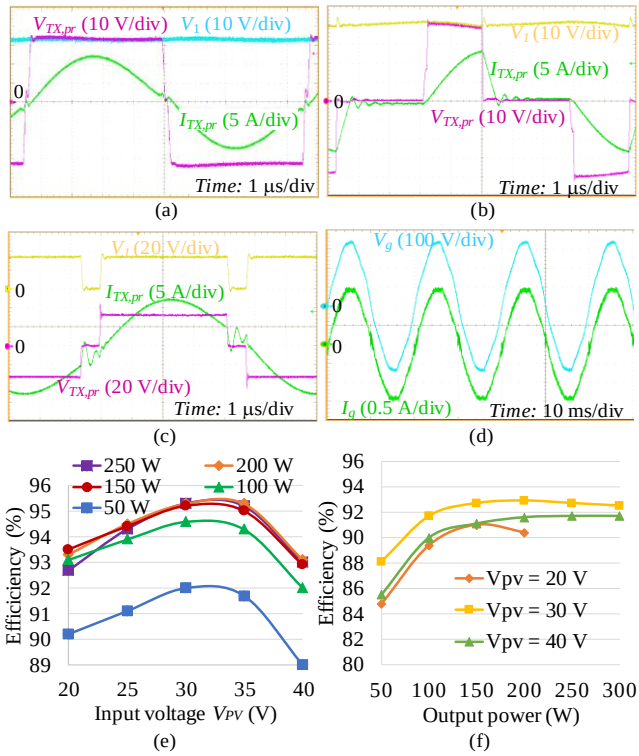

Fig. 6.3: Experimental waveforms in the (a) pass-through mode, (b) buck mode, and (c) boost mode. (d) Measured grid voltage and current waveforms. Measured efficiency curves of (e) the dc-dc stage and (f) the whole microinverter including the auxiliary power supply. Source: **[J5]**.

ture T_j can be obtained with an electro-thermal model. The rainflow counting algorithm helps to derive the number of cycles of different stresses. With the component lifetime model and damage accumulation model, the accumulative damage can be obtained subsequently. In reality, there are many variations for component and model parameters, whose effect on the lifetime distribution can be evaluated with the Monte Carlo simulation. Finally, the system wear-out failure probability can be derived with the Weibull analysis and system reliability model.

6.3 Electro-Thermal and Lifetime Modeling

6.3.1 Power Loss Modeling

The current stresses of critical components in the microinverter are measured under different PV output voltages and power levels, and thus the power

Table 6.1: Specifications and Parameters of the PV Microinverter Prototype. Source: [**J5**].

Descriptions	Parameters
Input voltage range	10-60 V
Nominal voltage	33 V
Most probable operating voltage range	20-40 V
Rated power	300 W
Switching frequency of dc-dc stage	110 kHz
Switching frequency of inverter stage	20 kHz
Switches S_{qZS}, $S_1 - S_4$	BSC035N10NS5
Switches $S_5 - S_8$	SCT2120AFC
Diodes $D_1 - D_2$	C3D02060E
Capacitors C_{qZS1} and C_{qZS2}	2.2 μF $\times$ 12, C1210C225K1R
Coupled inductor L_{qZS}	L_{mqZS}=12 μH, L_{lkqZS}=0.6 μH, custom
Resonant capacitors C_1 and C_2	10 nF // 33 nF MKP1840310104M // B32672Z6333K
DC-link capacitor C_{dc}	150 μF, 500-V electrolytic capacitor
Grid-side LCL filter: capacitor C_f	470 nF, B32653A6474K
Inductors L_{f1}	2.6 mH, custom
Inductors L_{f2}	1.8 mH, custom
Transformer TX	L_m=1 mH, L_{lk}=24 μH, n=6, custom

losses of MOSFETs, diodes, capacitors, and magnetic components can be calculated in different solar irradiances and ambient temperatures. The detailed characterization process is presented in [**J5**]. It is noted that the drain-source on-state resistance of a MOSFET, the voltage drop and on-resistance of a diode, and the equivalent series resistance (ESR) of an aluminum electrolytic capacitor are temperature dependent. Therefore, their junction/hotspot temperatures interact with their power losses. The interdependency is considered in the electro-thermal modeling. For other components, e.g., ceramic and film capacitors ($C_{qZS}, C_{r1}, C_{r2}, C_f$) and magnetic components (implemented with the 3C95 material), the dependency of their power losses on the hotspot temperatures is not significant and is therefore neglected [**J5**].

6.3.2 Thermal Modeling

The microinverter prototype is enclosed in a naturally-cooled aluminum case with a dimension of 200 mm $\times$ 150 mm $\times$ 45 mm. The enclosure is filled up with high-thermal-conductivity compound, and as a result, the thermal cross-coupling (TCC) among the main devices is pronounced and cannot be neglected. The thermal impedance network of an enclosed converter system is shown in Fig. 6.6. The thermal propagation from the junction to the ambient can be divided into two parts, i.e., from the junction to the enclosure and

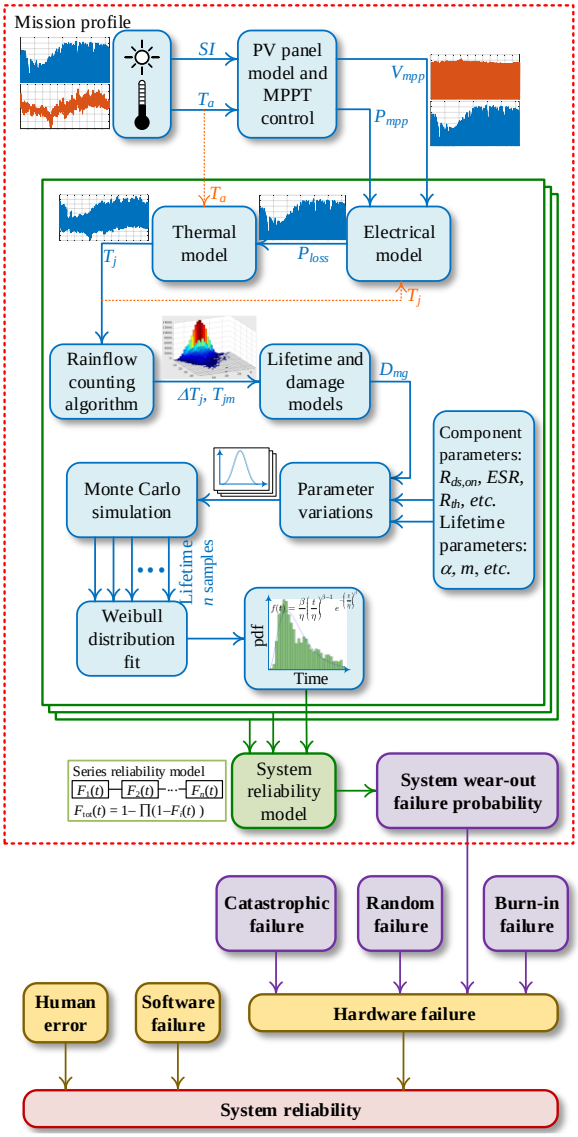

Fig. 6.4: Failure modes of power electronics systems and evaluation flowchart of the hardware wear-out failure probability. Source: [**J5**].

from the enclosure to the ambient.

Considering the PCB traces and real physical properties of components, a finite element method (FEM) structure model of the PV microinverter prototype has been built in ANSYS/Icepak, as shown in Fig. 6.5.

Enclosure-Ambient Thermal Impedance: The heat is transfered from the

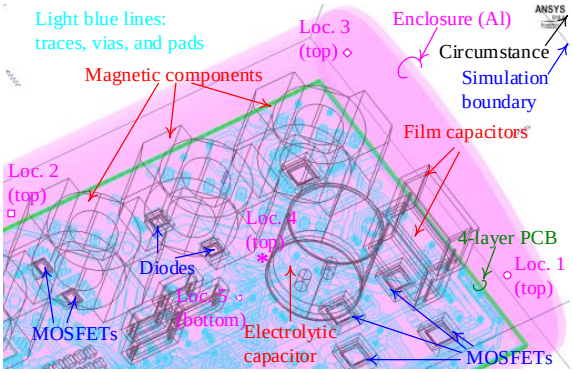

Fig. 6.5: Structure models of the main components, enclosure and PCB (including traces and vias) built in ANSYS/Icepak for FEM simulations. The PCB and the enclosure are placed horizontally. The enclosure is naturally cooled, i.e., all faces are exposed to the open air. Source: [**J5**].

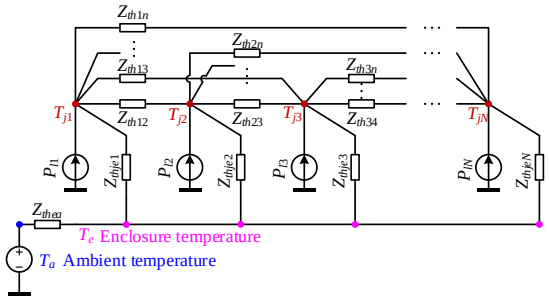

Fig. 6.6: Thermal impedance network of an enclosed converter system, including the self and mutual junction-enclosure thermal impedances. Source: [**J5**].

enclosure to the ambient by three methods, i.e., radiation, conduction, and convection. Meanwhile, the enclosure is a custom irregular cylinder, and thus, it is difficult to analytically quantify the enclosure-to-ambient thermal impedance Z_{thea} [**J5**]. Therefore, systematic FEM simulations have been conducted, and it is found that the aluminum enclosure is almost isothermal due to the filled high-thermal-conductivity compound. Based on the FEM simulations, the enclosure-ambient thermal impedance is modeled by a Foster model

$$Z_{thea} = R_{thea}(1 - \mathrm{e}^{-t/(R_{thea}C_{thea})}) \tag{6.1}$$

where C_{thea} is a constant as 2673 J/°C, but R_{thea} is determined by the total power loss P_l, i.e., $R_{thea} = 3.5P_l^{-0.216}$.

Junction-Enclosure Thermal Impedance: Conduction is the primary heat propagation approach inside the enclosed PV microinverter prototype, which

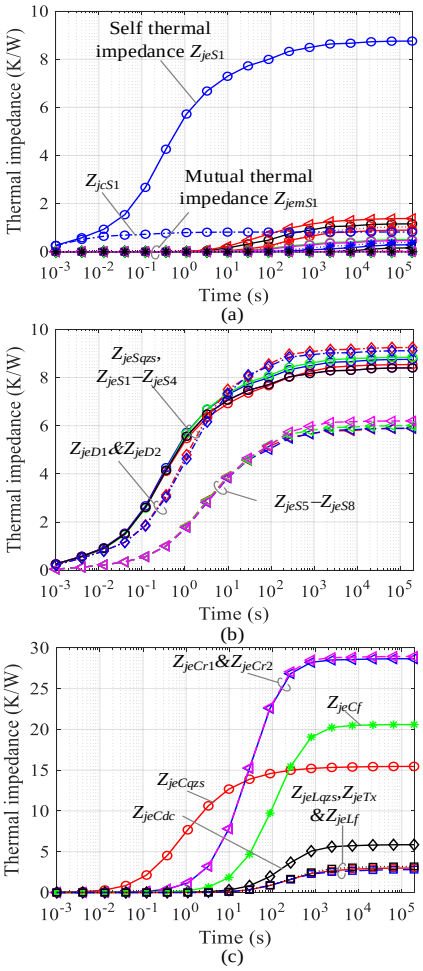

Fig. 6.7: FEM simulation results for thermal impedances. (a) Junction-case and junction-enclosure thermal impedances of S_1; mutual junction-enclosure thermal impedances between S_1 and other components. Self junction-enclosure thermal impedances of (b) semiconductor devices and (c) passive components. Source: **[J5]**.

implies that the system consisting of the enclosure, main components, and compound is linear and time-invariant. Thus, it is possible to apply the superposition principle. The junction/hotspot temperature of a device is thus

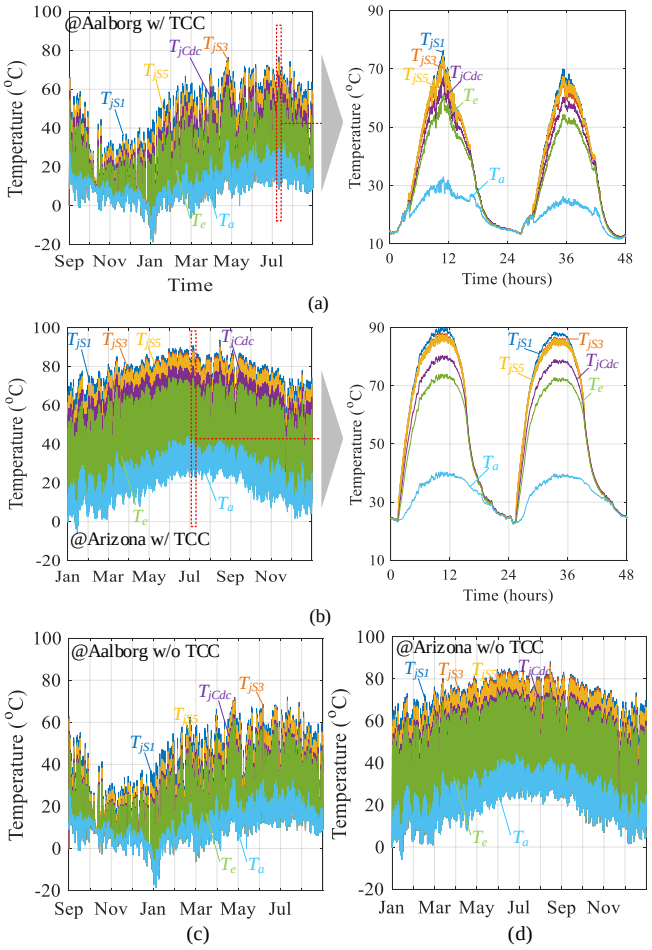

Fig. 6.8: Temperature profiles of critical components (S_1, S_3, S_5, C_{dc}) and the enclosure. (a) Aalborg, Denmark, considering the thermal cross-coupling (TCC) effect; (b) Arizona, USA, considering TCC; (c) Aalborg, Denmark, not considering TCC; (d) Arizona, USA, not considering TCC. Source: **[J5]**.

derived as

$$\begin{bmatrix} T_{j1}(t) \\ T_{j2}(t) \\ \vdots \\ T_{jN}(t) \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} Z_{je11}(t) & Z_{je12}(t) & \dots & Z_{je1N}(t) \\ Z_{je21}(t) & Z_{je22}(t) & \dots & Z_{je2N}(t) \\ \vdots & \vdots & \ddots & \vdots \\ Z_{jeN1}(t) & Z_{jeN2}(t) & \cdots & Z_{jeNN}(t) \end{bmatrix} * \begin{bmatrix} P_{l1}(t) \\ P_{l2}(t) \\ \vdots \\ P_{lN}(t) \end{bmatrix} + T_e \tag{6.2}$$

where T_{ji} is the junction/hotspot temperature of component i, Z_{jenn} represents the self junction/hotspot-to-enclosure thermal impedance, Z_{jemn} de-

notes the mutual junction/hotspot-to-enclosure thermal impedance between components m and n, T_e is the enclosure temperature, P_{ln} is the power loss of the nth component, and "*" denotes convolution [**J5**].

Multiple FEM simulations are performed to extract the elements of the thermal impedance matrix in (6.2). Fig. 6.7 shows the FEM simulation results for the self and mutual thermal impedances of S_1 and the self thermal impedances of other components. The FEM simulations for the junction-enclosure thermal impedances are then fitted as multiorder Foster thermal models, i.e.,

$$Z_{jemn} = \sum_{k=1}^{K} R_{jemn,k}(1 - e^{-t/\tau_{jemn,k}}) \tag{6.3}$$

where Z_{jemn}, R_{jemn}, and τ_{jemn} are junction-enclosure thermal impedance, resistance and time constant between components m and n [**J5**].

The junction-enclosure temperature difference, enclosure-ambient temperature difference and the junction temperature of component m can be calculated by the discrete equations [**J5**]

$$\begin{cases} \Delta T_{jem}(x+1) = \sum\limits_{n=1}^{N}\sum\limits_{k=1}^{K}\left[\begin{array}{l} \Delta T_{jemn,k}(x)e^{-t/\tau_{mn,k}} \\ \quad + P_{l,n}(x)R_{mn,k}(1 - e^{-t/\tau_{mn,k}}) \end{array}\right] \\ \Delta T_{ea}(x+1) = \Delta T_{ea}(x)e^{-t/\tau_{ea}} + P_{l,tot}(x)R_{ea}(1 - e^{-t/\tau_{ea}}) \\ T_{jm}(x+1) = \Delta T_{jem}(x+1) + \Delta T_{ea}(x+1) + T_a \end{cases} \tag{6.4}$$

where x denotes the time step, ΔT_{jem} is the junction-enclosure temperature difference, ΔT_{ea} represents the enclosure-ambient temperature difference, and T_{jm} is the junction temperature of component m.

6.3.3 Lifetime Modeling

According to the FMEA results in [98, 152], the progressive increase of the on-state resistance (wear-out) of MOSFETs is mainly caused by the growth of fatigue cracks and voids into the source metal layer [**J5**]. A 20% rise of the on-state resistance is chosen as the criteria of wear-out failure and a Coffin-Manson law based reliability model is built in [98]

$$N_f = \alpha \cdot (\Delta T_j)^{-m} \tag{6.5}$$

where N_f is the number of cycles to failure, ΔT_j is the junction temperature swing, and α and m are fitting parameters [**J5**]. A widely-used capacitor lifetime model is employed for the lifetime projection of capacitors [**J5**]

$$L_{cn} = L_{c0} \cdot 2^{\frac{T_0 - T_h}{n_1}} (V/V_0)^{-n_2} \tag{6.6}$$

in which L_{cn} is the lifetime under the thermal and electrical stress T_h and V, L_{c0} is the lifetime under the reference temperature T_0 and the nominal voltage

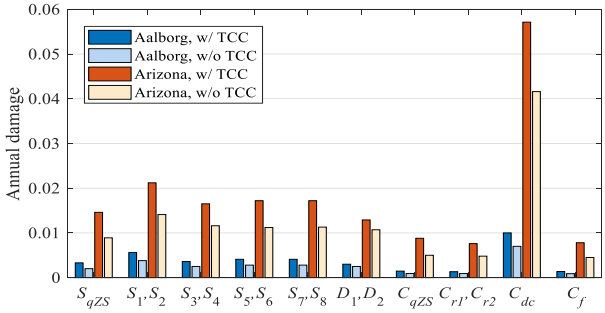

Fig. 6.9: Annual damage to each critical component in the topology of Fig. 6.1 when the microinverter operates at different locations with and without considering the TCC effect. Source: [**J5**].

V_0 [**J5**]. The coefficient n_1 is a temperature dependent constant, and n_2 is the voltage stress exponent [**J5**]. The values of n_1 and n_2 vary for different types of capacitors, and the relevant information is provided in [**J5**].

A commonly used damage accumulation model–Miner's rule [142] is employed to calculate the accumulative damage of a component. A device fails when the accumulative damage, D_{mg}, reaches 1.

6.4 Wear-Out Failure Analysis of the PV Microinverter

The mission profiles from two locations, Arizona, US and Aalborg, Denmark, are applied to the PV microinverter models, yielding the annual temperature profiles of the critical components and enclosure, as shown in Fig. 6.8. It can be seen that both the mission profile and the thermal cross-coupling (TCC) effect have a significant impact on the junction/hotspot temperatures of components [**J5**]. When operating at Arizona and Aalborg (see Fig. 6.8(a) and (b)), the highest component junction temperatures of the microinverter are 89 °C and 75 °C, respectively. If the thermal cross-coupling effect is neglected, a significant underestimation will be caused for the junction/hotspot temperatures, as shown in Fig. 6.8(c) and (d).

6.4.1 Static Annual Damage of Components

With and without considering the TCC effect, the annual damage of each critical component at the two locations is shown in Fig. 6.9 [**J5**]. It can be observed that the dc-link capacitor C_{dc} has the highest annual damage at both locations, i.e., 0.01 and 0.057 for Aalborg and Arizona, respectively [**J5**]. Assuming there are no other kinds of failures, the corresponding wear-out

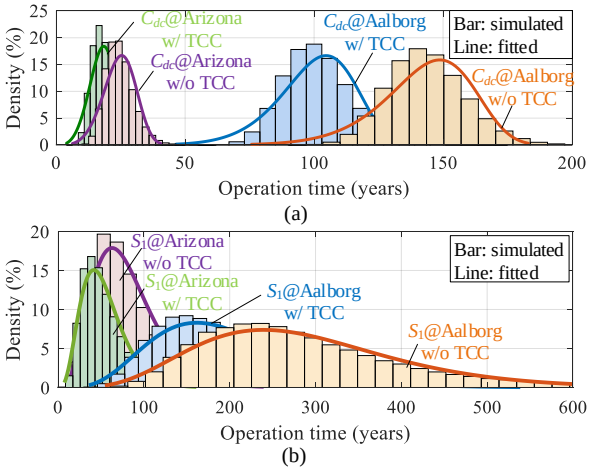

Fig. 6.10: Histograms of the years to the wear-out failure of (a) C_{dc} and (b) S_1 for a population of 1×10^5 samples operating at the two locations, with and without considering the TCC effect. Source: **[J5]**.

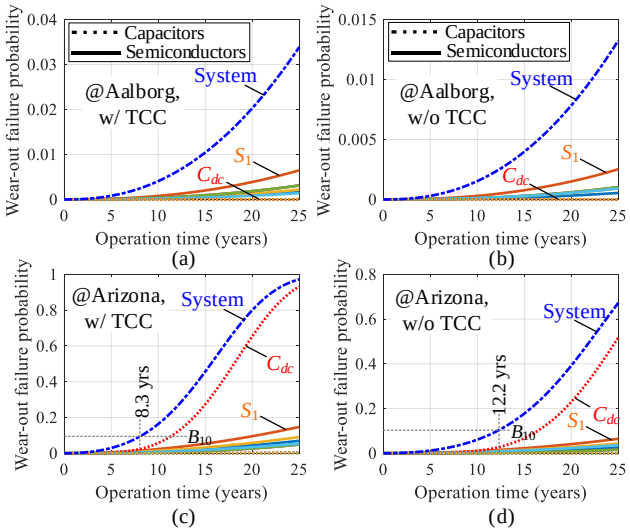

Fig. 6.11: Probability curves of wear-out failure for each component and the system when operating at (a) Aalborg, Denmark, with considering the TCC effect; (b) Aalborg, Denmark, without considering the TCC effect o; (c) Arizona, US, with considering the TCC effect; (d) Arizona, US, without considering the TCC effect. Source: **[J5]**.

lifetimes of the dc-link capacitor are 100 yrs and 17.54 yrs for the two operating locations **[J5]**. However, if the thermal cross-coupling effect is not considered, then the annual damages of C_{dc} at the two locations are 0.007

and 0.031, which results in an underestimation rate of about 30% [**J5**].

6.4.2 Monte Carlo Simulation

In the real-world operation, many uncertainties, e.g., parameter boundaries of the employed device lifetime models, parameter variations of devices, and mission profile variations, will influence the lifespan projection of the PV microinverter. Considering all the variations which presumably obey the normal distribution, a sensitive analysis–Monte Carlo simulation is conducted. The histograms of years to wear-out failure for the selected components, C_{dc} and S_5 are shown in Fig. 6.10(a) and (b), respectively.

6.4.3 System Failure Probability due to Wear Out

The histograms in Fig. 6.10(a) and (b) are fitted as the Weibull distribution [153]. Assume all the considered devices are connected in series in the reliability model, i.e., any component failure will lead to system failure [**J5**]. Then the system wear-out failure $F_{sys}(t)$ equals

$$F_{sys}(t) = 1 - \prod (1 - F_i(t)) \tag{6.7}$$

where $F_i(t)$ represents the cumulative distribution function (cdf) of wear-out failure of the ith component.

Fig. 6.11 shows the probability curves of wear-out failures for components and the system when operating at Aalborg, Denmark, and Arizona, US, with and without considering the thermal cross-coupling effect [**J5**]. First of all, it can be seen that the mission profile has a strong impact on the wear-out failure: when operating in a harsher environment, i.e., Arizona, the wear-out failure probabilities before 25-year operation are significantly higher [**J5**]. Secondly, neglecting the thermal cross-coupling effect will lead to an obvious underestimation of the wear-out failure probability; when operating at Aalborg, the predicted system wear-out failure probability before 25 years is 3.3% (see Fig. 6.11(a)), whereas the corresponding value is only 1.3% (see Fig. 6.11(b)) if neglecting the thermal cross-coupling effect [**J5**]. When operating at Arizona, the B_{10} lifetimes with and without considering the thermal cross-coupling effect are 8.3 yrs and 12.2 yrs (see Fig. 6.11(c) and (d)), respectively, which implies that about 45% lifetime overestimation can be made if neglecting the thermal cross-coupling effect [**J5**]. Also, it can be seen that the dc-link electrolytic capacitor C_{dc} has the highest wear-out failure probability when the operating environment is harsh, and thus dominates the system wear-out failure [**J5**]. Hence, it can be concluded that the dc-link electrolytic capacitor C_{dc} is the bottleneck of 25-year reliable operation for the studied PV microinverter [**J5**].

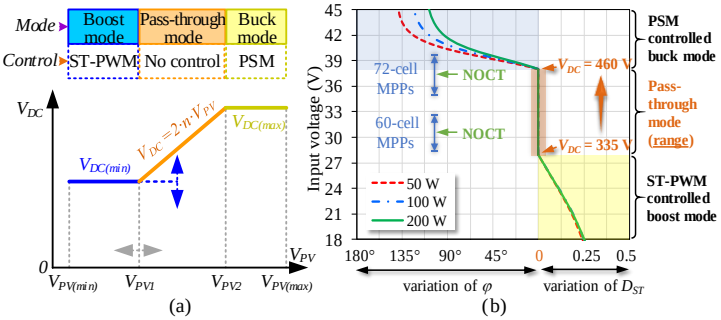

Fig. 6.12: Advanced multi-mode control of the qZSSRC with a variable dc-link voltage: (a) sketch of dc-link voltage variations; (b) regulation characteristics. Source: **[J5]**.

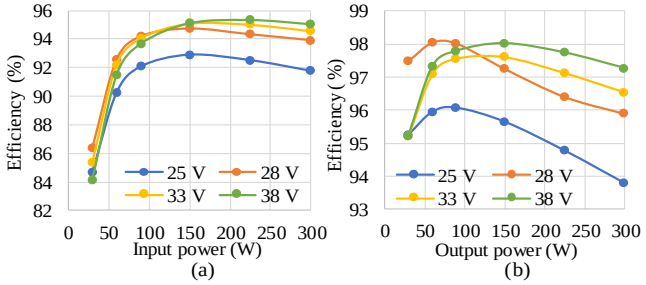

Fig. 6.13: Measured efficiency with the new control strategy: (a) the whole PV MI incl. the auxiliary power, (b) the dc-dc power stage. Source: **[J5]**.

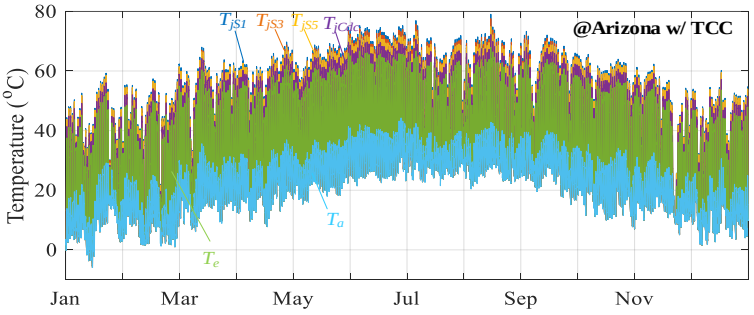

Fig. 6.14: Calculated temperature profiles of critical components (S_1, S_3, S_5, C_{dc}) and the enclosure of the PV microinverter with the new dc-link capacitor and new control scheme. The mission profile of Arizona is used and the thermal cross-coupling effect is taken into account in the temperature calculations. Source: **[J5]**.

6.5 Reliability Improvement of the PV Microinverter

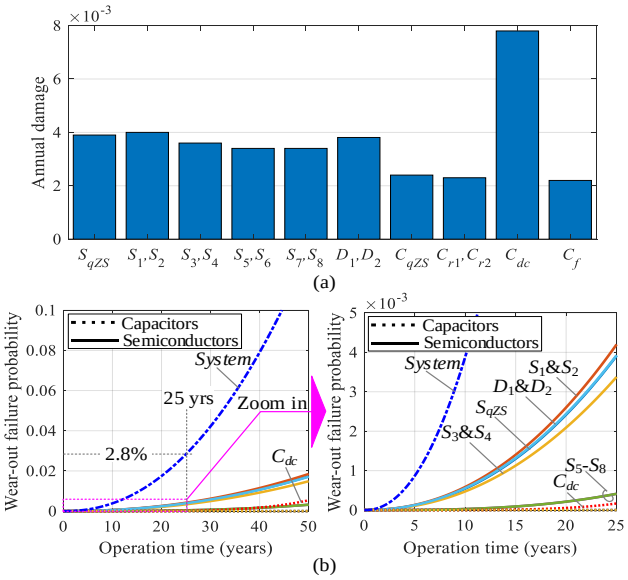

Fig. 6.15: Reliability evaluation results of the PV microinverter with the variable dc-link voltage control and the new electrolytic capacitor; the mission profile of Arizona is applied: (a) annual damage and (b) wear-out failure probabilities of each component and the system. Source: **[J5]**.

6.5.1 Advanced Multi-Mode Control of the qZSSRC

With the conventional multi-mode control scheme proposed in [151], the DC-DC converter operates in the PTM only at a particular input voltage, in which the converter has the highest efficiency, as shown in Fig. 6.3(e). However, it is not necessary for a grid-connected microinverter to have a stable dc-link voltage **[J5]**; hence, an advanced multi-mode (variable dc-link voltage) control scheme (see Fig. 6.12(a)) can be applied to the DC-DC converter, as illustrated in Fig. 6.12(b) **[J5]**. Specifically, the operation range of the PTM is $V_{in} \in [28, 38]$ V, and in this mode, the dc-link voltage varies with respect to V_{in} from 335 V to 460 V. When V_{in} is beyond the PTM range, the microinverter will operate in the buck or boost mode, and the dc-link voltage will be fixed at 460 V and 335 V, respectively. With the advanced control scheme, the efficiency performance of the microinverter can be significantly improved, as shown in Fig. 6.13. Thus, the power losses and junction/hotspot temperatures of components can be remarkably decreased.

6.5.2 New DC-Link Electrolytic Capacitor with Longer Nominal Lifetime

It has bee observed from Fig. 6.11(c) and (d) that the used dc-link electrolytic capacitor C_{dc} is the bottleneck for the long-term reliable operation of the commercial PV microinverter product. In the baseline design, the dc-link employs a cost-optimized 150-μF electrolytic capacitor, whose nominal lifetime is 5000 hours at 85 °C **[J5]**. In order to improve system reliability, this chapter proposes to replace the previous electrolytic capacitor with a new one with a longer nominal lifetime (5000 hours @105 °C) along with the advanced multi-mode control scheme.

6.5.3 Wear-Out Failure Probability

With the proposed advanced multi-mode control and the better electrolytic capacitor, the temperature profiles of S_1, S_3, S_5, C_{dc} and the enclosure are derived, as shown in Fig. 6.14. Compared with the baseline solution, the new design enables the microinverter to operate at lower temperatures (see Figs. 6.8 and 6.14). Fig. 6.15 shows the obtained annual damage and wear-out failure probability with the new design.

Because of the lower junction/hotspot temperature, the annual damages of components are reduced as well; notably, the annual damage of C_{dc} is remarkably decreased from 0.057 to 0.0078. The wear-out failure probabilities of the components and the system are shown in Fig. 6.15(b). With the new design, all the failure probabilities before 25 years are maintained low. For the system, its wear-out failure probability over 25-year operation is about 2.8%, which is significantly enhanced compared with the baseline solution (see Fig. 6.9(c)) **[J5]**.

6.6 Summary

This chapter presents a wear-out failure analysis and reliability improvement of a 300-W impedance-source PV microinverter product. A description on the product configuration and reliability evaluation process is first presented. With experimental measurements and FEM simulations, a system-level electro-thermal model and empirical lifetime models are then built for the components and enclosure of the PV microinverter. After that, the wear-out performance of the microinverter is evaluated before measures are taken to improve its reliability. It is concluded that 1) both the mission profile and thermal cross-coupling effect have a remarkable impact on the lifetime projection of the PV microinverter; 2) the dc-link capacitor is the weakest link in the product in terms of the wear-out performance; 3) the proposed variable dc-link voltage control and long-lifetime aluminum electrolytic capacitor can

significantly reduce the system wear-out failure probability.

Related Publications

J5. **Y. Shen**, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out Failure Analysis of an Impedance-Source PV Microinverter Based on System-Level Electro-Thermal Modeling," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1-14, 2018, Early Access.

Main Contribution:
A system-level electro-thermal modeling-based wear-out failure analysis and reliability improvement measures are proposed and detailed for a commercial PV microinverter product.

Chapter 7

Conclusion

This chapter summarizes the results and outcomes of the research during the PhD project - *Reliability-Oriented Design and Optimization of Photovoltaic Microinverters*. The main contributions are highlighted, and the research perspectives are discussed at the end of the chapter.

7.1 Summary

The main focus of this PhD project is on the reliability-oriented design and optimization of PV microinverters. Several challenges with PV microinverters have been discussed, and different solutions have been proposed in order to address those issues. A brief summary of this PhD thesis is presented as follows.

In *Chapter 1*, the background and state-of-the-art of microinverter topology, electro-thermal modeling of components, system-level reliability evaluation and multiobjective design optimization of power electronic converters are discussed. Thus, the motivations of this PhD research are summarized, and four research objectives are outlined: 1) development of high-efficiency wide-voltage-gain DC-DC converter topologies suitable for PV microinverters; 2) proposal of new methods for the electro-thermal modeling and design optimization of components and microinverter systems; 3) proposal and execution of a cost-volume-reliability Pareto optimization method for a PV microinverter; 4) demonstration of a reliability-oriented design method for a commercial PV microinverter product.

Chapter 2 firstly discusses a dual-mode rectifier based series resonant DC-DC converter for PV microinverter applications. The operation principle, modulation scheme, control strategy and key characteristics (i.e., voltage gain, RMS current and soft-switching) are detailed. A 1-MHz 250-W microinverter prototype has been built and tested to verify the theoretical analysis. It

turns out that the proposed DC-DC converter with a variable DC-link voltage control can maintain high efficiencies over a wide input voltage range (17 V - 43 V). Therefore, it is a good candidate for the DC-DC stage of two-stage PV microinverters. Additionally, a new structure-reconfigurable series resonant DC-DC converter is also discussed for the PV microinverter systems which require a configurable output voltage as well as a wide range of input voltage.

In order to optimize the thermal design in high-power-density power electronic converters, *Chapter 3* develops analytical thermal models for PCB vias and pads. The thermal resistance model of PCB via arrays is built and analyzed concerning multiple design variables. Then, an optimal trajectory is identified for the via design. FEM simulations and experimental tests show that the optimal trajectory helps to reduce the thermal resistance of vias. In the case of the power semiconductor devices cooled by a copper pad, an axisymmetric thermal model is developed, and an algorithm is proposed to fast size the copper pad under the junction temperature limit. Finally, experimental measurements verify the built thermal model and algorithm. *Chapter 4* presents the parameter characterization and electro-thermal modeling of a series of 650-V GaN eHEMTs. The key characteristics of a GaN eHEMT, i.e., the drain-source on-state resistance, parasitic capacitance, transconductance, and junction-case thermal impedance, are modeled as functions of the number of standard GaN die units inside. Due to the low parasitic capacitance of GaN eHEMTs, fast turn-off is easy to achieve and therefore, the turn-off loss can be approximated by the energy stored in the parasitic output capacitance.

Chapter 5 discusses a cost-volume-reliability Pareto optimization method for a PV microinverter. The operation principle and characteristics of the inverter-stage are analyzed before the systematic modeling of key performance metrics i.e., the power loss, thermal impedance, lifetime, cost, and volume. The cost-volume-reliability Pareto optimization is performed for the inverter, yielding a Pareto front which enables a design trade-off among cost, volume and reliability.

Finally, *Chapter 6* demonstrates a reliability-oriented design method for a PV microinverter product. The microinverter product and the reliability evaluation process are first described in brief. Then, system-level electro-thermal modeling and wear-out failure analysis are performed. It is found that both the mission profile and thermal cross-coupling effect have a significant impact on the reliability evaluation of the PV microinverter. Moreover, the DC-link capacitor in the baseline design is the weakest component concerning the wear-out failure. In order to improve the system-level reliability, a new variable DC-link voltage control is proposed and the DC-link capacitor is replaced with a better one, leading to a remarkable reliability improvement.

7.2 Main Contributions

The main contributions of this PhD project are summarized as follows:

A) High-Efficiency Wide-Voltage-Gain DC-DC Converters for PV Microinverters

- A new series resonant DC-DC converter with a dual-model rectifier is proposed for PV microinverter applications;
- The characteristics analysis and design optimization are conducted for the proposed converter;
- A 1-MHz microinverter prototype has been built and tested for verifications;
- A structure-reconfigurable DC-DC converter is proposed, analyzed, and implemented to suit for the grid-connected PV systems with a wide-input voltage range and different grid voltage levels, 110/120 V and 220/230/240 V.

B) Electro-Thermal Modeling of Components

- An analytical thermal resistance model and an optimal design trajectory are proposed for PCB vias;
- An analytical thermal resistance model and an algorithm are proposed for sizing PCB pads;
- Characterization of key parameters and modeling of electro-thermal performance are conducted for a series of 650-V GaN eHEMTs.

C) Cost-Volume-Reliability Pareto Optimization of a PV Microinverter

- System-level electro-thermal modeling is conducted for a PV microinverter;
- A cost-volume-reliability Pareto optimization method is proposed and executed for the inverter stage of the PV microinverter.

D) Reliability-Oriented Design of PV Microinverters

- System-level electro-thermal modeling considering the thermal cross-coupling effect is performed for an impedance-source PV microinverter product;
- A system-level reliability evaluation process is proposed and implemented for the PV microinverter product;
- Reliability-oriented design measures are proposed and applied to reduce the system-level wear-out failure of the microinverter product.

7.3 Research Limitations and Perspectives

Although several aspects for the reliability-oriented design optimization of PV microinverter have been investigated in this PhD project, there are still other challenges which need to be addressed:

- The proposed cost-volume-reliability Pareto optimization method has been executed in this PhD project, yielding a Pareto front. However, there is still a lack of experimental verification. Therefore, several prototypes with different (Pareto-optimal and non-optimal) designs will be tested to verify the performance metrics, i.e., cost, volume, efficiency, and operating temperature.
- This PhD research focuses on the reliability of two-stage PV microinverters. However, there are also single-stage and pseudo-DC-link microinverters whose overall performance may be better than the two-stage ones. A comprehensive performance benchmark of these architectures could be interesting to both the industry and academia.
- Empirical device lifetime models are employed to evaluate the damage accumulation over time. However, those models are derived by accelerated lifetime tests where the operating conditions may be different from those of the studied PV microinverters. These discrepancies may lead to errors for the calculated damage. Therefore, it would be useful to conduct more diverse life cycle tests such that the lifetime models of devices could be applicable to different industrial cases.
- There are many failure modes for a PV microinverter, e.g., the software failure, random failure, catastrophic failure, burn-in failure, and hardware wear-out failure. However, this research mainly focuses on the wear-out failure of main components (i.e., semiconductor devices and capacitor). In addition, other critical components (e.g., solder, connectors and varistor) are also not taken into account in the reliability analysis. Thus, the reliability of the PV microinverters may be overestimated. A more comprehensive and accurate reliability evaluation could be conducted by considering those failure modes and critical components.
- The open-air temperature of a location is used as the ambient temperature of PV microinverters. In the real field, however, the ambient temperature of a PV microinverter may be much higher depending on the installation condition and surrounding ventilation. Nevertheless, its impact may be compensated by disregarding the degradation of a PV panel due to less power. It would be interesting to investigate the impacts of both the installation condition and module degradation on the reliability of a PV microinverter.

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Part II

Papers

Paper A

A 1-MHz Series Resonant DC-DC Converter With a Dual-Mode Rectifier for PV Microinverters

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ABSTRACT

The photovoltaic (PV) output voltage varies over a wide range depending on operating conditions. Thus, the PV-connected converters should be capable of handling a wide input voltage range while maintaining high efficiencies. This paper proposes a new series resonant dc-dc converter for PV microinverter applications. Compared with the conventional series resonant converter (SRC), a dual-mode rectifier (DMR) is configured on the secondary side, which enables a twofold voltage gain range for the proposed converter with a fixed-frequency phase-shift modulation scheme. The zero-voltage switching (ZVS) turn-on and zero-current switching (ZCS) turn-off can be achieved for active switches and diodes, thereby minimizing the switching losses. Moreover, a variable dc-link voltage control scheme is introduced to the proposed converter, leading to a further efficiency improvement and input-voltage-range extension. The operation principle and essential characteristics (e.g., voltage gain, soft-switching, and root-mean-square current) of the proposed converter are detailed in this paper, and the power loss modeling and design optimization of components are also presented. A 1-MHz 250-W converter prototype with an input voltage range of 17 V – 43 V is built and tested to verify the feasibility of the proposed converter.

***Index terms*—** Series resonant dc-dc converter, wide input voltage range, 1-MHz switching frequency, photovoltaic microinverter

I. INTRODUCTION

Compared with central and string photovoltaic (PV) inverters, microinverters are favorable in low-power applications, due to the capability of module-level maximum power point tracking (MPPT), low installation efforts, easy monitoring and failure detection, and low maintenance cost [1]-[3]. Nevertheless, certain challenges remain for PV microinverters: 1) the efficiency performance of microinverters is relatively low compared with string inverters (e.g., peak efficiency is around 99.2 % [4]); 2) there is a trend that microinverters will be incorporated into PV modules in the future [5], [6], which implies that microinverters should be more compact (i.e., high power density and low profile); 3) panel-embedded microinverters may be inevitably heated up by the PV panels, accelerating the degradation [7], [8]. Improving the power conversion efficiency and reducing power losses can be an effective way to enhance the energy yield and reliability of PV microinverters [3], [9].

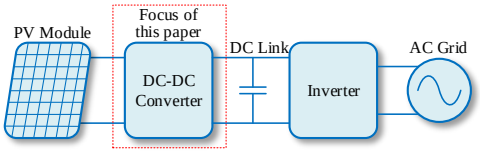

Fig. 1. Configuration of a two-stage grid-connected PV microinverter system.

In the literature, three power conversion structures can be found for PV microinverters, i.e., the high-frequency-link (single-stage) microinverter [10], pseudo-dc-link microinverter [11], and dc-link (two-stage) microinverter [12], [13]. The dc-link microinverters have the advantages of simpler structure, lower power decoupling capacitance, and easier performance optimization for each stage; therefore, recently, they attracted much interest [6], [9], [12]-[16]. Fig. 1 shows the configuration of a two-stage grid-connected PV microinverter system. Typically, the front-end dc-dc converter is controlled to achieve the MPPT of the PV module. Depending on the module characteristics and the operating conditions (i.e., the solar irradiance and ambient temperature), the output voltages of PV modules at maximum power points vary over a wide range (e.g., 20-40 V). Therefore, the dc-dc converter should be able to handle a wide input voltage range while maintaining high efficiencies. It is also required that the dc-dc converter should boost the low-voltage (< 50 V [6]) PV module output to a desired high voltage (at the dc link) in order to feed a grid-connected or standalone inverter [17]. Preferably, a high-frequency transformer is inserted into the front-end dc-dc stage to achieve the galvanic isolation, leakage current elimination, and a high voltage-boost ratio [13]. Furthermore, in order to reduce the system profile, it is required to increase the switching frequency and/or adopt low-profile passive components (e.g., planar magnetics [18] and low-profile decoupling capacitors [19]).

Traditional flyback converters with snubbers or active clamping circuits are simple in topology and low in cost; therefore they are adopted as the front-end dc-dc stage in some microinverters [20], [21]. However, the voltage stress of the primary switches is high and thus low-voltage MOSFETs with low on-state resistances cannot be used [22], [23]. In the phase-shift full-bridge dc-dc

converter, the primary switches can achieve zero-voltage-switching (ZVS); however, it is challenged when operating in a wide voltage gain range, e.g., the narrow ZVS range for the lagging leg switches, duty cycle loss, large circulating current, and voltage spikes across the output diodes [24].

The LLC resonant converter is a promising topology in terms of high efficiency and high power density [24]-[27]. However, the primary concern for this topology is that the voltage gain range is not wide and thus hybrid control schemes [28]-[30] have to be applied, which increases the realization complexity of the MPPT. For instance, a full-bridge LLC resonant converter is designed for PV applications in [28]; however, the burst mode control has to be used in addition to the variable frequency control. In [29], a hybrid control combining the pulse-frequency modulation (PFM) and phase-shift pulse-width modulation (PS-PWM) is employed to a full-bridge LLC resonant converter to improve the efficiency, but the control complexity is significantly increased as well.

In addition to the hybrid control schemes, many modified LLC resonant converter topologies have been proposed [17], [31]-[41]. Structural modifications can be made to the primary-side inverter [31]-[35], the secondary-side rectifier [36]-[38], and the transformer/resonant tank [39]-[41]. Instead of the conventional half-bridge or full-bridge structure, a variable frequency multiplier is applied to the LLC resonant tank to extend the voltage gain range while maintaining high efficiencies [32]. In [33], the primary-side full-bridge inverter is replaced by a dual-bridge inverter; thus, a multi-level ac voltage can be applied to the resonant tank, and a twofold voltage gain range can be achieved; however, the primary-side switches have high turn-off currents, and may suffer from high off-switching losses when operating in high step-up applications (e.g., PV microinverters). By combining a boost converter with an LLC resonant converter, two current-fed LLC resonant converters are proposed in [34], [35]. Nevertheless, the primary-side switches share uneven current stresses, which may lead to high conduction losses as well as high off-switching losses. To avoid the high off-switching losses on the high-current primary-side switches, [36]-[38] propose secondary-rectifier-modified LLC resonant converter topologies. Specifically, in [36] and [37], two diodes in the full-bridge rectifier are replaced with two active switches, yielding a controllable rectifier. In [38], two active switches are utilized to obtain a reconfigurable voltage multiplier rectifier, leading to a squeezed switching frequency range and improved efficiencies over a wide input voltage range; notably, the number of rectifier components is high (8 diodes + 2 active switches + 6 capacitors), and thus this topology may not be cost-effective for PV microinverter applications. Furthermore, [39]-[41] modify the transformer and resonant tank to extend the voltage gain range of the LLC resonant converter. In [39], an auxiliary transformer, a bidirectional switch (implemented with two MOSFETs in an anti-series connection), and an extra full-bridge rectifier are added to the conventional LLC resonant converter. Thus, the equivalent transformer turns ratio and magnetizing inductance can be adaptively changed in order to achieve a wide voltage gain range; however, the component count is high and the transformers utilization ratio is relatively low. To address the issues in [39] as well as to maintain high efficiencies over a wide input voltage range, *Sun et al* [41] proposes a new LLC resonant converter with two split resonant branches; in this way, two operation modes, i.e., the low- and medium-gain modes, are enabled, and the gain range

for mode transition is 1.5 times, leading to a smoother efficiency curve over the gain range. Furthermore, in [40], a new transformer plus rectifier structure with fractional and reconfigurable effective turns ratios is proposed for a widely varying voltage gain.

As aforementioned, there is a trend to increase the switching frequency and lower the converter profile such that the microinverter can be mechanically and physically integrated with a PV module [5], [6]. Therefore, the MHz operation and design optimization of resonant dc-dc converters [42]-[48] are becoming attractive to achieve so. Notably, the reported peak efficiency of a 1-MHz LLC resonant converter has reached 97.6 % with an optimal design of the integrated planar matrix transformer [46]. However, the voltage conversion ratios in these systems are fixed [43]-[48] or vary within a narrow range (± 5%) [42], which is not suitable for PV microinverter applications where the dc-dc stage should handle a wide voltage gain range.

In light of the above, this paper proposes a new dual-mode rectifier (DMR) based series resonant dc-dc converter for PV microinverter systems. A twofold voltage gain range can be achieved with a fixed-frequency phase-shift modulation scheme. The active switches can turn on under zero-voltage switching (ZVS) and the rectifier diodes can turn off under zero-current switching (ZCS), leading to minimized switching losses. Also, a variable dc-link voltage control is applied, yielding a significant efficiency improvement and input-voltage-range extension. The experimental tests on a 1-MHz microinverter prototype show that the proposed converter can achieve high efficiencies over a wide input voltage range, i.e., 17 V – 43 V.

This paper is an expansion of our previous conference publication in [49] by adding two topology derivatives, detailed characteristics analysis, power loss modeling and design optimization of components, and 1-MHz experimental verifications. The contributions of this paper are summarized as: i) three DMR-based series resonant dc-dc converter topologies are proposed for PV microinverter systems; ii) the operation principle, critical characteristics (including voltage gain, root-mean-square current, and soft switching), and design optimization of the basic DMR series resonant converter are analyzed in detail; iii) a variable dc-link voltage control is introduced to the proposed converter; iv) a 1-MHz microinverter prototype is built and tested to verify the feasibility of the proposed converter.

The remainder of this paper is organized as follows. Section II presents the operation principles of the proposed converter. In Section III, the key operating characteristics are analyzed and parameter design guidelines are presented. Then, the power loss modeling and design optimization of main components are performed in Section IV. After that, the control strategy, modulation implementation and extensive experimental tests are provided in Section V. Finally, conclusions are drawn in Section VI.

II. Operation Principles of the Proposed Converter

A. Topology Description and Operation Modes

The proposed DMR-based series resonant converter (DMR-SRC) is shown in Fig. 2. The DMR is implemented by adding a pair of anti-series transistors (S_5-S_6) between the midpoints of the diode leg (D_3-D_4) and the output capacitor leg (C_{o1} and C_{o2}). Thus,

two rectifier modes can be achieved by controlling the anti-series transistors S_5-S_6:

1) Half-Bridge Rectifier (HBR) mode: when the anti-series transistors S_5-S_6 are triggered on, a half-bridge rectifier (voltage doubler) consisting of D_1, D_2, S_5, S_6, C_{o1} and C_{o2} presents on the secondary side;

2) Full-Bridge Rectifier (FBR) mode: when S_5-S_6 are disabled, there is a full-bridge rectifier (D_1-D_4) on the secondary side.

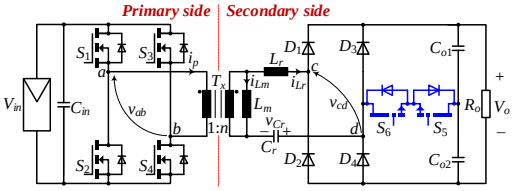

Fig. 2. Schematic of the proposed dual-mode rectifier based series resonant dc-dc converter.

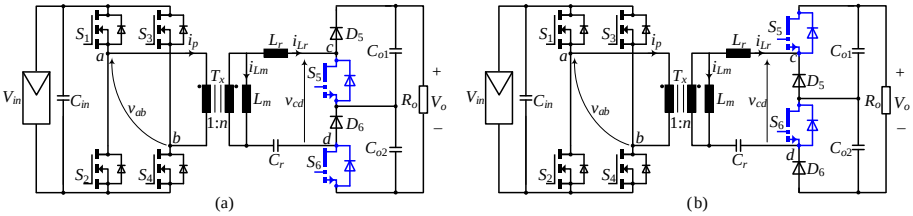

Fig. 3. Schematics of the extended series resonant converter topologies with dual-mode rectifiers for high-voltage output applications: (a) the extended topology *A* and (b) the extended topology *B*.

Inspired by the dual-mode rectification concept, two extended series resonant dc-dc converters are derived for high-voltage output applications, as shown in Fig. 3. All the secondary diodes and transistors only need to withstand half of the output voltage V_o. By controlling the secondary-side active switches S_5 and S_6, a dual-mode rectifier can be formed on the secondary side, and therefore a wide voltage gain can be achieved. Nevertheless, this paper will only focus on the basic topology shown in Fig. 2.

A fixed-frequency phase-shift modulation is applied to the proposed DMR-SRC, as illustrated in Fig. 4. The primary-side diagonal switches are driven synchronously, and the upper and lower switches of each leg are phase-shifted by π. On the secondary side, the turn-on instant of S_5 is synchronized with that of S_2 and S_3, but the turn-off of S_5 is lagged by a phase of ϕ with respect to that of S_2 and S_3. The gate signal of S_6 is shifted by a phase of π with that of S_5. It is noted that the fixed-frequency phase-shift modulation scheme is also applicable to the two extended topologies shown in Fig. 3(a) and (b).

With this modulation scheme, the voltage across the midpoints of the two primary-side switch legs, i.e., v_{ab}, is an ac square wave (with an amplitude of V_{in}) which applies to the transformer. In addition, the switching frequency f_s is equal to the series resonant frequency of the resonant inductor L_r and capacitor C_r, i.e., $f_s = f_r = 1/(2\pi\sqrt{L_r C_r})$.

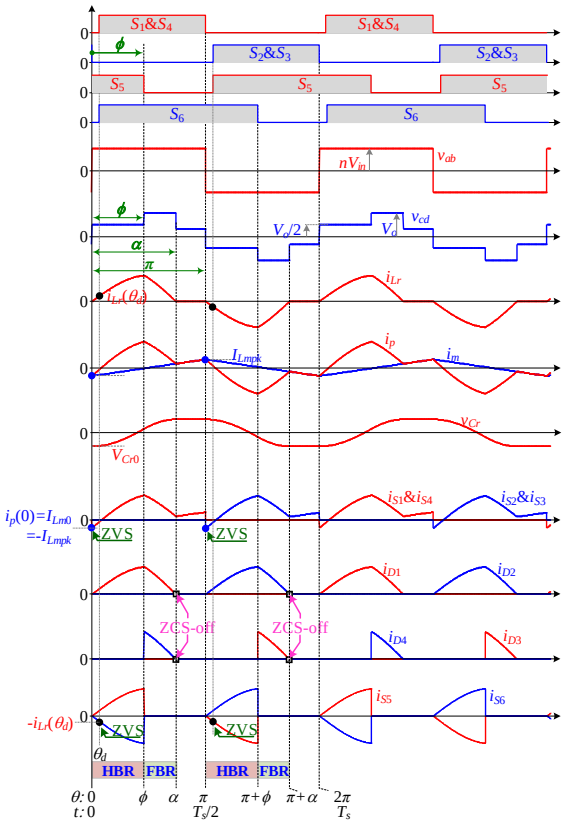

Fig. 4. Fixed-frequency phase-shift modulation for the proposed converter shown in Fig. 2 and key operating waveforms.

The primary-side transformer current i_p is the sum of the magnetizing current i_{Lm} and the resonant current i_{Lr} referred to the primary side, i.e.,

$$i_p = n(i_{Lm} + i_{Lr}) \tag{1}$$

where n represents the transformer turns ratio.

The waveform of capacitor voltage v_{Cr} has half-wave symmetry, i.e., $v_{Cr}(t) = -v_{Cr}(t + T_s / 2)$. Thus, the charge variation of the resonant capacitor over half a switching cycle [0, T_s/2] can be obtained as

$$\begin{aligned} q_{hs} &= [v_{Cr}(T_s / 2) - v_{Cr}(0)]C_r = -2V_{Cr0}C_r \\ &= \int_0^{T_s/2} i_{Lr}(t)\mathrm{d}t = \int_0^{T_s/2} \frac{i_p(t)}{n}\mathrm{d}t - \int_0^{T_s/2} i_{Lm}(t)\mathrm{d}t = \int_0^{T_s/2} \frac{i_p(t)}{n}\mathrm{d}t = \frac{T_s}{2nV_{in}} \frac{2}{T_s} \int_0^{T_s/2} [V_{in} i_p(t)]\mathrm{d}t = \frac{P}{2nf_r V_{in}} \end{aligned} \tag{2}$$

where V_{Cr0} denotes the initial resonant capacitor voltage at t = 0 (see Fig. 4), and P is the transferred power.

The voltage gain of the converter and the inductors ratio of L_m to L_r are defined as $G = V_o/(nV_{in})$, and $m = L_m / L_r$, respectively.

The quality factor is denoted as $Q = Z_r/R_o = P/(V_o^2/Z_r)$, in which the characteristic impedance $Z_r = \sqrt{L_r / C_r}$. Thus the quality factor Q is also termed as the normalized power.

The initial capacitor voltage V_{Cr0} can be obtained from (2) as

$$V_{Cr0} = \frac{P}{4nf_r C_r V_{in}} = -\frac{\pi G Q V_o}{2} \tag{3}$$

The magnetizing current i_{Lm} can be expressed as

$$i_{Lm}(\theta) = I_{Lm0} + \frac{nV_{in}}{m\omega_r L_r}\theta = I_{Lm0} + \frac{nV_{in}}{mZ_r}\theta \tag{4}$$

where $\theta = \omega_r t$ with $\omega_r = 2\pi f_r$ being the resonant angular frequency, and I_{Lm0} represents the initial magnetizing current at $\theta = 0$.

The peak magnetizing current I_{Lmpk} is reached at $\theta = \pi$, i.e., $I_{Lmpk} = i_{Lm}(\pi)$. Due to the half-wave symmetry of the magnetizing current i_{Lm}, we have

$$I_{Lm0} = i_{Lm}(0) = -i_{Lm}(\pi) = -I_{Lmpk} \tag{5}$$

Substituting (5) into (4) yields the peak and initial magnetizing currents, i.e.,

$$I_{Lmpk} = -I_{Lm0} = \frac{\pi n V_{in}}{2mZ_r} = \frac{\pi V_o}{2mZ_r G} \tag{6}$$

B. Operation Principle

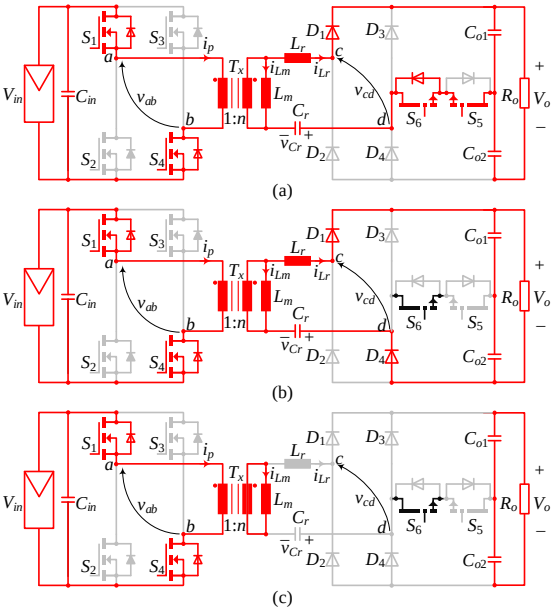

Fig. 5. Equivalent circuits of the proposed converter over the first half switching cycle [0, π]. (a) Stage I: [0, ϕ], (b) Stage II: [ϕ, α], and (c) Stage III: [α, π].

The key operating waveforms of the proposed DMR-SRC are shown in Fig. 4. Neglecting the deadtime, six stages can be identified over one switching cycle. Due to the symmetry of operation, only stages I-III over the first half switching cycle [0, π] are described.

Stage I ($\theta \in [0, \phi]$, see Figs. 4 and 5(a)): Before the time instant 0, S_2, S_3 and S_5 are conducting. At $\theta = 0$, S_2 and S_3 are turned off, the negative magnetizing current I_{Lm0} begins to charge/discharge the parasitic output capacitors (C_{oss1}-C_{oss4}) of primary-side switches, such that S_1 and S_4 can achieve ZVS-on. During this stage, S_5 is turned on, and a half-bridge rectifier is formed on the secondary side. The voltage v_{cd} is clamped by half of the output voltage $V_o/2$. The resonant inductor L_r and capacitor C_r resonate, and the resonant current i_{Lr} starts increasing from zero. When the parasitic output capacitor of S_6, i.e., C_{oss6}, is fully discharged, the antiparallel diode of S_6 begins to conduct. Thus, ZVS-on of S_6 can be achieved subsequently by applying the turn-on gate signal. The governing differential equations in this stage are obtained as

$$\begin{cases} \omega_r L_r \dfrac{\mathrm{d}i_{Lr}(\theta)}{\mathrm{d}\theta} = nv_{ab}(\theta) - v_{cd}(\theta) - v_{Cr}(\theta) = nV_{in} - V_o \,/\, 2 - v_{Cr}(\theta) \\ \omega_r C_r \dfrac{\mathrm{d}v_{Cr}(\theta)}{\mathrm{d}\theta} = i_{Lr}(\theta) \end{cases} \tag{7}$$

Considering the initial conditions $v_{Cr}(0) = V_{Cr0}$ and $i_{Lr}(0) = 0$, (7) can be solved as

$$\begin{cases} i_{Lr}(\theta) = (r_1 \,/\, Z_r)\sin\theta = A_1 \sin\theta \\ v_{Cr}(\theta) = -r_1 \cos\theta + nV_{in} - V_o \,/\, 2 \end{cases} \tag{8}$$

where $r_1 = nV_{in} - V_o \,/\, 2 - V_{Cr0}$, and $A_1 = r_1 \,/\, Z_r$.

Stage II ($\theta \in [\phi, \alpha]$, see Figs. 4 and 5(b)): At $\theta = \phi$, S_5 is turned off, the resonant current is diverted from S_5-S_6 to D_4, and a full-bridge rectifier is presented on the secondary side. Thus, the ac voltage v_{cd} is equal to the output voltage V_o, causing the resonant current to decrease sinusoidally. The governing differential equations in this stage are

$$\begin{cases} \omega_r L_r \dfrac{\mathrm{d}i_{Lr}(\theta)}{\mathrm{d}\theta} = nv_{ab}(\theta) - v_{cd}(\theta) - v_{Cr}(\theta) = nV_{in} - V_o - v_{Cr}(\theta) \\ \omega_r C_r \dfrac{\mathrm{d}v_{Cr}(\theta)}{\mathrm{d}\theta} = i_{Lr}(\theta) \end{cases} \tag{9}$$

The inductor current and capacitor voltage at $\theta = \phi$, i.e., $i_{Lr}(\phi)$ and $v_{Cr}(\phi)$, can be obtained from (8). Then, (9) can be solved as

$$\begin{cases} i_{Lr}(\theta) = \dfrac{r_2}{Z_r}\sin(\theta - \phi) + i_{Lr}(\phi)\cos(\theta - \phi) = A_2 \sin(\theta + \delta) \\ v_{Cr}(\theta) = -r_2 \cos(\theta - \phi) + i_{Lr}(\phi) Z_r \sin(\theta - \phi) + nV_{in} - V_o \end{cases} \tag{10}$$

where $r_2 = nV_{in} - V_o - v_{Cr}(\phi)$, $A_2 = \sqrt{(r_2 \,/\, Z_r)^2 + i_{Lr}^2(\phi)}$, and $\delta = \arccos[(r_2 \,/\, Z_r) \,/\, A_2] - \phi$.

Stage III ($\theta \in [\alpha, \pi]$, see Figs. 4 and 5(c)): When the resonant current i_{Lr} falls to zero at $\theta = \alpha$, D_1 and D_4 turn off under ZCS. Thus, the resonant tank is prevented from resonance and the resonant current and voltage are kept at 0 and V_{Cr0}, respectively. The output capacitors are discharged to supply the load.

III. CHARACTERISTICS OF THE PROPOSED CONVERTER

In this section, the characteristics of the proposed converter are analyzed in detail in terms of the DC voltage gain, RMS currents, and the soft-switching performance. Additionally, basic design guidelines are also presented.

A. DC Voltage Gain

Because of the half-wave symmetry of both the resonant inductor current i_{Lr} and the capacitor voltage v_{Cr}, we have

$$\begin{cases} i_{Lr}(\pi) = -i_{Lr}(0) = 0 \\ v_{Cr}(\pi) = -v_{Cr}(0) = -V_{Cr0} \end{cases} \tag{11}$$

Solving (3), (8), (10), and (11) yields the expressions for the voltage gain G and phase angle α as

$$\begin{cases} G = \dfrac{V_o}{nV_{in}} = \dfrac{1}{2\pi Q(3+\cos\phi)} \times \left\{ K + \dfrac{4\pi Q(4\pi Q + \sin^2\phi) - \cos^3\phi + 3\cos\phi - 2}{2 + 4\pi Q - \cos\phi - \cos^2\phi} \right\} \\ \alpha = \cos^{-1}\left\{ \dfrac{4(\sin\phi)^2(1+\cos\phi) - K[3 + 8\pi Q - 2\cos\phi - \cos(2\phi)]}{7 + 24\pi Q + 32\pi^2 Q^2 - 4(1+4\pi Q)\cos\phi - (3+8\pi Q)\cos(2\phi)} \right\} \end{cases} \tag{12}$$

where $K = \sqrt{8\pi Q(2\pi Q - \cos^2\phi - \cos\phi + 2) + (1-\cos\phi)^2}$.

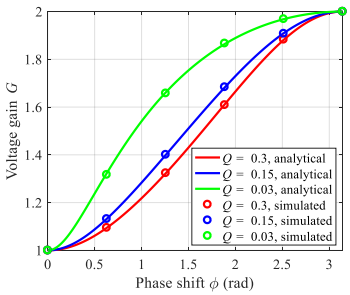

Fig. 6. Analytical and simulated results for the normalized voltage gain G with respect to the phase shift ϕ at different quality factors.

According to (12), the voltage gain can be depicted in Fig. 6. It can be seen that the range of the voltage gain is always between 1 and 2 irrespective of the quality factor (i.e., the load). It should be noted that the inductors ratio $m = L_m/L_r$ does not affect the voltage gain. Therefore, the magnetizing inductance can be designed as a large value under the condition that the ZVS-on of primary-side switches can be achieved. Circuit simulations of the proposed converter are conducted in PSIM, and the results are also presented in Fig. 6, which validates the obtained analytical gain model (12).

To compare, the voltage gain characteristics of the full-bridge series resonant converter (SRC) [50] and the full-bridge LLC resonant converter [25] are shown in Fig. 7. For the PFM controlled SRC, the light-load gain range is narrow (e.g., 0.85-1 at a light load Q = 0.1) even within a wide normalized switching-frequency range $f_n \in [1, 5]$. The PFM-controlled LLC resonant converter has improved gain characteristics. However, the heavy-load gain range is still narrow (e.g., 1-1.47 at a heavy load Q = 0.3). In order to have a high full-load gain peak, the characteristic impedance Z_r has to be decreased, resulting in a wider frequency range and/or increased conduction losses.

With the fixed-frequency PWM or phase-shift modulation (PSM) control, the gain ranges of the SRC and the LLC resonant converter are extended. However, the variation of the duty cycle D is also wide. When the duty cycle D is small, the conduction losses will rise and the soft-switching condition will be lost, because the peak magnetizing current is reduced dramatically in this case. In addition, when controlled with the PWM or PSM scheme, the primary-side (low-voltage and high-current side) switches of the SRC and LLC converter have to turn off at a large current, and thus the off-switching loss is large. By contrast, the peak magnetizing current of the proposed resonant converter does not vary significantly with respect to the voltage gain G: the variation range of I_{Lmpk} is twofold according to (6). Therefore, the ZVS-on of the primary-side switches can be achieved while keeping the magnetizing inductance large. Moreover, the primary-side switches in the proposed converter are turned off at the small peak magnetizing current; thus, the off-switching loss is small as well.

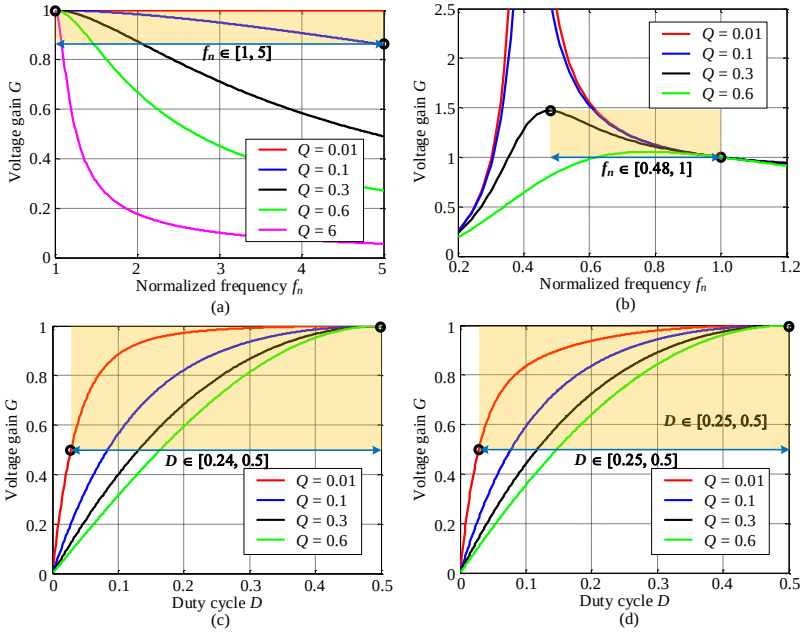

Fig. 7. Voltage gain characteristics of the full-bridge series resonant dc-dc converter and the full-bridge LLC resonant dc-dc converter: (a) SRC with PFM, (b) LLC resonant converter with PFM, (c) SRC with PWM or PSM, and (d) LLC resonant converter with PWM or PSM. In Fig. 7(a) and (b), the normalized switching frequency f_n is based on the series resonant frequency of the resonant tank.

Furthermore, the bill of materials (BOM) of the five topologies, i.e., the full-bridge SRC [50], the full-bridge LLC resonant converter [25], the proposed DMR-based SRC (see Fig. 2), and the derivatives *A* and *B* of the DMR-based SRC (see Fig. 3), is shown in Table I. The differences between the proposed and conventional topologies are highlighed in red. Compared with the conventional SRC and LLC resonant converter, the proposed DMR-based SRC (see Fig. 2) has a higher component count. More specifically, two active switches withstanding half of the output voltage are added on the secondary side, and the output capacitor is split into two low-voltage ones. Likewise, the proposed DMR-SRC derivatives *A* and *B* (see Fig. 3) also employ two secondary-side switches and two output capacitors in series. However, the secondary-side diode count is reduced from 4 to 2, and the voltage stress of the diodes is only half of the output voltage, which is beneficial to cost reduction.

TABLE I

COMPARISON OF BILL OF MATERIALS OF THREE TOPOLOGIES

Components		**Full-bridge SRC [50]**	**Full-bridge LLC resonant converter [25]**	**Proposed DMR-based SRC (Fig. 2)**	**Proposed DMR-SRC derivatives *A* and *B* (Fig. 3)**
Primary-side active switch	**Count**	× 4	× 4	× 4	× 4
	Voltage stress	Input voltage	Input voltage	Input voltage	Input voltage
Secondary-side active switch	**Count**	0	0	× 2	× 2
	Voltage stress	—	—	Half of output voltage	Half of output voltage
Diode	**Count**	× 4	× 4	× 4	× 2
	Voltage stress	Output voltage	Output voltage	Output voltage	Half of output voltage
Transformer		× 1	× 1	× 1	× 1
Resonant inductor		× 1	× 1	× 1	× 1
Resonant capacitor		× 1	× 1	× 1	× 1
Output capacitor	**Count**	× 1	× 1	× 2 in series	× 2 in series
	Voltage stress	Output voltage	Output voltage	Half of output voltage	Half of output voltage

B. RMS Currents

The secondary and primary transformer RMS currents can be obtained by

$$\begin{cases} I_{Lr,rms} = \sqrt{\dfrac{1}{\pi}\displaystyle\int_0^{\alpha} i_{Lr}^2(\theta)d\theta} \\ I_{p,rms} = \sqrt{\dfrac{1}{\pi}\displaystyle\int_0^{\alpha} i_{Lr}(\theta) + i_{Lm}(\theta)^{\,2}\, d\theta} \end{cases} \tag{13}$$

The final expressions of $I_{Lr,rms}$ and $I_{p,rms}$ are given in Appendix as (39). Fig. 8 shows the normalized RMS currents at different quality factors. The current normalization base is V_o/Z_r. It can be seen in Fig. 8 that at heavy loads, the RMS resonant current $I_{Lr,rms}$ increases with respect to the voltage gain. The reason is that when the gain increases, the input voltage decreases and thus the RMS current increases if the power is fixed. However, at light loads, the RMS current firstly increases and then decreases. This is because the angle α (see Fig. 4) is small at light loads when the voltage gain is in the middle area. A smaller α means a larger RMS current if the power is fixed. For the primary transformer RMS current $I_{p,rms}$, it is overall rising as the voltage gain G increases. However, at

light loads, $I_{p,rms}$ becomes flat with respect to G. When comparing the two RMS currents, it can be obtained that the difference between them is small. It is because the inductors ratio $m = L_m/L_r$ can be designed to be large for the proposed converter.

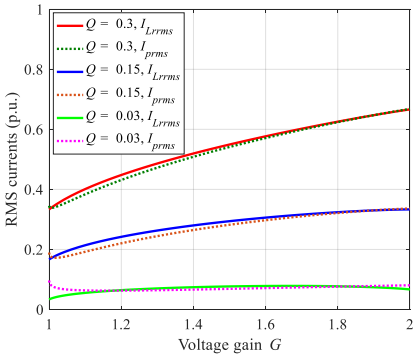

Fig. 8. Primary and secondary transformer RMS currents with respect to the voltage gain at $m = 6$.

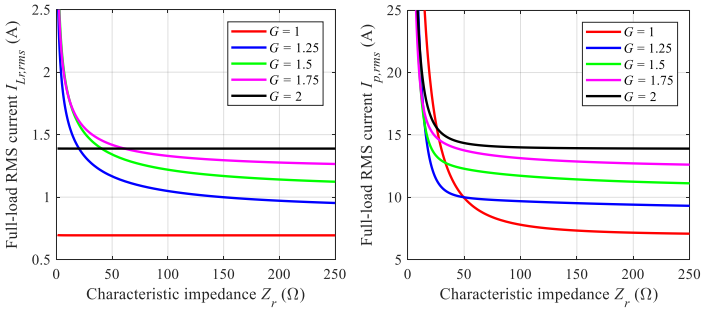

Fig. 9. Full-load RMS currents with respect to the characteristic impedance Z_r at different voltage gains. (a) Secondary-side RMS current $I_{Lr,rms}$; (b) Primary-side RMS current $I_{p,rms}$.

For the proposed converter, the characteristic impedance Z_r has a significant impact on the RMS current characteristics when the load is fixed. Fig. 9 shows the full-load RMS current curves under different characterisitc impedances Z_r and voltage gains G. As can be seen, the full-load RMS currents decrease with respect to the increase of the characteristic impedance Z_r except for $G = 1$ and $G = 2$ in Fig. 9(a). Considering the conduction losses, the characteristic impedance Z_r should be designed as large as possible. Moreover, when the resonant frequency is fixed, a larger Z_r means a larger L_r, which is beneficial to the short-circuit current suppression. However, a larger Z_r also leads to a larger ac voltage ripple and a higher voltage peak over the resonant capacitor C_r. Therefore, a tradeoff should be made in practice.

C. Soft-Switching

Ideally, the primary and secondary MOSFETs can achieve the ZVS turn-on if $i_p(0)$ and $-i_{Lr}(\theta_d)$ (see Fig. 4) are negative, as analyzed in Section II-B. This ideal ZVS condition always holds, as indicated by (6) and (8). In practice, however, there are parasitic

output capacitances in parallel with MOSFETs and diodes. Therefore, a certain amount of charge is required to fully discharge the output capacitance of the MOSFET during the deadtime interval, such that its antiparallel diode will conduct before the turn-on signal is applied [51]. Fig. 10 shows the ZVS mechanism of the primary and secondary transistors, and Fig. 11 illustrates the operating waveforms considering the deadtime and output capacitance of transistors. During the deadtime intervals, the output capacitances of the transistors are charged or discharged with i_p, i_{Lm} and/or i_{Lr}. It is assumed that $C_{oss1} = C_{oss2} = C_{oss3} = C_{oss4} = C_{oss,P}$, $C_{oss5} = C_{oss6} = C_{oss,S}$, and $C_{ossD1} = C_{ossD2} = C_{ossD3} = C_{ossD4} = C_{oss,D}$. Then, the voltage change and charge required for the ZVS-on can be obtained, as summarized in Table II.

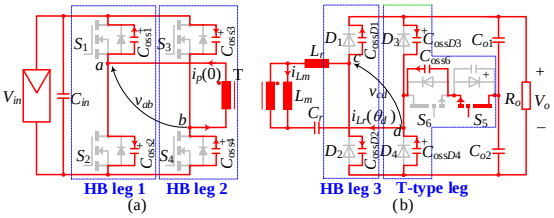

Fig. 10. ZVS mechanism of primary and secondary transistors (see Fig. 10): (a) ZVS turn-on of S_1 and S_4 at $t = 0$, and (b) ZVS turn-on of S_6 at $t = 0$. C_{oss1}-C_{oss4}, C_{ossD1}-C_{ossD4}, and C_{oss5}-C_{oss6} are the parasitic capacitances of transistors and diodes.

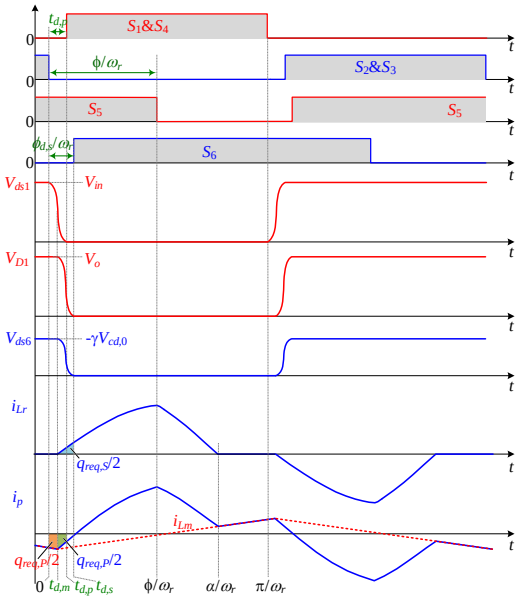

Fig. 11. Operating waveforms of the proposed converter considering the deadtime and output capacitances of transistors and diodes.

TABLE II

REQUIRED MINIMUM CHARGE TO ACHIEVE ZVS FOR DIFFERENT SWITCH LEGS.

Commu-tation mode	**Current to achieve ZVS**	**Output capacitor**		**Initial capacitor voltage at t = 0**	**Final capacitor voltage at t = $t_{d,P}$ or $t_{d,S}$**	**Absolute charge variation of a capacitor**	**Charge variation of an HB/T-type leg**	**Minimum charge q_{req} for ZVS-ON of all switches**
Primary side ZVS (see Fig. 9(a))	i_{Lm} and i_p	HB leg 1	C_{oss1}	V_{in}	0	$V_{in}C_{oss,P}$	$2V_{in}C_{oss,P}$	$q_{req,P} = 2V_{in}C_{oss,P}$
			C_{oss2}	0	V_{in}	$V_{in}C_{oss,P}$		
		HB leg 2	C_{oss3}	0	V_{in}	$V_{in}C_{oss,P}$	$2V_{in}C_{oss,P}$	
			C_{oss4}	V_{in}	0	$V_{in}C_{oss,P}$		
Secondary side ZVS (see Fig. 9(b))	i_{Lr}	HB leg 3	C_{ossD1}	$0.5V_o-(1-\gamma)V_{cd0}$	0	$[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}$	$[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}$	$q_{req,S} = \max\{[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}, -\gamma V_{cd0}(2C_{oss,D}+C_{oss,S})\}$
			C_{ossD2}	$0.5V_o+(1-\gamma)V_{cd0}$	V_o	$[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}$		
		T-type leg	C_{ossD3}	$0.5V_o+\gamma V_{cd0}$	$0.5V_o$	$-\gamma V_{cd0}C_{oss,D}$	$-\gamma V_{cd0}(2C_{oss,D}+C_{oss,S})$	
			C_{ossD4}	$0.5V_o-\gamma V_{cd0}$	$0.5V_o$	$-\gamma V_{cd0}C_{oss,D}$		
			C_{oss5}	0	0	0		
			C_{oss6}	$-\gamma V_{cd0}$	0	$-\gamma V_{cd0}C_{oss,S}$		

Primary-Side ZVS: The ZVS-on realization of S_1 requires a complete charging of C_{oss1} and a complete discharging of C_{oss2} during the deadtime interval $t_{d,P}$, as shown in Fig. 10 (a) and Fig. 11. The total required charge $q_{req,P}$ (see Table II) can be divided into $q_{req,P}/2$ within [0, $t_{d,m}$] and $q_{req,P}/2$ within [$t_{d,m}$, $t_{d,P}$], as illustrated in Fig. 11. Due to the high nonlinearity of the parasitic output capacitance with respect to the drain-source voltage, the current waveforms i_{Lm} and i_p will not be distorted significantly during the deadtime interval [52].

To achieve the complete charging and discharging of output capacitances, the charge provided by the currents i_{Lm} and i_p (see Fig. 11) during the deadtime interval [0, $t_{d,P}$] should satisfy

$$\begin{cases} \int_0^{t_{d,m}} -i_{Lm}(\omega_r t)dt = \int_0^{t_{d,m}} \left(-I_{Lm0} - \dfrac{nV_{in}}{mZ_r}\omega_r t\right)dt \geq \dfrac{q_{req,P}}{2} \\ \int_0^{t_{d,P}-t_{d,m}} -i_p(\omega_r t)dt = \int_0^{t_{d,P}-t_{d,m}} -[A_1\sin(\omega_r t) + i_{Lm}(\omega_r t)]dt \approx \int_0^{t_{d,P}-t_{d,m}} -I_{Lm0} - \left(\dfrac{nV_{in}}{mZ_r} + A_1\right)\omega_r t dt \geq \dfrac{q_{req,P}}{2} \end{cases} \tag{14}$$

From (14), it is obtained that the inductors ratio m should be designed according to

$$m = \frac{L_m}{L_r} \leq \min\left\{\frac{2nt_dV_{in}(2\pi - t_d\omega_r)}{8q_{req,P}Z_r + nV_{in}\omega_r t_d^2[G(\pi GQ-1)+2]}\right\} \tag{15}$$

Secondary-Side ZVS: Before the output rectifier conducts, e.g., before t = 0 in Fig. 11, a capacitor network composed of C_{ossD1}-C_{ossD4} and C_{oss6} presents on the secondary side, as shown in Fig. 10 (b). By applying the Kirchhoff's voltage and current laws to the capacitor network, the steady-state capacitor voltages (i.e., the voltages at t = 0), can be obtained as

$$\begin{cases} V_{D1,0} = V_o \,/\, 2 - (1-\gamma)V_{cd,0} \\ V_{D2,0} = V_o \,/\, 2 + (1-\gamma)V_{cd,0} \\ V_{D3,0} = V_o \,/\, 2 + \gamma V_{cd,0} \\ V_{D4,0} = V_o \,/\, 2 - \gamma V_{cd,0} \\ V_{dsS5,0} = 0 \\ V_{dsS6,0} = \gamma V_{cd,0} \end{cases} \tag{16}$$

where

$$\begin{cases} \gamma = \dfrac{2C_{oss,D}}{4C_{oss,D} + C_{oss,S}} \\ V_{cd,0} = -nV_{in} - V_{Cr0} = V_o\left(\dfrac{\pi GQ}{2} - \dfrac{1}{G}\right) \end{cases} \tag{17}$$

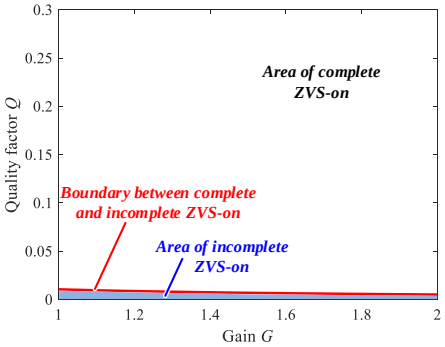

Fig. 12. Ranges of complete ZVS-on and incomplete ZVS-on for S_5 and S_6. The shaded area represents the range of incomplete ZVS-on, and the solid red line is the boundary between the complete and incomplete ZVS-on ranges.

The turn-on of S_6 lags the turn-off of S_2&S_3 with a deadtime $t_{d,s} = \phi_{d,s} / \omega_r$, and the turn-on of S_5 lags the turn-off of S_1&S_4 with the same deadtime $t_{d,s} = \phi_{d,s} / \omega_r$, as shown in Fig. 11. At $t = t_{d,s}$, the secondary-side capacitors reach new steady states with the final voltages showing in Table II. Then, the absolute charge variation of each capacitor and the minimum charge $q_{req,S}$ required for the secondary-side ZVS-on can be obtained, as listed in Table II. To achieve the ZVS-on operation for the secondary transistors S_5 and S_6, the charge provided by the resonant current should be larger than the required one $q_{req,S}$, i.e.,

$$\int_0^{\alpha/(\omega_r t)} i_{Lr}(\omega_r t)dt = \int_0^{\phi/(\omega_r t)} A_1 \sin(\omega_r t)dt + \int_{\phi/(\omega_r t)}^{\alpha/(\omega_r t)} A_2 \sin(\omega_r t + \delta)dt \geq q_{req,S} \tag{18}$$

Simplifying (18) yields the practical complete ZVS-on conditions for S_5 and S_6, i.e.,

$$A_1(1-\cos\phi) + A_2[\cos(\delta+\phi) - \cos(\delta+\alpha)] \geq \omega_r q_{req,S} \tag{19}$$

If (19) is not satisfied, S_5 and S_6 will withstand incomplete ZVS-on. Nevertheless, the drain-source voltage of S_5 and S_6 is low, i.e., $\leq V_o/2$. Therefore, the turn-on losses are not significant even operating under an incomplete ZVS-on condition. Based on (19), the areas for the complete ZVS-on and incomplete ZVS-on of S_5 and S_6 can be obtained, as shown in Fig. 12. It is seen that the incomplete ZVS-on occurs only when the quality factor Q (i.e., the load) is very low (e.g., $Q < 0.007$ at $G = 2$).

D. Design Guidelines

The flowchart of the design process for the main components of the proposed converter is shown in Fig. 13. Before the design, system specifications, e.g., the most possible PV voltage range, nominal output (dc-link) voltage, and maximum output power, are determined. Then, the voltage stresses of semiconductor devices and output capacitors can be obtained based on Table I. After that, the component parameters, e.g., output capacitances C_{o1}-C_{o2}, transformer turns ratio n, magnetizing inductance L_m, and resonant tank (L_r and C_r) can be determined. Subsequently, the current stresses of the main components can be calculated based on the mathematic models built in Sections II and III. Finally, the component selection and design optimization can be performed.

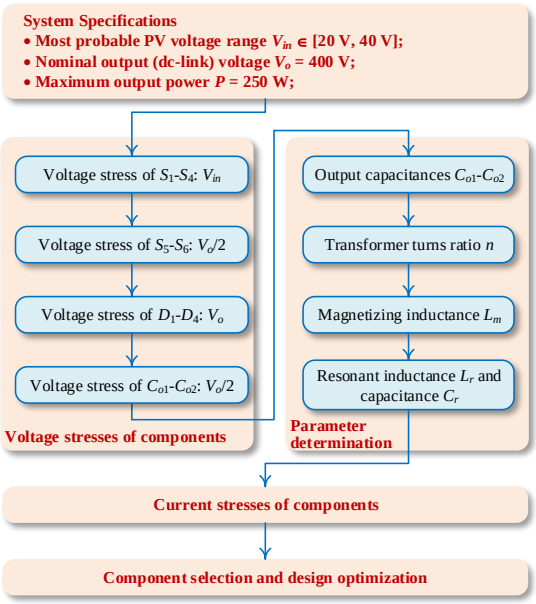

Fig. 13. Flowchart of the design process for the main components of the proposed converter.

The parameter determination process is detailed as follows.

1) Output (DC-Link) Capacitances

The output capacitors of the proposed dc-dc converter also act as an energy buffer in the two-stage PV microinverter. The instantaneous feeding power to the grid contains a fluctuating power at twice the line frequency, whereas the PV output is dc power.

Thus, the output (dc-link) capacitors are used to decouple the power mismatch. The electrical stresses over the dc-link capacitors can be calculated as [53]

$$\begin{cases} \Delta V_o \approx P / (2\pi f_0 C_o V_o) \\ I_{Co,rms} = P / (\sqrt{2} V_o) \end{cases} \tag{20}$$

where f_0 represents the line frequency, P is the average power injected to the grid, the equivalent output (dc-link) capacitance $C_o = 1/(1/C_{o1} + 1/C_{o2})$, ΔV_o is the peak-to-peak ripple of the output voltage V_o, and $I_{Co,rms}$ is the RMS current flowing through the output (dc-link) capacitors. Considering a 6%-voltage ripple on the dc-link voltage, the required minimum capacitance output capacitance equals 83 μF. In this design, two low-profile (height: 1.5 cm) 250-V 180-μF electrolytic capacitors are adopted and connected in series.

2) Transformer Turns Ratio n and Magnetizing Inductance L_m

The transformer turns ratio n is determined by

$$n = N_s : N_p = \frac{V_o}{G V_{in}} \tag{21}$$

where N_p and N_s are the numbers of primary and secondary winding turns. Considering the ranges of the voltage gain G (see Fig. 6) and the input voltage V_{in} (see Fig. 13), the transformer turns ratio n is chosen as 10.

For the magnetizing inductance L_m, it is used to assist the primary-side switches achieve the ZVS-on. A smaller L_m leads to a higher magnetizing current, thereby being beneficial to ZVS-on. However, the conduction loss will be increased due to the higher circulating current (i.e., magnetizing current). Therefore, the design principle of L_m is that it should be possibly large under the premise that the ZVS-on of S_1-S_4 can be achieved, as illustrated by (15).

3) Resonant Inductance and Capacitance

As analyzed in Section III-B, a trade-off between the RMS currents and the resonant capacitor voltage ripple (or peak voltage) should be made for the design of the characteristic impedance Z_r. Meanwhile, it is seen from Fig. 9 that the RMS current curves become flat when Z_r exceeds a certain value (e.g., 175 ~ 225 Ω), which means that increasing Z_r cannot further reduce the conduction losses. Therefore, the design of L_r and C_r follows

$$\begin{cases} f_s = f_r = \dfrac{1}{2\pi\sqrt{L_r C_r}} = 1 \text{ MHz} \\ 175\ \Omega \le Z_r = \sqrt{\dfrac{L_r}{C_r}} \le 225\ \Omega \end{cases} \tag{22}$$

Solving (22) and considering the availability of resonant capacitors yield L_r = 34 μH and C_r = 7.5 nF.

IV. Power Loss Modeling and Design Optimization

A. Power Semiconductors

1) Primary-Side Switches S_1-S_4

All the primary-side switches can achieve the ZVS-on and are turned off at the small peak magnetizing current I_{Lm0}. Therefore, the switching losses of the primary-side switches are small and can be neglected. The total conduction losses of the four switches S_1-S_4 can be calculated as

$$P_{S14,con} = 4R_{S14,on}(I_{p,rms} / \sqrt{2})^2 \tag{23}$$

where $R_{S14,on}$ is the on-state resistance of the primary-side switches S_1-S_4.

As analyzed in Section III, the voltage stress of S_1-S_4 equals the input voltage V_{in} which is determined by the PV module properties (e.g., number of cells and material) and environmental conditions (i.e., solar irradiance and ambient temperature). In this paper, a maximum input voltage of 43 V is considered for the proposed converter, and thus, the 80-V eGaN® FETs [54] from Efficient Power Conversion (EPC) Corporation are chosen for a sufficient voltage margin. The maximum RMS current flowing through S_1-S_4 is about $14.1 / \sqrt{2} = 10$ A (see Fig. 9(b)). Considering the availability of 80-V GaN transistors, EPC2029 is finally selected for the implementation of S_1-S_4.

2) Secondary-Side Switches S_5-S_6

The voltage stress of the secondary-side switches S_5-S_6 is half of the output voltage V_o. The maximum output voltage is 430 V in this paper, and the maximum withstanding voltage of S_5-S_6 is about 215 V. Considering a 1.5-2 times voltage margin, the voltage rating of S_5-S_6 should be 322.5-430 V. However, the available voltage ratings of GaN transistors on the market were either below 200 V or above 600 V when the PV microinverter was designed in 2017. To the best of our knowledge, the 350-V and 400-V GaN transistors [55], [56] has not been commercialized until 2018.

For a series of GaN transistors with the same voltage rating, their current ratings and drain-source on-state resistances are achieved by employing different numbers of standard die units in parallel. For instance, the numbers of die units inside the 650-V GaN eHEMTs, GS66502B, GS66504B, GS66506T and GS66508B [57] are 2, 4, 6, and 8, respectively, as shown in Fig. 14(a). Their drain-source on-state resistances are inversely proportional to the number of die units, whereas the parasitic input and output capacitances of a GaN transistor are proportional to the total die area. Thus, the lower the drain-source on-state resistance, the higher the parasitic input and output capacitances. In this case, the gate drive loss and incomplete ZVS loss [61] will be increased. For the proposed converter, the incomplete ZVS range of S_5-S_6 is very small, as indicated in Fig. 12. Hence, the conduction loss and cost are the main factors affecting the selection of GaN transistors. Fig. 14 (b) shows the market price of the 650-V GaN eHEMTs of GaN Systems. It can be seen that the price of a GaN transistor increases with respect to the number of die units inside. As mentioned before, the on-

state resistance and conduction loss can be reduced with a higher number of die units, but the implementation cost will be increased as well. Therefore, as a trade-off between the cost and the power conversion efficiency, GS66504B with N_{unit} = 4 is selected for S_5 and S_6.

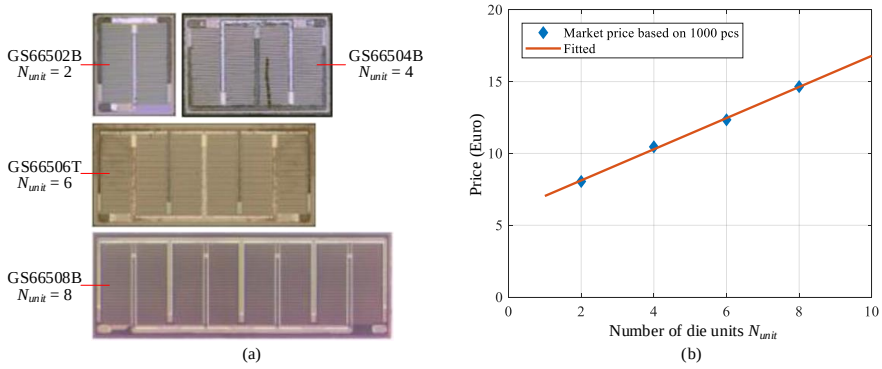

Fig. 14. (a) Microscopy images of four 650-V GaN dies [58]; The total die area of GS66508P (12.3 mm^2 [59]) is almost twice of GS66504B (6.1 mm^2 [60]). (b) Market price of GaN Systems' 650-V GaN eHEMTs with different numbers of die units; the survey was conducted at Mouser Electronics™ in 2017.

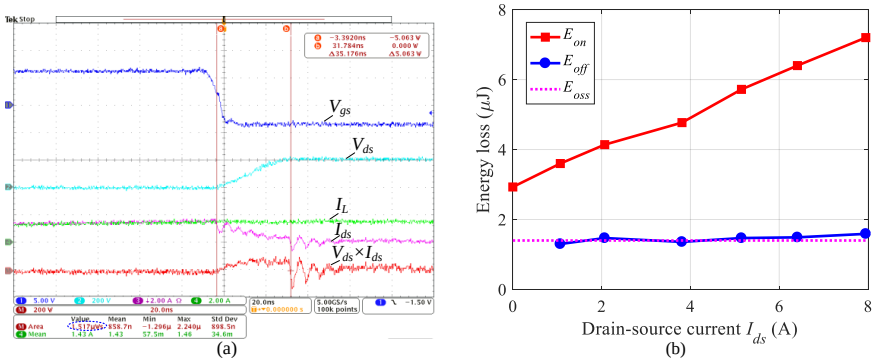

Fig. 15. Double-pulse test on the GaN eHEMT GS66504B: (a) measured turn-off waveforms of GS66504B, (b) comparison between the measured turn-off energy loss and the energy stored in the output capacitance of GS66504B at V_{ds} = 200 V.

The secondary switches S_5-S_6 can achieve the ZVS-on operation, but are turned off with a relatively large current, as shown in Fig. 4. Therefore, there may be an amount of turn-off losses if the turn-off speed is not fast enough. A double-pulse testing setup has been built up in order to explore the turn-off power losses of GS66504B devices. The turn-off waveforms at V_{ds} = 200 V and I_{ds} = 1.43 A are shown in Fig. 15(a). When the gate voltage V_{gs} falls to below the threshold voltage, the channel is cut off quickly, but the drain-source voltage V_{ds} has not significantly increased. Therefore, the drain-source current is diverted to the output capacitor of the GaN eHEMT, causing V_{ds} to rise from 0 to 200 V. The measured turn-off energy loss is approximately equal to the energy stored in the

output capacitor C_{oss}, as shown in Fig. 15(b). It should be noted that the calculated turn-off energy loss E_{off} ($\approx E_{oss}$) is not truly dissipated during the turn-off period. If the switch is subsequently turned on under hard switching, then the energy stored in the output capacitor C_{oss}, i.e., E_{oss}, will be dissipated on the channel. However, the switch in this converter can achieve the ZVS-on, which means that the energy stored in the output capacitor is transferred instead of being dissipated. Therefore, for the proposed converter, the secondary-side switches implemented with GaN HEMTs can achieve a quasi-lossless turn-off.

For the conduction loss of S_5-S_6, it can be calculated as

$$P_{S56,con} = 2R_{S56,on}I_{S56,rms}^2 \tag{24}$$

where $R_{S56,on}$ is the on-state resistance of S_5 and S_6, and $I_{S56,rms}$ is the RMS current flowing through S_5 and S_6.

3) Secondary-Side Rectifier Diodes

The rectifier diodes D_1-D_4 are operating in the discontinuous conduction mode (DCM), and theoretically, the ZCS-off can be achieved for D_1-D_4, as shown in Fig. 4. In practice, however, the ZCS condition (i.e., $i_{Lr}(\alpha) = 0$) cannot be always guaranteed due to the resonance of the parasitic output capacitors of rectifier diodes, resonant capacitor C_r, and series inductor L_r. If D_1-D_4 are implemented with silicon ultrafast recovery diodes, the reverse recovery losses will be high at the 1-MHz switching frequency despite of a quasi-ZCS operation. Hence, four 600-V SiC Schottky diodes, C3D02060E, are utilized in order to ensure a negligible reverse recovery loss at the 1-MHz switching frequency.

The conduction loss of the rectifier diodes can be calculated as

$$P_{D,con} = 2(I_{D12,avg} + I_{D34,avg})V_F + 2(I_{D12,rms}^2 + I_{D34,rms}^2)R_D \tag{25}$$

where V_F and R_D are the voltage drop at the zero current and the resistance of the diode, respectively; $I_{D12,avg}$ and $I_{D34,avg}$ represent the average currents of D_1-D_2 and D_3-D_4, respectively; and $I_{D12,rms}$ and $I_{D34,rms}$ denote the RMS currents of D_1-D_2 and D_3-D_4, respectively.

B. Magnetic Components

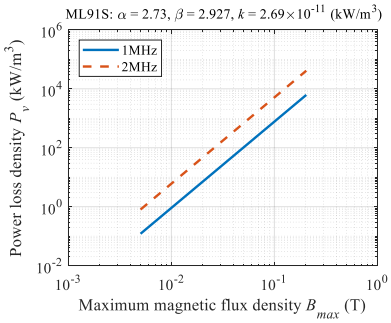

Fig. 16. Power loss density of ML91S material under sinusoidal excitation.

Planar transformers and inductors are used in this research, and the magnetic core material is ML91S from Hitachi Metal, which has the lowest core loss density at the 1-MHz frequency among all available materials [46], [47]. Fig. 16 presents the power loss density data of the ML91S material under the sinusoidal excitation. With curve fitting, its Steinmetz parameters k, α and β can be obtained, as shown in Fig. 16.

For the proposed converter, the magnetic cores are excited with nonsinusodial voltages, and therefore, the core loss density can be calculated with the improved generalized Steinmetz equation (iGSE) [62]

$$P_v = \frac{1}{T_s}\int_0^{T_s} k_i \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\mathrm{d}t \tag{26}$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}\left|\cos\varphi\right|^{\alpha} 2^{\beta-\alpha}\,\mathrm{d}\varphi} \tag{27}$$

The ac resistance of the winding increases dramatically with respect to the frequency due to the skin effect and proximity effect, and it can be calculated with the Dowell equation [63], [64]:

$$\frac{R_{ac}}{R_{dc}} = \frac{\xi}{2}\left(\frac{\sinh\xi+\sin\xi}{\cosh\xi-\cos\xi} + (2m-1)^2\frac{\sinh\xi-\sin\xi}{\cosh\xi+\cos\xi}\right) \tag{28}$$

where $\xi = h / \delta_s$, h is the thickness of PCB traces, δ_s is the skin depth of the conductor, and m is a magnetomotive force (MMF) ratio

$$m = \frac{F(h)}{F(h)-F(0)} \tag{29}$$

in which $F(0)$ and $F(h)$ are the MMFs at the borders of a layer. The winding loss calculation requires the RMS values of the harmonics of the resonant current i_{Lr}. Therefore, the resonant current is expanded based on Fourier series, as shown in the Appendix.

1) Transformer

For the transformer in the proposed converter, applying the Faraday's law to (26) yields a simplified core loss density equation:

$$P_v = k_i(2f_s)^{\alpha-\beta}\left(\frac{V_{in}}{N_p A_e}\right)^{\beta} \tag{30}$$

where N_p is the number of primary turns, and A_e is the effective sectional area of the magnetic core.

The planar core ER32/6/25 and 2-layer PCB windings (70-μm copper thickness for each layer) are adopted to fabricate the transformer. For the PCB winding layout, three arrangements are explored, as illustrated in Fig. 17. As can be seen, different winding arrangements lead to different MMF distributions, which affect the ac resistance and power loss of windings. Compared with the non-interleaving (see Fig. 17(a)) and interleaving (see Fig. 17(b)) winding arrangements, the arrangement 0.5P-S-P-S-0.5P (see Fig.

17(a)) enables the minimum MMF ratio for windings, and therefore the ac resistance can be reduced. In addition to the power loss, the intra- and inter-winding capacitances of planar transformers will affect the converter operation, and they should be controlled as low as possible for the proposed converter. It is proved in [65] and [66] that the arrangement 0.5P-S-P-S-0.5P can achieve the minimum stray capacitance while maintaining the lowest resistance.

Fig. 18 shows the calculated power losses of the planar transformers with different winding arrangements and different numbers of primary turns N_p. As can be seen, the winding arrangement 0.5P-S-P-S-0.5P can achieve the minimum power losses compared with the other two arrangements. From Fig. 18, it can also be observed that with the increase of the number of primary turns N_p, the core loss decreases, whereas the winding loss rises due to the increased resistance. The case when N_p = 2 allows the transformer to achieve the minimum power loss.

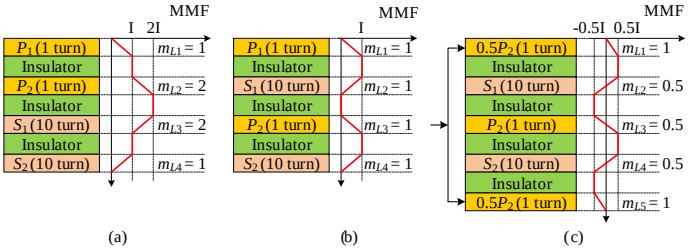

Fig. 17. MMF distribution of different winding arrangements in the case of N_p = 2: (a) non-interleaving winding arrangement: P-P-S-S, (b) interleaving winding arrangement: P-S-P-S, (c) 0.5P-S-P-S-0.5P. 'P' represents the primary winding and 'S' denotes the secondary winding.

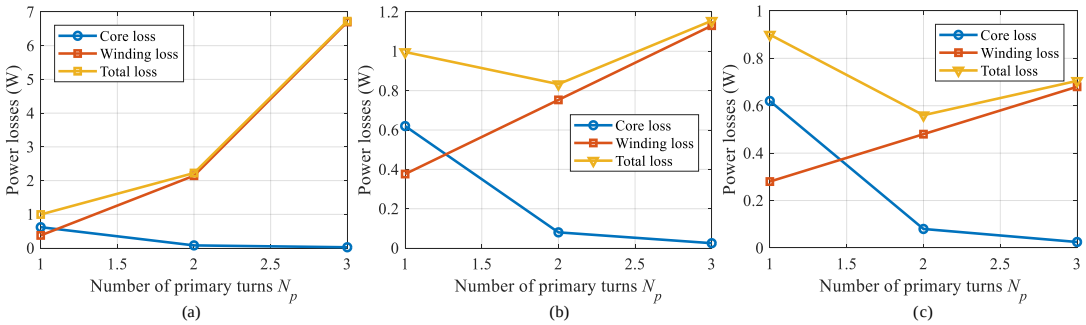

Fig. 18. Calculated power losses of planar transformers with different winding arrangements and different numbers of primary turns N_p: (a) non-interleaving winding arrangements: P-S for N_p = 1, P-P-S-S for N_p = 2, P-P-P-S-S-S for N_p = 3, (b) interleaving winding arrangement: P-S for N_p = 1, P-S-P-S for N_p = 2, P-S-P-S-P-S for N_p = 3, (c) 0.5P-S- 0.5P for N_p = 1, 0.5P-S-P-S-0.5P for N_p = 2, 0.5P-S-P-S-P-S-0.5P for N_p = 3.

2) Resonant Inductor

The voltage across the resonant inductor can be obtained as

$$v_{Lr}(t) = v_{ab}(t) - v_{cd}(t) - v_{Cr}(t) \tag{31}$$

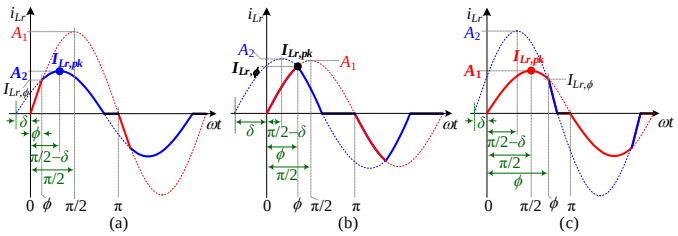

Fig. 19. Positions of the peak resonant current $I_{Lr,pk}$ in different operating conditions: (a) $0 \le \phi < \pi/2 - \delta$, (b) $\pi/2 - \delta \le \phi < \pi/2$, (c) $\pi/2 \le \phi \le \pi$.

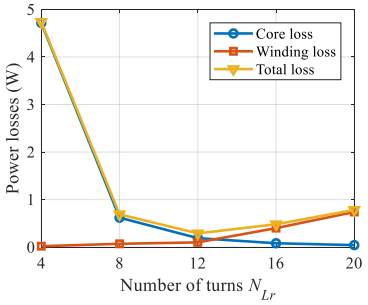

Fig. 20. Calculated power losses of planar inductors with different numbers of turns N_{Lr}.

Substituting (8) and (10) into (31) yields v_{Lr} over half a switching cycle [0 π], i.e.,

$$\left|\frac{dB}{dt}\right| = \frac{\left|v_{Lr}(t)\right|}{N_{Lr}A_{e,Lr}} = \frac{1}{N_{Lr}A_{e,Lr}} \times \begin{cases} A_1 Z_r \left|\cos(\omega_r t)\right|, & t \in [0, \phi / \omega_r] \\ A_2 Z_r \left|\cos(\omega_r t + \delta)\right|, & t \in (\phi / \omega_r, \alpha / \omega_r] \\ 0, & t \in (\alpha / \omega_r, \pi / \omega_r] \end{cases} \tag{32}$$

where

$$\phi = \arccos\left\{1 - \frac{4\pi QG(G-1)}{2 - G(1+\pi QG)}\right\} \tag{33}$$

For the magnetic flux density swing of the resonant inductor, it is related to the peak resonant current, which has three different cases, as illustrated in Fig. 19. Then, the flux density swing can be obtained as

$$\Delta B_{Lr} = \frac{L_r \Delta I_{Lr}}{N_{Lr}A_{e,Lr}} = \frac{L_r}{N_{Lr}A_{e,Lr}} \times \begin{cases} 2A_2, & 0 \le \phi < \dfrac{\pi}{2} - \delta \\ 2i_{Lr}(\phi), & \dfrac{\pi}{2} - \delta \le \phi < \dfrac{\pi}{2} \\ 2A_1, & \dfrac{\pi}{2} \le \phi \le \pi \end{cases} \tag{34}$$

where $A_1 = r_1 / Z_r$, $A_2 = \sqrt{(r_2 / Z_r)^2 + I_{Lr,\phi}^2}$, $\delta = \arctan[(r_2 / Z_r) / A_2] - \phi$, and $I_{Lr,\phi} = (r_1 / Z_r)\sin\phi$. The core loss can be subsequently calculated based on (26).

The magnetic core ER26/6/15 and 2-layer PCB windings (70-μm copper thickness for each layer) are used to implement the planar resonant inductor. The calculated power losses of planar inductors with different numbers of turns N_{Lr} are shown in Fig. 20. It is seen that N_{Lr} = 12 enables the inductor to achieve the minimum power loss.

C. Capacitors

The power losses in capacitors are generally composed of dielectric losses and thermal losses [67]. The dielectric losses associated with the cycle of charging and discharging of dielectrics are calculated as

$$P_{Cd} = C_r \left| V_{Cr0} \right| f_s \tan\delta \tag{35}$$

where tan δ is the dielectric loss factor of the chosen capacitor.

The thermal losses are derived as

$$P_{Cth} = R_e I_{Lr,rms}^2 \tag{36}$$

where R_e is the equivalent series resistance of the resonant capacitor C_r.

V. Control Strategy, Modulation Implementation, and Experimental Verifications

A. Control Strategy

Depending on the PV panel properties and the environmental conditions (i.e., the solar irradiance and ambient temperature), the PV output voltage and power at the maximum power points (MPPs) may change significantly. Fig. 21 depicts a typical operation profile, i.e., the maximum power with respect to the input voltage, for PV microinverter systems. In this case, the maximum power P_{max} is 250 W when V_{in} is within [25 V, 38 V], but P_{max} declines when V_{in} is out of this range. Six operating points are identified, as shown in Table III.

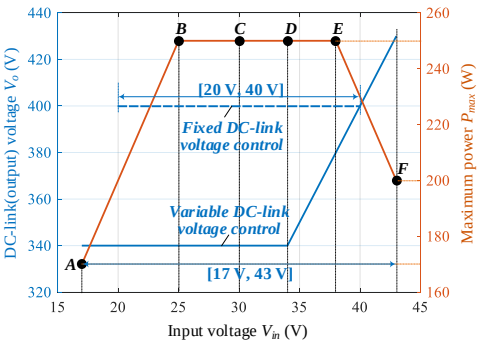

Fig. 21. Operation profile of the PV microinverter with fixed and variable DC-link voltage control schemes. The profile of the PV output power P_{PV} is determined by different PV panels as well as the environmental conditions (i.e., the solar irradiance and ambient temperature).

Table III

IDENTIFIED SIX OPERATING POINTS WITH FIXED AND VARIABLE DC-LINK VOLTAGE CONTROL STRATEGIES

Operating point	PV voltage V_{PV}	PV power P_{PV}	DC-link voltage V_o under the variable DC-link voltage control	DC-link voltage V_o under the fixed DC-link voltage control
A	17 V	170 W	340 V	NaN
B	25 V	250 W	340 V	400 V
C	30 V	250 W	340 V	400 V
D	34 V	250 W	340 V	400 V
E	38 V	250 W	380 V	400 V
F	43 V	200 W	430 V	NaN

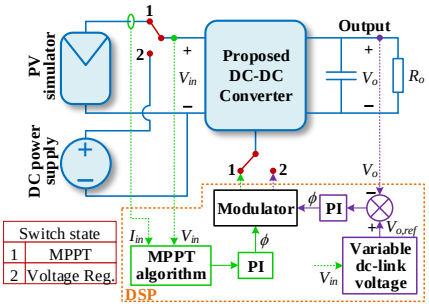

Fig. 22. Control diagram of the proposed dc-dc converter with two operation modes: output (dc-link) voltage regulation or MPPT.

In the PV microinverter systems (see Fig. 1), the dc-link voltage can be regulated either by the front-end dc-dc stage or by the dc-ac inverter stage. If the MPPT is implemented with the dc-dc stage, then the dc-link voltage will be regulated by the inverter stage, and vice versa. However, it is not necessary to always keep the DC-link voltage constant. In this paper, a variable DC-link voltage control is proposed, as shown in Fig. 21. When the input PV voltage V_{in} is lower than 34 V, the dc-link (output) voltage will be always regulated to 340 V; however, when V_{in} is higher than 34 V, then the dc-link (output) voltage reference will rise with the increase of V_{in}. Thus, the input voltage range can be extended from [20 V, 40 V] with the conventional fixed dc-link voltage control to [17 V, 43 V] with the new control. In the meanwhile, the RMS currents under the variable dc-link voltage control are also reduced which is beneficial to efficiency improvement.

As aforementioned, the proposed dc-dc converter can be controlled either to achieve the MPPT of the PV panel or to regulate the dc-link voltage. In order to demonstrate the feasibility of the proposed converter in both cases, a flexible control scheme is applied, as shown in Fig. 22. If operation mode 1 is enabled, the proposed dc-dc converter will be connected to a PV simulator and it will be controlled to achieve the MPPT; if operation mode 2 is selected, then the proposed converter will be powered by a dc power supply and it will be used to regulate the output voltage to the reference $V_{o,ref}$.

B. Modulation Implementation

Two enhanced pulse width modulator (ePWM) peripherals of TMS320F28075 digital signal processor (DSP), i.e., ePWM1 and ePWM2, are utilized, and their output signals are EPWM1A/EPWM1B and EPWM2A/EPWM2B, respectively. EPWM1A and

EPWM1B are the gate signals of S_1&S_4 and S_2&S_3, respectively. EPWM2A and EPWM2B are used to control S_5 and S_6, respectively. Each time-base counter *CTR* of the ePWM modules is running in the count-up-and-down mode, and the period registers of ePWM1 and ePWM2 are the same. The dead time of EPWM1A (S_1&S_4) and EPWM1B (S_2&S_3) is achieved by using the dead-band submodule of ePWM1. There is a phase shift *PHS2* between the two counters (*CTR2* and *CTR1*) of ePWM2 and ePWM1. The phase shift is used to generate the turn-on delay of S_5 and S_6 with respect to the turn-off events of S_1&S_4 and S_2&S_3, as indicated by $\phi_{d,s}$ in Fig. 11.

The values of the period registers *PRD1* and *PRD2* are determined by

$$PRD1 = PRD2 = f_s \,/\, (2f_{cpu}) \tag{37}$$

where f_{cpu} is the clock frequency of the microcontroller. For the two counter-compare registers *CMP2A* and *CMP2B*, their values and actions generated by the "*CTR2 = CMP2A/B*" event are different in two cases:

$$\begin{aligned} CMP2A &= \begin{cases} PRD2 \times (\phi - \phi_{d,s}) \,/\, \pi \\ Action:\ \text{EPWM2A clears at CAU} \end{cases}, \phi_{d,s} < \phi \le \pi \\ &\quad \begin{cases} PRD2 \times (\phi_{d,s} - \phi) \,/\, \pi \\ Action:\ \text{EPWM2A clears at CAD} \end{cases}, 0 \le \phi \le \phi_{d,s} \\ CMP2B &= \begin{cases} PRD2 \times \left[1 - (\phi - \phi_{d,s}) \,/\, \pi\right] \\ Action:\ \text{EPWM2B clears at CBD} \end{cases}, \phi_{d,s} < \phi \le \pi \\ &\quad \begin{cases} PRD2 \times \left[1 - (\phi_{d,s} - \phi) \,/\, \pi\right] \\ Action:\ \text{EPWM2B clears at CBU} \end{cases}, 0 \le \phi \le \phi_{d,s} \end{aligned} \tag{38}$$

The modulation scheme enable the converter control variable, i.e., the phase shift ϕ, to be adjusted from 0 to π.

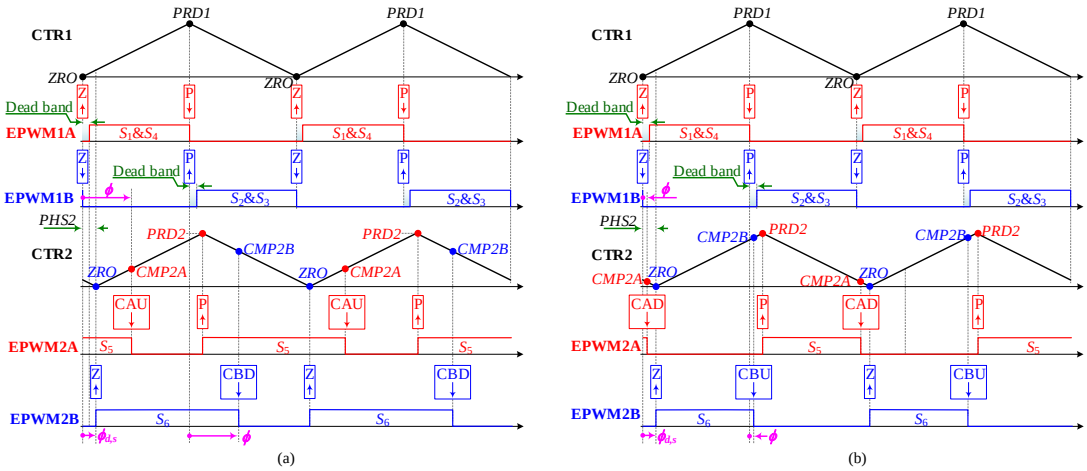

Fig. 23. Modulation waveforms based on TMS320F28075 DSP (a) $\phi > \phi_{d,s}$, (b) $\phi \le \phi_{d,s}$. *PRD1* and *PRD2* represent the period registers of the two ePWM modules (ePWM1 and ePWM2), *PHS2* is the phase register of ePWM2, *CMP2A* and *CMP2B* are the counter-compare *A* and *B* registers of ePWM2. CAU indicates the event when the counter *CTR2* equals the active *CMP2A* resister and *CTR2* is incrementing. CAD indicates the event when the counter *CTR2* equals the active *CMP2A* resister and *CTR2* is decrementing. CBU indicates the event when the counter *CTR2* equals the active *CMP2B* resister and *CTR2* is incrementing. CBD indicates the event when the counter *CTR2* equals the active *CMP2B* resister and *CTR2* is decrementing. *Z* and *P* represents the events when the counter equals zero and the period, respectively.

C. Experimental Verifications

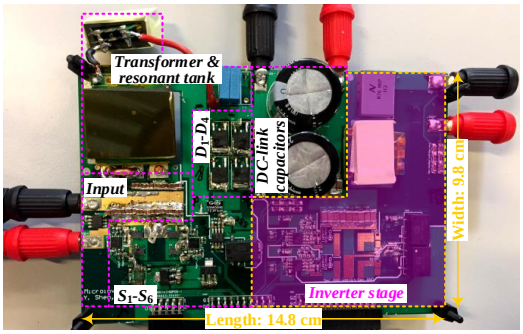

Fig. 24. Photo of the PV microinverter prototype.

TABLE IV
PARAMETERS OF THE CONVERTER PROTOTYPE

Parameters	Values
Input voltage V_{inN}	17-43 V
Nominal input voltage V_{inN}	34 V
Most probable PV (input) voltage range	20-40 V
Output voltage V_o	340-430 V
Rated power P_N	250 W
Transformer turns ratio $n = N_s : N_p$	10
Magnitizing inductance L_m	152 μH
Resonant inductor L_r	34 μH
Resonant capacitor C_r	0.75 nF
Switching frequency f_s	1 MHz
Primary-side switches S_1-S_4	eGaN FET, EPC2029
	$R_{ds,on}$ = 3.2 mΩ
Secondary-side switches S_5-S_6	GaN eHEMT, GS66504B
	$R_{ds,on}$ = 100 mΩ
Rectifier diodes D_1-D_4	SiC Schottky Diode, C3D02060E
DC-link capacitors C_{o1}& C_{o2}	LGJ2E181MELB15, 180 μF/250 V

A 250-W converter prototype with the dimension of 14.8 cm × 9.8 cm × 2 cm has been built up, as shown in Fig. 24. The detailed parameters are listed in Table IV. The steady-state performance at the six operating points (see Table III) are shown in Fig. 25. As can be seen, the steady-state waveforms are in close agreement with the theoretical analysis in Section II.

As stated in Section V-A, there are two control options for the dc-dc stage in microinverter applications, i.e., the dc-dc converter can be used either to achieve the MPPT or to regulate the dc-link voltage. Fig. 26 presents the dynamic experimental waveforms of the proposed converter with the output voltage closed-loop control (i.e., operation mode 2 is enabled in Fig. 22). As can be seen, the output voltage V_o can be regulated to the reference being 340 V after the load changes. A good dynamic performance is achieved: the transition time is less than 10 ms and the voltage overshoot and undershoot are quite small, i.e., less than 5 V.

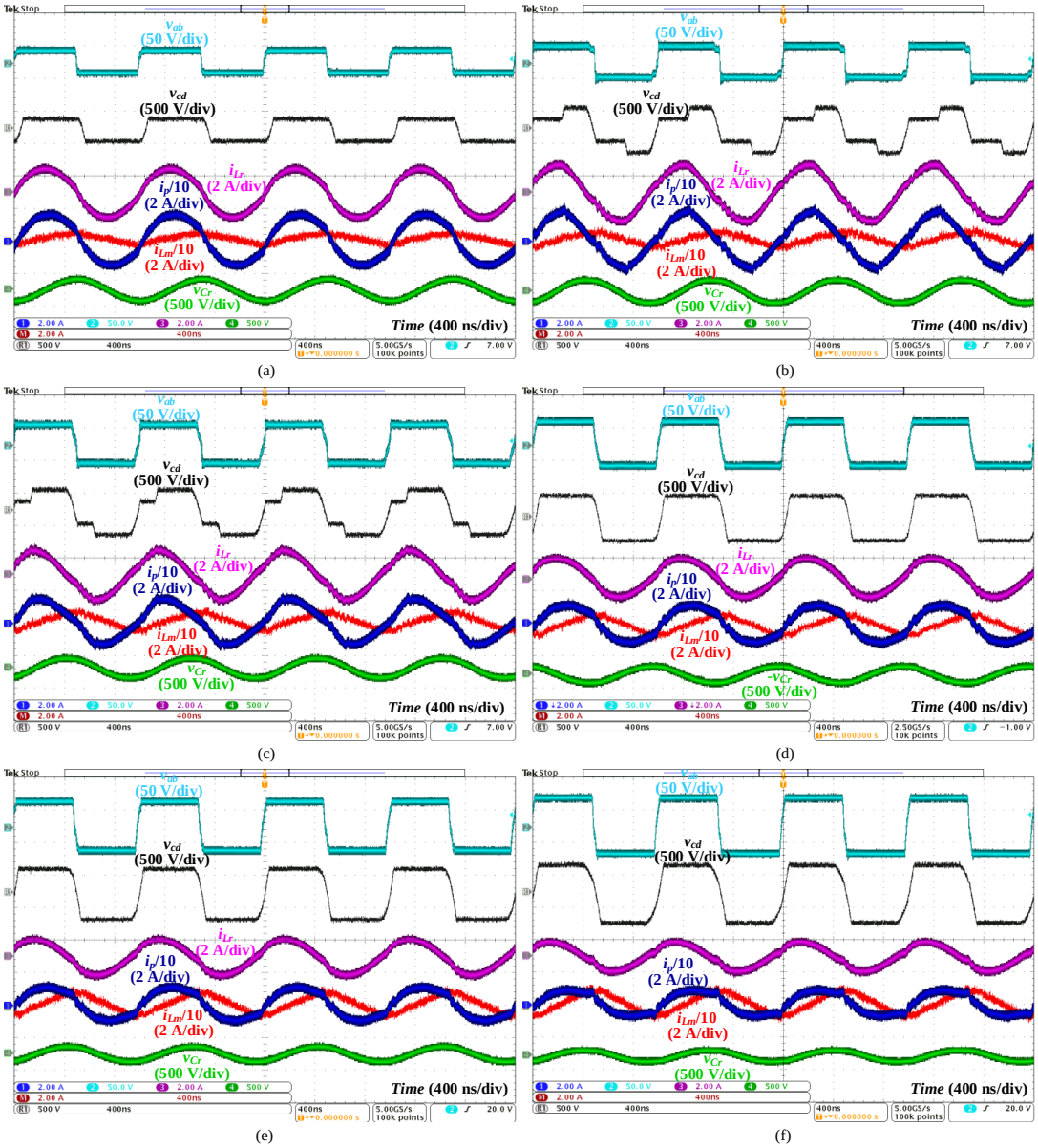

Fig. 25. Steady-state performance of the proposed converter under different conditions (see Fig. 21 and Table III): (a) operating point *A*: V_{in} = 17 V, V_o = 340 V, P_o = 170 W; (b) operating point *B*: V_{in} = 25 V, V_o = 340 V, P_o = 250 W; (c) operating point *C*: V_{in} = 30 V, V_o = 340 V, P_o = 250 W; (d) operating point *D*: V_{in} = 34 V, V_o = 340 V, P_o = 250 W; (e) operating point *E*: V_{in} = 38 V, V_o = 380 V, P_o = 250 W; (f) operating point *F*: V_{in} = 43 V, V_o = 430 V, P_o = 220 W.

Then, the MPPT control mode (i.e., operation mode 1 in Fig. 22) is selected for the proposed dc-dc converter, and the experimental dynamic performance is tested, as shown in Fig. 27. It is seen that the proposed converter with the MPPT control enables the PV simulator to track its maximum power points under different conditions.

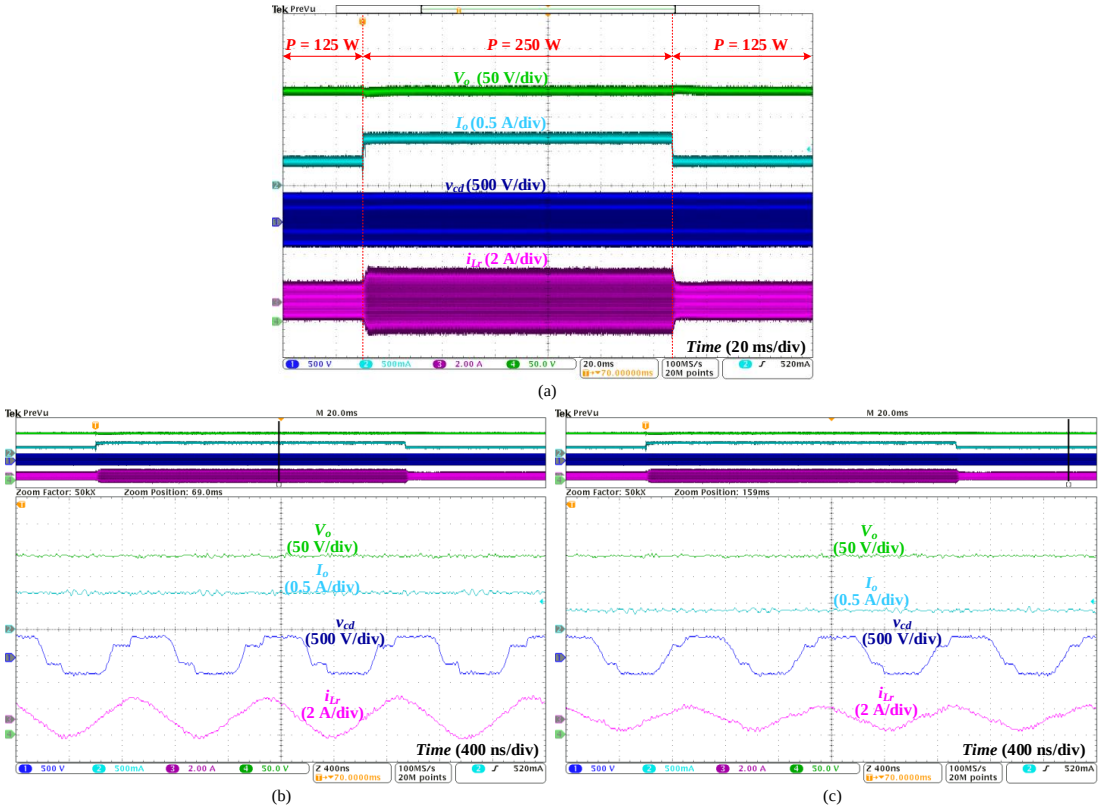

Fig. 26. Transient performance of the proposed converter with the output voltage closed-loop control (the input voltage V_{in} = 30 V and the output voltage reference V_{o_ref} = 340 V): (a) transition between P = 250 W and P = 125 W, (b) zoomed-in waveforms at P = 250 W, (c) zoomed-in waveforms at P = 125 W.

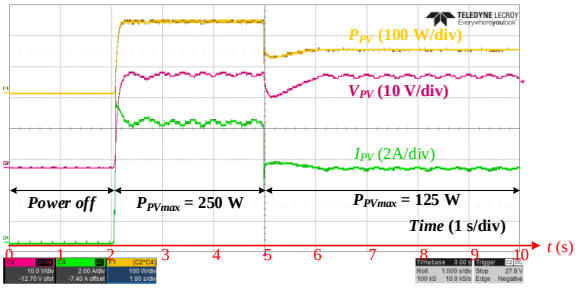

Fig. 27. Measured PV MPPT waveforms of the proposed converter powered by a PV simulator. At t = 2 s, the PV simulator is connected with the converter prototype, and the PV simulator operates at its maximum power point being 250 W after a short transition; at t = 5 s, the maximum power of the PV simulator steps to 125 W, and the MPPT controlled converter allows the PV simulator to track its maximum power point at 125 W.

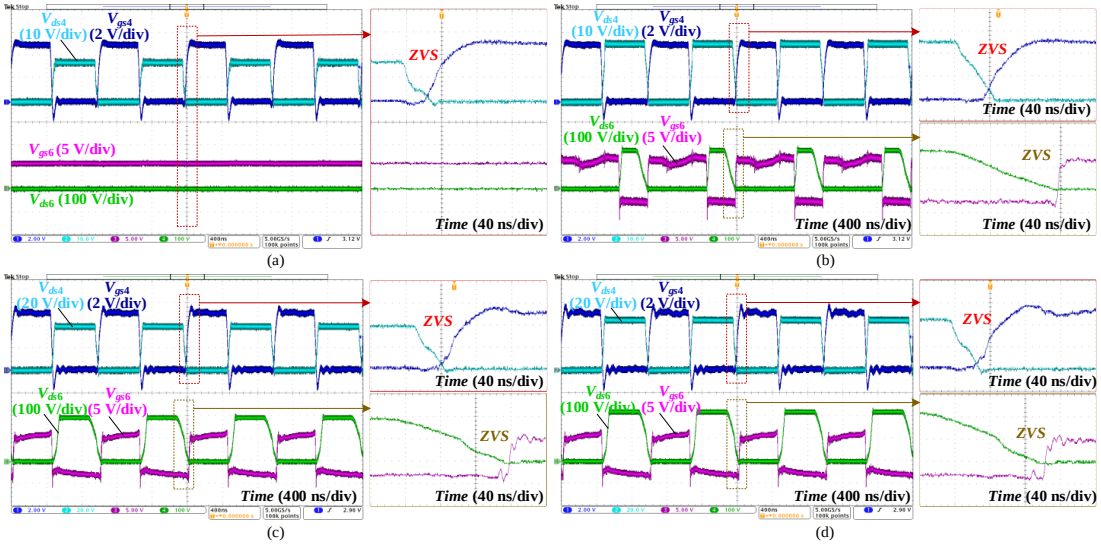

Fig. 28. Soft-switching waveforms of the proposed converter at different operating points: (a) operating point *A:* V_{in} = 17 V, V_o = 340 V, P_o = 170 W; (b) operating point *B:* V_{in} = 25 V, V_o = 340 V, P_o = 250 W; (c) operating point *E:* V_{in} = 38 V, V_o = 380 V, P_o = 250 W; (d) operating point *F:* V_{in} = 43 V, V_o = 430 V, P_o = 200 W.

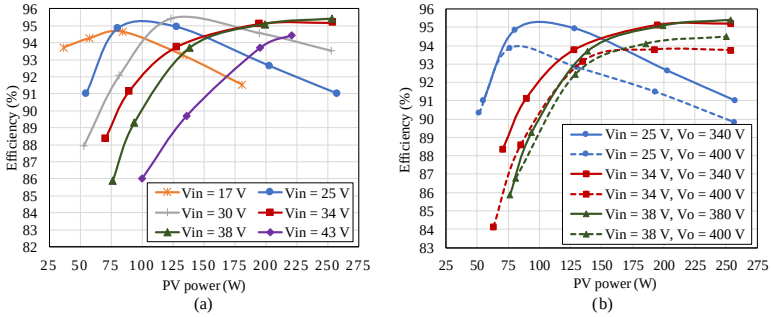

Fig. 29. Measured efficiency of the converter prototype: (a) efficiency curves at different input voltages with the variable dc-link voltage control; (b) efficiency comparison between the variable and fixed dc-link voltage control schemes; solid lines represent the efficiencies with the variable dc-link voltage control and dashed lines are the results with the fixed dc-link voltage control.

The soft-switching performance of the proposed converter is tested at different operating points, as shown in Fig. 28. Due to the symmetry of the topology and the modulation scheme, only the waveforms of S_4 and S_6 are given. As can be seen, the drain-source voltage has fallen to zero before the corresponding gate-source voltage rises to its threshold voltage. That is, the antiparallel diode conducts before the gate signal is applied. Thus, the ZVS-on is achieved, leading to a negligible turn-on loss for the switches.

The measured efficiency curves of the proposed converter with the variable dc-link voltage control (see Fig. 21) at different input voltages are shown in Fig. 29(a). As can be seen, peak efficiencies over 95% are achieved for a wide input voltage range, i.e., V_{in} = 25 V, 30 V, 34 V, 38 V and 43 V. The measured full-load (250-W) efficiency increases with respect to the input voltage. This is due to the fact that the RMS currents and conduction losses reduce as the input voltage rises. When the proposed converter is controlled to have a constant dc-link (output) voltage 400 V, the efficiency is measured at different input voltages V_{in} = 25 V, 34 V and 38 V, as shown in Fig. 29(b). It can be seen that the variable dc-link voltage control enables a significant efficiency improvement for the proposed converter. Moreover, the proposed variable dc-link voltage control allows the converter to cope with a more wide input voltage range $V_{in} \in$[17 V, 43 V] than the conventional fixed dc-link voltage control ($V_{in} \in$[20 V, 40 V]).

The power losses of the main components are calculated at different input voltages and control schemes, as shown in Fig. 30. Overall, the power semiconductors devices (S_1-S_4, S_5-S_6, D_1-D_4) and magnetic components (transformer T_x and resonant inductor L_r) represent the major power loss sources. The power losses of S_1-S_4, S_5-S_6, D_1-D_4 and L_r decline with respect to the increase of V_{in}, whereas the power loss of T_x rises due to the increased core loss at a higher input voltage V_{in}. Meanwhile, it is seen from Fig. 30 that the power losses of D_1-D_4 become higher with the variable dc-link voltage control; it is because D_1-D_4 suffer from a higher rectifier current in comparison with the fixed dc-link voltage (V_o = 400 V) control. Nevertheless, the new control scheme enables to reduce the power losses of other main components S_1-S_4, S_5-S_6, T_x, and L_r. Therefore, higher power conversion efficiencies can be achieved for the proposed converter.

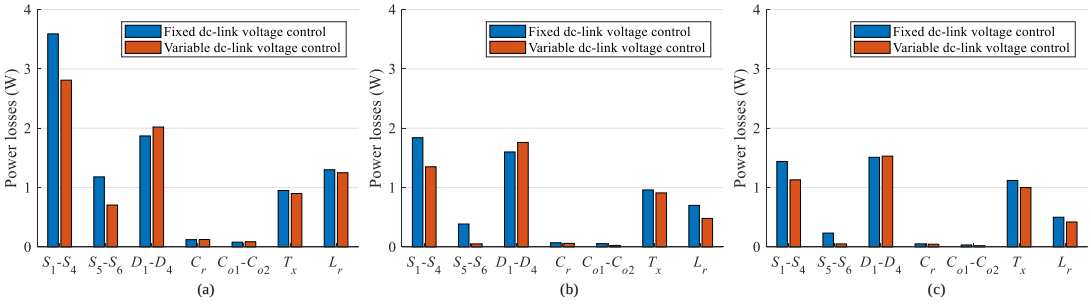

Fig. 30. Power loss breakdown of the proposed converter with different input voltages and control schemes. (a) V_{in} = 25 V, P = 250 W. (b) V_{in} = 34 V, P = 250 W. (c) V_{in} = 38 V, P = 250 W.

VI. CONCLUSION

In this paper, a new dual-mode rectifier based series resonant dc-dc converter is proposed for PV microinverter applications. The modulation, operation principles, and key characteristics are analyzed. A detailed power loss modeling and design optimization of main components are performed, and a variable dc-link voltage control scheme is introduced to the proposed converter. A 1-MHz

250-W converter prototype is tested and the experimental results have verified the theoretical analysis. The proposed converter with the variable dc-link voltage control can cope with a wide input voltage range, e.g., from 17 V to 43 V. The active switches and diodes can achieve ZVS-on and ZCS-off, respectively. Compared with the conventional constant dc-link voltage control, the proposed variable dc-link voltage control enables a remarkable efficiency improvement. High power conversion efficiencies (peak efficiency = 95.5 %) can thus be achieved over the wide input voltage range from 17 V to 43 V, as tested on the 250-W prototype. Therefore, the proposed topology is a promising converter candidate for PV microinverter systems.

ACKNOWLEDGMENT

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APPENDIX

The secondary and primary transformer RMS currents are expressed as

$$\begin{cases} I_{Lr,rms} = \dfrac{\sqrt{A_2^2(\sigma - \sin\sigma\cos\sigma) + A_1^2(\phi - \sin\phi\cos\phi)}}{\sqrt{2\pi}} \\ I_{p,rms} = \dfrac{V_o}{2\sqrt{3\pi}mGZ_r}\ 6\pi\left[(\alpha-\sigma)^2 - \phi^2\right] + 3\pi^2(-\alpha+\sigma+\phi) - 4(\alpha-\sigma)^3 + 4\phi^3 + \pi^3 \\ \quad + \sqrt{\dfrac{3}{\pi}}\left(\begin{array}{l} mA_2^2\sigma GZ_r \,/\, V_o + A_1\left[Gmr_1(\phi - \sin\phi\cos\phi) + 4\sin\phi + 2(\pi - 2\phi)\cos\phi - 2\pi\right] \\ \quad + A_2\left[2(-2\alpha + 2\sigma + \pi)\cos\sigma - \sin\sigma(A_2Gm\cos\sigma Z_r \,/\, V_o + 4) - 2(\pi - 2\alpha)\right] \end{array} \right) \end{cases} \tag{39}$$

where $\sigma = \alpha - \phi$.

The resonant current in (8) and (10) can be expanded into its Fourier series:

$$i_{Lr}(t) = \sum_{n=1,3,\ldots} \left[a_n \sin(n\omega_s t) + b_n \cos(n\omega_s t) \right] \tag{40}$$

where

$$\begin{cases} a_1 = \dfrac{1}{\pi}\ A_2[(\alpha-\phi)\cos\delta - \sin(\alpha-\phi)\cos(\alpha+\delta+\phi)] + A_1(\phi - \sin\phi\cos\phi) \\ b_1 = \dfrac{1}{\pi}\ A_2[\alpha\sin\delta + [\cos(\delta+2\phi) - \cos(\delta+2\alpha)]\,/\,2 - \phi\sin\delta] + A_1\sin^2\phi \\ a_n = \dfrac{1}{\pi(n^2-1)}\left(-A_2\left(\begin{array}{l} (n+1)\sin[\delta-(n-1)\alpha] + (n-1)\sin[\delta+(n+1)\alpha] \\ -2[n\sin(\delta+\phi)\cos(n\phi) - \cos(\delta+\phi)\sin(n\phi)] \end{array} \right) + 2A_1[n\sin\phi\cos(n\phi) + \cos\phi\sin(n\phi)] \right),\ n = 3,5,\ldots \\ b_n = \dfrac{1}{\pi(n^2-1)}\left(A_2\left(\begin{array}{l} (n+1)\cos[\delta-(n-1)\alpha] - (n-1)\cos[\delta+(n+1)\alpha] \\ -2[n\sin(\delta+\phi)\sin(n\phi) + \cos(\delta+\phi)\cos(n\phi)] \end{array} \right) + 2A_1[n\sin\phi\sin(n\phi) + \cos\phi\cos(n\phi) - 1] \right),\ n = 3,5,\ldots \end{cases} \tag{41}$$

Then, the RMS value of the n_{th} harmonic of the resonant current can be obtained as

$$I_{Lr,rms,n} = \sqrt{\frac{a_n^2 + b_n^2}{2}} \tag{42}$$

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Paper B

A Series Resonant DC-DC Converter With Wide-Input and Configurable-Output Voltages

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A Series Resonant DC-DC Converter With Wide-Input and Configurable-Output Voltages

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***Abstract*—This paper proposes a new series resonant DC-DC converter with four configurable operation states depending on the input voltage and output voltage levels. It suits well for the DC-DC stage of grid-connected photovoltaic (PV) systems with a wide-input voltage range and different grid voltage levels, i.e., 110/120 V and 220/230/240 V. The proposed converter consists of a dual-bridge structure on the primary side and a configurable half- or full-bridge rectifier on the secondary side. The root-mean-square (RMS) currents are kept low over a fourfold voltage-gain range; The primary-side MOSFETs and secondary-side diodes can achieve zero-voltage switching (ZVS) on and zero-current switching (ZCS) off, respectively. Therefore, the converter can maintain high efficiencies over a wide voltage gain range. A fixed-frequency pulse width modulated (PWM) control scheme is applied to the proposed converter, which makes the gain characteristics independent of the magnetizing inductance and thereby simplifies the design optimization of the resonant tank. The converter topology and operation principle are first described. Then the characteristics, i.e., the dc voltage gain, soft-switching, and RMS currents, are detailed before a performance comparison with conventional resonant topologies is carried out. Furthermore, the design guidelines of the proposed converter are also presented. Finally, the experimental results from a 500-W converter prototype verify feasibility of the proposed converter.**

***Index terms*—DC-DC converter, series resonant converter, reconfigurable structure, wide input voltage range, configurable output voltage.**

I. INTRODUCTION

The deployment of renewable energies, e.g., photovoltaic (PV) and fuel cell, are becoming increasingly popular around the worldwide. For instance, in 2016, the growth in solar PV capacity was larger than any other form of generation; since 2010, costs of new solar PV have come down by 70% [1].

In literature, many different power conversion structures can be found for the grid-connected renewable system, e.g., the single-stage conversion, the two-stage conversion with a pseudo dc-link, and the two-stage conversion [2]-[5]. Fig. 1 shows the typical structure of a two-stage grid-connected renewable energy system [2]-[5]. Conventionally, the galvanic isolation between the renewable energy source and the grid is achieved by placing a bulky line-frequency transformer at the output of the inverter. In medium and low power applications, it has become a trend to include the isolation transformer in the high-frequency dc-dc stage or inverter stage. This way, the isolation transformer volume can be shrunk significantly, and it can also help to eliminate the leakage current of PV panels [3], [4].

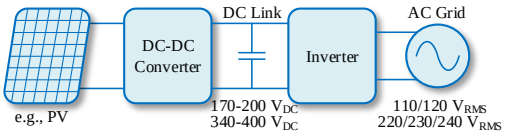


Fig. 1. Structure of a two-stage grid-connected renewable energy system [2]-[5].

Renewable energy sources, e.g., PV and fuel cell, feature a wide range of output voltage. Thus, the interface dc-dc converter should be capable of maintaining high efficiency over a wide input voltage range [6]-[7]. Meanwhile, there are two different mains voltage levels, e.g., 110 V/120 V and 220 V/ 230 V/240 V, in different countries [8]. When connecting to a 220/230/240-V grid, the inverter typically has a dc-link voltage of 340-400 V. However, for a 110/120-V grid, it is preferable that the dc-link voltage is halved, i.e., 170-200 V; this way, the reduced voltage and increased modulation index could help to minimize the switching loss and output current harmonics of the inverter [9], [10]. Therefore, the dc-dc converter should also be able to configure its output voltage flexibly, e.g., either 340-400 V or 170-200 V.

Traditional forward/flyback converters with snubbers are simple in topology, but the voltage stress of the primary switches is high and thus low-voltage MOSFETs with low on-resistances cannot be used [6], [11], [12]. In the phase-shift full-bridge dc-dc converter, the primary switches can achieve zero-voltage-switching (ZVS); however, it suffers from great challenges when operating in a wide voltage gain range, e.g., the narrow ZVS range for the lagging leg switches, duty cycle loss, large circulating current, and voltage spikes across the output diodes [13], [14].

Since 2003, the LLC resonant converter has gained an increasing attention and has been widely adopted by industries

due to its excellent performance in efficiency and power density [15]-[17]. Nevertheless, it is not able to handle a wide range of input voltage; otherwise, the switching frequency variation will be considerably large, and the transformer size and the conduction loss will increase significantly [18], [19]. In order to extend the input voltage range, many hybrid control schemes and resonant circuit topologies have been proposed [20]-[24]. In [20], a hybrid control combining the pulse-frequency modulation (PFM) and phase-shift pulse-width modulation (PS-PWM) is employed to the full-bridge LLC resonant converter; the efficiency performance is improved over a wide input range, but the control complexity is increased significantly as well. In [21], the bidirectional switch is added to the secondary resonant tank of a full-bridge series resonant dc-dc converter, whereas in [22], a bidirectional switch is placed on the primary side to form a dual-bridge LLC resonant converter. The full-bridge diode rectifier of resonant converters is replaced with a semi-active rectifier in [23]-[24]. All the modified topologies can deal with a wide range of input voltage while maintaining high efficiency; however, it is still difficult to configure their output voltage over a wide range.

Thanks to the electric vehicle industry boom, an increasing number of wide-output dc-dc converters emerge for battery chargers [25]-[30]. Most of the topologies are modified LLC resonant converter by altering the structures of the resonant tank [27], [28] or the output rectifier [29], [30]. This way, high efficiencies can be maintained over a wide output voltage range. However, the input voltages in [25]-[30] are fixed, and these topologies may not maintain high efficiencies when dealing with both wide-input and wide-output voltages.

The main contribution of this paper is that a structure-reconfigurable series resonant dc-dc converter which enables wide-input and configurable-output voltages, is proposed [31]. Both the primary-side inverter unit and secondary-side rectifier unit have two structures, and thus four structure combinations can be obtained. The reconfigurability enables the proposed converter with a fixed-frequency pulse-width modulation (PWM) scheme to achieve low conduction losses over a fourfold voltage gain range (from 0.5 to 2). Moreover, the primary switches and secondary switches/diodes can achieve ZVS-on and zero-current-switching (ZCS) off, respectively. As a result, this converter is able to maintain high efficiencies over a wide input voltage range and at two configurable output voltages. The proposed structure-reconfigurable SRC can be a good candidate for both 110/120-V and 220/230/240-V grid-connected renewable energy systems.

II. Operation Principle of the Proposed Converter

A. Topology and Operation Modes

The proposed universal series resonant dc-dc converter is shown in Fig. 2 [31]. Compared with the conventional full-bridge series resonant converter, two low-voltage switches S_5 and S_6 are inserted between the midpoints N and b, and the rectifier diode D_{o2} is replaced with a low-frequency switch S_{o2}. The voltage stress of S_5 and S_6 is only half of the input voltage, i.e., $V_{in}/2$.

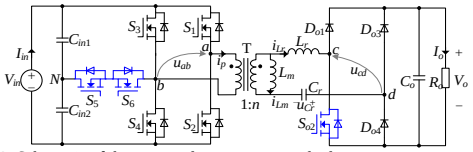


Fig. 2. Schematic of the proposed series resonant dc-dc converter.

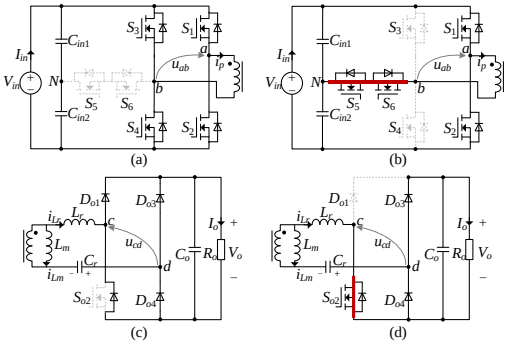


Fig. 3. Four structures in the proposed converter: (a) full-bridge inverter unit on the primary side; (b) symmetrical half-bridge inverter unit on the primary side; (c) full-bridge rectifier unit on the secondary side; (d) asymmetrical half-bridge rectifier (voltage doubler) unit on the secondary side.

There are four configurable structures in the proposed converter, as illustrated in Fig. 3. When S_5 and S_6 are turned off, the primary-side switches S_1–S_4 form a full-bridge inverter unit; when S_5 and S_6 are kept on and S_3 and S_4 are turned off, the two switches S_1–S_2 and the input capacitor C_{in1}–C_{in2} constitute a symmetric half-bridge inverter unit on the primary side. Thus, the amplitude of the voltage across the primary transformer winding, u_{ab}, can be multi-level, i.e., $\pm V_{in}$, $\pm V_{in}/2$ and 0. For the proposed converter, the magnetizing current is used to charge/discharge the parasitic capacitances of primary-side MOSFETs such that a complete ZVS-on can be achieved. To avoid an over-low peak magnetizing current and an incomplete ZVS-on, the voltage level of u_{ab} being 0 is not preferable. Thus, a two-level ($\pm V_{in}$ and $\pm V_{in}/2$) resonant tank voltage u_{ab} is generated by adopting a fixed-frequency PWM scheme, as illustrated in Fig. 4. With this modulation, both the full-bridge inverter state and the symmetrical half-bridge inverter state occur on the primary side during each half switching cycle (see Fig. 4).

With regard to the secondary-side structures, when S_{o2} is turned off, a full-bridge rectifier occurs and the output voltage V_o is equal to the amplitude of u_{cd}; however, when S_{o2} is kept in the on state, an asymmetrical half-bridge rectifier, i.e., a voltage doubler, can be formed and thus, the output voltage V_o is double of the AC amplitude of u_{cd}. This implies that a low-voltage (LV) or high-voltage (HV) output can be configured flexibly by turning off or turning on S_{o2}. Therefore, the two operation states are termed as the LV output mode and HV output mode, respectively.

The key waveforms of the proposed converter in the two operation modes are shown in Fig. 4. It can be noticed that the

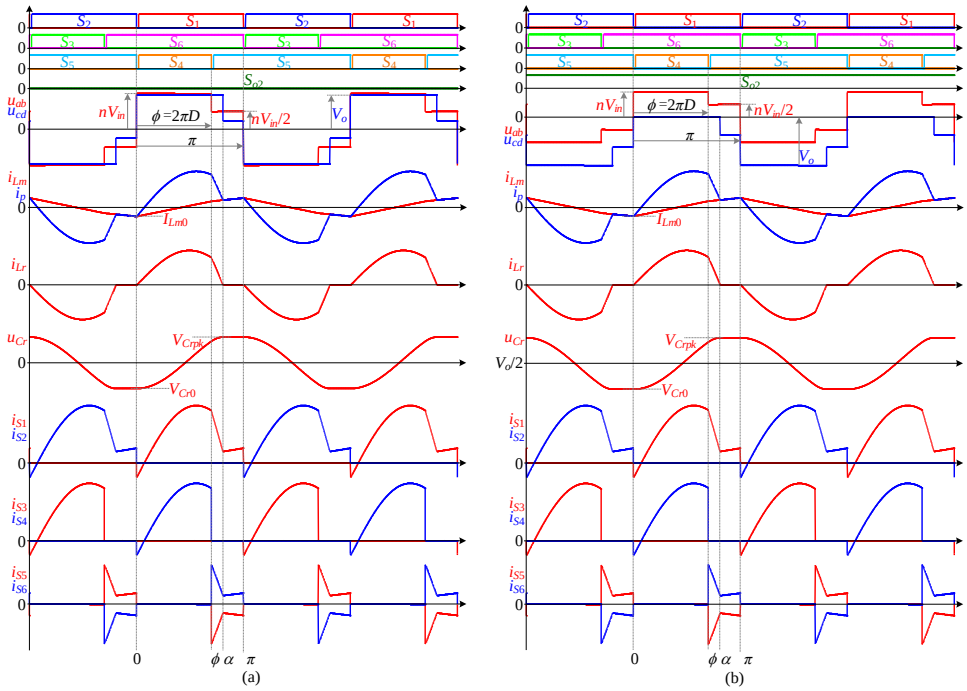


Fig. 4. Key waveforms of the converter operating in (a) the low-voltage (LV) output mode and (b) high-voltage (HV) output mode, where the output rectifier unit is configured as a full-bridge rectifier and an asymmetrical half-bridge rectifier (voltage doubler), respectively.

main difference between the two operation modes lies in the two voltage waveforms u_{cd} and u_{Cr}. In comparison with the LV output mode, there is a voltage offset of $V_o/2$ for u_{Cr} and u_o in the HV output mode. The output voltage in the HV output mode is double of that in the LV mode. Furthermore, both the current ripple frequency and amplitude of the output capacitor C_o are halved in the HV output mode, leading to an equal output voltage ripple in both modes.

B. Operation Principle

To simplify the analysis, the voltages and currents are normalized based on

$$\begin{cases} V_{base} = nV_{in} \\ I_{base} = nV_{in} / Z_r \end{cases} \tag{1}$$

where the characteristic impedance $Z_r = \sqrt{L_r / C_r}$.

The quality factor Q is defined as

$$Q = \begin{cases} \dfrac{Z_r}{R_o} = \dfrac{P_o Z_r}{V_o^2}, & \text{LV output mode} \\ \dfrac{4Z_r}{R_o} = \dfrac{4P_o Z_r}{V_o^2}, & \text{HV output mode} \end{cases} \tag{2}$$

The voltage gain G is defined as

$$G = V_o / (nV_{in}) \tag{3}$$

1) Low-Voltage Output Mode

In the LV output mode, the secondary-side switch S_{o2} is kept off, but its anti-parallel diode D_{o2} is used to form a full-bridge rectifier with other three output diodes D_{o1}, D_{o3}, D_{o4}. The voltage ripple across the resonant capacitor in this mode can be obtain by applying the ampere-second balance principle

$$\Delta V_{Cr} = \pi GQ \tag{4}$$

The initial resonant voltage equals to the valley voltage, i.e.,

$$V_{Cr0} = -\Delta V_{Cr} / 2 = -\pi GQ / 2 \tag{5}$$

Neglecting the deadtime, six stages can be identified over a switching cycle. Due to the symmetry of operation, only the first three stages over the first half switching cycle [0, π] are detailed.

Stage I $\theta \in [0, \phi]$ (see Figs. 4(a) and 5(a)): S_6 has been conducting before S_2 and S_5 are turned off at $\theta = 0$. The negative magnetizing current i_{Lm} begins to charge/discharge the output parasitic capacitors of S_1-S_5, i.e., C_{oss1}-C_{oss5}, such that S_1 and S_4 can achieve ZVS-on. At this stage, the voltage across the transformer, u_{ab}, equals to the input voltage V_{in}, and the inductor current i_{Lr} rises sinusoidally from 0. The output diodes D_{o1} and D_{o4} are conducting, and the resonant tank voltage u_{cd} equals to V_o. Thus, the normalized mathematic equations for the resonant tank can be expressed as

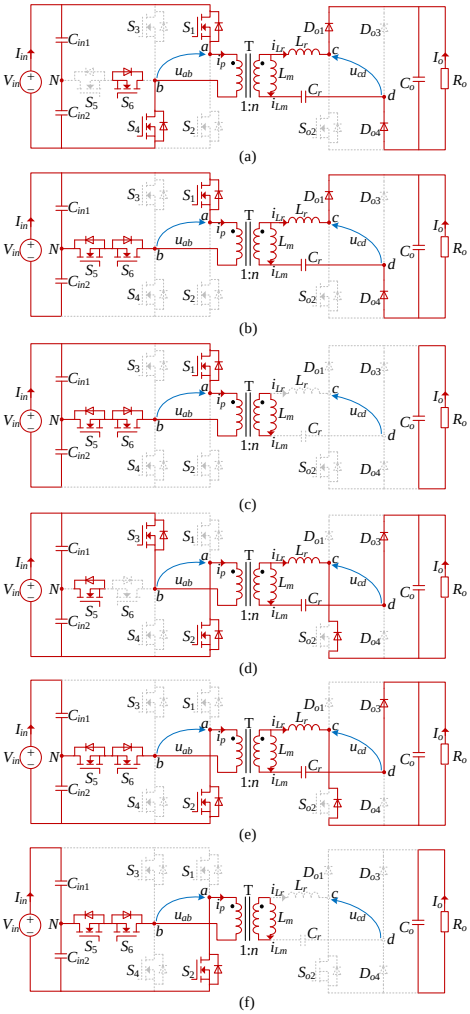


Fig. 5. Equivalent circuit of each switching state in the LV output mode: (a) Stage I [0, ϕ]; (b) stage II [ϕ, α]; (c) stage III [α, π]; (d) stage IV [π, $\pi+\phi$]; (e) stage V [$\pi+\phi$, $\pi+\alpha$]; (f) stage VI [$\pi+\alpha$, 2π].

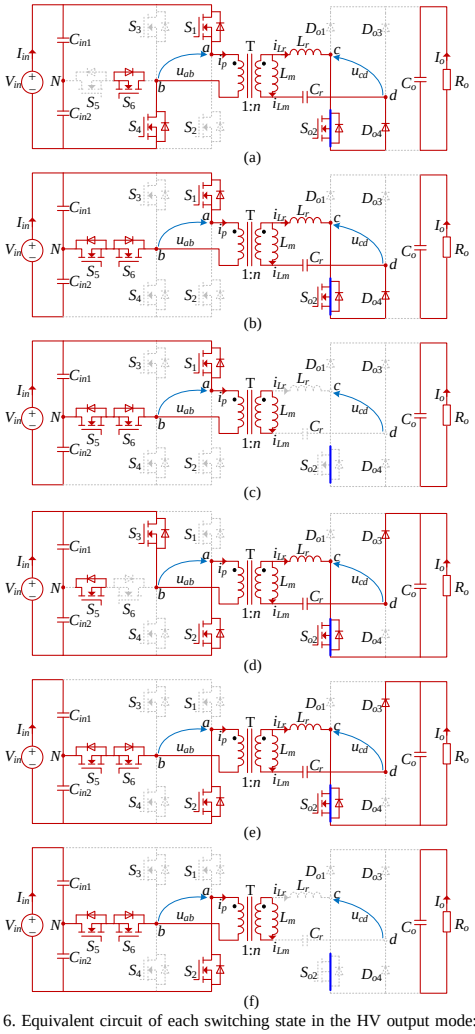


Fig. 6. Equivalent circuit of each switching state in the HV output mode: (a) Stage I [0, ϕ]; (b) stage II [ϕ, α]; (c) stage III [α, π]; (d) stage IV [π, $\pi+\phi$]; (e) stage V [$\pi+\phi$, $\pi+\alpha$]; (f) stage VI [$\pi+\alpha$, 2π];

$$\begin{cases} i_{Lr}(\theta) = r_1 \sin\theta \\ u_{Cr}(\theta) = 1 - G - r_1 \cos\theta \\ i_{Lm}(\theta) = I_{Lm0} + \theta / m \end{cases} \tag{6}$$

where $r_1 = 1 - G - V_{Cr0}$, and the inductors ratio $m = L_m / L_r$.

Stage II $\theta \in [\phi, \alpha]$ (see Figs. 4(a) and 5(b)): At $\theta = \phi$, the switch S_4 is turned off, and thus the positive transformer current i_p charges/discharges C_{oss3}-C_{oss5} such that S_5 achieves ZVS. During this stage, the transformer voltage u_{ab} equals to half of the input voltage, i.e., $u_{ab} = V_{in}/2$. Thus, the inductor current i_{Lr} decreases sinusoidally. The output diodes D_{o1} and D_{o4} are still conducting, and the voltage u_{cd} still equals to V_o. The normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\phi)\cos(\theta-\phi) + r_2 \sin(\theta-\phi) \\ u_{Cr}(\theta) = i_{Lr}(\phi)\sin(\theta-\phi) - r_2 \cos(\theta-\phi) + 1/2 - G \\ i_{Lm}(\theta) = i_{Lm}(\phi) + \theta / (2m) \end{cases} \tag{7}$$

where $r_2 = 1/2 - G - V_{Cr}(\phi)$.

Stage III $\theta \in [\alpha, \pi]$ (see Figs. 4(a) and 5(c)): The inductor current i_{Lr} decreases to 0 at $\theta = \alpha$, and the rectifier diodes D_{o1}

and D_{o4} turn off with ZCS. Due to the unidirectionality of diodes, reverse resonance is not possible. Thus, both the resonant inductor current and the resonant capacitor voltage are kept unchanged. However, the magnetizing inductor is excited by u_{ab}, and therefore i_{Lm} increases linearly, i.e.,

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\alpha) \\ u_{Cr}(\theta) = u_{Cr}(\alpha) \\ i_{Lm}(\theta) = i_{Lm}(\alpha) + \theta / (2m) \end{cases} \tag{8}$$

During all the operation stages, the primary transformer current i_p can be always expressed as

$$i_p = i_{Lr} + i_{Lm} \tag{9}$$

2) High-Voltage Output Mode

In the HV output mode, the secondary-side switch S_{o2} is kept in the on state. The voltage ripple across the resonant capacitor can be calculated as

$$\Delta V_{Cr} = \pi G Q / 2 \tag{10}$$

The voltage offset for the capacitor V_{Cr_dc} is half of the output voltage. Thus, its normalized initial resonant voltage is

$$V_{Cr0} = V_{Cr\_dc} - \Delta V_{Cr} / 2 = G / 2 - \pi G Q / 4 \tag{11}$$

Similarly, six stages are included during each switching cycle by neglecting the deadtime. Due to the symmetry of operation, only the first three stages over the first half switching cycle [0, π] are described. The primary-side switches operate in the same way as in the LV output mode; the only difference occurs on the secondary side which will be elaborated.

Stage I $\theta \in [0, \phi]$ (see Figs. 4(b) and 6(a)): At this stage, u_{ab} equals to V_{in}, S_{o2} and D_{o4} are conducting, and the voltage u_{cd} equals to zero. Thus, the normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = \lambda_1 \sin\theta \\ u_{Cr}(\theta) = 1 - \lambda_1 \cos\theta \\ i_{Lm}(\theta) = I_{Lm0} + \theta / m \end{cases} \tag{12}$$

where $\lambda_1 = 1 - V_{Cr0}$.

Stage II $\theta \in [\phi, \alpha]$ (see Figs. 4(b) and 6(b)): After $\theta = \phi$, u_{ab} equals to $V_{in}/2$, S_{o2} and D_{o4} are still conducting, and the voltage u_{cd} still equals to zero. The normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\phi)\cos(\theta-\phi) + \lambda_2 \sin(\theta-\phi) \\ u_{Cr}(\theta) = i_{Lr}(\phi)\sin(\theta-\phi) - \lambda_2 \cos(\theta-\phi) + 1/2 \\ i_{Lm}(\theta) = i_{Lm}(\phi) + \theta / (2m) \end{cases} \tag{13}$$

where $\lambda_2 = 1/2 - V_{Cr}(\phi)$.

Stage III $\theta \in [\alpha, \pi]$ (see Figs. 4(b) and 6(c)): At $\theta = \alpha$, the inductor current i_{Lr} decreases to 0, and D_{o4} turns off with ZCS. It results in

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\alpha) \\ u_{Cr}(\theta) = u_{Cr}(\alpha) \\ i_{Lm}(\theta) = i_{Lm}(\alpha) + \theta / (2m) \end{cases} \tag{14}$$

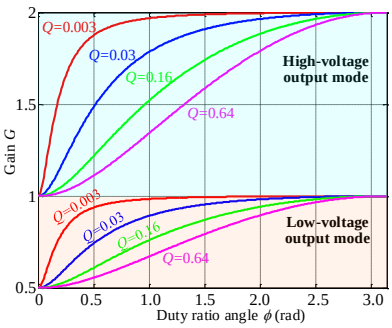


Fig. 7. Characteristics of the voltage gain with respect to the duty ratio angle ϕ and the quality factor Q in the LV and HV output modes.

III. Characteristics of the Proposed Converter

A. DC Voltage Gain

The initial magnetizing current in both the HV and LV modes can be derived as

$$I_{Lm0} = -\frac{\pi + \phi}{4m} \tag{15}$$

By applying the odd symmetry of the resonant voltage and current to (6) – (14), the voltage gain G can be obtained for both modes

$$G = \frac{3\pi Q - 2 + (2 - \pi Q)\cos\phi + K}{8\pi Q} \times \begin{cases} 1, \text{LV output mode} \\ 2, \text{HV output mode} \end{cases} \tag{16}$$

where $K = \sqrt{8\pi Q \sin^2\phi + [3\pi Q + 2 - (\pi Q + 2)\cos\phi]^2}$.

The curves of the voltage gain with respect to the duty ratio angle ϕ for different quality factors are shown in Fig. 7. As can be seen, the voltage gain range is from 0.5 to 2 regardless of the quality factor Q. In addition, it is seen that the dc voltage gain of the proposed converter is independent of the inductors ratio m, which is different from the conventional LLC resonant converter. Thus, the magnetizing inductance can be designed solely based on the ZVS conditions of MOSFETs.

In order to ensure the normal operation of the proposed converter, the peak voltage across the resonant capacitor, V_{Crpk}, cannot be higher than the output voltage V_o. Then the boundary conditions of normal operation can be obtained for both operation modes

$$Q \le \frac{2}{\pi} \Rightarrow \begin{cases} Z_r \le 2V_o^2 / (\pi P_o), \text{ LV output mode} \\ Z_r \le V_o^2 / (2\pi P_o), \text{ HV output mode} \end{cases} \tag{17}$$

Since the output voltage in the HV output mode is double of that in the LV output mode, the boundary conditions in (17) are the same for both modes.

B. Root-Mean-Square Currents

The root-mean-square (RMS) currents flowing through S_3/S_4 and S_5/S_6 in both the LV and HV output mode are calculated by

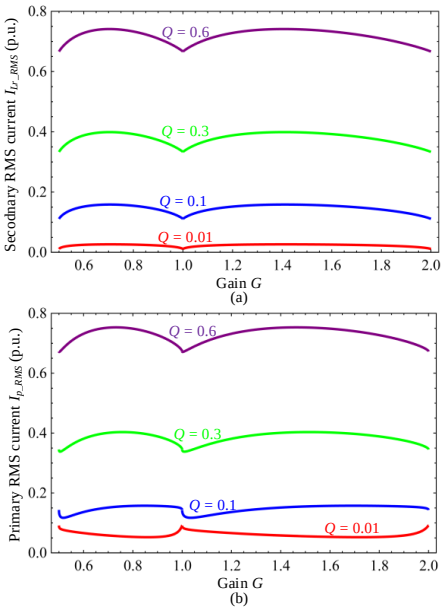


Fig. 8. The RMS currents with respect to the voltage gain G and the quality factor Q. (a) Secondary transformer RMS current; (b) Primary transformer RMS current.

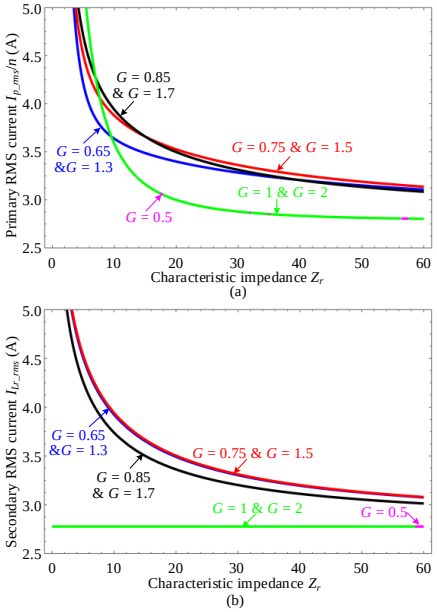


Fig. 9. Full-load RMS currents with respect to the characteristic impedance Z_r.

$$\begin{cases} I_{S34\_rms} = \sqrt{\dfrac{1}{2\pi}\displaystyle\int_0^{\phi} i_{Lp}^2(\theta)\,\mathrm{d}\,\theta} \\ \quad = \sqrt{\dfrac{\left\{\begin{array}{l} 6mI_{Lm0}[m\phi I_{Lm0} + 2mr(1-\cos\phi) + \phi^2] + 2\phi^3 \\ \quad + 3mr(mr\phi - [\sin\phi(mr\cos\phi - 4) + 4\phi\cos\phi]) \end{array}\right\}}{12\pi m^2}} \\ I_{S56\_rms} = \sqrt{\dfrac{1}{\pi}\displaystyle\int_{\phi}^{\pi} i_{Lp}^2(\theta)d\theta} \\ = \sqrt{\dfrac{3m\left\{\begin{array}{l} I_{Lm2}[4Am(1-\cos\delta) - \delta^2] + \delta I_{Lm0}(2mI_{Lm0} + \delta) \\ +2m\delta I_{Lm2}^2 + A[2\delta\cos\delta - \sin\delta(Am\cos\delta + 2) + Am\delta] \end{array}\right\} + \delta^3}{6\pi m^2}} \end{cases} \tag{18}$$

where $I_{Lm2} = i_{Lm}(\alpha)$, $\delta = \alpha - \phi$, and $A = \sqrt{i_{Lr}^2(\phi) + r_2^2}$.

Then the RMS currents flowing through the primary transformer winding and S_3/S_4 can be derived by

$$\begin{cases} I_{Lp\_rms} = \sqrt{2I_{S34\_rms}^2 + I_{S56\_rms}^2} \\ I_{S12\_rms} = I_{Lp\_rms} / \sqrt{2} \end{cases} \tag{19}$$

With regard to the resonant RMS current, it is obtained as

$$I_{Lr\_rms} = \sqrt{\frac{1}{\pi}\int_0^{\delta} i_{Lr}^2(\theta)\,\mathrm{d}\,\theta} = \sqrt{\frac{r_1^2[2\phi - \cos(2\phi)] + A^2[2\delta - \cos(2\delta)]}{4\pi}} \tag{20}$$

However, the mathematical expressions of the RMS currents flowing through D_{o1} and S_{o2} are different in the two modes:

$$\begin{cases} I_{Do1\_rms} = \begin{cases} I_{Lr\_rms}/\sqrt{2}, & \text{LV output mode} \\ 0, & \text{HV output mode} \end{cases} \\ I_{So2\_rms} = \begin{cases} I_{Lr\_rms}/\sqrt{2}, & \text{LV output mode} \\ I_{Lr\_rms}, & \text{HV output mode} \end{cases} \\ I_{Do34\_rms} = I_{Lr\_rms}/\sqrt{2}, & \text{Both modes} \end{cases} \tag{21}$$

Based on (19) and (20), the curves of the primary and secondary transformer RMS currents I_{p_RMS} and I_{Lr_RMS} are plotted in Fig. 8. It can be seen that the variations of the two RMS currents with respect to the voltage gain G are small. This means that the converter can achieve low conduction losses over the entire voltage gain range of [0.5, 2].

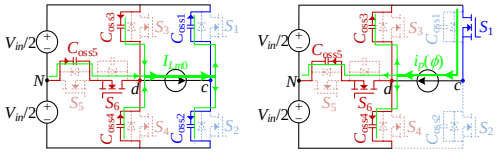
When the load is fixed, the relationship between the primary and secondary RMS currents and the characteristic impedance Z_r can be obtained, as shown in Fig. 9 (at full load 500 W). The RMS currents drops with respect to the increase of Z_r except for the three special cases G = 0.5, 1, and 2 in Fig. 9(b). In order to decrease the conduction losses, the characteristic impedance Z_r should be designed possibly large under the premise of the boundary conditions in (17).

C. Soft-Switching

As aforementioned, the primary-side switches S_1-S_6 can achieve ZVS-on. In practice, however, the realization of ZVS-on requires sufficient charges to completely charge/discharge the parasitic output capacitances of power MOSFETs S_1-S_6. Since the operation of the primary-side inverter unit remains the same for both the LV and HV output modes, the ZVS characteristics in the LV output mode will be analyzed. Also, due to the symmetry of circuit and modulation, only the commutations during the half switching cycle $\theta \in [0, \pi]$ are analyzed, as shown in Fig. 10. In order to quantify the required amount of charges for each commutation mode, detailed state analysis for the half switching cycle $\theta \in [0, \pi]$ is presented in Table I, where C_{oss14} denotes the output capacitance of S_1-S_2, and C_{oss56} represents the output capacitance of S_5-S_6.

TABLE I
REQUIRED MINIMUM CHARGE TO ACHIEVE ZVS FOR DIFFERENT SWITCH LEGS

Commutation mode	Current to achieve ZVS	Charged/discharged capacitor		Initial voltage	Final voltage	Absolute charge variation of a capacitor	Charge variation of a HB/T-type leg	Minimum charge q_{req} for ZVS-ON of all switches
ZVS-on of S_1 and S_4 (see Figs. 4 and 11(a))	I_{Lm0}	HB leg	C_{oss1}	V_{in}	0	$V_{in}C_{oss14}$	$2V_{in}C_{oss14}$	q_{reqI} = max{$2V_{in}C_{oss14}$, $V_{in}(C_{oss14}+0.5C_{oss56})$}
			C_{oss2}	0	V_{in}	$V_{in}C_{oss14}$		
		T-type leg	C_{oss3}	$0.5V_{in}$	V_{in}	$0.5V_{in}C_{oss14}$	$V_{in}(C_{oss14}+0.5C_{oss56})$	
			C_{oss4}	$0.5V_{in}$	0	$0.5V_{in}C_{oss14}$		
			C_{oss5}	0	$0.5V_{in}$	$0.5V_{in}C_{oss56}$		
			C_{oss6}	0	0	0		
ZVS-on of S_5 (see Figs. 4 and 11(b))	$i_p(\phi)$	HB leg	C_{oss1}	0	0	0	0	q_{reqII} = $V_{in}(C_{oss14}+0.5C_{oss56})$
			C_{oss2}	V_{in}	V_{in}	0		
		T-type leg	C_{oss3}	V_{in}	$0.5V_{in}$	$0.5V_{in}C_{oss14}$	$V_{in}(C_{oss14}+0.5C_{oss56})$	
			C_{oss4}	0	$0.5V_{in}$	$0.5V_{in}C_{oss14}$		
			C_{oss5}	$0.5V_{in}$	0	$0.5V_{in}C_{oss56}$		
			C_{oss6}	0	0	0		



(a) (b)

Fig. 10. ZVS mechanism of primary-side switches. (a) ZVS-on of S_1 and S_4 at t = 0 (see Fig.4), (b) ZVS-on of S_5 at $t = \phi / \omega_r$ (i.e., $\theta = \phi$, see Fig. 4).

The ZVS-on of S_1/S_4 and S_5 depends on the currents I_{Lm0} and $i_p(\phi)$, respectively. The inductors ratio m has a direct impact on the peak magnetizing current I_{Lm0} (15), and therefore determines the ZVS realizations of S_1-S_4. The current I_{Lm0} can be assumed to be constant during the deadtime interval t_d which is short compared to the switching period.

In order to achieve the ZVS-on of S_1-S_4, sufficient charge should be provided during the deadtime interval, i.e.,

$$\left|nI_{base}I_{Lm0}\right|t_d = -nI_{base}I_{Lm0}t_d > q_{reqI} \tag{22}$$

Combining (15), (22) and Table I yields the selection criterion for the magnetizing inductance L_m

$$L_m < \frac{t_d n^2 V_{in}(\pi+\phi)}{8\pi q_{reqIII} f_r} \tag{23}$$

where $\phi = \arccos\left(\frac{G[\pi Q(3-4G)-2]+2}{G(\pi Q-2)+2}\right)$.

As illustrated in Table I, the ZVS realization of S_5 and S_6 relies on the currents $i_p(\phi)$ which can be expressed as

$$i_p(\phi) = \frac{n^2 V_{in}}{Z_r} I_{Lm0} + \phi / m + r_1 \sin\phi \tag{24}$$

The ZVS condition of S_5 and S_6 can be derived as

$$i_p(\phi)t_d \geq q_{reqII}$$
$$\Rightarrow Q \geq \frac{4mZ_r q_{reqII} + n^2 t_d V_{in}(\pi-3\phi)}{2\pi G m n^2 t_d V_{in}\sin\phi} - \frac{2(1-G)}{\pi G} \tag{25}$$

Based on (25), the soft- and hard-switching areas of S_5 and S_6 can be obtained, as shown in Fig. 11. It's seen that the hard-switching area is small compared with the soft-switching area.

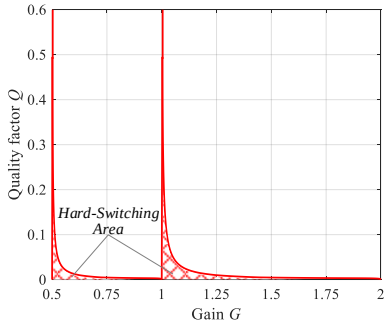


Fig. 11. Soft- and hard-switching areas of S_5 and S_6. The filled area represents the hard-switching range, whereas the rest represents the soft-switching area.

D. Performance Comparison

The voltage gain characteristics of the conventional full-bridge SRC and LLC resonant converter are shown in Fig. 12. For the pulse-frequency-modulated (PFM) SRC, the light-load gain range is narrow even within a wide normalized switching frequency range $f_n \in [1, 5]$, as indicated in Fig. 12(a). The PFM LLC resonant converter has an improved gain characteristics. However, the heavy-load gain range is still narrow (see Fig. 12(b)). In order to have a high full-load voltage gain peak, the characteristic impedance has to be decreased, thereby resulting in a wide frequency range and/or high magnetizing current and conduction losses [18], [19], [28]-[30].

With the fixed-frequency PWM or phase-shift modulation (PSM) control, the gain ranges of the conventional SRC and LLC resonant converter are extended, as shown in Figs. 12(c) and (d). However, the main issue is that the duty cycle variation is wide. When the duty cycle D is small, the conduction losses will rise and the soft-switching condition will be lost because the magnetizing current is reduced significantly in this case, as illustrated in Fig. 13. By contrast, both the RMS current and the magnetizing current of the proposed resonant converter do not vary significantly with respect to the gain G, as illustrated in Figs. 8 and 13. Thus, the ZVS-on of MOSFETs can be achieved and the conduction losses can be maintained low within a wide voltage gain range [0.5, 2]. Furthermore, the voltage gain range

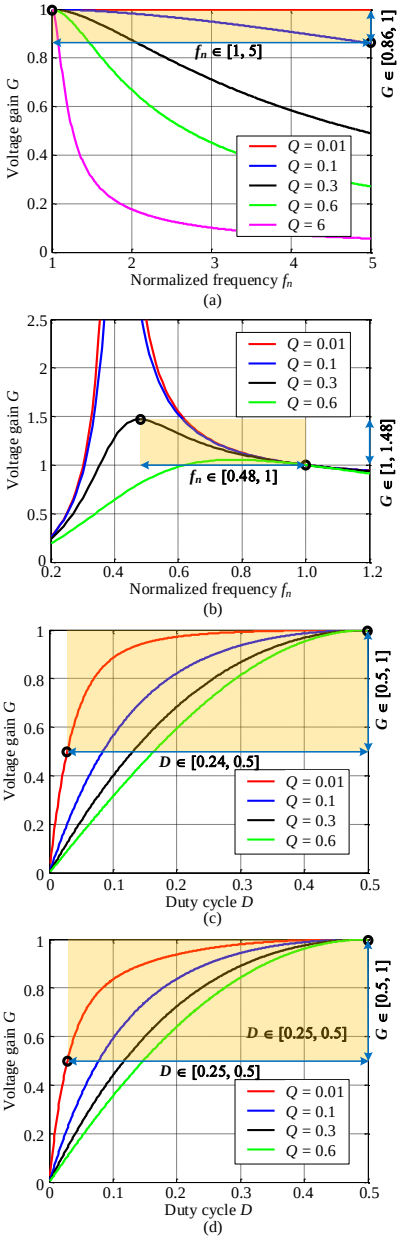


Fig. 12. Voltage gain characteristics of the conventional full-bridge SRC and LLC resonant converter. (a) SRC with PFM control; (b) LLC resonant converter with PFM control; (c) SRC with PWM or PSM control; (d) LLC resonant converter with PWM or PSM control.

of the proposed converter is independent of the inductors ratio m, i.e., the magnetizing inductance L_m does not affect the voltage gain G. Hence, the design of L_m and the resonant tank (L_r and C_r) can be carried out separately, which is easier than the conventional LLC resonant converter.

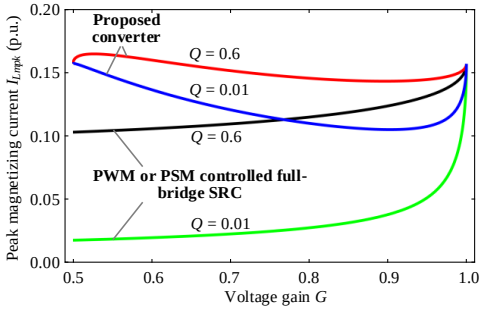


Fig. 13. Peak magnetizing currents with respect to the voltage gain G for the proposed converter and the conventional full-bridge series resonant converter.

E. Design Guideline

Considering the voltage gain range of [0.5, 2] (see Fig. 7) and the specified input and output voltage ranges (e.g., V_{in} ∈ [30 V, 60 V] and V_o = 200/400 V), the transformer turns ratio can be determined by

$$n = N_s : N_p = \frac{V_o}{GV_{in}} = 6.67 \tag{26}$$

In practice, n = 27 : 4 = 6.75 is designed for the transformer.

Unlike the conventional LLC resonant converters, the voltage gain of the proposed converter is independent of the inductors ratio m, and thus, the design of the resonant tank (L_r and C_r) and the magnetizing inductance L_m can be performed separately. As analyzed in Section III-B, the transformer RMS currents decreases with respect to the increase of the characteristic impedance Z_r at a specific load. In order to reduce the conduction losses, Z_r should be designed possibly large on the premise of (17). On the other hand, it is seen from Fig. 9 that the RMS current curves become flat when Z_r exceeds a certain value. However, a large Z_r will lead to a high voltage ripple for the resonant capacitor. Therefore, a trade off should be considered in practice. Nevertheless, the design of L_r and C_r should follow

$$\begin{cases} f_s = \dfrac{1}{2\pi\sqrt{L_r C_r}} \\ Z_r = \sqrt{\dfrac{L_r}{C_r}} \le \min\left(\dfrac{2V_{o,LV}^2}{\pi P_{o,\max}}, \dfrac{V_{o,HV}^2}{2\pi P_{o,\max}}\right) \end{cases} \tag{27}$$

where $P_{o,max}$ is the maximum output power, $V_{o,LV}$ and $V_{o,HV}$ represent the output voltages in the LV and HV output modes. In this paper, the switching frequency f_s = 100 kHz, $P_{o,max}$ = 500 W, $V_{o,LV}$ = 200 V and $V_{o,HV}$ = 400 V. Substituting the specifications to (27) and considering the availability of discrete resonant capacitors yield L_r = 38.4 μH and C_r = 66 nF.

As aforementioned, the magnetizing inductance affects the ZVS conditions of primary-side switches. A smaller magnetizing inductance facilitates the ZVS realization of S_1-S_4,

TABLE II
CONVERTER PARAMETERS

Description	Symbol	Parameter
Input voltage	V_{in}	30–60 V
Output voltage	V_o	200/400 V
Switching frequency	f_s	100 kHz
Rated power	P_o	500 W
Primary switches	S_1–S_4	IPP023N10N5, TO220
	S_5–S_6	IPP020N06N, TO220
Secondary diodes/switch	D_{o1}, D_{o3}, D_{o4}	STTH3R06, DO201
	S_{o2}	IPW65R110CFD, TO247
Transformer	T	Turns ratio: 4 : 27
		Magnetizing inductance L_m = 450 μH.
Resonant Inductor	L_r	38.4 μH
Resonant capacitor	C_r	66 nF

but it also results in a larger magnetizing (circuiting) current, and higher conduction losses. Therefore, the magnetizing inductance should be designed possibly large under the condition of satisfying the ZVS condition (23).

IV. EXPERIMENTAL VERIFICATIONS

A 500-W converter prototype has been built and its specifications and key parameters are listed in Table II. The full-load (500-W) experimental waveforms of the proposed converter in the LV (V_o = 200 V) and HV (V_o = 400 V) output modes are shown in Figs. 14 and 15, respectively. As can be seen, the steady-state operation matches well with the analysis. The proposed converter can deal with a wide input voltage range (from 30 V to 60 V) in both LV and HV output modes by changing the duty ratio angle ϕ. When the input voltage is between the range of (30 V, 60 V), e.g., V_{in} = 40 V in Figs. 14(b) and 15(b) and V_{in} = 50 V in Figs. 14(c) and 15(c), both the full-bridge and half-bridge states appear on the primary-side inverter unit. In both the LV and HV output modes, the primary-side switches operate in the same way, leading to the same current waveforms. However, the resonant voltage waveforms are different in both modes: u_{Cr} has a dc offset of 200 V in the HV output mode, whereas the offset in the LV output mode is zero. In addition, it can be noticed that there are high-frequency oscillations in u_{cd} when the resonant current i_{Lr} is in the discontinuous mode. The ringing is caused by the resonance between the resonant inductor L_r and the resonant capacitor C_r in series with the parasitic capacitors (e.g., the intra-winding capacitance of transformer, output capacitance of rectifier diodes, and stray capacitance of printed circuit board traces).

The measured transformer RMS currents at different input and output voltages are shown in Fig. 16. As can be seen, the RMS currents do not vary significantly with respect to the input voltage. Thus, the conduction loss can be kept low over the entire voltage gain range.

The soft-switching waveforms are shown in Fig. 17. Due to the symmetry of topology and operation, the drain-source and gate driver voltages of S_2, S_4 and S_6 are given. As can be seen, the drain-source voltage has decreased to zero before the corresponding gate driver voltage applies, implying the ZVS-on is achieved for MOSFETs.

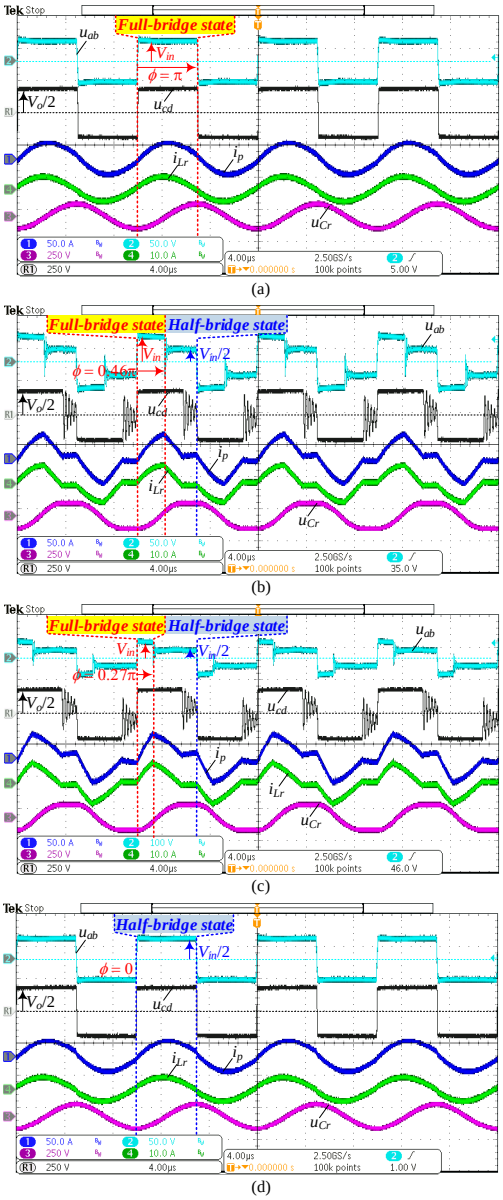
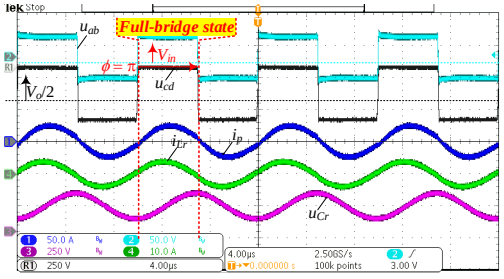
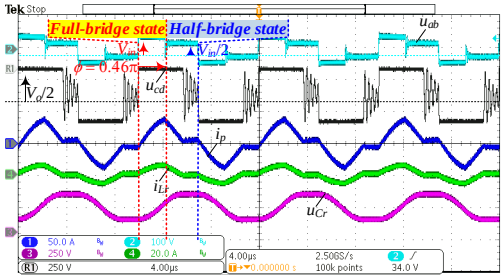


Fig. 14. Full-load experimental waveforms when operating in the LV output mode, i.e., V_o = 200 V. (a) V_{in} = 30 V; (b) V_{in} = 40 V; (c) V_{in} = 50 V; (d) V_{in} = 60 V.

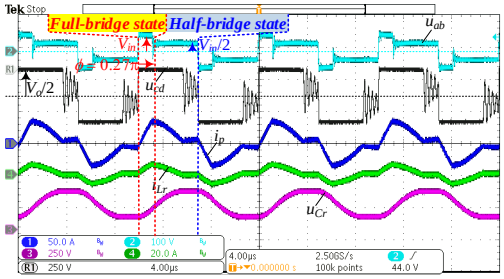
The efficiency performance of the proposed converter is measured under different conditions, as shown in Fig. 18. It indicates that a high-efficiency power conversion can be achieved over the wide voltage gain range from 0.5 to 2. Depending on the input voltage V_{in}, the measured full-load effi-



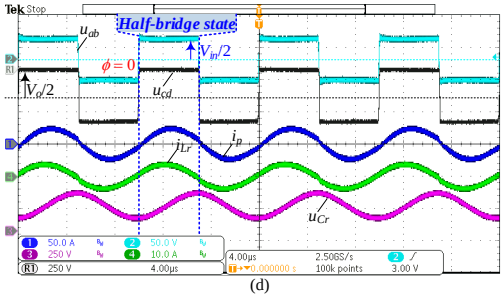
(a)



(b)



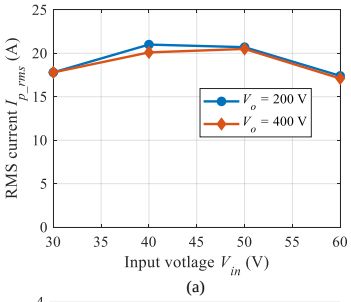
(c)



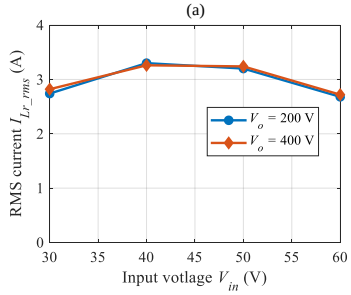
(d)

Fig. 15. Full-load experimental waveforms when operating in the HV output mode, i.e., V_o = 400 V. (a) V_{in} = 30 V; (b) V_{in} = 40 V; (c) V_{in} = 50 V; (d) V_{in} = 60 V.

ciency varies between 92.8 % and 95.4 % for the two output-voltage cases V_o = 200 V and V_o = 400 V. Notably, the efficiency performance at V_{in} = 40 V and V_{in} = 50 V is deteriorated compared with that at V_{in} = 30 V and V_{in} = 60 V.

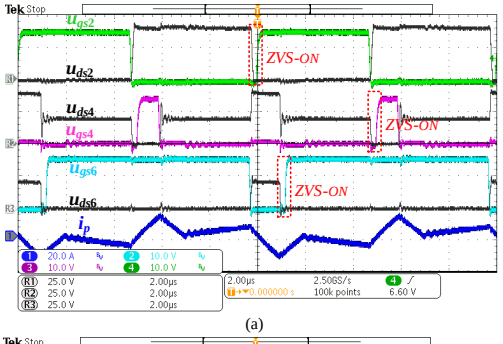


(a)

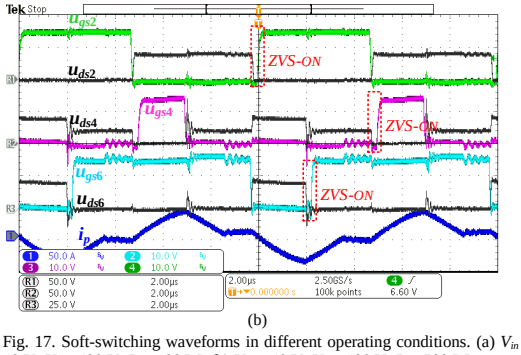


(b)

Fig. 16. Measured transformer RMS currents of the proposed converter at full-load (500-W) for different input and output voltages. (a) Transformer primary-side RMS current; (b) transformer secondary-side RMS current.



(a)



(b)

Fig. 17. Soft-switching waveforms in different operating conditions. (a) V_{in} = 40 V, V_o = 400 V, P = 100 W; (b) V_{in} = 40 V, V_o = 400 V, P = 500 W.

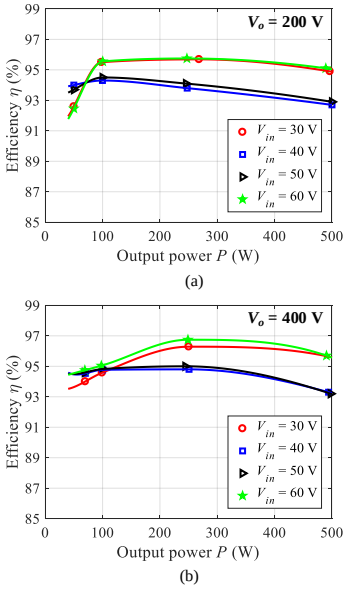


Fig. 18. Efficiency with respect to the output power for different input and output voltages (a) V_o = 200 V; (b) V_o = 400 V.

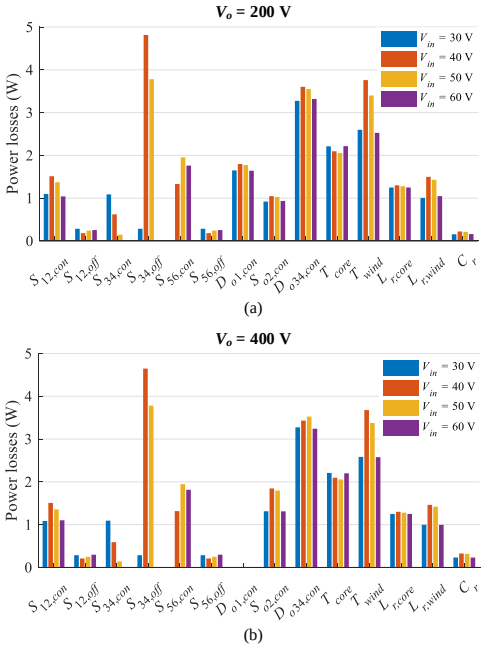


Fig. 19. Power loss breakdown at different input and output voltages (a) V_o = 200 V; (b) V_o = 400 V.

A power loss breakdown of the proposed converter is performed at different input and output voltages, as shown in Fig. 19. It is seen that the power semiconductor devices and magnetic components are the main power loss sources. The power loss distribution in the two cases V_o = 200 V and V_o = 400 V are almost the same except for D_{o1} and S_{o2}. Therefore, the measured full-load efficiencies at V_o = 200 V and V_o = 400 V are close in Figs. 18(a) and (b). However, as the change of the input voltage V_{in}, e.g., V_{in} deviates from 30 V and 60 V, the conduction losses of components become higher. Notably, the off-switching losses of S_3 and S_4 are significantly increased at V_{in} = 40 V and V_{in} = 50 V, which results in the measured efficiency drop in Figs. 18(a) and (b).

The issue of high off-switching losses can be alleviated by taking the following precautions:

1) minimize the loop inductance by introducing the capacitive layout [32] and/or replacing the in-line packages (e.g., TO220 with lead inductance of 10-20 nH [32]) with low-inductance packages (e.g., DPAK with a parasitic inductance of 2.5 nH, LGA with a parasitic inductance of 0.2 nH, GaN/px with a parasitic inductance of 0.2 nH [33]) for the primary-side switches;

2) reduce the turn-off gate resistance, increase the current capability of gate driver and/or use wide-bandgap (WBG) switches (e.g., GaN eFET [34] and GaN eHEMT [35]) to enable faster turn-off and lower off-switching losses.

V. Conclusion

In this paper, a new fixed-frequency PWM controlled structure-reconfigurable SRC is proposed for renewable energy systems. The operation principle and characteristics are analyzed in detail. The experimental results from a 500-W converter prototype are presented to verify the theoretical analysis. The proposed converter is able to deal with a wide input voltage range and to configure its output voltage to be compatible with both the 110/120-V and 220/230/240-V grid voltage levels. The primary switches can achieve ZVS-on and the secondary diodes turn off under ZCS. In addition, the conductions losses do not vary significantly despite the fourfold (from 0.5 to 2) voltage gain range. Therefore, the proposed converter can maintain high efficiencies over a wide voltage gain range.

Nevertheless, the primary switches S_3-S_4 suffer from a high turn-off current when the converter operates in the middle area of the gain range. Therefore, the precautions of lowering the switching loop inductance and enabling fast turn-off of switches should be taken to reduce the turn-off losses.

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Paper C

Thermal Resistance Modelling and Design Optimization of PCB Vias

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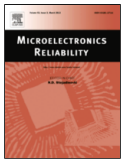

Thermal resistance modelling and design optimization of PCB vias

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ABSTRACT

Various reference printed circuit board (PCB) thermal designs have been provided by semiconductor manufacturers and researchers. However, the recommendations are not optimal, and there are some discrepancies among them, which may confuse electrical engineers. This paper aims to develop an analytical thermal model for PCB vias, and further to find the optimal design for thermal resistance minimization. Firstly, the vertical thermal resistance of a PCB via array is analytically modelled. Then the dependence of the thermal resistance on multiple design parameters is analysed, and the optimal via diameter is found for different PCB specifications. Finally, the developed thermal model and optimal trajectory are verified by computational fluid dynamics (CFD) simulations and experiments.

1. Introduction

The volume of modern power semiconductor devices (e.g., GaN transistors) is shrinking to achieve high power density, low parasitic inductance, and low power losses [1]. However, thermal management has been identified as the main barrier for further power density increase [2]. The heat generated inside the miniaturized semiconductors must be effectively dissipated to the ambient; otherwise, the high junction and board temperatures may cause serious reliability issues to the semiconductor, solder, thermal grease, and printed circuit board (PCB) [3–5].

In medium power applications, the surface-mounted devices (SMDs) are normally cooled by a heatsink attached to the PCB, where the thermal via array provides an effective thermal path for the heat transfer [6,7]. Many reference thermal designs can be found from device manufacturers' websites [8–11]. However, there are several problems:

1) the design guidelines recommended by the manufacturers are not optimal, and are for specific cases only [9];
2) depending on manufacturers, the thermal design guidelines are not in consistence; for instance, the thermal via diameter should be designed large to reduce thermal resistance according to [10]; however, [11] gives an opposite via diameter recommendation;
3) although the computational fluid dynamics (CFD) simulations feature high accuracy, the model generation time and computational cost could be fairly high [8];
4) CFD simulators are expensive and they are not always available for electrical engineers. Therefore, it is necessary to develop an analytical model for a quick design optimization of thermal vias.

Many efforts have been devoted to the thermal design of PCB vias. The research in [12,13] is based on either experimental results or CFD simulations; thus, only some general design guidelines are provided for specific applications. Analytical thermal models of vias are built in [6,14,15]; unfortunately, only partial parameters are analysed, and no optimal via design is derived.

This paper systematically analyses the impact of each parameter on the thermal resistance of PCB vias. Then the optimal via diameter is found with respect to the filler material, via spacing, and plating thickness. Finally, CFD simulations and experiments verify the developed analytical thermal models. The proposed thermal model enables engineers to optimize the PCB via design at lower cost and less time efforts.

2. Analytical thermal modelling of Vias

As aforementioned, in medium power cases, a cluster of small vias are normally used to transfer heat from the SMD to the heatsink, as shown in Fig. 1(a). Two simple via patterns (cf. Fig. 1(b) and (c)) can be designed for a PCB pad with the dimension of l (length) × w(width) × t(thickness). The number of copper layers is defined as N_l, and then the number of FR4 layers is $N_l - 1$. For the geometric parameters of the plated through holes (PTHs), i.e., the vias, the outer diameter is defined as ϕ, the copper plating thickness is represented as t_{PTH}, and the via-to-via spacing is denoted as p.

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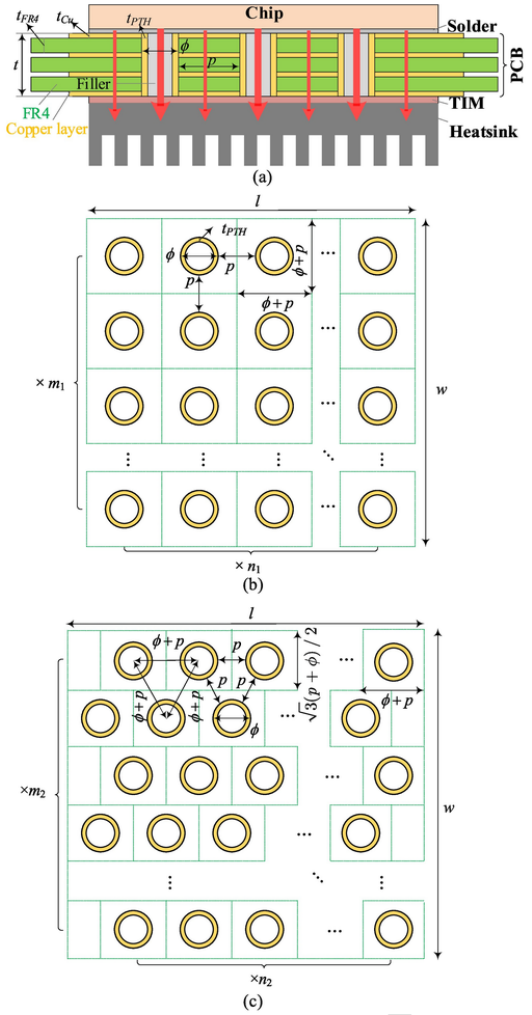

Fig. 1. (a) Vertical structure of a multilayer PCB with plated through holes (vias). Top view of a via array in (b) pattern I and (c) pattern II.

The heat flow through the copper barrels are much more significant than the heat spreading in the lateral direction, so it is assumed that heat transfers in the vertical direction only. Thus, the via arrays in patterns 1 and 2 can be divided into $m_1 \times n_1$ and $m_2 \times n_2$ cells, respectively. It can be seen from the horizontal cross section of the via array that the basic via unit in pattern I is a square of $(\phi + p) \times (\phi + p)$, whereas that in pattern II is rectangular with a dimension of $[\sqrt{3}(\phi + p)/2] \times (\phi + p)$. That is, there are dense vias in pattern II.

For each cell, the one-dimensional (1-D, vertical) thermal resistance can be calculated as $\Theta_{cell} = \Theta_{barrel} // \Theta_{filler} // (\Theta_{Cu} + \Theta_{FR4})$, where Θ_{barrel}, Θ_{filler}, Θ_{Cu} and Θ_{FR4} represent the vertical thermal resistances of the barrel, filler, copper layers and FR4 layers, respectively. To facilitate the analysis, the thermal resistance of via array is normalized based on $t/(k_{FR4}lw)$ which represents the thermal resistance of a pure FR4 board with a dimension of $l \times w \times t$. Then, the normalized thermal resistance of a via array in patterns I and II can be obtained as

$$\Theta_{via,n} = \frac{\Theta_{via}}{t/(k_{FR4} l w)} = \begin{cases} \dfrac{4(p+\phi)^2 k_{FR4}}{\underbrace{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH})}_{\text{plated copper in via}} + \underbrace{\pi k_{filler}(\phi - 2t_{PTH})^2}_{\text{via filler}} + \underbrace{\dfrac{t\left[4p^2 + 8p\phi + (4-\pi)\phi^2\right]}{N_{Cu} t_l / k_{Cu} + (t - N_{Cu} t_l)/k_{FR4}}}_{\text{copper and FR4 layers}}}, & I \\ \dfrac{2\sqrt{3}(p+\phi)^2 k_{FR4}}{\underbrace{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH})}_{\text{plated copper in via}} + \underbrace{\pi k_{filler}(\phi - 2t_{PTH})^2}_{\text{via filler}} + \underbrace{\dfrac{t\left[2\sqrt{3}(p+\phi)^2 - \pi\phi^2\right]}{N_{Cu} t_l / k_{Cu} + (t - N_{Cu} t_l)/k_{FR4}}}_{\text{copper and FR4 layers}}}, & II \end{cases} \quad (1)$$

With the same area for the via array, the thermal resistance of pattern II is about $\sqrt{3}/2 = 86.6\%$ of that in pattern I. The dependence of $\Theta_{via,n}$ on the number of layers N_l, copper thickness t_l, and PCB thickness t is shown in Fig. 2. As can be seen, the parameters, N_l (the number of copper layers), t_l (the thickness of a copper layer) and t(PCB thickness), have a negligible impact on the normalized thermal resistance, which implies that the term of the copper and FR4 layers in the denominator of Eq. (1) have a much higher value compared to the vias (including the plated copper and via filler). That is, the heat is mainly transferred through the vias. Therefore, the term of the copper and FR4 layers in the denominator of Eq. (1) can be neglected without scarifying accuracy, i.e.,

$$\Theta_{via,n} \approx \begin{cases} \dfrac{4(p+\phi)^2 k_{FR4}}{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH}) + \pi k_{filler}(\phi - 2t_{PTH})^2}, & I \\ \dfrac{2\sqrt{3}(p+\phi)^2 k_{FR4}}{4\pi k_{Cu} t_{PTH}(\phi - t_{PTH}) + \pi k_{filler}(\phi - 2t_{PTH})^2}, & II \end{cases} \quad (2)$$

3. Design optimization of vias

Equating the derivative of Eq. (2) as to ϕ to 0 and solving for ϕ yield the optimal via diameter for both patterns, i.e.,

$$\frac{d\Theta_{via,n}}{d\phi} = 0$$
$$\Rightarrow \phi_{opt} = \frac{2t_{PTH}(p + 2t_{PTH})\left(k_{Cu} - k_{filler}\right)}{2t_{PTH}\left(k_{Cu} - k_{filler}\right) - k_{filler} p}, \quad I \& II \quad (3)$$

which enables the via array to achieve the minimum thermal resistance.

It can be seen from Eq. (3) that the thermal resistance increases with respect to the rise of via spacing p. That is, p should be designed as small as possible. However, the allowed minimum p depends on PCB manufacturers, and is generally 8 mil (0.2 mm) in practice. In this case, the dependence of the thermal resistance on the via diameter ϕ and the filler material is illustrated in Fig. 3(a) and (b). For each filler material, there is an optimal via diameter which enables the via array to achieve the minimum thermal resistance, as indicated by the red lines in Fig. 3(a) and (b). The optimal via diameter increases with respect to the filler thermal conductivity, as illustrated in Fig. 3(c). This figure could

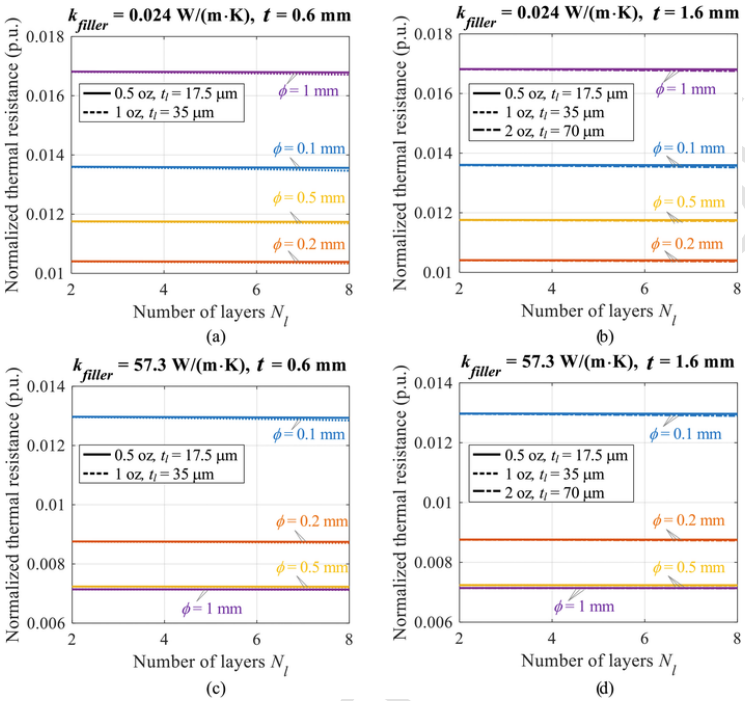

Fig. 2. Dependence of the normalized thermal resistance on the number of layers N_l, copper thickness t_l, and PCB thickness t with different filler materials. (a) k_{filler} = 0.024 W/(mK), t = 0.6 mm; (b) k_{filler} = 0.024 W/(mK), t = 1.6 mm; (c) k_{filler} = 57.3 W/(mK), t = 0.6 mm; (d) k_{filler} = 57.3 W/(mK), t = 1.6 mm. The thermal resistances are normalized based on $t/(k_{FR4}\, l\, w)$, as illustrated in Eq. (1). "p.u." represents "per unit", meaning the normalized thermal resistance is unitless.

help engineers choose the optimal via diameter in order to minimize the thermal resistances of via arrays. Specifically, when the vias are not filled, the optimal via diameter is about 0.25 mm; if ϕ = 0.8 mm is chosen, then there will be a 44% increase in the thermal resistance. When the vias are filled up with SnAgCu solder (k_{filler} = 57.3 W/mK), then the optimal via diameter is about 0.8 mm; if ϕ = 0.2 mm is chosen, then there will be a 23% increase in the thermal resistance.

4. CFD and experimental verifications

The CFD simulation results of a PCB via array for the DPAK (TO252) package are shown in Fig. 4. The thermal resistance of the PCB pad is significantly reduced from 120.32 K/W (no via) to 1.86 K/W (with vias, ϕ = 0.25). The calculated and simulated results for different via patterns, diameters and filler materials are shown in Fig. 5(a) and (b). As can be seen, there is a good agreement between calculations and simulations. Also, it is seen that a proper design of the vias (i.e., pattern, diameter, filler material, etc.) enables a remarkable thermal resistance reduction. Compared to the reference design provided in [9], the thermal resistance reduction can be up to 62% (from 2.63 K/W [9] to 1 K/W (pattern II, ϕ = 0.6 mm, solder filling)).

An experimental setup has been built, as shown in Fig. 6(a). Each chip generate 2.4-W power loss, and the thermal image of the experimental setup in the steady-state is shown in Fig. 6(b). Without filling, the via diameter of 0.25 mm help the chip achieve the lowest top-case temperature. If the vias are filled up with solder, then the vias of ϕ = 0.8 have the minimum thermal resistance. The trend agrees well with the analyses in Section 3.

5. Conclusion

This paper develops an analytical 1-D thermal resistance model for two patterns of PCB vias. The impact of different design parameters on the thermal resistance is analysed, and an optimal design trajectory is proposed for the thermal resistance minimization of vias. The CFD simulations and experimental measurements agree well with the analytical model. It is concluded that: 1) when the PCB parameters are determined, there exists an optimal via diameter which can achieve the minimum thermal resistance; 2) the via layout of pattern II and solder filling can help to reduce the thermal resistance. The proposed thermal model and trajectory enable engineers to fast and easily optimize the design of PCB vias.

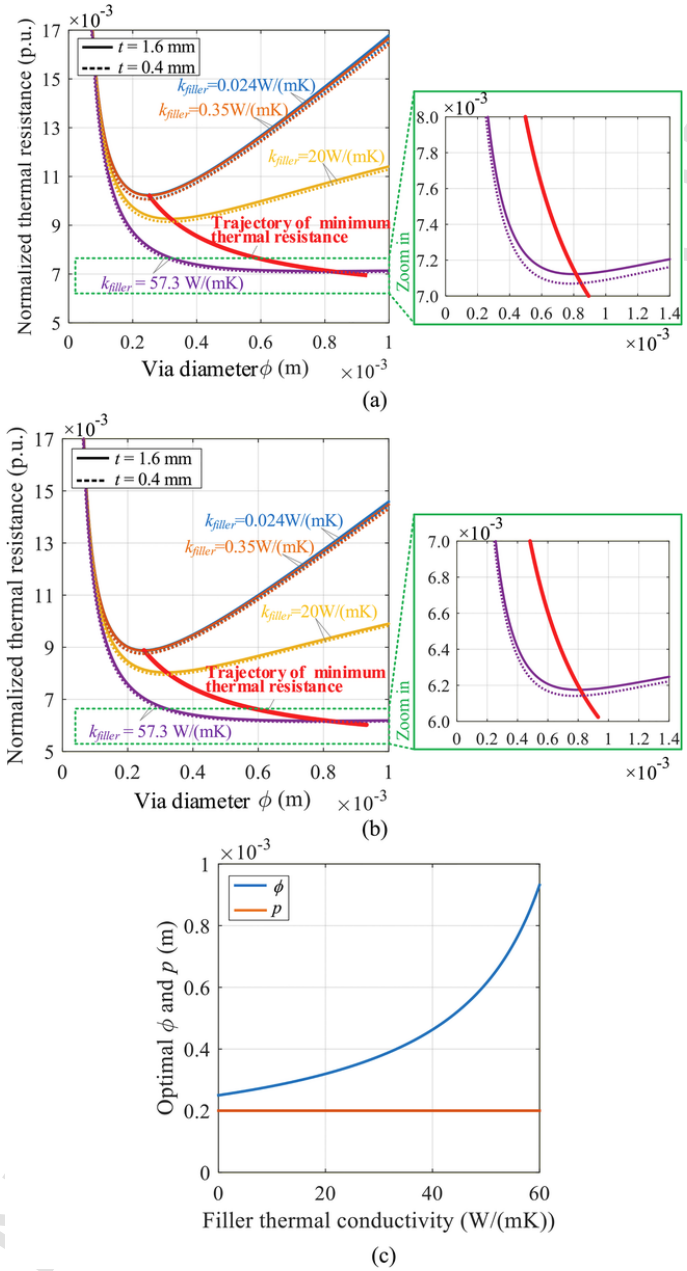

Fig. 3. Dependence of the normalized thermal resistance on the diameter ϕ at different PCB thickness and filler thermal conductivities for (a) pattern I and (b) pattern II. (c) Optimal via diameter and spacing with respect to the filler thermal conductivity: the optimal parameters enable the via array to achieve the minimum thermal resistance.

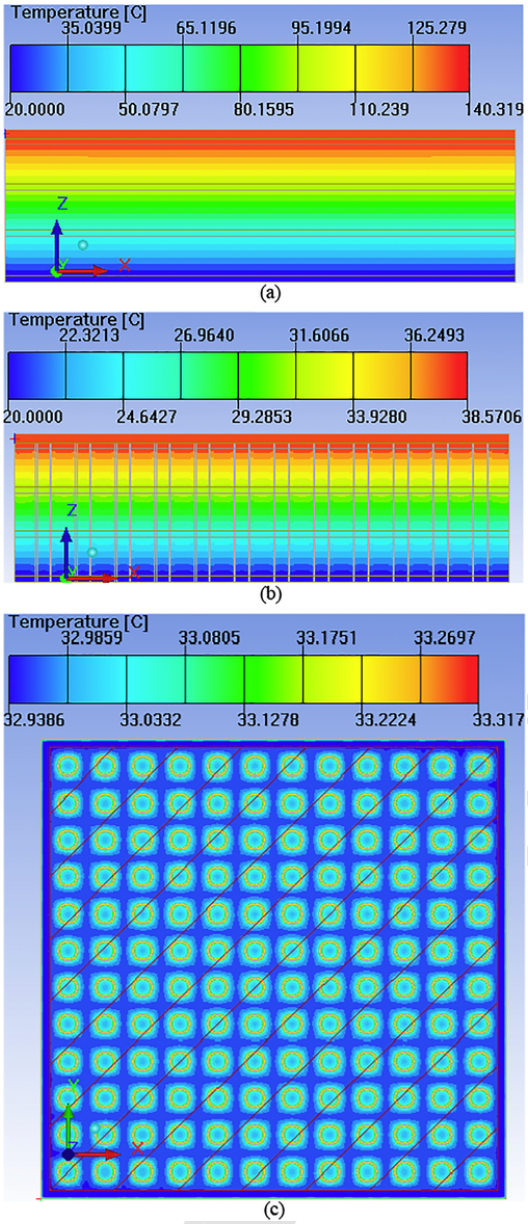

Fig. 4. CFD simulation results of different PCBs. (a) vertical cut plane, 4-layer PCB, thickness: 1.6 mm, 2-oz copper on each layer, no via, power $P = 1$ W; (b) 4-layer PCB, thickness: 1.6 mm, 2-oz copper each layer, via diameter $\phi = 0.25$ mm, power, $P = 10$ W, (c) 4-layer PCB (1.6 mm, 2 oz each layer), $\phi = 0.25$ mm, $P = 10$ W.

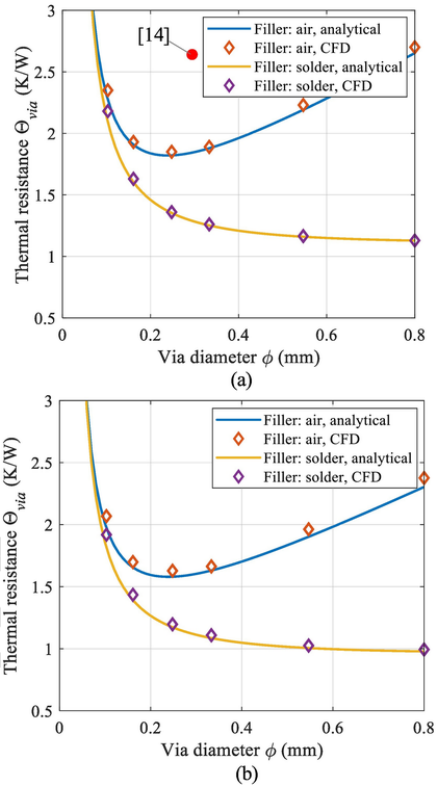

Fig. 5. Comparison between the calculated and simulated thermal resistance of vias with different parameters for the DPAK (TO-252): (a) pattern I; (b) pattern II.

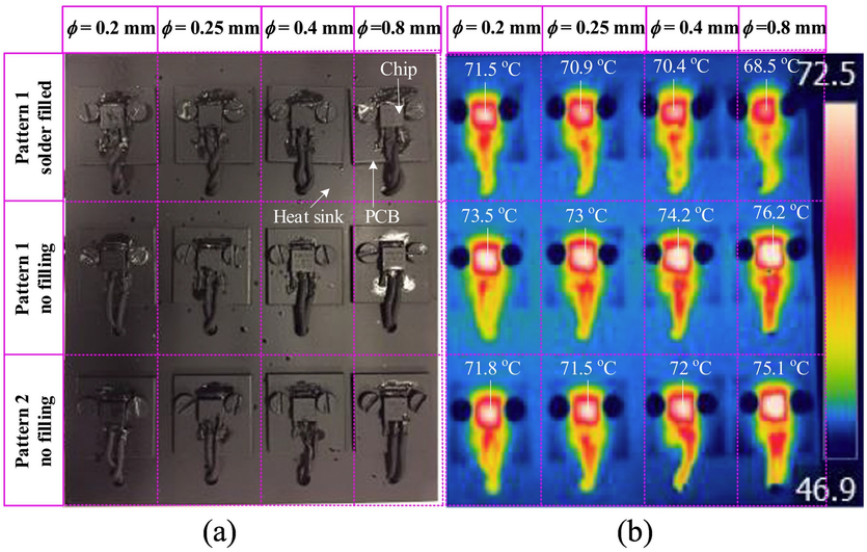

Fig. 6. (a) Photo of the experimental setup: each diode (package: TO252) is attached to a PCB and cooled by the heatsink; (b) thermal image of the experimental setup in steady-state when each diode generates 3-W power loss.

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Paper D

Thermal Modeling and Sizing of PCB Copper Pads

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Thermal Modeling and Sizing of PCB Copper Pads

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***Abstract*—In low power applications, a surface mounted device (SMD) is naturally cooled by attaching to a printed circuit board (PCB) copper pad. This paper proposes an analytical thermal resistance model and a sizing algorithm for PCB copper pads. Firstly, an axisymmetric thermal resistance model is developed for PCB copper pads where the heat conduction, convection and radiation all exist. Due to the interdependence of the conductive/radiative heat transfer coefficient and the board temperature, a new algorithm is proposed to fast obtain the thermal resistance and to predict the semiconductor junction temperature at different copper pad radii. The algorithm enables a fast sizing of copper pads based on different junction temperature limits. Finally, the developed thermal resistance model and algorithm are verified by computational fluid dynamics (CFD) simulations and experiments.**

Keywords—printed circuit board (PCB), copper pad, thermal resistance model

NOMENCLATURE

h	Heat transfer coefficient
h_{conv}	Convective heat transfer coefficient
h_{radi}	Radiative heat transfer coefficient
k	Thermal conductivity of a material
k_1	Lateral thermal conductivity of the middle (copper) zone
k_2	Lateral thermal conductivity of the outer (FR4) zone
L_c	Characteristic length of the hot plane
P	Total power generated by the heat source at the inner radius
r_b	Radius of the heat source (package)
r_s	Radius of the middle (copper) zone
r_e	Radius of the outer (FR4) zone
T_b	PCB board ($r = r_b$) temperature
T_c	Case temperature of the chip
T_j	Junction temperature of the chip
T_t	Top case temperature of the package
t	Thickness of the PCB
t_l	Thickness of the PCB copper layer
T_a	Ambient temperature
T_x	Temperature of the PCB surface
ε	emissivity of the PCB surface
Θ_{ba}	Thermal resistance from the inner zone edge ($r = r_b$) to the ambient
Θ_{jc}	Thermal resistance from the junction to the case
Θ_{jt}	Thermal resistance from the junction to the top case
Θ_{sa}	Thermal resistance from the copper zone edge ($r = r_s$) to the ambient
Θ_{ta}	Thermal resistance from the top case of a chip to the ambient
λ	Convective heat transfer parameter depending on PCB geometry and orientation
σ	Stefan-Boltzmann constant
ψ_{ea}	Equivalent thermal resistance from the FR4 zone edge ($r = r_e$) to the ambient
ψ_{sa}	Equivalent thermal resistance from the copper zone edge ($r = r_s$) to the ambient

I. INTRODUCTION

The size of modern power semiconductor devices (e.g., GaN transistors) are shrinking in order to achieve high power density, low parasitic inductance, and low power losses [1]-[2]. However, the thermal management is identified as the main barrier for a further power density increase [3]. The heat generated inside the miniaturized semiconductors must be effectively dissipated to the ambient; otherwise, the high junction and board temperatures may cause serious reliability issues to the semiconductor, solder, thermal grease, and printed circuit board (PCB) [4]-[7]. In addition, suitable heat dissipation measures should be considered as early as in the design and development phase, because subsequent modifications are generally more costly and involve increased engineering efforts [8]-[9].

In medium power applications, the surface-mounted devices (SMDs) are normally cooled by a heatsink attached to the PCB, where the thermal via array provides an effective thermal path for the heat transfer [10]-[12]. In the low power scenarios, a PCB copper pad is typically used for heat spreading, and the SMDs can be cooled by natural convection [13]. Although the computational fluid dynamics (CFD) simulations feature high accuracy, the model generation time and computational cost could be fairly high [13]. Therefore, it is necessary to develop an analytical model for a quick design of thermal pads.

The heat conduction, convection and radiation all exist for a naturally-cooled PCB, which makes the thermal analysis fairly complicated. Texas Instruments has developed an online PCB thermal calculation tool based on CFD thermal resistance data of different package sizes and pad dimensions [14]. However, some important factors (e.g., PCB thickness, number of copper layers, and copper thickness) are not taken into account; also, the online tool does not support design optimization. In addition

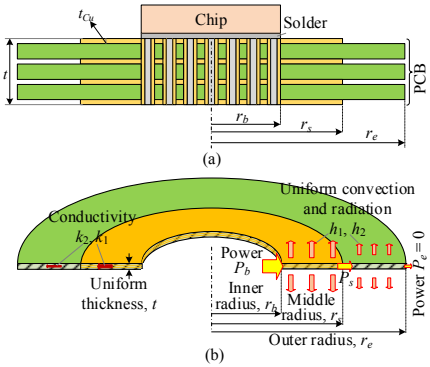

Fig. 1. Simplified PCB board. (a) Vertical cut plane of a PCB board; (b) Heat transfer in a circular PCB board: heat conduction in the radial direction, convection and radiation in the axial direction.

to the CFD simulations, many other numerical calculation methods are developed [13]-[16]. The study in [16] deals with a substrate for a ball grid array package, where a belt of densely populated vias and two continuous copper layers are placed; however, the built model is complicated and no CFD or experimental verifications are provided. For electrical engineers, it is more desired to have an analytical thermal model such that the temperature of devices with different designs and cooling methods can be fast predicted [17]-[18]. In [13] and [19], an analytical thermal resistance model is developed for PCB thermal pads; however, the heat transfer boundary and the convective heat transfer coefficient variation over temperature difference are not included, and as a result, there might be a remarkable error between the calculations and measurements.

This paper presents a new thermal resistance model for PCB copper pads. The board temperature interacts with the vertical convective and radiative heat transfer coefficients. Therefore, an algorithm is developed to find the minimum copper pad size at different PCB parameters, power losses, ambient temperatures and maximum junction temperature limits. Finally, CFD simulations and experimental measurements verify the developed thermal model and sizing algorithm.

II. Thermal Modeling of PCB Copper Pads

A. Heat Transfer in a Circular PCB

For the natural convection in air, the flow remains laminar when the temperature difference involved is less than 100 ºC and the characteristic length of the body is less than 0.5 m [20], which is almost always the case in electronic systems. Therefore, the airflow in the following analysis is assumed to be laminar. The natural convection heat transfer coefficient for laminar flow of air at atmospheric pressure, and radiation heat transfer coefficient are given as [20]

$$\begin{cases} h_{conv} = \lambda[(T_x - T_a)/L_c]^{0.25} \\ h_{radi} = \varepsilon\sigma[(T_x+273)^2 + (T_a+273)^2] \\ \qquad \times[(T_x+273)+(T_a+273)] \\ h = h_{conv} + h_{radi} \end{cases} \tag{1}$$

where T_x is the PCB surface temperature. The PCB mask is an epoxy based lacquer, which is an organic materials and has a high emissivity of about 0.9 [21].

Fig. 1 shows a simplified circular PCB board, where an axisymmetric heat source (package) is located at the inner radius, and the outer edge is assumed to be isothermal. In addition to the heat source, there are two heat transfer zones, i.e., the middle zone (copper zone) within [r_b, r_s] and the outer zone (FR4 zone) within [r_s, r_e]. Heat transfers in both the radial/lateral (conduction) and axial/vertical (convection and radiation) directions. For the lateral heat conduction, the thermal conductivities in the two zones are

$$\begin{cases} k_1 = k_{Cu}N_l t_l / t + k_{FR4}(1 - N_l t_l / t) \\ k_2 = k_{FR4} \end{cases} \tag{2}$$

In the vertical direction, it is assumed that the convective and radiative heat transfer coefficients, h_{conv} and h_{radi}, are constant along the radial direction. Then, in the cylindrical coordinate system, the governing equation for the steady-state heat transfer is [22]

$$\begin{cases} \dfrac{\mathrm{d}^2T}{\mathrm{d}r^2} + \dfrac{1}{r}\dfrac{\mathrm{d}T}{\mathrm{d}r} - \dfrac{h}{kt}(T - T_a) = 0 \\ P = -2\pi rkt\dfrac{\mathrm{d}T}{\mathrm{d}r} \end{cases} \tag{3}$$

where T represents the temperature at the radius of r.

By doing algebraic manipulations, (3) can be solved and the solutions are obtained as

$$\begin{cases} \Delta T = aI_0(z) + bK_0(z) \\ P = -2\pi ktz[aI_1(z) + bK_1(z)] \end{cases} \tag{4}$$

where $\Delta T = T - T_a$, $z = r\sqrt{h/(kt)}$, I_0 is the modified Bessel function of the first kind and order 0, I_1 is the modified Bessel function of the first kind and order 1, K_0 iss the modified Bessel function of the second kind and order 0, K_1 is the modified Bessel function of the second kind and order 1, and a and b are arbitrary constants. Eliminating a and b, and applying the two-port theory yield

$$\begin{bmatrix} \Delta T_i \\ P_i \end{bmatrix} = \mathbf{T}_{ij}\begin{bmatrix} \Delta T_j \\ P_j \end{bmatrix} = \begin{bmatrix} A_{ij} & B_{ij} \\ C_{ij} & D_{ij} \end{bmatrix}\begin{bmatrix} \Delta T_j \\ P_j \end{bmatrix} \tag{5}$$

where the subscript i and j represent the sending and receiving ports at any locations, $\mathbf{T}_{ij}$ is the transmission matrix,

$z_i = r_i\sqrt{h/(kt)}$, $A_{ij} = z_j[I_1(z_j)K_0(z_i) + I_0(z_i)K_1(z_j)]$,

$z_j = r_j\sqrt{h/(kt)}$,

$B_{ij} = [I_0(z_j)K_0(z_i) - I_0(z_i)K_0(z_j)]/(2\pi kt)$,

$C_{ij} = 2\pi ktz_iz_j[I_1(z_j)K_1(z_i) - I_1(z_i)K_1(z_j)]$,

$D_{ij} = z_i[I_0(z_j)K_1(z_i) + I_1(z_i)K_0(z_j)]$.

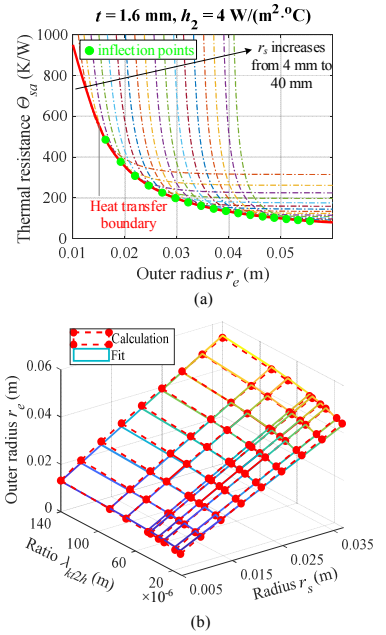

Fig. 2. (a) Curves of the thermal resistance Θ_{sa} with respect to r_s and r_e. (b) The heat transfer boundary r_e versus the copper radius r_s and the ratio λ_{kt2h}.

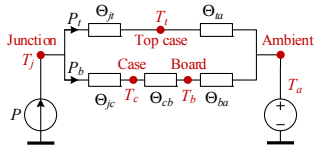

Fig. 3. Equivalent thermal resistance diagram for a DPAK package mounted on a PCB.

The heat transfer from r_s to r_e (including radial conduction and axial convection and radiation) can be illustrated with a two-port system, i.e., the temperature potential ΔT_s and heat flow P_s can be obtained as (5). Assume that the outer edge of $r = r_e$ is adiabatic in the horizontal direction, i.e., $P_e = 0$, then the thermal resistance from r_s to the ambient, Θ_{sa}, can be derived as

$$\begin{bmatrix} \Delta T_s \\ P_s \end{bmatrix} = \mathbf{T}_{se} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} = \begin{bmatrix} A_{se} & B_{se} \\ C_{se} & D_{se} \end{bmatrix} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} \tag{6}$$

$$\Theta_{sa} = \frac{\Delta T_s}{P_s} = \frac{A_{se}}{C_{se}} \tag{7}$$

As for the two-port system from r_b to r_s, we have

$$\begin{bmatrix} \Delta T_b \\ P_b \end{bmatrix} = \mathbf{T}_{bs} \begin{bmatrix} \Delta T_s \\ P_s \end{bmatrix} = \begin{bmatrix} A_{bs} & B_{bs} \\ C_{bs} & D_{bs} \end{bmatrix} \begin{bmatrix} \Delta T_s \\ P_s \end{bmatrix}$$
$$= \mathbf{T}_{bs}\mathbf{T}_{se} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} = \begin{bmatrix} A_{bs}A_{se} + B_{bs}C_{se} & A_{bs}B_{se} + B_{bs}D_{se} \\ C_{bs}A_{se} + D_{bs}C_{se} & C_{bs}B_{se} + D_{bs}D_{se} \end{bmatrix} \begin{bmatrix} \Delta T_e \\ 0 \end{bmatrix} \tag{8}$$

Then the thermal resistance from r_b to the ambient, and the temperature at r_b can be obtained

$$\Theta_{ba} = \frac{\Delta T_b}{P_b} = \frac{A_{bs}A_{se} + B_{bs}C_{se}}{C_{bs}A_{se} + D_{bs}C_{se}} \tag{9}$$

$$T_b = T_a + P_b\Theta_{ba} \tag{10}$$

Manipulating (6) and (8) yields the equivalent thermal resistance from r_s to the ambient and the thermal resistance from r_e to the ambient when an axisymmetric heat source is located at r_b

$$\psi_{sa} = \frac{\Delta T_s}{P_b} = \frac{A_{se}}{C_{bs}A_{se} + D_{bs}C_{se}} \Rightarrow T_s = T_a + P_b\psi_{sa} \tag{11}$$

$$\psi_{ea} = \frac{\Delta T_e}{P_b} = \frac{1}{C_{bs}A_{se} + D_{bs}C_{se}} \Rightarrow T_e = T_a + P_b\psi_{ea} \tag{12}$$

It should be noted that ψ_{sa} and ψ_{ea} are defined similarly to the thermal metric ψ_{JT} adopted by the industry (JEDEC Standard: JESD51-2 [23]). They are not true thermal resistances, but could be used to calculate the temperatures at r_s and r_e.

The analysis above is carried out by assuming that the heat source, copper pad and PCB are circular. In practice, the majority of them are rectangular in shape; thus the equivalent radius of a rectangular shape can be approximated by $r_x = \sqrt{a_x b_x / \pi}$ where a_x and b_x are the rectangular side lengths, and the subscript 'x' denotes 'b', 's', and 'e'.

B. Heat Transfer Boundary

In order to satisfy the boundary condition that there is no conductive heat flow at r_e, the thermal resistance Θ_{sa} (7) is investigated with respect to different parameters, i.e., r_e, t, and h, as shown in Fig. 2. When r_s is specified, the thermal resistance Θ_{sa} decreases with respect to the increase of r_e; however, the decrease of Θ_{sa} becomes insignificant when r_e exceeds the inflection point r_{ec}, which means that the heat flow beyond r_{ec} can be negligible and the inflection points can be chosen as the heat transfer boundary. It should be noted that r_{ec} depends on both the copper radius r_s and the ratio of $k{\cdot}t$ to h_2, i.e., $\lambda_{kt2h} = kt / h_2$. It is quite difficult to directly obtain the analytical expression of r_{ec}. Therefore, curve fitting is carried out, as shown in Fig. 2(b). It is found that the outer radius r_e can be determined by

$$r_e = 3\lambda_{kt2h}^{0.095}(r_s + 0.005) \tag{13}$$

III. Sizing of PCB Copper Pads

A. Algorithm for Copper Pad Sizing

When an SMD is mounted on a PCB, the heat generated inside the device will be dissipated in two parallel pathways: one is from the junction to the top case, and finally to the ambient; the other is from the junction to the bottom case, then to the board, and finally to the ambient. Fig. 3 shows the

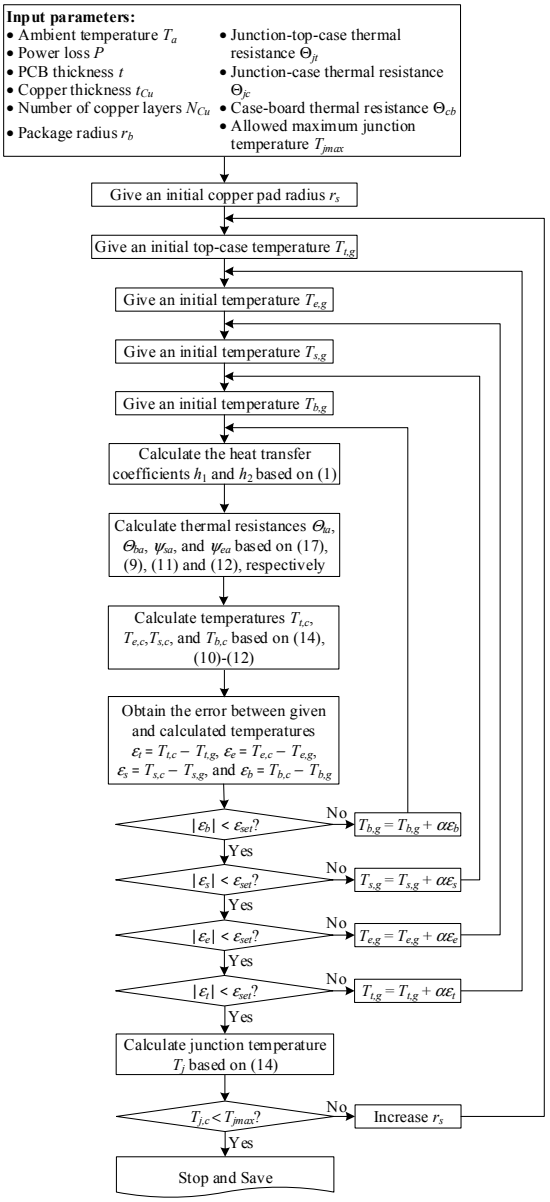

Fig. 4. Flowchart for calculating the thermal resistance of a PCB copper pad.

equivalent thermal resistance diagram for a DPAK package mounted on a PCB. If all the thermal resistances are known, then the top-case and junction temperatures can be predicted by

$$T_t = \frac{P\Theta_{ta}(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})}{\Theta_{jt} + \Theta_{ta} + \Theta_{jc} + \Theta_{cb} + \Theta_{ba}} + T_a \quad (14)$$

$$T_j = \frac{P(\Theta_{jt} + \Theta_{ta})(\Theta_{jc} + \Theta_{cb} + \Theta_{ba})}{\Theta_{jt} + \Theta_{ta} + \Theta_{jc} + \Theta_{cb} + \Theta_{ba}} + T_a \quad (15)$$

If the top-case temperature T_t and other thermal resistances are determined, then the board-ambient thermal resistance Θ_{ba} can be obtained as

$$\Theta_{ba} = \frac{P\Theta_{ta}(\Theta_{cb} + \Theta_{jc}) - (T_t - T_a)(\Theta_{jc} + \Theta_{cb} + \Theta_{jt} + \Theta_{ta})}{T_t - T_a - P\Theta_{ta}} \quad (16)$$

For the heat transfers from the junction to the top-case, from the junction to the bottom-case, and from the case to the board, there is only heat conduction, and therefore the corresponding thermal resistances Θ_{jt}, Θ_{jc}, and Θ_{cb} are constant if neglecting the relatively small material property variation over temperature. However, the heat transfers from the top-case to the ambient and from the board to the ambient involve convection and radiation. Hence, the thermal resistances Θ_{ta} and Θ_{ba} are temperature related. Meanwhile, the total power loss P is divided into two parts P_t and P_b, i.e., $P = P_t + P_b$. Thus, the thermal resistance Θ_{ta} and Θ_{ba} interact with each other as well. Therefore, an algorithm taking into account all the five thermal resistances in Fig. 3 is developed to design the copper pad size, as shown in Fig. 4.

Before the design, the system parameters, e.g., the ambient temperature T_a, total Power loss P, PCB thickness t, copper thickness t_{Cu}, number of copper layers N_{Cu}, package radius r_b, junction-top-case thermal resistance Θ_{jt}, junction-case thermal resistance Θ_{jc}, case-board thermal resistance Θ_{cb}, allowed maximum junction temperature $T_{jmax,}$ should be determined. Firstly, a small initial value is given to the copper pad radius r_s before the four given temperatures $T_{t,g}$, $T_{e,g}$, $T_{s,g}$, and $T_{b,g}$, are initialized. Then the heat transfer coefficients h_1 and h_2 can be calculated based on (1), and the thermal resistances Θ_{ta}, Θ_{ba}, ψ_{sa}, and ψ_{ea} can be obtained accordingly. After that, the calculated temperatures $T_{t,c}$, $T_{e,c}$, $T_{s,c}$ and $T_{b,c}$ are compared with the given temperatures $T_{t,g}$, $T_{e,g}$, $T_{s,g}$, and $T_{b,g}$; also the errors can be obtained, i.e., $\varepsilon_t = T_{t,c} - T_{t,g}$, $\varepsilon_e = T_{e,c} - T_{e,g}$, $\varepsilon_s = T_{s,c} - T_{s,g}$, and $\varepsilon_b = T_{b,c} - T_{b,g}$. If the absolute error ε_x is greater than the preset limit ε_{lmt}, then the given temperature $T_{x,g}$ will be updated by adding $\alpha\varepsilon_x$ where α is an incremental coefficient and the subscript x represents 't', 'e', 's', or 'b'. If all four temperature errors are smaller than ε_{lmt}, then the algorithm proceeds to calculate the junction temperature T_j according to (15). If the calculated T_j is higher than the allowed maximum junction temperature, then the copper pad radius r_e will be increased. Otherwise, it implies that the current copper pad radius r_e is large enough for cooling. In this way, we can find the minimum r_e, which can help to achieve the maximum power density while meeting the thermal specifications.

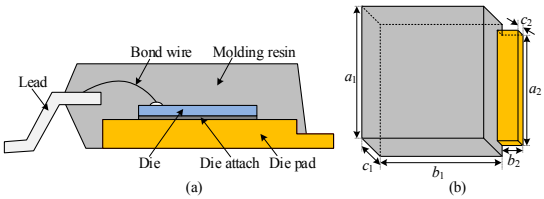

Fig. 5. (a) DPAK package structure; (b) Simplified package outline dimensions of diode VS-6EWL06FN-M3 [24].

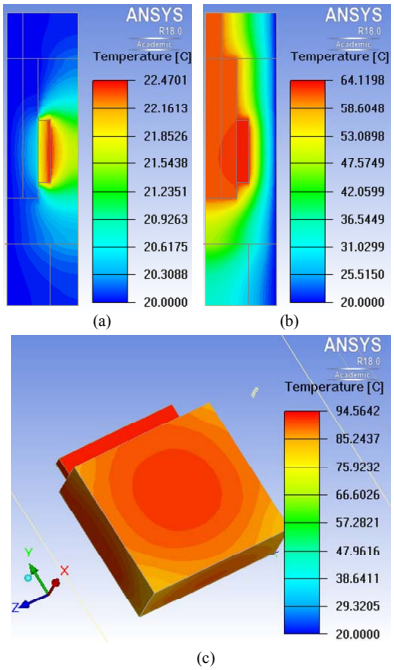

Fig. 6. CFD simulation results of the DPAK diode VS-6EWL06FN-M3 in ANSYS/Icepak. (a) Junction-case thermal resistance Θ_{jc}. (b) Junction-top-case thermal resistance Θ_{jt}. (c) Top-case-ambient thermal resistance Θ_{ta}.

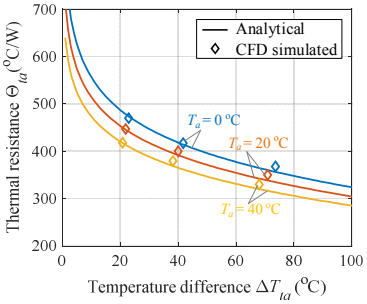

Fig. 7. CFD simulation results of the thermal resistance from the diode surface to the ambient for different ambient temperatures.

B. *Thermal Modeling of DPAK Package*

The realization of the proposed algorithm requires the knowledge of the thermal resistances Θ_{jt}, Θ_{ta}, and Θ_{jc}, which are package dependent and usually not available in datasheets. Therefore, detailed thermal modeling of DPAK package is conducted here. When a DPAK package is mounted on a PCB, the equivalent thermal resistance diagram is shown in Fig. 3. To extract the thermal resistances Θ_{jt}, Θ_{ta}, and Θ_{jc}, a detailed structure model is built, as shown in Fig. 5(a). For the heat transfer paths from the junction to the top-case and from the junction to the case, only heat conduction is involved. The thermal simulation with ANSYS/Icepak is used to obtain the thermal resistances Θ_{jc} and Θ_{jt}, as shown in Fig. 6(a) and (b). It is found that the two thermal resistances are Θ_{jc} = 2.47 °C/W and Θ_{jc} = 44.12 °C/W.

As for the heat transfer from the top surface of the diode to the ambient, heat conduction, convection and radiation all exist, and the heat transfer coefficient depends on both the ambient temperature and the temperature difference between the top surface and the ambient. An analytical model of the thermal resistance Θ_{ta} is firstly built. The simplified package outline dimensions are shown in Fig. 5(b). Assume that the package is placed horizontally, and its surfaces are cooled by natural convection. Then the thermal resistance from the surface to the ambient can be obtained as

$$\Theta_{ta} = \frac{1}{\left(\begin{array}{l} 2c_1(a_1+b_1)\left(\lambda_{ver}[(T_t-T_a)/c_1]^{0.25}+h_{radi1}\right) \\ +c_2(a_2+2b_2)\left(\lambda_{ver}[(T_t-T_a)/c_2]^{0.25}+h_{radi2}\right) \\ +a_1b_1\left(\lambda_{hor}[(a_1+b_1)(T_t-T_a)/(2a_1b_1)]^{0.25}+h_{radi1}\right) \\ +a_2b_2\left(\lambda_{hor}[(a_2+b_2)(T_t-T_a)/(2a_2b_2)]^{0.25}+h_{radi2}\right) \end{array}\right)} \tag{17}$$

where the radiative heat transfer coefficients $h_{radi1} = \varepsilon_1\sigma(T_a+273+T_t+273)[(T_a+273)^2+(T_t+273)^2]$ and $h_{radi2} = \varepsilon_2\sigma(T_a+273+T_t+273)[(T_a+273)^2+(T_t+273)^2]$ are for the molding resin surface and the tab surface, respectively, and λ_{hor} = 1.32 and λ_{ver} = 0.59 are constants for horizontal and vertical plates, respectively [20].

To verify the built analytical thermal resistance model of Θ_{ta}, multiple CFD simulations are done in ANSYS/Icepak, as shown in Fig. 6(c) and Fig. 7. It is seen that there is a negligible error (maximum error: 3.2 %) between the simulations and the analytical results.

IV. Experimental Verification

Four DPAK diodes VS-6EWL06FN-M3 are mounted on four 2-layer PCBs (70-μm copper thickness for each layer) with different sizes of copper pads, as shown in Fig. 8. All diodes are serially connected to a dc power source, and thus the diodes can generate equal power losses, which are further dissipated by the copper pad and natural convection. The steady-state

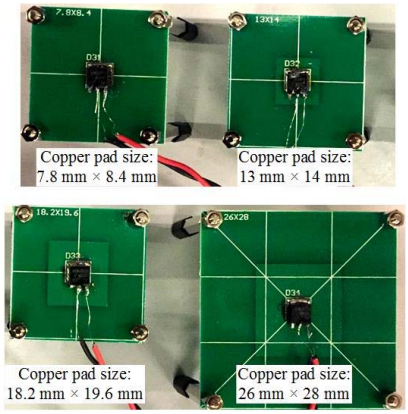

Fig. 8. Photo of the built PCBs with different copper pad sizes.

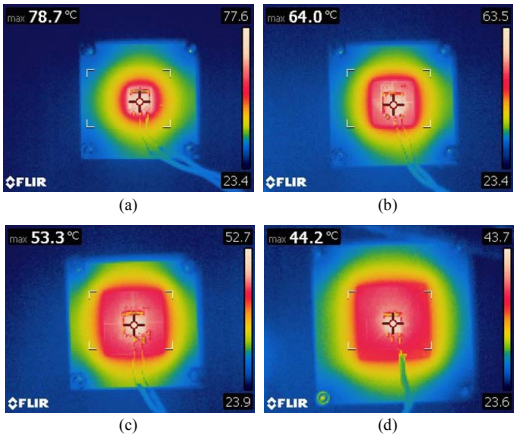

Fig. 9. Thermal images of diodes mounted on PCBs with 0.5-W power losses injected and different sizes of copper pads.

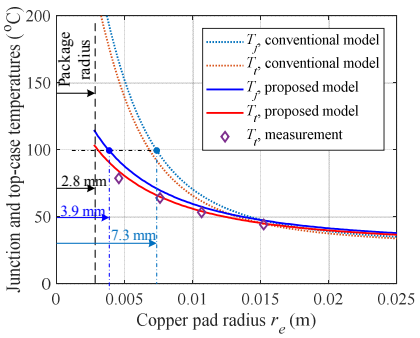

Fig. 10. Comparison of junction and top-case temperatures between measurements and calculations when 0.5-W power losses are generated inside the diode.

thermal images of the diodes are captured for different sizes of copper pads, as shown in Fig. 9.

Fig. 10 depicts the measured and calculated junction and top-case temperatures when $P = 0.5$ W. As can be seen, there is a significant top-case temperature difference between the conventional model [13], [19] and the measurements, especially when the copper pad radius is smaller than 15 mm. In contrast, the proposed model can help to predict the top-case temperature with a small error. Therefore, the new model can be used to predict the junction temperature. The maximum operating junction temperature of the selected diode VS-6EWL06FN-M3 is 175 °C [24]. For the sake of high reliability, the maximum junction temperature T_{jmax} should be lower than the limit, e.g., $T_{jmax} = 100$ °C. Then the minimum copper radius can be found, as illustrated in Fig. 10. Based on the proposed model, the minimum copper radius r_e is 3.9 mm, whereas the conventional model gives a minimum copper radius of 7.3 mm, which corresponds to a 250% increase of the copper pad area compared to the design of $r_e = 3.9$ mm.

V. Conclusions

This paper proposes a new method for sizing PCB copper pads. An axisymmetric thermal resistance model is firstly developed for naturally cooled PCB pads. Then an algorithm is proposed to find the thermal resistance of the PCB pad and the junction temperature of the chip at different pad sizes and ambient temperatures. CFD simulations and experimental measurements agree well with the analytical model. It is concluded that 1) the conventional analytical thermal model for PCB pads overestimates the semiconductor junction temperature, particularly when the copper pad is small in size (< 15 mm); 2) the proposed thermal model and algorithm are able to predict the device junction temperature and size the copper pad with small errors.

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Paper E

Cost-Volume-Reliability Pareto Optimization of a Photovoltaic Microinverter

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Cost-Volume-Reliability Pareto Optimization of a Photovoltaic Microinverter

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***Abstract*— A multiobjective Pareto optimization routine is proposed to systematically assess the concepts with respect to the annual degradation, annual energy loss, volume and cost of a PV microinverter. As an important performance criterion, the reliability is included in the multiobjective optimization, which previously has not been discussed in the literature. Thus, a practical trade-off can be made among annual degradation, annual energy yield, volume and cost for the PV microinverter. Firstly, the operation principle and characteristics of the inverter stage operating in the boundary conduction mode (BCM) are detailed for the waveform modeling. Then, the components parameters are characterized and the electro-thermal models are developed for the microinverter system. After that, the critical performance metrics, i.e., reliability, cost, and volume, are modeled before the multiobjective Pareto optimization is conducted. A one-year mission profile from Arizona, US, is employed for the calculations of the annual energy loss and accumulative damage.**

I. Introduction

Photovoltaic (PV) inverters can be classified into three categories: central inverters, string inverters, and microinverters. Compared with the first two categories, microinverters feature more advantages in low-power applications due to the module-level maximum power point tracking (MPPT) capability, low system installation effort, easy monitoring and failure detection, and better safety [1]–[4]. Nevertheless, there are still some challenges for microinverters:

- The power conversion efficiency of microinverters is still relatively low compared with transformerless string inverters (e.g., a peak efficiency of 99.2% is reported in [5]); thus, the efficiency performance of microinverters needs to be improved to strengthen their advantages concerning energy yields [3];

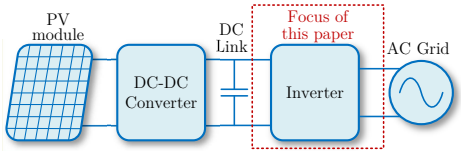


Fig. 1. Configuration of a two-stage grid-connected PV microinverter system.

- There is a trend that a PV microinverer will be integrated into a PV module [6], [7], which implies that the microinverter should be more compact;
- The panel-embedded microinverter may be inevitably heated up by the PV panel, accelerating the degradation of components [8], [9];
- Due to the higher number of converters, the microinverter-based PV systems may have a big overhead [3].

In the literature, three power conversion structures can be found for PV microinverters, i.e., the high-frequency-link (single-stage) microinverter [10], pseudo dc-link microinverter [11], and dc-link (two-stage) microinverter [12], [13]. The dc-link microinverters have the advantages of simpler structure, lower power decoupling capacitance, easier grid voltage/var support, and easier performance optimization for each stage; therefore, they have attracted a growing interest [7], [12], [14], [15]. Fig. 1 shows the configuration of a two-stage grid-connected PV microinverter system. Typically, the front-end dc-dc converter is controlled to achieve the MPPT of the PV module, whereas the inverter stage is used to regulate the dc-link voltage as well as to perform various grid-connection functions [7].

The performance metrics of a PV microinverter include efficiency, energy caption, grid integration, cost, volume, reliability, etc. Most early studies as well as current work focus on the efficiency [3], [10], [12], [14], [16]–[20], energy caption [21], [22], grid support function [7], [15], power decoupling [23]–[26], and levelized cost of energy (LCOE) of PV microinverters [4], [27]–[29]. In the literature of PV microinverters, the most attention has been paid to the power conversion efficiency, which could not only reduce the cost of energy but also improve system reliability [14]. The efficiency improvement of a PV microinverter can be achieved by the innovations on converter topology [16]–[18], modulation scheme [10], [12], control strategy [14], [19], [20], and system design (including component selection, PCB design, cooling design, etc.) [3]. The energy caption enhancement of a PV microinverter system can be realized by adopting a shade-tolerant (global) MPPT algorithm [21] or using a differential power processing architecture [22]. To enable the grid-support functions, e.g., Volt/VAR support and harmonics mitigation, advanced controls are applied to the two-stage microinverters in [7], [15]. A growing number of works have recently focused on the both passive and active power decoupling techniques of PV microinverters for higher reliability or smaller physical size [23]–[26]. Furthermore, one of the most popular benchmarking criteria for different PV microinverter techniques is the levelized cost of energy (LCOE), which is widely adopted in industry, academia and government [4], [27], [28]. The LCOE of a PV microinverter system can be lowered by reducing the system cost and increasing the efficiency and reliability [29].

The lifetime/warranty of PV modules is about 25 years, but inverters have to be replaced every 5 to 10 years [30], implying that the reliability of a microinverter needs improvement to get along with a PV module. Therefore,

the reliability-oriented design of PV microinverters under a harsh environment is paramount [9], [31]. Based on a failure mode and effects analysis (FMEA) survey for MLPE products [32], the loose connection of dc input and ac output connectors, wear-out of dc-link electrolytic capacitors, varistor failure-short from the surge, and degradation of MOSFETs and diodes are identified as the top four failure modes. Due to the compound filled inside microinverter enclosures, the erosion of critical components from humidity is prevented; thus, the temperature cycling is reported as the most significant stressor that affects the reliability of microinverter products [32].

Recently, increasing effort has been made to the reliability of discrete power electronics components or modules (e.g., IGBT [33], MOSFET [34], and capacitor [35]).In the literature, only a few studies focused on the microinverter reliability can be found, and most of them use the MIL-HDBK-217 handbook [36] to determine the failure rates of microinverters [37], [38]. Unfortunately, the constant failure rates only describe the large-population statistics of random failures, and the wear-out failure is not considered. Meanwhile, the MLPE market is relatively nascent and there is not enough long-term usage data or independent reliability testing; therefore, accelerated testing of PV MI products is conducted in [8] for a long-term reliability prediction. It turns out that the times-to-failure of microinverters from different manufacturers deviate significantly due to the design. Based on a system-level electro-thermal model, a wear-out failure analysis and improvement on a PV microinverter is conducted in [14]. However, other performance metrics, e.g., cost and volume, are not taken into account.

The multiobjective optimization of power electronics enables designers to make the trade-off among multiple performance metrics. During the last decade, the efficiency plus power density Pareto optimizations of a power factor correction (PFC) rectifier, LC output filters, inductive power transfer coils, switched capacitor converters have been presented in [39]–[42], respectively. Recently, another important goal, cost, is also taken into account in the multiobjective Pareto optimization of dual active bridge (DAB) converters [43]. However, another crucial performance criterion, reliability, is still neglected in the existing multiobjective optimization literature. On the other hand, only a few papers can be found for the multiobjective optimization of PV microinverters. In [44], a comparative study on different microinverter architectures is conducted to make a trade-off between efficiency and Volt/VAR support capability. Dong $etal$ [7] presents a detailed procedure considering multiple performance metrics (e.g., efficiency, cost, and reliability) and compliances (e.g., EMC and safety compliance, and agency compliance); however, only part of the design possibilities are explored, and therefore, the design may not be Pareto optimal.

In light of the limitations of current research, this paper proposes a systematic routine for the multiobjective (including the annual damage, annual energy loss, volume, and cost) Pareto optimization of a PV microinverter. Firstly, the operation principle and characteristics of the inverter stage in the boundary conduction mode (BCM) are detailed for the waveform modeling. Then, the components parameters are characterized and the electro-thermal models are developed for the microinverter system. After that, the critical performance metrics, reliability, cost, and volume, are modeled before the multiobjective Pareto optimization is conducted.

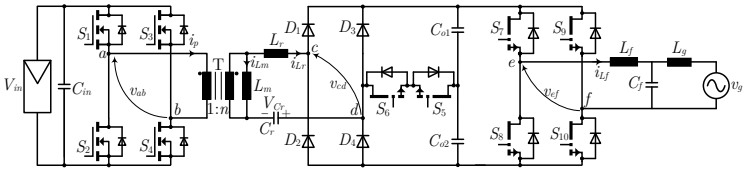


Fig. 2. Schematic of the proposed two-stage PV microinverter.

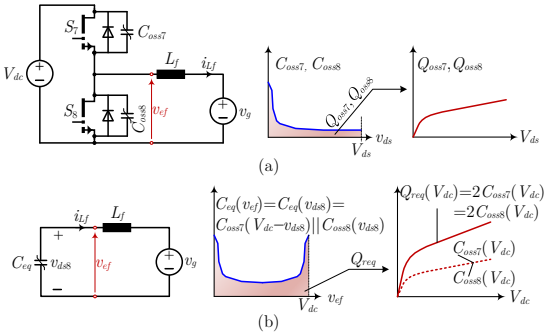


Fig. 3. (a) Parasitic output capacitors of GaN transistors in a bridge-leg; (b) Equivalent output capacitor of the bridge-leg.

II. Operation Principle and Characteristics of the Proposed PV Microinverter

A. Topology Description

Fig. 2 shows the proposed two-stage PV microinverter topology which consists of a dual-mode-rectifier based series resonant converter (DMR-SRC) as the font-end stage and a full-bridge inverter as the secondary stage. The main functions of the front-end stage dc-dc converter include allowing the PV panel to achieve the maximum power point tracking (MPPT), providing galvanic isolation and stepping up the low PV voltage to the high dc-link voltage. Due to the dual-mode rectification, the dc-dc stage can handle a wide PV output voltage range while maintaining high efficiencies. The detailed operation principles, characteristics and experimental verifications have been given in [18]. The main focus of this paper is the design optimization of the inverter stage composed of the active switches $S_7 - S_{10}$, filter inductor L_f and capacitor C_f.

B. Boundary-Conduction-Mode Operation

The inverter is controlled to operate in the boundary conduction mode(BCM) [45] such that the active switches $S_7 - S_{10}$ can achieve ZVS. The bridge leg $S_7 - S_8$ operates at high frequencies whereas the other bridge leg $S_9 - S_{10}$ is synchronous with the grid voltage v_g. In the positive half line cycle, i.e., $v_g > 0$, S_{10} will be controlled to operate in the the on state and S_9 will be kept in the off-state; when the grid voltage enters into its negative half cycle, i.e., $v_g < 0$, then S_{10} will be turned off, and S_9 will be kept in the on state. Due to the symmetry of topology and operation, only the positive half line cycle is analyzed.

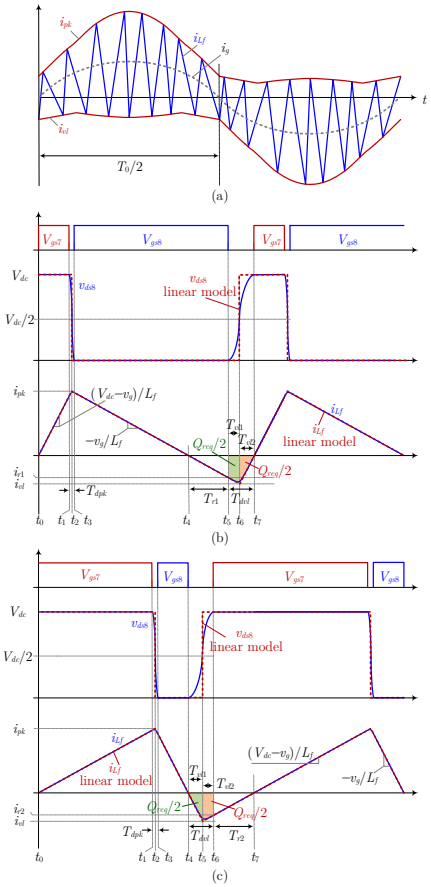


Fig. 4. (a) Inductor current over a line cycle; (b) Inductor current and drain-source voltage of S_8, i.e., V_{ds8}, in the case of $v_g < V_{dc}/2$; (c) Inductor current and drain-source voltage of S_8, i.e., V_{ds8}, in the case of $v_g > V_{dc}/2$.

When $v_g > 0$ and S_{10} are kept on, the inverter can be regarded as a buck dc-dc converter with a varying output v_g, as shown in Fig. 3. The ZVS realization of a switching leg relies on the charging and discharging the parasitic output capacitors of switches. The parasitic output capacitor of a GaN HEMT is highly nonlinear and it varies with respect to its drain-source voltage v_{ds}, as illustrated in Fig. 3(a). For a bridge leg, e.g., $S_7 - S_8$, the two parasitic output capacitors are in parallel in capacitance but in series in the drain-source voltage, i.e., $C_{eq}(v_{ef}) = C_{eq}(v_{ds8}) = C_{oss7}(v_{ds7})||C_{oss8}(v_{ds8}) = C_{oss7}(V_{dc} - v_{ds8})||C_{oss8}(v_{ds8})$. Thus, the equivalent output capacitance of a bridge leg is a bathtub curve with respect to the bridge output voltage v_{ef}. The charge stored in a capacitor, e.g., Q_{oss7}, can be obtained by

$$Q_{oss7}(V_{ds}) = \int_0^{V_{ds}} C_{oss7}(v_{ds})dv_{ds} = \int_{V_{ds}}^{0} C_{oss7}(v_{ds})dv_{ds} \tag{1}$$

where V_{ds} is the starting or ending voltage when fully discharging or charging a capacitor. For the half-bridge composed with the two parasitic capacitors C_{oss7} and C_{oss8}, the required charge to fully charge or discharge C_{eq} can be calculated by

$$Q_{req}(V_{dc}) = 2Q_{oss7}(V_{dc}) = 2Q_{oss8}(V_{dc}) \tag{2}$$

With the BCM modulation, the triangular inductor current i_{Lf} has two bounds, i.e., the upper bound i_{pk} and the lower bound i_{vl}, as shown in Fig. 4(a). The average inductor current, i.e., the gray dashline, equals to the grid current. The lower bound of the triangular inductor current is used to achieve ZVS of S_7 and S_8. In order to minimize the conduction losses, the inductor rms current should be kept possibly low. Therefore, the lower current bound i_{vl} should be maintained small in the absolute value under the condition of ZVS. Thus, when the grid voltage v_g changes over time, the mathematical expression of the lower bound i_{vl} varies as well.

Case I: $v_g < V_{dc}/2$

In this case, the inductor current i_{Lf} and the drain-source voltage of S_8, v_{ds8}, are shown in Fig. 4(b). Seven intervals can be identified over a switching cycle $[t_0, t_7]$ (see Figs. 3 and 4(b)):

Interval 1 $[t_0, t_1]$: S_7 is turned on whereas S_8 is in the off state. Thus, inductor current i_{Lf} increases linearly as

$$i_{Lf}(t) = \frac{V_{dc} - v_g}{L_f}(t - t_0) \tag{3}$$

Interval 2 $[t_1, t_2]$: at t_1, S_7 is turned-off, and thus the positive inductor current i_{Lf} begins to charge C_{oss7} and discharge C_{oss8}. Before v_{ds8} (i.e., v_{eq}) falls to $V_{dc}/2$, the inductor current i_{Lf} can be approximated as being increasing as (3) due to the high nonlinearity of C_{eq} (see Fig.3); it has been demonstrated in [39] that this kind of approximation lead to a negligible error for the inductor current waveform. When the charge provided by i_{Lf} from $t = t_1$ equals $Q_{req}/2$, the voltage v_{ds8} (i.e., v_{eq}) decreases to $V_{dc}/2$ (see Fig. 3). According to the linear switching model proposed in [39], the voltage v_{ds} $(= v_{eq})$ steps down from the dc-link voltage V_{dc} to 0.

Interval 3 $[t_2, t_3]$: at t_2, $v_{ds8} = 0$ and the inductor current starts being discharged as

$$i_{Lf}(t) = i_{pk} - \frac{v_g}{L_f}(t - t_2) \tag{4}$$

Interval 4 $[t_3, t_4]$: At $t = t_3$, the charge provided by i_{Lf} equals to Q_{req}, and thus v_{ds8} declines to 0. From this time instant, the body diode of S_8 begins conducting, and S_8 can achieve ZVS-on with a turn-on gate signal applied subsequently. In this stage, the inductor current is still decreasing as (4).

Interval 5 $[t_4, t_5]$: The inductor current i_{Lf} falls to 0 at $t = t_4$, from which i_{Lf} becomes negative and begins flowing through the drain-source channel of S_8 instead of its body diode.

Interval 6 $[t_5, t_6]$: At t_5, S_8 is switched off, and thus the negative inductor current begins charging C_{oss8} and discharging C_{oss7}. Before v_{ds8} climbs to $V_{dc}/2$, the inductor current i_{Lf} keeps linearly decreasing as (4).

Interval 7 $[t_6, t_7]$: At t_6, the charge accumulated from t_5 amounts to $Q_{req}/2$, and v_{ds8} reaches $V_{dc}/2$. Then, the valley inductor current i_{vl} is reached and the inductor current i_{Lf} starts linearly rising with the slope as in (3). When the charged accumulated from t_5 reaches Q_{req}, v_{ds8} rises to V_{dc}, and v_{ds7} falls to 0. Subsequently, S_7 can be turned on under ZVS.

Preferably, the accumulated charges during [t_5, t_6] and [t_6, t_7] both are equal to $Q_{req}/2$ in order to achieve the minimum inductor rms current. Therefore, the timing of gate drive signals is crucial, i.e., S_8 should be turned off at $i_{Lf} = i_{r1}$ while i_{Lf} is decreasing, and S_7 should be turned on at $i_{Lf} = 0$ while i_{Lf} is increasing.

Case II: $v_g > V_{dc}/2$

The operation principle in case II is similar with that in case I, as illustrated in Fig. 4. Likewise, seven intervals can be identified over a switching period. The operation in the first four intervals is the same as that in case I, and therefor it is not repeated.

Interval 5 $[t_4, t_5]$: The inductor current i_{Lf} falls to 0 at $t = t_4$, at which S_8 is turned off instead of being maintained in the on state in case I. Thus, the inductor L_f begins to charge C_{oss8} and discharge C_{oss7}. Because of the high nonlinearity of C_{oss7} and C_{oss8}, the inductor current can be approximated as being decreasing linearly in this interval.

Interval 6 $[t_5, t_6]$: At t_5, the valley inductor current i_{vl} is reached, the charge accumulated from t_5 amounts to $Q_{req}/2$, v_{ds8} reaches $V_{dc}/2$, and thus the inductor current i_{Lf} begins to linearly rise based on the linear switching model [39].

Interval 7 $[t_6, t_7]$: An amount of charge of $Q_{req}/2$ is accumulated within the interval $[t_5, t_6]$, which means that v_{ds8} has climbed to V_{dc} and v_{ds7} has fallen to 0 at $t = t_6$. Thus, S_7 can be turned on under ZVS. During the interval of $[t_6, t_7]$, the inductor current i_{Lf} is still increasing but negative in direction.

It can be seen that in case II, S_8 should be turned off at $i_{Lf} = 0$ while i_{Lf} is decreasing, and S_7 should be turned on at $i_{Lf} = i_{r2}$ while i_{Lf} is increasing.

C. Characteristics

As aforementioned, in order to achieve ZVS while maintaining the lowest conduction losses, the turn-off of S_8 and turn-on of S_7 occur at $i_{Lf} = i_{r1}$ and $i_{Lf} = i_{r2}$, respectively. The two switching currents i_{r1} and i_{r2} vary over a line cycle, and they can be obtained by solving the geometry problems shown in Fig. 4(b) and (c):

$$i_{r1} = \begin{cases} -\frac{\sqrt{L_f Q_{req}(V_{dc}-2v_g)}}{L_f}, & v_g < \frac{V_{dc}}{2} \\ 0, & v_g \geq \frac{V_{dc}}{2} \end{cases} \tag{5}$$

$$i_{r2} = \begin{cases} 0, & v_g < \frac{V_{dc}}{2} \\ -\frac{\sqrt{L_f Q_{req}(2v_g-V_{dc})}}{L_f}, & v_g \geq \frac{V_{dc}}{2} \end{cases} \tag{6}$$

Similarly, the peak and valley inductor currents i_{pk} and i_{vl} can be obtained as

$$i_{pk=} \begin{cases} 2i_g + \sqrt{\frac{Q_{req}(V_{dc}-v_g)}{L_f}}, & v_g < \frac{V_{dc}}{2} \\ 2i_g + \sqrt{\frac{Q_{req}v_g}{L_f}}, & v_g \geq \frac{V_{dc}}{2} \end{cases} \tag{7}$$

$$i_{vl} = \begin{cases} -\sqrt{\frac{Q_{req}(V_{dc}-v_g)}{L_f}}, & v_g < \frac{V_{dc}}{2} \\ -\sqrt{\frac{Q_{req}v_g}{L_f}}, & v_g \geq \frac{V_{dc}}{2} \end{cases} \tag{8}$$

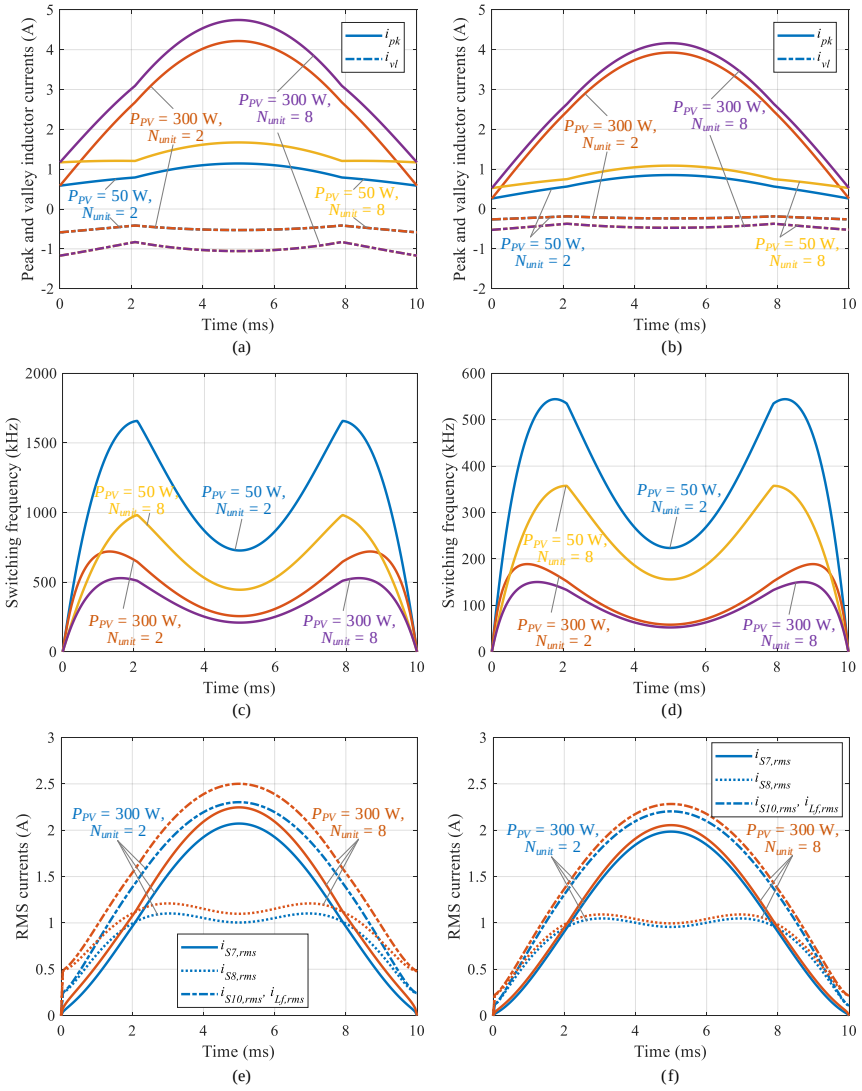


Fig. 5. Characteristics of currents and switching frequency over half a line cycle at different design parameters: (a) peak and valley inductor currents at L_f = 50 μH, (b) peak and valley inductor currents at L_f = 250 μH, (c) switching frequency at L_f = 50 μH, (d) switching frequency at L_f = 250 μH, (e) RMS currents $i_{S7,rms}, i_{S8,rms}, i_{S10,rms}$ and $i_{Lf,rms}$ at L_f = 50 μH, (f) RMS currents $i_{S7,rms}, i_{S8,rms}, i_{S10,rms}$ and $i_{Lf,rms}$ at L_f = 250 μH

As can be seen, the two switching currents i_{r1} and i_{r2} and the valley inductor current i_{vl} depend on Q_{req}, L_f, v_g and V_{dc}, but is independent of the grid current i_g which represents the feed-in power. For the peak inductor current i_{pk}, however, it is also proportional to the grid current i_g, as illustrated in Figs. 5(a) and (b) where N_{unit} denotes

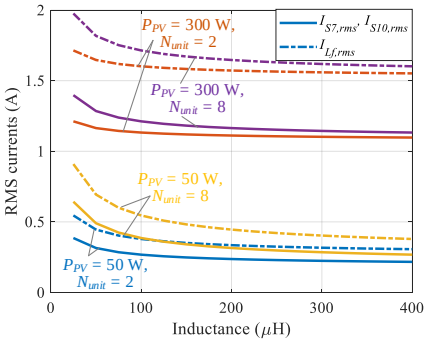


Fig. 6. Average RMS currents at different design parameters.

the number of die units inside the GaN eHEMT ($S_7 - S_{10}$). The current rating of a GaN eHEMT is achieved by embedding different numbers of die units in parallel. With a different N_{unit}, the parasitic output capacitance C_{oss} of a GaN eHEMT will be also different, which will be detailed in Section III-A.

The switching frequency f_s can be obtained by adding all the time durations from t_0 to t_7:

$$f_s = \begin{cases} \frac{2V_{dc}\left(i_g L_f + \sqrt{L_f Q_{req}(V_{dc}-v_g)}\right)}{v_g(V_{dc}-v_g)}, & v_g \le \frac{V_{dc}}{2} \\ \frac{2V_{dc}\left(i_g L_f + \sqrt{L_f Q_{req} v_g}\right)}{v_g(V_{dc}-v_g)}, & v_g > \frac{V_{dc}}{2} \end{cases} \tag{9}$$

Then, the characteristics of the switching frequency f_s versus time can be depicted at different operation conditions, including the feed-in power P_{PV} and the number of die units inside a GaN eHEMT (N_{unit}). As can be seen, the switching frequency f_s varies over half a line cycle. As the decrease of P_{PV} and N_{unit}, the switching frequency f_s will be increased. When the filter inductance L_f is low (e.g., $L_f = 50\mu H$ in Fig. 5), the highest switching frequency at low powers may be unacceptably high, leading to high inductor losses and increased implementation complexity.

It is assumed that in case I (see Figs. 4(b)) the inductor current i_{Lf} flows through S_8 within $[t_2, t_6]$ and through S_7 within $[t_6, t_2]$; in case II (see Figs. 4(c)), the inductor current i_{Lf} flows through S_8 within $[t_2, t_5]$ and through S_7 within $[t_5, t_2]$. Based on [46], the local rms values, $i_{S7,rms}$ and $i_{S8,rms}$, of the switch currents for the positive half line period can be derived as

$$\begin{cases} i_{S7,rms} = \sqrt{\frac{1}{3T_s}\left(i_{pk}^2 t_{on} - i_{vl}^2 \frac{L_f i_{vl}}{V_{dc}-v_g}\right)} \\ i_{S8,rms} = \sqrt{\frac{1}{3T_s}\left(i_{pk}^2 t_{off} - i_{vl}^2 \frac{L_f i_{vl}}{v_g}\right)} \\ i_{Lf,rms} = i_{S10,rms} = \sqrt{i_{S7,rms}^2 + i_{S8,rms}^2} \\ i_{S9,rms} = 0 \end{cases} \tag{10}$$

The real-time rms currents $i_{S7,rms}$, $i_{S8,rms}$, $i_{S10,rms}$, and $i_{Lf,rms}$ can be plotted at different N_{unit}, and L_f, as shown in Figs. 5(e) and (f).

Since the modulation for the negative half line cycle is complementary to the positive half cycle, all switches have the same rms currents over a mains period:

$$I_{S7,rms} = I_{S8,rms} = I_{S9,rms} = I_{S10,rms} = \frac{I_{Lf,rms}}{\sqrt{2}} = \sqrt{\frac{1}{T_0}\int_0^{T_0/2}\left(i_{S7,rms}^2(t) + i_{S8,rms}^2(t)\right)dt} \quad (11)$$

Fig. 6 depicts the average RMS currents $i_{S7,rms}$, $i_{S10,rms}$, and $i_{Lf,rms}$ at different design parameters, i.e., P_{PV}, N_{unit}, and L_f. As can be seen, the RMS currents are remarkably increased with the power rise from 50 W to 300 W. As the increase of N_{unit}, the rms currents also become higher, but the increase is not significant. Furthermore, it is seen that the RMS currents decrease with respect to L_f. However, the decrease becomes insignificant when L_f exceeds a certain value.

III. Parameter Characterization and Electro-thermal Modeling

A. Parameter Characterization of GaN eHEMTs

For the series of 650-V GaN eHEMTs from GaN Systems$^{\mathrm{TM}}$, the current rating and drain-source on-state resistance of a transistor are achieved by employing different standard die units in parallel, as shown in Fig.7. The numbers of die units inside GS66502B, GS66504B, GS66506T and GS66508B are 2, 4, 6, and 8, respectively. Thus, their drain-source on-state resistances at 25 °C are inversely proportional to the number of die units N_{unit}, i.e., $R_{ds,on@20C} = 200$ mΩ for GS66502B [50], 100 mΩ for GS66504B [51], 67 mΩ for GS66506T [52], and 50 mΩ for GS66508B [53].

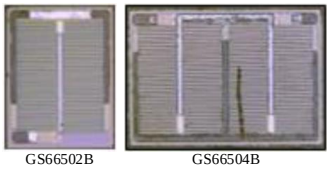
1) Normalized Drain-Source On-State Resistance: Due to the advanced GaNPX® package, a very low parasitic inductance (0.2 nH) can be achieved for the 650-V GaN eHEMTs [54]. As results, a fast turn-on/off is possible, the turn-off loss of a GaN eHEMT can be as low as the energy stored in the parasitic output capacitor, and the drain-source current flowing through the device can be evenly distributed to each die unit. Therefore, the characteristics of a GaN unit are firstly investigated here.

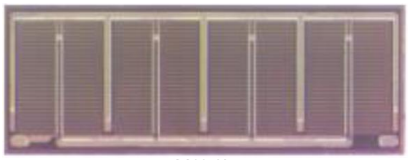
Fig. 8 presents the dependence of the on-state resistance per unit $r_{ds,on}$ on the drain-source current flowing through a die unit, i_{ds} and the junction temperature T_j. As can be seen, the drain-source on-state resistance per GaN unit increases with respect to the junction temperature T_j and drain-source current i_{ds}. All the four GaN eHEMTs have almost the same performance for the normalized on-state resistance $r_{ds,on}$. Therefore, the drain-source on-state resistance of a GaN device with N_{unit} die units can be fitted as

$$R_{ds,on}(I_{ds}, T_j) = \frac{r_a \exp(r_b I_{ds}/N_{unit}) + r_c \exp(r_d I_{ds}/N_{unit})}{N_{unit}} \quad (12)$$

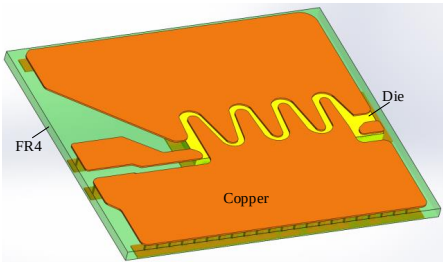
in which $I_{ds} = N_{unit} i_{ds}$ is the total drain-source current flowing through the GaN device, r_a, r_b, r_c, and r_d are junction temperature dependent parameters and can be fitted as $r_a = r_{a1}\exp(r_{a2}T_j)$, $r_b = r_{b1}\exp(r_{b2}T_j)$, $r_c = r_{c1}\exp(r_{c2}T_j)$, and $r_d = r_{d1}\exp(r_{d2}T_j)$, where $r_{a1}, r_{a2}, r_{b1}, r_{b2}, r_{c1}, r_{c2}, r_{d1}$, and r_{d2} are fitted coefficients.

2) Normalized Parasitic Capacitance: The switching performance and gate drive loss depend on the parasitic capacitances of a GaN eHEMT, i.e., the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse capacitance C_{rss}. The capacitances are proportional to the total die area of a GaN eHEMT. Based on the datasheets [50]–[53], the capacitance per unit with respect to the drain-source voltage v_{ds} can be obatined, as shown in Fig.

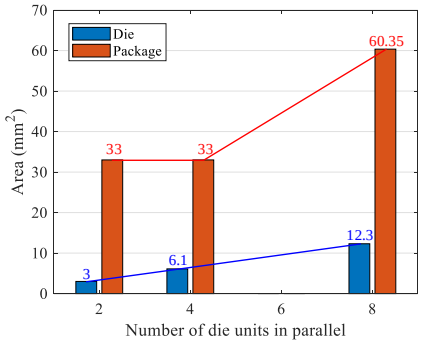




(a)



(b)



(c)

Fig. 7. Die and package of the 650-V GaN eHEMTs of GaN Systems^{TM}. (a) Microscopy images of four 650-V GaN dies [47]; The numbers of die units inside GS66502B, GS66504B, GS66506T and GS66508B are 2, 4, 6, and 8, respectively. The total die area of GS66508P (12.3 mm^2 [48]) is almost twice of that of GS66504B (6.1 mm^2 [49]). (b) Package structure of GaN eHEMT GS66508P built up in Solidworks. (c) Die and package areas of the GaN eHEMTs GS66502B, GS66504B and GS66508B.

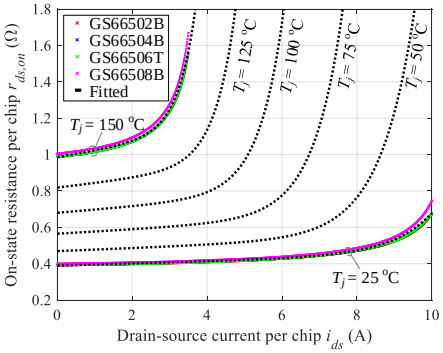


Fig. 8. Drain-source on-state resistance per 650-V GaN die unit of GaN Systems. The crosses represent the values from the datasheets [50]–[53], and the dashed lines are the fitting results.

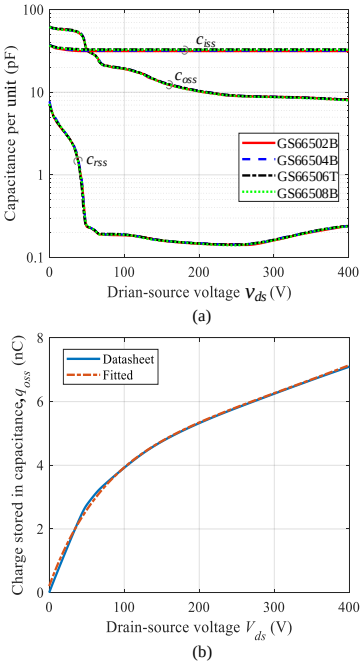


Fig. 9. Normalized capacitance and charge per GaN die unit: (a) output capacitance, reverse capacitance and input capacitance per die unit for a series of 650-V eHEMTs from GaN Systems, GS66502B, GS66504B, GS66506T and GS66508B, (b) fitted charge stored in the output capacitance of a die unit.

9. It is seen that all the investigated GaN transistors, i.e., GS66502B, GS66504B, GS66506T, and GS66508B, share the same normalized capacitance for the three capacitors, c_{iss}, c_{oss}, and c_{rss}. Therefore, the actual parasitic capacitance of a GaN eHEMT can be obtained by $C_{iss} = N_{unit}c_{iss}$, $C_{oss} = N_{unit}c_{oss}$, and $C_{rss} = N_{unit}c_{rss}$.

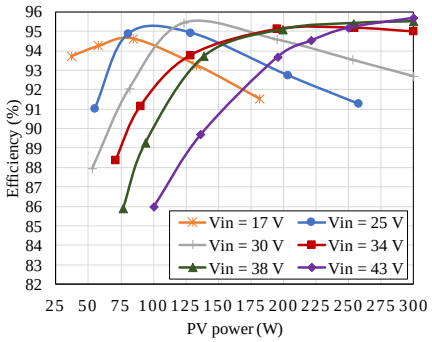


Fig. 10. Measured efficiencies of the dc-dc stage in the PV microinverter prototype.

Particularly, the charge stored in the parasitic output capacitor C_{oss}, i.e., Q_{oss}, determines the ZVS realization of a GaN eHEMT. Therefore, the characteristics of the output charge per unit, q_{oss}, with respect to the drain-source voltage v_{ds} are shown in Fig. 9(b). The parasitic output charge is governed by

$$q_{oss}(V_{ds}) = \int_0^{V_{ds}} c_{oss}(v_{ds})dv_{ds} = \int_{V_{ds}}^0 c_{oss}(v_{ds})dv_{ds} \tag{13}$$

where V_{ds} represents the starting or ending drain-source voltage when charging or discharging the parasitic output capacitor c_{oss}. It can be seen that the parasitic output charge of a GaN device is also proportional to the embedded die units inside. Fitting the normalized output charge yields

$$q_{oss}V_{ds} = q_a \exp(q_b V_{ds}) + q_c \exp(q_d V_{ds}) \tag{14}$$

where q_a, q_b, q_c and q_d are fitted coefficients. Then the actual parasitic output charge Q_{oss} can be derived by $Q_{oss} = N_{unit}q_{oss}$.

B. Power Loss Modeling

1) DC-DC Stage: Since both the dc-dc stage and the inverter stage are integrated into the same PCB, and they will be enclosed by a aluminum case, the power losses of the dc-dc stage will affect the enclosure temperature. Therefore, the power loss characteristic of the dc-dc stage needs to be taken into account. A 60-cell PV module, JinkoSolar JKM300M-60 [55], is assumed to supply the microinverter. The dc-dc stage enables the PV module to operate at maximum power points (MPPs) irrespective of the solar irradiance S_I and ambient temperature T_a. The measured efficiency of the font-stage dc-dc converter is shown in Fig. 10 [18]; then a power loss lookup table can be created with respect to the maximum power point, i.e., the input voltage V_{in} and power P_{in}.

2) GaN eHEMTs $S_7 - S_{10}$: Since all GaN eHEMTs in the inverter stage, i.e., $S_7 - S_{10}$, can achieve ZVS, their switching loss can be neglected. Thus, only the conduction loss $P_{l,S7}$ is taken into account, and it can be obtained as

$$P_{l,S7} = \frac{1}{T_0}\int_0^{T_0} i_{S7}^2(t)R_{ds,on}(i_{S7}, T_j)dt \approx \frac{1}{T_0}\sum_{m=1}^{M} i_{S7,rms}^2(m\Delta t)R_{ds,on}(i_{S7,rms}, T_j)\Delta t \tag{15}$$

where i_{S7} and $i_{S7,rms}$ are the real-time current and rms current flowing through S_7, and $R_{ds,on}$ is the drain-source on-state resistance of S_7. It is noted that $R_{ds,on}$ depends on both the drain-source current i_{S7} and the junction temperature T_j, as illustrated in Fig. 8.

3) Filter Inductor L_f: The planar ER cores have shorter mean turn lengths than EE cores, and therefore provide lower winding resistances for the same core area. The ferrite material 3C95 features a flat power loss density curve with respect to temperature [56]. Hence, the four standard 3C95 ER cores, ER18/3.2/10, ER23/3.6/13, ER25/6/15, ER32/6/25, are chosen as the candidate to implement the filter inductor L_f.

The power losses of the filter inductor L_f consist of the core loss and the winding loss. Since he magnetic cores are excited with nonsinusodial voltages, and the core loss density can be calculated with the improved generalized Steinmetz equation (iGSE) [57]

$$P_v = \frac{1}{T_s}\int_0^{T_s} k_i \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\mathrm{d}t \tag{16}$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\varphi|^{\alpha} 2^{\beta-\alpha} d\varphi} \tag{17}$$

α, β and k are Steinmetz coefficients of the material 3C95, T_s is the excitation period, B is the real-time magnetic flux density, and ΔB is the peak-peak flux density.

Mathematically, the inductor current over a line cycle T_0 can be expressed as a Fourier series. Then, the inductor winding loss $P_{wl,Lf}$ can be obtained by

$$P_{wl,Lf} = \sum_{k=0}^{K} I_{Lf,rms,k}^2 R_{ac,k} \tag{18}$$

where k represents the harmonic order, K is the highest harmonic order considered, $I_{Lf,rms,k}$ is the rms value of the kth harmonic of i_{Lf}, and $R_{ac,k}$ is the resistance of a conductor at the frequency of kf_0.

Meanwhile, the AC resistance of the winding increases dramatically with respect to frequency due to the skin effect and proximity effect, and it can be calculated with the Dowell equation:

$$R_{ac,k} = R_{dc}\frac{\xi}{2}\left(\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2\frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right) \tag{19}$$

where R_{dc} is the dc resistance of a conductor in the winding, $R_{ac,k}$ is the ac resistance of the conductor at the frequency kf_0, $\xi = \sqrt{\pi}d/(2\delta_k)$, d is the conductor diameters, δ_k is the skin depth of the conductor at the frequency kf_0, and m is the number of the layer under consideration.

C. Thermal Modeling

Most of the PV microinverter products on the market are filled up with high-thermal-conductivity compound [14] in order to improve the cooling performance and protect the converters from humidity erosion. For the proposed microinverter, it is implemented with a four-layer PCB and will be enclosed in an aluminum enclosure with a thickness of 2 mm and a dimension of 150 mm $\times$ 100 mm $\times$ 20 mm by natural cooling. Likewise, the enclosure

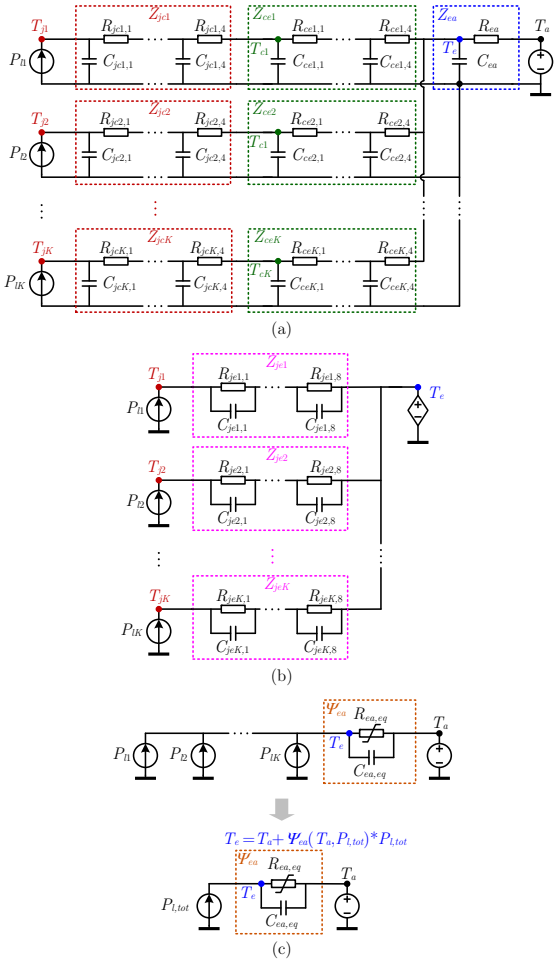


Fig. 11. Thermal impedance network of an enclosed converter system. (a) Junction-ambient thermal impedances represented by Cauer thermal models. (b) Junction-enclosure thermal impedances composed of multi-order Foster thermal models. (c) Equivalent enclosure-ambient thermal impedance represented by a multi-order Foster thermal model.

will be filled up with elastic 2-component polyurethane casting compound whose thermal conductivity (0.7 W/(K·m)) is almost 30 times higher than that of still air [58].

The heat propagation from components to the ambient can be divided into three parts, i.e., from the junction/hotspot to the case, from the case to the enclosure, and from the enclosure to the ambient, as shown in Fig. 11(a). The thermal behavior of a system can be modeled by a series of lumps of thermal resistance R and capacitance C which together are referred as the thermal impedance Z. According to the connection of RC lumps, they can be grouped into the Foster and Cauer-type thermal networks. The Cauer RC network enables the series connection of

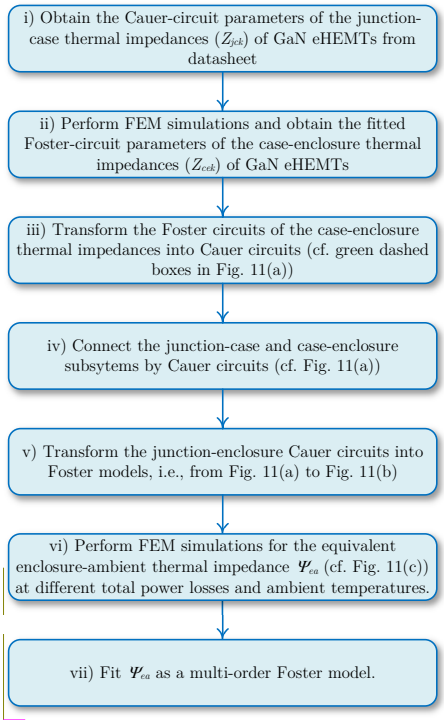


Fig. 12. Proposed flowchart of the thermal impedance network derivation for the long-term junction temperature calculation.

subsystems, and therefore it is considered accurate to predict the temperature of a system [59]. However, the Cauer model parameters are normally hard to derive because the internal geometry, materials, and effective heat path of devices all have to be determined [59].

The Foster RC network is built by fitting the measured temperature dynamics of devices, which means that it is only a behavioral description of a subsystems but no true physical description. Therefore, it is not appropriate to connect multiple Foster-type thermal subsystems; otherwise, there will be a significant error for the temperature prediction [59], [60]. Fortunately, the Foster-type circuit can be transformed into a Cauer circuit which allows for the construction of the thermal models of the complete system [60]. On the other hand, the mathematical representation of the Cauer form is much more complicated than the Foster equation. The Cauer-model parameters cannot be directly used for fast discrete temperature calculation. Therefore, the system-level Cauer model has to be transformed back into a Foster-type circuit for fast discrete temperature calculation.

A system-level thermal modeling method is proposed for the enclosed PV microinverter system, as shown in Fig. 12. With the derived thermal impedances, the junction temperature of the kth eHEMT can be obtained by the

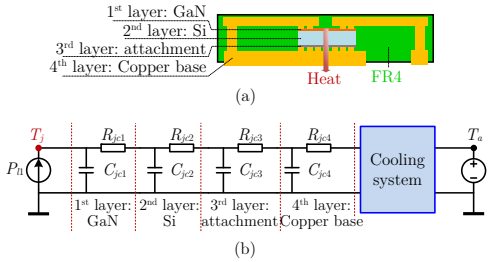


Fig. 13. (a) Vertical structure of a bottom-cooled GaN eHEMT with the GaNPX® package; (b) Four-layer Cauer-type junction-case thermal impedance model.

incremental convolution equations, i.e.,

$$\begin{cases} \Delta T_{jek}(x+1) = \sum_{n=1}^{N} \left[\Delta T_{jek,n}(x) e^{-t/\tau_{k,n}} + P_{lk}(x) R_{k,n}(1 - e^{-t/\tau_{k,n}})\right] \\ \Delta T_{ea}(x+1) = \Delta T_{ea}(x) e^{-t/\tau_{ea,eq}} + P_{l,tot}(x) R_{ea,eq}(1 - e^{-t/\tau_{ea,eq}}) \\ T_{jk}(x+1) = \Delta T_{jek}(x+1) + \Delta T_{ea}(x+1) + T_a \end{cases} \tag{20}$$

where x represents the number of steps in calculation, ΔT_{jek} is the junction-enclosure temperature difference of the kth device, $\Delta T_{jek,n}$ is the junction-enclosure temperature difference calculated by the nth Foster RC lump (i.e., $R_{k,n}$ and $\tau_{k,n}/R_{k,n}$), P_{lk} is the power loss of the device, ΔT_{ea} is the enclosure-ambient temperature difference, and T_a is the ambient temperature.

The detailed thermal modeling of Z_{jc}, Z_{ce} and ψ_{ea} for the PV microinverter system are as follows:

1) Junction-Case Thermal Impedance of GaN eHEMTs: The vertical structure of a bottom-cooled GaN eHEMT with the GaNPX package is shown in Fig. 13(a). For the heat transferred from the junction to case, there are four layers involved, i.e., a GaN die layer, a Si layer, an attachment layer, and a copper base layer. Thus, the Cauer-type junction-case thermal model can be illustrated in Fig. 13(b), where the Cauer-type RC parameters can be derived based on the geometry dimension and material property of each layer. The thermal resistance can be calculated by $R_{th} = d/(\lambda \cdot A_c)$, where d is the layer thickness, λ is the material thermal conductivity in W/(m-K), and A_c is the chip area. The junction-case thermal capacitance is governed by $C_{th} = c \cdot \rho \cdot d \cdot A_c$, where c is the specific heat in Ws/(gK), and ρ is the material density in g/m3. It is obvious that the junction-thermal resistance is theoretically inversely proportional to the total chip area A_c or the number of die units N_{unit} whereas the thermal capacitance is directly proportional to A_c or N_{unit}. The RC parameters of each layer of the 650-V GaN eHEMTs (GS66502B, GS66504B, GS66508B) are extracted from the datasheets [50], [51], [53]. Then the normalized thermal resistance r_{jcn} and capacitance c_{jcn} (i.e., the thermal resistance and capacitance per die unit) can be obtained by $r_{jcn} = R_{jcn} N_{unit}$ and $c_{jcn} = C_{jcn}/N_{unit}$, where n represents the layer number. For different numbers of units N_{unit}, the normalized thermal resistance c_{jcn} and capacitance c_{jcn} of each layer are almost the same, as illustrated in Fig. 14.

The thermal performance of a GaN eHEMT is also determined by the cooling system which may vary significantly with different designs. Most of the PV microinverter products on the market are filled up with high-

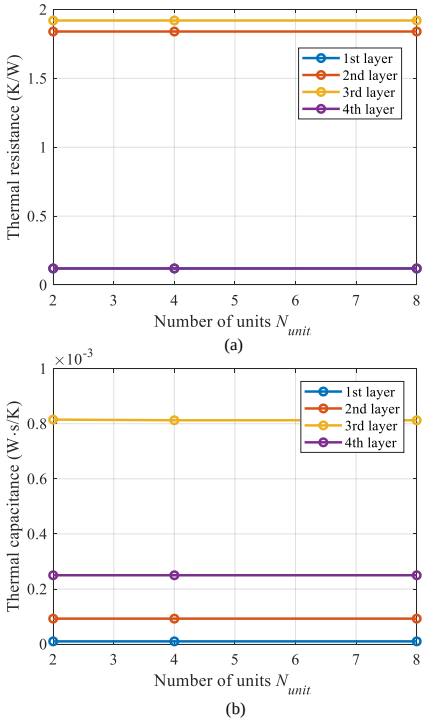


Fig. 14. Normalized thermal resistance and capacitance of each layer for the 650-V GaN Systems eHEMTs GS66502B ($N_{unit} = 2$), GS66504B ($N_{unit} = 4$) and GS66508B ($N_{unit} = 8$). (a) thermal resistance per unit; (b) thermal capacitance per unit.

thermal-conductivity compound [14] in order to improve the cooling performance and protect the converters from humidity erosion. However, the compound reinforces the thermal cross coupling among the components inside the microinverter enclosure. The heat propagation from the components to the ambient can be divided into three parts, i.e., from the junction/hotspot to the case, from the case to the enclosure, and from the enclosure to the ambient. For the first two heat transfer paths, heat conduction is the main way, whereas the third heat transfer path, i.e., from the enclosure to the environment, involves all the three heat transfer approaches, heat conduction, convection and radiation. The heat transfer rate of convection is related to the temperature gap between the enclosure surface and the circumstance, whereas the radiation intensity depends on the absolute temperatures [**?**]. The participation of convection and radiation makes the whole thermal system nonlinear [14].

2) Case-Enclosure and Junction-Enclosure Thermal Impedance of GaN eHEMTs: The conduction is the main heat transfer way inside the compound-filled enclosure. For the heat transfer from the case to the enclosure, it is quite difficult to perform an analytical characterization because of the irregular geometry of heat transfer medium. Hence, detailed structure models of all main components, enclosure, and PCB (including traces and vias) are built in ANSYS/Icepak based on real dimensions and material properties, as shown in Fig. 15. To extract the

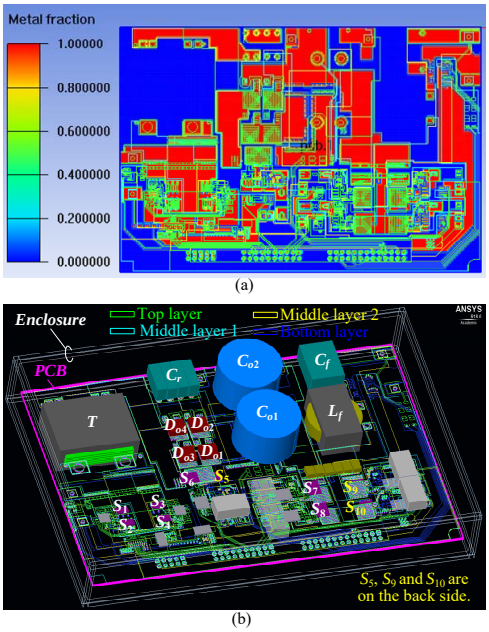


Fig. 15. FEM simulation model built in Ansys/Icepak. (a) Percentage of copper on the PCB top layer; (b) Enclosure, PCB (including traces and vias) and main components of the PV microinverter.

case-enclosure thermal impedance of eHEMTs, multiple system-level FEM simulations are conducted for the three cases of $S_7 - S_{10}$ being implemented with GS66502B, GS66504B or GS66508B, as shown in Fig. 16(a). Since GS66502B and GS66504B have the same package dimension, their case-enclosure thermal impedances are the same. Meanwhile, it is noticed that the Z_{ce} difference among $S_7 - S_{10}$ are negligible. Therefore, the average Z_{ce} of $S_7 - S_{10}$ is obtained to represent their case-enclosure thermal impedance, as shown in 16.

Then, the average Z_{ce} curves are fitted as multiorder Foster models which are further transformed into Cauer models with the method proposed in [60]. Thus, the junction-case and case-enclosure Cauer-type RC circuits can be connected in series, as shown in 17. At low and high frequencies, Z_{je} is dominated by Z_{ce} and Z_{jc}, respectively. Finally, the junction-enclosure thermal impedance curves are fitted as multiorder Foster models in order to perform fast numerical calculation for one year data.

3) Enclosure-Ambient Thermal Impedance of System: All the three heat transfer ways, i.e., conduction, convection and radiation, are involved in the heat propagation from the enclosure to ambient environment. Therefore, its heat transfer coefficient depends on the temperatures of enclosure and ambient environment. The enclosure has a thickness of 2 mm and is made of aluminum with a high thermal conductivity (205 W/(m·K)). Thus, the enclosure is almost isothermal. To obtain the equivalent enclosure-ambient thermal impedance ψ_{ea} (see 11), multiple FEM simulations are conducted at different total power losses and ambient temperatures, as shown in 18. Then, the FEM simulation

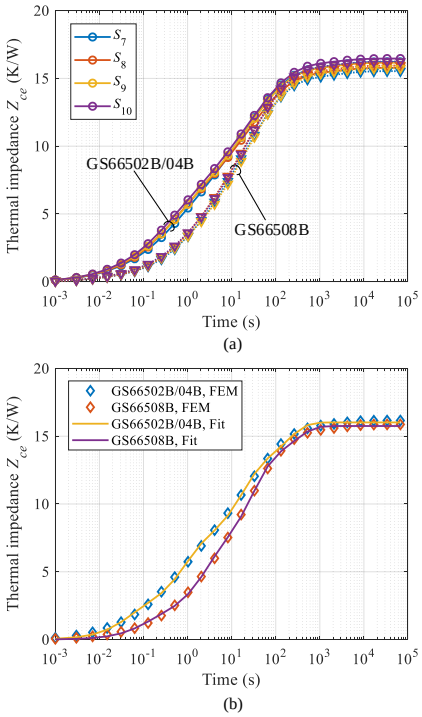


Fig. 16. Case-enclosure thermal impedance of $S_7 - S_{10}$ implemented with different GaN eHEMTs (GS66502B, GS66504B and GS66508B): (a) FEM simulations for $S_7 - S_{10}$, (b) fitted case-enclosure thermal impedance.

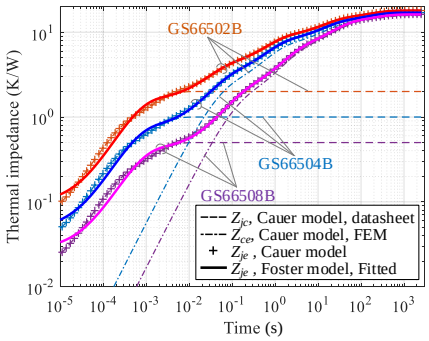
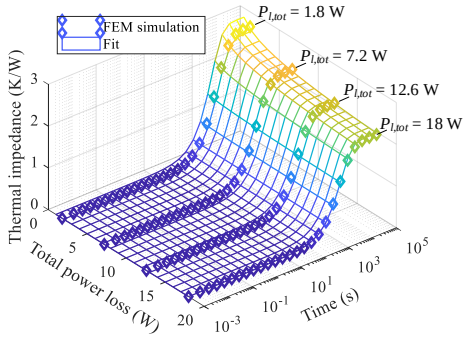


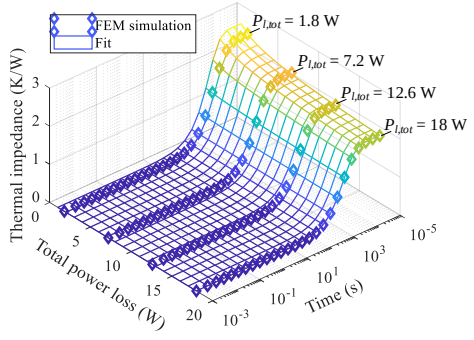
Fig. 17. Junction-enclosure thermal impedance of GaN eHEMTs GS66502B, GS66504B and GS66508B.

results are fitted as a first-order Foster model

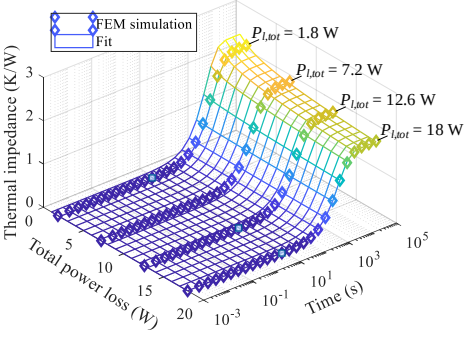
$$\psi_{ea} = R_{ea,eq}\left(1 - e^{-t/(R_{ea,eq}C_{ea,eq})}\right) \tag{21}$$



(a)



(b)



(c)

Fig. 18. Equivalent enclosure-ambient thermal impedance ψ_{ea} at different ambient temperatures and power losses: (a) the ambient temperature $T_a = 20°\text{C}$, (b) $T_a = 40°\text{C}$, (c) $T_a = 60°\text{C}$.

where $C_{ea,eq}$ is found to be constant as 1100 J/K but $R_{ea,eq}$ is a function of the total power loss and ambient temperature, i.e., $R_{ea,eq} = (1.742 P_{l,tot}^{-0.114})(1.8 - 7.48 \times 10^{-3} T_a)$.

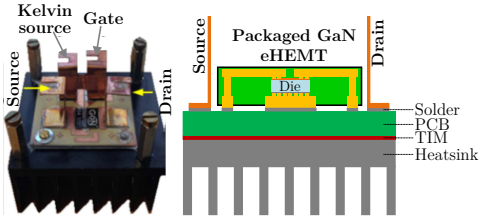


Fig. 19. Photo of vertical structure of a device under test.

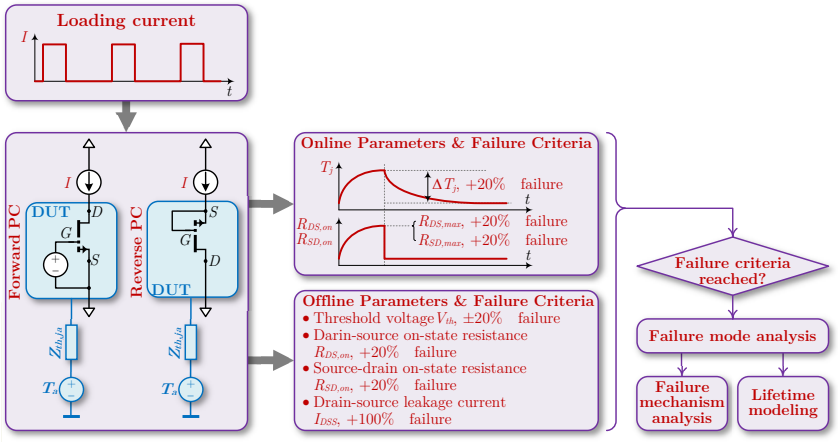


Fig. 20. Principle of the DC power cycling test.

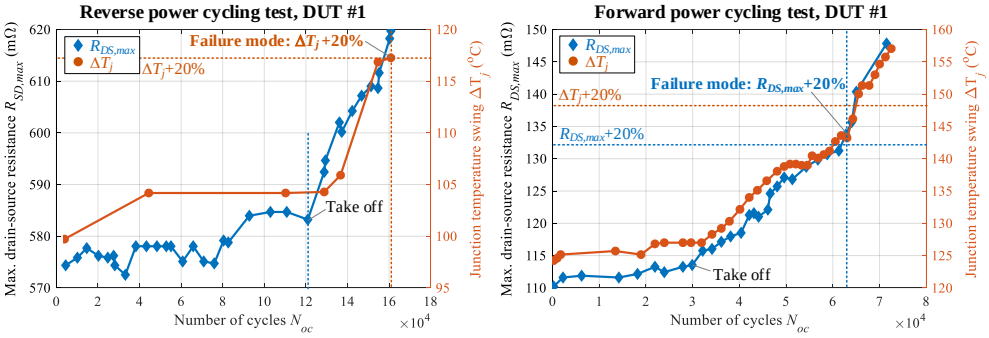


Fig. 21. Measured maximum source-drain/drain-source on-state resistance $R_{SD,max}/R_{DS,max}$ and junction temperature swing ΔT_j with respect to the number of cycles N_{oc} for the forward and reverse power cycling tests. The two parameters, $R_{SD,max}/R_{DS,max}$ and ΔT_j are monitored online by an oscilloscope and an infrared thermal camera, respectively.

IV. Modeling of Lifetime, Cost and Volume

A. Lifetime Modeling of GaN eHEMT

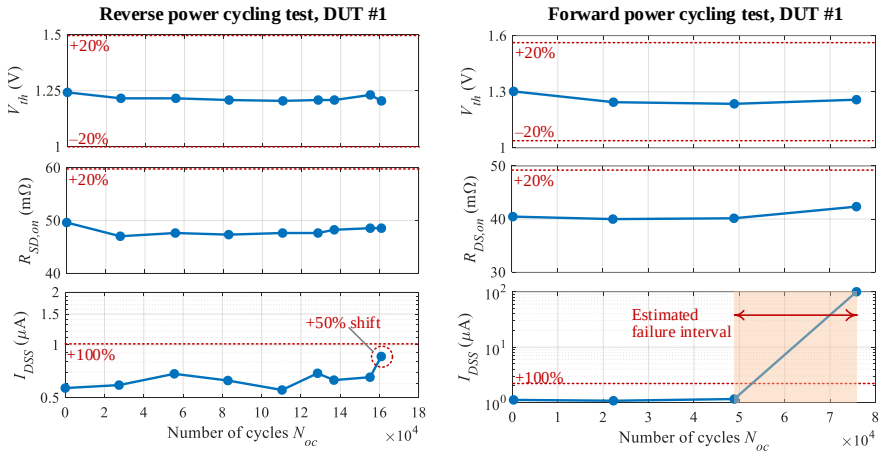


Fig. 22. Measured threshold voltage V_{th}, source-drain/drain-source on-state resistance $R_{SD,max}/R_{DS,max}$, and drain-source leakage current I_{DSS} with respect to the number of cycles for the forward and reverse power cycling tests. The devices under test are periodically detached from the power cycling test setup, and then these offline parameters can be periodically measured by using a curve tracer.

TABLE I

RESULTS OF THE POWER CYCLING TESTS ON SIX GS66508P SAMPLES

DUT No.	Junction temperature swing ΔT_j (°C)	Mean junction temperature T_{jm} (°C)	No. of cycles to failure N_{ocf}	Mean No. of cycles to failure $N_{ocf,m}$	Failure mode
#1 Reverse mode	99.9	101.1	160×10^3	160×10^3	$\Delta T_j + 20\%$
#2 Reverse mode	/	/	$74 \times 10^3 - 106 \times 10^3$	90×10^3	$I_{DSS} + 100\%$
#3 Reverse mode	100.2	102.4	$214 \times 10^3 - 305 \times 10^3$	260×10^3	$I_{DSS} + 100\%$
#1 Forward mode	124.2	85.8	$49 \times 10^3 - 73 \times 10^3$	61×10^3	$R_{DS,max} + 20\%$ $I_{DSS} + 100\%$
#2 Forward mode	124.1	88.3	22×10^3	22×10^3	$R_{DS,max} + 20\%$
#3 Forward mode	120.1	86.2	38×10^3	38×10^3	$R_{DS,max} + 20\%$

1) Power Cycling Tests: DC power cycling (PC) tests [61] on the GaN eHEMT GS66508P have been conducted to obtain the degradation characteristic and lifetime model of the 650-V GaN eHEMTs with respect to thermal stresses. The photo and vertical structure of a device under test (DUT) are shown in Fig. 19 , and the principle of the DC power cycling test [54], [62], [63] is illustrated in Fig. 20. The tests are divided into two types: forward PC test and reverse PC test.

- *Forward PC Test:* in this mode, the gate of the DUT, i.e., a GaN eHEMT, is always triggered, and a periodical forward current I flows through the transistor. Then the conduction loss generated inside the DUT heats up itself periodically.
- *Reverse PC Test:* in this mode, the periodical current I flows through the DUT in the reverse direction, i.e., from the source to the drain. Likewise, the DUT is heated up periodically by its conduction loss.

During the PC tests, a few critical parameters are measured online or offline to diagnose the normality of an aging DUT. The online parameters, i.e., the junction temperature swing ΔT_j and the maximum source-drain/drain-source

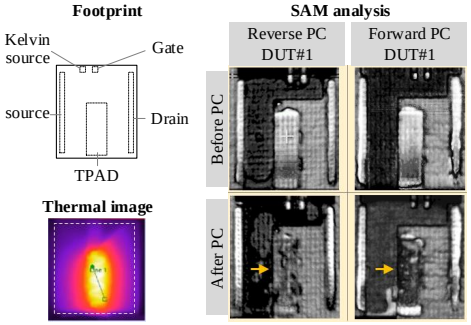


Fig. 23. SAM images of DUTs before and after PC tests.

on-state resistance $R_{DS,max}/R_{SD_max}$, are monitored in real time during the PC by an infrared thermal camera and an oscilloscope, respectively. For the offline parameters, i.e., the gate-source threshold voltage V_{th}, the drain-source on-state resistance $R_{DS,on}$, the source-drain on-state resistance $R_{SD,on}$, and the drain-source leakage current I_{DSS}, they are measured periodically by detaching the DUT from the PC test setup and using a curve tracer. The online and offline parameters are used to indicate the degradation of the DUT with respect to the number of cycles. Compared with the initial values before PC, a $+20\%$ increase in ΔT_j, $R_{DS,max}$, $R_{SD,max}$, $R_{DS,on}$ or $R_{SD,on}$, a $\pm 20\%$ change in V_{th}, or a $+100\%$ increase in I_{DSS} during the PC test indicates the failure of the DUT. Finally, the failure mode and mechanism can be analyzed, and a preliminary lifetime model can be derived.

As shown in Table I, two sets of PC tests on six DUTs have been carried out under two different stress conditions: 1) 3 DUTs in the reverse mode, the junction temperature swing $\Delta T_j \approx 100$ °C and the mean junction temperature $T_{jm} \approx 100$ °C; 2) 3 DUTs in the forward mode, $\Delta T_j \approx 125$ °C and $T_{jm} \approx 87.5$ °C. DUT#1 in the reverse mode and DUT#1 in the forward mode are selected as a representative for each stress condition. Fig. 21 shows the online parameters $R_{SD,max}/R_{DS,max}$ and ΔT_j with respect to the number of cycles N_{oc}. As can be seen, both online parameters are maintained at the levels close to the initial values at the early life stages. When the number of cycles N_{oc} exceeds a certain point, both online parameters start taking off, i.e., rise sharply over N_{oc}.

Fig. 22 presents the measured data of offline parameters for the DUT#1 in the reverse mode and the DUT#1 in the reverse mode. Significant changes in V_{th} and $R_{SD,on}/R_{DS,on}$ have not been observed by the end of the tests. For the drain-source leakage current I_{DSS}, however, there is a pronounced variation observed. As aforementioned, six DUTs in total have been tested. A noticeable I_{DSS} rise occurs to five of the six GaN transistor samples. The failure modes of three DUTs are I_{DSS} failure. It should be noted that if the failure is decided by the offline parameters, then the number of cycles to failure is an interval, instead of an exact number as the offline characterization is conducted infrequently.

2) Failure Mechanism Analysis: Two failure phenomena of GaN eHEMTs have been observed: thermal conductivity degradation and I_{DSS} failure [54], [62], [63]. For the thermal conductivity degradation of semiconductor devices, it can be explained by the bond wire lift off and solder joint fatigue from thermo-mechanical stresses [64]. There is no bond wire used in the GaNPX® package; therefore, the solder joint fatigue is the main failure

mechanism. The solder joint fatigue of the aged samples is investigated by scanning acoustic microscope (SAM) analysis. Fig. 23 presents the thermal image taken from the topside of a GaN DUT during PC and the SAM images of DUTs before and after PC tests. It is seen that the thermal stress is mainly focused on the thermal pad (TPAD) region of the discrete GaN device. Normal quality of the solder joints is observed in the SAM images before the PC test, whereas the apparent delamination of solder joints can be observed from the SAM images after the PC test. The solder joint delamination under the TPAD confirms the observed thermal conductivity degradation during PC tests (see Fig. 21).

The second failure mode is the drain-source leakage current I_{DSS} increase. The failures of DUTs#2#3 in the reverse mode and DUT#1 in the forward mode are decided by the I_{DSS} limit. The in-depth analysis on the I_{DSS} failure can be found in [63]. It is confirmed in [63] that the cause of the I_{DSS} failure lies in the GaN semiconductor device, instead of the DUT structure or the GaNPX® package.

3) Preliminary Lifetime Model: The relationship between the number of cycles to failure N_{ocf} of a GaN HEMT and the applied stresses (mean junction temperature T_{jm} and junction temperature swing ΔT_j) can be modeled by the Coffin-Manson-Arrhenius equation [65]:

$$N_{ocf} = A(\Delta T_j)^{-n} \exp\left(\frac{E_a}{k_b(T_{jm}+273)}\right) \tag{22}$$

where the activation energy E_a = 1.8 eV [66], k_b = 8.62 $\times$ 10^{-5} eV/K is the Boltzmann constant, and the two parameters $A = 1.92 \times 10^{11}$ and $n = 15.18$ are obtained from the DC power cycling test results (see Table I). It should be noted that the built lifetime for the 650-V GaN eHEMTs is preliminary and needs more comprehensive experimental verifications. Nevertheless, it is used in this research to evaluate the wear-out performance of GaN eHEMTs.

As for the damage accumulation, the commonly used Miners rule, which assumes that the damage accumulates linearly [67], is employed, i.e.,

$$D_{mg} = \sum_k \frac{N_{oc,k}}{N_{ocf,k}} \tag{23}$$

where $N_{ocf,k}$ is the number of cycles to failure under the specific T_{jm} and ΔT_j, and $N_{oc,k}$ is the number of cycles of the same loading stress during the period of operation time under consideration. The device fails when the damage D_{mg} is accumulated to 1.

B. Cost and Volume Modeling of GaN eHEMT and Planar Inductor

1) Cost: A survey on the market price of 650-V GaN eHEMTs, 3C95 ER magnetic cores and Litz wires was conducted at Mouser Electronics™ [68], Digi-Key Electronics™ [69] and HSM Wire™ [70] in spring 2018. The minimum ordering quantities (MOQs) are 1000 pieces for the GaN transistors, 500 sets for the magnetic cores, and 50 kg for the Litz wires. Fig. 24(a) shows the market price of GaN eHEMTs with different numbers of die units. As can be seen, the transistor price increases linearly with respect to the number of die units N_{unit} inside the transistor. The price of GaN Systems 650-V eHEMTs can be fitted as [71]

$$C_{ost} = C_{ost,pack} + c_{ost,unit} N_{unit} \tag{24}$$

where $c_{ost,unit} = 1.1$ €/unit is the specific price per die unit and $C_{ost,pack} = 6$ € is the package related price.

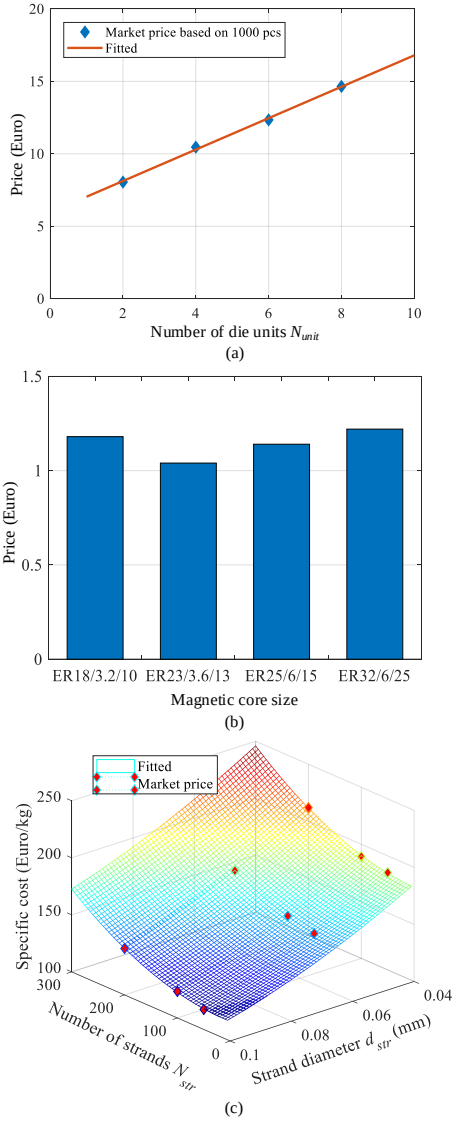


Fig. 24. Market prices of (a) GaN Systems 650-V GaN eHEMTs with different number of die units, (b) magnetic cores with different sizes, and (c) Litz wires with different numbers of strands N_{str} and strand diameters d_{str}.

The prices of 3C95 ER cores from Ferroxcube$^{\text{TM}}$ are shown in Fig. 24(b). It is seen that the price increases with respect to the core size for the three big cores, ER23/3.6/13, ER25/6/15 and ER32/6/25. For ER18/3.2/10, it has the smallest size and therefore has the least material consumption. However, the small size of ER18/3.2/10 may increase

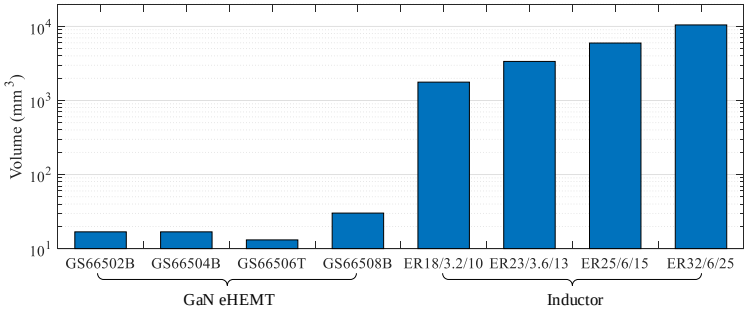


Fig. 25. Volume of GaN eHEMTs and inductors.

the manufacturing cost. Hence, the smallest size of core, ER18/3.2/10, is not the cheapest. Nevertheless, there is no significant price difference among the four selected cores. The inductor core price only takes about $2\% - 3.8\%$ of that of four GaN eHEMTs. Therefore, the cost of the inverter stage is dominated by the GaN eHEMTs.

For the cost of Litz wire in the inductor L_f, it depends on many factors, e.g., the number of strands N_{str}, the strand diameter d_{str}, the minimum order quantity, and the market copper price [72]. Multiple quotas were made at HSM Wire$^{\text{TM}}$ [70] for the Litz wires with difference parameters, as shown in Fig. 24(c). It is seen that the specific cost of Litz wire increases with respect to the increase of N_{str} and the decrease of d_{str}, and can be fitted as

$$c_{ost,Litz} = c_0 + c_{N1}N_{str} + c_{d1}d_{str} + c_{N2}N_{str}^2 + c_{Nd}N_{str}d_{str} + c_{d2}d_{str}^2 \tag{25}$$

where $c_0, c_{N1}, c_{d1}, c_{N2}, c_{Nd}$ and c_{d2} are fitting parameters.

2) Volume: The volumes of the 650-V GaN eHEMTs and ER cores are calculated based on the datasheets [50]–[53], [73], as shown in Fig. 25. The gate drive circuits are the same for different GaN eHEMTs, i.e., GS66502B/04B/06T/08B. Therefore, the only difference lies in the volumes of themselves. However, the largest size of GaN eHEMT, GS66508B, only accounts for 1.5% of the volume of the smallest inductor ER18/3.2/10. Therefore, the volume of the inverter stage is dominated by the inductor L_f.

V. Cost-Volume-Reliability Pareto Optimization of the Microinverter

A. Design Flowchart

A cost-volume-reliability Pareto optimization scheme is proposed for the microinverter, as shown in Fig. 26. The system specifications, i.e., the dc-link voltage V_{dc}, the grid voltage V_g, the maximum input power $P_{PV,max}$, and the real-field mission profile (solar irradiance S_I and ambient temperature T_a), are predetermined parameters. Regarding the design variables, multiple parameters can be identified, including the power P_{dzn} at which the inductor is optimized, the filter inductance L_f, the number of die units (N_{unit} representing the current rating) inside a GaN eHEMT for $S_7 - S_{10}$, the magnetic core dimension D_{core} and Litz wire gauge G_{Litz} for L_f. The first three design parameters, P_{dzn}, N_{unit}, and L_f, influence the inductor current and switching frequency, whereas

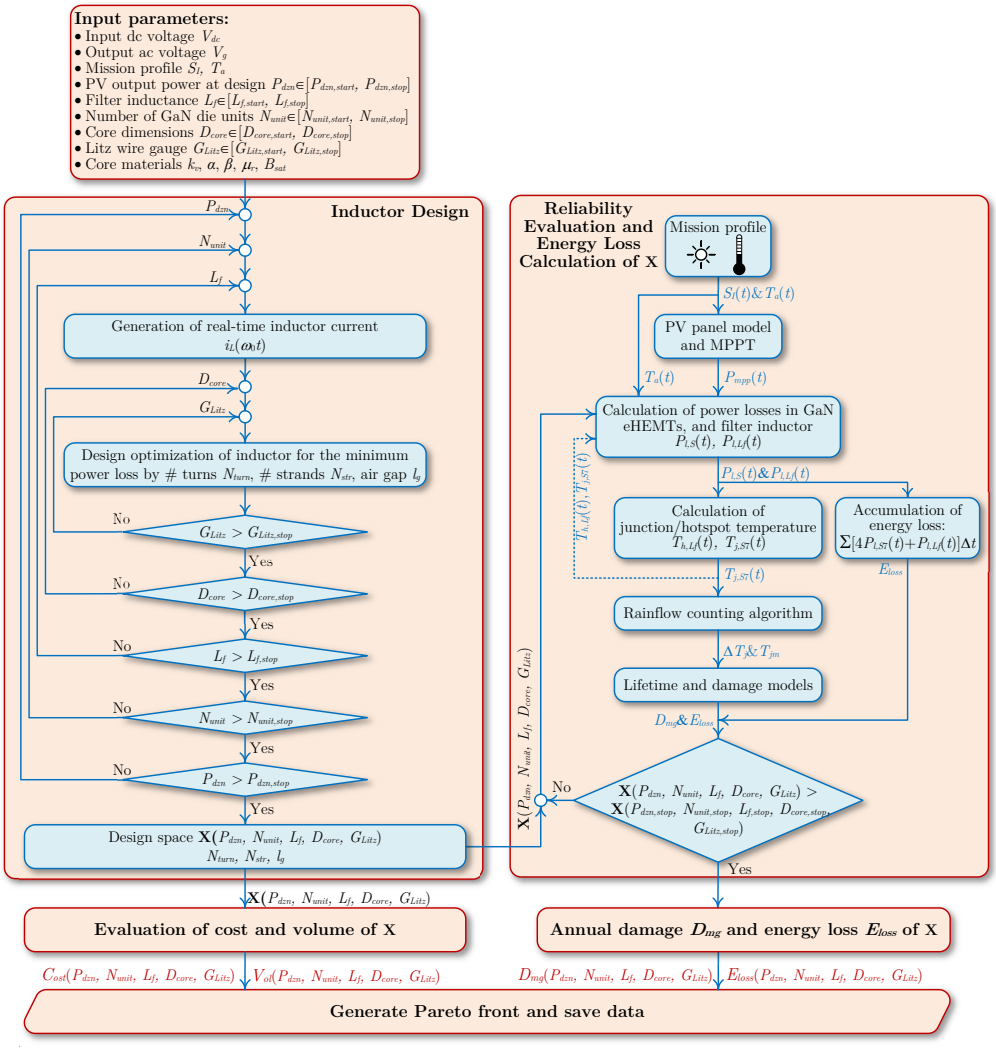


Fig. 26. Flowchart of the proposed reliability-oriented design.

D_{core} and G_{Litz} only affect the inductor design optimization. Each design parameter is defined as a vector and its value varies within a range.

Firstly of all, each combination of P_{dzn}, N_{unit}, and L_f is used to generate the real-time inductor current $i_L(\omega_0 t)$, over a line cycle. Together with different magnetic core dimensions D_{core} and Litz wire gauges G_{Litz}, the derived real-time current is then used to optimize the inductor design, yielding the optimal inductor parameters (i.e., the

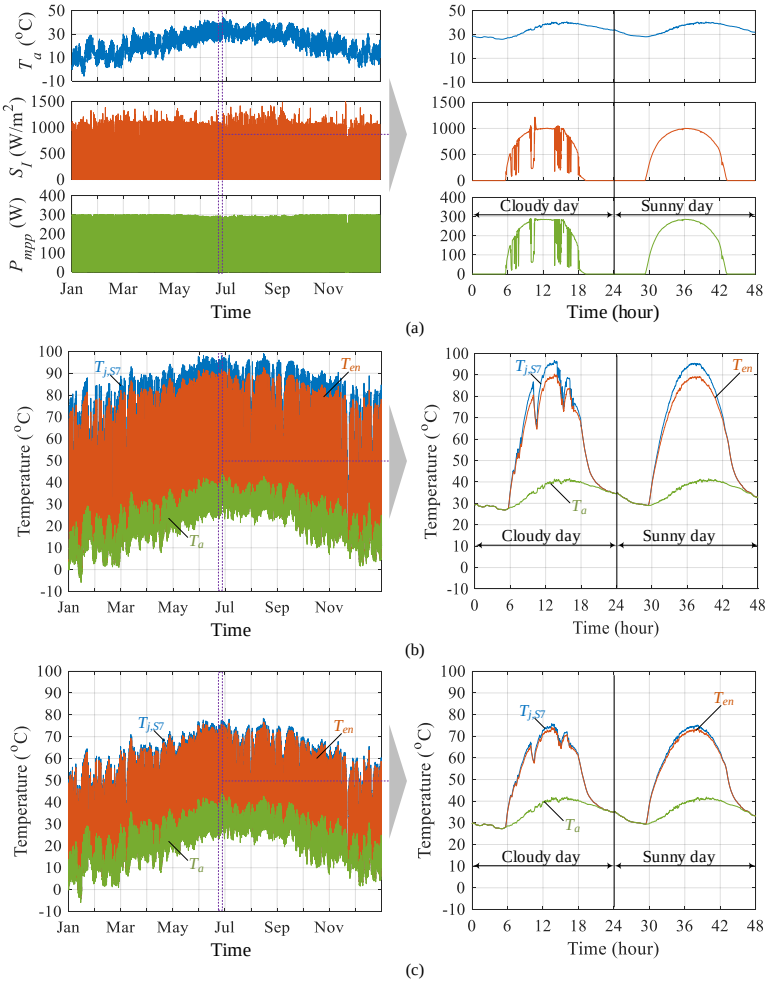


Fig. 27. Mission profile and calculated annual temperature profiles of the GaN eHEMT junction and the enclosure when the PV microinverter operates in Arizona, US. (a) Annual mission profile: the ambient temperature T_a, the solar irradiance S_I, and the maximum power P_{mpp} with the 60-cell PV module, JinkoSolar JKM300M-60; (b) Temperature profiles of the microinverter with design parameter set A: $P_{dzn} = 300$ W, $S_7 - S_{10}$ = GS66502B (N_{unit} = 2), $L_f = 375$ μH, inductor core D_{core} = ER18/3.2/10, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields $N_{turn} = 173$, $N_{str} = 19$, and $l_g = 0.303$ mm. (b) Temperature profiles of the microinverter with design parameter set B: $P_{dzn} = 250$ W, $S_7 - S_{10}$ = GS66508B (N_{unit} = 8), $L_f = 125$ μH, inductor core D_{core} = ER32/6/25, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields $N_{turn} = 20$, $N_{str} = 481$, and $l_g = 0.142$ mm.

number of turns N_{turn}, the number of strands N_{str}, and the air gap l_g) for the minimum inductor power loss. Thus, a design space $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$ can be obtained and further evaluated with respect to the cost and volume characteristics.

Then, the reliability and annual energy loss of the design space $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$ are assessed, as shown on the right red block of Fig. 26. The real-field mission profile, i.e., the solar irradiance (S_I) and ambient temperature T_a directly determines the electrical and thermal loadings, and thus affects the degradation process of the components inside the PV microinverter. With a PV panel model and an MPPT control algorithm, the long-term mission profile can be translated into the real-time voltage and power at the maximum power point, $V_{PV,mpp}(t)$ and $P_{PV,mpp}(t)$, which are the input of the microinverter. Then the real-time power $P_{PV,mpp}(t)$ and ambient temperature T_a are sent to calculate the power losses of the GaN eHEMTs and the inductor with the design database $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$. The thermal impedance model built in Section III-C is subsequently utilized to calculate the junction temperature of the GaN eHEMTs and the hotspot temperature of the inductor. Due to the interdependece of the power losses and the junction temperature, multiple iterations will be executed in this stage. The rainflow counting algorithm [74] is employed to extract the number of temperature cycles with different characteristics (e.g., the mean junction temperature T_{jm}, and the temperature swing ΔT_j). After that, the lifetime and damage accumulation models (22)-(23) can be used to estimate the accumulated damage over a year. Meanwhile, the annal energy loss on the GaN eHEMTs and inductor can also be calculated for each design. As results, the annual damage D_{mg} and energy loss E_{loss} of the whole design database $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$ can be obtained.

Four objectives are selected for the inverter, i.e., the cost of GaN eHEMTs and inductor $\mathbf{C_{ost}}$, the inductor volume $\mathbf{V_{ol}}$, the annual damage of GaN eHEMTs $\mathbf{D_{mg}}$, and the annual energy loss of the inverter stage $\mathbf{E_{l,inv}}$. It is preferable to minimize all these objectives, $\mathbf{C_{ost}}(\mathbf{X})$, $\mathbf{V}_{ol}(\mathbf{X})$, $\mathbf{D_{mg}}(\mathbf{X})$, $\mathbf{E_{l,inv}}(\mathbf{X})$ in the design space $\mathbf{X}(P_{dzn}, N_{unit}, L_f, D_{core}, G_{Litz})$. With the multiobjective genetic algorithm [75], the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$-$\mathbf{D_{mg}}$ Pareto-optimal front can be generated, which could help designers make the trade-off among cost, volume, energy loss and reliability.

B. Cost-Volume-Reliability/Energy Loss Pareto Optimization

As a case study, it is assumed that the PV microinverter will be operating in Arizona, US, where the solar irradiance is abundant over the whole year. Fig. 27(a) shows its annual solar irradiance S_I and ambient temperature T_a. As can be seen, its maximum daily solar irradiance is approximately 1000 W/m^2 throughout the whole year.

A 60-cell PV module, JinkoSolar JKM300M-60, is assumed to supply the microinverter. The dc-dc stage enables the PV module to operate at the maximum power points (MPPs) irrespective of the solar irradiance S_I and ambient temperature T_a. Based on the I-V characteristics of the PV module JinkoSolar JKM300M-60, the annual PV output power at the maximum power point P_{mpp} can be obtained, as shown in Fig. 27(a).

Five design variables have been identified and their ranges are as follows:

- the power on which the design is based, P_{dzn} = 50 W, 100 W, ..., 300 W;
- the number of die units inside the GaN eHEMT, N_{unit} = 2, 4, 8;
- the filter inductance, $L_f = 50\mu$H, 75μH, ..., 375μH;
- the core dimension of L_f, D_{core} = ER18/3.2/10, ER23/3.6/13, ER25/6/15, ER32/6/25;
- the Litz wire gauge of L_f, G_{Litz} = AWG38, AWG40, AWG42, AWG44, AWG46.

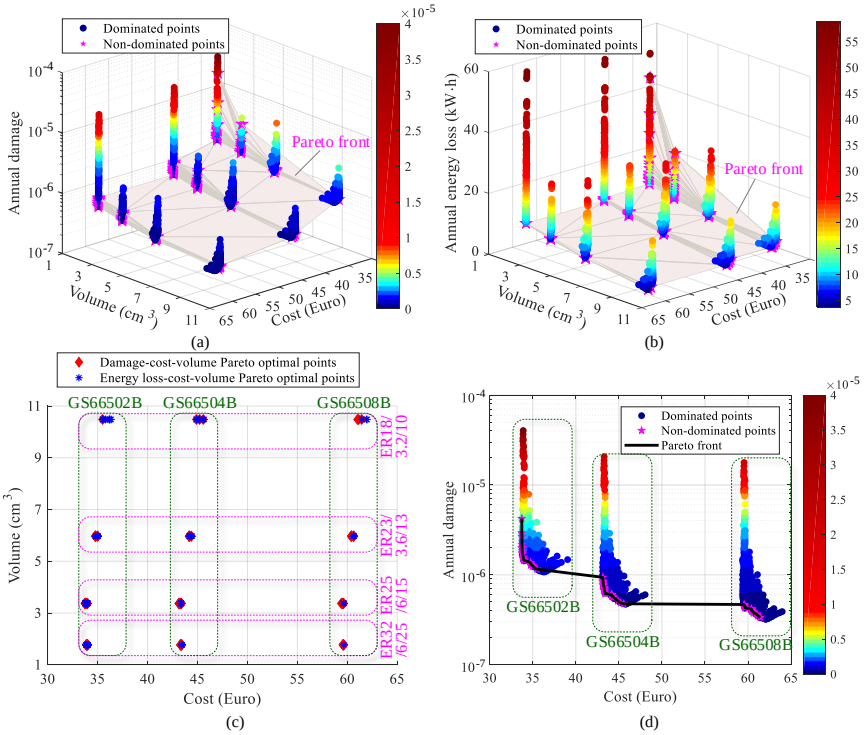


Fig. 28. Inverter cost, inductor volume, annual energy loss and annual damage for each design in the space **X**: (a) $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ Pareto-optimal front; (b) $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal front; (c) projection of the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal points on the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$ plane; (d) $\mathbf{C_{ost}}$-$\mathbf{D_{mg}}$ Pareto-optimal front.

With the proposed reliability-oriented design method (see Fig.26), a space or database containing 5040 design options can be generated. For each design, the inductor is optimized to achieve the minimum power loss by finely tuned parameters, i.e., the number of turns N_{turn}, the number of strands N_{str} and the length of air gap l_g.

Figs. 27(b) and (c) show the junction and enclosure temperature profiles of the PV microinverter with two design cases:

Case A: $P_{dzn} = 300$ W, $S_7 - S_{10}$ = GS66502B (N_{unit} = 2), $L_f = 375$ μH, inductor core D_{core} = ER18/3.2/10, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields $N_{turn} = 173$, $N_{str} = 19$, and $l_g = 0.303$ mm;

Case B: $P_{dzn} = 250$ W, $S_7 - S_{10}$ = GS66508B (N_{unit} = 8), $L_f = 125$ μH, inductor core D_{core} = ER32/6/25, Litz wire gauge G_{Litz} = AWG46; in this case, the inductor optimization yields $N_{turn} = 20$, $N_{str} = 481$, and $l_g = 0.142$ mm.

As can be seen, the maximum junction temperature of GaN eHEMTs with *Case A* reaches 99 °C, whereas *Case B* enables $T_{j,S7}$ to fall to 78 °C. With a 21-°C decrease for the maximum junction temperature, the annual

damage is reduced from 7×10^{-6} to 4×10^{-7}. A two-day mission profile and junction temperature profiles are also given in Fig. 27 to make a comparison between the sunny day and cloudy day. When operating in a sunny day, the temperature profiles of the microinverter are smooth due to smooth solar irradiance. In the cloudy condition, the solar irradiance varies significantly, then the temperature profiles change as well. However, the temperature changes are not as drastic as S_1 due to the thermal capacitances of materials.

For each design in the space $\mathbf{X}$, the inverter cost, inductor volume, annual inverter energy loss, and annual damage of GaN eHEMTs are evaluated and shown in Fig. 28(a) and (b). Then the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal fronts can be identified, as indicated in Fig. 28(a) and (b), respectively. The design variables have a significant impact on both the annual inverter energy loss and the annual damage of GaN eHEMTs. The Pareto-front can help to significantly reduce the annual damage and energy loss. Fig. 28(c) depicts the projection of the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal points on the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$ plane. As can be seen, the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{D_{mg}}$ and $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$-$\mathbf{E_{l,inv}}$ Pareto-optimal points almost overlap on the $\mathbf{C_{ost}}$-$\mathbf{V_{ol}}$ plane, implying that the annual damage is monotone with respect to the annual energy loss. The minimum annual damage of GaN eHEMTs and the minimal annual inverter energy loss can be simultaneously obtained. Fig. 28(d) shows the $\mathbf{C_{ost}}$-$\mathbf{D_{mg}}$ Pareto-optimal front of the inverter stage. It is seen that the overall cost is dominated by the employed GaN eHEMTs.

VI. Conclusion

This paper discusses the cost-volume-reliability Pareto optimization of a PV microinverter. The operation principle and characteristics of the inverter are analyzed, and the models of power loss, thermal impedance, lifetime, cost and volume are built for main components. Finally, a cost-volume-reliability Pareto optimization method is proposed and executed, yield a Pareto front which enables a design trade-off among the three performance metrics. At a similar cost and volume, the proposed design could significantly reduce the annual damage and energy loss for the studied microinverter.

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Paper F

Wear-out Failure Analysis of an Impedance-Source PV Microinverter Based on System-Level Electro-Thermal Modeling

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Wear-out Failure Analysis of an Impedance-Source PV Microinverter Based on System-Level Electro-Thermal Modeling

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***Abstract*—The wear-out performance of an impedance-source photovoltaic (PV) microinverter (MI) is evaluated and improved based on two different mission profiles. The operating principle and hardware implementation of the MI are firstly described. With the experimental measurements on a 300-W MI prototype and system-level finite element method (FEM) simulations, the electro-thermal models are built for the most reliability-critical components, i.e., power semi-conductor devices and capacitors. The dependence of the power loss on the junction/hotspot temperature is considered, the enclosure temperature is taken into account, and the thermal cross-coupling effect between components is modeled. Then the long-term junction/ hotspot temperature profiles are derived and further translated into components' annual damages with the lifetime and damage accumulation models. After that, the Monte Carlo simulation and Weibull analysis are conducted to obtain the system wear-out failure probability over time. It reveals that both the mission profile and the thermal cross-coupling effect have a significant impact on the prediction of system wear-out failure, and the dc-link electrolytic capacitor is the bottleneck of long-term reliability. Finally, the multi-mode control with a variable dc-link voltage is proposed, and a more reliable dc-link electrolytic capacitor is employed, which results in a remarkable reliability improvement for the studied PV MI.**

***Index Terms*—PV microinverter, reliability, wear out, electro-thermal modeling**

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I. Introduction

Over the last decade, the solar photovoltaic (PV) energy continues to experience a significant growth tendency due to the dramatic price reduction of PV modules in the world market [1], and the progressive evolution of PV converters whose efficiency has been reported as high as 99% [2].

Compared to the central and string PV inverters, the microinverters (MIs) feature more advantages in low power applications such as module-level maximum power point tracking (MPPT), low PV-system installation effort, and easy condition monitoring and failure detection [3]-[5]. However, there are also some challenges for PV MIs. First, the MIs are normally cooled by natural convection and they are installed close to the PV module, which means that they can be subjected to a more extreme environment than central inverters typically located in climate controlled environment [6]-[7]. In addition, there is a trend that the MI will be incorporated into the module frame in the future [6]. The lifetime/warranty of PV modules is about 25 years, but the inverters have to be replaced every 5 to 10 years [8]; this implies that the lifetime of the MIs needs to be extended to match that of the PV modules. Therefore, reliability evaluation and reliability-oriented design of PV MIs under a harsh environment is paramount [9]-[10].

Recently, increasing efforts have been made to the power electronics reliability, especially to discrete components or modules (e.g., IGBT, MOSFET, and capacitor) [10]-[20]. Only a few works [10], [13], [19] focus on the system-level reliability but not for PV module-level power electronics (MLPE). In addition, one significant drawback of previous general reliability assessments is that the local ambient temperature and the thermal cross-coupling effect between components are not considered; thus, the reliability performance might be overestimated. Based on a failure mode and effects analysis (FMEA) survey for MLPE products [21], the loose connection of dc input and ac output connectors, wear-out of dc-link electrolytic capacitors, varistor failure-short from the surge, and degradation of MOSFETs and diodes are identified as the top four failure modes; meanwhile, temperature cycling is reported as the most important stressor that affects the reliability of MLPE products. Only a few studies focused on the MI reliability can be found in literature, and most of them use the MIL-HDBK-217 handbook [22] to determine the failure rates of MIs [20]. Unfortunately, the constant failure rates only describe the large-population statistics of random failures, and the wear-out failure is not considered. Meanwhile, the MLPE

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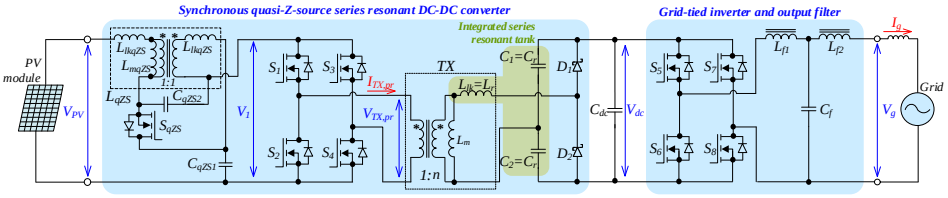

Fig. 1. Schematic of the impedance-source PV microinverter.

Fig. 2. Photo of the built PV microinverter prototype.

market is relatively nascent and there is not enough long-term usage data or independent reliability testing; therefore, accelerated testing of PV MI products is conducted in [6] for a long-term reliability prediction. It turns out that the time-to-failure of MIs from different manufacturers deviates significantly due to the design.

The PV MI system demands a wide input voltage and load regulation range at high DC voltage gains [23]. The impedance-source converters featuring the immunity to shoot-through and open states, continuous input current, low inrush current, buck-boost functionality as well as high control flexibility, and thus have recently gained much attention [24]-[25]. In [26], a quasi-Z-source series resonant dc-dc converter (qZSSRC) is proposed for MLPE applications; with a multimode control, the qZSSRC is capable of maintaining high efficiency within the six-fold variation of the input voltage (10~60 V). This feature enables the implementation of the shade-tolerant (global) MPPT, thus ensuring the maximum possible energy yield from the PV module even when two out of three substrings are shaded or in the conditions of opaque shading which could be caused by the fallen leaves or bird droppings [27]. Alternatively to the shoot-through pulse width modulation (PWM) and phase-shift modulation (PSM) in [26], the qZSSRC could also be controlled by the asymmetrical PWM [28], variable frequency [29] or the topology morphing [30], which significantly widens gain range and increases application flexibility.

Although the impedance-source converters properly match the demanding requirements of the PV MLPE application, their reliability performance is an open question. This paper aims to investigate the wear-out failure of an impedance-source PV MI. A mission profile based system-level wear-out assessment method is proposed and applied. A detailed electro-thermal model is built with the aid of system-level finite element method (FEM) simulations and experimental measurements on a 300-W MI prototype. Then, the mission profiles are translated into long-term junction/hotspot temperature profiles and annual damages for components. The Monte Carlo simulation and Weibull analysis are conducted to obtain the system wear-out failure over time. Finally, the variable dc-link voltage control is applied and the electrolytic capacitor is replaced with a more reliable one to improve system reliability. Compared with conventional reliability assessments, several improvements are made: 1) the dependence of component power loss on the junction/hotspot temperature is experimentally characterized and applied; 2) system-level FEM simulations are performed and the enclosure temperature is incorporated into the electro-thermal model; 3) the thermal cross-coupling effect between components is considered and modeled.

II. System Description and Reliability Evaluation

A. System Description

The schematic of the impedance-source PV MI is shown in Fig. 1. The two-stage MI consists of the quasi-Z-source series resonant dc-dc converter (qZSSRC) and the full-bridge inverter. The detailed operation principle and parameter design guidelines have been presented in [26]. There are three operation modes for the front-end qZSSRC:

1) Pass-Through Mode (PTM): The qZSSRC operates as the series-resonant converter (SRC) in the DC transformer mode. The normalized DC voltage gain is unity [26]:

$$G_{PTM} = \frac{V_{dc}}{2nV_{PV}} = 1 \tag{1}$$

2) Buck Mode: The operation of the qZSSRC is similar to that of the SRC with phase-shift modulation (PSM) control at the resonant frequency and discontinuous resonant current. The latter is due to small leakage inductance values of conventional transformers ($Q \ll 1$). The normalized DC voltage gain depends on the phase shift angle φ and the quality factor Q as in [26]:

$$G_{buck(DCM)} = \frac{V_{dc}}{2nV_{PV}} = 0.5\left(AB + \sqrt{A^2B^2 + A\frac{8}{\pi Q}}\right) \tag{2}$$

where $A = (1-\cos[\pi(1-\varphi/180)])/2$, $B = 2/(\pi Q) - 1$, and $Q = (8\pi f_{sw} L_{lk} P_{dc})/V_{dc}^2$.

3) Boost Mode: the voltage is controlled by shoot-through pulse width modulation (ST-PWM) implemented as a symmetrical overlap of active states. The normalized DC voltage gain in this mode depends on the shoot-through duty cycle D_{ST} [26]:

$$G_{boost} = \frac{V_{DC}}{2nV_{PV}} = \frac{1}{1-2D_{ST}}. \tag{3}$$

A 300-W PV MI prototype, consisting of the main circuit, auxiliary power supply circuit and microcontroller unit (MCU), has been built, as shown in Fig. 2. The detailed specifications and parameters are given in Table I. The measured full-load waveforms and efficiency curves at different input voltages and power levels are shown in Fig. 3.

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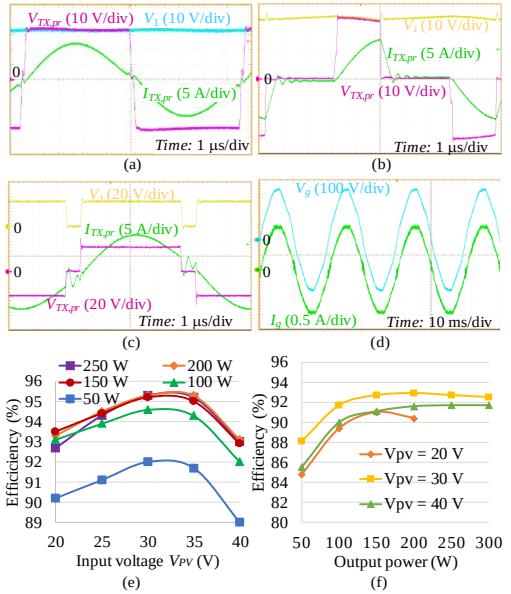

Fig. 3. Experimental waveforms in the (a) pass-through mode, (b) buck mode, and (c) boost mode. (d) Measured grid voltage and current waveforms. Measured efficiency curves of (e) the dc-dc stage and (f) the whole microconverter including the auxiliary power supply.

TABLE I
SPECIFICATIONS AND PARAMETERS OF THE MICROINVERTER PROTOTYPE

Descriptions	Parameters
Input voltage range	10–60 V
Nominal voltage	33 V
Most probable operating voltage range	20–40 V
Rated power	300 W
Switch. frequency of dc-dc stage	110 kHz
Switch. frequency of inverter stage	20 kHz
Switches S_{qZS}, $S_1 \ldots S_4$	BSC035N10NS5
Switches $S_5 \ldots S_8$	SCT2120AFC
Diodes $D_1 \ldots D_2$	C3D02060E
Capacitors C_{qZS1} and C_{qZS2}	2.2 μF × 12, C1210C225K1R
Coupled inductor L_{qZS}	L_{mqZS}=12 μH, L_{lkqZS}=0.6 μH, custom
Resonant capacitors C_1 and C_2	10 nF // 33 nF, MKP1840310104M and B32672Z6333K
DC-link capacitor C_{dc}	150 μF, 500-V electrolytic capacitor
Grid-side LCL filter: capacitor C_f	470 nF, B32653A6474K
Inductors L_{f1}	2.6 mH, custom
Inductors L_{f2}	1.8 mH, custom
Transformer *TX*	L_m=1 mH, L_{lk}=24 μH, n=6, custom

B. Reliability Evaluation Process

The failure modes of a power electronics system include the hardware failure, software failure and human error [10], as shown in Fig. 4. The hardware failure consists of the catastrophic, random, burn-in and wear-out failures. According to the FMEA survey for MLPE products in [21], connector contact failure, wear-out of electrolytic capacitor, short-circuit of varistor, and degradation of MOSFET/diode are reported as the top-four frequently happened failure modes, and the temperature cycling is identified as the most critical stressor affecting reliability. Therefore, this paper evaluates the wear-out failure of critical components, i.e., power semiconductors and capacitors, based on the flowchart illustrated in Fig. 4.

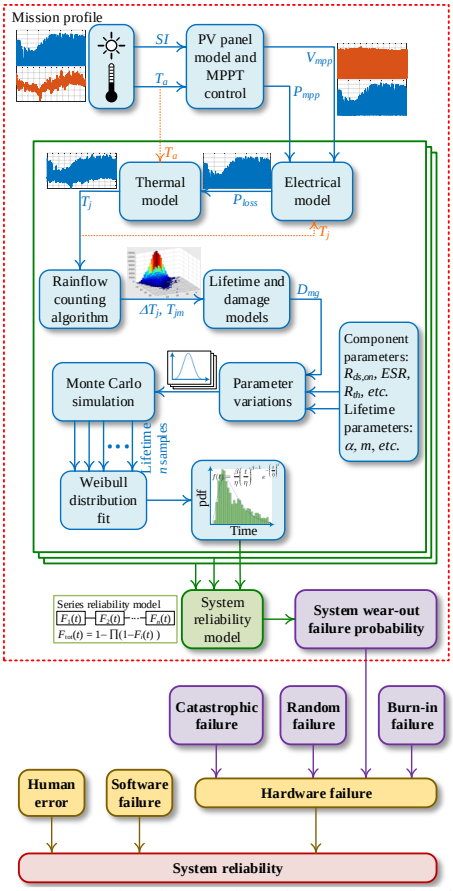

Fig. 4. Failure modes of power electronics systems and evaluation flowchart of the hardware wear-out failure probability.

The real-field mission profile, i.e., the solar irradiance (SI) and ambient temperature T_a for the PV MI system, directly determines the electrical and thermal loadings, and thus affects the degradation process of the components. With a PV panel model and an MPPT control, the long-term mission profile can be translated into the real-time voltage and power at the maximum power point, $V_{PV(mpp)}$ and $P_{PV(mpp)}$, which are the input of the MI. The power loss and junction/hotspot temperature of a component can be subsequently calculated based on the electrical and thermal models. The rainflow counting algorithm [31] is employed to extract the number of temperature cycles with different characteristics (e.g., the mean junction temperature T_{jm}, and the temperature swing ΔT_j). After that, the lifetime and damage accumulation models can be used to estimate the accumulated damage over a year. The junction/hotspot temperature T_j also affects the power loss, which is taken into account. When the damage is accumulated to 1, it is assumed that the component fails. Then the static wear-out lifetime of a component can be derived. In the real world, however, the parameters of the component and lifetime models have variations, which would affect the distribution of wear-out

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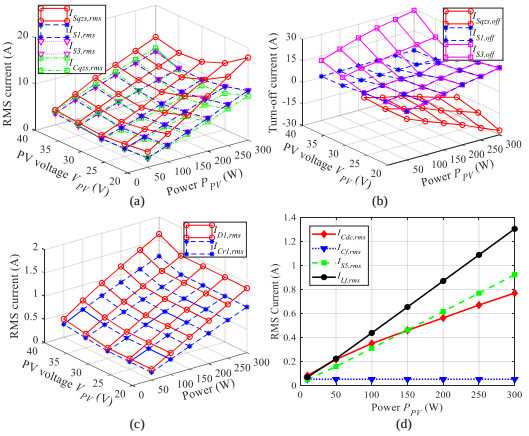

Fig. 5. Measured current characteristics of critical components. (a) RMS and (b) off-switching currents of primary-side components in the dc-dc stage; (c) RMS currents of secondary-side devices in the dc-dc stage; (d) RMS currents of inverter-stage devices.

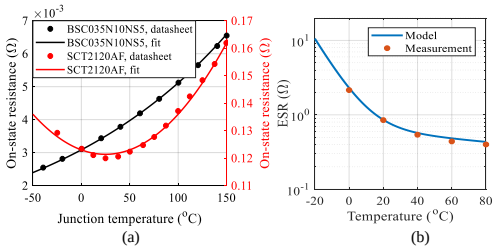

Fig. 6. Temperature characteristics of MOSFETs and an electrolytic capacitor. (a) Dependence of the on-state resistance $R_{ds,on}$ on the junction temperature for MOSFETs. (b) Dependence of ESR (at 100 Hz) on the hotspot temperature for the aluminum electrolytic capacitor used in the prototype.

failure probability. Therefore, a sensitivity analysis—Monte Carlo simulation is conducted based on a large population of samples. With the Weibull distribution fitting, the probability density function (pdf) for each component can be derived; and the system wear-out failure probability finally can be obtained with the reliability model for a series connected system.

III. Electro-Thermal and Lifetime Modeling of Critical Components

A. Power Loss Modeling

1) Power Semiconductor Devices

The current stress characteristics are measured for critical components, as shown in Fig. 5. The power loss of MOSFETs consists of the conduction loss $P_{T,con}$, turn-on loss $P_{T,on}$, and turn-off loss $P_{T,off}$. The conduction loss calculation is straight-forward, i.e., $P_{T,con} = I_{T,rms}^2 R_{ds,on}$, where $I_{T,rms}$ is the root-mean-square (RMS) current flowing through the MOSFET and $R_{ds,on}$ represents its on-state resistance which is a function of the junction temperature (cf. Fig. 6(a)). For the MOSFETs (S_{qZS}, S_1-S_4) in the dc-dc converter stage, their soft-switching conditions depend on the operation modes, as illustrated in [26]. For the inverter stage, the unipolar modulation is applied and the MOSFETs are hard-switched. The switching losses of MOSFETs are calculated with the model given in [32]. Two SiC Schottky diodes C3D02060E are employed for D_1-D_2, and the conduction loss is derived by $P_{D,con} = I_{D,avg} V_{D0} + I_{D,rms}^2 R_{D,on}$, where $V_{D0} = 0.98 - 0.0011 \times T_{jD}$, $R_{D,on} = 0.18 + 0.0018 \times T_{jD}$ [33], and T_{jD} is the junction temperature of the diode.

2) Capacitors

For the MI, the instantaneous power $p(t)$ contains a fluctuating power at twice the line frequency, which is decoupled by the dc-link capacitor C_{dc}. The electrical stresses over C_{dc} can be calculated by [34]

$$\Delta V_{dc} \approx P / (\omega_0 C_{dc} V_{dc}),\ I_{Cdc,rms} = P / (\sqrt{2} V_{dc}) \quad (4)$$

where P is the average power injected to the grid, ΔV_{dc} is the peak-to-peak ripple of the capacitor voltage V_{dc}, and $I_{Cdc,rms}$ is the RMS current flowing through C_{dc}. The aluminum electrolytic dc-link capacitor C_{dc} can be modeled as an ideal capacitor in series with an equivalent series resistor (ESR) [34]-[35]. There are two degradation mechanisms for the electrolytic capacitors [9]: chemical reactions due to electrolyte evaporation and contaminants, leading to deterioration of the dielectric material; localized heating, ion transport, and chemical processes caused by the leakage current [36]. The main stressor is the internal hotspot temperature T_h that is determined by the power loss $P_{Cdc,loss} = I_{Cdc,rms}^2 \cdot ESR(T_h)$. The ESR of an electrolytic capacitor is temperature dependent [37]-[38]; the temperature characteristic of the used electrolytic capacitor is measured and modeled as shown in Fig. 6(b).

For the ceramic and film capacitors (C_{qzs}, C_{r1}-C_{r2} and C_f), their power losses can be calculated in a similar way. However, their temperature characteristics are different from electrolytic capacitors. For the polypropylene film capacitors, the dependency of their capacitance on the temperature is very weak (0.023%/°C); in the meanwhile, the dissipation factor (DF) is largely unaffected by temperature [39]-[40]. Similarly, when the hotspot temperature is increased from 0 °C to 100 °C, the capacitance and DF of X7R ceramic capacitors decrease by only 5% and 1.5%, respectively [41]. Therefore, the impact of hotspot temperature on the power losses of polypropylene film and X7R ceramic capacitors are neglected in this paper.

3) Magnetic Components

The power losses of magnetic components consist of the core loss and the winding loss. The improved generalized Steinmetz equation (iGSE) [42] describes core loss, and the winding loss can be obtained with the Dowell model [43]-[44]. All the magnetic components were implemented with the Ferrite core 3C95 whose power loss density curve is flat with respect to temperature; this holds for various conditions of frequency and flux density [45]. Hence, the temperature dependence of the power losses in magnetic components is neglected.

B. Thermal Modeling

The PV MI is built with a four-layer PCB and is enclosed in an aluminum case (200 mm×150mm×45mm) by natural cooling. The case is filled up with elastic 2-component polyurethane casting compound [46] whose thermal conductivity (0.7 W/(K·m)) is almost 30 times higher than that of still air. Thus, the thermal cross-coupling effect between components (heat sources) cannot be neglected. However, most manufacturers provide the junction/core-ambient or case-ambient thermal resistance of a single component in a specific cooling condition.

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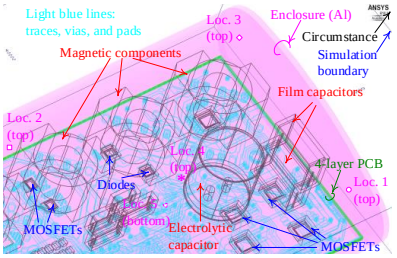

Fig. 7. Structure models of the main components, enclosure and PCB (including traces and vias) built in ANSYS/Icepak for FEM simulations. The PCB and the enclosure are placed horizontally. The enclosure is naturally cooled, i.e., all faces are exposed to the open air.

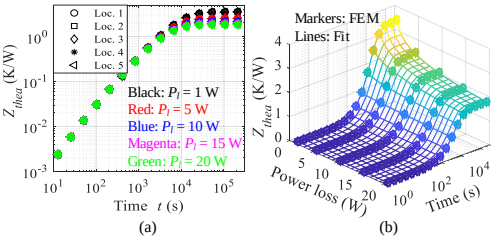

Fig. 8. (a) FEM simulated and (b) fitted enclosure-to-ambient thermal impedance at different power loss levels and enclosure locations.

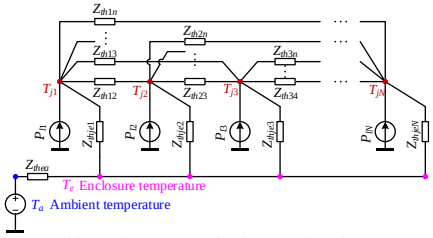

Fig. 9. Thermal impedance network of an enclosed converter system, including the self and mutual junction-enclosure thermal impedances.

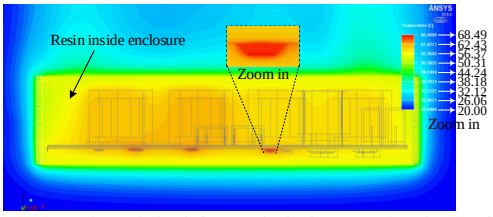

Fig. 10. FEM thermal simulation results in the case of total power loss $P_{l,tot}$ = 17.5 W. Temperature contour plane cut in the front view.

Apparently, these values cannot be used in the thermal analysis. Also, the mutual thermal resistance (thermal cross-coupling) depends on the heat transfer medium and the geometry/layout of components. Therefore, system-level FEM simulations are conducted to extract the self and mutual thermal resistances.

1) Enclosure-to-Ambient Thermal Impedance

The heat conduction, convection and radiation all exist in the thermal transfer from the enclosure to the circumstance. The heat transfer rate of convection is related to the temperature gap between the surface and the circumstance, whereas radiation intensity depends on the absolute temperature [47]-[48].

The enclosure of the studied MI is a custom hollow elliptical cylinder (cf. Fig. 7), which makes it difficult to analytically obtain the enclosure-to-ambient thermal impedance Z_{thea}. Therefore, multiple FEM simulations with ANSYS/Icepak are conducted at different power loss values and enclosure points, as shown in Fig. 8(a). It can be seen that the enclosure location has a negligible impact on Z_{thea}, i.e., it is almost isothermal, as the Aluminum and the filled compound have a high thermal conductivities. The enclosure-to-ambient thermal impedance Z_{thea} is a function of the total power loss of the MI, P_l, as well as time, and can be fitted as a first-order Foster model (cf. Fig.8(b))

$$Z_{thea} = R_{thea}(1 - \mathrm{e}^{-t/(R_{thea}C_{thea})}) \tag{5}$$

where C_{thea} is found to be constant as 2673 J/°C but R_{thea} is a function of the total power loss, $R_{thea} = 3.5P_l^{-0.216}$. It should be noted that the enclosure is placed horizontally in all the FEM simulations above. If the microinverter is installed vertically in practice, then the FEM-simulated thermal resistance is found as $R_{thea} = 3.45P_l^{-0.213}$ which is very close to that in the horizontal orientation. Hence, for this custom aluminum enclosure, it can be assumed that the enclosure-to-ambient thermal impedance Z_{thea} is independent of its orientation.

2) Junction-to-Enclosure Thermal Impedance Network

Thermal resistance network of a converter with N main components (heat sources) is shown in Fig. 9. The mutual thermal impedance is present between the components. It is difficult to perform the analytical calculation because of the irregular geometry of heat transfer medium. Conduction is the main heat transfer way inside the compound-filled converter, i.e., the components and compound inside the enclosure form a linear and time-invariant (LTI) system [49]. Therefore, the superposition principle can be applied [50]-[51] and the junction temperature for each component can be obtained by

$$\begin{bmatrix} T_{j1}(t) \\ T_{j2}(t) \\ \vdots \\ T_{jN}(t) \end{bmatrix} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} Z_{je11}(t) & Z_{je12}(t) & \cdots & Z_{je1N}(t) \\ Z_{je21}(t) & Z_{je22}(t) & \cdots & Z_{je2N}(t) \\ \vdots & \vdots & \ddots & \vdots \\ Z_{jeN1}(t) & Z_{jeN2}(t) & \cdots & Z_{jeNN}(t) \end{bmatrix} * \begin{bmatrix} P_{l1}(t) \\ P_{l2}(t) \\ \vdots \\ P_{lN}(t) \end{bmatrix} + T_e \tag{6}$$

where T_{ji} is the junction/hotspot temperature of component i, Z_{jenn} represents the self junction/hotspot-to-enclosure thermal impedance, Z_{jemn} denotes the mutual junction/hotspot-to-enclosure thermal impedance between components m and n, T_e is the enclosure temperature, P_{ln} is the power loss of the nth component, and "*" denotes convolution.

Detailed structure models for all main components, enclosure, and PCB (including traces and vias) are built in ANSYS/Icepak based on real dimensions and material properties, as shown in Fig.7. To extract the thermal impedances in (6), multiple system-level FEM simulations are conducted, as shown in Fig. 10. It can be seen that the local ambient temperature of each component has no significant difference due to the filled compound. The self thermal impedance of S_1 and mutual thermal impedances between S_1 and other components are depicted in Fig. 11(a). The

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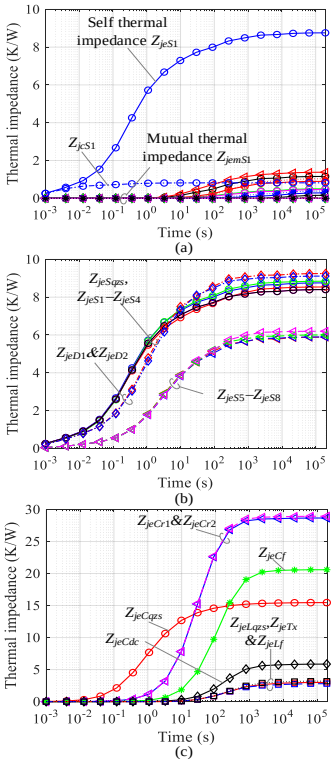

Fig. 11. FEM simulation results for thermal impedances. (a) Junction-case and junction-enclosure thermal impedances of $S1$; mutual junction-enclosure thermal impedances between $S1$ and other components. Self junction-enclosure thermal impedances of (b) semiconductor devices and (c) passive components.

self thermal impedance of semiconductor devices and passive components are shown in Fig. 11(b) and (c).

There are 19 main heat sources in the given MI. To speed up the subsequent calculation for the long-term junction temperature, the adjacent devices with the same part number and the same power loss are combined into one heat source. Thus, S_1-S_2, S_3-S_4, S_5-S_6, S_7-S_8, D_1-D_2 and C_{r1}-C_{r2} are simplified into S_{12}, S_{34}, S_{56}, S_{78}, D_{12} and C_{r12}, respectively. With the system-level FEM simulations, the junction-enclosure thermal resistance (i.e., steady-state thermal impedance) matrix also can be obtained:

$$\mathbf{R}_{je} = \begin{bmatrix}
8.5 & 0.95 & 0.3 & 0 & 0 & 0 & 0.73 & 0 & 0 & 0 & 1.1 & 0 & 0 \\
0.96 & 5 & 0.5 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0.35 & 0 \\
0.29 & 0.5 & 4.9 & 0 & 0 & 0 & 0.34 & 0.54 & 0 & 0 & 0.31 & 1 & 0 \\
0 & 0 & 0 & 3.4 & 1.1 & 0.25 & 0 & 0 & 0.8 & 0.85 & 0 & 0 & 0.36 \\
0 & 0 & 0 & 1.1 & 3.4 & 0.16 & 0 & 0 & 0.58 & 0.7 & 0 & 0 & 0.22 \\
0 & 0 & 0 & 0.23 & 0.16 & 5.2 & 0 & 0.34 & 0.33 & 0 & 0 & 0.2 & 0.3 \\
0.72 & 1 & 0.36 & 0 & 0 & 0 & 15.5 & 0 & 0 & 0 & 0.76 & 0.3 & 0 \\
0 & 0 & 0.51 & 0 & 0 & 0.32 & 0 & 20.4 & 0 & 0 & 0 & 0.7 & 0 \\
0 & 0 & 0 & 0.8 & 0.56 & 0.32 & 0 & 0 & 5.8 & 0.73 & 0 & 0 & 0.4 \\
0 & 0 & 0 & 0.84 & 0.7 & 0 & 0 & 0 & 0.74 & 20.6 & 0 & 0 & 0.42 \\
1.1 & 1 & 0.33 & 0 & 0 & 0 & 0.74 & 0 & 0 & 0 & 2 & 0.29 & 0 \\
0 & 0.3 & 1 & 0 & 0 & 0.16 & 0.23 & 0.7 & 0 & 0 & 0.27 & 1.95 & 0 \\
0 & 0 & 0 & 0.35 & 0.21 & 0.34 & 0 & 0 & 0.4 & 0.42 & 0 & 0 & 2
\end{bmatrix} \quad (7)$$

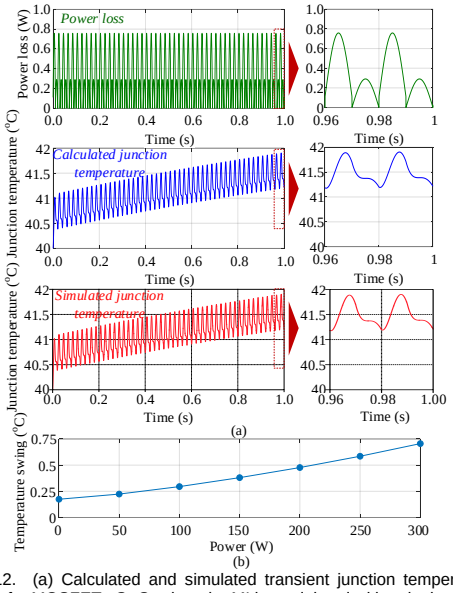

Fig. 12. (a) Calculated and simulated transient junction temperature profile for MOSFETs S_5-S_8 when the MI is modulated with unipolar PWM and injecting active power to the grid. (b) Junction temperature swing of S_5-S_8 with respect to the MI power level.

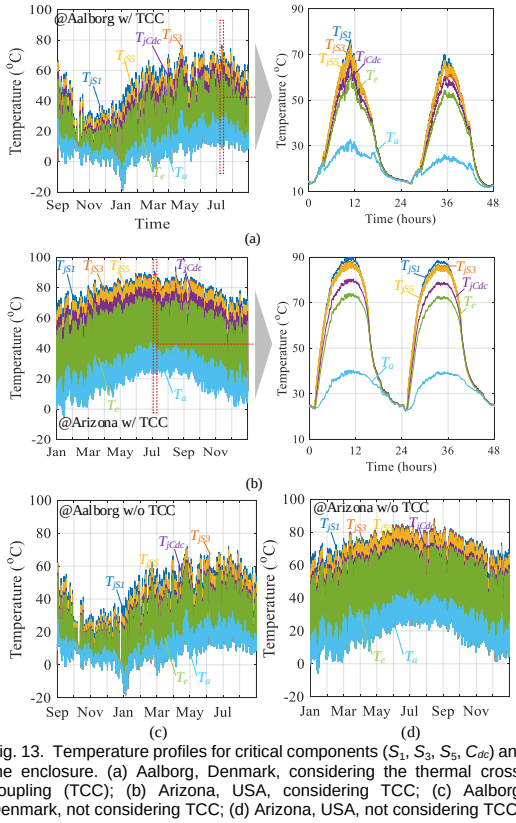

Fig. 13. Temperature profiles for critical components (S_1, S_3, S_5, C_{dc}) and the enclosure. (a) Aalborg, Denmark, considering the thermal cross-coupling (TCC); (b) Arizona, USA, considering TCC; (c) Aalborg, Denmark, not considering TCC; (d) Arizona, USA, not considering TCC.

where the diagonal elements are the self thermal resistances and the non-diagonal elements represent the mutual thermal resistances. Analyzing the degree of symmetry of (7) yields

$$S_m = \frac{|| (\mathbf{R_{je}} - \mathbf{R'_{je}}) / 2 ||}{|| (\mathbf{R_{je}} + \mathbf{R'_{je}}) / 2 ||} = 0.39\% . \quad (8)$$

This implies that the thermal resistance matrix has a fairly high degree of symmetry due to the reciprocity of heat conduction [50]-[51]. The thermal impedance Z_{jemn} can be fitted as a *Kth*-order Foster model:

$$Z_{jemn} = \sum_{k=1}^{K} R_{jemn,k}(1 - e^{-t/\tau_{jemn,k}}) \quad (9)$$

where R_{jemn} and τ_{jemn} are junction-enclosure thermal resistance and time constant between components *m* and *n*. The ambient-enclosure temperature difference and the junction temperature of component *m* can be calculated from the discrete equations:

$$\begin{cases} \Delta T_{jem}(x+1) = \sum_{n=1}^{N}\sum_{k=1}^{K}\left[\Delta T_{jemn,k}(x)e^{-t/\tau_{mn,k}} + P_{l,n}(x)R_{mn,k}(1 - e^{-t/\tau_{mn,k}})\right] \\ \Delta T_{ea}(x+1) = \Delta T_{ea}(x)e^{-t/\tau_{ea}} + P_{l,tot}(x)R_{ea}(1 - e^{-t/\tau_{ea}}) \\ T_{jm}(x+1) = \Delta T_{jem}(x+1) + \Delta T_{ea}(x+1) + T_a \end{cases} \quad (10)$$

The unipolar pulse width modulation (PWM) [52] is applied to the inverter stage, and it is assumed that only active power is injected to the grid. During the positive half cycle of the grid voltage, S_5 and the body diode of S_6 turn on alternately, and S_8 and the body diode of S_7 conduct alternately. During the negative half cycle, S_6 and the body diode of S_5 turn on alternately, and S_7 and the body diode of S_8 conduct alternately. The channel of each MOSFET conducts during a half cycle, whereas the body diode conducts during the other half cycle. The (conduction and switching) power losses of the MOSFET channel and its body diode are different, leading to an asymmetrical power loss profile for the MOSFETs in the inverter stages, as shown in Fig. 12(a). Fig. 12 also presents the calculated and simulated junction temperature profiles of S_5-S_8 for 300-W active power injected to the grid. Evidently, their junction temperature profile has 50-Hz fluctuations, which are caused by the periodical power losses at 50 Hz. The calculations agree well with simulations. The amplitude of the 50-Hz temperature swing rises with respect to the MI power increase, as indicated in Fig. 12(b).

C. Lifetime and Damage Accumulation Modeling

According to the FMEA results in [12] and [18], the progressive increase of the on-state resistance (wear-out) of MOSFETs is mainly caused by the growth of fatigue cracks and voids into the source metal layer. A 20% rise of the on-state resistance is chosen as the criteria of wear-out failure and a Coffin-Manson law based reliability model is built in [12]

$$N_f = \alpha \cdot (\Delta T_j)^{-m} \quad (11)$$

where N_f is the number of cycles to failure, ΔT_j is the junction temperature swing, and α and *m* are fitting parameters.

A widely-used capacitor lifetime model is employed for the lifespan projection of capacitors [15], [19]

$$L_{cn} = L_{c0} \cdot 2^{\frac{T_0 - T_h}{n_1}} (V / V_0)^{-n_2} \quad (12)$$

in which L_{cn} is the lifetime under the thermal and electrical stress T_h and V, L_{c0} is the lifetime under the reference temperature T_0 and the nominal voltage V_0. The coefficient n_1 is a temperature dependent constant, and n_2 is the voltage stress exponent.

For snap-in aluminum electrolytic capacitors, the temperature-dependent parameter n_1 is 10 and the voltage stress exponent n_2 is 5 when the applied voltage is 80 %-100 % of the rated voltage [53]-[54]. The temperature-dependent parameter n_1 = 10 also holds for film capacitors [15], [36], [57]. However, the voltage stress exponent n_2 for film capacitors is reported from around 7 to 9.4 in [9], [15], [36], from 5 to 10 in [55], from 7 to 12 in [56], and 7 in [57]. The discrepancy between the values may be attributed to the different technologies adopted by the different manufacturers [55]. To have an unbiased lifetime estimation of film capacitors, the median value 8.2 is adopted. For the ceramic capacitor used, the manufacturer provides the coefficients n_1 = 8, and n_2 = 3 [58].

According to the commonly used Miner's rule [59]-[60], the damage accumulates linearly:

$$D_{mg} = \sum_k (n_k / N_{fk}) \quad (13)$$

where n_k is the number of cycles with a specific thermal loading stress, and N_{fk} is the number of cycles till failure for the same stress. The device fails when the accumulated D_{mg} reaches 1.

IV. Wear-Out Failure Analysis of the Microinverter

A. Static Annual Damage of Components

The mission profiles from Aalborg, Denmark, and Arizona, USA, are applied to the electro-thermal model. Then, the junction/hotspot temperature profiles for each component and the enclosure temperature can be derived (cf. Fig. 13). The resolution is 100 points/s to accommodate 50-Hz junction temperature fluctuations of the inverter MOSFETs. If the thermal cross-coupling (TCC) effect is not considered, the junction/hotspot temperatures of components will be underestimated, as shown in Fig. 13(c) and (d). It should be noted that a MI is typically installed on the mounting rack of PV panels, and thus the real ambient temperature of the MI may be higher than the applied one which represents the open-field temperature. The PV module degradation is ignored to offset this methodology flaw.

With and without considering the TCC effect, the annual damage of each critical component at the two locations is shown in Fig. 14(a). It can be observed that the dc-link capacitor C_{dc} has the highest annual damage at both locations, i.e., 0.01 and 0.057 for Aalborg and Arizona, respectively. Assuming there are no other kinds of failures, the corresponding wear-out lifetimes of the dc-link capacitor are 100 yrs and 17.54 yrs for the two operating locations. However, if the thermal cross-coupling effect is not considered, then the annual damages of C_{dc} at the two locations are 0.007 and 0.031, which results in an underestimation rate of about 30 %. The mean ambient temperature of Arizona over a year, T_{am}, is 22.34 °C. If the solar irradiance of Arizona remains the same, but the mean ambient temperature T_a varies, then the annual damage of each component will change as well, as shown in Fig. 14(b). It can be seen that the annual damages of capacitors rise significantly with respect to the increase of T_{am}, while the damages of semiconductors increase slightly. This results from (11) where the number of cycles to failure is mainly dependent on the junction temperature swing instead of its mean value.

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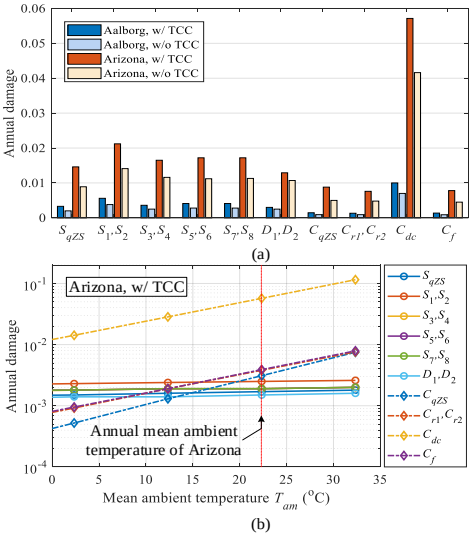

Fig. 14. Annual damage to each critical component. (a) Annual damage when the MI operates at different locations with and without considering the thermal cross-coupling (TCC). (b) Annual damage of each component versus the mean ambient temperature in Arizona.

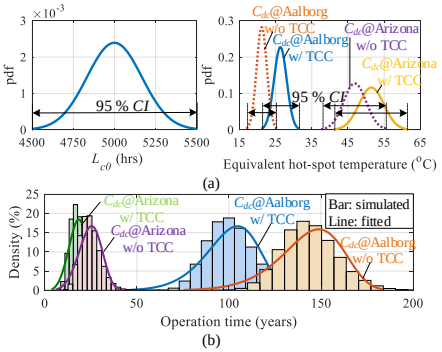

Fig. 15. (a) Probability density functions of the parameters for the dc-link capacitor C_{dc}; (b) Histograms of years to wear-out failure for a population of 1×10^5 capacitor samples operating at two locations, with and without considering the TCC effect.

B. Monte Carlo Simulation and System Failure Probability Due to Wear-out

There are some uncertainties which may affect the MI lifetime in the real-world operation. First, the parameters in the lifetime model could vary. For instance, the applied lifetime model for MOSFETs is derived from the testing data in [12], and the parameters α and m have boundaries. Second, the parameters of the employed devices vary, which is caused by the manufacturing process variations among the devices with the same part number. According the datasheet, the on-state resistances of the MOSFETs employed in the two stages vary within ±20% and ±10%, respectively. Third, the mission profile could also vary due to the climate change.

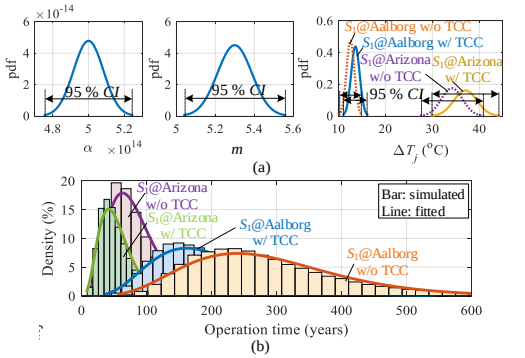

Fig. 16. (a) Probability density functions of the parameters for S_1; (b) Histograms of years to wear-out failure for a population of 1×10^5 samples operating at two locations, with and without considering the TCC effect.

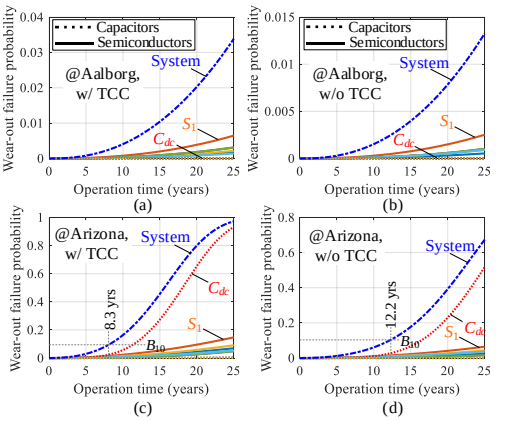

Fig. 17. Probability curves of wear-out failure for each component and the system when operating at (a) Aalborg, Denmark, with considering the thermal cross-coupling (TCC) effect; (b) Aalborg, Denmark, without considering the TCC effect o; (c) Arizona, US, with considering the TCC effect; (d) Arizona, US, without considering the TCC effect.

It is assumed that all the variations mentioned above obey the normal distribution. The second and third types of uncertainties (e.g., $R_{ds,on}$ of MOSFET, ESR of capacitor, ambient temperature, and solar irradiance) directly affect the junction/hotspot temperature. Hence, the junction/hotspot temperature swing will vary within a certain range. The probability density functions (pdfs) of the parameters of C_{dc} and S_1 are shown in Figs. 15(a) and 16(a), considering a 95% confidence interval (CI). For other devices, their parameters variations are also considered.

To analyze the impact of all the uncertainties on the system wear-out failure, the continuous mission profile should be converted into an equivalent static one, which produces the same degradation [61]. Then a sensitivity analysis—Monte Carlo simulation can be carried out by simultaneously taking into account all parameter variations. The population number for each sample is 1×10^5 in the Monte Carlo simulation. The histograms of years to wear-out failure for the selected

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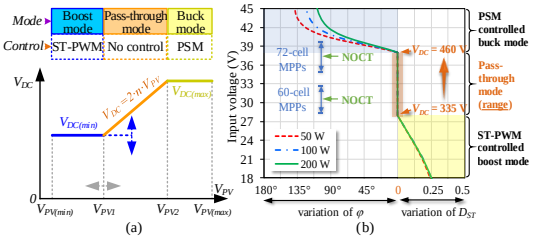

Fig. 18. Advanced multi-mode control of the qZSSRC with a variable dc-link voltage: (a) sketch of dc-link voltage variations; (b) regulation characteristics.

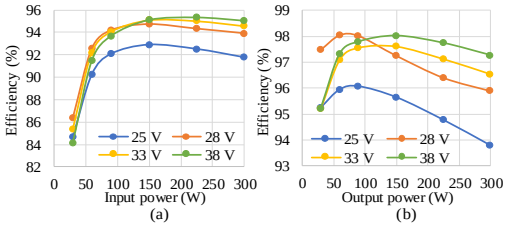

Fig. 19. Measured efficiency with the new control strategy: (a) the whole PV MI incl. the auxiliary power, (b) the dc-dc power stage.

components, C_{dc} and S_5, are shown in Figs. 15(b) and 16(b), respectively, which are fitted with the Weibull distribution [61]:

$$f(t)=\frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1}e^{-\left(\frac{t}{\eta}\right)^{\beta}},\ F(t)=1-e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{14}$$

where β is the shape parameters and η is the scale parameter.

Assume all the considered devices are connected in series in the reliability model, i.e., any component failure will lead to system failure. Then the system wear-out failure $F_{sys}(t)$ equals:

$$F_{sys}(t)=1-\prod(1-F_i(t)) \tag{15}$$

where $F_i(t)$ represents the cumulative distribution function (cdf) of the component wear-out failure.

Fig. 17 shows the probability curves of wear-out failures for components and the system when operating at Aalborg, Denmark, and Arizona, US, with and without considering the thermal cross-coupling effect. First, it can be seen that the mission profile has a strong impact on the wear-out failure: when operating in a harsher environment, i.e., Arizona, the wear-out failure probabilities before 25-year operation are significantly higher. Second, neglecting the thermal cross-coupling effect will lead to an obvious underestimation of the wear-out failure probability; when operating at Aalborg, the predicted system wear-out failure probability before 25 years is 3.34 % (cf. Fig. 17(a)), whereas the corresponding value is only 1.3 % (cf. Fig. 17(b)) if neglecting the thermal cross-coupling effect. When operating at Arizona, the B_{10} lifetimes with and without considering the thermal cross-coupling effect are 8.3 yrs and 12.2 yrs (cf. Fig. 17(c) and (d)), respectively, which implies that about 45 % lifetime overestimation can be made if neglecting the thermal cross-coupling effect. In addition, it can be seen that the dc-link electrolytic capacitor C_{dc} has the highest wear-out failure probability when the operating environment is harsh, and thus dominates the system wear-out failure. Hence, it can be concluded that the dc-link electrolytic capacitor C_{dc} is the bottleneck of 25-year reliable operation for the studied PV MI.

V. Reliability Improvement of the Microinverter

It can be concluded from the reliability evaluation results (cf. Fig. 17) that the 25-year wear-out failure probability of the studied PV microinverter is high when operating in a harsh environment—Arizona, US. Therefore, measures will be taken to improve its reliability.

A. Advanced Multi-Mode Control of the qZSSRC

The multi-mode control of the qZSSRC [26] results in the operation in the pass through mode (PTM) only at the particular voltage where (1) holds true for the fixed dc-link voltage. The PTM corresponds to the peak efficiency. However, it is not necessary for the grid-tied microinverter to have a stable dc-link voltage. Hence, an advanced multi-mode control with a variable dc-link voltage (cf. Fig. 18(a)) could be implemented on the qZSSRC to cover the voltage ranges of the most probable maximum power points (MPPs) of the 60- and 72-cell Silicone (Si) PV modules in PTM, as shown in Fig. 18(b). The lower bound of the PTM range is defined by the peak grid voltage $V_{g(pk)}$ with an assumption that the dc-link voltage is 10 V above that:

$$V_{PV1}=\frac{V_{g(pk)}+10}{2n} \tag{16}$$

The grid RMS voltage is usually within the range of 207 V to 253 V, which results in possible variations of the minimum dc-link voltage $V_{DC(min)}$ from 305 V to 370 V. For the rated grid voltage of 230 V, this voltage equals $V_{DC(min)}$ = 335 V. The upper bound of the PTM is limited by the voltage rating of the dc-link capacitor. Considering the existing technology, the electrolytic capacitor rated voltage of 500 V could be recommended. Assuming $V_{DC(max)}$ = 460 V, then a safety margin of 40 V is achieved:

$$V_{PV2}=\frac{V_{DC(\max)}}{2n} \tag{17}$$

The PTM is active between V_{PV1} = 28 V and V_{PV2} = 38 V for the nominal grid RMS voltage of 230 V. The control characteristic of the qZSSRC shown in Fig. 18(b) at the nominal grid voltage features a considerable PTM range owing to the proposed advanced multi-mode control. Remarkably, the PTM overlaps with the ranges of the most probable MPPs of the 60- and 72-cell Si PV modules over the temperature variations between 30 °C and 60 °C. This also includes the standard nominal operating cell temperature (NOCT) of 45 °C. The MPPs outside the PTM correspond to the temperatures that are rarely observed in practice.

The advanced multi-mode control with a variable DC-link voltage results in an efficiency improvement by over 2% for the PV microinverter, as shown in Fig. 3 and Fig. 19. This means that the power losses and the junction/hotspot temperatures of components will be reduced, which is beneficial for reliability improvement.

B. Long-Lifetime DC-Link Electrolytic Capacitor

From Fig. 17(c), it is seen that the long-term (e.g., 25 years) reliability bottleneck of the PV microinverter operating in a harsh environment is the dc-link electrolytic capacitor C_{dc}. Therefore, C_{dc} should be selected carefully. In the baseline

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design, the dc-link employs a cost-optimized 150-μF electrolytic capacitor, whose nominal lifetime is 5000 hours at 85 ºC. To decrease the wear-out failure probability, an emerging high-reliability electrolytic capacitor (ESR at 100 Hz at 25°C: 0.54 Ω, nominal lifetime: 5000 hours @105°C), will be used in the new design along with the variable DC-link voltage control.

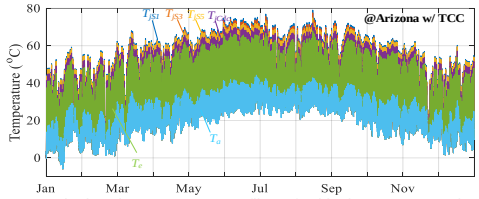

Fig. 20. Calculated temperature profiles of critical components (S_1, S_3, S_5, C_{dc}) and the enclosure of the PV microinverter with the variable dc-link voltage control when operating in Arizona, US.

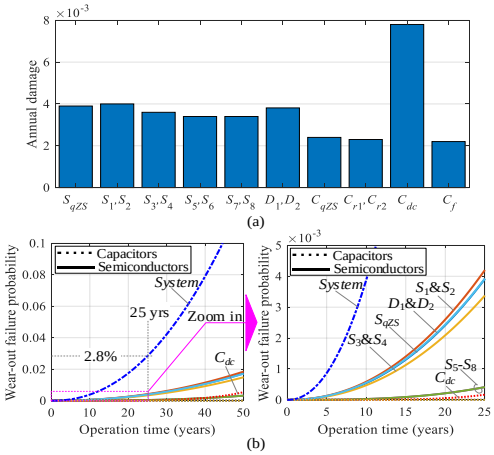

Fig. 21. Reliability evaluation results of the PV microinverter with the variable dc-link voltage control and the new electrolytic capacitor; the mission profile of Arizona is applied: (a) annual damage and (b) wear-out failure probabilities of each component and the system.

C. Wear-Out Failure Probability Estimation

With the advanced multi-mode control and the new DC-link capacitor, the temperatures of the selected critical components (S_1, S_3, S_5, C_{dc}) and the enclosure can be obtained, as shown in Fig. 20. Compared with the baseline solution, the new design enables the microinverter to operate at lower temperatures (cf. Fig. 13 and Fig. 20); the maximum temperature reduction is about 14 ºC. The reliability evaluation procedure is repeated for the new design, and the results are shown in Fig. 21. It is seen from Figs. 14(a) and 21(a) that the annual damage to each component is decreased due to the lower junction/hotspot temperature. Particularly, the annual damage to the dc-link capacitor C_{dc} is significantly reduced from 0.057 to 0.0078 because of the lower hotspot temperature and longer nominal capacitor lifetime. Fig. 21(b) shows the probability curves of wear-out failure for the components and the system. As can be observed, the 25-year wear-out failure probability of each component is kept at a low level. The wear-out failure probabilities over time obey the Weibull distribution, but the shape parameters of the capacitors are larger than those of the semiconductors, as illustrated in Fig. 21(b). Therefore, at the early stage of life cycle, the system wear-out failure is dominated by semiconductors. Nevertheless, the system wear-out failure probability over 25-year operation is about 2.8 %, which is a dramatic improvement compared to the baseline solution (cf. Fig. 17(c)).

VI. Conclusions

The wear-out performance of a 300-W PV microinverter is evaluated by applying different mission profiles, experimental measurements, system-level FEM simulations, Monte Carlo simulation, and Weibull analysis. Harsh operating conditions of microinverters compel the enclosure to be filled up with thermally conducting casting compound, causing a strong thermal cross-coupling effect between components. The performed analysis reveals that: 1) the mission profile has a significant impact on the system wear-out failure; 2) neglecting the thermal cross-coupling effect will lead to a remarkable underestimation of the system wear-out failure probability; 3) the DC-link electrolytic capacitor is the bottleneck for the long-term (e.g., 25-year) reliable operation of the studied PV microinverter. In order to reduce the system wear-out failure probability, the variable DC-link voltage control is applied and the original cost-optimized DC-link capacitor is replaced with a more reliable aluminum electrolytic capacitor. It is shown that the probability of system failure due to wear-out over 25 years can be significantly reduced with the new design.

Nevertheless, the reliability evaluation results need to be treated cautiously. The aim of the wear-out failure probability prediction is to identify the weakest link in the PV micro-inverter, and to benchmark different modulation/control/design techniques for reliability improvement. The wear-out failure probability in real operation may differ from the estimation in this paper due to several limitations: 1) the applied empirical device lifetime models are derived by accelerated testing at a specific condition and may lead to errors due to different operating conditions; 2) depending on the installation position of the microinverter, its real ambient temperature may be much higher than the open-field ambient temperature; 3) the degradation of PV modules will slow down the wear-out of microinverters; 4) in addition to wear-out, there are also other failure modes (cf. Fig. 4) which may affect the hardware failure, but are not taken into account in this paper.

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