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DOI (link to publication from Publisher):
10.5278/vbn.phd.engsci.00078

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

INTERHARMONICS ANALYSIS AND MITIGATION IN ADJUSTABLE SPEED DRIVES

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DISSERTATION SUBMITTED 2016

AALBORG UNIVERSITY
DENMARK

Interharmonics Analysis and Mitigation in Adjustable Speed Drives

by

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A Dissertation Submitted to
the Faculty of Engineering and Science at Aalborg University
in Partial Fulfillment for the Degree of
Doctor of Philosophy in Electrical Engineering

April 2016
Aalborg, Denmark

Dissertation submitted: February 28, 2016

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PhD Series: Faculty of Engineering and Science, Aalborg University

ISSN (online): 2246-1248
ISBN (online): 978-87-7112-521-4

Published by:
Aalborg University Press
Skjernvej 4A, 2nd floor
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Rosendahls, 2016

Public Defence of PhD Dissertation

Thesis Title:

Interharmonics Analysis and Mitigation in Adjustable Speed Drives

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Thursday, April 28, 2016
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Dedicated to my parents for their encouragement and exceptional love.

Preface

This thesis is written according to the project entitled "*Interharmonics Analysis and Mitigation in Adjustable Speed Drives*". The Ph.D. project is supported mainly by Iran Ministry of Science, Research and Technology (MSRT) and partially by the Department of Energy Technology, Aalborg University, Denmark.

This research project was done under the supervision of Prof. Frede Blaabjerg and Prof. Poh Chiang Loh from the Department of Energy Technology, Aalborg University, and Dr. Firuz Zare from the Global Research and Development Centre, Danfoss Drives A/S, Denmark. First and foremost, I would like to express my deepest gratefulness to my supervisor, Prof. Frede Blaabjerg, for his constructive discussions, patient guidance and continuous supports in the Ph.D. project period. His extreme inspiration and professional behaviors learned me how I should get through the difficulties during the Ph.D. project. I do believe that the precious lessons I earned under his supervision will deeply influence both my career and personal life. I would also like to give my sincere thanks to my co-supervisor Prof. Poh Chiang Loh for the time he spent to discuss the detail issues with me, and for his valuable guidance at the Ph.D project. Besides, I would like to express my deepest respect to my lovely co-supervisor Dr. Firuz Zare for his inspirational proposals, technical discussions and tremendous encouragements. He was my supervisor at the B.Sc. and M.Sc period, and also my co-supervisor at the Ph.D period. I should say I owe all my knowledge to his brightness and kindness. It was my pleasure to work with him such long time.

My gratitude also goes to Dr. Pooya Davari from the Department of Energy Technology for his useful discussions and great encouragement in the last year of my Ph.D. It was a short period but very constructive.

I would also like to take this opportunity to thank all my colleagues from the Department of Energy Technology for providing a warm environment and full of enthusiasm. My best wishes to my lovely friends - Dr. Qobad Shafiee, Dr. Reza Ahmadi, Dr. Amir Sajjad Bahman, Dr. Alireza Rezaniakolaei, Dr. Bakhtyar Hoseinzadeh, Dr. Seyed-Mostafa Farashbashi-Astaneh, Mohammadkazem Bakhshizadeh and Esmaeil Ebrahimzadeh. Moreover, my special appreciations are extended to John K. Pedersen, Tina Larsen, Corina Busk Gregersen, Mette Skov Jensen, Eva Janik and Casper Jørgensen for their valuable assistance in different ways.

Hamid Soltani

February, 2016
Aalborg Øst, Denmark

Abstract

With the growing use of power electronics technology in different applications, many efforts have simultaneously been devoted to improve the grid quality issues. In this respect, harmonic and interharmonic distortions are among the most important criteria, which are needed to meet the required standards. Meanwhile, issues related to interharmonics have recently gained more attention besides classical harmonics, due to their specific negative effects as well as those common with harmonics. Interharmonic distortions can seriously hamper the normal operation of the power system by means of side effects such as excitation of undesirable electrical and/or mechanical resonances, misoperation of control devices, and so forth. Adjustable Speed Drive (ASD) based on double-stage AC-DC-AC converter is considered as one of the main sources of interharmonics in the grid. Literature survey shows that most of the works focus on analyzing and reducing the harmonics in power system and motor drives, while less attempts are devoted to interharmonic-related issues. In this respect, this Ph.D. project has investigated and evaluated the adjustable speed drive input current interharmonics caused by different sources, and proposed some appropriate solutions to enhance the grid quality. The main scopes of this research work can be introduced as: *1) General study of interharmonic sources and identification in Voltage-Source Inverter (VSI-) fed ASD*, *2) Input current interharmonic characterization in a double-stage VSI-fed ASD*, and *3) Mitigation of ASD's input current interharmonics due to motor current imbalance.*

Chapters 2 and 3 present a general study on the harmonic and interharmonic sources and detections in the ASD. The study is particularly performed with respect to a VSI-fed ASD with very low switching frequency and a naturally sampled Sinusoidal Pulse Width Modulation (SPWM) strategy in Chapter 2. Then, some practical challenges associated with interharmonics detection are followed in Chapter 3. A thorough discussion introduces the existing desynchronized interharmonics detection method, which in this thesis is applied as highly accurate measurement strategy.

Thereafter, the ASD input current interharmonics are evaluated in Chapters 4 and 5 with respect to the inverter's modulation strategy, and to the ASD's passive filter effects. In Chapter 4, the symmetrical regularly sampled SPWM, Space Vector Modulation (SVM), and Discontinuous Pulse Width Modula-

tion (DPWM2), and also the asymmetrical regularly sampled SVM modulation techniques are chosen as the most popular modulation strategies applied in the motor drive applications. A frequency mapping characterizes the ASD's input current interharmonic locations. Then, it recommends the suitable strategy associated with the fixed-frequency switching methods (e.g., SPWM, SVM, and DPWM2) in order to reduce the drive input current interharmonic components. Chapter 5 investigates the effects of the ASD's passive filters (AC choke, DC choke, and DC-link capacitor) on the input current interharmonics caused by motor current imbalance. This investigation has been carried out in both cases of the balanced and the unbalanced load conditions.

In Chapter 6, some active compensation methods are proposed in order to mitigate the ASD's input current interharmonics generated by the motor current imbalance. In the case of partially-controlled ASD, where an inverter is connected to the front-end diode rectifier back-to-back sharing a common DC link, the AC- and/or DC- side active compensators are proposed for input current interharmonics reduction. Moreover, in the case of a fully-controlled ASD (a back-to-back converter), the drive input current interharmonics are mitigated by proposing an appropriate control strategy.

The contribution of this research work is a better understanding of the drive input current interharmonics with respect to different modulation techniques. It investigates the interharmonics issue both in cases of balanced and unbalanced load conditions. Appropriate solutions are proposed in order to reduce the drive input current interharmonics. It is expected that the outcome of this work would be helpful for people investigating the origin of interharmonics, and looking for new potential strategies for their reduction.

Dansk Abstrakt

Med den stigende brug af effektelektronik i forskellige applikationer har der været gjort bestræbelser på at forbedre spændings-kvaliteten af elnettet, eksempelvis styret i form af nye standarder. I denne forbindelse er harmoniske og interharmoniske forvrængninger blandt de mest vigtige kriterier, som er nødvendige for at opfylde standarder, der er gældende for effektelektronisk apparater. I den sidste tid har spørgsmål vedrørende interharmoniske fået en større opmærksomhed ud over de klassiske harmoniske forstyrrelser på grund af deres specifikke negative påvirkninger, såvel som dem der er fælles med de harmoniske problemer. Interharmoniske kan forstyrre den normale drift via bivirkninger som excitation af uønskede elektrisk og/eller mekaniske resonanser, eller forstyrrelser i selve reguleringen og kommunikationen. Motorstyringer baseret på et to-trins AC-DC-AC konverter betragtes som en af de vigtigste kilder til interharmoniske i el-nettet. Undersøgelser viser, at den primære litteratur fokuserer på at analysere og reducere harmoniske i el-systemet og motor drev, mens langt færre forsøger at afdække de interharmoniske problemer. Derfor har dette Ph.D. projekt undersøgt og evalueret motorstyringers nuværende interharmoniske på el-nettet forårsaget af forskellige kilder, og har foreslået nogle passende løsninger til at forbedre el-nettets kvalitet. De vigtigste anvendelsesområder for dette forskningsarbejde kan introduceres som: 1) Generel undersøgelse af interharmoniske kilder og deres identifikation i frekvensomformer-styret motorer, 2) Interharmonisk karakterisering i en motorstyring, og 3) Reduktion af motorstyringens interharmoniske på grund af ubalance i motorstrømmen.

Kapitel 2 og 3 foretager en generel undersøgelse af de harmoniske og interharmoniske kilder i motorstyringer. Studierne er især udført i forhold til at en Voltage Source Inverter fødet motor med en relativ lav skifte frekvens er anvendt og som samtidig anvender en naturligt samplet Sinus-formet Pulse Width Modulations (SPWM) strategi. Derefter er der nogle praktiske udfordringer forbundet med interharmonisk detektion, som er beskrevet i detaljer i kapitel 3. Efter diskussionen introduceres eksisterende asynkrone interharmonisk detektions metoder, som i denne afhandling er anvendt som en meget nøjagtig måle-strategi.

Derefter bliver de interharmoniske strømme på net-siden evalueret i kapitel 4 og 5 i forhold til motorstyringens modulations strategi, og i forhold til de

passive filter-effekter i mellemkredsen. I kapitel 4 undersøges den symmetrisk naturligt samplet SPWM, Space Vector Modulation (SVM), og Diskontinuerlig Pulse Width Modulation (DPWM2), og også den asymmetriske naturlig samplet SVM modulation teknikker som er valgt da de er de mest populære modulations strategier i motordrev applikationer. En detaljeret kortlægning af de nuværende interharmoniske strømme på net-siden er foretaget. Dernæst anbefales en passende kompenseringsstrategi med fast skifte frekvens (fx SPWM, SVM, og DPWM2) for at reducere motorstyringens net-side interharmoniske komponenter. I kapitel 5 undersøges virkningerne af motorstyringens passive filtre (AC spole, DC spole, og DC-link kondensator) på net-siden, når de interharmoniske er forårsaget af motorstrøms ubalance.

I kapitel 6 er der foreslået nogle aktive kompensations-metoder til at kunne afbøde net-sidens interharmoniske, som igen er skabt af motorens ubalance. I tilfælde af at en delvis kontrolleret motorstyring anvendes, hvor en inverter er forbundet med en diode ensretter tilsluttet el-nettet, er en aktiv AC- og DC- side kompensationsmetode foreslået for at kunne reducere net-sidens interharmoniske. Endvidere i tilfælde af en fuldt kontrolleret motorstyring (en back-to-back konverter) er anvendt, vil de skabte interharmoniske kunne afbødes ved en ny foreslået kontrolstrategi.

Bidragene i denne PhD afhandling er en bedre forståelse af de interharmoniske på net-siden som stammer fra motor-styringen via forskellige modulations metoder. Afhandlingen undersøger også de interharmoniske både i tilfælde af balanceret og ubalanceret belastningsforhold på motor-siden. Passende løsninger foreslås til at kunne reducere de interharmoniske fra motorstyringen. Det forventes, at resultatet af dette arbejde ville være nyttigt for folk, der undersøger oprindelsen af interharmoniske, og undersøger nye potentielle strategier til at kunne reducere dem.

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Part I Report

Chapter 1

Introduction

This chapter firstly presents the background and motivation of this research project. It includes a short description about harmonic and interharmonic distortions and their impact on the grid, followed by the objectives and limitations of the project. Then, the thesis structure is presented to give a better understanding about the flow of the research work.

1.1 Background and motivation

In modern electrical energy systems, voltages and especially currents may become very irregular due to large numbers of non-linear loads and generators in the grid. In this regard, power electronic based systems such as adjustable speed drives, power supplies for IT-equipment and high efficiency lighting and inverters in systems generating electricity from distributed renewable energy sources are important sources to create disturbances [1–5]. Distortions encountered are, for example, harmonics, interharmonics, rapid amplitude variations (flicker) and transients, which are all elements of 'power quality' problems.

A voltage waveform in a conventional power system is expected to be pure sinusoidal with a fundamental frequency and a rated amplitude. When non-linear loads are connected to an electric power system they tend to draw non-linear currents, and consequently, to distort the grid voltage due to the impedance on the network [6]. Mathematically, the distorted voltage and/or current signal can be represented as a combination of the grid fundamental frequency components and its multiples named as harmonic frequency components. In the case that systems operating at different frequencies are tied to each other via non-linear devices, the frequency interaction may result in interharmonic distortions.

1.1.1 Harmonic distortions

Harmonics are defined as sinusoidal voltages or currents whose frequencies are multiple integers of the fundamental frequency [6]. Proliferation of non-linear

loads in power systems has increased harmonic pollution and has deteriorated the power quality. It is worth to mention that the rapid variations in distortion levels are basically considered in the category of transients rather than harmonics [7]. In this respect, as the speed of the variations decreases, at some point the distortion is more clearly described as being a set of harmonics of varying magnitude rather than a transient phenomena.

IEC 61000-4-3 [8] has set a window of 3 seconds as the shortest window over which harmonics should be measured, and IEC 61000-3-2 [9] allows a 50 % increase in distortion level for this period, for certain types of equipment. The fundamental principles which led to the harmonic standards can be noted as:

a) Avoid system and load damage and disruption due to high harmonic levels.

b) Limit harmonic losses to an acceptable level.

c) When mitigation is necessary, find an economical and equitable solution.

Regarding the harmonic identity, it should be noted that harmonics are typically assumed to be periodical and time-invariant. This is while harmonic components are steadily changing with time [10]. It is then always appreciated to look at the harmonics based on time-variant identities and evaluate the harmonic distortions in this perspective.

Harmonic distortions, which are tied to either voltage magnitudes and current flow amplitudes may result in severe effects on the connected power system. It may cause erratic behavior in microcontrollers, breakers, and relays. In addition, these distortions may lead to increased temperature and consequently to increased losses, transformer derating, possible equipment failure over time, and interaction between the controllers.

1.1.2 Interharmonic distortions

According to IEC 61000-4-7 [11], interharmonic frequencies are defined as any frequencies, which are not integer multiples of the fundamental frequency. Generally, two basic mechanisms lead to the interharmonics generation. The non-linear interaction between two systems operating at different frequencies can give rise to interharmonics. These interactions are usually a consequence of the switching characteristics of power electronic devices [12] or rapid changes of current in the equipment and installation. Due to the non-linear interaction, the fundamental frequency component and its harmonics from one source modulate with the propagated waveforms coming from the other frequency source. Consequently, the interharmonic components settle in the sidebands of the fundamental and harmonic frequencies. The second mechanism is associated with the asynchronous switching of power converters, where, the output frequency of the power converter is not synchronized with the fundamental frequency of the power system. In this condition, interharmonic components

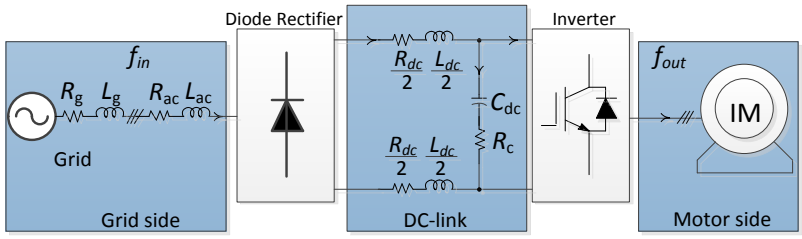


Figure 1.1: *Typical structure of a voltage sourced adjustable speed drive.*

may appear at different frequencies with respect to the power supply voltage harmonics. Practical applications which cause interharmonic distortions are adjustable speed drives [13–15], arcing loads [16–18], static converters [19], and ripple controls [19, 20].

In respect to interharmonic distortions, much research works are devoted to the identification of interharmonic sources, their adverse effects, and measurement strategies [12, 17, 21–25]. However, the ever increasing usage of power electronic devices made this issue even more important and there is an ongoing global discussion to set a regulation in the standards for interharmonic distortions.

1.2 Project motivation

As mentioned earlier, the presence of harmonic distortions in the power system may induce problems like overloading of neutrals, nuisance tripping of circuit breakers, over-stressing of power factor correction capacitors and zero-crossing noise. In addition, these distortions cause overheating and losses in transformers [26], and interference with communication lines [27].

With respect to interharmonic distortions, they can induce the same effects on the power system as those associated with the harmonic distortions [28, 29]. Basically, the common negative effects have less significance in the interharmonic distortions because of their typically smaller magnitudes compared with the harmonic one. Interharmonic components, although smaller in magnitudes, may cause their own unique problems. The problems have mainly roots on the interharmonic characteristics, where they can spread to a wide range in the frequency spectrum. Light flicker [30–32], sideband torques on the motor/generator shaft [33–35], interference with control and protection signals [19, 36, 37], dormant resonance excitation [15, 38, 39] are some of the most significant negative effects caused by interharmonic distortions.

Adjustable Speed Drives (ASDs) are considered as one of the main sources of interharmonics in the power system, where the load (induction machine, permanent magnet motor) is usually required to operate at different frequency conditions. Meanwhile, the ASD's input/output frequency interactions can lead to the input/output interharmonic components. Considering the ASD struc-

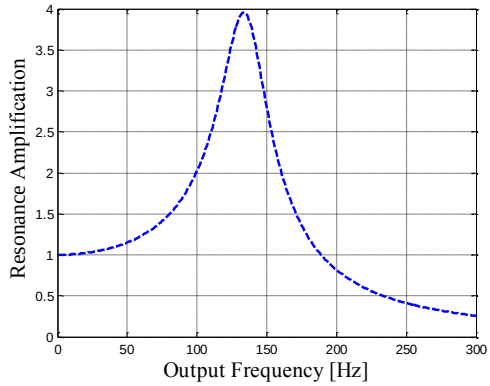


Figure 1.2: *A typical ASD's equivalent DC-link resonance amplification.*

ture shown in Figure 1.1, the DC-link filter (DC-link inductor L_{dc} and capacitor C_{dc}) and the AC-side inductor L_{ac} have significant effects on the drive interharmonics emission to the grid. The drive output harmonics when transferred to the grid side via the DC link, have to deal with an equivalent DC-link resonance amplification, as shown in Figure 1.2 (by using L_{ac}=4.5 mH, R_{ac}=0.2 Ω, L_{dc}=2 mH, R_{dc}=0.09 Ω, C_{dc}=125 μF, and R_c=0.5 Ω). Those DC-link oscillations accommodated around the resonance frequency will be magnified, and then give rise to a higher amplitude interharmonics in the grid side. Moreover, it can be seen in Figure 1.2 that the DC-link high order oscillations will be decreased while the filter's effect on the low frequency oscillations are negligible. Hence, an appropriate design procedure and well selection of drive passive filters can play an important role in the interharmonic emissions. Although, the authors in [13] discussed the relative effects of DC-link inductance and source inductance on interharmonic propagation, there is still a special need to consider the direct effects of the filter components on the input current interharmonics at different working points of the ASD.

The ASD's inverter modulation strategy may also play an important role in the interharmonics emission. The interharmonics generation process of the double-stage ASD has been studied in [14], where a naturally sampled Sinusoidal Pulse Width Modulation (SPWM) technique has been chosen for the inverter at a relatively low switching frequency. The theoretical analysis was realized to provide a good understanding of the harmonics interaction, and consequently to assess the interharmonics. However, more attention is needed to precisely analyze the ASD interharmonic frequencies in practical applications. In respect to the most common modulation techniques in drive applications (e.g., SPWM, Space Vector Modulation (SVM), and Discontinuous Pulse Width Modulation (DPWM2) techniques), it is worth to investigate their effects on the drive interharmonic components.

Besides many investigations dedicated to the interharmonic sources in ASDs,

mitigation of interharmonics is another scope, which has not been studied thoroughly. In [40], an investigation has been initiated with the intention of mitigating interharmonics by applying harmonic dithering. Although sound in concept, the dithering approach discussed in [40] is more for spreading the intensities of interharmonics over a frequency range, rather than eliminating them. In [41], an investigation has been initiated regarding interharmonics minimization by applying a DC-link active compensator. However, it has been implemented only in current source AC-drive and suffers also from applying a full-bridge inverter as an active compensator which definitely increases the costs.

The above considerations initiated this research project and the main motivation of this project is to examine the ASD input current interharmonics to find more optimal strategies, which can give rise to the less interharmonic components.

1.3 Project objectives

With the rapid growth of power electronics applications, the deteriorate effects of interharmonics are becoming more and more evident. Consequently, interharmonics power quality issues have gained more attention in the recent years. In order to address the identified shortfalls, the objectives of this project are,

- How the effect of the fixed frequency modulation techniques like SPWM, SVM and DPWM2 can be evaluated on the input current interharmonic components of the double-stage Voltage Source Inverter (VSI)-fed ASDs?
- What is the effect of ASDs filter (AC choke, DC choke, and DC-link capacitor) on the drive input current interharmonics distortion?
- How can the ASDs input current interharmonic components be reduced? Is it possible to mitigate distortions properly?

The goal of this dissertation is to scrutinize the interharmonic generation process in the double-stage VSI-fed ASD, where the most common fixed frequency modulation strategies (e.g., SPWM, SVM and DPWM2) in drive application are implemented. The obtained results will provide a good insight into the modulation technique effects on the interharmonics issues. Thereafter, the effect of the drive filter components on the input current interharmonics will be investigated in the cases of balanced and unbalanced output current. Moreover, for those interharmonics generated by the drive output current imbalance, some active compensators are applied to reduce the related interharmonics.

1.4 Thesis outline

The obtained results of this project are documented in the form of Ph.D. thesis, which consists of the ***Report*** and the ***Publications***. In the ***Report***, a summary of this research work is presented, whilst in the ***Publications***, the papers

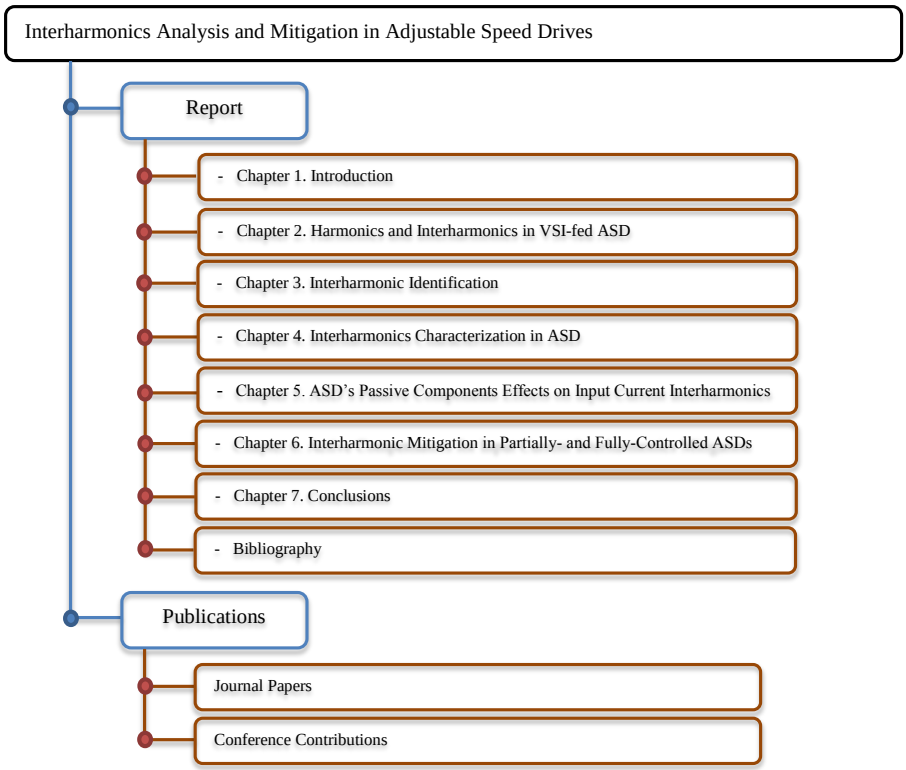


Figure 1.3: *Thesis structure with a report and publication part.*

derived in Ph.D. period are presented. A general framework of the project is shown in Figure 1.3 and is organized as follows:

A brief background of this research work is introduced in Chapter 1. It investigates the importance of the harmonic and interharmonic distortions in the grid. The motivation and objectives of the project are then addressed followed by the thesis outline.

Chapter 2 generally investigates the ASD's interharmonic components when a naturally sampled sinusoidal pulse width modulation technique is applied for the inverter switching. It shows how the drive output harmonic components may pass through the DC link and lead to input voltage and/or current interharmonic distortion.

Chapter 3 introduces some practical challenges with respect to interharmonics identification. The harmonics and interharmonics evaluation methods proposed by the IEC standard are also shortly presented. Then, a thorough discussion introduces existing desynchronized interharmonics detection methods, which are applied in this research work as highly accurate measurement strategies.

In Chapter 4, the double-stage VSI-fed ASD input current interharmonics are evaluated with respect to the adopted modulation techniques. The symmetrical regularly sampled SPWM, SVM, and DPWM2 techniques are selected as well as the asymmetrical regularly sampled SVM modulation technique, due to being the most popular modulation techniques applied in motor drive applications. Finally, the suitable strategy associated with the fixed frequency switching methods (i.e., SPWM, SVM, and DPWM2) is proposed in order to reduce the drive input current interharmonic components.

Chapter 5 investigates the effects of adjustable speed drive passive components on the input current interharmonics. The evaluation has been done both for the unbalanced and balanced motor current cases.

Chapter 6 suggests implementing some active compensation methods in order to reduce the drive input current interharmonics generated by the motor current imbalance. In the case of a partially-controlled ASD, an AC-side or DC-side parallel active compensators are proposed to decrease the drive interharmonic components. Also for the fully-controlled ASD (with applying a back-to-back converter), a control strategy is proposed to reduce the drive input current interharmonics.

Chapter 7 concludes the thesis, summarizes the main contributions of this research, and gives some proposals for future work.

1.5 List of publications

A list of the papers derived from this project, which are published till now or have been submitted, is given as follows:

Journal Papers

J1. **H. Soltani**, F. Blaabjerg, F. Zare, and P. C. Loh, "Effects of passive components on the input current interharmonics of adjustable-speed drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 1, pp. 152–161, Mar. 2016.

J2. **H. Soltani**, P. Davari, F. Zare, P. C. Loh, and F. Blaabjerg, "Characterization of input current interharmonics in adjustable speed drives," *IEEE Trans. Power Del.*, Under second review.

Conference Contributions

C1. **H. Soltani**, P. C. Loh, F. Blaabjerg, and F. Zare, "Sources and mitigation of interharmonics in back-to-back controllable drives," in *Proc. IEEE-EPE*, 2014, pp. P.1– P.9.

C2. **H. Soltani**, P. C. Loh, F. Blaabjerg, and F. Zare "Interharmonic analysis and mitigation in adjustable speed drives," in *Proc. IEEE-IECON Conf.*, 2014, pp. 1556–1561.

C3. **H. Soltani**, P. Loh, F. Blaabjerg, and F. Zare, "Interharmonic mitigation of adjustable speed drives using an active DC-link capacitor," in *Proc. ICPE-ECCE Asia*, 2015, pp. 2018–2024.

C4. **H. Soltani**, P. Davari, F. Zare, P. C. Loh, and F. Blaabjerg, "Input current low-frequency interharmonics in adjustable speed drives caused by different

modulation techniques," in *Proc. IEEE-APEC*, 2016, Accepted/In press.

Chapter 2

Harmonics and Interharmonics in VSI-fed ASD

This chapter focuses on the harmonics and interharmonics generation process in a double-stage VSI-fed ASD, where a three-phase diode rectifier is connected to an inverter sharing a common DC link. The inverter output harmonic components are first analzed when using the SPWM modulation technique. Then, the interaction between the inverter output-side harmonics and the diode rectifier input-side harmonics, which can lead to the drive input-side interharmonics, are discussed.

2.1 Introduction

Double-stage voltage sourced AC-DC-AC ASDs are witnessed as a major source of interharmonics in the power system. A block diagram of adjustable speed drives with the associated harmonics and interharmonics interactions are shown in Figure 2.1. In this respect, fundamental frequency, f_{in}, of the grid is first rectified via a three-phase diode rectifier. Then, at the DC link, when using passive filters (inductor and capacitor), a smoother DC voltage is obtained to feed the rear-end PWM inverter. Finally, the three-phase inverter supplies the output loads at the required power and frequency levels. Since the diode rectifier and the PWM inverter convert the fundamental frequency by switching operations, they produce harmonics associated with the fundamental frequencies. Considering that in ASD applications, the output frequency varies in a wide range, the system's input frequency, f_{in}, is different with the output frequency, f_{out}. The harmonic components at both sides, when propagated through the DC link, will interact with the other side harmonic components, which in turn will give rise to the interharmonics at both sides of the ASD.

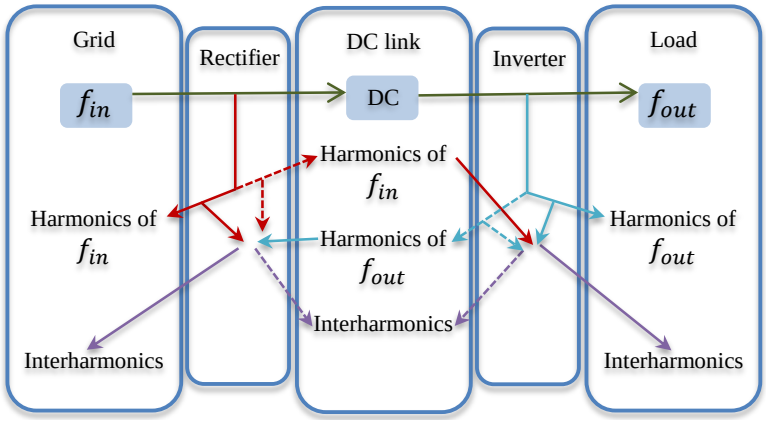


Figure 2.1: *Block diagram of a double-stage voltage sourced ASD with the associated harmonics and interharmonics interaction.*

Harmonic and interharmonic frequencies in ASD are characterized by the configuration of the devices. The ASD structure and the associated modulation technique determine the interharmonic locations. Although some other issues such as the load torque variations and motor shaft eccentricity may also cause interharmonic components in ASD, they are not included in the scope of this dissertation. In this chapter, harmonic and interharmonic components associated with the double-stage VSI-fed ASD are analyzed, when the naturally sampled SPWM modulation technique is implemented.

2.2 Harmonic analysis

2.2.1 Three-phase diode rectifier

A three-phase diode rectifier is the most popular structure for rectifying the three-phase grid voltage in adjustable speed drive specially in the medium to higher power applications. As long as the regulated DC-link voltage meets the limitations at different loading conditions, this structure is an appropriate choice, otherwise, the diodes have to be replaced by switching devices such as thyristors and silicon-controlled rectifiers. Figure 2.2 shows the typical structure of a six-pulse diode rectifier. A proper design of the DC-link inductor L_{dc} and capacitor C_{dc} results in a smoother DC-link current and voltage variations, respectively.

Assuming the rectifier is supplied by an infinite bus, the DC-link voltage is formed of six hump-shape ripples at one fundamental period of the power supply, as shown in Figure 2.3. Considering a ripple-free DC-link current i_{rect}, the input current i_a is composed of periodic rectangular pulses with the frequency of the grid fundamental component. Hence, the diode rectifier's input current can be mathematically represented by the well-known Fourier expansion and

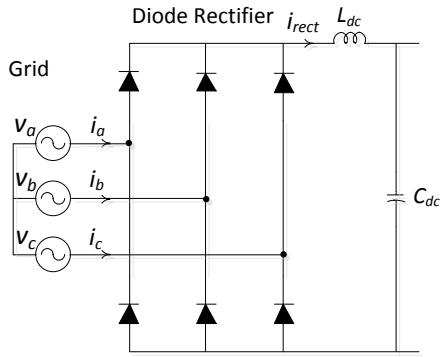


Figure 2.2: *Typical structure of a six-pulse diode rectifier connected to a stiff grid.*

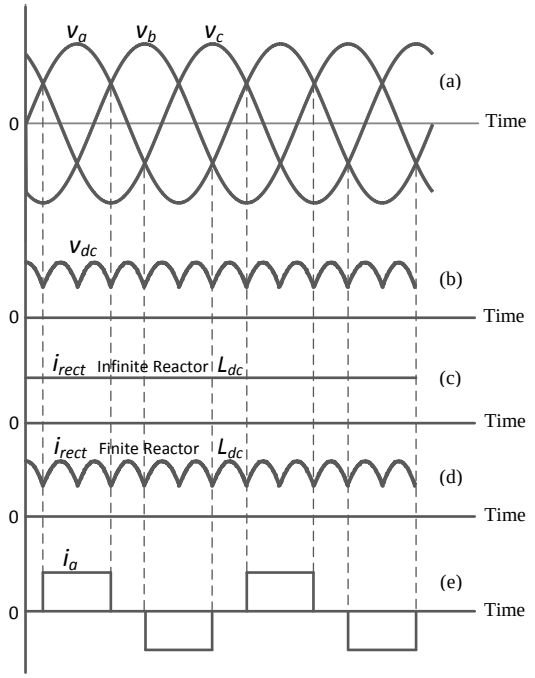


Figure 2.3: *Diode rectifier voltages and currents waveforms. (a) Three-phase input voltages. (b) DC-link voltage. (c) DC-link current with infinite size inductor. (d) DC-link current with finite size inductor. (e) Input current with infinite size inductor.*

it is given as below,

$$\begin{aligned} i_a &= \tfrac{2\sqrt{3}}{\pi} i_{rect}[\cos 2\pi f_{in}t - \tfrac{1}{5}\cos 2\pi(5f_{in})t + \tfrac{1}{7}\cos 2\pi(7f_{in})t - ...] \\ &= \tfrac{2\sqrt{3}}{\pi} i_{rect}[\cos 2\pi f_{in}t \pm \sum_{k'=1}^{\infty} \tfrac{1}{6k'\pm 1}\cos[(6k' \pm 1)(2\pi f_{in})t] \end{aligned} \tag{2.1}$$

where, the DC-link current and the grid fundamental frequency are notated as i_{rect} and f_{in} respectively. In the calculation of (2.1), the DC-link current $i_{rect}$is considered as constant value due to applying a large DC-link inductor L_{dc}. In a practical condition, the DC-link current see the oscillation with the same frequencies as those of the DC-link voltage. Thus, it contains the 6th order multiples of the grid fundamental frequency, and its frequency components f_{dc}^h can be represented as,

$$f_{dc}^h = 6 \cdot m \cdot f_{in} \qquad m = 1, 2, 3, ... \tag{2.2}$$

From (2.1), it can be noted that the input currents have the frequency orders of $(6k' \pm 1)$ with respect to the fundamental frequency. The harmonic frequency of $(6k' \pm 1)f_{in}$ can then be modulated with the 6th order oscillations of DC-link current i_{rect}, by implementing the trigonometric identity given in (2.3),

$$sin\, a \cdot sin\, b = \frac{1}{2}[cos\,(a-b) - cos\,(a+b)] \tag{2.3}$$

By substituting (2.2) into (2.1), and, using the trigonometric identity of (2.3), the input current harmonic frequencies f_{in}^h can be described as

$$\begin{aligned} f_{in}^h &= [6 \cdot (k' + m) \pm 1] \cdot f_{in} \\ &= (6k \pm 1) \cdot f_{in} \qquad\qquad k = 1, 2, 3, ... \end{aligned} \tag{2.4}$$

2.2.2 Pulse width modulated inverter

Voltage source inverter fed ASDs are widely used in industry [42] from low to medium-high power applications, where they convert up to a few MVA power ratings. SPWM modulation technique is considered as one of the major modulation methods implemented on ASDs inverter, mainly because of its simple structure and linear controllability. In this chapter, the harmonic and interharmonic analyses are performed based on the synchronous naturally sampled SPWM, where the carrier frequency f_c is a multiple integer of the drive's output fundamental frequency f_{out}. It is worth to mention that implementing a non-synchronous PWM may cause undesired harmonics in the inverter output, and consequently, can give rise to unknown input current interharmonics.

Figure 2.4 shows the general structure of a three-phase IGBT inverter, which supplies the Induction Machine (IM) as a load. As a result of the switching, the DC-link voltage will be converted to a pulse train, whose fundamental frequency is equal to the desired output frequency. Figure 2.5 illustrates the modulation process leading to the inverter output switched pulse train. By

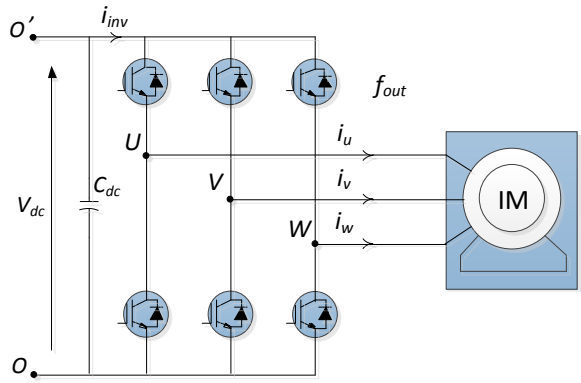


Figure 2.4: *PWM inverter feeding three-phase Induction Motor (IM).*

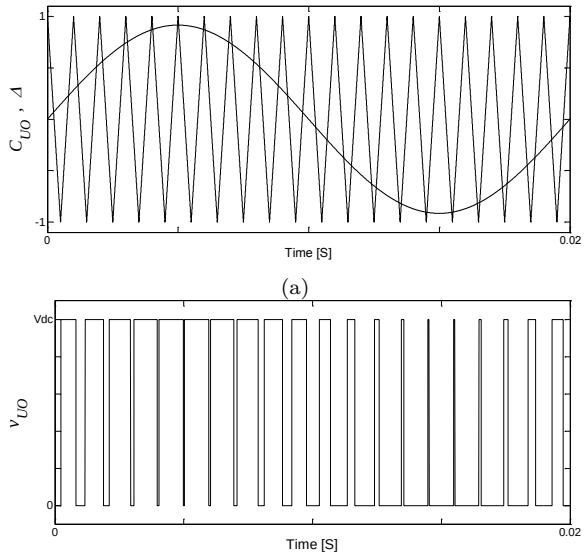


Figure 2.5: *Synchronous sinusoidal PWM: (a) C_{UO} is the sinusoidal modulation signal for the phase U, and, Δ is the carrier signal, (b) v_{UO} is the output voltage pulse train with reference to Figure 2.4.*

comparing the carrier signal Δ with the modulation signal C_{UO}, the output voltage pulse train v_{UO} is generated. The output voltages v_{VO} and v_{WO} can also be obtained by comparing Δ with other two modulation signals C_{VO} and C_{WO}, which are phase shifted by 120° and 240° with respect to C_{UO}. The generated pole voltages contains a DC value V^0, the fundamental component v^1_{XO} and harmonics $\tilde{v}_{XO}$ (mainly located around the switching frequency and

its multiples), and consequently can generally be presented as follows,

$$v_{XO} = V^0 + v^1_{XO} + \tilde{v}_{XO} \tag{2.5}$$

where X denotes the nodes U, V and W shown in Figure 2.4. The harmonic components $\tilde{v}_{XO}$ can be considered as follows,

$$\tilde{v}_{XO} = \sum_{n=2}^{\infty} A_n \sin(2\pi n f_{out} t + n\varphi_X) \tag{2.6}$$

with A_n and f_{out} representing Fourier coefficient and the fundamental frequency of the output voltage. The phase angle of C_{XO} ia also notated as φ_X. The Fourier coefficient A_n can be calculated as [14],

$$\begin{aligned} A_n &= \tfrac{m_a V_{dc}}{2} \left\{ \sum_{p=1}^{\infty} [1-(-1)^{n+p\cdot(m_f-1)}] \cdot \; R(n,p,m_f,m_a,\varphi_X) \right\} \\ &= \tfrac{m_a V_{dc}}{2} \left\{ \sum_{p=1}^{\infty} Q(\cdot) \;\; \cdot \;\; R(n,p,m_f,m_a,\varphi_X) \right\} \end{aligned} \tag{2.7}$$

where the modulation index m_a is the ratio of amplitudes between the reference and carrier signal. The pulse ratio m_f is defined by the ratio between the carrier and the fundamental frequency, and,

$$R(\cdot) = \frac{J_{pm_f+n}(p\varepsilon)\cdot e^{ipm_f\varphi_X} - J_{pm_f-n}(p\varepsilon)\cdot e^{-ipm_f\varphi_X}}{p\varepsilon} \qquad \text{with } \varepsilon = \tfrac{(m_a\pi)}{2} \tag{2.8}$$

The coefficients in (2.7) contain $J_y(z)$, which represents the Bessel functions of the first kind of the order y and argument z. By substituting (2.7) into (2.6), and after some manipulations, the inverter output harmonic components $\tilde{v}_{XO}$ can be obtained as,

$$\tilde{v}_{XO} = \tfrac{V_{dc}}{\pi} \sum_{\substack{n=-\infty,\\ n\neq\{0,\pm1\}}}^{+\infty} \sum_{p=1}^{+\infty} \{Q(\cdot)\, J_{pm_f+n}(\tfrac{pm_a\pi}{2}) \; \tfrac{1}{p} \; \sin[2\pi n f_{out} t + (pm_f+n)\varphi_X]\} \tag{2.9}$$

Regarding (2.5), it is worth to mention that, if the pulse ratio m_f is chosen to be an *odd* integer value then v_{XO} contains only odd harmonics and the DC component V^0 is exactly equal to $\frac{V_{dc}}{2}$. However, selecting an *even* integer value for m_f results in both *odd* and *even* harmonics for v_{XO}. Moreover, the DC component V^0 may be different from $\frac{V_{dc}}{2}$.

With respect to the parity of m_f, the harmonic components of $\tilde{v}_{XO}$ in (2.9) can be investigated. The $Q(\cdot)$ term in (2.9) can be either 0 or 2. If m_f is chosen to be an *odd* value, then $Q(\cdot)$ can be rewritten as follows,

$$Q(\cdot) = 1-(-1)^{n+p(m_f-1)} = 1-(-1)^n \tag{2.10}$$

Table 2.1: *Parameters p and k regarding even and odd m_f in terms of harmonic analysis using synchronous SPWM.*

odd m_f		even m_f	
p	k	p	k
even	odd	even	integers
odd	even	odd	integers

From (2.10) it can be seen that the value of $Q(\cdot)$ only depends on n parameter. Considering an *odd* integer value for n, it can be represented as $(-p \cdot m_f + k)$, and, $\tilde{v}_{XO}$ in (2.9) can be rearranged as

$$\tilde{v}_{XO} = \frac{2V_{dc}}{\pi} \sum_{p=1}^{+\infty} \frac{1}{p} \sum_{k=-\infty}^{+\infty} \{J_k(\tfrac{pm_a\pi}{2}) \ \sin[2\pi(-pm_f + k)f_{out}t + k\varphi_X]\}, \quad p + k = odd \tag{2.11}$$

However, if m_f is chosen to be an *even* value, $Q(\cdot)$ is dependent on both n and p. In this case, $\tilde{v}_{XO}$ in (2.9) can contain all harmonic components, and, n can generally be represented as $(p \cdot m_f + k)$, where, p and k can be all integer values.

Regarding the parity of m_f, the harmonic components at the inverter output side can be expressed as,

$$f_{out}^h = |p \cdot m_f \pm k| \, f_{out} \tag{2.12}$$

with f_{out} and f_{out}^h denoting the fundamental frequency and the harmonic components at the output of the inverter respectively. The feasible sets of p and k in respect to the m_f value are listed in Table 2.1.

2.3 Interharmonic analysis

In a double-stage VSI-fed ASD, where a front-end three phase diode rectifier is connected to a PWM inverter back-to-back via a DC-link filter, the existing harmonics in the grid side and the load side can be transferred to the other side through the DC link, and consequently, can give rise to the interharmonics generation at the drive's input side, DC link and load side.

In order to analyze the harmonics interaction in the ASD, it is assumed that the inverter does not dissipate or generate power and the load is also balanced. In this condition, the DC-link inverter-side current i_{inv} can be obtained as,

$$i_{inv} = \frac{1}{V_{dc}}(v_{UO} \cdot i_u + v_{VO} \cdot i_v + v_{WO} \cdot i_w) \tag{2.13}$$

where v_{UO}, v_{VO} and v_{WO} denote the three-phase pulsating voltages associated with the poles UO, VO and WO, respectively. The drive's output currents are represented as i_u, i_v and i_w and they are defined in Figure 2.4.

Table 2.2: *Parameters p and r regarding even and odd m_f in terms of harmonic analysis using synchronous SPWM.*

odd m_f		even m_f	
p	r	p	r
even	even	even	integers
odd	odd	odd	integers

According to (2.13), the harmonic components of the DC-link inverter-side current i_{inv} can be evaluated by modulating the harmonics of v_{UO}, v_{VO} and v_{WO} with those of the corresponding currents i_u, i_v and i_w. The harmonic components of the inverter pole voltage v_{XO} with $X = U, V, W$ are evaluated as (2.12). By selecting the induction motor as a load and considering a balanced operation, the harmonic components of the output currents are accommodated at the same frequencies as those of the corresponding voltages. The harmonic components $f^h_{dc,out}$ of the DC-link inverter-side current can thus be deduced as [14],

$$f^h_{dc,out} = |p \cdot m_f \pm (k \pm 1)|\, f_{out} = |p \cdot m_f \pm r|\, f_{out} \tag{2.14}$$

where the parameters p and k can be assigned based on Table 2.1 and the parameter $r = k \pm 1$. The feasible combination of p and r with respect to m_f is represented in Table 2.2. The harmonic components $f^h_{dc,out}$ of the DC-link inverter-side current with implementing a SPWM modulation technique will then interact with the drive input current harmonics and consequently will give rise to the drive input current interharmonics. It is worth to mention that the six-order harmonics f^h_{dc} in the DC link, generated by the front-end diode rectifier will also interact with the inverter output-side harmonics and can lead to load-side interharmonics. A feasible ASD input current interharmonics can be represented as follows,

$$f^{ih}_{in} = |(6m \pm 1) \cdot f_{in} \pm (pm_f \pm r) \cdot f_{out}| \tag{2.15}$$

where $m = 0, 1, 2, \ldots$, and, p and r can be obtained from Table 2.2. Recalling the equations (2.2) and (2.12), the drive output current interharmonics can also be represented as,

$$f^{ih}_{out} = |6m \cdot f_{in} \pm (pm_f \pm k) \cdot f_{out}| \tag{2.16}$$

where $m = 1, 2, \ldots$, and, p and k can be obtained from Table 2.1. As for the pulse ratio m_f value, it is also worth to mention that an integer value should be adopted in order to have a synchronous PWM. Thus the modulation ratio can generally be represented as,

$$m_f = round(\tfrac{f^*_{sw}}{f_{out}}) \tag{2.17}$$

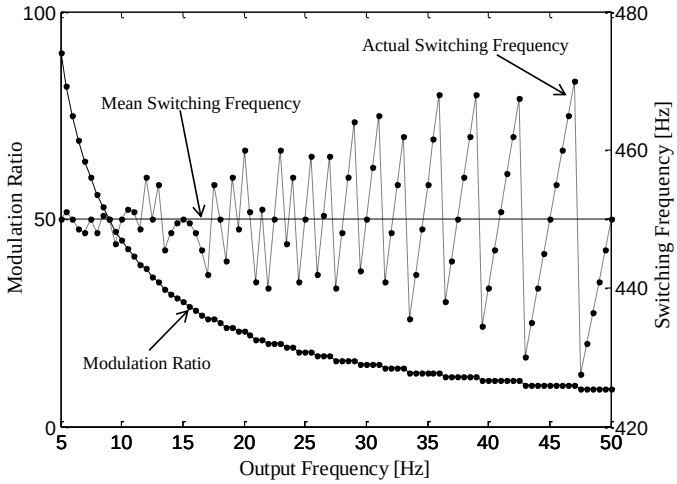


Figure 2.6: *The inverter modulation ratio m_f and the switching frequency f_{sw} when implementing the synchronous SPWM.*

where f_{sw}^* denotes the asynchronous switching frequency and the *round*(.) function gives the integer nearest to the argument. Figure 2.6 illustrates the modulation ratio variations in ASD, when a constant value of 450 Hz is adopted for the inverter mean switching frequency f_{sw}^* at different output frequencies f_{out}. The actual inverter switching frequency f_{sw} is also plotted in this figure. It can be seen that the modulation ratio varies, when the ASD is operating at different output frequencies.

The drive input current interharmonic frequencies with respect to the output frequency, obtained using (2.15) are represented in Figure 2.7. The required pulse ratio m_f is considered as that plotted in Figure 2.6. The source and the inverter mean switching frequencies are fixed at 50 Hz and 450 Hz, respectively. For the sake of clarity, only those interharmonic components generated by the interaction between some of the inverter output-side harmonics with the grid-side fundamental frequency component are shown in this figure. It is evident from Figure 2.7 that at some output frequency ranges, overlapping of the input-side interharmonic components can happen. In these conditions, it is sophisticated to separately address the interharmonics origins.

The above-mentioned theoretical analysis in respect to the ASD input current interharmonic frequencies was performed when a naturally sampled SPWM modulation technique is considered for the inverter operation. The interharmonic locations plotted in Figure 2.7 will provide good understanding of the ASD interharmonic generation process, when the motor works at different speeds.

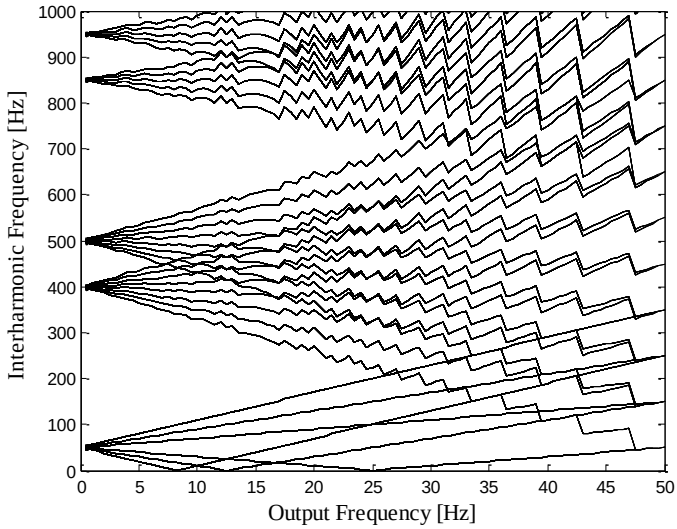


Figure 2.7: *The drive input current interharmonic frequency versus output frequency, obtained using equation (2.15), with* $m = 1$*, modulation ratio* m_f *as given in Figure 2.6, and* (p, r)=$\{(0, 2),\ (0, 4),\ (0, 6),\ (1, 1),\ (1, 3),\ (1, 5),\ (1, 7),\ (2, 0),\ (2, 2),\ (2, 4)\}$*.*

2.4 Summary

This chapter has demonstrated the interharmonics generation process in a double-stage voltage-source inverter-fed adjustable speed drive, composed of a three-phase diode rectifier along with a three-phase inverter. It has first evaluated the harmonic generation process in the front-end diode rectifier and at the rear-end PWM inverter. Then, the harmonic interactions are analyzed leading to the drive input-side/output-side interharmonics. The study was based on applying the naturally sampled Sinusoidal Pulse Width modulation technique and with an ideal grid condition.

Chapter 3

Interharmonic Identification

This chapter reviews some of the existing harmonic and interharmonic identification methods, which are introduced for the interharmonics detection and measurement. It first assesses some of the interharmonic estimation methods used for the stationary and the time-varying signals. Then, the harmonic and interharmonic distortion measurements based on a grouping method, referred to as the *IEC technique*, will be addressed. Finally, a desynchronized processing technique for harmonic and interharmonic analysis is discussed.

3.1 Introduction

Harmonic and interharmonic analysis have always been of great concern for the power quality issues, the control and also the protection of the power system. Assuming a stationary condition for harmonics, which is normally the case in comparison with other power quality disturbances, the harmonic analysis can be performed in the frequency domain by implementing the Discrete Fourier Transform (DFT) and its developed model referred to as Fast Fourier Transform (FFT) approaches. Measurement and analysis experiences have shown that with the presence of interharmonic components in the grid, the direct implementation of FFT can lead to inaccurate frequency analysis and a spectral leakage problem [17, 43, 44]. This inaccuracy can also happen when the grid fundamental frequency also witnesses some deviations from its nominal value, mainly because of the power mismatch between the source and the load [45]. Following the aforementioned difficulties, many investigations have been launched in recent years to estimate the power system harmonic and interharmonic component parameters with an acceptable level of accuracy.

The interharmonic identification method can generally be divided into three categories; DFT or FFT based methods, parametric methods with high resolution, and recursive dynamic analysis methods. Figure 3.1 represents a clas-

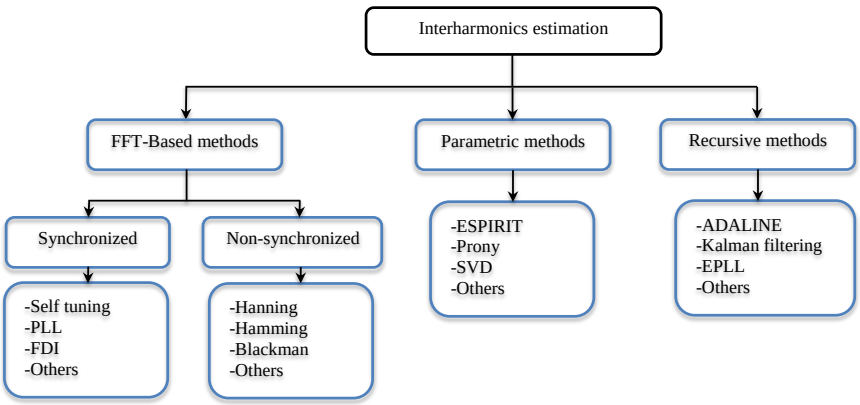


Figure 3.1: *Classification of the interharmonic estimation methods.*

sification of the commonly used interharmonic estimation methods. A brief explanation of these identification methods will be presented in the following section.

3.2 Interharmonic estimation methods

3.2.1 FFT-based methods

The power system frequency variation has a significant impact on the accuracy of the FFT when a fixed sampling frequency is used. Moreover, the picket-fence effect, which may occur due to adopting the insufficient fundamental frequency cycles, can result in inaccurate estimation with the presence of interharmonics. The minimum distinguishable interval in the frequency spectrum called frequency resolution f_0 can also be defined as,

$$f_0 = \frac{1}{T_w} = \frac{f_s}{N} \tag{3.1}$$

where N denotes the number of points sampled at the sampling frequency f_s, and, T_w is the duration of the observation window. The International Electrotechnical Commission (IEC) Standard 61 000-4-7 proposed a method to standardize the harmonic and interharmonic measurement [11]. According to this method, a Rectangular time Window (RW) of exactly ten cycles for 50 Hz systems or exactly twelve cycles for 60 Hz systems is recommended to utilize Discrete Fourier Transform (DFT), corresponding in both cases to approximately 200 ms. In this regard, the frequency resolution is fixed at 5 Hz and those interharmonics accommodated between the bins spaced of 5 Hz would spill over the adjacent interharmonic bins.

The FFT-based method can actually be divided into two parts; with the synchronized and the non-synchronized analysis approaches. In the synchronization approach, the power system fundamental frequency is estimated first

via implementing the synchronization techniques with re-sampling mechanism such as self-tuning window, Phase-Locked-Loop (PLL), Frequency-Domain Interpolation (FDI), and then the FFT will be performed, which will result in a frequency domain spectrum with less interference [46–49]. In some cases, instead of applying the synchronization with re-sampling mechanism, where the sampling frequency is synchronized with the fundamental frequency, the sampled data would be constructed again with the newly obtained sampling frequency via some interpolation techniques like Newton's method, polynomial, etc [43].

In order to reduce the estimation error and the spectral leakage problems in the non-synchronized approach, several windowing techniques such as Hanning, Hamming, Blackman can be implemented [50]. For further reduction of the harmonics spillover on the interharmonic components in this approach, a double-stage technique can be applied to filter the harmonics [51]. Further discussion associated with the non-synchronized estimation method will be presented later in this chapter.

3.2.2 Parametric methods

In non-synchronized conditions, the parametric methods can be applied in order to provide a frequency spectrum of the sampled signal with a high frequency resolution. The Estimation of Signal Parameters via Rotational Invariance Techniques (ESPRIT) and the Prony-based method are some of the most commonly used parametric approaches. In these methods, the estimation order and the interference from noise have significant influence on the measurement performance. The computational burden may increase, when a high accuracy is required.

The ESPRIT parametric method is applied to the entire data sequence, and, it employs sinusoidal models to estimate the frequencies and the amplitudes of the sampled signals [52–54]. The problem of estimating the signal parameters in a non-stationary data is addressed with implementing the sliding-window approach, which is very similar to the Short-Time Fourier Transform (STFT) as applied successfully for many years.

In the Prony's method, the sampled signal is approximated with a linear combination of complex conjugate exponentials (a polynomial), and it is not characterized by a fixed frequency resolution. The unknown polynomial coefficients for the identification of the frequency components can then be obtained with different approaches such as autocorrelation, covariance, autoregression, and singular value decomposition techniques [55–57]. In case of having a time-varying signal, an adaptive Prony's method can be applied for parameter estimation.

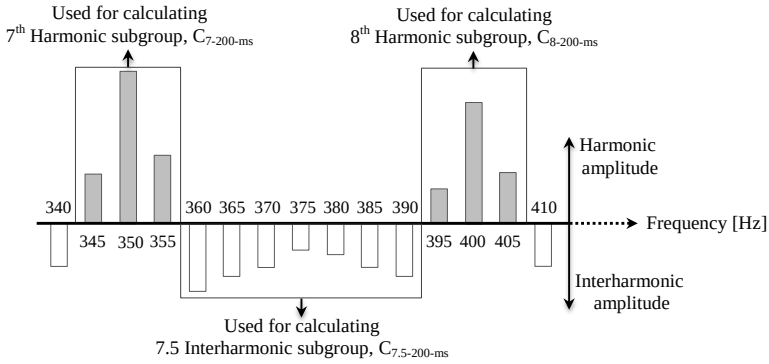


Figure 3.2: *Harmonics and interharmonics grouping based on IEC 61 000-4-30.*

3.2.3 Recursive methods

The recursive method is generally the parametric method, which assumes more knowledge about the spectrum of the analyzed signal. In order to estimate the parameters of the signal, a proper model should be selected. The Kalman filtering, the Adaptive Linear Element (ADALINE) and the Enhanced Phase-Locked-Loop (EPLL) are considered as the most commonly used recursive methods.

Kalman filtering is a state estimation method based on an optimal estimator with the minimum error covariance [58–60]. It introduces a set of dynamic state equations and a set of observation equations for the observed data. In order to accurately estimate the parameters, it is necessary to have good knowledge about dynamic process and the measurement model. The ADALINE method provides an adaptive filter for noise cancellation and signal extraction. Considering a large estimation order in this method, it experiences a heavy computational burden [61–63]. The EPLL method, which is able to estimate the frequency, amplitude, and phase angle of a signal, actually works as a bandpass filter [64–67]. Thus, for the harmonic and interharmonic estimation via EPLL, it is needed to be composed of several series and parallel connections.

Generally, the recursive methods are mostly suitable for harmonic estimation rather than interharmonics, because the interharmonics locations are not given beforehand, and consequently, they are not considered in the signal model. In order to implement these methods for interharmonics estimation, the decomposition bases should be increased, that may cause numerical stability and convergence problems.

3.3 Harmonics and interharmonics in standard framework

Voltage harmonics and interharmonics measurement methods and results interpretation approaches are recommended in the latest IEC standard draft IEC

61 000-4-30 [68]. It utilizes Discrete Fourier Transform (DFT), which is performed over a Rectangular time Window (RW) of exactly ten cycles for 50 Hz systems or exactly twelve cycles for 60 Hz systems, corresponding to a time window width (T_w) of 200 ms. It is also recommended to choose a sufficiently high sampling frequency f_s to allow for the analysis of frequency components up to 9 kHz. According to the IEC standard, Harmonic subgroup (HG) of amplitude $C^2_{n-200-ms}$ is defined as follows,

$$C^2_{n-200-ms} = \sum_{k=-1}^{1} C^2_{10n+k} \tag{3.2}$$

where C_i represents the rms value of the DFT output, shown in Figure 3.2. Interharmonic subgroup (IG) of amplitude $C^2_{n+0.5-200-ms}$ is introduced as,

$$C^2_{n+0.5-200-ms} = \sum_{k=2}^{8} C^2_{10n+k} \tag{3.3}$$

The general evaluation of the harmonic subgroup (HG) and interharmonic subgroup (IG) can be performed in a continuous condition, where borders of ± 7.5 Hz from the center of the harmonic groups and ± 17.5 Hz from the center of interharmonic groups are considered. Consequently, the general expression for harmonic and interharmonic subgroups, corresponding with those defined by the IEC standard, can be represented as follows,

$$C^2_{n-T_w-s} = G_w\Big(\sum_{k=-\alpha}^{\alpha} C^2_{n.10r+k} + \tfrac{\delta}{\delta_w}\big(C^2_{n.10r+\alpha+1} + C^2_{n.10r-\alpha-1}\big)\Big) \tag{3.4}$$

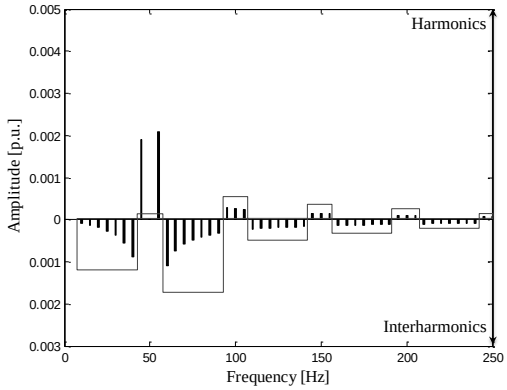
$$C^2_{n+0.5-T_w-s} = G_w\Big(\sum_{k=\beta}^{\gamma} C^2_{n.10r+k} + \tfrac{\delta}{\delta_w}\big(C^2_{n.10r+\beta-1} + C^2_{n.10r+\gamma+1}\big)\Big) \tag{3.5}$$

where the window grouping scale factor and the scallop loss are notated as G_w and δ_w respectively. The other parameters r, δ, α, β, and γ can be defined as,

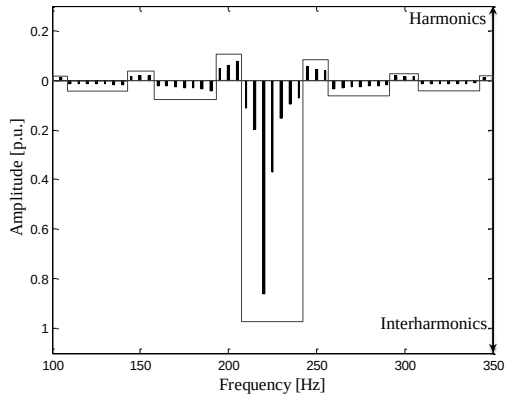
$$\begin{aligned} &r = \tfrac{T_w}{0.2};\ \ \delta = \lceil 1.5 \cdot r \rceil - \lfloor 1.5 \cdot r \rfloor;\ \ \alpha = N_F - 1,\ \ \beta = N_F + 1 - \delta; \\ &\gamma = \lceil 8.5 \cdot r \rceil - 1 \end{aligned} \tag{3.6}$$

with $N_F = \left\lceil \frac{7.5}{0.5} r \right\rceil = \lceil 1.5 \cdot r \rceil$.

As mentioned earlier, the spectral leakage can usually occur in power system waveform analysis, mainly due to the error in synchronizing the fundamental frequency and harmonics, and also, due to the picket fence effect, which is normally seen for measurement of those interharmonics non-synchronized with DFT bins. In this condition, applying the Rectangular Window (RW) for the harmonic and interharmonic grouping, based on IEC standard recommendation, can result in an inaccurate measurement [50]. This inaccuracy is mainly induced due to the rectangular window characterization in the frequency domain, with the narrowest main lobe, but the highest and slowly decaying side lobs. Figure 3.3 illustrates the effects of fundamental frequency f_1 deviation



(a)



(b)

Figure 3.3: *Frequency spectrum and grouping bars of the signal when applying a 200 ms rectangular window width, (a) The signal is a sinusoidal tone with amplitude of 1 p.u. and frequency of 50.01 Hz. (b) The signal is an interharmonic with amplitude of 1 p.u. and frequency of 221.5 Hz.*

and non-synchronized interharmonic on the harmonic and interharmonic grouping analysis when applying RW. As it can be seen from Figure 3.3(a), a small frequency variation in the fundamental frequency component, with frequency of f_1 =50.01 Hz and amplitude of 1 p.u., results in some errors in the harmonic and interharmonic grouping measurements. Figure 3.3(b) displays the grouping values and the frequency spectrum of a signal with amplitude of 1 p.u. and the frequency of 221.5 Hz. In this condition, the nearest bins are accommodated at 220 Hz and 225 Hz with the frequency resolution of 5 Hz using a rectangular time window of 200 ms, and consequently, the picket fence phenomena gives rise to the spectral leakage problem.

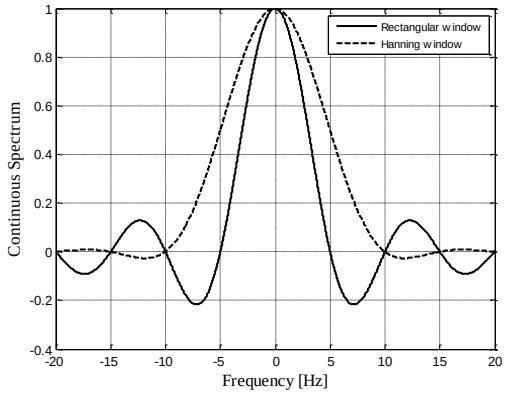


Figure 3.4: *Continuous spectrum of Rectangular Window (RW) and Hanning Window (HW).*

In order to reduce the leakage problem in constructing the harmonic and interharmonic groups, several windowing techniques with quickly decaying side lobes can be implemented. Meanwhile, applying a Hanning window is recognized as one of the most suitable cases that can be utilized for the harmonic and interharmonic groups construction, because of a main lobe width exactly double and side lobe width exactly equal compared to those of RW [69]. The spectral characteristics of the Rectangular and Hanning windows are depicted in Figure 3.4. Assuming the input sampled signal is defined as (3.7), then the signal component of the window spectrum can be represented as (3.8),

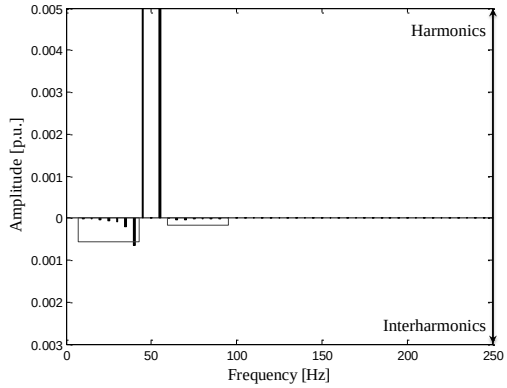
$$f(nT) = A \cdot \exp(+jw_k nT) \tag{3.7}$$

$$F(w_k) = \sum_n w(nT)\, A \exp(+jw_k nT) \exp(-jw_k nT) = A \sum_n w(nT) \tag{3.8}$$

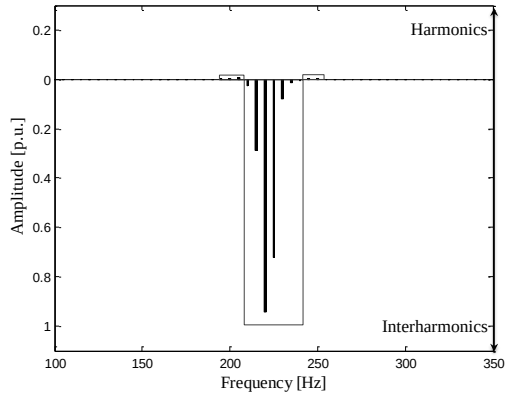
where $w(nT)$ represents the windowing weighting effect. As it can be seen in (3.8), the frequency spectrum is proportional to the signal amplitude. This proportional factor is the sum of the window terms. In a Rectangular window with N term, this proportionality factor is equal to N. In the case of applying the Hanning window, where the window slowly goes to zero near the boundaries, this factor will be reduced by half. Thus, in applying the Hanning window instead of the Rectangular window, a coherent gain of A_C =0.5 should be considered for the spectral amplitudes correction.

In order to apply the Hanning window in the harmonic and interharmonic grouping method, it should comply with the IEC standard framework. From Figure 3.4, it is evident that by implementing HW, a synchronized tone have two side components (0.5 p.u.) other than the central one (1 p.u.). This condition increases the grouping values, defined in (3.2) by half. So, a grouping gain can also be considered for applying HW as follows,

$$A_G = \sqrt{\tfrac{3}{2}} \tag{3.9}$$



(a)



(b)

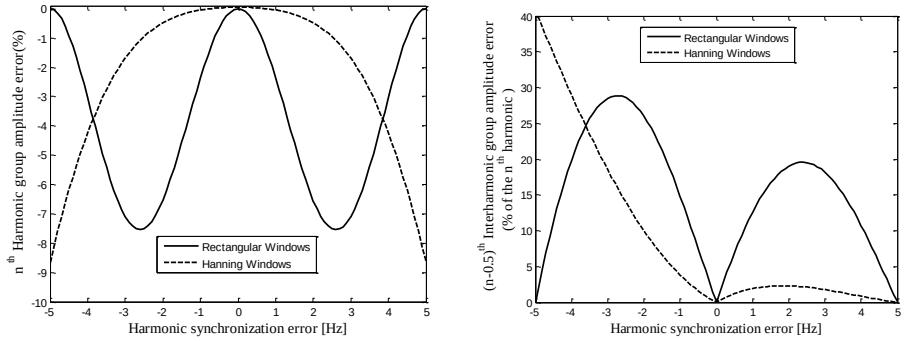
Figure 3.5: *Frequency spectrum and grouping bars of the signal with applying a 200 ms width Hanning window, (a) The signal is a sinusoidal tone with amplitude of 1 p.u. and frequency of 50.01 Hz. (b) The signal is an interharmonic with amplitude of 1 p.u. and frequency of 221.5 Hz.*

As a result of the above-mentioned correction factors, the required expression for the harmonic and interharmonic grouping measurement when using HW can be represented as follows,

$$C^2_{n-200-ms} = G_w \sum_{k=-1}^{1} C^2_{w-10n+k} \tag{3.10}$$

$$C^2_{n+0.5-200-ms} = G_w \sum_{k=2}^{8} C^2_{w-10n+k} \tag{3.11}$$

where C_w is the DFT coefficient and, G_w is the window grouping factor defined



(a) (b)

Figure 3.6: *Sensitivity analysis of the group amplitude error when applying different windowing techniques. (a) n^{th} HG amplitude error with respect to harmonic synchronization error. (b) $(n-0.5)^{th}$ IG amplitude error with respect to harmonic synchronization error.*

as,

$$G_w = \frac{1}{(A_C \cdot A_G)^2} \tag{3.12}$$

The efficiency of the grouping analysis with respect to using HW can be evaluated in the presence of the desynchronization tones as those assessed earlier in Figure 3.3. Figure 3.5 displays improvement in terms of the grouping values and spectral leakage problem. This improvement is mainly due to the lower side lobe level and its faster roll-off in HW with respect to RW. However, the larger main lobe in HW can give rise to a lower dynamics and resolution compared with the RW, especially for those tones which are close in the frequency. Thus, it is worth to consider a sensitivity analysis of the group amplitude error when applying different windowing techniques.

Figure 3.6 illustrates the harmonic and interharmonic group amplitude errors with respect to the harmonic synchronization error, when applying a 200 ms Rectangular and Hanning time windows. The harmonic synchronization error Δf_n is made via a 1 p.u. tone frequency deviation from the center of the estimated harmonic frequency f_{1e}, and, it is defined as,

$$\Delta f_n = n \cdot \Delta f_1 = n \cdot (f_{1e} - f_{1a}) \tag{3.13}$$

where the grid actual frequency value is noted as f_{1a}.

From the harmonic group amplitude error shown in Figure 3.6(a), it is evident that a small fundamental frequency variation may give rise to a significant error in the case of applying RW, specially at high order harmonics. For the interharmonic group amplitude, the same trend may occur with respect to the harmonic synchronization error, where the Rectangular windowing shows a poor performance compared with applying the Hanning windows, as shown

in Figure 3.6(b). However, in both cases, for the highest frequency deviations, applying the Hanning window may cause the same results as those of the Rectangular window.

3.4 Desynchronized processing technique

The harmonics frequency desynchronization gives rise to the most significant spectral leakage problem, which can reach to the same order of the interharmonics of interest, and consequently can lead to inaccurate interharmonic measurements. In order to reduce the leakage caused by the harmonic frequency deviation, a desynchronized processing technique can be implemented [51]. In this technique, the actual frequencies, amplitudes, and phase angles of the fundamental and harmonic components are first estimated via implementing a high accuracy frequency-domain interpolation [70, 71], and then the estimated harmonics will be filtered away from the sampled signal. Consequently, the remaining data can be assessed in terms of the interharmonic pollution by using the FFT, where the minimum harmonics leakage is present.

Generally, a power system signal $f(t)$, with the fundamental frequency of f_1, and sampled at a fixed sampling frequency f_s can be represented as,

$$f(k) = f(t)\ _{t=\frac{k}{f_s}} \qquad k = 1, 2, 3, ... \tag{3.14}$$

This sampled signal is composed of the harmonics f^H and interharmonics f^I components, and can be written as follows,

$$f(k) = f^H(k) + f^I(k) \tag{3.15}$$

After applying an appropriate window of length $T_w = L/f_s$, the sampled data can be represented as,

$$f_w(k) = f(k) \cdot w(k) \qquad k = 0, 1, ..., L-1 \tag{3.16}$$

Then, by applying the FFT, the signal spectrum can be evaluated. In the desynchronized windowing technique (T_w is selected as a fixed window with 10 times of the grid rated fundamental period), the FFT results in inaccurate parameters measurement. By adopting an appropriate frequency-domain interpolation techniques for the desynchronized spectral components, the frequency $\hat{f}_n$, the amplitude $\hat{A}_n^H$, and the phase angle φ_n^H of the harmonic components can be obtained. So, the estimated harmonic components can be considered as,

$$\hat{f}^H(k) = \sum_{n=1}^{N} \hat{A}_n^H \sin(2\pi \hat{f}_n \cdot k \cdot T_s + \hat{\varphi}_n^H) \qquad T_s = 1/f_s \tag{3.17}$$

The estimated harmonics signal can then be filtered from the original data sequence, which gives rise to the estimated interharmonic components as follows,

$$\hat{f}^I(k) = f(k) - \hat{f}^H(k), \qquad k = 0, 1, ..., L-1 \tag{3.18}$$

In this condition, the leakage effects caused by the harmonic tones are minimized and the interharmonic evaluation can be performed with high accuracy by implementing another appropriate windowing. Thus

$$\hat{f}^I_{w'}(k) = \hat{f}^I(k) \cdot w'(k) \qquad k = 0, 1, ..., L-1 \tag{3.19}$$

the windowed signal in (3.19) is used for the FFT analysis.

By applying the above-mentioned desynchronized procedure, the harmonic subgroup (HG) of amplitude $C_{n-200-ms}$, and the interharmonic subgroup (IG) of amplitude $C_{n+0.5-200-ms}$ should be redefined as follows,

$$C^2_{n-200-ms} = \sum_{i=-1}^{1} \left(\hat{F}^I(10n+i)\right)^2 + \left(\hat{A}^H_n\right)^2 \tag{3.20}$$

$$C^2_{n+0.5-200-ms} = \sum_{i=2}^{8} \left(\hat{F}^I(10n+i)\right)^2 \tag{3.21}$$

where the FFT components of $\hat{f}^I_{w'}$ in (3.19) is notated as $\hat{F}^I$.

According to the IEC standard, it is highly recommended to provide a smoothing of the results obtained during the analyses. Smoothed results derived from the average value over 15 contiguous time windows updated in each 200 ms (in a 3-second window) can be represented as,

$$C^2_{n-3-s} = \frac{1}{15} \sum_{i=1}^{15} C^2_{i,n-200-ms} \tag{3.22}$$

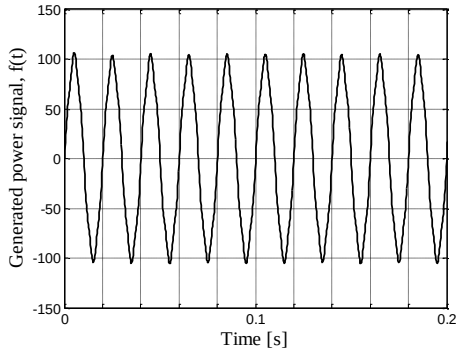
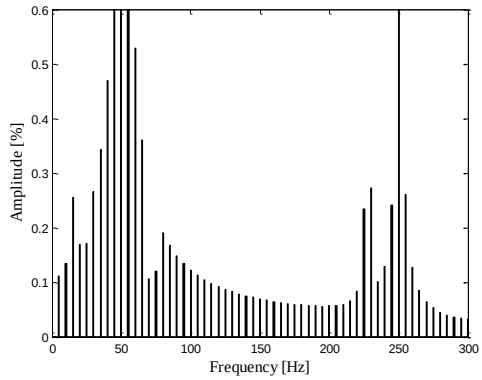


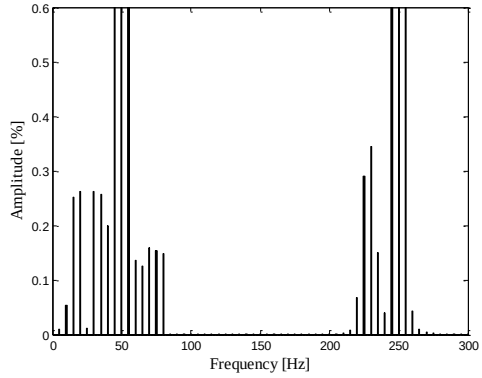
Figure 3.7: *A typical power system signal waveform, which is composed of the harmonic and interharmonic tones listed in Table 3.1.*

Table 3.1: *The generated harmonic and interharmonic tones for the i^{th} analysis.*

	harmonics		interharmonics					
Frequency [Hz]	50.05	250.25	17.5	32.5	70	75	227	230
Amplitude [%]	100	5	0.3	0.3	0.3	0.3	0.3	0.3
Phase angle [deg]	3.6(i-1)	18(i-1)	180(i-1)	180(i-1)	0(i-1)	0(i-1)	144(i-1)	0(i-1)



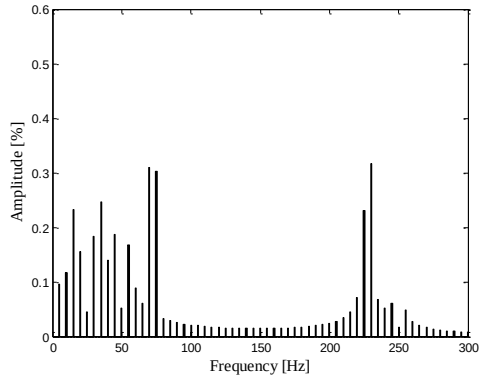
(a)



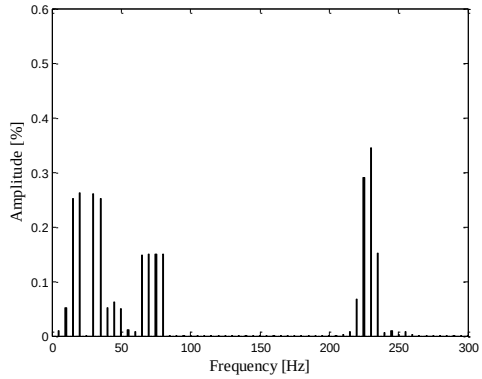
(b)

Figure 3.8: *Spectral components of the signal given in Table 3.1, by applying (a) RW complying IEC procedure. (b) HW complying IEC procedure.*

Figure 3.7 displays the time-domain waveform of a typical power system signal, whose harmonic and interharmonic tones are listed in Table 3.1. The corresponding spectral components of the signal is shown in Figure 3.8, by applying the IEC Rectangular and Hanning windows measurement techniques. The tones phase variations for evaluating the 15 analyses in a 3-second window are considered according to the formulas provided in Table 3.1. The results obtained by implementing the desynchronized processing Rectangular window DP RW and Hanning window DP HW, according to the IEC procedure, are presented in Figure 3.9. The comparative results of the interharmonic groups (0.5, 1.5, 2.5, 3.5, 4.5, 5.5 corresponding to the frequency ranges [10-40], [60-90], [110-140], [160-190], [210-240], [260-290] Hz) are listed in Table 3.2. It can be seen that applying the Rectangular window can lead to higher measurement errors due to the spectral leakage phenomena. Moreover, it is evident that



(a)



(b)

Figure 3.9: *Spectral components of the signal given in Table 3.1, by applying (a) Desynchronized RW complying IEC procedure. (b) Desynchronized HW complying IEC procedure.*

Table 3.2: *Comparative results of Interharmonic subgroups IGs with implementing different techniques.*

Groups	Actual value	RW	HW	DP RW	DP HW
0.5	0.42%	0.77%	0.46%	0.48%	0.42%
1.5	0.42%	0.73%	0.26%	0.50%	0.24%
2.5	0.00%	0.24%	0.00%	0.04%	0.00%
3.5	0.00%	0.16%	0.00%	0.04%	0.00%
4.5	0.42%	0.43%	0.40%	0.42%	0.40%
5.5	0.00%	0.19%	0.04%	0.04%	0.00%

applying the HW improves the results accuracy. It is worth to mention that, although the standard IEC procedure can be improved by using the HW and the

desynchronized techniques, it is still inadequate to estimate all interharmonic groups.

3.5 Summary

This chapter has discussed different harmonic and interharmonic identification methods. The FFT-based, the parametric, and the recursive methods were compared in terms of interharmonics identification and detection. Then, the harmonic and interharmonic subgroup terms, defined based on the IEC standard framework, were evaluated and discussed. The effect of the windowing techniques in standard framework were investigated with respect to the spectral leakage problem. Finally, a double-stage interharmonic identification method called "desynchronized processing technique" was assessed, which seems to give the best results. However, the main focus in this thesis is to investigate the interharmonic sources in ASD, and consequently, in order to provide a high accuracy identification for our measurement, a 3-second Hanning window is used for the experimental results.

Chapter 4

Interharmonic Characterization in ASD

This chapter characterizes the input current interharmonics of a double-stage VSI-fed ASD, when different fixed frequency modulation techniques are applied on the inverter. The effects of symmetrical regularly sampled modulation strategies on the ASD input current interharmonic distortion will be presented at three different modulation techniques SPWM, SVM, and DPWM2. The interharmonic generation process is thoroughly developed from the inverter output side to the rectifier input side. Moreover, the effect of the asymmetrical regularly sampled SVM method will be presented.

4.1 Introduction

The interharmonic amplitudes, frequencies and origins can be subjected to further investigation in order to characterize theses components. Their amplitude investigation is highly important for compatibility problems. The precise analysis of interharmonics amplitude produced by ASDs is difficult, especially realizing that different real-world factors such as the grid background distortion and the converter non-linearities may easily affect the drive interharmonical performance. Nevertheless, evaluation of the drive input current interharmonics amplitude needs to be performed in all operating conditions of the drive [72,73]. The interharmonics frequency evaluation has also been of highly importance, which has initiated some research works focusing on their origins [14, 15]. By knowing the interharmonics location in advance, the optimal operating strategy can be adopted to avoid the undesirable consequences.

The interharmonics generation process of the double-stage ASD has been studied in [14], where a naturally sampled Sinusoidal Pulse Width Modulation (SPWM) technique has been chosen for the inverter at relatively low switching frequency. The theoretical analysis was realized to provide a good understanding of the harmonics interaction, and consequently to assess the interharmonics.

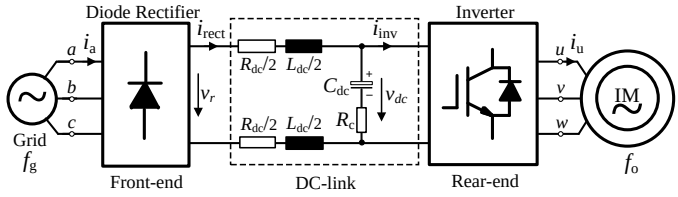


Figure 4.1: *Equivalent circuit diagram of an adjustable-speed drive for system analysis with an Induction Motor (IM).*

However, more attention is needed to precisely analyze the ASD interharmonics frequencies in practical applications.

In a digital implementation of the pulse width modulation techniques, it is difficult to apply the naturally sampled modulation strategy due to its complexity. Instead, the regularly sampled modulation strategies, symmetrical and asymmetrical, which can be easily implemented digitally are selected as the most appropriate modulation methods. In addition, the literature studies show the better performance of asymmetrical regularly sampled modulation technique compared with the symmetrical one from a harmonic point of view [74]. In this regard, the effects of the symmetrical and/or asymmetrical regularly sampled modulation strategies on the drives interharmonics frequency locations can be subjected to further investigation.

In this chapter the ASD's input current interharmonic frequencies will be analyzed, when the fixed frequency modulation techniques (i.e., the symmetrical regularly sampled SPWM, SVM, and DPWM2 modulation techniques) are selected for inverter operation. It shows how the inverter output side harmonics caused by the double-edge symmetrical regularly sampled modulation may flow into the grid and consequently may result in the drive input current interharmonic components. Moreover, a frequency mapping is derived for the associated interharmonic frequencies. In addition, the possible effects of the double-edge asymmetrical regularly sampled SVM on the interharmonics location will be evaluated and discussed. A comparison between the symmetrical and asymmetrical strategies is made to illustrate their performances from an interharmonics perspective.

4.2 Harmonics transfer at inverter level

In this section, the transfer of the ASD output side harmonics through the inverter stage will be investigated. The double-stage ASD system model is illustrated in Figure 4.1. The system begins with a three-phase diode-bridge rectifier which rectifies the AC supply voltage and provides the desired voltage level in the DC link. The provided DC-link filters (i.e., DC-link inductors and capacitor) will lead to a smoother current and voltage for powering the rear-end inverter. The inverter is then used to synthesize three-phase balanced

voltages at the output terminals with an arbitrary frequency f_o from the DC-link voltage.

With applying a pulse width modulation strategy, where a low-frequency reference signal is compared with a high-frequency carrier signal, the switched output voltage waveforms can be obtained. Since the PWM process does not generally generate periodic pulsating waveforms, a double-Fourier integral approach can be applied to analytically quantify the harmonic components of the inverter output voltage. As a result, the general form of the output voltages v_x $(x = u, v, w)$ can be expressed as (4.1), with a DC component, baseband harmonics (simple harmonics of the fundamental output frequency f_o), harmonics of the carrier frequency f_c, and carrier sidebands, which are accommodated around the carrier harmonics [74]

$$\begin{aligned} v_x(t) = \tfrac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(n[w_o t - p\tfrac{2\pi}{3}]) \\ + B_{0n}\sin(n[w_o t - p\tfrac{2\pi}{3}])] \\ + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} [A_{mn}\cos(mw_c t + n[w_o t - p\tfrac{2\pi}{3}]) \\ + B_{mn}\sin(mw_c t + n[w_o t - p\tfrac{2\pi}{3}])] \end{aligned} \tag{4.1}$$

with m and n variables stating the carrier index and the baseband index, respectively. The fundamental and carrier angular frequencies are also defined as w_o and w_c, respectively. The p values are 0, 1 and -1 with respect to the output phases u, v and w. The spectral coefficients A_{mn} and B_{mn}, which are defined by a double Fourier series can be obtained according to the selected modulation strategy.

The PWM process is normally implemented with the three most commonly used sampling strategies; the naturally sampling, the symmetrical regularly sampling and the asymmetrical regularly sampling strategies. In a digital implementation of a naturally sampling technique, where a pure sinusoidal reference waveform should be compared with the carrier signal, it is difficult to find the exact intersection point between the modulation and modulating signals. As a result, the regularly sampled (symmetrical and/or asymmetrical) modulation methods are mostly applied for the PWM process. The implementation strategies of the symmetrical and asymmetrical regularly sampled modulation techniques are depicted in Figure 4.2(a) and (b). As it can be observed, for the symmetrical case the sampled signal during each carrier interval is used to be compared with the respected carrier waveform at the next carrier interval. As for the asymmetrical one shown in Figure 4.2(b), it can be observed that the same comparative process is performed during each half carrier interval.

The theoretical closed form solutions of the average pole voltage corresponding with the double-edge symmetrical regularly sampled SPWM, SVM, and DPWM2 techniques can be obtained with a considerable manipulation as given in (4.2)–(4.4), respectively. The corresponding solution in respect to the double-edge asymmetrical regularly sampled SVM is also given in (4.5). The parameter q is defined as $q = m + n(w_o/w_c)$. The coefficients in (4.2)–(4.5)

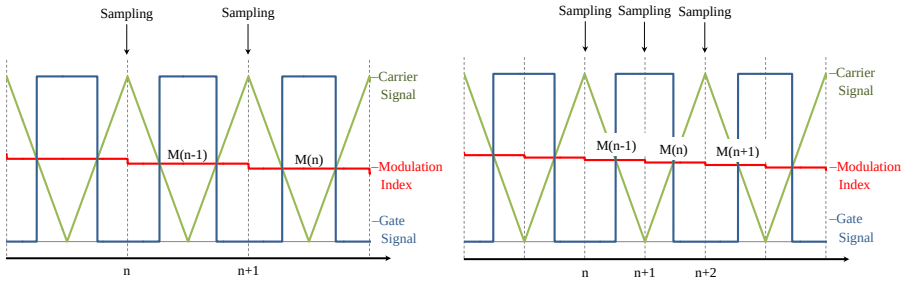


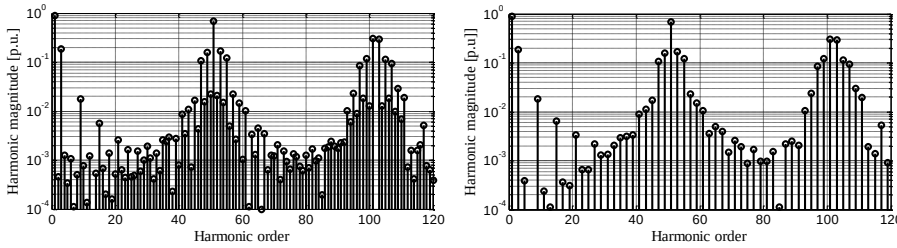
Figure 4.2: *Modulation schemes. (a) Model of the symmetrical regularly sampled modulation strategy with the corresponding gate signal. (b) Model of the asymmetrical regularly sampled modulation strategy with the corresponding gate signal.*

contains $J_y(z)$, which represents the Bessel functions of the first kind of the order y and argument z.

Figure 4.3(a) and (b) shows the inverter output voltage frequency spectrum normalized with respect to the DC-link voltage for the modulation index $M =$ 0.9 and a pulse ratio w_c/w_o= 51, when the symmetrical and asymmetrical regularly sampled SVM modulation techniques are used. Based on this figure, it is evident that applying the asymmetrical regularly sampled SVM can lead to less output voltage harmonics compared with the symmetrical case.

$$A_{mn} + jB_{mn} = \frac{4V_{dc}}{q\pi} J_n(q\frac{\pi}{2}M)\ \sin([q+n]\frac{\pi}{2}) \tag{4.2}$$

$$\begin{aligned} &A_{mn} + jB_{mn} = \\ &\frac{8V_{dc}}{q\pi^2} \left(\begin{array}{l} \frac{\pi}{6}\sin([q+n]\frac{\pi}{2})(J_n(q\frac{3\pi}{4}M) + 2\cos(n\frac{\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)) \\ +\frac{1}{n}\sin(q\frac{\pi}{2})\cos(n\frac{\pi}{2})\sin(n\frac{\pi}{6})(J_0(q\frac{3\pi}{4}M) - J_0(q\frac{\sqrt{3}\pi}{4}M))\ |n \neq 0 \\ +\sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} [\frac{1}{n+k}\sin([q+k]\frac{\pi}{2})\cos([n+k]\frac{\pi}{2})\sin([n+k]\frac{\pi}{6}) \\ \quad (J_k(q\frac{3\pi}{4}M) + 2\cos([2n+3k]\frac{\pi}{6})J_k(q\frac{\sqrt{3}\pi}{4}M))] \\ +\sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} [\frac{1}{n-k}\sin([q+k]\frac{\pi}{2})\cos([n-k]\frac{\pi}{2})\sin([n-k]\frac{\pi}{6}) \\ \quad (J_k(q\frac{3\pi}{4}M) + 2\cos([2n-3k]\frac{\pi}{6})J_k(q\frac{\sqrt{3}\pi}{4}M))] \end{array} \right) \end{aligned} \tag{4.3}$$



(a) (b)

Figure 4.3: *Theoretical harmonic spectrum of the inverter output voltage with the modulation index $M = 0.9$ and pulse ratio $w_c/w_o = 51$. (a) Harmonic spectrum with symmetrical regularly sampled SVM strategy, (b) harmonic spectrum with asymmetrical regularly sampled SVM strategy.*

$$
\begin{aligned}
&A_{mn} + jB_{mn} = \\
&\frac{2V_{dc}}{q\pi^2}\left(\begin{array}{l}
\frac{4\pi}{3}\cos(n\frac{\pi}{6})\sin([q+n]\frac{\pi}{2})\cos(q\frac{\pi}{2})J_n(q\frac{\sqrt{3}\pi}{2}M) \\
+\frac{1}{n}\sin(q\pi)\sin(n\frac{\pi}{3})(1-J_0(q\frac{\sqrt{3}\pi}{2}M))\,|n\neq 0 \\
+\frac{j}{n}\sin(q\pi)(1-\cos(n\frac{\pi}{3}))(2\cos(2n\frac{\pi}{3})J_0(q\frac{\sqrt{3}\pi}{2}M)+1)\,|n\neq 0 \\
+\sum\limits_{\substack{k=1\\k\neq -n}}^{\infty}[\frac{2}{n+k}J_k(q\frac{\sqrt{3}\pi}{2}M)[\sin([2q+k]\frac{\pi}{2})\cos([4n+5k]\frac{\pi}{6}) \\
+\sin(k\frac{\pi}{2})\cos([2n+k]\frac{\pi}{6})][\sin([n+k]\frac{\pi}{3})+j(1-\cos([n+k]\frac{\pi}{3}))]] \\
+\sum\limits_{\substack{k=1\\k\neq n}}^{\infty}[\frac{2}{n-k}J_k(q\frac{\sqrt{3}\pi}{2}M)[\sin([2q+k]\frac{\pi}{2})\cos([4n-5k]\frac{\pi}{6}) \\
+\sin(k\frac{\pi}{2})\cos([2n-k]\frac{\pi}{6})][\sin([n-k]\frac{\pi}{3})+j(1-\cos([n-k]\frac{\pi}{3}))]]
\end{array}\right)
\end{aligned}
\tag{4.4}
$$

$$
\begin{aligned}
&A_{mn} + jB_{mn} = \\
&\frac{8V_{dc}}{q\pi^2}\left(\begin{array}{l}
\frac{\pi}{6}\sin([m+n]\frac{\pi}{2})(J_n(q\frac{3\pi}{4}M)+2\cos(n\frac{\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)) \\
+\frac{1}{n}\sin(m\frac{\pi}{2})\cos(n\frac{\pi}{2})\sin(n\frac{\pi}{6})(J_0(q\frac{3\pi}{4}M)-J_0(q\frac{\sqrt{3}\pi}{4}M))\,|n\neq 0 \\
+\sum\limits_{\substack{k=1\\k\neq -n}}^{\infty}[\frac{1}{n+k}\sin([m+k]\frac{\pi}{2})\cos([n+k]\frac{\pi}{2})\sin([n+k]\frac{\pi}{6}) \\
\qquad (J_k(q\frac{3\pi}{4}M)+2\cos([2n+3k]\frac{\pi}{6})J_k(q\frac{\sqrt{3}\pi}{4}M))] \\
+\sum\limits_{\substack{k=1\\k\neq n}}^{\infty}[\frac{1}{n-k}\sin([m+k]\frac{\pi}{2})\cos([n-k]\frac{\pi}{2})\sin([n-k]\frac{\pi}{6}) \\
\qquad (J_k(q\frac{3\pi}{4}M)+2\cos([2n-3k]\frac{\pi}{6})J_k(q\frac{\sqrt{3}\pi}{4}M))]
\end{array}\right)
\end{aligned}
\tag{4.5}
$$

By considering a highly inductive load such as the Induction Motor (IM), the inverter three-phase output current i_x $(x = u, v, w)$ can be assumed to be sinusoidal and they are given as

$$i_u(t) = I_o\cos(w_o t + \theta) \tag{4.6}$$

$$i_v(t) = I_o \cos(w_o t + \theta - \frac{2\pi}{3}) \tag{4.7}$$

$$i_w(t) = I_o \cos(w_o t + \theta + \frac{2\pi}{3}) \tag{4.8}$$

where the amplitude of the output currents and the displacement factor are denoted as I_o and θ respectively. Assuming that the inverter operates as a lossless system, with a balanced load condition, the DC-link inverter side current i_{inv} can be evaluated as follows

$$i_{inv}(t) = S_u(t) \cdot i_u(t) + S_v(t) \cdot i_v(t) + S_w(t) \cdot i_w(t) \tag{4.9}$$

where the inverter switching functions are notated as $S_u(t), S_v(t), S_w(t)$ and can be defined by

$$S_x(t) = \frac{v_x(t)}{V_{dc}}, \qquad x = u,\, v,\, w \tag{4.10}$$

the DC value of the DC-link voltage is represented as V_{dc}. Therefore, the harmonic components of the DC-link inverter side current can be obtained using (4.9) and (4.10).

In order to quantify the DC-link current oscillations inherited from the inverter output side, the closed form solution in (4.1) can be evaluated separately in terms of the baseband harmonic components and the carrier group components. Substituting the baseband harmonic components (first summation in (4.1)) and equations (4.6)–(4.8) into (4.9) and (4.10) will give rise to (4.11), where the associated DC-link oscillations i_{inv-b} are obtained.

$$\begin{aligned} i_{inv-b}(t) = \sum_{n=1}^{\infty} [& \tfrac{A_{0n} I_o}{2V_{dc}} [\cos((n+1)w_o t + \theta) + \cos((n-1)w_o t - \theta) \\ & + \cos((n+1)w_o t + \theta - (n+1)\tfrac{2\pi}{3}) + \cos((n-1)w_o t - \theta - (n-1)\tfrac{2\pi}{3}) \\ & + \cos((n+1)w_o t + \theta + (n+1)\tfrac{2\pi}{3}) + \cos((n-1)w_o t - \theta + (n-1)\tfrac{2\pi}{3})] \\ & + \tfrac{B_{0n} I_o}{2V_{dc}} [\sin((n+1)w_o t + \theta) + \sin((n-1)w_o t - \theta) \\ & + \sin((n+1)w_o t + \theta - (n+1)\tfrac{2\pi}{3}) + \sin((n-1)w_o t - \theta - (n-1)\tfrac{2\pi}{3}) \\ & + \sin((n+1)w_o t + \theta + (n+1)\tfrac{2\pi}{3}) + \sin((n-1)w_o t - \theta + (n-1)\tfrac{2\pi}{3})]] \end{aligned} \tag{4.11}$$

As for the contribution of the carrier group harmonics of the switched output waveform on the DC-link current oscillations, the same evaluation method can be applied. With substitution of the carrier group components (double summation in (4.1)) and (4.6)–(4.8) into (4.9) and (4.10), the corresponding DC-link oscillation i_{inv-c} is calculated as (4.12).

$$
\begin{aligned}
&i_{inv-s}(t) = \\
&\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \tfrac{A_{mn}I_o}{2V_{dc}}[\cos(mw_ct+(n+1)w_ot+\theta)+\cos(mw_ct+(n-1)w_ot-\theta) \\
&\quad +\cos(mw_ct+(n+1)w_ot+\theta-(n+1)\tfrac{2\pi}{3}) \\
&\quad +\cos(mw_ct+(n-1)w_ot-\theta-(n-1)\tfrac{2\pi}{3}) \\
&\quad +\cos(mw_ct+(n+1)w_ot+\theta+(n+1)\tfrac{2\pi}{3}) \\
&\quad +\cos(mw_ct+(n-1)w_ot-\theta+(n-1)\tfrac{2\pi}{3})] \\
&\quad +\tfrac{B_{mn}I_o}{2V_{dc}}[\sin(mw_ct+(n+1)w_ot+\theta)+\sin(mw_ct+(n-1)w_ot-\theta) \\
&\quad +\sin(mw_ct+(n+1)w_ot+\theta-(n+1)\tfrac{2\pi}{3}) \\
&\quad +\sin(mw_ct+(n-1)w_ot-\theta-(n-1)\tfrac{2\pi}{3}) \\
&\quad +\sin(mw_ct+(n+1)w_ot+\theta+(n+1)\tfrac{2\pi}{3}) \\
&\quad +\sin(mw_ct+(n-1)w_ot-\theta+(n-1)\tfrac{2\pi}{3})]
\end{aligned}
\tag{4.12}
$$

The harmonic coefficients A_{mn} and B_{mn} in equations (4.11) and (4.12), which should be evaluated for each modulation strategy, will determine the harmonic components of the DC-link inverter side current. Therefore, these effects are considered individually in the following, for the symmetrical and asymmetrical modulation methods.

4.2.1 Symmetrical regularly sampled strategy

In respect to regularly sampled symmetrical modulation technique, the baseband harmonic coefficients A_{0n} and B_{0n} are potentially existing for all values of n, referring to equation (4.1). However, further inspection of (4.11) shows that only the triple multiples of the output frequency w_o will appear at the DC link under balanced condition. As a result, the effects of the output voltage baseband harmonic components on the DC-link current oscillation $f^h_{dc-b-sym}$ can be obtained as

$$f^h_{dc-b-sym} = 3 \cdot k \cdot f_o\,, \qquad k = 1,\, 2,\, 3,\, ... \tag{4.13}$$

Here, it is worth to note that in equation (4.13), the *odd* triple multiples of the output frequency (i.e., $3f_o$, $9f_o$, ...) are caused by the corresponding *even* order baseband harmonics of the output frequency (i.e., $\{2^{th},\, 4^{th}\}$, $\{8^{th},\, 10^{th}\}$, ...), and, the *even* triple multiples (i.e., $6f_o$, $12f_o$, ...) are generated by the associated *odd* order baseband harmonics of the output frequency (i.e., $\{5^{th},\, 7^{th}\}$, $\{11^{th},\, 13^{th}\}$, ...).

In respect to the contribution of the carrier group harmonics, with further investigation of (4.12), it is found that although the carrier group coefficients A_{mn} and B_{mn} are present for all values of m and n, only the carrier harmonic components and their differences from the triple multiple of the fundamental frequency w_o emerge at the DC-link inverter side current. Thus, the effects of the carrier sideband harmonics on the DC-link oscillation frequencies $f^h_{dc-c-sym}$

can be developed as

$$f^h_{dc-c-sym} = \{(m \cdot f_c)\,,\, (m \cdot f_c \pm 3 \cdot k \cdot f_o)\}\,, \qquad k = 1,\, 2,\, 3,\, ... \tag{4.14}$$

A precise investigation of (4.12) makes it clear that the first carrier sidebands for $n = \pm 1$ produce the carrier frequency oscillations at the DC-link current, given in (4.14). Moreover, the *odd* triplen sidebands of $f^h_{dc-c-sym}$ (i.e., $(m \cdot f_c) - 3f_o$, $(m \cdot f_c) - 9f_o$, ...) are produced by the related *even* order sidebands of the output voltages (with the sets of n as $\{-2, -4\}$, $\{-8, -10\}$, ...), and, the *even* triplen sidebands (i.e., $(m \cdot f_c) - 6f_o$, $(m \cdot f_c) - 12f_o$, ...) are created by the associated *odd* order sideband carriers of the output voltages (with the sets of n as $\{-5, -7\}$, $\{-11, -13\}$, ...).

The general expression of the DC-link inverter side current oscillations, with applying the symmetrical regularly sampled modulation strategy is then established by the combination of (4.13) and (4.14) as follows

$$f^h_{dc-sym} = \{f^h_{dc-b-sym}\,,\, f^h_{dc-c-sym}\} \tag{4.15}$$

4.2.2 Asymmetrical regularly sampled strategy

In the asymmetrical regularly sampled method the baseband harmonic coefficients A_{0n} and B_{0n} are zero for *even* order harmonics (more details about these coefficients can be found using (4.5)). Therefore, the *odd* triple multiples of the output frequency (i.e., $3f_o$, $9f_o$, ...), which were present in the case of symmetrical technique, would be removed by an asymmetrical method implementation. The contribution of the baseband harmonics on the DC-link current oscillation is then expressed as

$$f^h_{dc-b-asym} = 6 \cdot k \cdot f_o\,, \qquad k = 1,\, 2,\, 3,\, ... \tag{4.16}$$

In this condition, like in the symmetrical case, the *even* triple multiples (i.e., $6f_o$, $12f_o$, ...) are made by the corresponding *odd* order baseband harmonics of the output frequency (i.e., $\{5^{th}, 7^{th}\}$, $\{11^{th}, 13^{th}\}$, ...).

As for the effect of the output voltage carrier group harmonics on the DC-link current, with the examination of (4.5) it can be found that the carrier group coefficients A_{mn} and B_{mn} would be zero when $\{(m + n) =$ *even* value$\}$. Afterwards, these coefficients caused by all other combinations of m and n can be evaluated in equation (4.12). Further inspection of (4.12) using the remaining harmonic coefficients would give rise to the DC-link current oscillations with the frequencies of $f^h_{dc-c-asym}$

$$f^h_{dc-c-asym} = \left\{ \begin{array}{l} (m \cdot f_c \pm 3 \cdot k' \cdot f_o), \\ \qquad\qquad \text{for } k' = 1,\, 3,\, 5,\, ... \text{ and } m = \textit{odd} \\ \\ (m \cdot f_c),\, (m \cdot f_c \pm 6 \cdot k' \cdot f_o), \\ \qquad\qquad \text{for } k' = 1,\, 2,\, 3,\, ... \text{ and } m = \textit{even} \end{array} \right\} \tag{4.17}$$

Thereafter, the total harmonic components frequencies of the DC-link current generated by the asymmetrical regularly sampled technique can be evaluated by

$$f^h_{dc-asym} = \{f^h_{dc-b-asym}\,,\, f^h_{dc-c-asym}\} \tag{4.18}$$

4.3 Harmonics transfer at the rectifier level

The DC-link inverter-side current oscillations, after flowing through the DC link stage, will be multiplied by the well-known six-pulse diode rectifier switching functions $\{S_a(t),\, S_b(t),$ and $S_c(t)\}$, defined in (4.19)–(4.21) as

$$\begin{aligned} S_a(t) = 2\sqrt{3}/\pi[&\cos(w_g t) - 1/5\,\cos(5w_g t) \\ &+1/7\,\cos(7w_g t)\, - 1/11\,\cos(11w_g t) + ...] \end{aligned} \tag{4.19}$$

$$S_b(t) = S_a(t - T/3) \tag{4.20}$$

$$S_c(t) = S_a(t + T/3) \tag{4.21}$$

where the grid voltage fundamental period and the angular frequency are notated as T and w_g.

The rectifier switching functions given in (4.19)–(4.21) when multiplied by the DC-link current oscillations inherited from the inverter switching operation, will give rise to ASD input current interharmonic components, and can be written as (4.22) and (4.23) for the symmetrical and the asymmetrical strategies, respectively.

$$f^h_{ih-sym} = \left|[6\,\cdot\,(v-1)\,\pm\,1]\,\cdot\,f_g\,\pm\,f^h_{dc-sym}\right|, \quad v = 1,\,2,\,3,\,... \tag{4.22}$$

$$f^h_{ih-asym} = \left|[6\,\cdot\,(v-1)\,\pm\,1]\,\cdot\,f_g\,\pm\,f^h_{dc-asym}\right|, \quad v = 1,\,2,\,3,\,... \tag{4.23}$$

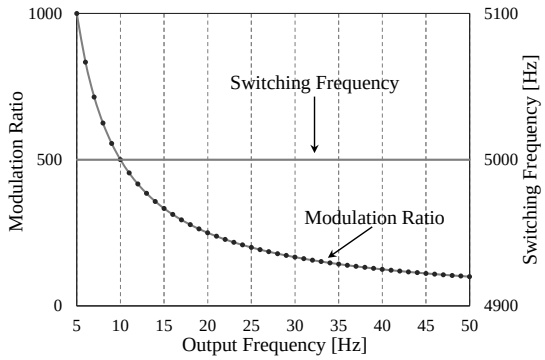


Figure 4.4: *The inverter switching frequency and the corresponding modulation ratio at different output frequency f_o variation ranges.*

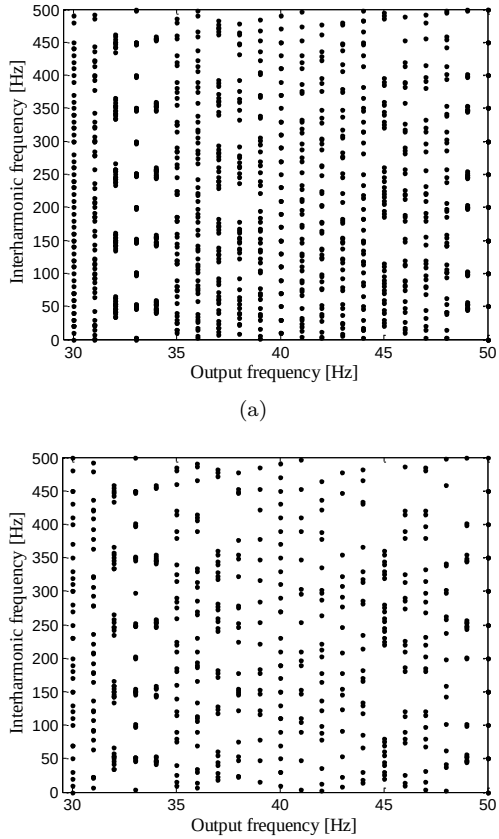


Figure 4.5: *ASD input current i_a interharmonics frequency location with respect to output frequency f_o variations, (a) By applying the symmetrical modulation method using (4.22). (b) By applying the asymmetrical modulation method using (4.23).*

with f_g stated as the input voltage fundamental frequency.

Figure 4.4 shows the selected modulation strategy at the inverter, where the switching frequency is considered as a constant value of 5 kHz during the output frequency f_o variations from 5–50 Hz. For the sake of clarification, the drive input current interharmonic locations, obtained using (4.22) and (4.23), are plotted in Figure 4.5(a) and (b), only for the output frequency f_o range of 30–50 Hz. It should be noted that, for plotting Figure 4.5(a) and (b), the interactions between the significant AC side harmonics ($1^{st}, 5^{th}, 7^{th}$ and 11^{th}), and the DC-link harmonic currents below 400 Hz caused by the inverter operation have been considered.

As it can be seen in Figure 4.5(a) and (b), the drive input current inter-

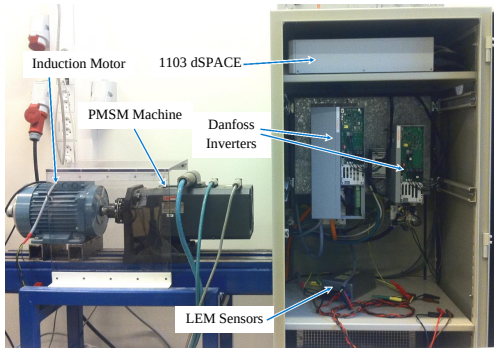


Figure 4.6: *Laboratory setup for experimental verification.*

Table 4.1: *Simulation and Experimental Parameter Values.*

Symbol	Parameter	Value
$v_{a,b,c}$	Grid phase voltage	225 V_{rms}
f_{in}	Grid frequency	50 Hz
L_{dc}, R_{dc}	DC link inductor & resistor	8 mH, 360 mΩ
C_{dc}, R_c	DC Link Capacitor & Resistor	125 μF & 500 mΩ
f_c	Inverter switching frequency	5 kHz
v_{LL}	Induction motor rated voltage	380 V_{rms}
P_{IM}	Induction motor rated power	2.2 kW

harmonics change their locations with respect to output frequency variations. Most interharmonic overlaps occur at the output frequencies of 33 and 50 Hz, where the interharmonics accommodate at the input side harmonic frequencies and are very close to them. Moreover, it can be observed that based on the theoretical investigation, applying the asymmetrical modulation strategy may result in less interharmonic components compared with the symmetrical one.

4.4 Hardware setup and practical implementation

4.4.1 Hardware setup

In order to validate the accuracy of the developed calculations, an experimental setup was used based on the drive system shown in Figure 4.1. The system parameter values used for MATLAB simulation and experimental work are listed in Table 4.1. Figure 4.6 shows the employed experimental setup. The induction motor is controlled with a constant Voltage-to-Frequency (V/F) strategy using a 2.5 kW Danfoss inverter, and the load torque is implemented by controlling a Permanent Magnet Synchronous Machine (PMSM) coupled with the induction motor via a 10 kW Danfoss inverter. The control algorithm was executed on a

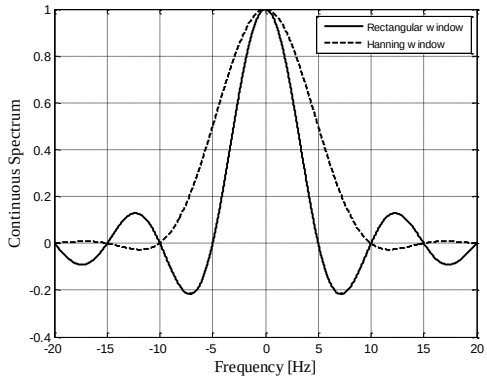


Figure 4.7: *Continuous spectrum of Rectangular Window (RW) and Hanning Window (HW).*

dSPACE1103 real-time platform. Moreover, a California MX30 grid simulator has been used to remove the potential grid background distortion.

4.4.2 Measurement

It is worthwhile to mention that, the interharmonics detection and measurements usually suffer from the spectral leakage phenomenon and the picket fence effect. In this respect, it is always difficult to measure and analyze the signal interharmonic components with acceptable levels of accuracy.

The spectral leakage can usually occur in power system waveform analysis, mainly due to the error in synchronizing the fundamental frequency and harmonics, and also, due to the picket fence effect normally seen for measurement of those interharmonics non-synchronized with DFT bins. In this condition, applying the Rectangular Window (RW) for the harmonic and interharmonic identification may result in an inaccurate measurement [50]. This inaccuracy is mainly induced due to the rectangular window characterization in the frequency domain, with the narrowest main lobe but the highest and slowly decaying side lobs.

In order to reduce the leakage problem during the interharmonics identification, several windowing techniques with quickly decaying side lobes can be implemented. Meanwhile, applying Hanning window is recognized as one of the most suitable choices for the harmonic and interharmonic detections, because of a better side-lobe behavior compared to that of RW [69]. The spectral characteristics of the Rectangular and Hanning windows, which already have been discussed in Chapter 3 are shown in Figure 4.7 for a 5-Hz frequency resolution. In the investigations during the experimental measurement, a high accuracy DFT (with a 3-second Hanning window) [50] has been implemented for the interharmonics detection. With this choice of windowing, an approximately 0.33 Hz frequency resolution has been obtained, and the leakage problem was

minimized.

4.5 Simulation and laboratory test results

The calculation presented in previous section was a general evaluation of the drive input-side current interharmonics with respect to output frequency variations when the symmetrical and/or asymmetrical regularly sampled modulation strategies are selected. These strategies are normally implemented in fixed-frequency modulation techniques. To validate the accuracy of the theoretical analysis, a set of simulation and experimental tests were considered based on the adjustable speed drive system shown in Figure 4.1. In this investigation, the most common modulation techniques in ASDs (i.e., the symmetrical regularly sampled SPWM, SVM, and DPWM2, and also the asymmetrical regularly sampled SVM) have been evaluated in terms of the drive input current interharmonics.

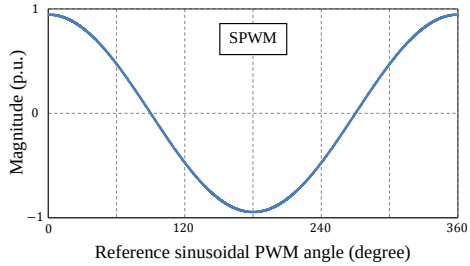
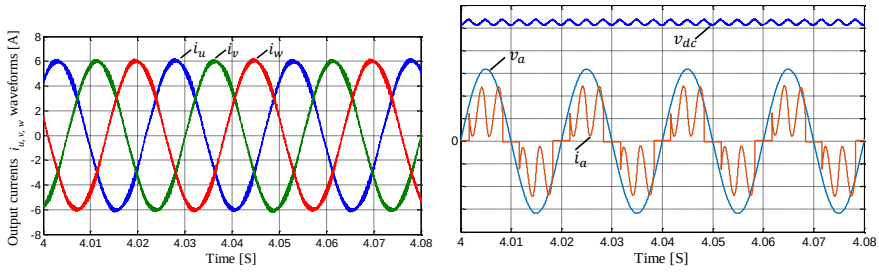


Figure 4.8: *Phase-u reference waveform for SPWM scheme with modulation index M=0.945.*



(a) (b)

Figure 4.9: *(a) The simulated three-phase motor currents $i_{u,v,w}$ waveforms, (b) The simulated input current i_a (2.5 A/div), input phase voltage v_a (100 V/div), and DC-link voltage v_{dc} (100 V/div) waveforms, when the induction motor is operating at the output frequency f_o= 40 Hz and a load torque value of 12 Nm.*

4.5.1 Symmetrical regularly sampled SPWM modulation technique

The sinusoidal pulse width modulation technique is considered as the most common PWM technique for high power ASDs, with low switching frequency. However, its implementation can not optimally benefit from the DC-link voltage to make the inverter output voltages. In this study, in order to have a comparison among the SPWM technique and two other techniques (SVM and

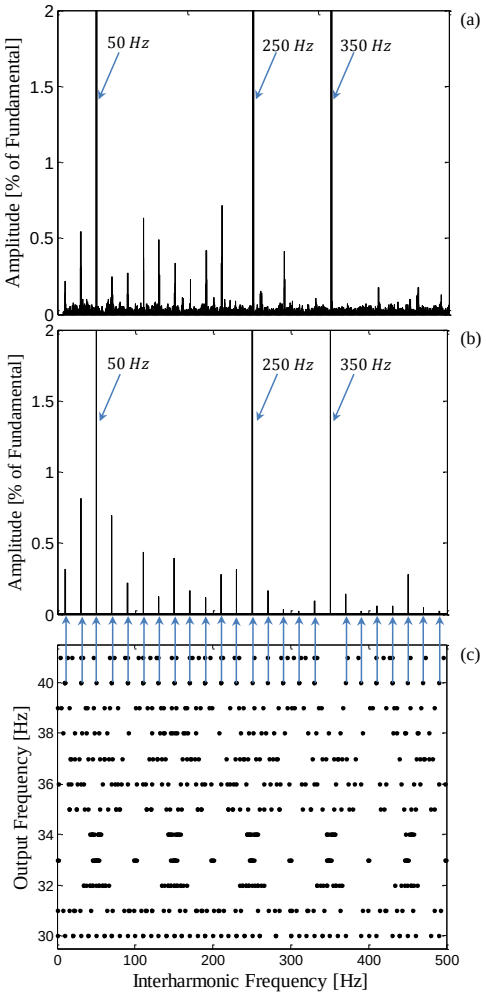


Figure 4.10: *Drive input current i_a interharmonics at the output frequency f_o= 40 Hz and load torque of 12 Nm by applying SPWM technique: (a) Experimental results, (b) Simulation results, and (c) Output frequency versus interharmonic frequencies.*

DPWM2), the inverter modulation index M in the SPWM case is set to be 1.15 times more than that of SVM and DPWM2 cases. Figure 4.8 shows the phase-u reference waveform for sine-triangle PWM implementation.

Figure 4.9(a) and (b) show the simulated ASD output currents, the input current and voltage, and DC-link voltage waveforms, when a SPWM modulation technique has been used for the inverter operation. The induction motor is also set to run at the output frequency f_o of 40 Hz with a load torque value of 12 Nm. Regarding the selected (V/F) control strategy and the investigated system parameters as in Table 4.1, the modulation index will be close to 0.945 at the output frequency of 40 Hz.

The associated input current interharmonic locations can be observed in Figure 4.10, as well as the well-known characteristic harmonics. The interharmonics frequency mapping, already shown in Figure 4.5(a), has been rescaled in Figure 4.10(c) for further clarification. An intersection between a horizontal line at the output frequency f_o of 40 Hz with the plotted black points in Figure 4.10(c) results in the corresponding drive input current interharmonic frequencies. As it can be observed, the interharmonics locations obtained using the theoretical analysis in (4.22) are in good agreement with the MATLAB simulation and experimental results, illustrated in Figure 4.10(a) and (b).

4.5.2 Symmetrical regularly sampled SVM modulation technique

The space vector modulation technique is a more advanced, computation-intensive and arguably the best among all PWM strategies for adjustable speed drive applications, where the load neutral point is normally isolated. This method considers the interaction of the inverter output phases and optimizes the harmonic content of the three-phase induction motor. In this respect, the ASDs interharmonic components, when a SVM modulation technique is implemented on the inverter, can be subjected to further investigations. The phase-u reference waveform for applying the space vector modulation is drawn in Figure 4.11. The reference waveform modulation index M in this condition

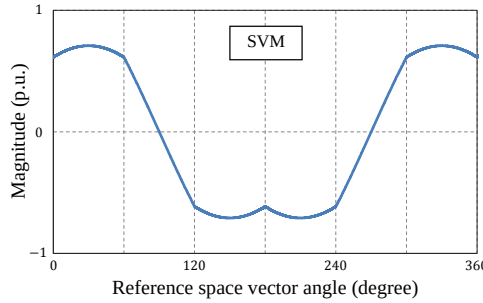


Figure 4.11: *Phase-u reference waveform for SVM scheme with modulation index M=0.818.*

will be close to 0.818, when the motor is operating at the output frequency of 40 Hz. The input current i_a interharmonic components obtained using the MATLAB simulation and experimental results are shown in Figure 4.12. The simulation and experimental results illustrated in Figure 4.12(a) and (b) show the accuracy of the frequency locations as shown in Figure 4.12(c). It can also be observed that the interharmonics amplitude in this case is rather the same as those of SPWM technique shown in Figure 4.10. This is mainly due to the

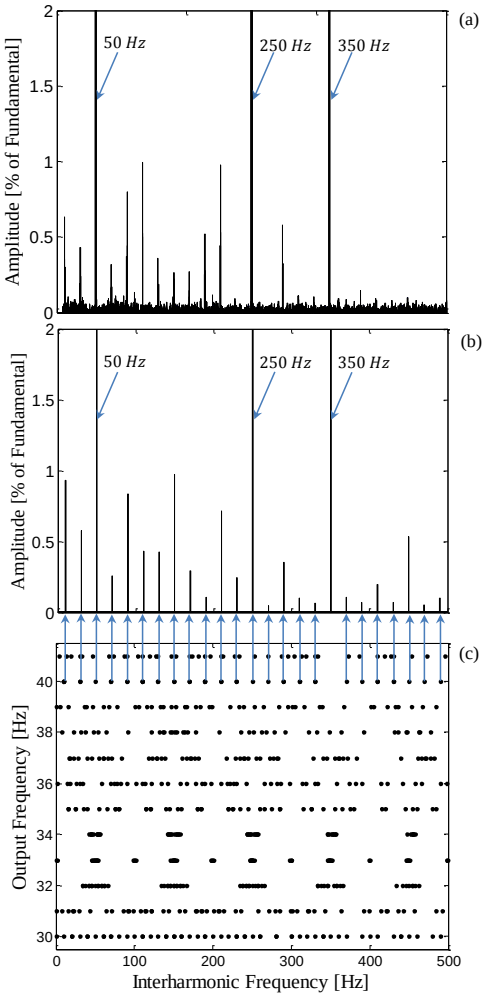


Figure 4.12: *Drive input current i_a interharmonics at the output frequency f_o= 40 Hz and load torque of 12 Nm by applying SVM technique: (a) Experimental results, (b) Simulation results, and (c) Output frequency versus interharmonic frequencies.*

applied high switching frequency (f_{sw} =5 kHz) on the inverter. In this condition, although the carrier sideband harmonics in space vector modulation have smaller decaying rate compared with the SPWM case, their associated effects at low frequency remain rather the same.

4.5.3 Symmetrical regularly sampled DPWM2 modulation technique

The discontinuous pulse width modulation-30 degree lagging clamp (DPWM2) scheme, clamps the inverter pole terminals to the positive and negative terminals of the DC link for a 60° interval each in a fundamental period, as shown in Figure 4.13. Since it usually is preferred to avoid the switching when the current through the devices is near its peak value, applying the DPWM2 technique can be found suitable for the applications where the power factor pf is close to 0.866 lag, such as the motor drive application.

Figure 4.14 shows the adjustable speed drive input current i_a interharmonics when the motor is operating at the output frequency f_o of 40 Hz and load torque value of 12 Nm, and, a DPWM2 modulation technique is selected for the inverter operation. Like the SVM modulation technique, the reference waveform modulation index M for the inverter operation is close to 0.818 to provide the desired output voltage fundamental frequency based on the selected (V/F) control strategy. As it can be seen in Figure 4.14, there is a good agreement between the simulation and experimental results, and the plotted interharmonic frequencies. It is worth to note that the presence of two distinctive interharmonic components at 70 and 170 Hz is due to higher amplitude of the DC-link third harmonic (of the output frequency) oscillation. As already discussed in Section 4.2, the DC-link third harmonic (of the output frequency) oscillation is basically generated by the second and the fourth order frequency of the output voltages.

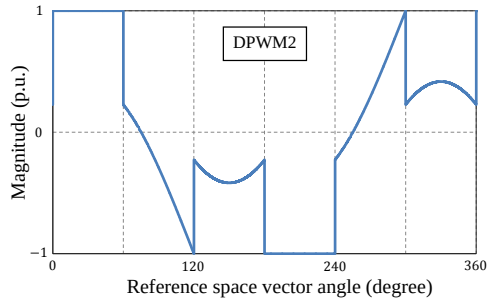


Figure 4.13: *Phase-u reference waveform for DPWM2 scheme with modulation index M=0.818.*

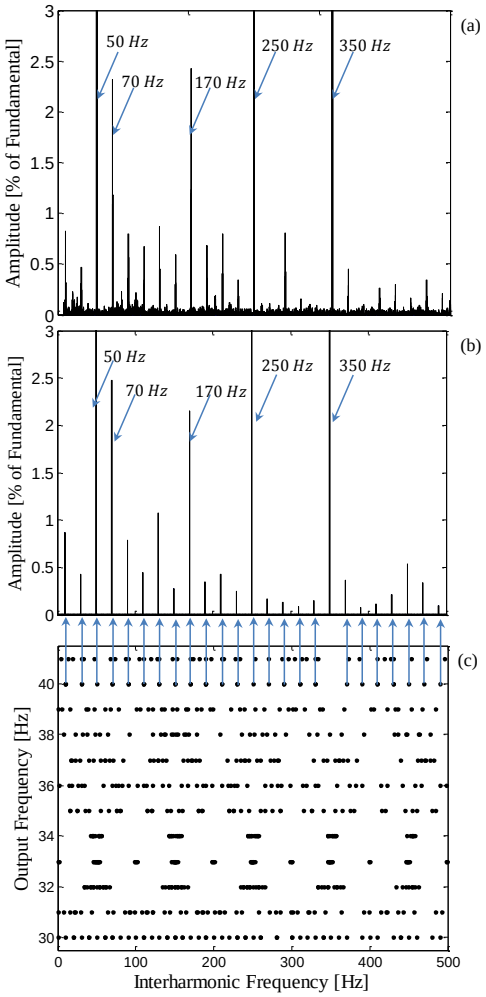


Figure 4.14: *Drive input current i_a interharmonics at the output frequency f_o= 40 Hz and load torque of 12 Nm by applying DPWM2 technique: (a) Experimental results, (b) Simulation results, and (c) Output frequency versus interharmonic frequencies.*

4.5.4 Asymmetrical regularly sampled SVM modulation technique

The accuracy of the theoretical analysis was also subjected to further examination in the case of applying the asymmetrical regularly sampled strategy on the inverter. Figure 4.15 shows the frequency evaluation of the drive input current when an asymmetrical modulation method is implemented on the drive. Like in the previous cases, the investigation is performed at the output frequency f_o of 40 Hz and the load torque value of 12 Nm.

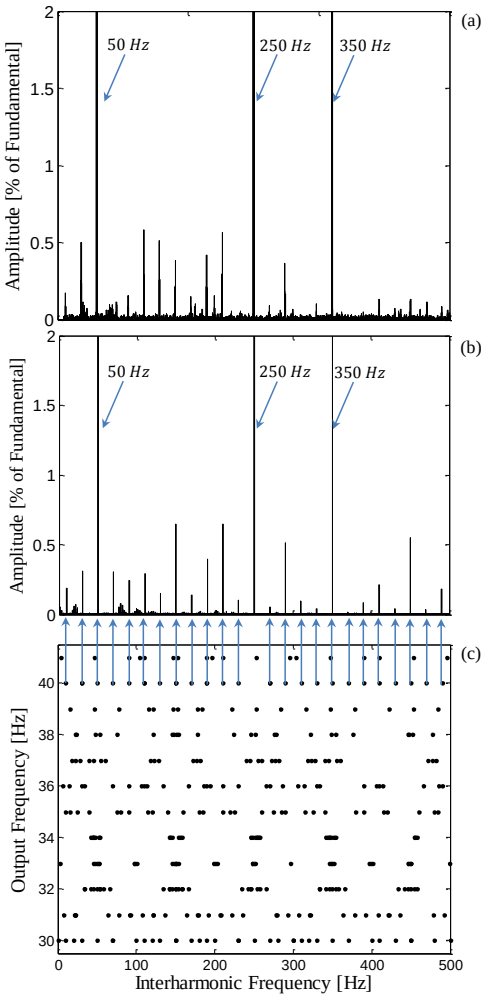


Figure 4.15: *Drive input current i_a interharmonics at the output frequency f_o= 40 Hz and load torque of 12 Nm by applying an asymmetrical regularly sampled SVM modulation technique: (a) Experimental result, (b) Simulation result, and (c) Output frequency versus interharmonic frequencies.*

The associated theoretical frequency locations are drawn in Figure 4.15(c). The frequency spectrum of the simulated drive input current is depicted in Figure 4.15(b), where the interharmonic components are well accommodated at the expected locations. The experimental result shown in Figure 4.15(a) verifies the validity of the theoretical calculations and the simulation results. It is worthwhile to mention that the asymmetrical modulation method usually leads to less harmonic distortion at the output side of the rear-end inverter compared

with the symmetrical modulation technique. In this respect, by implementing the asymmetrical strategy, less harmonics would be transferred from the output side to the DC link, and consequently, less interharmonic overlaps may occur at the input side of the ASD compared with the symmetrical one. As a result, different scenario may happen by implementing these two techniques in respect to the interharmonic amplitudes.

Based on the Figures 4.10–4.15, it can be observed that there are some deviations between the simulation and the experimental results with respect to the interharmonic amplitudes. In the simulation model, switching transient and protect algorithm effects such as blanking time have not been considered. These issues can influence the current and the voltage waveforms and consequently the overall error between the simulation and the test results.

4.6 Conclusion

In this chapter, the adjustable speed drive input current interharmonics generated by double-edge symmetrical and asymmetrical regularly sampled modulation strategies have comprehensively been analyzed. The investigation has been operated at different fixed-frequency pulse width modulation techniques (i.e., the symmetrical regularly sampled SPWM, SVM, and DPWM2, and also the asymmetrical regularly sampled SVM modulation techniques). The harmonics transfer from the output side of the rear-end inverter to the input side of the front-end diode rectifier, which causes the interharmonics distortion, has been analyzed with respect to the baseband harmonics and the carrier sideband harmonics, separately. Then, the drive input current interharmonic frequencies have been plotted using the proposed analysis. Finally, the results obtained by MATLAB simulation and experimental tests demonstrate accuracy of the analytical calculations. The investigation provides a benchmark for estimating the ASD input current interharmonic frequencies, which helps to choose the correct frequency resolution for the DFT spectrum analysis.

Generally, addressing the drive input current interharmonics amplitude is a complicated issue, which needs a very precise model of interharmonics interactions, when the ASD is working at different operating conditions. This issue will be more sophisticated knowing that the interharmonics may usually have some overlaps at specific frequencies. In overlap condition they could easily cancel or intensify each others. Our investigations show that applying the DPWM2 modulation technique may give rise to higher interharmonic amplitudes compared with the SPWM and SVM modulation techniques, when the ASD is operating at high switching frequency. Moreover, the investigations in the drive input current interharmonics show that with applying the asymmetrical modulation technique, less overlaps of interharmonics will occur compared with the symmetrical one. As a result, selecting an asymmetrical method may give rise to interharmonics with lower amplitude.

Chapter 5

ASD's Passive Components Effects on Input Current Interharmonics

As mentioned in the previous chapters, current and voltage sourced adjustable speed drives exert distortion current into the grid, which may produce some interharmonic components other than the characteristic harmonic components normally studied. This chapter studies the effects of passive components on the input current interharmonics of adjustable speed drives with and/or without motor current imbalance during operation. The investigations are done at different motor operating frequencies and load torque values. It shows that selecting small filter components (AC choke, DC choke and DC-link capacitor) results in different performances in respect to those interharmonics generated by the motor current imbalance and other non-characteristic interharmonics.

5.1 Introduction

Double-stage variable speed drives are presently among the main sources of interharmonics injected into the grid in addition to typical harmonics [75–82], where a variable speed motor is fed through an AC/DC/AC drive with a diode-bridge rectifier and a PWM inverter connected back-to-back sharing a common DC link.

If the DC link is not well buffered via a sufficiently large capacitor or inductor, the inverter output current frequency components will pass through the DC link and the rectifier and will then interact with the input current frequency components and consequently give rise to unsteady current distortions. Increasing the DC-link capacitor or the inductor may be an attractive solution, but it has its own limitations such as higher cost and volume and maybe even a shorter compromised lifetime of the converters. In addition, ad-

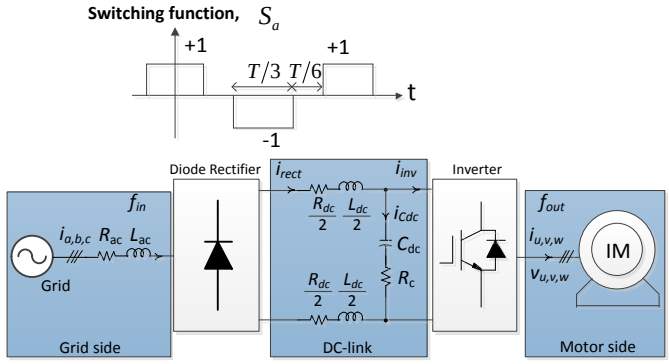


Figure 5.1: *Equivalent circuit of an adjustable-speed drive for system analysis with an induction motor (IM).*

vanced achievements in the design of the capacitors with longer lifetime and a higher voltage fluctuation tolerance have made them promising to be used in the power converter applications.

Besides many investigations done in the literature related to the interharmonic sources and identification methods, with a global trend towards using smaller passive filters (AC choke, DC choke and DC-link capacitor) for ASD, it is needed to consider the effects of these passive components on the interharmonic issues. Although, the authors in [13] discussed the relative effects of DC-link inductance and source inductance on interharmonic propagation, there is still a especial need to consider the direct effects of the filter components on the input current interharmonics at different working points of the ASD. This chapter first investigates the disturbance (initiated by motor unbalanced currents) propagation from the inverter output side to the rectifier input side of ASD. Then the effects of ASD passive filter components on the grid-side current interharmonics will be analyzed in five different cases, when the motor currents are unbalanced. Finally, the filter effects on the input current total interharmonic distortions, in the case of balanced load, at different motor operating frequencies and load torques are investigated.

5.2 Unbalanced load conditions

5.2.1 Interharmonics initiated by load current imbalance

Figure 5.1 shows a schematic diagram of the VSI-fed adjustable speed drive for analyzing the input current interharmonic components. The SVM method is chosen for the modulation because of its superior performance characteristics especially in adjustable speed drive applications. In this case, the existence of a current distortion at the inverter output gives rise to the grid-side current interharmonics. Scaling and offset errors in the drive's current transducers,

unbalanced loads and also overmodulation operating mode of the inverters are typically main sources of the inverter output current imbalance. The following analysis explains how the inverter current distortions may lead to the input current interharmonic components.

According to the symmetrical component theory, the three-phase unbalanced motor currents $\{i_u,\ i_v,\ i_w\}$ can be separated into three sets of balanced and uncoupled components: the positive-sequence current components ($\{i_u^p,\ i_v^p,\ i_w^p\}$ with magnitude I_{out}^p frequency w_{out} and phase θ_{out}^p) and the negative-sequence components ($\{i_u^n,\ i_v^n,\ i_w^n\}$ with magnitude I_{out}^n frequency w_{out} and phase θ_{out}^n),which can be written as,

$$i_u = i_u^p + i_u^n = I_{out}^p \sin(w_{out}t + \theta_{out}^p) + I_{out}^n \sin(w_{out}t + \theta_{out}^n) \tag{5.1}$$

$$i_v = i_v^p + i_v^n = I_{out}^p \sin(w_{out}t + \theta_{out}^p - \tfrac{2\pi}{3}) + I_{out}^n \sin(w_{out}t + \theta_{out}^n + \tfrac{2\pi}{3}) \tag{5.2}$$

$$i_w = i_w^p + i_w^n = I_{out}^p \sin(w_{out}t + \theta_{out}^p + \tfrac{2\pi}{3}) + I_{out}^n \sin(w_{out}t + \theta_{out}^n - \tfrac{2\pi}{3}) \tag{5.3}$$

The inverter-side DC-bus average current can be obtained by the sum of the inverter-side DC-link current i_{inv} over one output fundamental period. Figure 5.2 shows the three-phase output reference signals $\{v_u, v_v, v_w\}$ and the related six intervals used in space vector modulation. The PWM signals and the corresponding inverter-side DC-link current over one switching period T_s in interval A are also illustrated in Figure 5.3, where S_1, S_3 and S_5 are the gating signals of the inverter upper switches associated with the three-phase output reference signals v_u, v_v and v_w respectively. Based on Figure 5.3 and the three-phase unbalanced motor currents represented above, the average DC-link current $I_{inv,A}$ over one switching period in interval A can simply be obtained as

$$\begin{aligned} I_{inv,A} &= \tfrac{1}{T_s}\int_0^{T_s} i_{inv}dt = \tfrac{2T_1}{T_s} i_u + \tfrac{2T_2}{T_s}(i_u + i_w) \\ &= \tfrac{3}{4} m I_{out}^p \cos(\theta_{out}^p) - \tfrac{3}{4} m I_{out}^n \cos(2w_{out}t + \theta_{out}^n) \end{aligned} \tag{5.4}$$

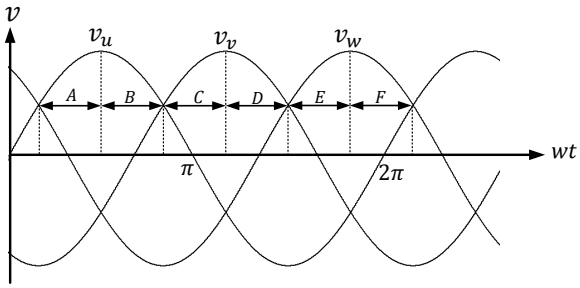


Figure 5.2: *Three-phase output reference signals divided into six intervals (A → F).*

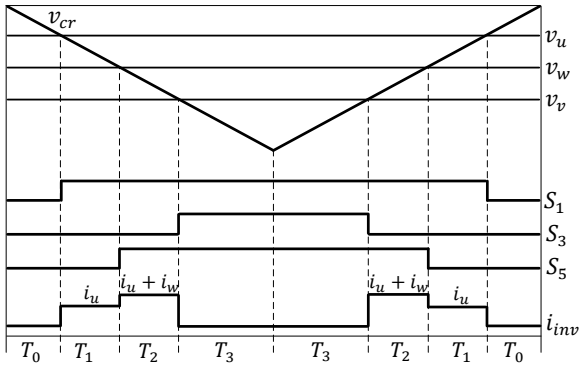


Figure 5.3: *PWM and DC-link inverter-side current waveforms in interval A.*

where m is the modulation index and T_1 and T_2 are the time durations specified in Figure 5.3 and they can be calculated as

$$T_1 = \frac{mT_s}{4}(\sin(w_{out}t) - \sin(w_{out}t + \tfrac{2\pi}{3})) \tag{5.5}$$

$$T_2 = \frac{mT_s}{4}(\sin(w_{out}t + \tfrac{2\pi}{3}) - \sin(w_{out}t - \tfrac{2\pi}{3})) \tag{5.6}$$

Using the same calculations, the inverter-side DC-bus average current in the other five intervals will be similar as in (5.4), which finally results in the inverter-side DC-link average current I_{inv} for one fundamental cycle of the inverter output current to be

$$\begin{aligned} I_{inv} &= I_{dc} - i_{\sim inv} = I_{dc} + I_{\sim inv}\cos(2w_{out}t + \theta_{inv}) \\ &= \tfrac{3}{4}mI^p_{out}\cos(\theta^p_{out}) - \tfrac{3}{4}mI^n_{out}\cos(2\omega_{out}t + \theta^n_{out}) \end{aligned} \tag{5.7}$$

where I_{dc} and $i_{\sim inv}$ are the desired DC current and the oscillation components of the inverter-side DC-bus current respectively. From (5.7) it can be seen that the output current unbalance causes a harmonic component, which is twice the output frequency in addition to the DC quantity. The DC component in (5.7) is associated with the fundamental positive-sequence current and the AC component is related to the presence of the motor current imbalance. According to the circuit law, the inverter-side DC-bus current is divided as $i_{inv} = i_{rect} - i_{Cdc}$, where i_{rect} and i_{Cdc} are the DC currents flowing out of the rectifier DC terminals and through the DC-link capacitor. Therefore the rectifier-side DC-bus average current I_{rect} will have oscillations at twice the inverter output operating frequency and it can be expressed as (5.8)

$$I_{rect} = I_{dc} + I_{\sim rect}\cos(2w_{out}t + \theta_{rect}) \tag{5.8}$$

The second term in (5.8) is a ripple component with magnitude, frequency and phase notated as $I_{\sim rect}$, $2w_{out}$ and θ_{rect}.

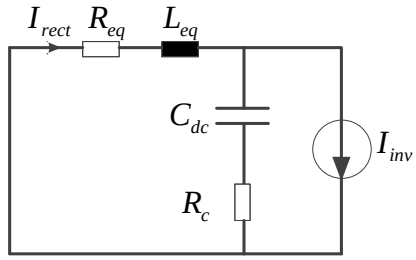


Figure 5.4: *DC-link equivalent circuit for motor drive.*

Table 5.1: *Parameter values for simulation study of interharmonics in ASD.*

Parameter	Case 1	Case 2	Case 3	Case 4	Case 5
Rated Input Power	2.2 kW	2.2 kW	2.2 kW	2.2 kW	2.2 kW
Rated Input Voltage	400 V	400 V	400 V	400 V	400 V
Inverter Carrier Frequency	5 kHz	5 kHz	5 kHz	5 kHz	5 kHz
DC-link Capacitor, C_{dc}	125 μF	125 μF	125 μF	15 μF	15 μF
Resistor, R_c	500 mΩ	500 mΩ	500 mΩ	100 mΩ	100 mΩ
DC-link Inductor, L_{dc}	$--$	8 mH	2 mH	$--$	900 μH
DC-link Resistor, R_{dc}	$--$	360 mΩ	90 mΩ	$--$	40 mΩ
Input Inductor, L_{ac}	6 mH	$--$	4.5 mH	900 μH	$--$
Input Resistor, R_{ac}	270 mΩ	$--$	200 mΩ	40 mΩ	$--$
Motor Nominal Input Voltage	380 V	380 V	380 V	380 V	380 V

The DC-link equivalent circuit depicted in Figure 5.4 represents the current transfer from the inverter DC side to the rectifier DC side. Considering a Continuous Conduction Mode (CCM) operation of the front-end diode rectifier, the equivalent DC-link inductance L_{eq} and damping resistance R_{eq} are [15],

$$L_{eq} = L_{dc} + 2L_{ac} \tag{5.9}$$

$$R_{eq} = R_{dc} + 2(R_{ac} + r_d) + \frac{3}{\pi} w_{in} L_{ac} \tag{5.10}$$

where the last term in (5.10) accounts for the voltage drop caused by diode commutations, w_{in} is the grid voltage angular frequency and r_d denotes the diode dynamic resistance.

In order to assess the effects of passive components on the DC-link disturbance current excitations, five different cases (Cases 1–5) whose parameter values are listed in Table 5.1 are taken into account in this study. The DC-link Resonance Factors (RFs), defined in (5.11), are drawn in Figure 5.5 for the cases considered,

$$RF = \frac{I_{\sim rect}}{I_{\sim inv}} = \frac{Z_C}{Z_C + Z_L} \tag{5.11}$$

Based on Figure 5.5, from one point of view, there is almost no DC-link

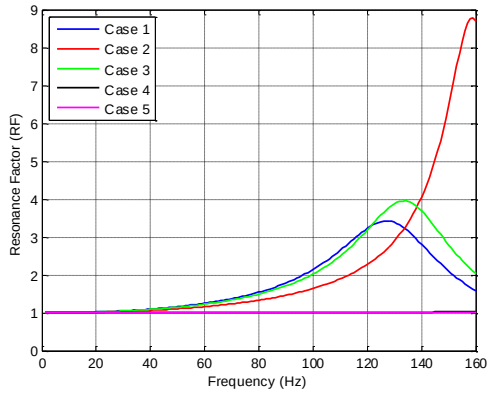


Figure 5.5: *DC-link RFs associated with Cases 1–5.*

resonance excitation associated with the last two cases in which the drive filter components (AC choke, DC choke and DC-link capacitor) values are much smaller than those of the first three cases, within the motor frequency ranges (0–50 Hz). Obviously, the higher resonance frequencies (∼970 and 1370 Hz for Cases 4 and 5, respectively) associated with the last two cases may excite the dormant current oscillations located at those regions. From another point of view, adopting larger values of the filter components may not necessarily lead to lower current oscillations transferred from the inverter DC side to the rectifier DC side. Actually, by selecting a larger DC-link filter, the corresponding DC-link resonance frequency will decrease and consequently it may worsen the current oscillations located at lower frequencies. Thus, depending on the motor operating conditions, the drive filter design needs specific attention concerning the DC-link disturbance excitations.

After leaking through the DC-link stage, the second order oscillation of the rectifier-side DC-link current will be multiplied by the rectifier switching functions $\{S_a, S_b, S_c\}$. Using Fourier series analysis, the rectifier switching functions observed in Figure 5.1 can be obtained as follows,

$$S_a(t) = 2\sqrt{3}/\pi[\cos(w_{in}t) - 1/5\ \cos(5w_{in}t) + 1/7\ \cos(7w_{in}t) - ...] \tag{5.12}$$

$$S_b = S_a\,(t - T/3) \tag{5.13}$$

$$S_c = S_a\,(t + T/3) \tag{5.14}$$

Thereafter, the rectifier switching functions $\{S_a, S_b, S_c\}$, when multiplied with the rectifier-side DC-bus current given in (5.8), give rise to the three-phase input current expressions as shown in (5.15) to (5.17). It is evident that the distortion currents initiated by the motor current imbalance pass through the double-stage ASD and then generate interharmonic currents in the power system. These exclusive interharmonic components are accommodated symmetrically around input side fundamental frequency and the characteristic rectifier

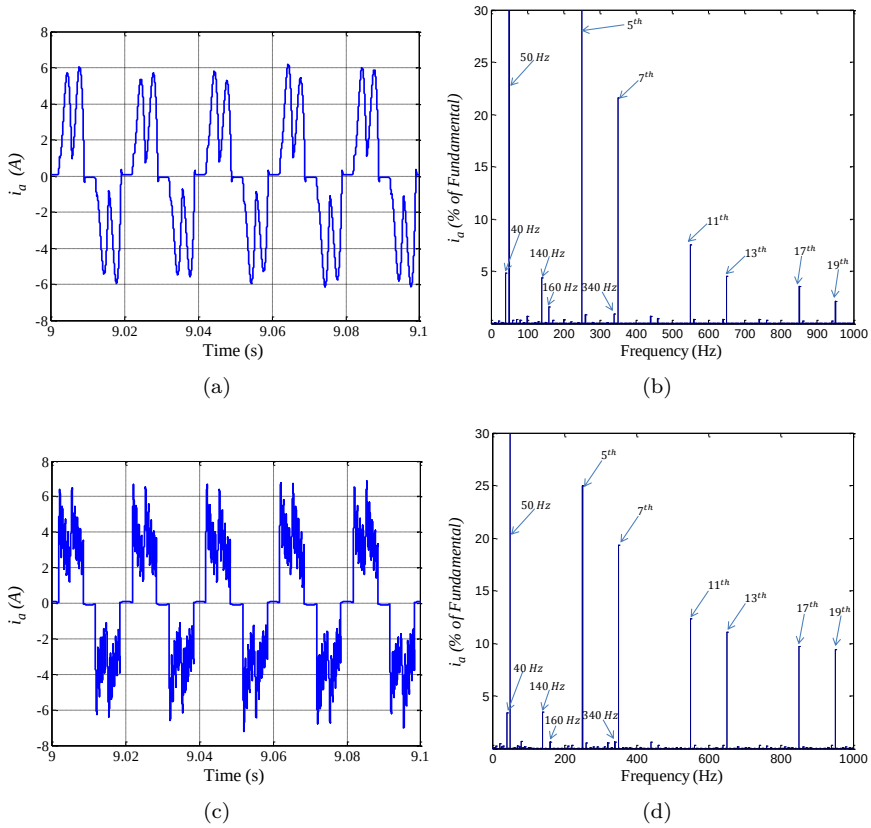


Figure 5.6: *Drive input current i_a waveforms and frequency spectrum at load torque T_L value of 12 Nm, and an output frequency f_{out} of 45 Hz with cases from Table I. (a) Input current waveform in Case 1. (b) Input current spectra in Case 1. (c) Input current waveform in Case 5. (d) Input current spectra in Case 5.*

harmonics. Based on (5.15) to (5.17), although higher order interharmonics may have much lower magnitudes, they are potentially able to excite parallel resonances in the grid.

$$\begin{aligned} i_a = S_a I_{rect} = \left(2\sqrt{3}I_{dc}/\pi\right)\left[\cos(w_{in}t) - 1/5\cos\left(5w_{in}t\right) + 1/7\cos\left(7w_{in}t\right) + \ldots\right] \\ + \left(\sqrt{3}I_{\sim rect}/\pi\right)\left\{\left[\cos((w_{in}+2w_{out})\,t + \theta_{rect}) + \cos((w_{in}-2w_{out})\,t - \theta_{rect})\right]\right. \\ -1/5\left[\cos((5w_{in}+2w_{out})\,t + \theta_{rect}) + \cos((5w_{in}-2w_{out})\,t - \theta_{rect})\right] \\ \left.+1/7\left[\cos((7w_{in}+2w_{out})\,t + \theta_{rect}) + \cos((7w_{in}-2w_{out})\,t - \theta_{rect})\right] + \ldots\right\} \end{aligned} \tag{5.15}$$

$$i_b = i_a\left(t - T/3\right) \tag{5.16}$$

$$i_c = i_a\left(t + T/3\right) \tag{5.17}$$

Figure 5.6 depicts the drive input current waveforms with the corresponding frequency spectra at the load torque T_L value of 12 Nm and the output frequency f_{out} of 45 Hz for Cases 1 and 5, respectively. As it can be seen from Figure 5.6(b) and (d), the input current contains interharmonic components located at the frequencies of $|90 \pm 50|$, $|90 \pm 250|$, and $|90 \pm 350|$ Hz. However, some interharmonic components, other than those generated by the motor current imbalance, can also be recognized in the input current spectra, Figure 5.6(b) and (d).

5.2.2 Effect of passive components

In this section, the effects of adjustable speed drive filters (as defined in Table 5.1) on the input current interharmonic components are studied. A series of simulations has been carried out in MATLAB using the simulation model shown in Figure 5.1. A 2.2 kW induction motor is used with the output frequency range of f_{out}=24–48 Hz, at three different constant load torque values of T_L=12, 9, and 6 Nm. The motor is controlled by using a simple constant voltage-to-frequency method and an inductor of 4 mH was also added to emulate a motor-winding imbalance. As a consequence, a motor current imbalance of about five to six percent was provided at different output speeds at each constant load torque value. Figure 5.7 illustrates the DC-link resonance factor associated with Case 1, at different output frequencies and load torque values. A good agreement between the calculated results (blue solid line) and simulations (green square points) is observed at the load torque value of 12 Nm. The same convergence can also be seen for the load torque value of 9 Nm (blue dots), above the DC-link oscillation frequency of 70 Hz. As it can be seen, a small current disturbance amplification will occur at the DC-link stage, when the load torque is equal to 6 Nm in which the front-end diode rectifier operates almost in the Discontinuous Conduction Mode (DCM). In accordance with (5.15)

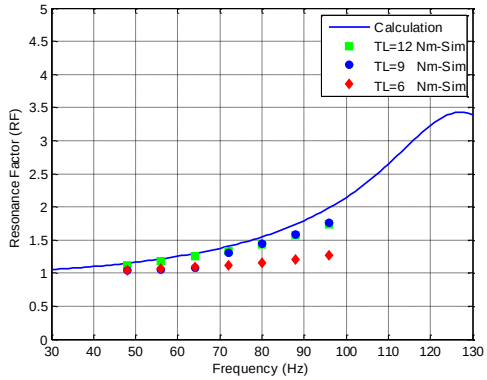


Figure 5.7: *Simulated and calculated DC-link resonance factor associated with Case 1 at different output frequencies and load torque values.*

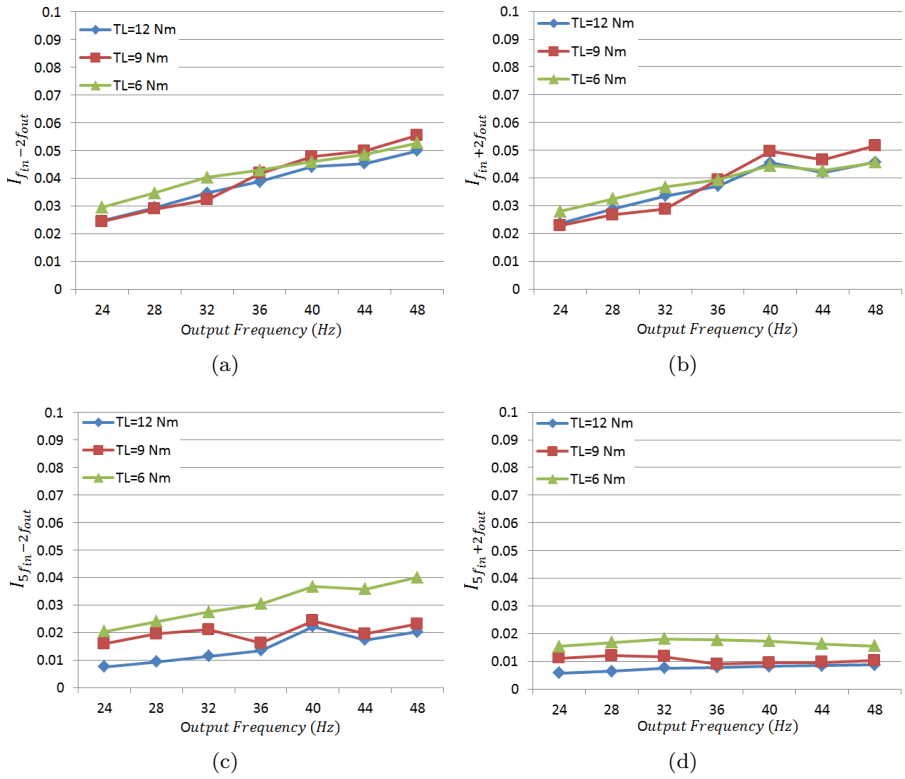


Figure 5.8: *Simulated normalized input current interharmonic components in Case 1 (see Table 5.1) versus output frequencies of the ASD at different load torque T_L values. (a) Interharmonics coupled with and below the fundamental frequency $I_{f_{in}-2f_{out}}$. (b) Interharmonics coupled with and above the fundamental frequency $I_{f_{in}+2f_{out}}$. (c) Interharmonics coupled with and below the fifth-order frequency $I_{5f_{in}-2f_{out}}$. (d) Interharmonics coupled with and above the fifth-order frequency $I_{5f_{in}+2f_{out}}$.*

to (5.17), the grid current interharmonic components initiated by the motor current imbalance mainly appear around the fundamental frequency and its harmonics. Nonetheless, only those interhamonics around the grid current fundamental and fifth order frequencies, which normally have larger amplitudes are plotted in Figure 5.8 for Case 1. It should be noted that all interharmonic values, I_i, illustrated in Figure 5.8 are calculated in accordance with (5.18)

$$I_i = \frac{I_{ipeak}}{I_{fpeak}} \tag{5.18}$$

where I_{ipeak} and I_{fpeak} are the peak values of the related grid current interharmonic and the fundamental frequency respectively. The index i represents

the related interharmonic frequency.

At a constant load torque value, the input current interharmonic components will increase when the motor speed increases, especially for the first sets of interharmonics around the fundamental frequency, as seen in Figure 5.8. Based on Figure 5.8, it can also be seen that the DC-link resonance factors, as already shown in Figure 5.7, are in good harmony with those interharmonic components accommodated around the supply current fundamental frequency ($I_{f_{in}-2f_{out}}$ and $I_{f_{in}+2f_{out}}$ depicted in Figure 5.8(a) and Figure 5.8(b) respectively). However, the interharmonics located around the fifth order harmonic ($I_{5f_{in}-2f_{out}}$ and $I_{5f_{in}+2f_{out}}$ shown in Figure 5.8(c) and Figure 5.8(d)) may not follow the associated DC-link current disturbance amplifications. It is worth to mention that for the interharmonic components surrounding the fifth order harmonic, the lower load torque values are almost associated with a higher relative interharmonic values, as shown in Figure 5.8(c) and Figure 5.8(d).

Figure 5.9 compares the DC-link resonance factor values related to Cases

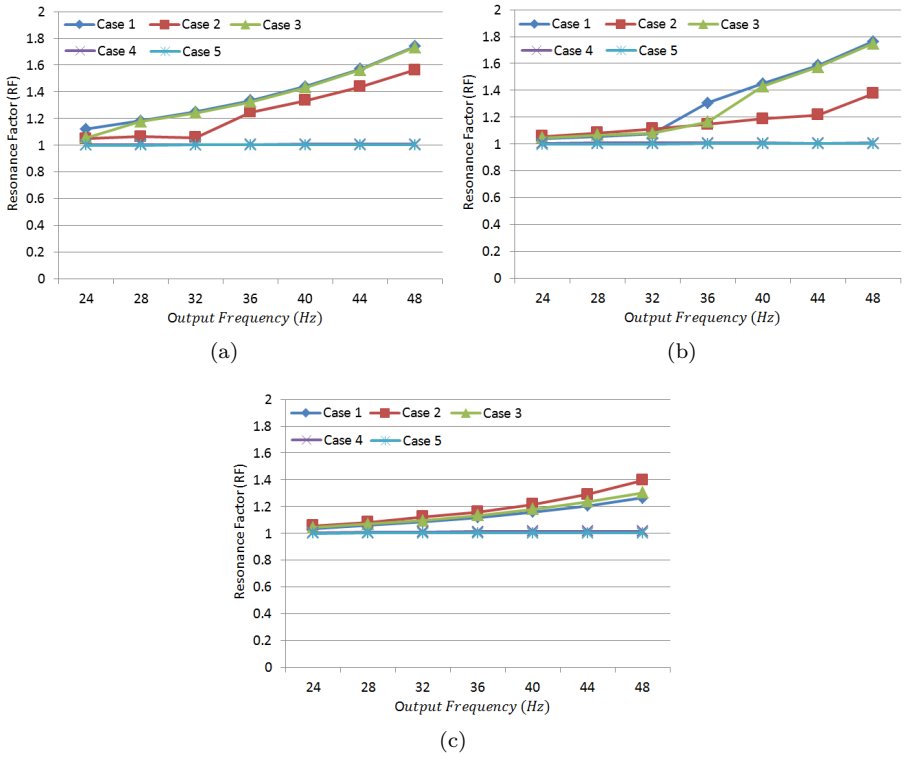


Figure 5.9: *Simulated DC-link resonance factors associated with Cases 1–5 versus different output frequencies of the ASD. (a) load torque equal to 12 Nm. (b) load torque equal to 9 Nm. (c) load torque equal to 6 Nm.*

1–5 at the output frequency range of 24–48 Hz at three constant load torque values (equal to 12 Nm, 9 Nm and 6 Nm). As expected, the last two cases (Cases 4 and 5) show lower DC-link current disturbance amplification from the inverter DC side to the rectifier DC side. Moreover, considering the equal output current imbalance and modulation index for the first three cases, Case 2 shows less harmonic amplification in the DC link, at the load torque value of 12 Nm (which is close to full load operating mode of ASD), as shown in Figure 5.9(a). However, Figure 5.9(c) depicts that for the load torque of 6 Nm (which is close to the half load operating mode of the ASD), the Case 2 is associated with a higher DC-link resonance factor.

A comprehensive comparison of the input current interharmonics related to

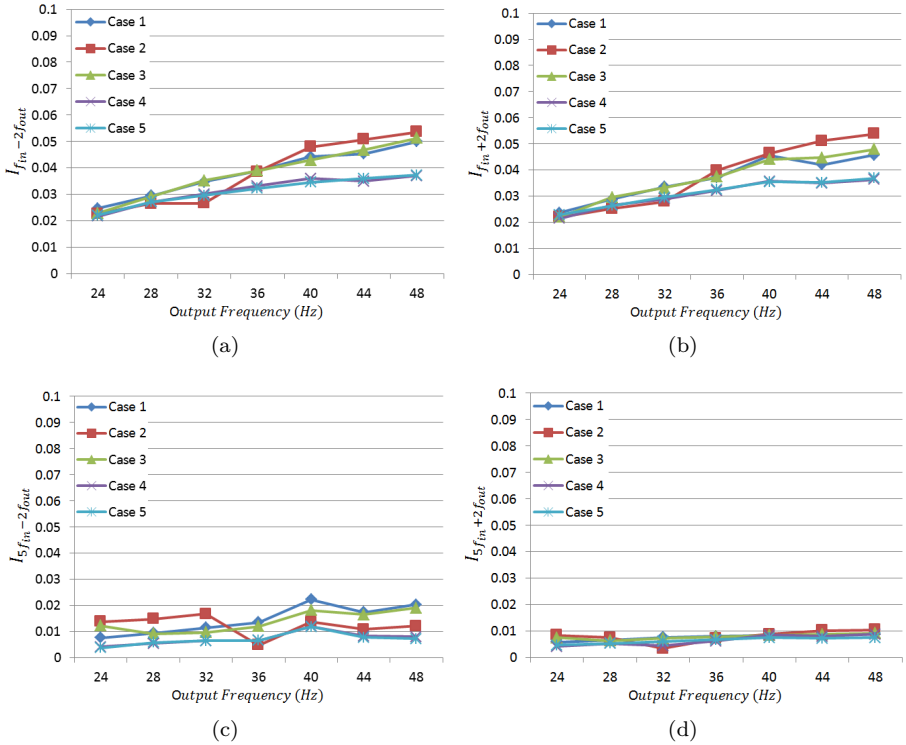


Figure 5.10: *Simulated normalized input current interharmonic components in Cases 1–5 versus output frequencies of the ASD at the load torque T_L equal to 12 Nm. (a) Interharmonics coupled with and below the fundamental frequency $I_{f_{in}-2f_{out}}$. (b) Interharmonics coupled with and above the fundamental frequency $I_{f_{in}+2f_{out}}$. (c) Interharmonics coupled with and below the fifth-order frequency $I_{5f_{in}-2f_{out}}$. (d) Interharmonics coupled with and above the fifth-order frequency $I_{5f_{in}+2f_{out}}$.*

the five investigated cases at the output frequency range of 24–48 Hz and the load torques of 12 and 6 Nm are plotted in Figure 5.10 and Figure 5.11. Based on Figure 5.10(a) and (b), among the first three cases, Case 2 represents smaller interharmonic values at the lower motor output speeds (below 36 Hz) for those interharmonics located around the grid current fundamental frequency. This is while for the higher output speed ranges, these interharmonics take higher values in Case 2. At the load torque equal to 12 Nm, it can also be seen that the last two investigated cases show almost better performance in all operating conditions, as shown in Figure 5.10. At lower load torque value of 6 Nm, Case 2 gives always higher values of the input current interharmonic components, Figure 5.11. In addition, the superior performance of the last two cases with

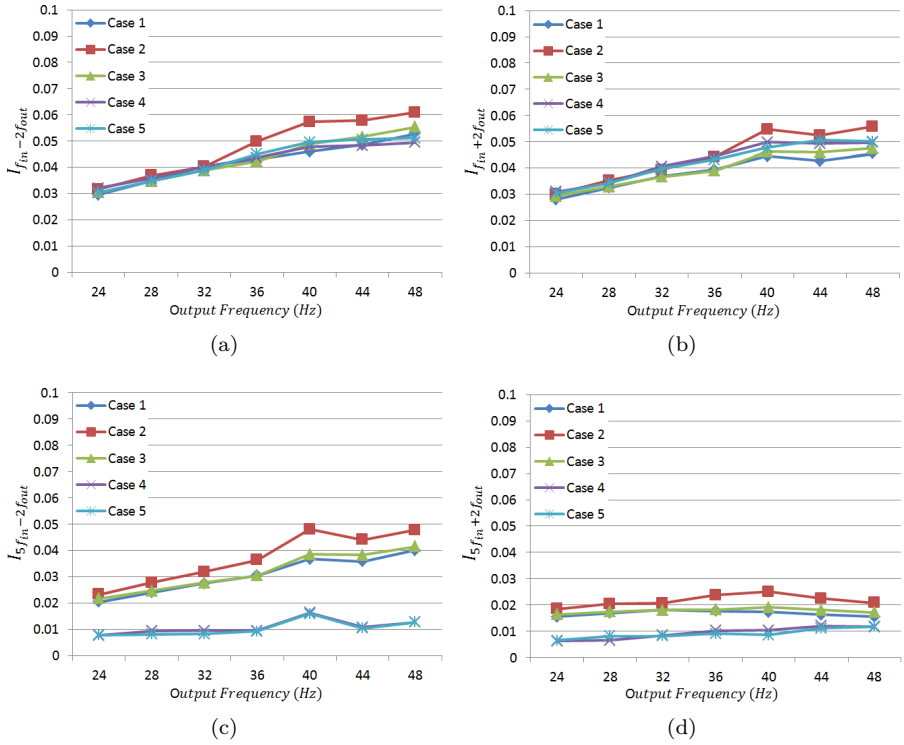


Figure 5.11: *Simulated normalized input current interharmonic components in Cases 1–5 versus output frequencies of the ASD at the load torque T_L equal to 6 Nm. (a) Interharmonics coupled with and below the fundamental frequency $I_{f_{in}-2f_{out}}$. (b) Interharmonics coupled with and above the fundamental frequency $I_{f_{in}+2f_{out}}$. (c) Interharmonics coupled with and below the fifth-order frequency $I_{5f_{in}-2f_{out}}$. (d) Interharmonics coupled with and above the fifth-order frequency $I_{5f_{in}+2f_{out}}$.*

respect to the current interharmonic components located around the fifth order grid current frequency are observed in Figure 5.11(c) and Figure 5.11(d).

The results presented so far clearly show that with the presence of any possible output current imbalance, a suitable design of the equivalent DC-link filters may lead to a better performance of the ASD handling of the input current interharmonics. It also shows that Case 2 (i.e. putting the filters in the DC side of the front-end diode rectifier) is usually giving higher values of the interharmonics especially when the motor is operating near the nominal speed at full load torque operating mode and/or it functions at the low load torque conditions.

Following the global trend towards using smaller DC-link filter components in ASD applications, the last two cases were devoted to analyze their effects on the ASD input current interharmonics. The results demonstrate superior performances of the last two cases compared with the first three cases in terms of the input current interharmonics caused by motor unbalanced currents. However, considering high resonance frequencies related to the last two cases, it is needed to study their performances at the higher disturbance frequencies of the DC-link current.

5.3 Balanced load conditions

In this section the possible effects of the equivalent DC-link passive filters on the input current interharmonics are studied considering a balanced operating mode of the ASD. Like the unbalanced load conditions, the investigated parameters are used as given in Table 5.1. In order to assess the drive input current quality in the five above-mentioned cases, three of the indices are taken into account: 1) the total harmonic current distortion (THD), 2) the total interharmonic current distortion up to 2 kHz (TIHD_{2kHz}), and 3) the total interharmonic current distortions between 2 kHz and 9 kHz (TIHD_{2-9kHz}). These indices are considered as (5.19)-(5.21),

$$THD = \frac{\sqrt{\sum_{h\in \mathrm{H}} I_h^2}}{I_1},\ H = \text{set of harmonics} \tag{5.19}$$

$$TIHD_{2kHz} = \frac{\sqrt{\sum_{ih\in \Lambda} I_{ih}^2}}{I_1},\ \Lambda = \text{set of interharmonics up to 2 kHz} \tag{5.20}$$

$$TIHD_{2-9kHz} = \frac{\sqrt{\sum_{ih\in \gamma} I_{ih}^2}}{I_1},\ \gamma = \text{set of interharmonics between 2 and 9 kHz} \tag{5.21}$$

The importance of the defined indices can be considered for the compatibility problem and the tough regulations for interharmonic components. In the case of linear modulation and balanced loading, the input current interharmonics in ASD usually accommodate around the switching frequency and its

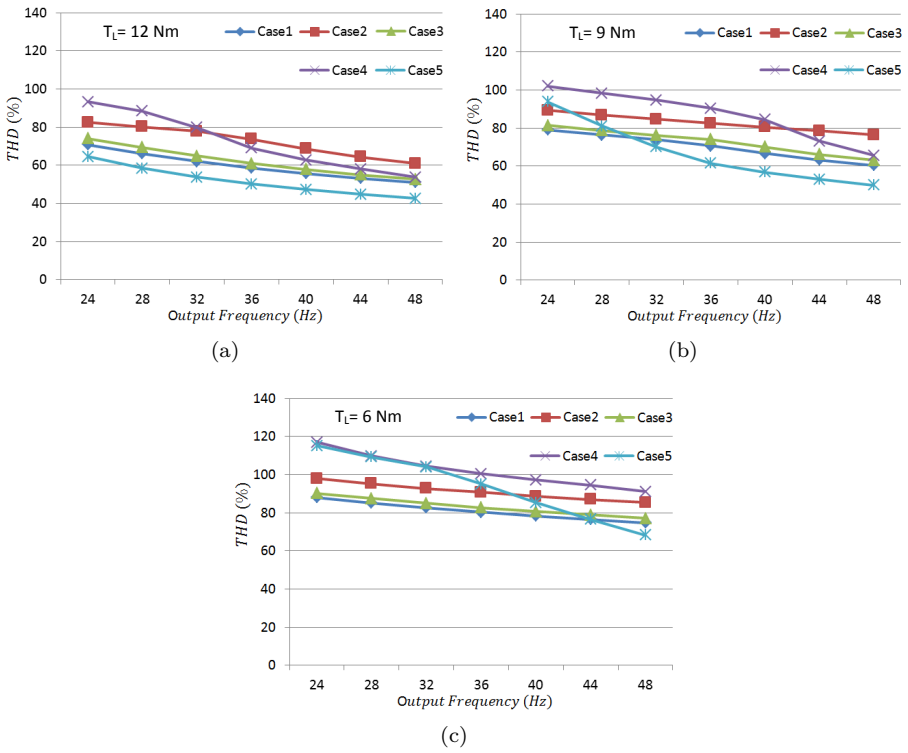


Figure 5.12: *ASD input current THD values associated with Cases 1–5 at different output frequencies. (a) load torque equal to 12 Nm. (b) load torque equal to 9 Nm. (c) load torque equal to 6 Nm.*

integer multiple components other than those appearing at the lower frequencies. This was the reason for choosing the two different indices (TIHD_{2kHz} and TIHD_{2-9kHz}) for interharmonic assessment.

The input current total harmonic distortion THD traces at the motor output frequency range of 24–48 Hz and three load torque values of 12, 9, and 6 Nm are plotted in Figure 5.12. It can be observed that the results associated with Case 5 demonstrate its good performance especially at high load torque values, even though it benefits from small filter components. From this standpoint and with taking the input current THD values into consideration, choosing small components as ASD filters will make them even competitive compared with selecting larger filters for ASD. Moreover, between the first three investigated cases (Cases 1–3), the traces show the priority for Case 1 at different operating modes.

Figure 5.13 illustrates the input current total interharmonic distortions (TIHD_{2kHz} and TIHD_{2-9kHz}) of the ASD in Cases 1–5 at two load torque

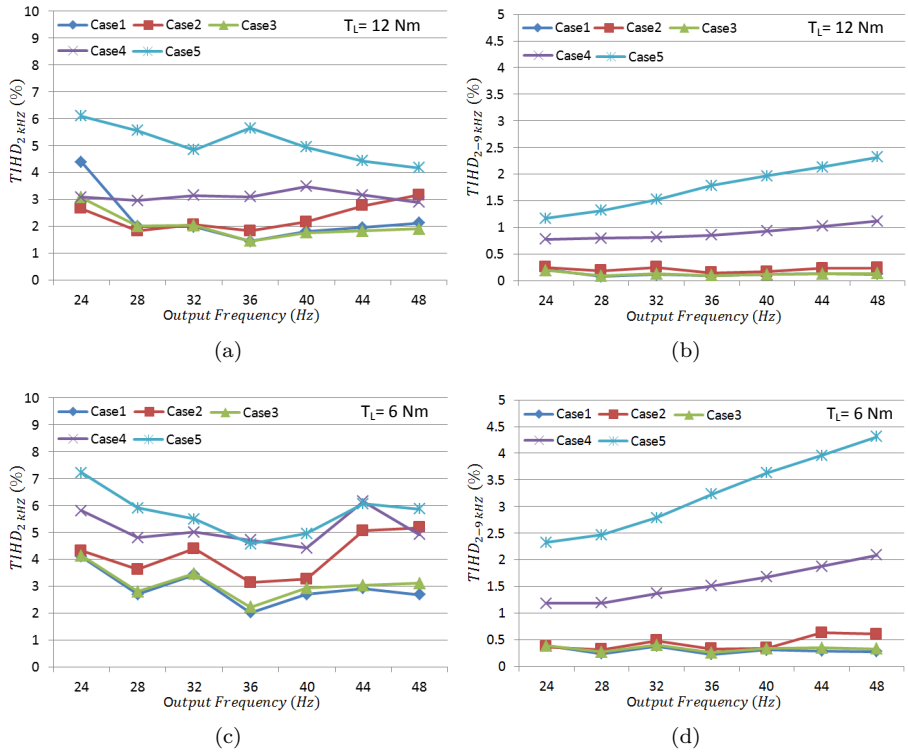


Figure 5.13: *Simulated input current total interharmonic distortions in Cases 1–5 versus output frequencies of the ASD. (a) $TIHD_{2kHz}$ at the load torque of 12 Nm. (b) $TIHD_{2-9kHz}$ at the load torque of 12 Nm. (c) $TIHD_{2kHz}$ at the load torque of 6 Nm. (d) $TIHD_{2-9kHz}$ at the load torque of 6 Nm.*

values of 12 and 6 Nm. Unlike the promising results of Case 5 with respect to the THD values especially at higher load torque conditions, as shown in Figure 5.12, this case represents the worst condition in respect to interharmonic components. This phenomenon is more evident at the total current interharmonic distortions between 2 and 9 kHz in Figure 5.13(b) and Figure 5.13(d), where $TIHD_{2-9kHz}$ increases significantly at higher output frequencies of the motor. By comparing the results related to the load torque values of 12 and 6 Nm, it can also be seen that the lower torque value gives higher current interharmonic distortions. Meanwhile, among the first three investigated cases, Case 2 presents the worst condition with respect to interharmonic distortions. Moreover, due to the fact that the DC-link resonances in the first three cases are accommodated at low frequencies, their effects on interharmonic magnification are less than the last two cases in which the DC-link resonances are

located at higher frequencies. With the on-going interests towards using a small DC-link filter for ASD, the depicted results obtained here makes it necessary to consider the interharmonic distortions especially for those interharmonics accommodated above 2 kHz.

5.4 Conclusion

In this chapter, the effects of ASD passive filters on the grid current interharmonics are investigated at separate drive output frequencies and also at different load torque values. Particular attention is given to both cases of the unbalanced and balanced operating modes of the ASD. The results show that in discontinuous conduction operation mode of the front-end diode rectifier, the DC-link resonance amplification decreases, however it does not necessarily mean a lower input current interharmonic distortions.

In the unbalanced operating condition, implementing small filter components for ASD results in a competitive performance in comparison with the larger filter components. However, for the balanced operating mode the results depicted a weak performance for the smaller filters in respect to interharmonic distortions. Moreover, almost in all operating conditions (at the same operating speed), it is shown that the drive input current distortions are higher at the lower load torque values. The comparative results of the five investigated filter cases should be useful for people concerning the drive input current distortions at the low and high frequency ranges.

Chapter 6

Interharmonic Mitigation in Partially- and Fully-Controlled ASDs

This chapter presents the mitigation of the ASD's input current interharmonics generated originally due to the motor current imbalance. The investigation discusses the possibility of interharmonics mitigation in the cases of partially and fully controlled ASD. AC side three-phase active filters and DC-link parallel active capacitor are first studied to remove the input current interharmonic components in the case of implementing a partially-controlled (with diode rectifier) ASD. Then, a control strategy is proposed for interharmonics mitigation in the case of applying a fully-controlled (back-to-back) ASD.

6.1 Introduction

Till now, several investigations have been initiated focusing more on the interharmonic sources, their identifications and their negative effects on the power supplies [12–15, 17, 30, 73, 83–85]. These studies are really useful to identify interharmonic components, but actually more attempts are needed related to the interharmonics reduction. In [41], an investigation has been done regarding interharmonics minimization by applying a DC-link active compensator. However, it has been implemented only in a current sourced AC drive and it also suffers from applying a full-bridge inverter as an active compensator, which definitely increases the costs. A separate DC source for an active compensator and also manually tuning of the filter are other shortfalls of that study. In [40], a dithering method has been proposed related to the interharmonics mitigation below a specific limit. But it actually spreads the intensities of the interharmonics over a wide frequency range and increases the noise level. Also, a virtual impedance based resonance suppression method discussed in [86] has shown a

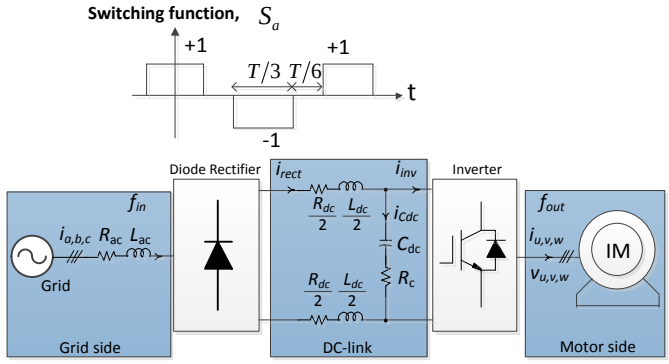


Figure 6.1: *Equivalent circuit of an adjustable-speed drive for system analysis with an induction motor (IM).*

Table 6.1: *Parameters for simulation study of interharmonics in ASD.*

Symbol	Parameter	Value
$v_{a,b,c}$	Grid phase voltage	230 V_{rms}
f_{in}	Grid frequency	50 Hz
L_{ac}, R_{ac}	Grid inductor & resistor	203 μH & 13 mΩ
L_{dc}, R_{dc}	DC-link inductor & resistor	120 μH & 3.5 mΩ
C_{dc}, R_c	DC-link capacitor & resistor	4800 μF & 20 mΩ
f_{sw}	Inverter switching frequency	5 kHz
v_{LL}	Induction motor rated voltage	400 V_{rms}
P_{IM}	Induction motor rated power	75 kW

significant reduction of interharmonic currents, though it only is applied for the current source motor drives.

In this chapter an AC-side three-phase active filter and also a new DC-link located active capacitor is first proposed to minimize the input current interharmonic components of a classical adjustable speed drive, where a three-phase diode rectifier is connected to a rear-end inverter sharing a common DC link. The concept of using these active compensators can generally be applied to different types of ASDs. However a Voltage Source AC/DC/AC Converter (VSC) with unbalanced load currents which exerts input current interharmonics [15] is considered as a case study here. Then, the investigation will be followed by implementing a back-to-back ASD using a specific control strategy to mitigate the associated interharmonics.

6.2 Partially-controlled ASD

The harmonic transfer through the adjustable speed drive with motor current imbalance has been fully introduced in Chapter 5. It is shown that how the motor unbalanced currents may give rise to the drive input current interharmonic components. For the sake of clarity, the diagram of the VSI-fed adjustable speed drive is again illustrated in Figure 6.1, whose assumed parameters are listed in Table 6.1.

In order to address the transfer of harmonics, the drive system shown in Figure 6.1 was simulated in Matlab/Simulink. A 75 kW induction motor is

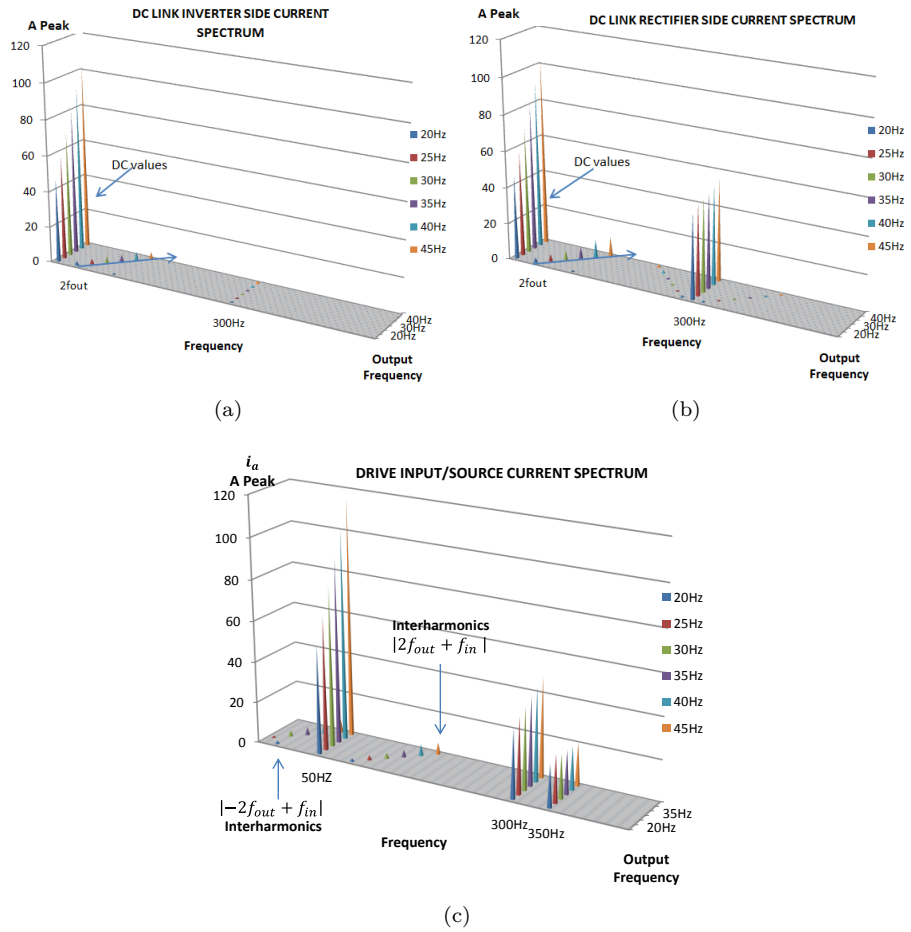


Figure 6.2: *ASD output current distortion transfer at load torque, T_L, equal to 460 Nm and f_{out}=20–45 Hz. (a) Inverter-side DC-bus current i_{inv} spectra. (b) Rectifier-side DC-bus current i_{rect} spectra. (c) Input current i_a spectra.*

considered with the output frequency range of f_{out}= 20–45 Hz and a constant load torque value of T_L= 460 Nm. The motor is controlled by implementing a simple constant voltage-to-frequency method, and an inductor of 0.125 mH was also added to one of the phases of the motor to emulate a motor-winding imbalance. As a consequence, a motor current imbalance of about five to six percent was provided by this method.

Figure 6.2 illustrates how an ASD output current distortion flows through the DC-link stage and will appear as grid current interharmonics. As it can be seen in Figure 6.2(a), the motor current distortions will cause inverter-side DC-link current oscillations at twice the output frequency, where their magnitude may be even higher than the sixth order oscillation inherited from the drive input current. Afterwards, these oscillations encounter with the DC-link resonance excitation caused by the drive passive filter components (AC choke, DC choke and DC-link capacitor) and the same oscillation frequency will consequently be created at the rectifier-side DC-link current, which may have even more amplitude than those of the inverter side current distortion as it is shown in Figure 6.2(b). It is worth to mention that the inverter-side current distortions will interact with all harmonic components of the rectifier-side DC-link current, and will distribute around them. However, these components will normally appear with lower amplitudes at higher frequencies, as seen in Figure 6.2(b). Finally, the input current interharmonic components accommodated around the fundamental frequency are shown in Figure 6.2(c). In this figure, the interharmonic components located around the grid characteristic harmonic frequency are not shown because of their small amplitudes. However, the higher order interharmonics even with small magnitude are potentially able to excite the dormant resonance in the power system.

In the case of using partially-controlled ASD (i.e. double-stage ASD with diode rectifier), it may be difficult to remove interharmonics so they are not passed into the grid. In this condition, benefiting from an external device like an active compensator can be a solution for solving the problem. This part of the investigation evaluates the performance of the active devices for removing interharmonic components others than the harmonic ones. Figure 6.3 represents an equivalent circuit of a partially-controlled adjustable speed drive combined with some of the proposed active devices for removing harmonic and interharmonic currents. For instance, a Shunt Active Power Filter (SAPF) which is widely investigated and applied for harmonic compensation, and also, the parallel DC-link compensators can be considered to compensate for the interharmonic currents caused by the motor current imbalance.

By using the same methods and control techniques as those implemented for harmonics compensation, the parallel active power compensators [87, 88], as shown in Figure 6.3(a) & (d), can generate interharmonic currents with opposite angle of the associated oscillations initiated by the motor current imbalance. In this way, interharmonic components are neutralized at the connection point. In order to achieve an appropriate response, Shunt Active Power Filter (SAPF) needs to be located near the rectifier to be able to transfer the motor

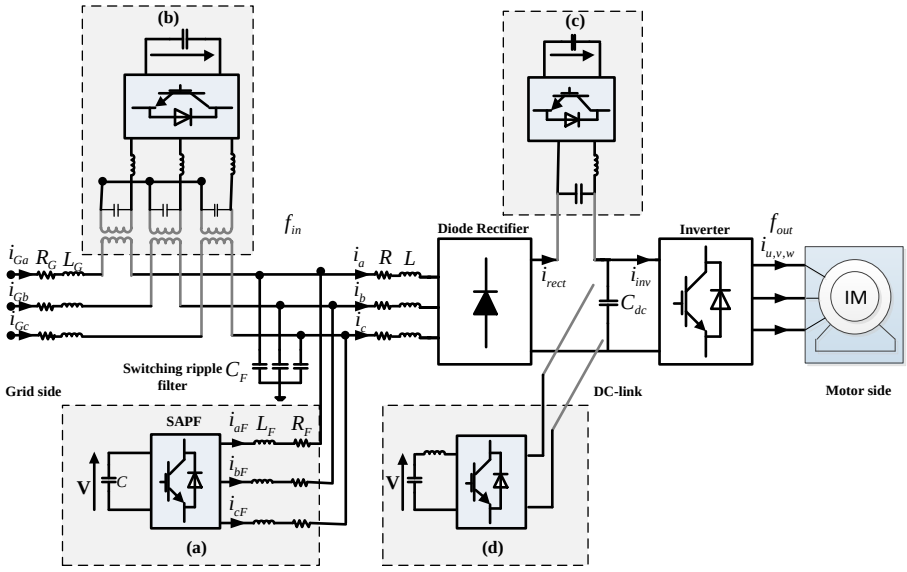


Figure 6.3: *Equivalent circuit of an adjustable speed drive combined with some potential active interharmonic compensators. a) AC-side shunt active power filter, b) AC-side series active compensator, c) DC-link series active compensator, d) DC-link shunt active compensator.*

operating frequency to the SAPF's controller as fast as possible via communication cable. Otherwise, in the case of applying SAPF far from the rectifier, an identification algorithm has first to be provided to determine the interharmonic frequencies for the controller.

Series active compensators which are used for voltage stability and even for harmonics compensation can also be adopted for removing interharmonic currents. The main idea of applying the series compensators, as shown in Figure 6.3(b) & (c), is to block the interharmonics and prevent them transferring into the grid. In this respect, after recognizing the related interharmonic components, the controller should provide an adequate voltage across the output terminals to create a high virtual impedance against that specific component.

6.2.1 Shunt active power filter (SAPF)

A control block diagram of the employed shunt active power filter, shown in Figure 6.3(a), is illustrated in Figure 6.4. A resonant controller [89], whose transfer function is given in (6.1), is chosen for selective harmonic and interharmonic compensation. The resonant frequency w_{ih} must be set to target the harmonic and interharmonic components. Its gain K_{ih} must also be raised to provide a high resonant peak needed for precise tracking. The assumed

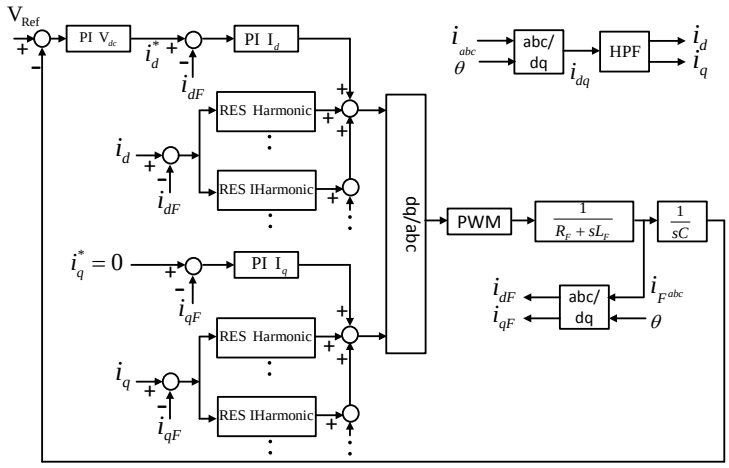


Figure 6.4: *Control block diagram for the shunt APF shown in Figure 6.3(a).*

Table 6.2: *Simulation parameter values for SAPF.*

Symbol	Parameter	Value
V	DC-link voltage	900 V
f_{swf}	Switching frequency	10 kHz
C	DC-link capacitor	2200 μF
L_F, R_F	Inductor & resistor	750 μH & 20 mΩ
C_F	Switching ripple capacitor	100 μF

parameters of the SAPF for the simulation study are given in Table 6.2.

$$G_{ih}(s) = \frac{2K_{ih}\omega_c s}{s^2+2\omega_c s+\omega_{ih}^2} \tag{6.1}$$

Figure 6.5(a) illustrates the grid current spectra without any compensation in the case of the motor current imbalance at 40 Hz motor operation frequency. As mentioned earlier, in this investigation an inductor of 0.125 mH is added in order to introduce 5 percent motor current imbalance. It clearly shows the presence of interharmonics as sidebands of the fundamental power supply frequency at 30 Hz and 130 Hz, and also sidebands of the other current harmonics for example, at 170 Hz and 330 Hz for 5th harmonic, and 270 Hz and 430 Hz for 7th harmonic. It can also be seen that, like the case of harmonic components, magnitudes of the interharmonic components decrease when their frequencies increase. Moreover, Figure 6.5(a) shows that magnitudes of the interharmonics located around the fundamental grid frequency are more than the magnitudes

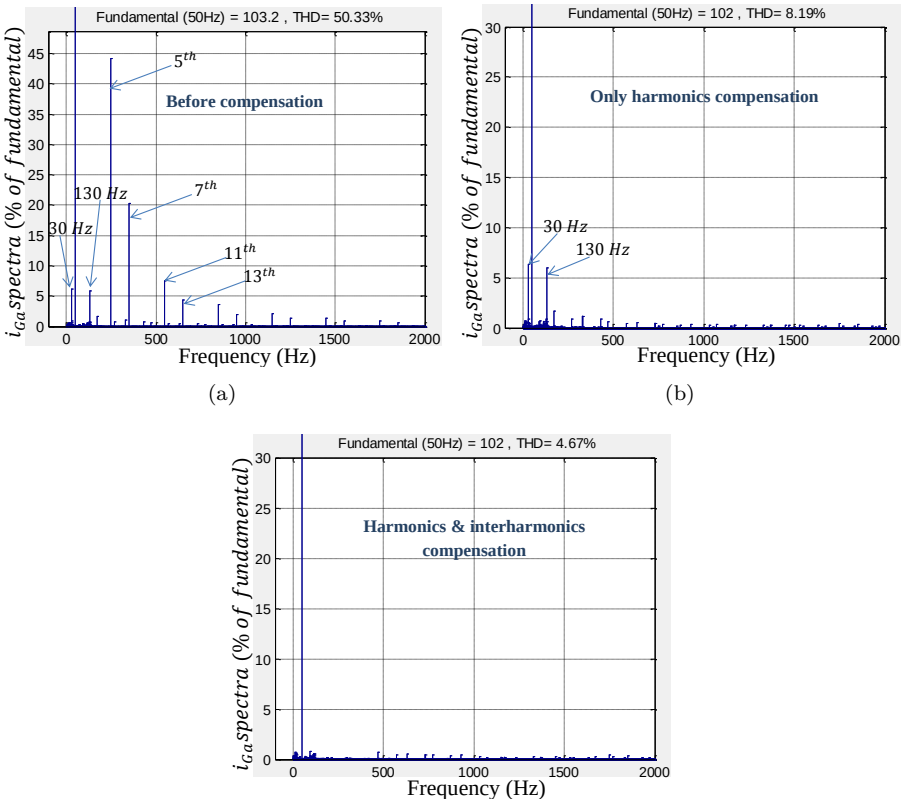


Figure 6.5: *Grid current spectra at a load torque, T_L, equal to 460 Nm, f_{out}=40 Hz and with a 5% motor current imbalance. (a) Before compensation, (b) After harmonics compensation and (c) After harmonics and interharmonics compensation.*

of 13th and 17th order harmonics. Figure 6.5(b) shows the spectral component of the grid current after applying the selective harmonic compensation up to 37th order. It should be noted that, after removing the harmonic components, the presence of the interharmonic components still keeps the THD value high, about 8 percent. In addition, the presence of interharmonics, especially at low frequencies, may have negative effects for power system. Finally, the results related to interharmonic compensation up to those around 7th order harmonic are illustrated in Figure 6.5(c). By compensating these interharmonic components, the THD value decreases from about 8 percent to less than 5 percent. According to the results shown in Figure 6.5, it is worth to mention that some active harmonic compensators, which are previously installed into the power

system, can be optimized to simultaneously remove interharmonic components too.

6.2.2 DC-link active capacitor

As discussed earlier, in an ASD, the inverter output current distortions may leak through the DC-bus subsystem and be transferred to the grid side, appearing as interharmonic components. The active DC-link compensators which have recently attracted more interests in several power electronic applications, such as reduction of the DC-link capacitance for three-phase and single-phase rectifiers [88,90], can be a solution for decreasing the grid current interharmonic components caused by the motor unbalanced currents.

Here, the DC-link active capacitor whose topology is illustrated in Figure 6.6 is proposed to compensate the targeted DC-link oscillations and consequently remove the related grid current interharmonics.

The proposed topology is composed of two IGBT switches S_1, S_2 , an inductor L_a working as an energy transferring element and also a capacitor C_a acting as an energy storage component. The control objective is to compensate the DC-link inverter-side ripple current $i_{\sim inv}$, already introduced in (5.7), initiated by the load current imbalance. When the ripple current $i_{\sim inv}$ is positive, the switch S_1 will be turned on and off in order to sink the ripple energy from the DC bus to the compensation circuit. During the turn-on time of switch S_1, the ripple current will charge the inductor L_a and the capacitor C_a. Here, the capacitor is the main storage component, while the inductor only transfers the ripple energy, which leads to the discontinuous conduction mode operation of the compensation circuit. During the turn-off period of switch S_1, the inductor will release its energy more to the capacitor. When the ripple current $i_{\sim inv}$ is negative, switch S_2 will be turned on and off in order to release the ripple energy stored in the capacitor back to the DC bus. During the turn-on time of switch S_2, the energy stored in the capacitor will charge the inductor while when it is turned off, the energy of both the capacitor and the inductor will be transferred to the DC bus. The ripple current compensation can thus be

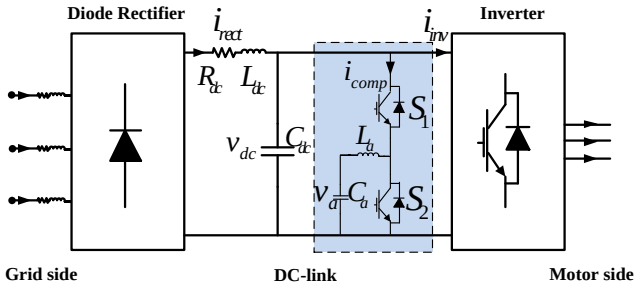


Figure 6.6: *Schematic diagram of an adjustable speed drive with an active DC-link interharmonic compensator.*

achieved by calculating the correct duty cycles for switches S_1 and S_2.

In order to achieve the control objective, the average compensation current i_{comp} in each sampling period should be equal to the oscillation component of the DC-link inverter-side current $i_{\sim inv}$. Figure 6.7 illustrates the duty-cycles related to the switch S_1 and S_2 and the corresponding charging and discharging state of the transferring inductor L_a. Regarding the switching frequency of the compensation circuit 5 kHz and the frequency of oscillatory current $i_{\sim inv}$ which is maximum 100 Hz (when the motor operating frequency is 50 Hz), the DC-bus voltage v_{dc} and the active compensator's capacitor voltage v_a can be considered as constant values, V_{dc} and V_a respectively, in each sampling period. Therefore, a constant slope of the compensation current during the turn-on and turn-off intervals of the switches will be considered (as shown in Figure 6.7) to calculate the required duty cycles D_1^1 and D_2^1 for the switches S_1 and S_2 respectively.

As the transferring inductor L_a works in a discontinuous conduction mode,

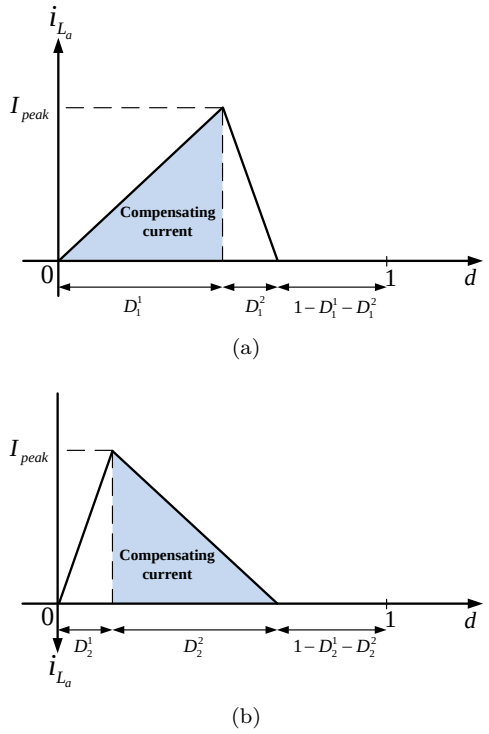


Figure 6.7: *Compensation scheme. (a) Duty-cycle related to the switch S_1 and the corresponding charging and discharging state of the inductor L_a when the ripple current is positive. (b) Duty-cycle related to the switch S_2 and the corresponding charging and discharging state of the inductor L_a when the ripple current is negative.*

the relationship between the turn-on and turn-off intervals of the switch S_1, when the ripple current $i_{\sim inv}$ is positive and can be calculated as follows,

$$D_1^2 = \frac{V_{dc}-V_a}{V_a} D_1^1 \tag{6.2}$$

where D_1^1 is the duty cycle of the switch S_1 expressed as a ratio of the switch ON time to the time of one complete switching cycle, T_s. The duration of the OFF state to the time of one switching cycle T_s is notated as D_1^2.

For the sake of ripple compensation, the average compensating current, as shown in blue area of Figure 6.7(a), should be equal to the DC-link inverter-side ripple current average value,

$$\frac{1}{2} \times D_1^1 \times I_{peak} = i_{\sim inv} \tag{6.3}$$

when the ripple current component $i_{\sim inv}$ is positive, the peak current value I_{peak} of inductor L_a in each switching cycle is

$$I_{peak} = \frac{V_{dc}-V_a}{L_a} D_1^1 T_s \tag{6.4}$$

Thus, when the DC-link inverter-side current ripple is positive, the required duty cycle for the switch S_1 can be obtained from (6.3) and (6.4) as follows,

$$D_1^1 = \sqrt{\frac{2 \cdot i_{\sim inv} \cdot f_s \cdot L_a}{V_{dc}-V_a}} \tag{6.5}$$

where the switching frequency of the control circuit is notated as f_s.

As mentioned earlier, when the DC-link inverter-side current is negative, the switch S_2 will be turned on and off to deliver the energy stored in the capacitor C_a into the DC bus. During the turn-on time of the switch S_2, this energy will charge the transferring inductor L_a. Then, during the turn-off time of the switch S_2, the whole energy of the compensating circuit, illustrated in blue area of Figure 6.7(b), will be transferred into the DC bus. The relationship between the turn-on and turn-off intervals of the switch S_2, when the ripple current $i_{\sim inv}$ is negative, can be calculated as follows,

$$D_2^2 = \frac{V_a}{V_{dc}-V_a} D_2^1 \tag{6.6}$$

where, the duty cycle of the switch S_2 is notated as D_2^1 , expressed as a ratio of the switch ON time to the time of one complete switching cycle, T_s. The duration of the OFF state to the time of one switching cycle T_s is defined as D_2^2.

In this condition, the average compensating current, as shown by the blue area of Figure 6.7(b), should be equal to the DC-link inverter-side ripple current average value,

$$\frac{1}{2} \times D_2^2 \times I_{peak} = i_{\sim inv} \tag{6.7}$$

The peak current value I_{peak} of inductor L_a in each switching cycle, when the oscillatory current component $i_{\sim inv}$ is negative can be expressed as,

$$I_{peak} = \frac{V_{dc}-V_a}{L_a} D_2^2 T_s \tag{6.8}$$

Therefore, the required duty cycle D_2^1 for the switch S_2 can be obtained from (6.6), (6.7) and (6.8) as follows,

$$D_2^1 = \sqrt{\frac{2 \cdot i_{\sim inv} \cdot f_s \cdot L_a \cdot (V_{dc} - V_a)}{{V_a}^2}} \tag{6.9}$$

Based on equations (6.5) and (6.9), the required duty cycles are calculated for the switches S_1 and S_2 in order to compensate the DC-link inverter-side current ripple component $i_{\sim inv}$. In this way, the active DC-link compensator prevents the targeted ripple component to be passed from the DC-link inverter side to the front-end diode rectifier, leading to input current interharmonic reduction. In the control circuit, a voltage loop is also applied to set the average value of the active compensator's capacitor voltage v_a. The output of this voltage loop then will be added to the DC-link inverter-side current ripple component $i_{\sim inv}$ to form the reference current for the compensation.

The drive system shown in Figure 6.1 was simulated in Matlab/Simulink using those parameters given in Table 6.1 and with applying the proposed active DC-link compensator at 40 Hz motor input voltage frequency. In this simulation, the DC-link compensator inductor L_a and capacitor C_a values are 300 μH and 300 μF respectively. For the compensator capacitor C_a, a voltage control loop is also considered to keep its average voltage value at 570 V.

Figure 6.8 illustrates the active compensator's capacitor voltage v_a waveform and the corresponding DC-link inverter-side ripple current component. As it can be seen in Figure 6.8, when the DC-link inverter-side current $i_{\sim inv}$ is positive, the ripple energy will go through the active compensator, and the ca-

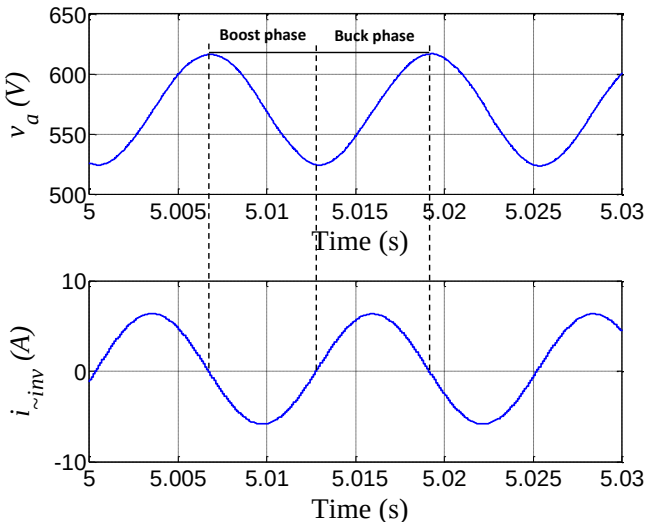
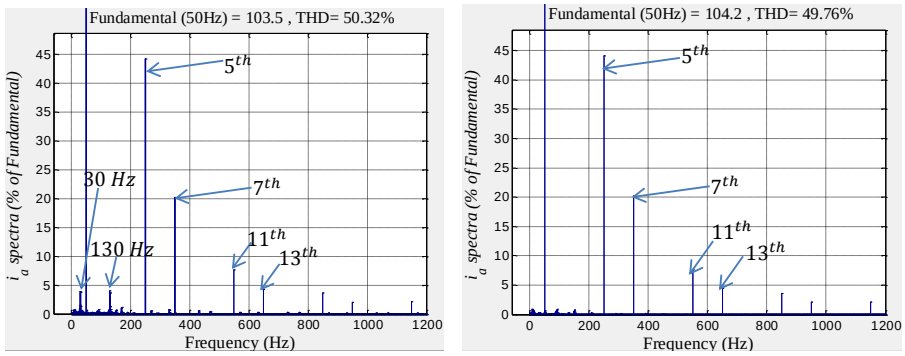


Figure 6.8: *Simulation waveforms with the active DC-link interharmonic compensator.*



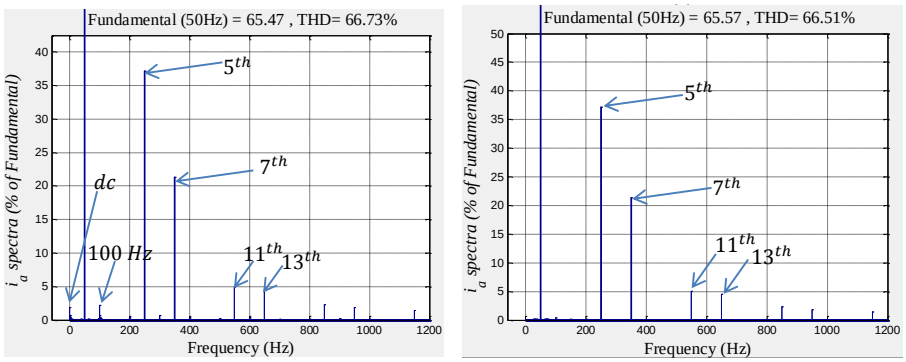
(a) (b)

Figure 6.9: *Input current i_a spectra when the motor input voltage frequency is equal to 40 Hz. (a) Before applying the DC-link compensator. (b) After applying the DC-link compensator.*

pacitor C_a will be charged. In this condition, the active compensator operates as a DC-DC buck converter. When this current is negative, the ripple energy saved in the capacitor will be released into the DC bus leading to the oscillation current compensation. At this step, the active compensator operates as a DC-DC boost converter, which is able to deliver the required energy to the DC bus.

The effect of this compensation on the grid-side AC current interharmonic components is depicted in Figure 6.9 at 40 Hz motor operating frequency. As expected, when there is no compensation, the main interharmonic components will appear around the input current fundamental frequency component at 30 Hz and 130 Hz, plotted in Figure 6.9(a). However, these current interharmonics will be also accommodated around the input current characteristic harmonic components with lower amplitudes.

The input current spectra after implementing the DC-link active capacitor are shown in Figure 6.9(b). As it can be seen, the input current interharmonic components have been decreased significantly. Finally, the input current spectra in the case of 25 Hz motor input voltage frequency are shown in Figure 6.10. In this condition, the main input current interharmonic components appear as DC component and 100 Hz component, as shown in Figure 6.10(a). The result after implementing the active compensator is shown in Figure 6.10(b). Although with the lower inverter output frequency, the input current interharmonics appear in smaller amplitudes (as a consequence of the lower inverter modulation ratio in the constant voltage-to-frequency control method of ASD), but they still have their importance because of locating at the lower frequencies even at zero frequency.



(a) (b)

Figure 6.10: *Input current i_a spectra when the motor input voltage frequency is equal to 25 Hz. (a) Before applying the DC-link compensator. (b) After applying the DC-link compensator.*

6.3 Fully-controlled ASD

Beside the methods proposed in the previous section, a back-to-back based adjustable speed drive can also be applied to block the interharmonic currents transferring from motor side to grid side. Figure 6.11 shows the typical block representation of a back-to-back controlled motor drive, whose parameters assumed are as given in Table 6.3. The system begins with a front-end rectifier rectifying the three-phase grid voltages to provide a DC voltage for powering the rear-end inverter. The inverter then converts the DC voltage to a set of three-phase balanced sinusoidal voltages for driving the motor. The fundamental frequency of the inverter is determined by the demanded motor speed, which typically is not the same as the grid frequency. This leads to the creation of interharmonics seen at the grid side, and vice versa, when distortions surface at the other end. The distortion assumed here is again created at the motor side by inserting an inductance of 0.125 mH in series with one phase of the motor. The currents drawn by the motor will then be unbalanced, which when "processed" by the following three mechanisms, give rise to interharmonics in the grid.

6.3.1 Sources 1 and 2 related to DC voltage ripple

The DC-link inverter-side current oscillation caused by the motor current imbalance was already formulated in Chapter 5, and can be represented as,

$$\begin{aligned} i_{inv} &= I_{dc} - i_{\sim inv} = I_{dc} + I_{\sim inv}\cos\left(2w_{out}t + \theta_{inv}\right) \\ &= \tfrac{3}{4}mI^{p}_{out}\cos\left(\theta^{p}_{out}\right) - \tfrac{3}{4}mI^{n}_{out}\cos\left(2\omega_{out}t + \theta^{n}_{out}\right) \end{aligned} \tag{6.10}$$

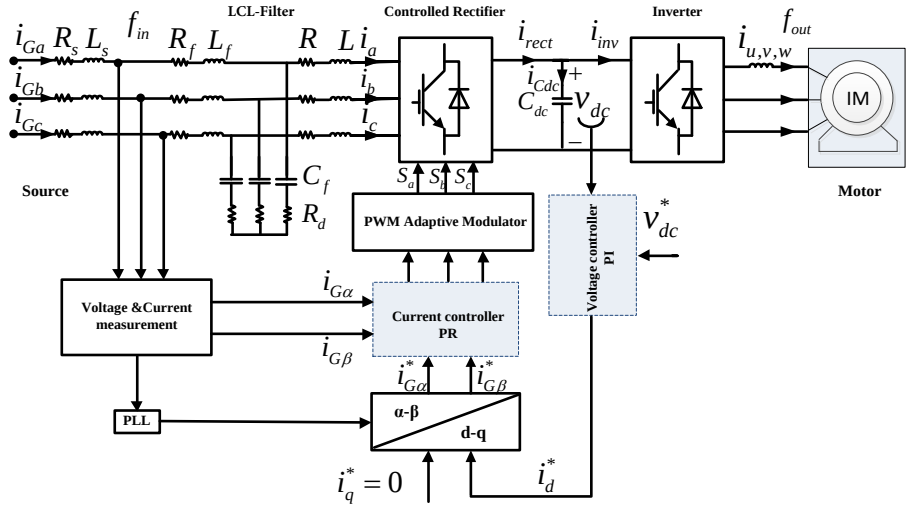


Figure 6.11: *Equivalent circuit of an adjustable speed drive for system analysis and control system for interharmonic compensation.*

Table 6.3: *Simulation parameter values for back-to-back based ASD implementation.*

Symbol	Parameter	Value
$v_{a,b,c}$	Grid voltage (line to line)	380 V_{rms}
f_{in}	Grid frequency	50 Hz
L_s, R_s	Grid inductor & resistor	28 μH & 8 mΩ
L, R	rectifier-side inductor & resistor	760 μH & 5 mΩ
L_f, R_f	grid-side inductor & resistor	500 μH & 5 mΩ
C_f	Filter capacitor	40 μF
R_d	Damping resistor	1 Ω
v_{dc}	DC-link voltage	700 V
C_{dc}	DC-link capacitor	1500 μF
f_{sw}	Inverter switching frequency	5 kHz
v_{LL}	Induction motor rated voltage	400 V_{rms}
P_{IM}	Induction motor rated power	75 kW

This current can basically be divided into the current passing through the DC-link capacitor i_{Cdc}, and, the current flowing out of the front-end rectifier i_{rect}. In the steady state, i_{Cdc} contains only the ripple component, which when flows through the finite DC-link capacitance, gives rise to the DC-link voltage expression in (6.11),

$$v_{dc} = V_{dc} + V_{dc2} cos\left(2\omega_{out} t + \theta_{dc2}\right) \tag{6.11}$$

The first term in (6.11) is the desired DC voltage V_{dc}, while the second term is a ripple component with magnitude, frequency and phase notated as V_{dc2}, $2\omega_{out}$ and θ_{dc2}. The DC-link ripple component, if it is not compensated and when multiplied with the rectifier switching functions in (6.12)-(6.14), gives rise to those input voltage expressions in (6.15)-(6.17), which obviously, has interharmonic components located at $\omega_{in}\pm 2\omega_{out}$. The magnitude and phase of these interharmonic voltages are notated as $(S_{in}V_{dc2})/2$ and θ_{dc2}, which when interacted with the grid impedances, give rise to interharmonic current components located at the same frequencies. Other interharmonic components can also be formed by other combinations of the grid and motor operating conditions, which in general can be represented by the frequency expression of $k_{in}\omega_{in}\pm k_{out}\omega_{out}$, where k_{in} and k_{out} are integers.

$$s_a = S_{in}\sin\left(\omega_{in}t\right) \tag{6.12}$$

$$s_b = S_{in}\sin\left(\omega_{in}t - \tfrac{2\pi}{3}\right) \tag{6.13}$$

$$s_c = S_{in}\sin\left(\omega_{in}t + \tfrac{2\pi}{3}\right) \tag{6.14}$$

$$\begin{aligned} v_a = s_a v_{dc} &= S_{in}V_{dc}\sin\left(\omega_{in}t\right) \\ &+ \tfrac{S_{in}V_{dc2}}{2}\left[\sin\left(\left(\omega_{in}+2\omega_{out}\right)t + \theta_{dc2}\right) + \sin\left(\left(\omega_{in}-2\omega_{out}\right)t - \theta_{dc2}\right)\right] \end{aligned} \tag{6.15}$$

$$\begin{aligned} v_b = s_b v_{dc} &= S_{in}V_{dc}\sin\left(\omega_{in}t - \tfrac{2\pi}{3}\right) \\ &+ \tfrac{S_{in}V_{dc2}}{2}\left[\sin\left(\left(\omega_{in}+2\omega_{out}\right)t + \theta_{dc2} - \tfrac{2\pi}{3}\right) + \sin\left(\left(\omega_{in}-2\omega_{out}\right)t - \theta_{dc2} + \tfrac{2\pi}{3}\right)\right] \end{aligned} \tag{6.16}$$

$$\begin{aligned} v_c = s_c v_{dc} &= S_{in}V_{dc}\sin\left(\omega_{in}t + \tfrac{2\pi}{3}\right) \\ &+ \tfrac{S_{in}V_{dc2}}{2}\left[\sin\left(\left(\omega_{in}+2\omega_{out}\right)t + \theta_{dc2} + \tfrac{2\pi}{3}\right) + \sin\left(\left(\omega_{in}-2\omega_{out}\right)t - \theta_{dc2} - \tfrac{2\pi}{3}\right)\right] \end{aligned} \tag{6.17}$$

Besides (6.15)-(6.17), the DC-link voltage v_{dc} can also create interharmonics at the grid through a second path better explained with the diagram shown in Figure 6.11. In the diagram and practically all grid-interfaced converters, the DC-link voltage v_{dc} is measured, subtracted from a constant reference V_{dc-ref}, and then fed to a proportional-integral (PI) controller for regulation purposes. Since the PI controller gain is finite at non-zero frequency, some amount of $2\omega_{out}$ ripple from v_{dc} will leak through to the inverse d-q transformation block, where it is multiplied with sine and cosine functions locked at the grid frequency of ω_{in} by the Phase-Locked-Loop (PLL). The important observation noted is the multiplication of sinusoidal expressions at different frequencies ($2\omega_{out}$ a nd ω_{in}) has again occurred, which as understood from (6.15)-(6.17), will lead to spectral components at $\omega_{in}\pm 2\omega_{out}$. These spectral components will flow through an inner Proportional-Resonant (PR) controller and pulse-width modulator of the rectifier, eventually ending up as interharmonics at the AC input of the rectifier.

6.3.2 Source 3 related to DC current ripple

Earlier, focus has been $2\omega_{out}$ voltage ripple of v_{dc}, which as explained, is caused by the $2\omega_{out}$ current ripple of i_{Cdc}. A current ripple of i_{rect} would follow rather the same mechanism mentioned for the DC-link voltage ripple, when especially the DC-link is not well buffered. According to the circuit law, the DC-link inverter-side current oscillations at $2\omega_{out}$ flowing to the rectifier side will exert the same ripple frequency on the DC-link rectifier-side current, which when multiplied with the rectifier average switching functions given in (6.12)-(6.14), gives rise to expressions for the rectifier input currents, whose frequencies are like those obtained in (6.15)-(6.17). It should be pointed out that multiplication involving sinusoidal functions at two different frequencies ($2\omega_{out}$ and ω_{in}) has again occurred like in (6.15)-(6.17) and it is thus a third mechanism, through which motor distortions can leak to the grid as interharmonics.

6.3.3 Mitigation of sources 1 and 2 related to DC voltage ripple

Interharmonics related to the DC voltage ripple is produced according to (6.15)-(6.17) during the modulation process. To mitigate this cause, the simplest scheme is to divide the rectifier switching functions $\{s_a, s_b, s_c\}$ by a scaled amount of the measured DC-link voltage, expressed as v_{dc}/V_{dc} , before the modulation. The resulting input voltages then change according to (6.18)-(6.20), where multiplication of sinusoids at different frequencies can no longer be seen. No doubt, such DC-link voltage compensation has been used in most drive systems, but it has never been explicitly linked to interharmonics. The link has been formalized here, demonstrating how interharmonics related to the DC-link voltage ripple can be removed by including a simple DC-link voltage division.

$$v_a = \frac{s_a}{v_{dc}/V_{dc}} v_{dc} = S_{in} V_{dc} \sin(\omega_{in} t) \tag{6.18}$$

$$v_b = \frac{s_b}{v_{dc}/V_{dc}} v_{dc} = S_{in} V_{dc} \sin\left(\omega_{in} t - \tfrac{2\pi}{3}\right) \tag{6.19}$$

$$v_c = \frac{s_c}{v_{dc}/V_{dc}} v_{dc} = S_{in} V_{dc} \sin\left(\omega_{in} t + \tfrac{2\pi}{3}\right) \tag{6.20}$$

The compensation in (6.18)-(6.20) is however not useful when considering the second source of interharmonics caused by the leaking of DC voltage ripple through the outer PI controller as shown in Figure 6.11. To stop the leak, the PI controller could be complemented by a notch filter tuned at $2\omega_{out}$, whose actual value depends on the present motor speed, and is hence variable. Such variation can easily be incorporated by implementing a notch filter indirectly with a resonant filter [89], whose peak is always set to one. The transfer function of the resonant filter is given in (6.21), whose resonant frequency $\omega_h = 2\omega_{out}$ can be changed with the motor speed. The sensitivity of the resonant peak can also be changed by varying ω_c to change its bandwidth.

$$G_h(s) = \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_h^2} , \qquad G_h(j\omega_h) = 1 \tag{6.21}$$

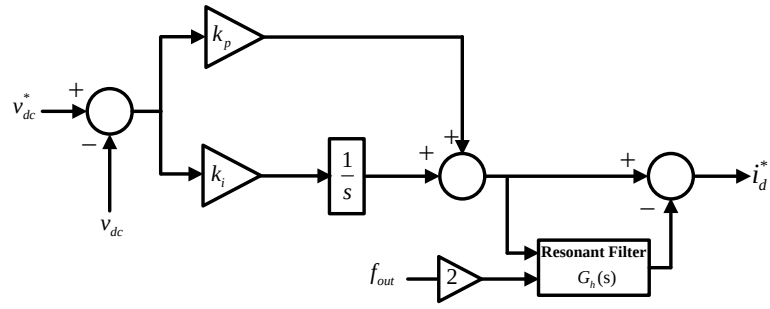


Figure 6.12: *Block diagram showing resonant filter after the outer PI controller for use in a back to back converter.*

Upon added to the PI controller like in Figure 6.12, the unity resonant filter will pass only the $2\omega_{out}$ ripple of $i^*_{d-int} = PI \times (V^*_{dc} - v_{dc})$, which when subtracted from i^*_{d-int}, gives a constant active current command i^*_d for feeding to the inverse d-q transformation block. Being a constant reference, no multiplication of sinusoids at different frequencies happens in the inverse d-q transformation block, resulting in no interharmonics created at the rectifier input.

6.3.4 Mitigation of source 3 related to DC current ripple

Source 3 is caused by the $2\omega_{out}$ ripple in i_{rect}, which can hence be mitigated by reducing that ripple to zero. Nulling the ripple can be done by decreasing the impedance of C_{dc} to zero or increasing the DC output impedance of the rectifier to infinity at the frequency of interest. Decreasing the impedance or increasing the capacitance of C_{dc} is however not economically viable, leaving only the rectifier DC output impedance for consideration, which in theory, can be increased by modifying the rectifier control without adding extra hardware. However, the required control cannot be implemented directly at the rectifier DC terminals because of the pulsating nature of the DC current i_{rect}. An alternative indirect scheme is therefore proposed, whose principle is based on reversing the source-to-effect mechanism. That means regulating the rectifier AC input currents to force their interharmonic components at $\omega_{in} \pm 2\omega_{out}$ to zero. By doing so, the $2\omega_{out}$ ripple in i_{rect}, which is the source of interharmonics, will be nullified. Controlling the rectifier input current in this way is thus equivalent to adding an infinite impedance at the rectifier output to force the $2\omega_{out}$ ripple of i_{rect} to be zero.

Using the indirect approach also has the advantage of simplicity without significantly modifying the drive control structure as shown in Figure 6.11. The proposed control scheme can, in fact, be realized by plugging additional resonant controllers to the inner PR current control block shown in Figure 6.11. The transfer function representing these resonant controllers is already given in (6.1), where the resonant frequency must be set to $\omega_{ih} = \omega_{in} \pm 2\omega_{out}$.

6.3.5 Proposed methodology

The methodology proposed for mitigating grid interharmonics caused by motor distortions, includes the three control schemes explained above. The same schemes can equally be applied to the inverter for stopping grid distortions from affecting the motor, even though it has not been explicitly elaborated in the thesis. For both cases, influences exerted by the schemes are dependent on C_{dc}, whose value, if small, will result in larger voltage and current ripples at the DC-link. The larger ripples, when compensated, can be felt more prominently than the case of large C_{dc}. Among the three schemes, influences from the resonant filter in (6.21) are also expected to be stronger than the other two schemes. Explanation of that is related to the avoidance of double amplification of the $2\omega_{out}$ ripple in v_{dc}, caused by the proportional terms in the outer PI and inner PR controllers. Its inclusion will therefore help to reduce the interharmonics significantly, even though a thorough mitigation will still require the inclusion of the other two schemes, especially when using a smaller C_{dc}.

To evaluate the proposed methodology, the drive system shown in Figure 6.11 has been simulated in Matlab/Simulink using the parameters listed in Table 6.3. Simulations were first performed with the methodology turned off, whose obtained waveforms for the motor unbalanced currents at 40 Hz are shown in Figure 6.13(a). These motor currents, consequently give rise to uneven grid input currents, whose spectrum in Figure 6.13(b) clearly shows the presence of interharmonics at 30 Hz and 130 Hz. Simulations were next performed with the proposed methodology turned on and the observed motor currents are plotted in Figure 6.14(a). The spectrum of the grid currents is

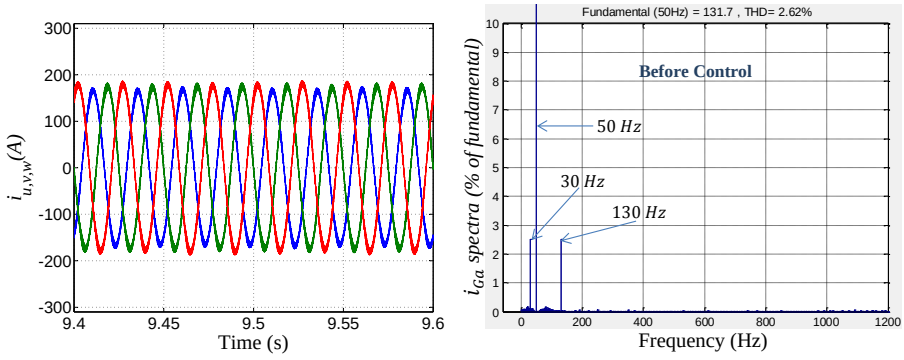


Figure 6.13: *Simulation results at load torque T_L equal to 460 Nm, f_{out} = 40 Hz and with a motor current imbalance of 5% before applying the proposed control strategy. (a) Motor currents. (b) Grid current spectra in common coupling point.*

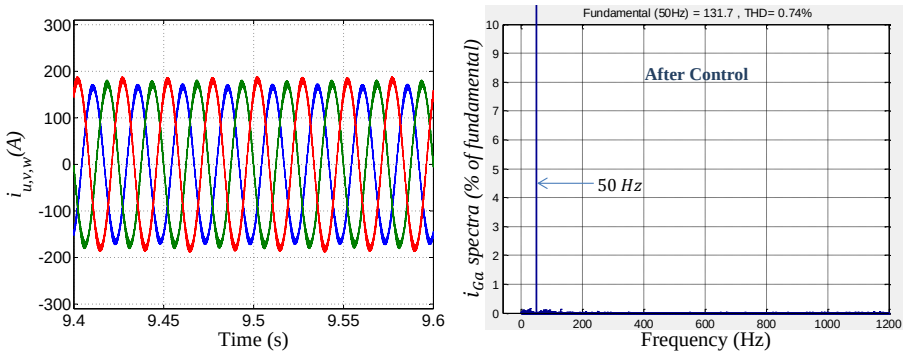


Figure 6.14: *Simulation results at load torque T_L equal to 460 Nm, f_{out}= 40 Hz and with a motor current imbalance of 5% after applying the proposed control strategy. (a) Motor currents. (b) Grid current spectra in common coupling point.*

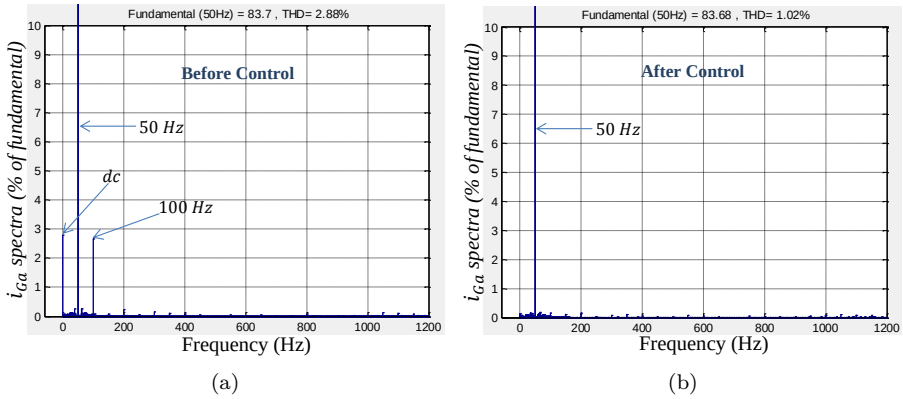


Figure 6.15: *Input current i_{Ga} spectra when the motor input voltage frequency is equal to 25 Hz. (a) Before applying the proposed control strategy. (b) After applying the proposed control strategy.*

given in Figure 6.14(b), which now does not have interharmonics. Such compensation is important, especially with more drives or other AC systems tied to the grid.

In another case, simulations were performed at 25 Hz motor input voltage frequency and the results are given in Figure 6.15. As expected, before applying the proposed control scheme, the input current spectrum shows two interharmonic components at zero and 100 Hz, Figure 6.15(a). The effectiveness of

the proposed method was then examined with the methodology turned on and shows clearly in Figure 6.15(b) that the related interharmonics are removed from the input current, leading to a pure 50 Hz fundamental component.

6.4 Conclusion

In this chapter, the ASD's input current interharmonics mitigation methods were discussed when they are originally caused by the motor current imbalance. It first presented applying an AC-side three-phase active filter, and also, an active DC-link capacitor for removing the interharmonic components in ASD. The DC-link active capacitor can remove the oscillations at the DC-link stage and before their interaction with the drive input-side harmonics. Thus it is not needed to target the interharmonics separately as those required in the case of applying the AC-side active filter. Moreover, the parallel operation of the DC-link compensator in the circuit makes it more promising compared with implementing a DC-link series active compensator. In the case of applying a back-to-back ASD, a control methodology has been proposed to remove the drive input current interharmonics.

Notably, the interharmonic mitigation by active compensation methods is not usually practical, when motor is working at a normal operating condition. In normal condition, the ASD's input current interharmonics contain very low amplitude as well as spreading in a wide frequency range, which makes it very difficult to identify, to detect , and to remove them. In this respect, it is highly recommended to reduce the interharmonics at the first step by finding their sources, and by selecting an appropriate design strategy.

Chapter 7

Conclusion

This chapter summarizes the work, which has been done throughout the Ph.D. project and concludes the main contribution documented in this thesis. Also, some new research perspectives are included for the future work.

7.1 Summary

This project is organized to understand better the origins of the interharmonics in adjustable speed drive applications, which is of a growing concern associated with interharmonic problems in the grid. Also, ongoing discussions on passing some limitations for the interharmonic components has motivated this work, and this investigation was subjected to find possible solutions in such cases.

In Chapter 2, the harmonic interactions, and consequently, the interharmonic distortions were introduced in a double-stage voltage source inverter-fed adjustable speed drive. The investigations were based on a naturally-sampled sinusoidal pulse width modulation technique for the inverter. It investigated how the inverter output harmonics are transferred via the DC link, and are involved in the drive input current distortions. A feasible understanding of the interharmonics location has been obtained based on the drive input-side interharmonics frequency mapping. The interharmonic description and the principles presented launched the basis for the next chapter studies.

Chapter 3 addressed the significance of the interharmonics detection and identification strategies. A rather comprehensive evaluation was performed based on several identification techniques. The FFT-based, the parametric, and the recursive methods were evaluated in terms of the interharmonic detection accuracy. Also, the concept of grouping technique for harmonic and interharmonic measurements was introduced in a standard framework. One of the most common identification errors, the leakage problem, was also addressed with respect to the Rectangular and Hanning windows. Then, a desynchronized process technique was discussed for the accurate interharmonic measurements. However, in order to perform a precise measurement in the study, a 3-second

time width Hanning window with high accuracy was implemented and used.

In Chapter 4, the ASD's input current interharmonic components were comprehensively evaluated with respect to the SPWM, SVM, and DPWM2 modulation techniques. A general study first addressed the interharmonics generation in ASD, while applying the symmetrical and asymmetrical regularly sampled modulation techniques for the inverter. The simulations and experimental validations show higher amplitude interharmonics in the DPWM2 case compared with the two other modulation techniques. Moreover, it is shown that implementing the asymmetrical regularly-sampled modulation may give rise to less interharmonic overlaps compared with the symmetrical one. The results showed that it can provide a good insight into the interharmonics assessment, with respect to the fixed-frequency switching strategies applied on the inverter.

Chapter 5 addresses the effect of ASD's passive filters on the input current interharmonic distortions. The study was performed for the balanced and unbalanced load currents. The interharmonic generation process due to the motor current imbalance was first introduced, and then the effects of different passive filter combinations were assessed. Based on the obtained results, implementing small DC-link filters shows a competitive performance compared to larger filter in terms of the interharmonics generated by motor current imbalance. The investigation was also followed by studying the effect of passive filters on the Total Interharmonic current Distortion TIHD index in the ASD, with a balanced load operation condition. It was shown that selecting the smaller filter components can result in much higher interharmonic distortions compared to the larger filter values.

In Chapter 6, the mitigation of the drive input current interharmonics generated by motor current imbalance was pursued as the most important issue. The investigation was performed based on the partially and fully controlled ASD. In partially-controlled ASD (with the front-end diode rectifier), implementing some active compensators were proposed. The mitigation can be achieved with targeting the associated interharmonics in the AC side by applying a three-phase active power filter. Moreover, a DC-link active capacitor, which can be attached in parallel to the drive DC link, was also proposed to remove the associated oscillations. As it was shown, applying the active DC-link capacitor benefits from targeting the oscillation at the DC-link stage, and before its interaction with the drive input-side harmonic components. Thus, it is not required to remove the interharmonics separately at the AC side. In the case of applying a fully-controlled ASD (with back-to-back converter), a control methodology has been proposed on the front-end rectifier to block the oscillations at the DC link and prevent them from flowing into the grid side. The proposed control strategy actually provides an infinite impedance indirectly at the rectifier level regarding the targeted oscillations.

7.2 Contributions in the thesis

Following contributions can be highlighted in this research project:

Effect of Different Modulation Strategies on ASD's Interharmonics

The effects of naturally-sampled SPWM technique on ASD's interharmonics were already addressed in the literature. However, the significance of the SVM and DPWM2 modulation techniques in motor drive application has not been addressed, and this project has investigated the ASD's input current interharmonics with respect to the symmetrical regularly sampled SPWM, SVM, and DPWM2, and also to the asymmetrical regularly sampled SVM modulation techniques. An interharmonic frequency mapping has been introduced by mathematical analysis in respect to the symmetrical and the asymmetrical modulation strategies. The theoretical analysis, which characterizes the ASD's input current interharmonic frequencies in a case of balanced operating condition, has been then verified by a series of simulation studies and experimental works. A comprehensive comparison of the drive input current interharmonics has been performed with respect to the different modulation techniques.

Passive Filter Effects on ASD's Interharmonics

The thesis has also investigated smaller passive filters in ASD applications which is a global trend, and this research has highlighted the effects of such design on the drive input current interharmonics. A combination of some well-chosen filters was assessed in terms of drive interharmonics at different motor operating conditions. The key role of the drive's passive filters on the harmonic transfer, which gives rise to the interharmonics, was also studied. In this respect, the harmonic interactions with the DC stage were analyzed considering the filters effect, and can be used for future filter design.

Interharmonics Mitigation Methods

This research work proposed some active compensation methods to reduce the interharmonic components generated by ASDs. In the case of partially-controlled ASD with a front-end diode rectifier, the three-phase active filter, which is usually implemented for removing the drive harmonics, can also be used for reducing some interharmonics. Moreover, a DC-link parallel active capacitor was proposed to remove the associated oscillations at the DC-link stage, leading to the drive input current interharmonics mitigation. In the case of applying a fully-controlled ASD with a back-to-back converter, a new control method was proposed to block the DC-link oscillations and not being transfered into the grid.

7.3 Future work

As potential future investigations related with the interharmonic issues in ASDs, the following could be done:

- The interharmonic sources corresponding to some fixed frequency modulation strategies (SPWM, SVM, and DPWM2) have been evaluated in this thesis. Considering the possibility of applying Random Modulation

techniques in ASD applications, the interharmonics evaluation can be subjected to further investigations in these cases. The non-periodic characteristic of the inverter switching function makes it necessary to use the power spectral density analysis for the drive interharmonics assessment.

- The interharmonics identifications in this study were limited to the full-load operating mode of ASD. The experimental work showed also the presence of some interharmonics at low load torque values, other than those demonstrated in the full load condition. Thus, it is worth to investigate the drive interharmonics sources at the lower load torque conditions.

- ASD's passive filters have a key role in magnifying the DC-link oscillations. An optimal design of these filters can contribute to less interharmonics distortions in ASD. Moreover, the filter design can lead to a managed control of the specific interharmonics components. Thus, appropriate design of the drive's filter components in respect to the harmonic and interharmonic distortions, can be subjected to new research studies.

- Several mitigation methods has been proposed to reduce the ASD's input current interharmonics caused by motor current imbalance. It is worth to implement a very low cost interharmonics mitigation method, which can handle the interharmonics with different origins (e.g., motor current imbalance, motor shaft eccentricity and etc).

- Our investigations showed that there are some deviations between the simulation and the experimental results with respect to the interharmonic amplitudes. In the simulation model, switching transient and protect algorithm effects such as blanking time have not been considered. In this respect, the effects of nonlinearities on the drive input current interharmonics can be subjected to further studies.

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Part II Publications

Journal Papers

Two journal papers have been derived from this research project. One paper has been published in IEEE Journal of Emerging and Selected Topics in Power Electronics, and the second paper submitted to the Special Section on Contemporary Issues in Power Quality - IEEE Transactions on Power Delivery is in review process.

J1. Hamid Soltani, Frede Blaabjerg, Firuz Zare, and Poh Chiang Loh, "Effects of passive components on the input current interharmonics of adjustable-speed drives," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 1, pp. 152–161, Mar. 2016.

J2. Hamid Soltani, Pooya Davari, Firuz Zare, Poh Chiang Loh, and Frede Blaabjerg, "Characterization of input current interharmonics in adjustable speed drives," IEEE Transaction on Power Delivery, Under second review.

Conference Contributions

There are four conference papers published (accepted) from this research project.

C1. Hamid Soltani, Poh Chiang Loh, Frede Blaabjerg, and Firuz Zare, "Sources and mitigation of interharmonics in back-to-back controllable drives," in Proceeding of the 16th European Conference on Power Electronics and Applications, 2014, pp. P.1–P.9.

C2. Hamid Soltani, Poh Chiang Loh, Frede Blaabjerg, and Firuz Zare "Interharmonic analysis and mitigation in adjustable speed drives," in Proceeding of the 40th Annual Conference of the IEEE Industrial Electronics Society, 2014, pp. 1556–1561.

C3. Hamid Soltani, Poh Chiang Loh, Frede Blaabjerg, and Firuz Zare "Interharmonic mitigation of adjustable speed drives using an active DC-link capacitor," in Proceeding of the 9th International Conference on Power Electronics – ECCE Asia, 2015, pp. 2018–2024.

C4. Hamid Soltani, Pooya Davari, Firuz Zare, Poh Chiang Loh, and Frede Blaabjerg, "Input current low-frequency interharmonics in adjustable speed drives caused by different modulation techniques," in the Applied Power Electronics Conference and Exposition, 2016, Accepted/In press.

ISSN (online): 2246-1248
ISBN (online): 978-87-7112-521-4

AALBORG UNIVERSITY PRESS