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# ACTIVE STABILIZATION TECHNIQUES FOR CASCADED SYSTEMS IN DC MICROGRIDS

**BY**
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# Active Stabilization Techniques for Cascaded Systems in DC Microgrids

Ph.D. Dissertation

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Curriculum Vitae

**Preface:**

This Ph.D. dissertation entitled “Active Stabilization Techniques for Cascaded Systems in DC Microgrids” has been submitted to the Doctoral School of Aalborg University, in partial fulfillment of the requirement for the Ph.D. degree.

All researches are carried out at the Department of Energy Technology, Aalborg University from July 2018 to June 2021 under supervision of Associate Prof. Mohsen Soltani and co-supervision of Associate Prof. Amin Hajizadeh.

This dissertation has been submitted in the partial fulfillment for the Ph.D. degree. The thesis is based on the published and submitted papers, and parts of the papers are used directly or indirectly in the thesis. The present form of the thesis cannot be openly published, only limited and closed circulation as copyright may not be ensured.

Omid Lorzadeh

Preface

## *English Summary*

In recent years, multi-converter DC power distribution networks or DC Microgrids (MGs) have been extensively used in applications such as more electric aircraft, more electric ships, hybrid vehicles, and data centers. This is owing to high power transfer capacity, no frequency and reactive power control requirements, and avoidance of numerous power conversions provided by these systems. Hence, this has led to the superiority of these types of systems over their AC MGs counterparts in terms of achieving simple control structures and higher productivity. DC/DC conversion cascaded systems (shortened cascaded systems) are known as the prevailing subsystems in DC MG relying on their modularity and high efficiency. Despite the potential instability resulting from interactions between the individually designed feedback-controlled converters in these predominant interconnections, supplying loads in a tightly-controlled form (active loads) such as constant power loads (CPLs) inject a destabilizing effect into the network. CPLs tend to destabilize the system owing to their negative resistance characteristics that cause reduced system damping, limited cycle oscillation and voltage collapse on the DC bus, degraded stability margins, and in the worst case, the shutdown of the whole system.

Consequently, addressing active load's instability effect is one of the most vital issues in obtaining a stable cascaded system, which has lately become an attractive and challenging topic. Although several stabilization techniques have been proposed in this area, most of them suffer from shortcomings and limitations that include the use of complex corrective control structures with various levels of conservatism in the design and satisfaction of stability criteria. Besides, their effectiveness and applicability against unforeseen changes in the network, such as changes in input voltage level and load set, as

well as step changes in the output voltage reference, have not been comprehensively evaluated.

Prompted by the mentioned challenges, this work proposes novel active damping (AD)-based stabilization techniques for suppressing CPL instability of cascaded systems in DC MGs without affecting the dynamic performance of the load-side converter. These proposed design-oriented active stabilization approaches take advantage of simple control structures with straightforward adjustment of a control parameter. The presented AD stabilization methods are tested by Matlab/Simulink in the discrete-time domain and also experimental implementation by dSPACE for three cascaded systems comprising basic DC/DC converters, i.e. Buck, Boost, and Buck-Boost converters loaded with CPLs and resistive load. The results are provided as proof of concept, thus validating the theoretical findings and demonstrating the advantages of the proposed approaches during different operational cases such as input voltage changes, plug and play (PnP) operational of CPLs, and step changes in output voltage references. The outcome of this work proves the effectiveness and operational feasibility of the AD-based stabilization techniques on the cascaded systems feeding multiple CPLs in DC MGs.

## *Dansk Resume*

I de senere år har multi-converter DC strømforsyningsnetværk eller DC Microgrids (MG'er) været meget udbredt i applikationer såsom mere elektriske fly, mere elektriske skibe, hybridbiler og datacentre. Dette skyldes høj effekt overførselskapacitet, ingen krav til frekvens og reaktiv effektstyring og undgåelse af adskillige effektkonverteringer leveret af disse systemer. Derfor har dette ført til overlegenhed af disse typer systemer i forhold til deres AC MG'er-kolleger med hensyn til at opnå enkle kontrolstrukturer og højere produktivitet. DC/DC-kaskade konverterings systemer (kortere kaskade systemer) er kendt som de fremherskende undersystemer i DC MG, der er afhængige af deres modularitet og høj effektivitet. På trods af den potentielle ustabilitet som følge af interaktioner mellem de individuelt design konvertere i disse dominerende sammenkoblinger, levering af belastninger i stramt kontrolleret form (aktive belastninger) såsom konstant effektbelastning (CPL'er) injicerer en destabiliserende effekt i systemet. CPL'er har tendens til at destabilisere systemet på grund af deres negative modstandskarakteristika, der forårsager reduceret system dæmpning, begrænset cyklusoscillation og spændingskollaps på jævnstrømsbussen, forringede stabilitetsmargener og i værste fald nedlukning af hele systemet.

Derfor er adressering af aktiv belastnings stabilitet effekt et af de mest vitale problemer i at opnå et stabilt kaskadet system, som for nylig er blevet et attraktivt og udfordrende emne. Selv om flere stabiliseringsteknikker er blevet foreslået på dette område, lider de fleste af dem med mangler og begrænsninger, der inkluderer brugen af komplekse korrigerende kontrolstrukturer med forskellige niveauer af konservatisme i udformningen og opfyldelsen af stabilitetskriterier. Derudover er deres effektivitet og anvendelighed mod uforudsete ændringer i netværket, såsom variationer i

indgangsspænding og belastningssæt, samt trinændringer i udgangsspændingsreferencen ikke blevet vurderet grundigt. Tilskyndet til de nævnte udfordringer foreslår dette arbejde nye aktive dæmpnings baserede (AD)-baserede stabiliseringsteknikker til undertrykkelse af CPL-ustabilitet af kaskadede systemer i DC MG'er uden at påvirke den dynamiske ydeevne for belastningsside konverteren. Disse foreslåede designorienterede aktive stabiliseringsmidler drager fordel af enkle kontrolstrukturer med ligetil justering af en kontrolparameter. De præsenterede AD-stabiliseringsmetoder testes af Matlab / Simulink i det diskrete tidsdomæne og også eksperimentel implementering af dSPACE til tre kaskadede systemer, der omfatter grundlæggende DC/DC konvertere, dvs., Buck, Boost og Buck-Boost-omformere indlæst med CPL'er og resistiv belastning. Resultaterne tilvejebringes som bevis på konceptet og validerer således de teoretiske fund og demonstrerer fordelene ved de foreslåede tilgange under forskellige operationelle tilfælde såsom indgangs spændings ændringer, tilslut og brug operation af CPL'er og trinændringer i udgangsspændingsreferencer. Resultatet af dette arbejde beviser effektiviteten, og den operationelle gennemførlighed af AD-baserede stabiliseringsteknikker på de kaskadede systemer, der fodrer flere CPL'er i DC MG'er.

## Acknowledgment

At First, I would like to express my great gratitude to my supervisor, Associate Professor Mohsen Soltani for all trust and helps given to me to pursue a Ph.D. He always inspired and encourage me with new ideas during this journey. He has not been only an advisor also as a friend making the work environment more pleasant for me. Also, I am highly indebted to my co-supervisor, Associate Professor Amin Hajizadeh, for help, supports, and valuable comments to ensure the success of my researches on this Ph.D. study.

I sincerely thank my friends and colleagues, Meisam Sadi, Mehdi Nikbakht Fini, Mojtaba Yousefi, Navid Bayati, and Zahra Nourbakhsh Soltani for making enlivening, and interesting times on my Ph.D. journey.

I also like to thank Prof. Hamacher and Dr. Vedran Perić and their team, CoSES, at Technical University of Munich (TUM) in Germany for hosting me during study abroad. Thanks for the hospitality of the CoSES team and for making a successful scientific research for me.

At the end, I would like to say a huge thanks to my family from the bottom of my heart. Thanks, Mehrnaz, my lovely wife, for encouraging me with her patience and kindness as well as my honey girl, Rose, through this way. Thanks, my mother, Farideh, and my father, Ghasem, for trusting me on my ideas and guiding me during tough moments. Also thanks my brothers, Mohammad Ali, and Iman for helping me with my entire life.

I would like to thank God for giving me the strength, and knowledge to undertake this research study and to persevere and complete it satisfactorily. Without his blessings, this achievement would not have been possible.

# Contents

Contents

# Chapter 1
# Introduction

*This chapter gives an introduction, background, motivation, and aims of this thesis.*

## 1.1. Background and Motivation

With the increasing trend of developments in power electronics, modern control technologies, worldwide demand for more and more use of renewable energy sources, and energy storage systems, DC distribution is treated as one of the preferred architectures for power distribution grids [1]-[6]. These systems have the potential for higher efficiency and reliability (by preventing multiple conversion stages), better power transfer capacity of lines, and rapid response compared to their AC counterparts [1]-[6]. In addition to these features, DC distribution systems also offer benefits in terms of the non-existence of reactive power flow and power quality issues as well as the elimination of synchronization problems (due to lack of frequency and phase), leading to non-complexity in control structures and robust performance in comparison with AC-linked systems [1]-[6]. These superiorities have led modern societies to move more and more towards the use of DC distribution with different voltage and power levels in many practical applications [1]-[3],[7] and [8]. Nowadays, modern transportation systems (air, land, and sea), residential and commercial facilities, all new appliances, data centers, telecom systems as well as renewable energy resources increasingly rely on DC power distribution technology [2]. Accordingly, the use of DC at low voltage levels has dramatically increased in these applications, where all of them can be classified under a similar label, i.e., DC Microgrid (MG) [1]. In general, DC MGs can operate on an island or grid- connected modes [1],[2]. The schematic diagram of generic DC MGs is illustrated in Fig.1.1. As seen, in DC MGs,

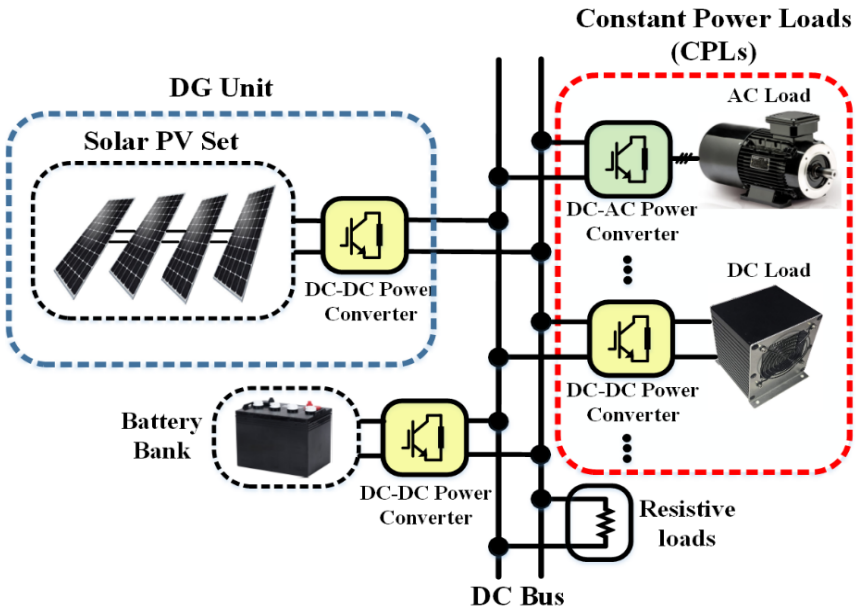



Fig. 1.1 A typical structure of DC MGs.

from the source-side, the distributed generation (DG) units (power sources plus their respective controllable power electronics converters) power is injected into the intermediate DC bus to generate a regulated voltage on it [9]. In terms of loading, besides passive (resistive) loads, active loads are mainly connected to the DC bus through tightly regulated point-of-load converters (POLCs) [9]. Therefore, the cascaded interconnection of source- and load-side subsystems is a prominent configuration in such networks, where switching power converters are usually designed and tested individually with only resistive loads [9]-[13] and [15]. A generic model of such configuration in DC MGs is depicted in Fig. 1.2. In these structures, even if each converter is individually well-designed, it can lead to poor dynamic performance, impedance interactions between the source and load side circuits, and ultimately inject an unstable state into the system [9],[10]. In this regard, POLCs in a multi- converter DC distribution system having a cascaded

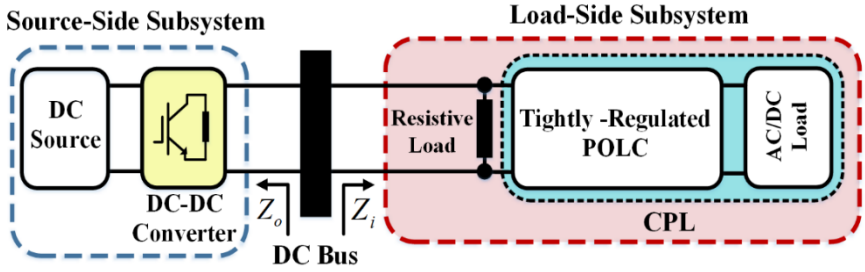



Fig. 1.2 a generic cascaded system.

structure with a rapid that behaves as constant power loads (CPLs) can be considered a clear example of these issues [8]-[10]. CPLs receive constant power from their feeder, regardless of its terminal voltage when the bandwidth and control loop gain of the load converter is adequately grater than that of the source converter [9], [11]. From the point of view of the upstream circuit, the CPL characteristic behaves as a negative resistance [9]. Though the inherent incremental negative resistance feature of the CPL guarantees the fast-dynamic performance of the converter of the load-side, it will jeopardize the stability of cascaded systems [9]-[12],[15]. This instability effect on cascaded systems can cause reduced system damping, limited cycle oscillation and voltage collapse on the DC bus, degraded stability margins, and in the worst case, blackout of the whole microgrid. Therefore, the stability issues and active stabilization solutions for DC MGs under such loads can be an attractive and challenging topic.

## 1.2. Project Objectives

Motivated by the mentioned issues and challenges in the previous section, overcoming CPL instability in the architecture indicated in Fig. 1.2 is one of the key points in obtaining a stable low voltage direct current (LVDC) network or DC MGs. Although several techniques have been presented for active stabilization of the CPL's destabilizing effects in DC MG applications based

on different stability criteria, many of them suffer from shortcomings and limitations. Weaknesses of existing techniques can be included as follows, but not limited to:

- Complex control structures with different control parameters and the use of a high number of measurement sensors.
- High levels of conservatism in designing and satisfying stability criteria.
- Affecting the desirable and fast dynamic performance of the load-side converter.
- Incompatibility, inflexibility, and impracticality for all cascaded systems comprising the basic DC/DC converters (Buck, Boost, Buck-Boost) feeding CPLs (Lack of benefit from a similar control structure).
- Absence of a comprehensive evaluation regarding their effectiveness and dynamic performance under unforeseen changes in the system, i.e., load level (PnP operation), input voltage amplitude, and step changes in the output voltage reference, simultaneously.

Therefore, research to achieve active stabilization approaches for suppressing CPL's instability in DC MGs that well address the limitations and shortcomings of past works remains a critical research gap in this area. Hence, the research hypotheses are as follows:

• It is possible to robustly stabilize with fast dynamic response for the DC-DC cascaded systems with multiple CPLs in DC MGs under anticipated changes in the input voltage, load level, and output reference voltage while maintaining desirable dynamic load performance.

Accordingly, the aims of this project are classified as follows, step by step;

- Investigating the dynamic characteristics of DC MGs and analyzing instability issues.
- Modelling DC/DC conversion cascaded systems with resistive load and CPL in DC MG applications and evaluating dynamic and transient performance under different operational cases.
- Small-signal stability analysis for three DC/DC conversion cascaded systems (Buck, Boost, Buck-Boost converters) with resistive and multiple CPLs, separately and identification of stability conditions for these dominant structures.
- Proposing new active stabilization methods to compensate for the CPL instability effects with the aim of covering the limitations and shortcomings of existing works.
- Experimental implementation of proposed stabilization schemes to confirm their feasibility in real life and to validate theoretical findings.

## 1.3. Outline of the thesis

The outcome of this Ph.D. thesis is expected to be a collection of related published/submitted articles during the performed project period. In addition, the structure of this thesis is as follows:

**Chapter 1.** This chapter briefly introduces stability issues and their challenges for DC MGs, motivation, research objectives, list of published journals and conference papers.

**Chapter 2.** First, this section begins by describing the dynamic characteristics of DC MGs and defining the problem for the stability of these systems. Then, a literature review on the active stabilization solutions, the techniques functional comparison, and existing works for suppressing DC MG's destabilizing effects induced by CPLs are carried out.

**Chapter 3.** presents a new source-side AD-based stabilization method for cascaded systems in DC MGs. This stabilizer approach is realized by a virtual series *RC* damper in parallel with the source converter's capacitor for suppressing CPL destabilizing effect without compromising the dynamic performance of the load converter. Using this design-oriented AD control scheme that takes advantage of an easy control structure with a simple adjustment of the control parameter, the system stability is ensured. The superiority and effectiveness of the proposed stabilizer technique in terms of the transient and dynamic performances, reference voltage tracking, and robust stability compared to other methods that are close to ours, are tested and validated by simulations and experimentation implementations. The content of this chapter has been presented in the first journal paper that is published in IEEE Transaction of Energy Conversion.

**Chapter 4.** introduces a novel active stabilization method for cascaded systems in DC MGs using an adaptive parallel-virtual-resistance (APVR) control scheme. The presented load adaptive-based source-side AD stabilizer approach is achieved by positive proportional-derivative feedback of the equivalent load current with an intrinsic self-tuning control parameter without affecting the dynamic performance of the load set. The design-oriented APVR control strategy ensures stability and dynamic performance of the system through actively compensating the CPLs (active loads) destabilizing effect by utilizing a simple control structure and easy control parameter adjustment. Moreover, the high robustness and effectiveness of the offered active stabilization idea against unforeseen variations in input voltage level and plug-and-play (PnP) of CPLs (load changes) without knowledge of their value are verified. Simulation and experimental results have been validated the applicability and flexibility of the proposed stabilizer technique by applying and testing on the three cascaded systems containing basic DC/DC converters

(Buck, Boost, and Buck-Boost) supplying CPLs in DC MG. The content of this chapter has been reported in the second journal paper that is under review in IEEE Journal of Emerging and Selected Topics in Power Electronics.

## 1.4. List of publications

The following is a list of papers published/ submitted during the Ph.D. study.

Journal Papers

**J1.** O. Lorzadeh, I. Lorzadeh, M. Soltani and A. Hajizadeh, "Source-Side Virtual RC Damper-Based Stabilization Technique for Cascaded Systems in DC Microgrids," in IEEE Transactions on Energy Conversion, doi: 10.1109/TEC.2021.3055897. (Published)

**J2.** O. Lorzadeh, I. Lorzadeh, M. Soltani, A. Hajizadeh, and K. Jessen "Active Load Stabilization of Cascaded Systems in DC Microgrids Using Adaptive Parallel-Virtual-Resistance Control Scheme," IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021. (under review).

Conference

**C1.** O. Lorzadeh, I. Lorzadeh, M. N. Soltani, and A. Hajizadeh, "A novel active stabilizer method for dc/dc power converter systems feeding constant power loads," in 2019 IEEE 28th International Symposium on Industrial Electronics (ISIE), pp. 2497–2502. IEEE, 2019.

**C2.** O. Lorzadeh, I. Lorzadeh, M. N. Soltani, and A. Hajizadeh, "H infinity-based robust controller for step-down non-isolated dc/dc converter loaded by constant power load in dc microgrids," in 2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), pp. 1–6. IEEE, 2020.

The chronology of the papers follows Fig.1.3.

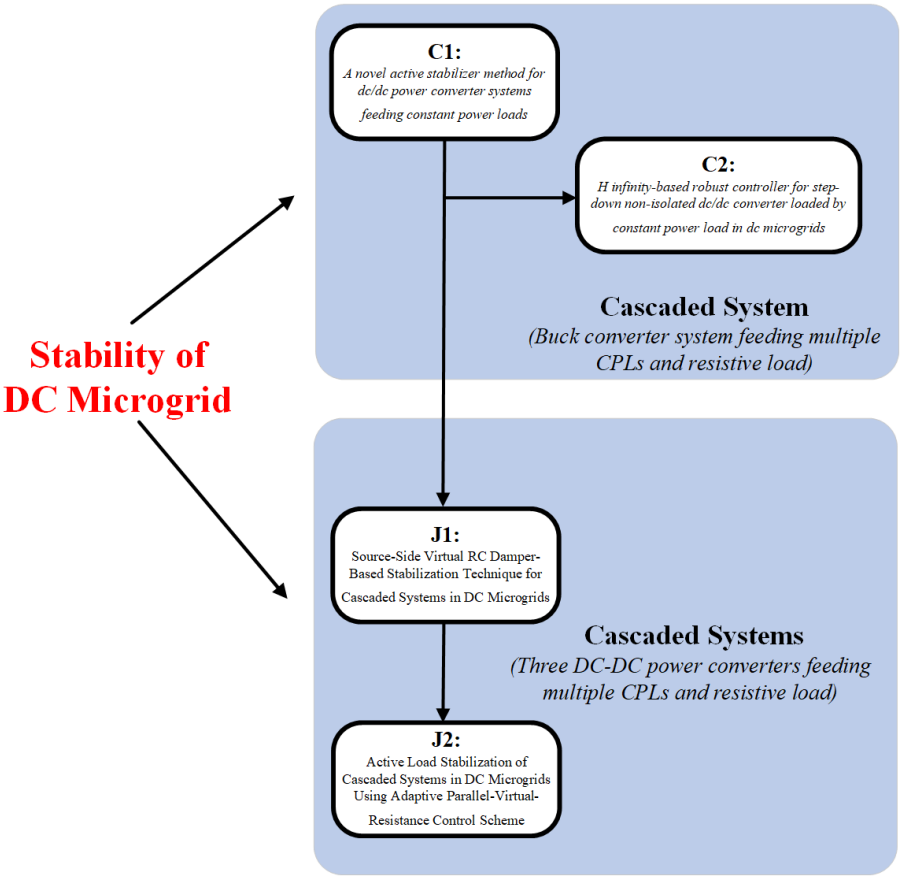



Fig. 1.3 Chronology of papers

## 1.5. Scientific contributions

- The transient and dynamic behaviors, as well as the stability of three basic DC/DC converter systems feeding resistive load and multiple CPLs (cascaded systems) in DC MGs, are separately tested and analyzed under four performance scenarios as follows:

I. Without and with applying proposed stabilization methods.

II. Sudden variations in the input voltage amplitude.

III. Unforeseen changes in load level (CPL power rating).

IV. Step changes in voltage level of the output reference.

- Using a similar control structure with only various analytical concepts for the stability of these systems, which confirms the high compatibility and flexibility of the proposed stabilization methods.
- Three separate experimental setups have been built and used to show the feasibility of the proposed active stabilization approaches for these predominant structures in DC MGs.
- The effectiveness, robustness, and acceptable dynamic performance of the offered active stabilization schemes are validated under the above scenarios by simulation and experimental results.
- The superiorities of the proposed stabilization ideas compared with other stabilization methods, which are close to our work, are proven by a comprehensive performance comparison.

Chapter 1

# Chapter 2
# Stabilization of DC Microgrids

## 2.1. Dynamic Characteristics of DC Microgrids

Commonly, using dynamics corresponding to time constants ranging in different time scales can identify stability issues in DC MGs. At longer scales, which sometimes vary from seconds to hours, the need to match the powers produced and consumed is a worrying factor in stability in these ranges [1],[2]. This means that from a static point of view, the power generated must match the energy consumed in the loads and sources, while dynamically, the response ramps of the power sources must be able to track load changes [1],[2]. In static and dynamic terms, these stability issues related to the matching of production and demand are still essentially similar to the stability concerns noticed in AC power systems and MGs. The usual method to solve these stability issues is to add energy storage [1],[13], which can behave as temporary sources by discharging and charging dependent on power demands.

As discussed, stability concerns related to mismatching of the power generation and consumption are accounted as common issues in AC and DC MGs [1],[9], and [11]. However, shorter time scale-based stability issues more commonly occur in DC MGs compared to AC power systems because these concerns arise in the presence of loads linked to the tightly-regulated power converters (Point-of-Load converters) acting as CPLs [1]-[3],[11]-[15]. Therefore, the framework of this work has been focused on the discussion of DC MGs stability in the presence of CPLs and introducing appropriate approaches to suppress the effect of instability injected into the system by these load types.

## 2.2. Challenges of stability in DC Microgrids

The purpose of this section is to describe in detail the instability issue originated by CPLs for the cascaded configuration shown in Fig. 1.2, which introduces severe challenges to the DC MG [1]-[6],[9]-[13].

### 2.2.1 Problem Definition

The essential challenge in the stability issue of multi-converter LVDC networks emerges when individually well-designed switching converters are tested on the grid. This is because connecting them to other circuits will no longer maintain the stability conditions of closed-loop converters designed as a freestanding device and may impose unforeseeable dynamic responses on the system [9],[12], and [15]. Also, these predominant structures in DC MG applications are commonly loaded with large active loads such as motor drives or electronic loads, which all these loads tend to be energized by POL converters [3],[16]. These loads act as instantaneous CPLs when tightly-controlled by their respective converters, which have a rapid dynamic response with minimal output voltage ripple [9]-[12],[17], and [18]. In this case, when the bandwidth and control loop gain of the load side converter is adequately greater than that of the converter at the source side [9],[11], CPLs draw constant power from their upstream circuit, regardless of its terminal voltage [14]-[16]. CPLs introduce incremental negative resistance characteristic for their upstream circuit. It is worth noting that in the design of switching converter, the important aim of the designer is to obtain a high-efficiency system, i.e.,

$$P_o = P_{in} = V_{in} I_{in} \tag{2-1}$$

Where $V_{in}$, $I_{in}$, $P_{in}$, and $P_o$ are the input voltage, input current, input power,

and output power of load converter, respectively. After adding the disturbances in (2-1) and considering the behavior of the load converter as CPL [16],[19],

$$P_o + \hat{p}_o = (V_{in} + \hat{v}_{in}) \cdot (I_{in} + \hat{i}_{in}) = Cons \cdot \tag{2-2}$$

Replacing (2-1) to (2-2) and neglecting the second-degree disturbance term,

$$\hat{Z}_{in} \triangleq \frac{\hat{v}_{in}}{\hat{i}_{in}} = -\frac{V_{in}^{\ 2}}{P_o} \cdot \tag{2-3}$$

According to (2-3), though the inherent negative resistance property of CPL ensures the fast-dynamic performance of the load converter, it will negatively affect the stability of the cascaded systems [2],[9],[19], and [20]. Hence, if the network is not supported with a suitable stabilization scheme over during the transient and any unwanted disturbance in the system, the voltage will go zero as the current goes to infinity, and vice versa [16],[17]. Finally, the system state variables will no longer return to equilibrium and the system will become unstable. Therefore, the major effects of CPL instability on cascaded systems in DC MGs can cause reduced system damping, limited cycle oscillation and voltage collapse on the bus voltage, degraded stability margins, and in the worst case, the whole system will shut down [1]-[4],[9]-[11]. Consequently, suppressing CPL instability in the structure illustrated in Fig. 1.2 is one of the vital concerns in obtaining a stable LVDC network. In addition, the accepted control approach must be robust enough to ensure the stability of the system against anticipated variations while simultaneously maintaining fast dynamic performance [9]-[16].

## 2.3. Active Stabilization of a cascaded system with CPL

### 2.3.1 Literature Review

In this part, a review of the literature presents on compensation for the destabilizing effects caused by CPLs in cascaded systems in DC MGs. In this way, several methods have been accomplished to mitigate CPL instability in cascading systems in accordance with the different stability criteria, [4]-[19], and [32]. The main concept behind these approaches is the effective improvement of the system damping rate by some modifications that can be commonly categorized into three zones of system-level compensation, namely source-level, load-level or the use of additional circuits at the intermediate level [9],[11],[24]-[26], and [31]-[42]. To fulfill this purpose, various solutions have been performed, which are based on passive (hardware) [33]-[35], and active (software) damping methods [9],[11],[16],[19],[24]-[26],[31]-[32], and [36]-[42]. Passive damping methods are easily realized by passive components to the network. However, system performance and efficiency under these approaches inevitably deteriorates due to the increased size, cost, weight, power dissipation, and decreasing the system bandwidth [2],[9],[16]. In contrast, active damping (AD) techniques with having a high flexibility and efficiency present adequate damping rate for the system control strategy through dynamic modifications [9],[16]. The control concept for these methods is based on satisfying the stability criteria for cascaded systems with emphasis on the modification of $Z_{in}$ (input impedance of the load-side circuit) or/and $Z_o$ (output impedance of the source-side circuit). It should be noted that when the upstream circuit of the CPL is uncontrollable, the AD control solutions at the load-side and intermediate levels are considered as executable options. In load-side compensators, to mitigate CPL effects, $Z_{in}$ is modified by injecting a current or power stabilizing signal into the load converter control loops [16]. However, the CPL control loop will be adversely affected by the dynamics of the AD stabilization strategy and as a result, it cannot maintain its

desirable and fast performance [2],[9]. In intermediate-side AD compensators implemented by an additional active damper between the source and load subsystems, stabilization is realized through effective shaping of $Z_{in}$ or/and $Z_o$ [9],[16]. Although these approaches maintain the network modularity feature, they can impose negative effects on the system, such as increased costs, system complexity, and energy loss [2],[9],[21]. The source-side AD methods dynamically modify $Z_o$ either by adding an ancillary effective damping loop to the source converter [9],[11], [19],[31],[32],[36], and [38] or by increasing the control loop bandwidth of it [24]. Therefore, in these approaches, since overcoming CPL destabilization effect in the cascaded systems is achieved by modifying the control structure of the converter of source-side, the favorable dynamic performance of the load converter will not be jeopardized [2],[9], and [36]. Accordingly, the source-side-based active stabilizers are usually more preferred by researchers and designers over the AD stabilization approaches at the load side [9],[11]. In [31], a source-side AD control scheme is proposed for cascaded systems with CPL in DC MGs, where the system stability condition is satisfied by enhancing damping rate via the virtual insertion of a resistance in series with the inductor corresponding to the source converter [31]. However, due to the inherent shortcomings of the presented idea in [31], including the limited stable band to increase the damping rate and the restriction in the value of the virtual maximum resistance [9], dynamic and transient performance under different performance conditions cannot be appropriately guaranteed. In general, many of the impedance-based active stabilization strategies that have been proposed to date have complex control structures with different levels of conservatism in the design and realization of the stability criteria [9],[16]. In addition, their

effectiveness and dynamic performance against unforeseen changes in the cascaded system has not been evaluated holistically [9],[11], and [31].

Motivated by these issues, this work proposes novel design-oriented source-side active stabilization schemes for stabilizing cascaded systems with CPLs in DC MGs without negative impact on the favorable performance of the load converter. These AD control strategy-based stabilizer techniques utilize simple control structures with straightforward control parameter tuning to achieve a reliable and robust stable level. The flexibility, and applicability, of these control schemes will be well-demonstrated by applying to three cascade systems consisting of basic DC/DC converters (Buck, Boost, and Buck-Boost) supplying multiple CPLs and resistive loads. Effectiveness and robustness of the active stabilizer approaches will be confirmed by simulation and experimental results.

# Chapter 3

# Source-Side Virtual *RC* Damper-Based Active Stabilization Strategy

*Based on JP1, this chapter proposes new source-side active stabilization scheme for DC cascaded systems in DC MGs*

This chapter presents a new stabilization approach based on source-side AD control scheme to overcome the CPL instability effects for DC cascaded systems in DC MGs, which has been published in [9].

## 3.1. Methodology

As discussed in the previous chapter, compensating the active load instabilities (CPLs) in the configuration illustrated in Fig. 1.2 is one of the key subjects in obtaining a stable DC MG and also a desired voltage on the DC bus. Therefore, this chapter presents a novel virtual series *RC* damper that is placed in the output of the source-side subsystem without affecting the favorable performance of the load converter. The presented active stabilization strategy is achieved by feeding back the capacitor current source converter via a precise and well-designed proportional term [9]. Using this design-oriented AD technique that uses a easy control mechanism with simple control parameter setting (see Fig. 3.1), stability and dynamic performance of the system are ensured in a rigorous deterministic way [9]. In the following, the main advantages and new contributions of the proposed active stabilization method are presented, which completely covers the deficiencies of the existing techniques and shows outstanding performance in comparison with them.

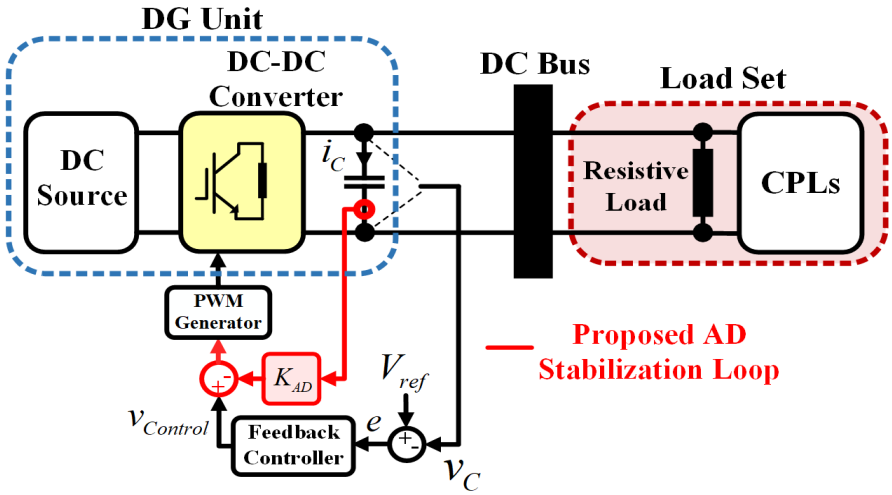



Fig. 3.1. The proposed control strategy based on virtual *RC* damper applied to the cascaded systems with multiple CPLs and resistive load in DC MG.

### 3.1.1 Advantages and Main Contributions

*1) Easy control mechanism with simplicity in control parameter adjustment* [9]

Using these competencies, it is easy to explore the possibility of generalizing this control approach for more complicated DC MGs at source level.

*2) Operational ability with high flexibility and compatibility* [9]

This privileged feature is since the proposed active stabilization technique with a same control scheme and only with different analytical concepts is well-applicable in the three main cascaded systems with multiple CPLs in the DC MGs [9].

3) Without any adverse effects on *the desirable dynamic performance of the load-side converter* [9]

Verification of the effectiveness of a control technique in overcoming exclusively unfavorable effects without adversely affecting other optimal system conditions is an important and vital factor. Since the proposed stabilizer

control strategy is created by modifying the source converter's voltage control signal, the CPL destabilizing effects are omitted without adverse effect on the dynamic performance of the load converter [9].

4) *High robustness versus unanticipated changes in the system (changes in input Voltage level, load changes (power rating in CPLs), and step change in reference voltage)* [9]

The presented AD control approach without the need for new information from the network shows high robustness with admissible transient and fast dynamic responses to possible unforeseeable changes in the system [9].

## 3.2. Proposed Virtual *RC* Damper-Based Active Stabilizer Method for Cascaded Systems in DC MGs

In this part, given the system dynamics, the stability issue of the cascaded systems comprising the DC/DC converters supplying multiple CPLs and resistive loads is individually analyzed [9]. Besides, the principles of control idea and its operation as well as the circuit physical concept created by the suggested stabilizer scheme for these systems in DC MGs, have been theoretically analyzed. Effectiveness, and robustness of this technique are validated by simulation and experimental results [9]. It is worth mentioning that all DC/DC converters supplying CPLs that are operating in continuous conjunction mode (CCM) have unstable performance under both voltage mode control (VMC) and current mode control (CMC) [2],[9]. Therefore, owing to the simplicity in design and execution as well as the assessment of the presented active stabilizer strategy in the worst operating conditions from the point of view of stability, the performance of the source side converters is considered in CCM and under VMC [9]. However, the proposed method can also be well-accomplished for these systems in CMC.

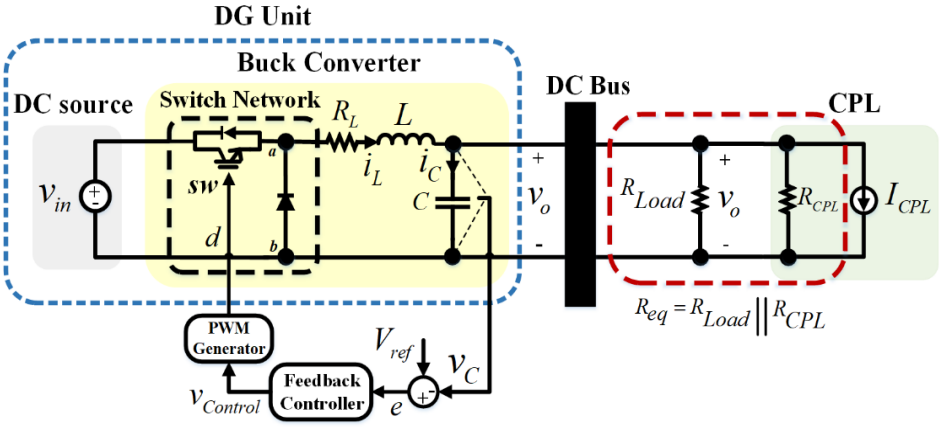



Fig. 3.2. A DC/DC buck converter feeding CPL and resistive load in cascaded form [9].

## 3.2.1 DC/DC Buck Converter feeding Resistive Load and CPLs

### 3.2.1.1 Modeling and Stability Analysis

Fig. 3.2 illustrates a DC/DC buck converter system loaded by CPLs and resistive load. In this configuration, CPL has been modeled by its small-signal circuit consisting of a negative resistance ($R_{CPL}$=-$V^2$/$P$) in parallel with an independent current source ($I_{CPL}$=2$P$/$V$), where $V$ and $P$ are terminal voltage and power of the CPL for a certain operating point, respectively [9]. Though $I_{CPL}$ does not impact on the system stability, $R_{CPL}$ reduces system damping and tries to impose instability on the system [9]. $L$ and $C$ are the inductor and capacitor of the source-side converter, $R_L$ is the inductor's inherent resistance, $V_{in}$ is the input voltage, $R_{eq}$ is the small-signal equivalent load resistance. To extract the linearized circuit averaged model of the cascaded system shown in Fig. 3.2, the averaged switch modeling technique is applied into the system with subintervals during each switching period [9]. The process of

implementing the averaged switch modeling method is summarized in the following steps.

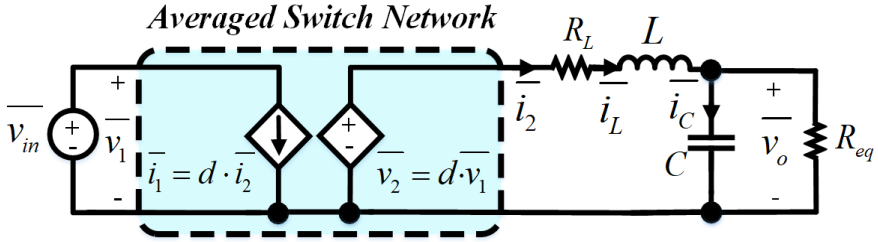



Fig. 3.3. The averaged time-invariant network of Fig. 3.2 (Step 1) [9].

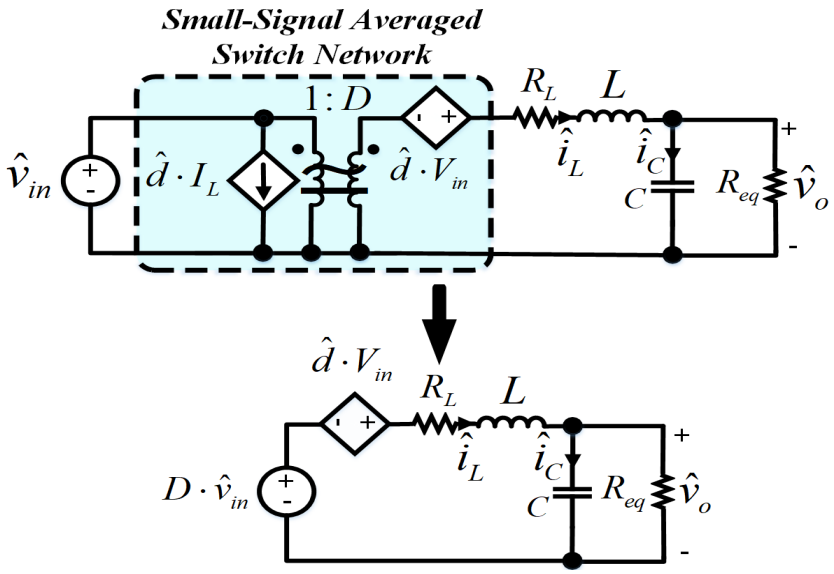



Fig. 3.4 Simplified averaged model of. 3.2 (Step 2) [9].

***Step 1.*** The switch network shown in Fig. 3.2 can be modeled a as two-port network with four variables, called, $v_1$, $i_1$, $v_2$, and $i_2$ [9],[43]. Two of these variables can be random candidate as independent inputs ($v_1$, $i_2$) and the remaining two quantities are then considered as dependent outputs ($i_1$, $v_2$)

[43],[9]. The only action necessary at this stage is to calculate the average values of the dependent sources, where they are represented by $\overline{x}$ .

***Step 2.*** First, in this section, suppose that the parameters of the averaged system model are equal to the corresponding dc values, *X,* plus small ac variations, $\tilde{x}$ . As specified in Fig. 3.4, by replacing these perturbed signals in the model demonstrated in Fig. 3.3, and disregarding the second-order terms derived from the multiplication of ac values, the small-signal averaged model is achieved [9].

Consequently, the small-signal control-to-output transfer function and its related poles can be readily derived as (1) and (2), respectively.

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_{in}}{LC \cdot s^2 + (R_L C + \frac{L}{R_{eq}}) \cdot s + (1 + \frac{R_L}{R_{eq}})} \cdot \tag{3-1}$$

$$P_1, P_2 = \frac{-(\frac{L}{R_{eq}} + R_L C) \pm \sqrt{(\frac{L}{R_{eq}} + R_L C)^2 - 4LC(1 + \frac{R_L}{R_{eq}})}}{2LC} \cdot \tag{3-2}$$

Since $R_{eq} \langle 0$ and $\left|R_{eq}\right| \rangle R_L$ (real condition), due to the presence of a complex conjugate pole pair in the right half-plane (RHP), the system operation will be in an unstable position [9]. Hence, by applying Routh's stability criterion for (1), the stability condition for the system is satisfied through the realization of the following inequality [9].

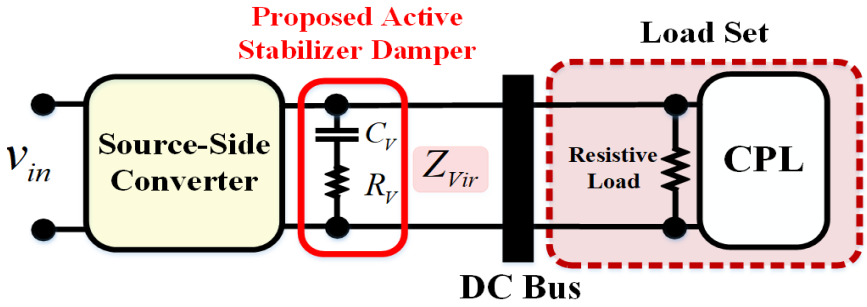



Fig. 3.5. control realization of the presented AD control scheme [9].

$$R_L C \rangle \frac{L}{\left|R_{eq}\right|}. \tag{3-3}$$

Evidently, $R_{eq}$ cannot be changed flexibly for specific CPL and restrictions on the $R_{Load}$ control [9]. Therefore, it can be concluded that to satisfy (3), one of the $LC$ filter parameters should be adjusted properly, that is, either increasing $R_L$ or $C$, and or decreasing $L$. Generally, $L$ is usually chosen to meet other design requirements, like CCM, and the favorable inductive current ripple magnitude [43]. Hence, as is clear from (3), this case does not match the stability condition mentioned for the inductor value. Also, actively increasing $R_L$ cannot be a proper solution to overcome CPL instability effects under different loading cases [9],[31]. As a result, in this case, the only parameter that can be freely adjusted is $C$. However, increasing $C$ alone guarantees the stability performance of the system in exchange for slowing down the dynamic response. Consequently, as shown in Fig. 3.5, to ensure stability of the system, improved dynamic performance and enhanced damping, the virtual insertion of a series *RC* damper into the source's converter output would be a great choice [9].

### 3.2.1.2 Control Realization

a) Circuit Physical Meaning

This section describes in detail how to influence and design the suggested AD-based stabilizer scheme for stabilizing buck converter system supplying multiple CPLs in DC MGs.

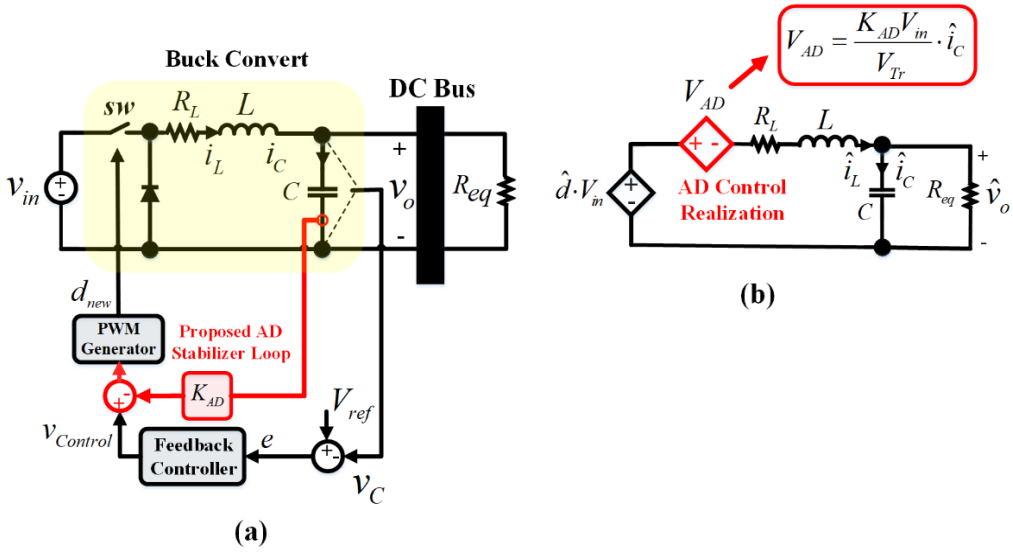



Fig. 3.6. The proposed AD control strategy for the buck converter feeding CPLs and resistive load. (a) Circuit model. (b) Modified small-signal averaged circuit [9].

In this regard, Fig. 3.5(a) illustrates the circuit schematic of the cascaded system shown in Fig. 3.2 considering the suggested AD control strategy. As seen, this active stabilizer approach is realized by the proportional feedback of the source converter capacitor current and subtracting it from the voltage control signal [9]. Thus, by substituting $\hat{d}_{new} = \hat{d} - (K_{AD} \cdot \hat{i}_C / V_{Tr})$ in lieu of $\hat{d}$ in Fig. 3.4, the simplified small-signal average model is modified by neglecting the ac term of input voltage source (see Fig. 3.5(b)). It is well understood that the presented AD technique behaves as a dependent voltage source for suppressing CPL's instability effect by dynamically modifying the converter

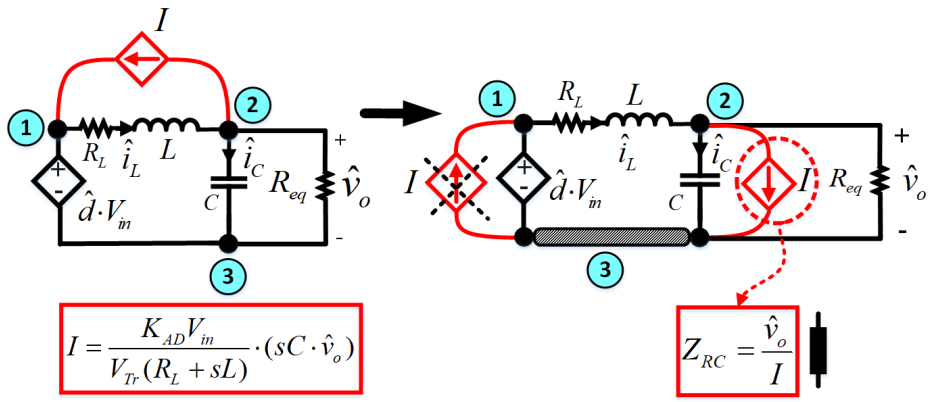



Fig. 3.7. Another analytical commentary of Fig. 3.5(b).

CPL's instability effect by dynamically modifying the converter output voltage. As can be seen from Fig. 3.5 (b), the proposed AD control scheme presents an interesting concept of a physical circuit, the result of which is shown graphically in Fig. 3.6. This outcome is achieved based on the circuit analysis, the process which is summarized step-by-step as bellow [9]:

***1)*** *Conversion of the Thevenin circuit including the voltage source* $V_{AD}$ *and the impedance* $R_L - L$ *to the related Norton equivalent circuit.*

***2)*** *Deleting the dependent current source, I, between nodes 1 and 2 and transferring it from node 2 toward node 3 and finally to node 1.*

At this point, the dependent current source parallel to the voltage source can be neglected [9].

***3)*** *Conversion of the dependent current source to an impedance.*

According to one of the efficient rules used in circuit analysis, which states: "Each dependent current source that depends on its voltage can be modeled as an impedance", the proposed active stabilization technique injects a virtual series RC damper in parallel to the converter output (see Fig. 3.7) [9].

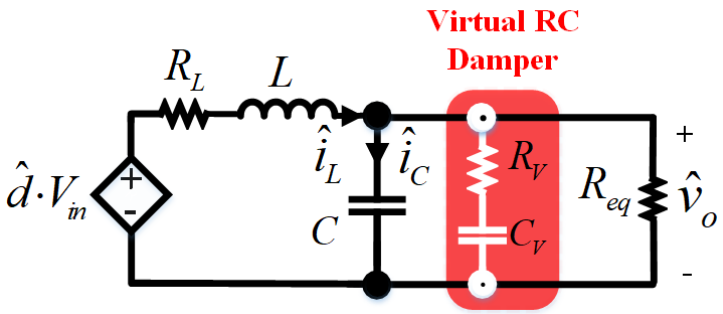



Fig. 3.8. The circuit physical meaning of the suggested AD control strategy for to the buck converter feeding multiple CPLs and resistive load.

In this way, $R_V$ and $C_V$ can be readily achieved as [9]

$$\frac{\hat{v}_o}{I} = \frac{LV_{Tr}}{K_{AD}CV_{in}} + \frac{1}{s}\left(\frac{R_L V_{Tr}}{K_{AD}CV_{in}}\right) = R_V + \frac{1}{sC_V} \tag{3-4}$$

b) Choosing an Effective AD Term ( $K_{AD}$ )

As obvious from (4), since the effect of resistance term ( $R_V$ ) is more negligible than capacitance term ( $C_V$ ) at around DC frequency, the system's equivalent capacitance can be regarded with an acceptable approximation as $C + C_V$ [9]. In this regard, as discussed in the previous section, by increasing the equivalent capacitor of source-side output, i.e., (Increasing $C_V$ ), the damping rate can be significantly improved to stabilize the system. It is important to note that in order to avoid slowing down the response of the system owing to increased capacitance alone, the existence of the term resistance in the damper branch is vital. Considering (3) and the stability analysis discussed, the minimum required capacitor to compensate instability effects induced by CPL is obtained as [9]

$$C_{\min} = \frac{L}{R_L \left| R_{eq} \right|}. \tag{3-5}$$

Therefore, the damping gain ( $K_{AD}$ ) must be chosen effectively so that $C_V$ is much larger than $C_{V,\min}$ , i.e. [9];

$$C_{V,eff} \gg C_{V,\min} = (C_{\min} - C) \tag{3-6}$$

Whereby, given the importance of choosing a suitable and optimal $K_{AD}$ for offsetting the CPL instability, the design process algorithm is outlined below;

***Step 1)*** *Computing the* $C_{\min}$ [9].

Given the value of $\left| R_{eq} \right|$ at the desired output voltage, the $C_{\min}$ required to meet the system stabilization conditions is calculated by (3-5) [9].

***Step 2)*** *Computing the* $C_{V,\min}$ .

In this step, minimum value of admissible virtual capacitor, $C_{V,\min}$ , is achieved by $C_{\min} - C$ .

***Step 3)*** *Computing the* $K_{AD,\min}$ .

With obtaining of $K_{AD,\min}$ by (3-7), a virtual series *RC* damper ( $C_{V,\min}$ and $R_{V,\max}$ ) can be realized [9].

$$K_{AD,\min} = \frac{C_{V,\min} R_L V_{Tr}}{C V_{in}}. \tag{3-7}$$

***Step 4)*** *Choosing an effective* $K_{AD}$ ( $K_{AD,eff}$ ).

To reach a robust level of the system with an acceptable damping rate and desirable dynamic performance along with a safe phase margin, an effective choice for the AD controller gain must be accomplished by the designer. This represents high flexibility in choosing $K_{AD}$ an allowable stable band complies with design requirements [9].

It must be acknowledged that since $K_{AD}$ has a reverse dependence on $V_{in}$ and $\left|R_{eq}\right|$, it shall be set much larger than $K_{AD,\min}$ to attain high robustness against descending changes of those agents. This indicates that only in the initial $K_{AD}$ adjustment requires to know $V_{in}$ and the equivalent load set. As a result, with unforeseen changes in these factors, stability can be well guaranteed only by designing the $K_{AD,eff}$ without knowing their new values[9].

It should be noted that the digital implementation of the proposed active stabilizer loop is an important subject that must be considered. Indeed, in practice, the factors influencing digitally-controlled systems include pulse width modulation (PWM) and computational delays [9],[16],[44]. Given that the synchronous sampling approach is commonly applied to the digitally-controlled systems, one sampling period $T_s$ for computation delay effect and half of the sampling period for PWM delay caused by the zero-order-hold (*ZOH*) effect are considered. These delays are accomplished in the control loop of the digitally-controlled converter at the output related to the difference between the presented AD loop and the digital PI controller's output via the cascaded connection of $Z^{-1}$ and *ZOH* blocks [9]. This phase lag effect owing to delay factors yield a decrease in the phase margin in the high-frequency range. Therefore, in the low-frequency range and the small value of $T_s$, the

virtual $RC$ damper-based control scheme will not be affected by the delays effect, and can only limit the upper band of $K_{AD}$.

Table 3.1. The Parameters of the Cascaded Systems with CPL and resistive load [9].

| Source-Side Converter | $L$ | $C$ | $R_L$ | $R_{Load}$ | $P_{CPL}$ | $V_{in}$ | $V_o$ | $D$ |
|---|---|---|---|---|---|---|---|---|
| **Buck** | 20 mH | 350 $\mu$F | 45 m$\Omega$ | 470 $\Omega$ | 2250 W | 200 V | 150 V | 0.75 |
| **Boost** | 2.4 mH | 750 $\mu$F | 5 m$\Omega$ | 200 $\Omega$ | 2250 W | 100 V | 150 V | 0.33 |
| **Buck-Boost** | 2.4 mH | 750 $\mu$F | 5 m$\Omega$ | 200 $\Omega$ | 1800 W | 120 V | 150 V | 0.55 |

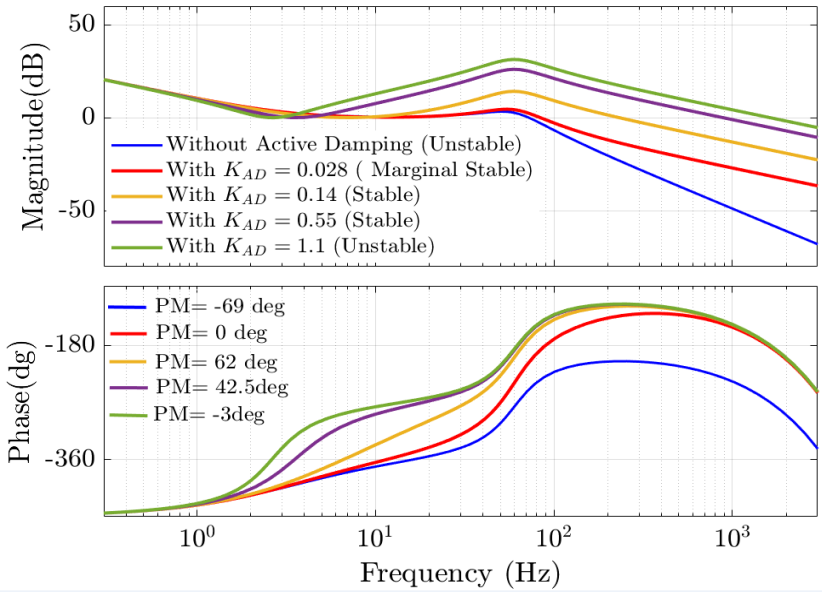



Fig. 3.9. Bode analysis of the open-loop gain of $\hat{v}_o / \hat{d}$ related to the buck converter supplying CPL. Red line: $C_{V,\min} = 43.2mF$, $R_{V,\max} = 10.2\Omega$ ; Yellow line: $C_V = 5C_{V,\min}$, $R_V = 0.2R_{V,\max}$ Purple line: $C_V = 20C_{V,\min}$, $R_V = 0.05R_{V,\max}$ [9].

Bode analysis of the open-loop gain corresponding to the control-to output of Fig. 3.6(a) is plotted in Fig. 3.8 given the relevant delays and the parameters given in Table I. As seen from Fig.3.8,

$$\angle\left[e^{-jT_{Sw}}G(s)\right]=-\pi \tag{3-8}$$

$$\left|e^{-jT_{Sw}}G(s)\right|=1 \tag{3-9}$$

where

- $G(s)=\frac{\hat{v}_o}{\hat{d}}(s)\Big|open-loop=e^{-jT_{sw}}\cdot\left[Eq.(1)\right]\cdot\left(G_{AD}(s)+G_{PI}(s)\right)$,
- $G_{AD}(s)=s\cdot K_{AD,\max}.C$ : (AD Controller)
- $G_{PI}(s)=K_P+\frac{K_I}{s}$ : (PI Controller)

the system reaches marginal stability status for the minimum amount of AD gain ( $K_{AD,\min}$ ) [9]. As the $K_{AD}$ increases, the damping rate enhances, which indicates an improvement in the system phase margin. Thereby, the stability of the closed-loop control system is also guaranteed. However, due to the effect of considered delays in the digital control system, increasing the $K_{AD}$ from a certain value leads to gradually decreasing the phase margin, and ultimately, the system approaches instability. Therefore, the allowable stable band can be defined for $K_{AD}$ as $\left[K_{AD,\min},K_{AD,\max}\right]$. The value of the lower band was obtained by (7) and upper band that defined as the maximum amount of the allowable damping gain can be easily derived by solving (8) and (9). Then, $K_{AD,\max}\cong 0.98$ is attained through substituting the parameters of Table. 3.1 in the expressed equations and fulfilling them simultaneously. Consequently, the permissible stable band is specified as $\left[0.028,0.98\right]$, which well confirmed the results achieved from Fig. 3.8. In general, it should be mentioned that the aim of an efficient design is to reach a robust system with effective damping rate and desirable dynamic performance, as well as a safe phase margin. Therefore, in this regard, effective selection of $K_{AD}$ in

order to meet the targets of an efficient design will be very important. This in turn indicates the high flexibility of the proposed stabilization scheme in selecting an admissible damping gain rate that can vary from the designer's point of view depending on the design requirement [9]. However, by choosing efficient $K_{AD}$ ( $K_{AD,eff}$ ) that is certainly much higher than $K_{AD,\min}$ , in addition to desired dynamic and transient performance, the robust stability of the system against abrupt changes in voltage input and load level will also be well-guaranteed [9]. It should be noted that considering the relationship between capacitor voltage and current, it seems that the AD control feedback of the proposed stabilization approach can also be realized using the output voltage-derived feedback with the adjusted gain $CK_{AD}$ . With this frame of mind, first, we will encounter a PID controller with a design-oriented derivative part, not a standard PID controller. Second, the capacitor current feedback-based control scheme, which utilizes information about the load current and dynamics related to the source converter inductor current, has a different dynamic and functional nature than the output voltage of the source converter derivative term. Third, the derivative term related to output voltage for the PID controller introduces a considerable noise into the closed-loop system of power converters compared with other AD approaches that use information of the capacitor current. This adverse impact is mainly arising from the parasitic resistance and inductance of the source converter's output capacitor, which are determined as the equivalent series resistance (ESR) and equivalent series inductance (ESL), respectively [9],[43], and [45]. Moreover, it can have harmful effects on the network by generating impulse responses along with large overshoots/undershoots, and discrete jumps at switching transitions during small and large signal transients or even at steady-state [9],[45], and [46]. These adverse reactions significantly reduce phase margin and ultimately

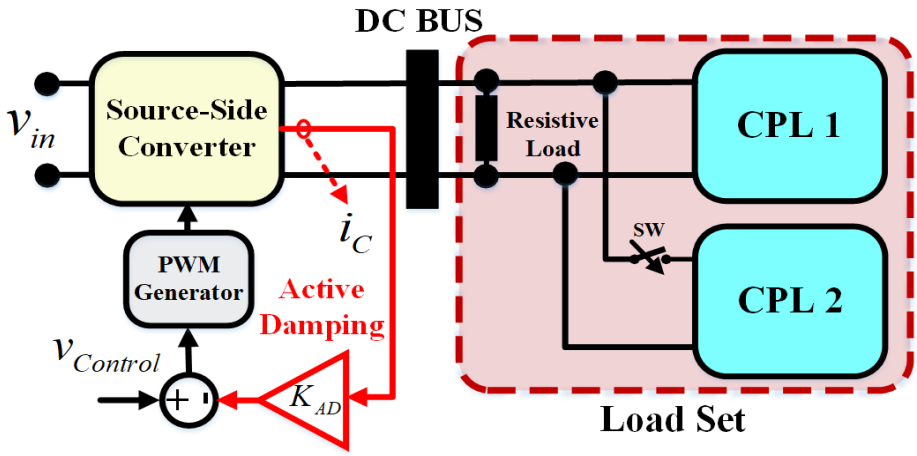



Fig. 3.10. DC MG topology intended for simulation and laboratory tests [9].

compromise the system stability [9], [47], and [48]. Although by decreasing the cut-off frequency of the low-pass filter corresponding to the derivative term, noise and phase margin can be enhanced, it causes jeopardizing of the closed-loop control bandwidth performance and also slowing down the system's dynamic responses. Accordingly, under this approach, there will always be a trade-off between the filter bandwidth and the damping performance of a closed-loop system [9]. Given these interpretations, it can be seen that by further reduction of the filter bandwidth, the stable band of $K_{AD}$ is severely limited and as a consequence, the advantages of the derivative part cannot be fully utilized. Eventually, it can be concluded that for robust stabilization of cascaded systems loaded by multiple CPLs, the presented capacitor current-based AD control scheme has a reliable and acceptable performance in various operating conditions with minimal recovery time and slight output voltage deviation for different transient times compared with PI + designed D control approach [9].

### 3.2.1.3 Simulation and Experimental Results

To verify the validity and effectiveness of the presented control strategy, a simulation was accomplished on a generic DC MG demonstrated in Fig. 3.9 using MATLAB/Simulink in the discrete-time domain with the parameters mentioned in Table I [9]. Meantime, in order to be more in line with the real conditions and to show the feasibility of the proposed AD stabilization method, digital control system delays consisting of the PWM and computational delays are also considered in the simulated model [9]. Besides, as shown in Fig. 3.11, to corroborate the applicability of the presented stabilization method in practice, the hardware configurations of the cascaded systems comprising the three DC/DC converters feeding CPLs (see Fig. 3.10) have also been separately fabricated and tested. In this laboratory setup, the control part is implemented by real hardware controller-SPACE 1202, whose sampling rate is 10 kHz. The switching frequency has been selected equal to the sampling rate of the control part [9]. Also, a low-pass filter with a cut-off frequency of about 50 kHz between the analog-to-digital converter and the current sensor has been implemented to compensate for the distortion effect caused by switching noises in capacitor's current sampling [9],[49]. It is worth noting that this cut-off frequency would be proper given that the switching noise frequency is usually higher than 1 MHz [9],[50]. The system parameters for the experimental test were intended similarly to the simulation implementation. The following three operational cases have been studied under both simulation and experimental tests.

***Case 1:*** Evaluating the system performance without and with the offered AD stabilizer technique.

***Case 2:*** Evaluating transient stability and dynamic performance of the system under variations in input voltage amplitude.

***Case 3:*** Evaluating transient stability and dynamic performance of the system under CPL changes (power rating).

Before analyzing the achieved results, how to effectively choose $K_{AD}$ based on the design process presented in the previous section, is given numerically.

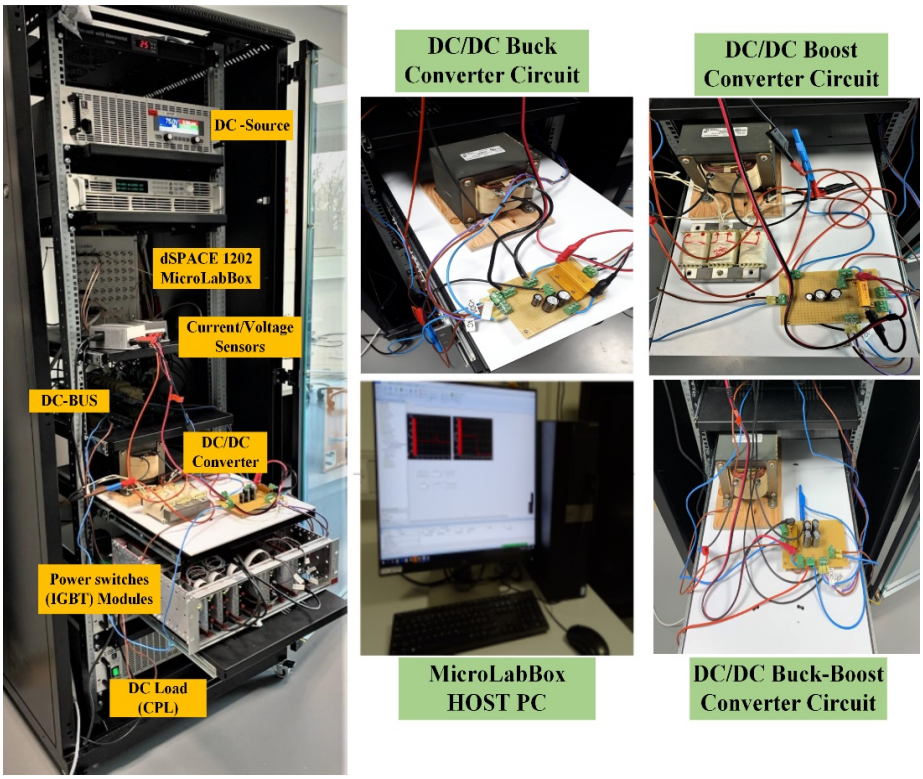



Fig. 3.11. The laboratory platform.

Negative equivalent load resistance of the cascaded system based on a certain desired output voltage of the source converter is obtained as [9]:

$$R_{eq} = R_{CPL} \left\| R_{Load} = -\frac{150^2}{2250} \right\| 470 = -10.2\Omega \cdot \tag{3-10}$$

Then, for satisfying the system stability, minimum required virtual capacitor is derived as [9]

$$C_{V,\min} = \frac{L}{R_L \left| R_{eq} \right|} - C = 43.2mF. \tag{3-11}$$

Therefore, in accordance with (3-7), the $K_{AD,\min}$ can be easily obtained as [9]

$$K_{AD,\min} = \frac{C_{V,\min} R_L V_{Tr}}{C V_{in}} = 28 \times 10^{-3} \Omega. \tag{3-12}$$

As previously described in detail, for having an efficient damping rate with admissible phase margin (see Fig.3.9) and high robustness versus unexpected variations in load level and input voltage, as well as preventing slowing down the system's dynamic response, $K_{AD,eff} = 0.55$ ( $R_V = 519.5m\Omega$, $C_V = 855.5mF$ ) that is almost 20 times larger than $K_{AD,\min}$ has been selected [9]. Therefore, in accordance with (7), the $K_{AD,\min}$ can be easily achieved as

$$K_{AD,\min} = \frac{C_{V,\min} R_L V_{Tr}}{C V_{in}} = 28 \times 10^{-3} \Omega. \tag{3-13}$$

In Case 1, as can be seen from Figs. 3.12(a) and 3.13(a), when the proposed active stabilizer strategy is turned off $\left(0 \le t \le 1s\right)$, severe unstable fluctuations arise on the DC bus voltage of the cascaded system owing to the CPLs [9]. Once the AD controller is turned on, unstable oscillations in DC bus voltage are quickly damped, and the system becomes stable. Due to the desired duty cycle depicted in Figs. 3.12(b) and 3.13(b), stability and effective damping performance of the system by employing the presented control scheme can also be well-authenticated [9]. Hence, in first step, 12. 5%

reduction in the amplitude of the input voltage is applied in case 2 (see Fig. 3.12(a)). In the second step (case 3), CPL 750W has been connected to the

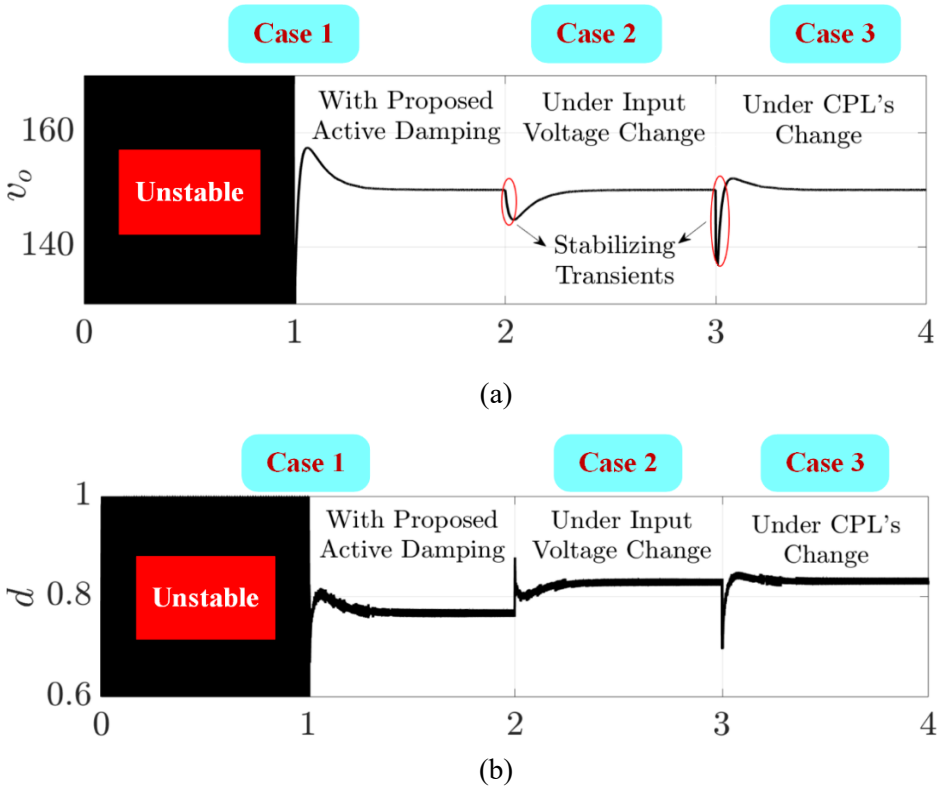



Fig. 3.12. Simulation results of the buck converter systems supplying CPLs under three operation cases. (a) Output voltage. (b) Switch duty cycle [9].

system in parallel with the existing CPL 2250W at t=3s. As can be understood from the results, after these sudden changes, without making unstable fluctuations, the DC bus voltage with stable transitions and fast dynamic responses reaches the desired value (output voltage reference) [9]. According to the three operational cases, acceptable results have also been obtained for the switch duty cycle (see Figs. 3.12(b) and 3.13(b)) [9]. Evidently, the results

demonstrate the robustness of the proposed active stabilizer strategy against unforeseen changes in the system.

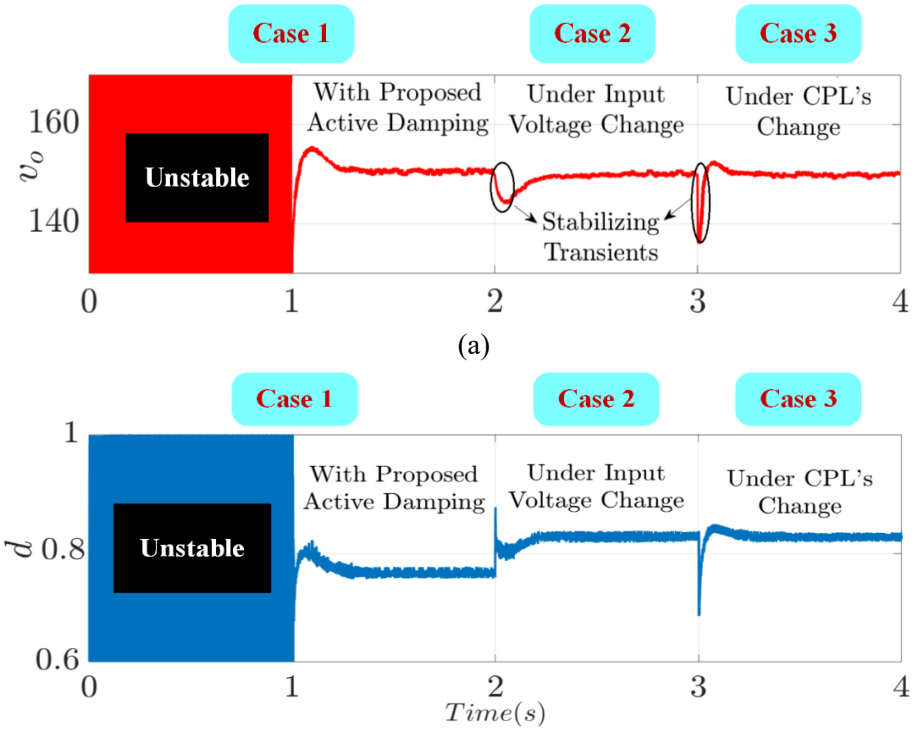
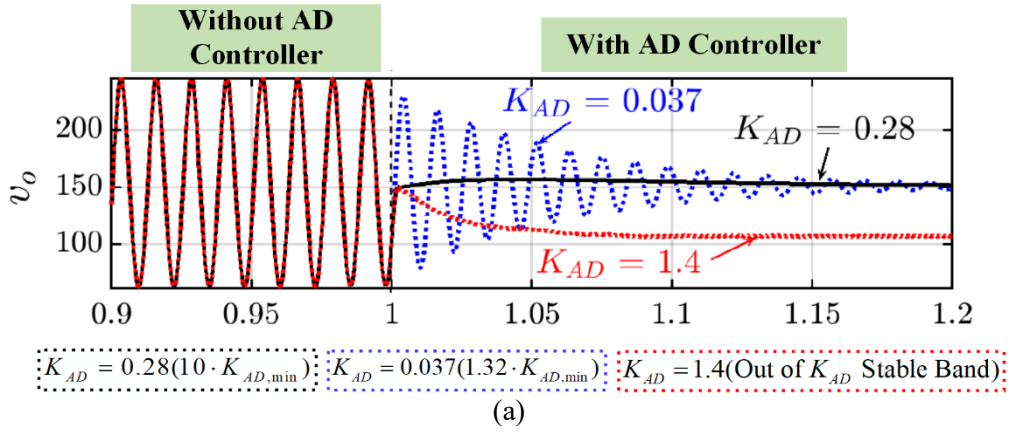
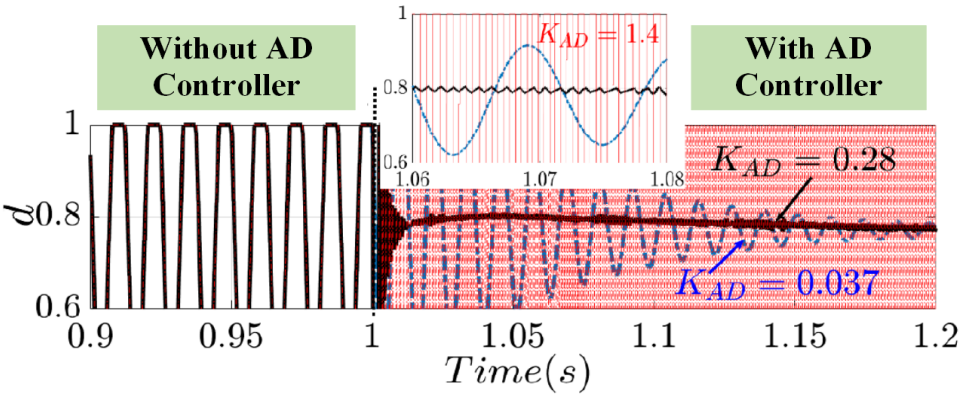



Fig. 3.13. Experimental results of the buck converter feeding CPLs (three operation cases). (a) Output voltage. (b) Switch duty cycle [9].






(b)

Fig. 3.14. Buck converter systems loaded with CPLs and resistive loads. (a) The dynamic performance for different $K_{AD}$. (b) Switch duty cycle variations for different $K_{AD}$ [9].

As seen in Fig. 3.14(a), by increasing $K_{AD}$ in the permissible stable band $(K_{AD} = 10 \cdot K_{AD,\min} = 0.28)$, unstable fluctuations in DC bus voltage are rapidly damped compared to $K_{AD} = 0.037$ $(1.32 \cdot K_{AD,\min})$ [9]. However, with a further increase in $K_{AD}$ and over its allowable stable range, e.g., $K_{AD} = 1.4$, the performance of the presented stabilization approach will no longer appropriately follow the output voltage reference and lead to system instability, of which these results are also well confirmed. in Fig.3.9. These outcomes can also be approved by Fig.3.14(b) which shows the switch duty cycle variations under the different $K_{AD}$ [9]. Eventually, it can be concluded that the CPL instability effect can be effectively compensated using the proposed active stabilizer scheme, provided that $K_{AD}$ meets the stability condition by virtually introducing an appropriate series *RC* damper that is placed in parallel with the capacitor of the source converter [9].

### 3.2.1.4 Comparative Study with the PI + Designed D Control

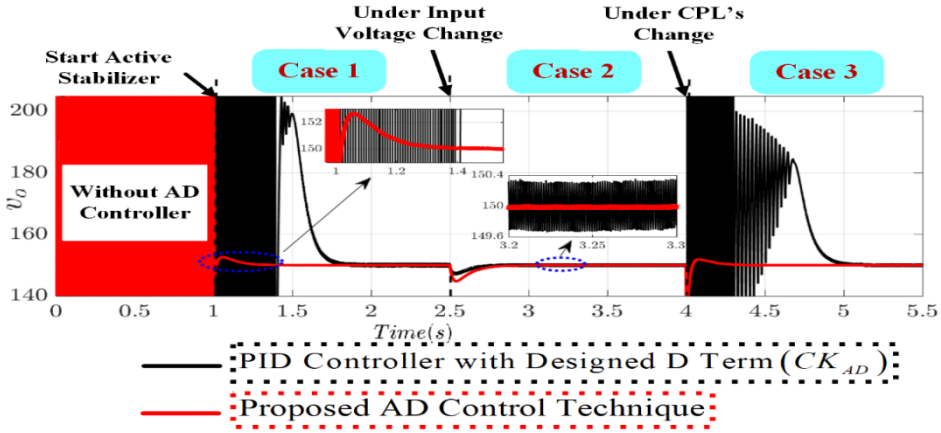



Fig. 3.15. Comparative experimental results between the proposed method and the PI + designed D (CKAD) controller with a similar damping gain rate (KAD = 0:55) for the buck converter powering CPLs [9].

As illustrated in Fig.3.15, to exhibit and accredit the superiority of the proposed active stabilization method over the PI + designed D control approach, their dynamic performance and transient stability has been experimentally compared for a similar damping gain for three operational cases [9]. In Table 3.2, the comparative results on the performance of both control strategies are also outlined. Reference voltage tracking, transient recovery time, and dynamic performance for the buck converter systems loaded with CPLs under changes in input voltage and load level (CPL power rating) have been comprehensively evaluated. The rate of change at the system level for this comparison is similar to the conditions analyzed in the previous section [9]. As is well understood in Figure 3.15 and Table 3.2, using the AD control strategy presented at t = 1s, the sharp unstable fluctuations of the bus voltage are rapidly damped. In addition, under this stabilization method, the achievement of an optimal dynamic response with a minimum transient recovery time is also achieved. On the other hand, the stabilization approach

Table 3.2. A Performance Comparison Between the Proposed Active Stabilizer Scheme and PI+Designed D Control Technique Under the Same Damping $\left(K_{AD}=0.55\right)$ for the Buck Converter Feeding CPLs [9].

| **Proposed AD Control Strategy** | | | |
|---|---|---|---|
| **Evaluation of Transient and Dynamic Performance** | | | |
| **Response Characteristics** | **Case 1** | **Case 2** | **Case 3** |
| Dynamic Response Time | Very Fast | Very Fast | Very Fast |
| Maximum Overshoot or Undershoot | 2.8% | 3.2% | 2.6% |
| Settling Time (Transient Recovery Time) | 185 ms | 220 ms | 208 ms |
| **PI + Designed D Control Strategy** | | | |
| **Evaluation of Transient and Dynamic Performance** | | | |
| **Response Characteristics** | **Case 1** | **Case 2** | **Case 3** |
| Dynamic Response Time | Very Slow | Very Fast | Very Slow |
| Maximum Overshoot or Undershoot | 230% | 2.1% | 285% |
| Settling Time (Transient Recovery Time) | 785 ms | 205 ms | 1.05 s |

based on PI + designed D controller demonstrates a weak and slow dynamic response with remarkable oscillations in transient performance [9]. The advantages of the proposed stabilizer scheme are also absolutely obvious when applying a sudden changes in load level ( CPL power rating). Moreover, it is clear that in the PI + designed D control strategy, both proper transient recovery time and insignificant output voltage deviations cannot be realized simultaneously [9]. Accordingly, by evaluating and the results obtained, it can be concluded that in the stabilization of cascaded systems consisting of DC/DC power converters supplying CPLs, the suggested method is more efficient, robust, and more reliable than the PI+designed D control method [9].

### 3.2.1.5 Comparative Study with the Virtual Series *RL* Damper-Based Stabilization Technique Proposed by [31]

Since the stabilization method presented in [15] is close to our control idea, a comparative study has been conducted to show the superiority of our contributions over it. The active stabilization approach used in [31] has

introduced a virtual series resistance to improve the damping rate and overcome the CPL instability effect for DC cascaded system. This realization of control was obtained by feedback the proportional coefficient of the inductor current of the source converter and subtracting it from the voltage control signal. However, this technique cannot be an adequate control idea in various performance states owing to intrinsic shortcomings and limitations. The first constraint is the restriction in stable band $K_{AD}$ for this stabilization strategy so that it shows inflexibility in the proposed AD controller. In this regard, for instance, by applying the AD control approach offered by [15] to the cascaded system depicted in Fig. 3.2 with the parameters determined in Table 3.1, the allowable stable range for $K_{AD}$ is restricted to $(0.027, 0.051)$. It is evident that in this condition, the maximum damping rate is only 1.5 times its minimum amount. In contrast, as described in detail, for attaining a safe phase margin and admissible damping effect, $K_{AD,\max}$ achieved by our proposed active stabilizer strategy is 20 times $K_{AD,\min}$. Second, considering that the permissible virtual $R_{L,\max}$ is limited to $\left|R_{eq}\right|$, under an intensive descending change in the load level (CPL power rating), the stability of system may not be preserved. Therefore, the proposed active stabilization technique in [31] cannot provide reliable and robust performance against sudden changes in load set. Third, as seen in Fig. 3.16, the proposed AD control scheme applied to the system illustrated in Fig.3.2 presents a fast-dynamic response with a decrease of about 75% in settling time and also significant improvement in rise time.

### 3.2.2 DC/DC Boost and Buck-Boost Converters feeding Resistive Load and CPLs

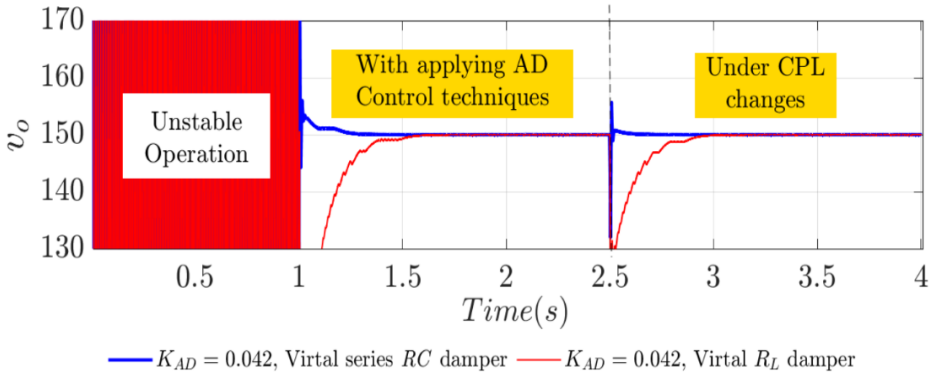



Fig. 3.16. Comparison of dynamic and transient performance of the AD technique offered by [31] with the proposed active stabilizer scheme [9].

### 3.2.2.1 Modeling and Stability Analysis

Figs. 3.17 and 3.18 show the boost and buck-boost converter systems feeding multiple CPLs and resistive loads, respectively [9]. A similar implementation process related to the averaged switch modeling method, such as steps 1 and 2, explained in detail in Section 3.2.1, is accomplished to obtain their simplified small signal-averaged equivalent models (see Figs. 3.19(a) and (b)). Then, the control-to-output transfer functions are derived (14) and (15), respectively, and also the poles are obtained by (16) [9]. According to the location of the poles and by considering $R_L \langle \left| R_{eq} \right| \cdot D'^2$ and $R_{eq} \langle 0$; the

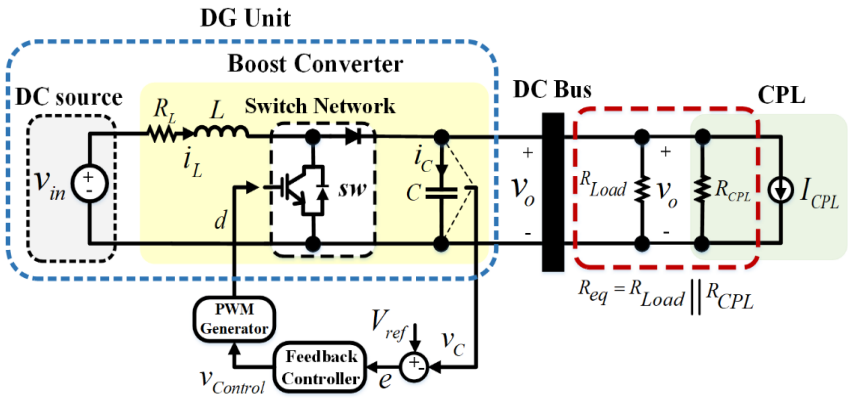



Fig. 3.17. A DC/DC boost converter supplying multiple CPLs.

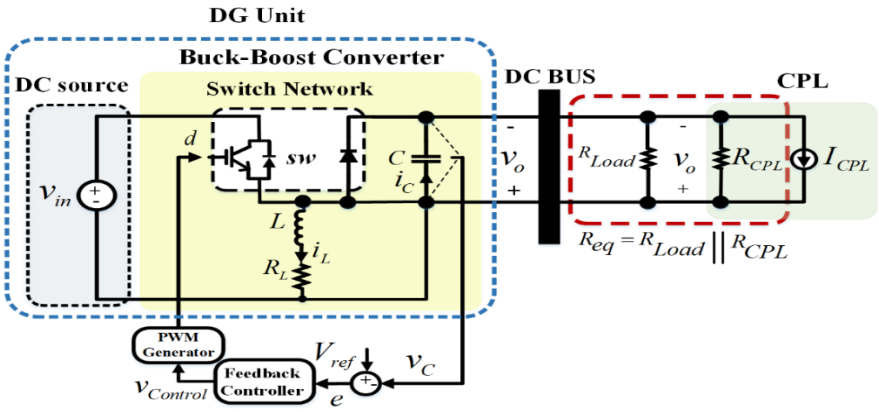
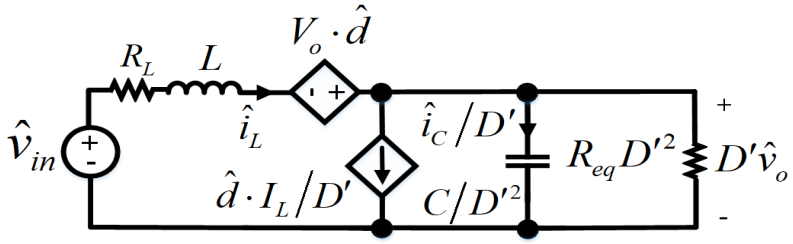
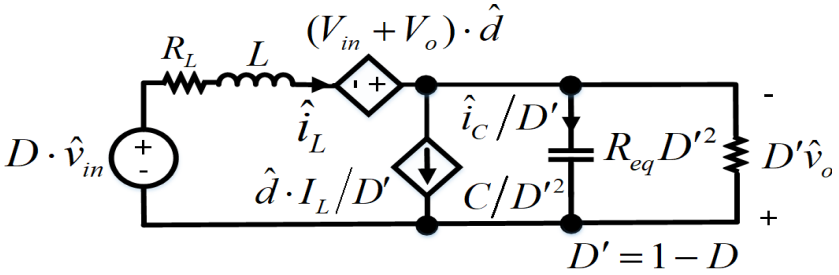



Fig. 3.18. A DC/DC buck-boost converter with multiple CPLs.

stability conditions of these cascaded systems, like the configuration demonstrated in Fig.3.2, can be satisfied by $R_L C \rangle \frac{L}{|R_{eq}|}$.




(a)




(b)

Fig. 3.19. Simplified small-signal averaged equivalent circuit. (a) Boost converter. (b) Buck-boost converter [9].

### 3.2.2.2 Control Realization

#### a) Circuit Physical Meaning

By employing the proposed AD control technique, Fig. 3.19(a) is dynamically modified as Fig. 3.20 through substitution of $\hat{d}-\left(K_{AD}\cdot\hat{i}_C/V_{Tr}\right)$ instead of $\hat{d}$ [9]. As observed in Fig.3.20, the control realization of this stabilizer strategy leads to the addition of the dependent voltage and current sources, namely $I_{AD}$ and $V_{AD}$, into the simplified small-signal averaged model shown in Fig.3.19(a) [9]. As a result, using an efficient circuit analysis, the presented control approach introduces an interesting circuit physical meaning as demonstrated in Fig. 3.21. Given the DC relations and also considering the actual conditions, $R_L \ll \left|R_{eq}\right|\cdot D'^2$, $I-I_{AD}$ can be obtained as

$$I-I_{AD}=\frac{K_{AD}\cdot\hat{i}_C}{V_{Tr}}\left[\frac{V_o}{R_L+sL}-\frac{V_o}{D'^2\left|R_{eq}\right|}\right]\cong\frac{K_{AD}V_o\hat{i}_C}{V_{Tr}(R_L+sL)}\cdot \tag{3-14}$$

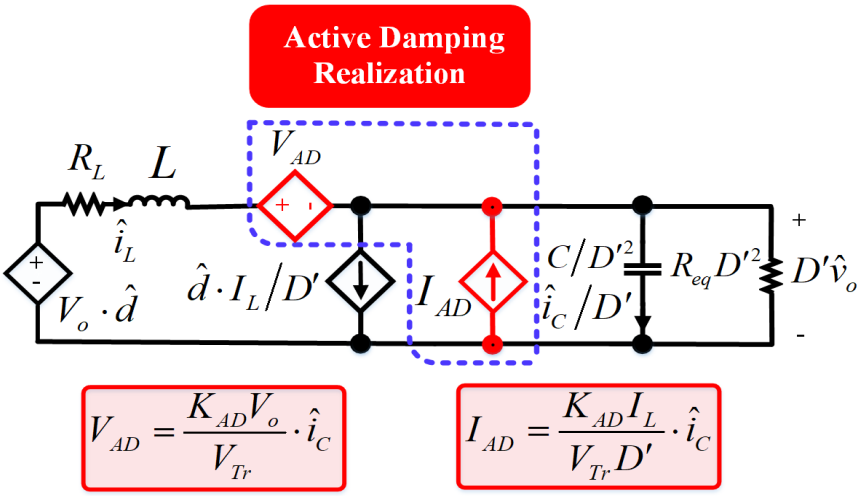



Fig. 3.20. Modified small-signal averaged equivalent circuit of the boost converter feeding CPLs with applying the proposed control strategy [9].

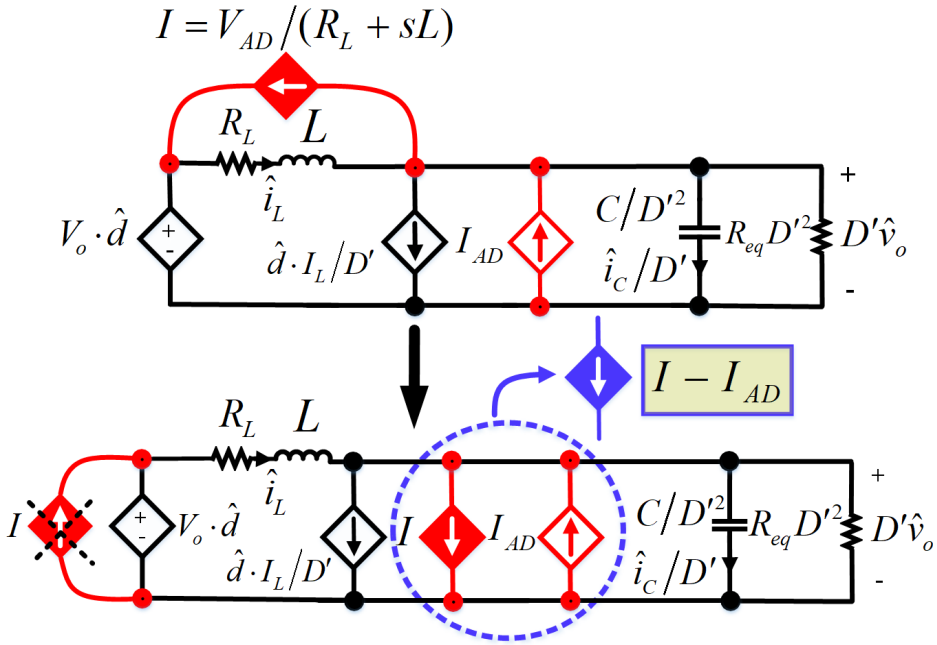



Fig. 3.21. Another analytical commentary of Fig. 3.20.

Thus, as seen in Fig. 3.22, the averaged equivalent circuit of the boost converter feeding CPLs is virtually modified to actively overcome the CPL instability effects. In this case, $C_V$ and $R_V$ are derived as follows [9];

$$\frac{D'\hat{v}_o}{I - I_{AD}} = \frac{LD'V_{Tr}}{K_{AD}CV_o} + \frac{1}{s}\left(\frac{D'R_LV_{Tr}}{K_{AD}CV_o}\right) = R_V + \frac{1}{sC_V} \cdot \tag{3-15}$$

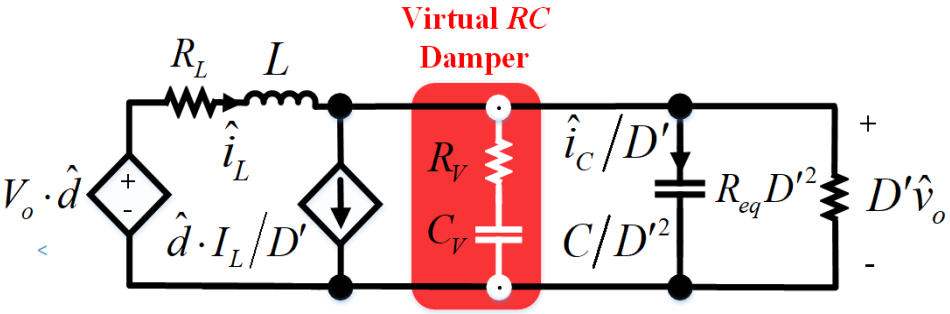



Fig.3.22. The circuit physical concept of the presented active stabilization approach devoted to the boost power converter supplying CPL [9].

The AD control realization procedure of the presented stabilizer strategy for the buck-boost converter system is also shown in Figs. 3.23 to 3.25. According to the similar above-mentioned conditions, $I - I_{AD}$ can be derived as [9];

$$I - I_{AD} = \frac{K_{AD} \cdot \hat{i}_C}{V_{Tr}} \left[ \frac{(V_{in} + V_o)}{R_L + sL} - \frac{V_o}{D'^2 \left| R_{eq} \right|} \right] \cong \frac{K_{AD}(V_{in} + V_o)\hat{i}_C}{V_{Tr}(R_L + sL)} \cdot \tag{3-16}$$

This can result in virtual incorporation of a series $RC$ branch as demonstrated in Fig. 3.25, which $C_V$ and $R_V$ are achieved as [9],

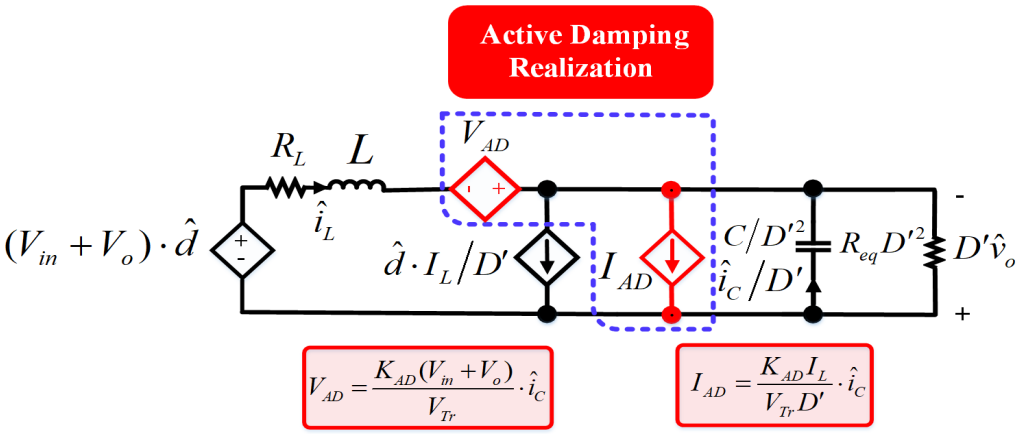



Fig. 3.23. Modified small-signal averaged model of the buck-boost converter supplying CPLs with applying the presented control strategy [9].

$$\frac{D'\hat{v}_o}{I - I_{AD}} = \frac{LD'V_{Tr}}{K_{AD}C(V_{in} + V_o)} + \frac{1}{s}\left( \frac{D'R_L V_{Tr}}{K_{AD}C(V_{in} + V_o)} \right) = R_V + \frac{1}{sC_V} \cdot \tag{3-17}$$

b) Choosing an Effective $K_{AD}$

The method of identifying the allowable range of efficient damping gain for boost and buck-boost converter systems feeding multiple CPLs is the same as the procedure presented for the buck converter system. As a result,

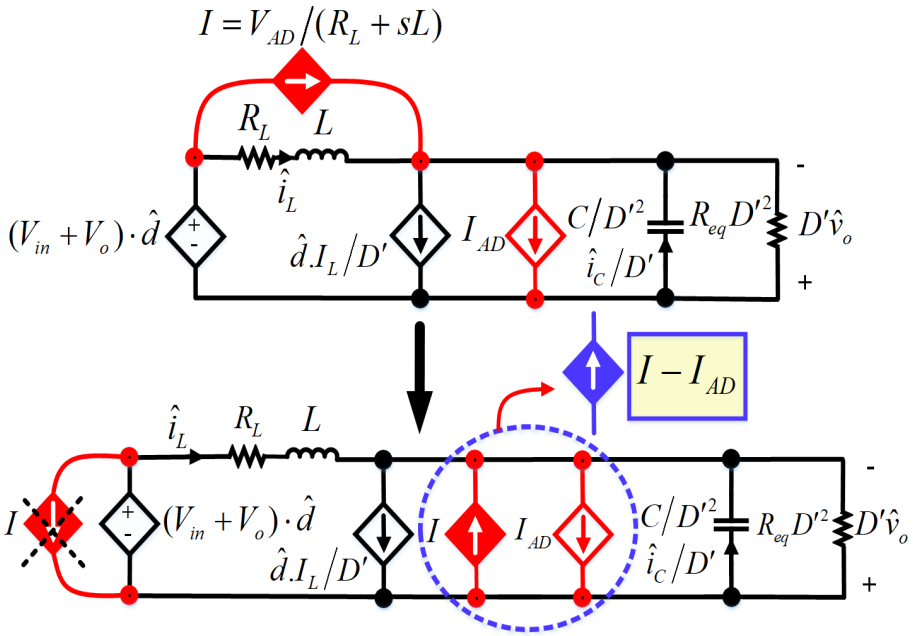



Fig. 3.24. Another analytical commentary of Fig. 3.23.

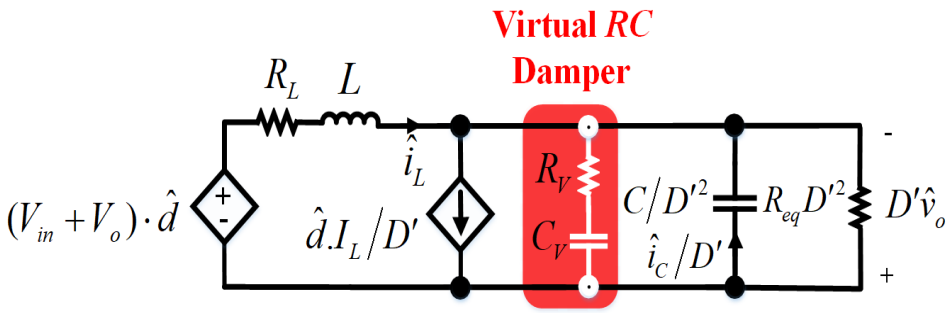



Fig. 3.25. The circuit physical concept of the proposed active stabilizer strategy applied to the buck-boost power converter feeding CPL [9].

$K_{AD}$ stable band of these cascaded systems are respectively specified by (18) and (19). To improve the damping rate of the system and achieve an admissible level of robustness against abrupt changes in the influencing factors, i.e. input voltage, CPL power rating, and voltage step changes in output reference,

without knowledge of their new values, effective $K_{AD}$ must be sufficient select larger than the corresponding $K_{AD,\min}$, provided that the system dynamic performance is not affected and also a safe phase margin is gained.

$$K_{AD} \rangle \frac{D' C_{V,\min} R_L V_{Tr}}{C V_o} = K_{AD,\min} \cdot \tag{3-18}$$

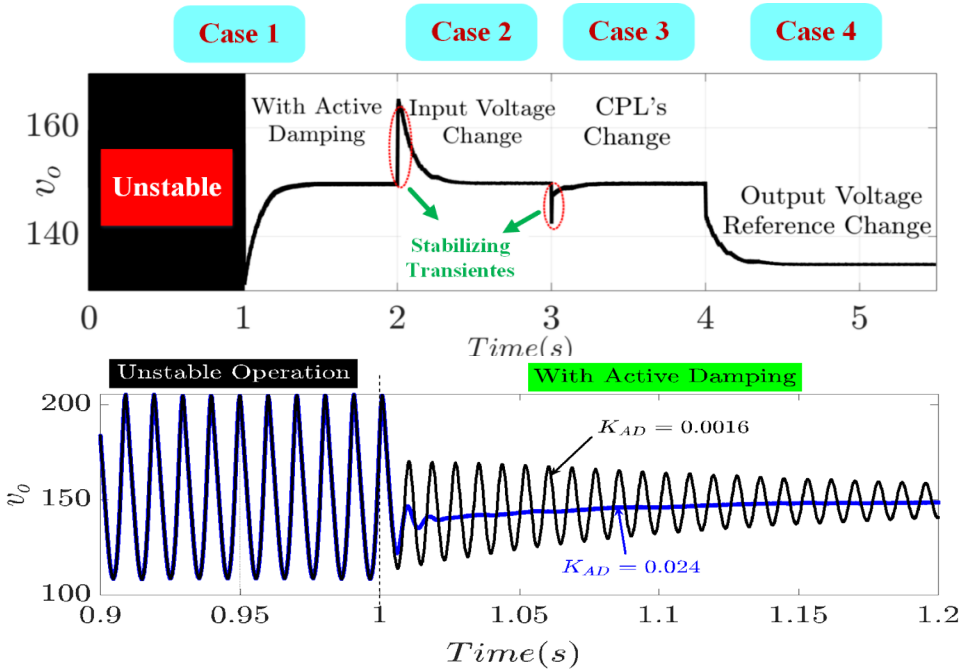
$$K_{AD} \rangle \frac{D' C_{V,\min} R_L V_{Tr}}{C (V_{in} + V_o)} = K_{AD,\min} \cdot \tag{3-19}$$

### 3.2.2.3 Simulation and Experimental Results

The discrete-time simulations in MATLAB/Simulink for the model shown in Fig. 3.9 considering computation and PWM delays were performed in order to corroborate the effectiveness of the suggested active stabilization idea on the boost and buck-boost converter systems loaded with CPLs. Moreover, experimental tests under different performance conditions based on the built laboratory rack and related circuits (see Fig. 3.10) to validate the applicability and feasibility of this technique in real life have been carried out. Table 3.1 shows the parameters intended for the laboratory and simulation tests. Since (18) and (19) are dependent on the output voltage, the assessment of the dynamic performance and transient stability of the system under step changes of the reference output voltage is also added to the previous three functional cases. These simulation and experimental tests have been done under $K_{AD,eff} = 0.026$ ($R_V = 541.5 m\Omega$ and $C_V = 886.3 mF$) for boost converter system and $K_{AD,eff} = 0.0078$ ($R_V = 679.8 m\Omega$ and $C_V = 706 mF$) for buck-boost converter system. By selecting these values for $K_{AD}$, which is 20 times higher than the corresponding $K_{AD,\min}$, improved damping rate, safe phase margin, fast dynamic and transient performance, and high robustness

versus sudden changes in the system are achieved. In case 1, as can be seen from Figs. 3.26(a), 3.27(a), 3.28(a), and 3.28(b), without applying the proposed active stabilizer, fluctuations arise on the output voltage of these source converters owing to CPL instability. When the presented technique at t = 1 s is started, the severe oscillations in bus voltage are quickly damped, and ultimately it leads to the system being stable. For robustness evaluation of the proposed AD control technique on the cascaded systems, transient stability and dynamic performance are also studied for different scenarios in cases 2 to 4. To do so, for the cascaded system depicted in Fig.3.16, at t=2 s, an

(a)




(b)

Fig. 3.26. Simulation results of the boost converter system with CPLs. (a) Output voltage. (b) Dynamic performance under different active damping terms [9].

incremental change of 20% has been applied to the input voltage level. Besides, a CPL 750W has been plugged into the DC bus in parallel with the existing CPL 2250W in case 3 (t = 3 s). In case 4, a 10% reduction for the output voltage reference at t= 4s is also considered. As understood from the results, after these unexpected changes occur in the system, the DC bus voltage with stable transitions and fast dynamic responses reaches the desired value without causing unstable fluctuations. In the same way, for the configuration shown in Fig. 3.17, a 42% increase in the input voltage in case 2 has occurred at t = 2 s (switch from boost mode to buck mode). In Case 3, a new CPL with a power rating of 600W is connected to the bus (t= 3 s) in parallel to the CPL 1800W that was already linked into the system [9]. Moreover, like the boost

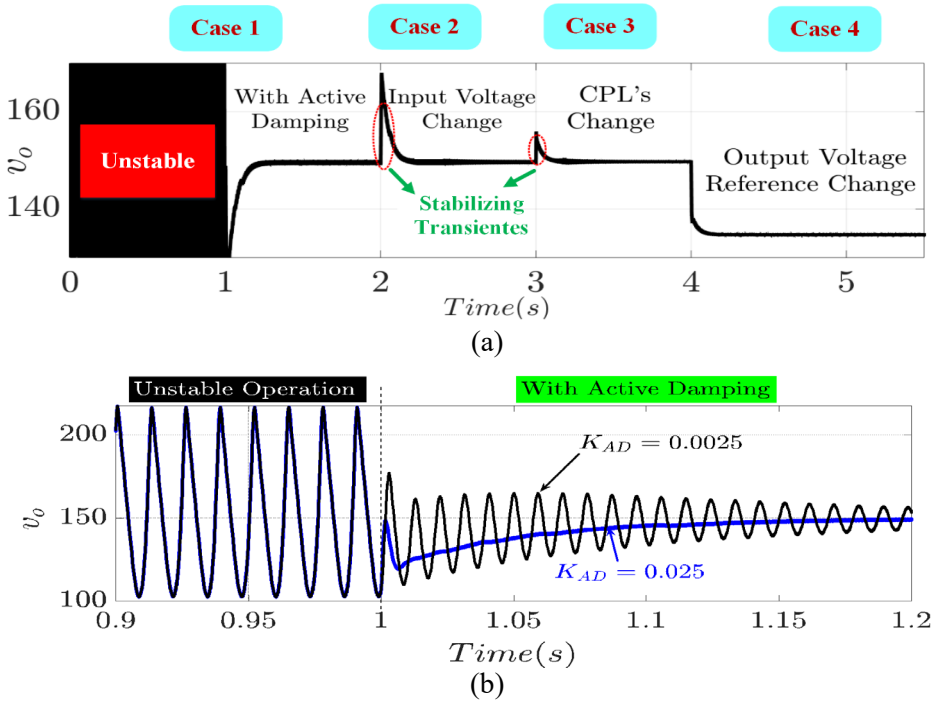



Fig. 3.27. Simulation results of the buck-boost converter system with CPLs under four operation cases. (a) Output voltage (b) Dynamic performance under different active damping terms [9].

converter system, a 10% is applied to the output voltage reference in case 4 (t= 4 s). The obtained results well-confirm the high robustness and effectiveness of the proposed AD control method in different operating conditions and unwanted changes in the system. To display the dynamic performance of this stabilizer under various $K_{AD}$, other simulations have been provided as Figs. 3.26(b) and 3.27(b). As seen in these outcomes, unstable fluctuations of DC bus voltage are stabilized with a rapid damping process by acceptable increasing $K_{AD}$.

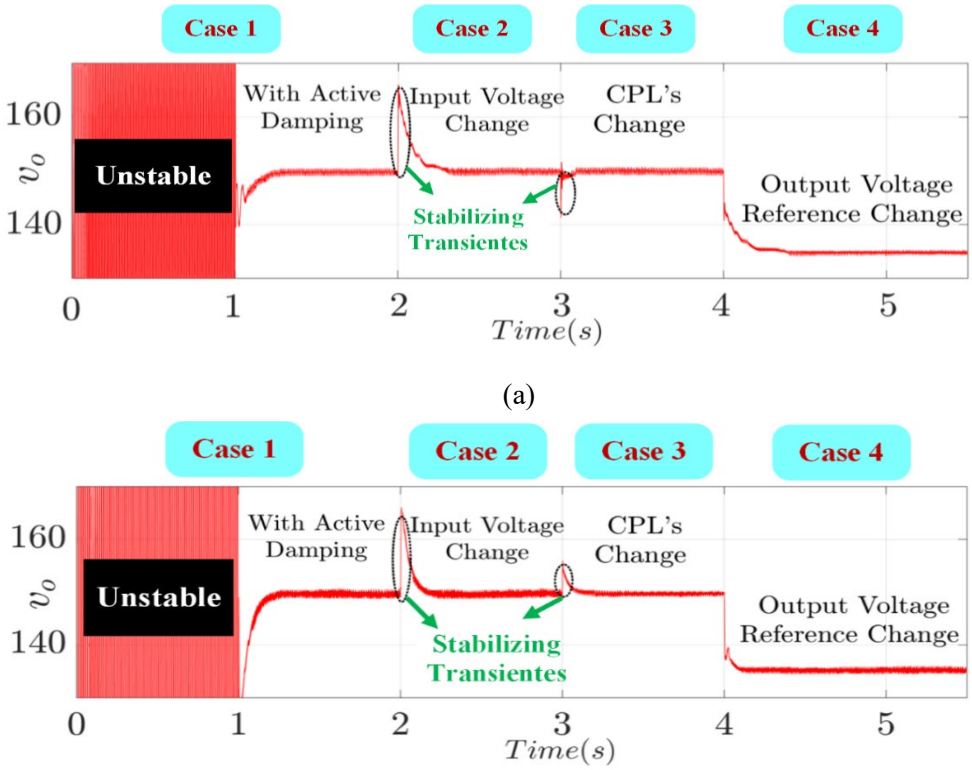



Fig. 3.28. Experimental results of the boost and buck-boost converters feeding CPLs under four operation cases (output voltage). (a) boost circuit. (b) buck-boost circuit [9].

Chapter 3

# Chapter 4

# Source-Side Adaptive Parallel-Virtual Resistance (APVR) Control Strategy-Based Stabilization Scheme

*Based on JP2, this chapter proposes new active load stabilization technique for DC cascaded systems in DC MGs*

This chapter introduces an adaptive AD control scheme-based active stabilizer strategy approach realized in the source side for stabilizing the cascaded systems in DC MGs.

## 4.1. Methodology

As argued, notwithstanding instability caused by interactions between the individually designed feedback-controlled converters in cascaded system configuration, powering loads in a tightly regulated mode (active loads) such as CPLs can yield system instability. Therefore, to address this issue, this chapter presents a new active stabilizer approach based on an adaptive parallel-virtual resistance (APVR) control strategy in the output of the source-side subsystem without affecting the desired dynamic performance of the load converter. The proposed active stabilization idea is achieved by a positive proportional-derivative feedback of the equivalent load current with an intrinsic self-tuning control parameter. Therefore, system stability is certified by actively suppressing CPL destabilizing effects through this design-oriented technique, which benefits a simple control structure with straightforward control parameter adjustment. The main merits and new contributions of the APVR-based stabilization approach are summarized as follows.

- *Easy Control Structure with Straightforward Control Parameter Setting:*

  The suggested AD scheme utilizes a fast-inner stabilizer loop with admissible bandwidth that relies on a simple control structure along with an easy setting of its control parameter. Benefiting from these advantages and the lack of complexity of the control scheme, the possibility of extending it to more complex LVDC systems is easily explored.

- *High Compatibility, Flexibility, and Modularity:*

  These superior performance features are highlighted because the APVR control strategy can well applicable for the three basic DC/DC converters loaded with multiple CPLs using only a similar control structure but with various analytical concepts.

- *Lack of influence on Load Converter's Dynamic Performance:*

  Given that the proposed AD method is realized directly by modifying the source-converter voltage control signal that leads to the creation of a pure positive adaptive virtual resistance in the source-side subsystem, the destabilization in the system is suppressed without negatively impacting the load dynamic performance.

- *Stability Is Ensured by an Intrinsic and Precise Adaptive Control Approach:*

  System stability guaranteeing is achieved through a precise and designed oriented way by virtual inserting of a parallel positive resistor at the source converter output. This load adaptive-based active stabilizer is realized based on an equivalent load current feedback with the capability of intrinsic self-tuning as per load changes.

- *High Robustness Versus Abrupt Changes – Input Voltage and Plug-and-Play of CPLs:*

The presented technique provides a fast and stable transient response and appropriate dynamic performance with a highly robust strategy against unforeseen changes in load and input voltage levels. This capability is achieved with the initial precise design and the ability to self-adjust the control parameter of the APVR control scheme.

## 4.2. Unified Average Modeling of the DC/DC Converter Systems Loaded by Resistive Load and CPLS

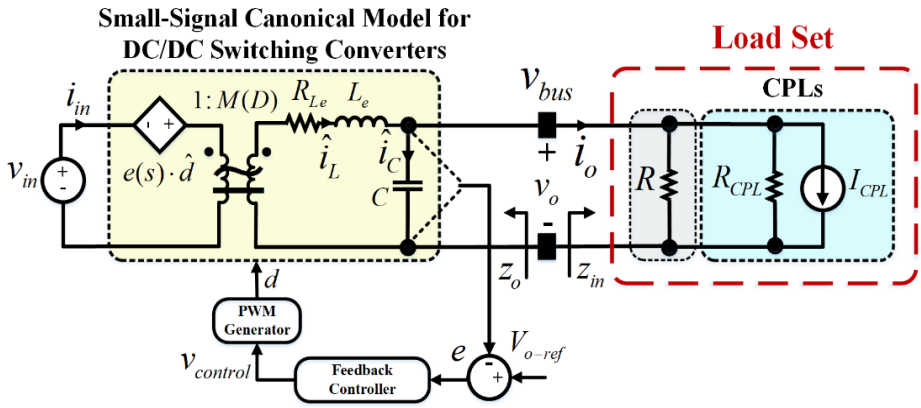



Fig. 4.1. Unified equivalent circuit model of the DC cascaded systems feeding CPL and resistive load.

Fig.4.1 demonstrates a unified equivalent circuit schematic of closed-loop controlled DC cascaded systems shown in Fig.1.1, where $d$ is defined as a duty cycle of the source converter and $M(D)$ is a conversion ratio of the converter. In this model, DC/DC switching converter of the source side as a simplified small-signal canonical circuit model and CPLs as a negative resistance in parallel with an independent current source have been modeled. In terms of stability issues, $I_{CPL}$ will be ineffective, but instead, the negative effect of the $R_{CPL}$ degrades system damping and helps to destabilize the system. The canonical model parameters for the DC/DC converter systems

Table 4.1. Canonical model parameters for the DC/DC converters

| Source Converter | $M(D)$ | $R_e$ | $L_e$ | $e(s)$ |
|---|---|---|---|---|
| **Buck** | $D$ | $R_L$ | $L$ | $\frac{V_o}{D^2}$ |
| **Boost** | $\frac{1}{D'}$ | $\frac{R_L}{D'^2}$ | $\frac{L}{D'^2}$ | $V_o\left(1-\frac{(R_L+sL)}{D'^2R_{eq}}\right)$ |
| **Buck-Boost** | $\frac{D}{D'}$ | $\frac{R_L}{D'^2}$ | $\frac{L}{D'^2}$ | $-\frac{V_o}{D^2}\left(1-\frac{D(R_L+sL)}{D'^2R_{eq}}\right)$ |

consisting of the buck, boost, and buck-boost converters have been brought in Table.4.1 [43]. By replacing the canonical model parameters associated with each converter, the simplified small-signal equivalent circuit of DC cascaded systems with multiple CPLs and resistive load is easily achieved.

## 4.3. Proposed APVR Control Strategy for Cascaded Systems in DC MGs

### 4.3.1 DC/DC Buck Converter feeding Resistive Load and CPLs

In this section, we first explain how to apply and realize the APVR-based stabilizer technique for stabilization of the buck converter system linked to the multiple CPLs and resistive load. Then, feasibility and effectiveness of the proposed control strategy is authenticated by simulations and laboratory results. In light of these outcomes, robustness, the transient response and dynamic performance of the network in the presence of abrupt variations in input voltage value and load changes (plug-and-play (PnP) of CPLs) have also been assessed and analyzed.

#### 4.3.1.1 Control Realization of the APVR Control Strategy

a) Circuit Physical Meaning

By applying the canonical form parameters in the configuration shown in Fig.4.1, and ignoring the second-order terms derived via multiplication of ac

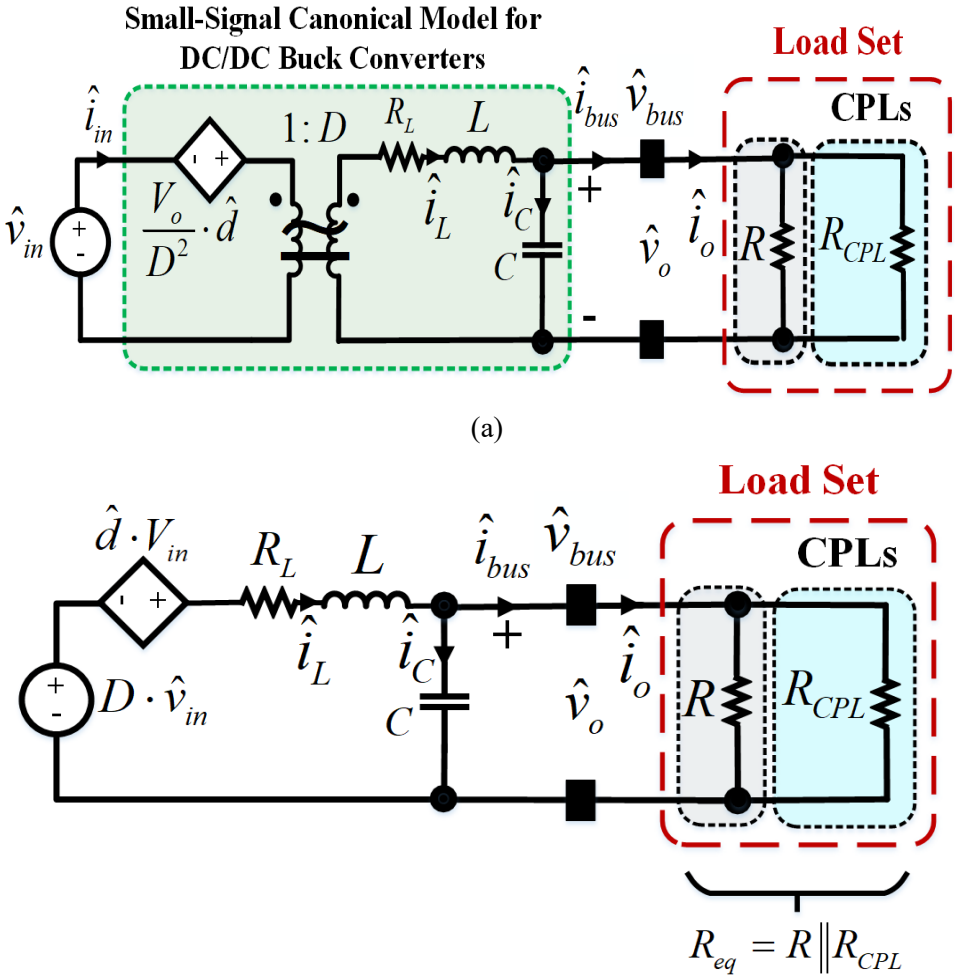



Fig. 4.2. Small-signal averaged equivalent circuit of a DC/DC buck converter feeding CPLs. (a) Circuit schematic. (b) Simplified circuit.

Afterwards, by moving all the available elements from the left to the right of the transformer, the simplified small-signal model can be achieved in Fig. 4.2 (b). Fig. 4.3(a) shows the proposed APVR-based AD control scheme applied

to the buck converter system supplying CPLs and resistive load. As seen, this technique is implemented based on a proportional

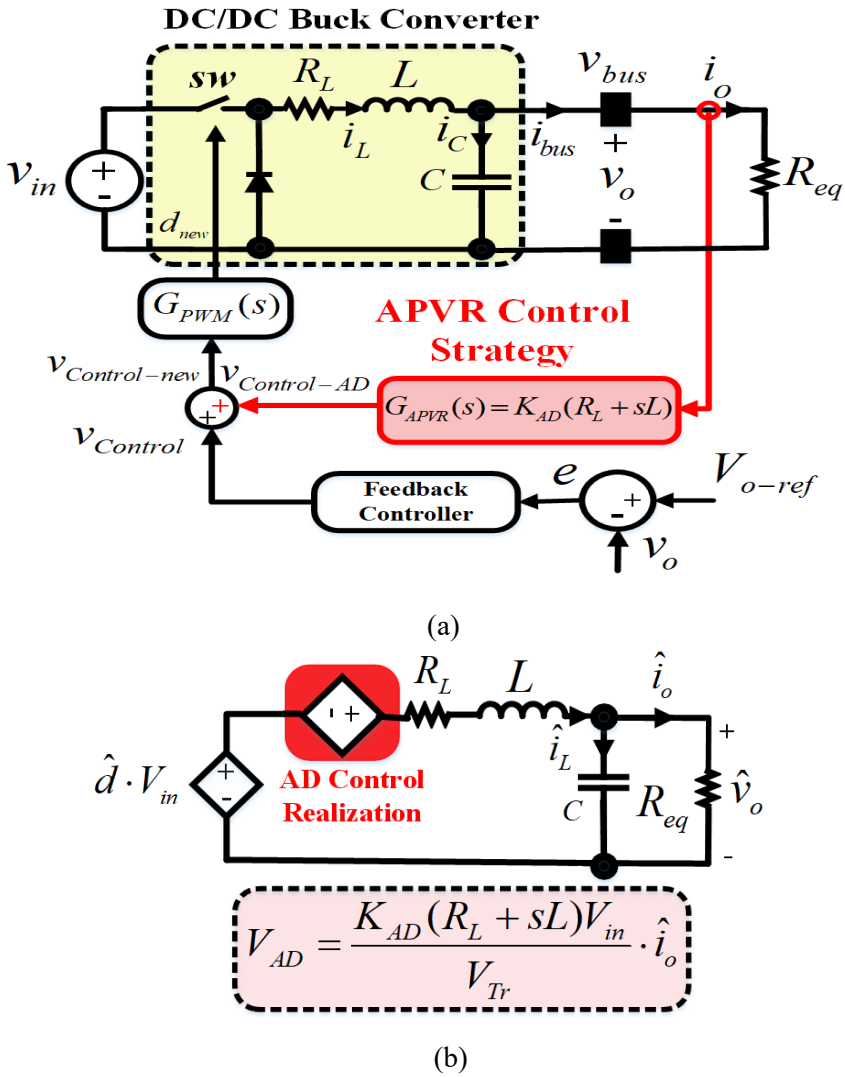



Fig. 4.3. The proposed APVR control strategy for the buck converter system feeding multiple CPLs. (a) Circuit model. (b) Modified small-signal averaged model.

derivative positive feedback of the equivalent load current that has the inherent self-adjusting capability of its control parameter. It behaves as a fast-inner stabilizing loop and adds a new voltage control signal into the available voltage control loop. The designed feedback loop coefficients are determined by multiplying the control parameter designed damping gain $(K_{AD})$ with the $R-L$ impedance of the respective source converter. Accordingly, by modifying $\hat{d}$ (initial control signal) in Fig. 4.2(b) as $\hat{d}_{new}=\hat{d}+\hat{d}_{AD}$, and neglecting the ac term related to the input voltage, the simplified small-signal averaged model modified as Fig. 4.3(b). $\hat{d}_{AD}$ is APVR-based control signal and obtained as

$$\hat{d}_{AD}=\left[\frac{K_{AD}\cdot(R_L+sL)\cdot\hat{i}_o}{V_{Tr}}\right] \tag{4-1}$$

where, $V_{Tr}$ is defined as the amplitude of triangular carrier signal.

It found that the applied AD stabilizer loop behaves as a dependent voltage source $V_{AD}$ to alter the converter's output voltage dynamically for compensating CPL's instability effect. It is evident from Fig. 4.3(b), the proposed AD control approach presents an attractive circuit physical meaning, which its result has been graphically represented in Fig. 4.4. This realization is obtained based on an efficient circuit analysis, whose theoretical process has been stated step-by-step below:

***Step 1)*** Conversion of the Thevenin circuit containing the dependent voltage source $V_{AD}$ and the $R-L$ impedance to the respective Norton circuit.

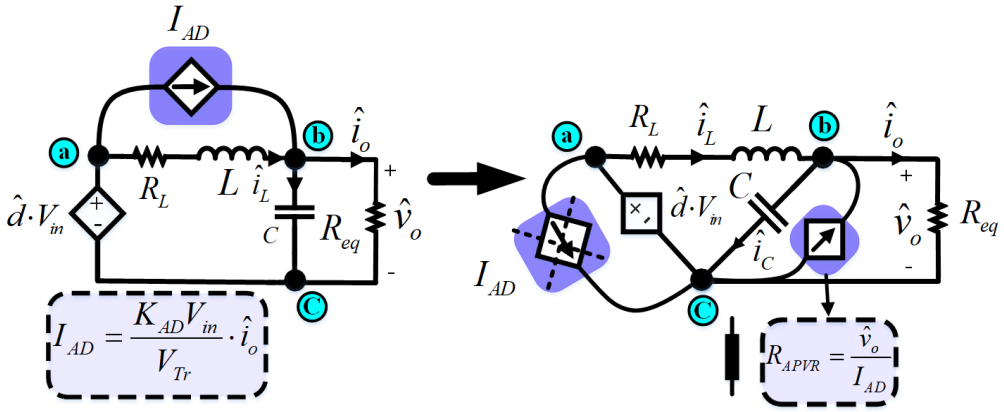



Fig. 4.4: Another analytical commentary of Fig. 4.3(b).

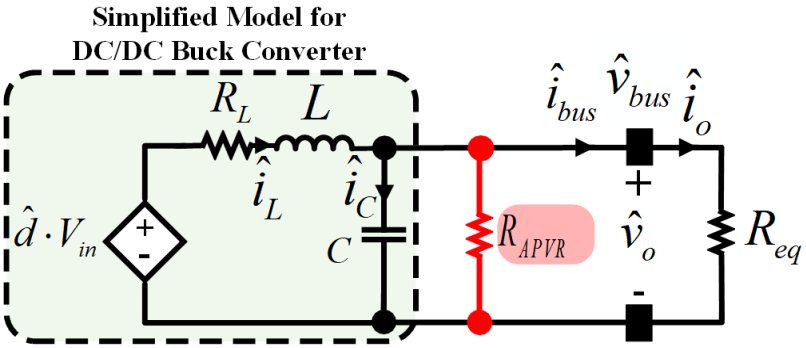



Fig. 4.5 The circuit physical concept of the APVR control strategy for the buck converter supplying multiple CPLs and resistive load.

***Step 2)*** Deactivating the dependent current source $I_{AD}$ and shifting it from node a toward node c and lastly to node b.

Obviously, the $I_{AD}$ in parallel with the voltage source can be disregarded (see Figure 4.4).

***Step 3)*** Conversion of the dependent's current source to its corresponding resistance.

Consequently, the physical circuit concept of the APVR strategy's control realization leads to the virtual insertion of a parallel positive resistor at the output of the source-side circuit because each dependent current source can be modeled by an impedance whose value depends on its voltage (see Fig. 4.5). Eventually, considering that $\hat{i}_o = \frac{\hat{v}_o}{R_{eq}}$, $R_{APVR}$ can be easily calculated as

$$\frac{\hat{v}_o}{I_{AD}} = R_{APVR} = \frac{-R_{eq}V_{Tr}}{K_{AD}V_{in}}. \tag{4-2}$$

Given (4-2) and since in real condition $R_{eq} \langle 0$, $R_{APVR}$ helps in actively suppressing the CPL destabilizing effect. Therefore, by choosing an efficient $K_{AD}$, the system will achieve robust stability with acceptable transient and dynamic performance.

b) Designing of Effective AD Control Coefficient

It is obvious that if $R_{APVR} \langle \left| R_{eq} \right|$ in (4-2) is satisfied, the stability of the system shown in Fig. 4.2(a) will be confirmed by fulfilling Routh's stability criterion for the small-signal control-to-output transfer function with the presence of the APVR-based active stabilizer method (see (4-3)).

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_{in}}{LC \cdot s^2 + (R_L C + \frac{L}{A}) \cdot s + (1 + \frac{R_L}{A})}. \tag{4-3}$$

where

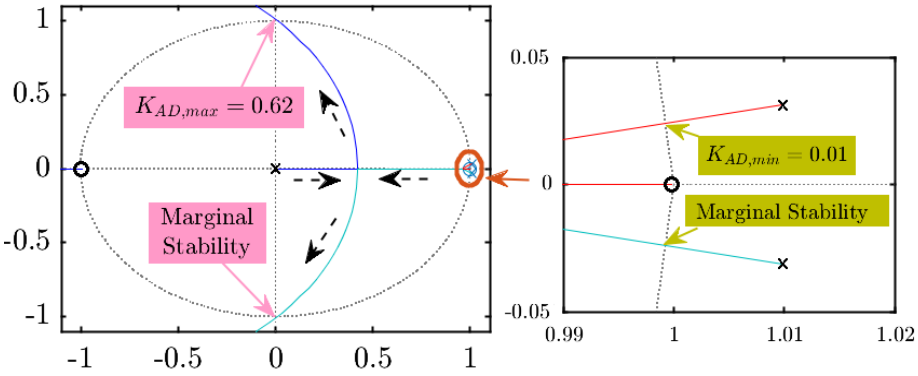



Fig. 4.6: Root locus of control-to-output transfer function for the buck converter system supplying CPL based on variation effect of the controller damping gain.

$$A = R_{APVR} \| R_{eq} \tag{4-4}$$

Then, the minimum $K_{AD}$ can be achieved as

$$K_{AD,\min} = \frac{V_{Tr}}{V_{in}}. \tag{4-5}$$

As mentioned in the previous chapter, the digital implementation of the AD stabilization loop is an important issue that needs to be addressed. Whereby, in practice, PWM and computational delays are considered influential factors in digitally-controlled systems. In this regard, like the implementation done for the presented active stabilization method in Chapter 3, sampling period $T_S$ is considered as the computational delay and also, half of the sampling period, $T_S/2$ , is taken into account as for the PWM delay arising from the zero-order-hold (ZOH) effect. Next, the stability analysis is accomplished by considering these delays in examining the effect of $K_{AD}$ changes and also determining its

Table 4.2. The Parameters of the Cascaded Systems

| Source Converter | $L$ | $C$ | $R_L$ | $R_{Load}$ | $P_{CPL}$ | $V_{in}$ | $V_o$ | $D$ |
|---|---|---|---|---|---|---|---|---|
| **Buck** | 20 mH | 470 $\mu$F | 45 m$\Omega$ | 470 $\Omega$ | 250 W | 100 V | 50 V | 0.5 |
| **Boost** | 2.4 mH | 860 $\mu$F | 5 m$\Omega$ | 200 $\Omega$ | 750 W | 100 V | 150 V | 0.33 |
| **Buck-Boost** | 2.4 mH | 860 $\mu$F | 5 m$\Omega$ | 200 $\Omega$ | 750 W | 120 V | 150 V | 0.55 |

stable band (maximum permissible $K_{AD}$) using the root-locus analysis method. The discrete root loci of (4-3) has been plotted in Fig. 4.6, with the parameters determined in Table 4.2. As understood from root locus analysis, without activating the APVR control method ($K_{AD}=0$), the closed-loop system performance shows an unstable behavior owing to the existence of a complex conjugate pole pair in outside the unit circle. After starting the AD control-based stabilizer approach and under $K_{AD}=K_{AD,\min}=0.01$, the system reaches marginal stability. In addition, by increasing the $K_{AD}$, which represents an increase in system damping rate and thus improving the system phase margin, the unstable poles of the system are transferred to the inner unit circle and consequently, the stability of the closed-loop control system is achieved. However, due to control system delays, increasing damping gain from a certain value, $K_{AD,\max}=0.62$, leading to a gradual reduction in damping rate and the return of closed-loop poles outside the unit circle, and ultimately the system goes to instability condition (see Fig.4.6). Hence, the allowable stability band based on $K_{AD}$ can be defined as $\left[K_{AD,\min}, K_{AD,\max}\right]$ We should keep that in mind, this stable band can be expanded by the reducing $T_s$. By the way, achieving robust stability with a desirable damping rate and having fast transient and dynamic responses at the system level is adopted as a principle in controller efficient design. Towards this end, the initial and

optimal choice of $K_{AD}$ at the startup will be very important. Therefore, since $K_{AD,\min}$ is conversely dependent on $V_{in}$, the optimal $K_{AD}$ ($K_{AD,eff}$) must be determined much higher than $K_{AD,\min}$ to guarantee the system robustness in case of unexpected variations in input voltage without knowledge of its new value. Besides, the transient and dynamic performance of the system against unforeseen changes in load level is another issue in terms of robust stability that needs to be considered. To this end, the next part explains how to obtain robust stability and optimal dynamic performance thanks to the intrinsic load adaptive characteristics of the proposed AD method.

C) Intrinsic Load Adaptive feature

To better understand this efficient characteristic, how to achieve it is described below. Assuming that during initial setup, due to the presence of the CPL, $R_{eq} = -R_{eq,inital}$, and based on the design process described in the Subsection (b), the effective AD control gain is selected as initial $K_{AD,eff}$. As soon as a sudden change happens in the load value during operation, i.e. $R_{eq,new} = -m \cdot (R_{eq,initial})$, in which $m$ is a positive real number expect zero, the new equivalent load current will be $1/m$ times of $\hat{i}_{o,initial}$. Hence, new control signal will be attained as $\hat{d}_{AD,new} = (\frac{1}{m}) \cdot \hat{d}_{AD,initial}$. Subsequently, the initial virtual resistance is automatically changed to $R_{APVR,new} = m^2 \cdot (R_{APVR,initial})$. This means that the proposed APVR stabilizing strategy has capability of setting AD gain $(K_{AD,new} = (\frac{1}{m}) \cdot K_{AD,initial})$ without knowing the new information of load equivalent value. This load-adaptive

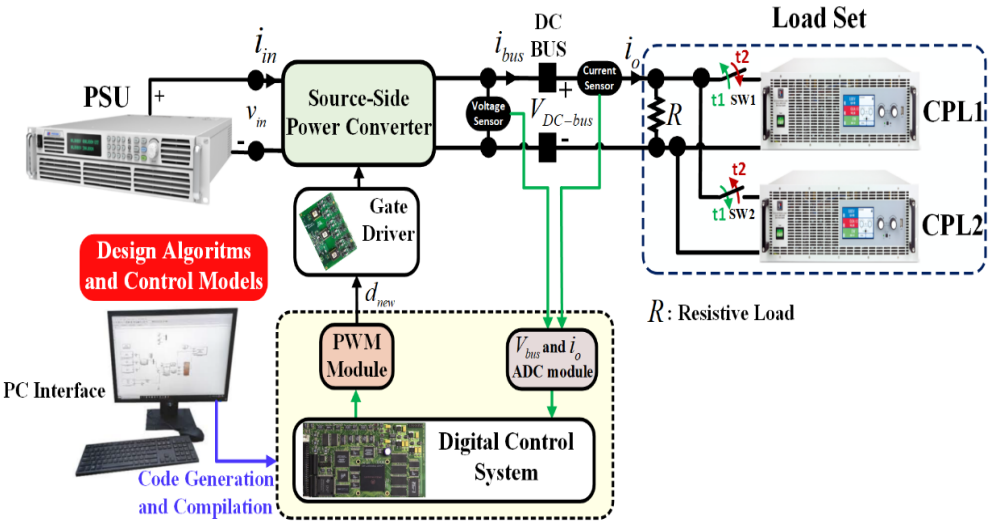



Fig. 4.7: Schematic of the experimental configuration [16].

online self-adjusting feature maintains the system's robust stability $(R_{APVR,new} \langle |R_{eq,new}|)$ with a rapidly dynamic response.

### 4.3.1.2 Simulation and Experimental Results

To prove the validity and effectiveness of the proposed APVR control strategy, a simulation was carried out using MATLAB/Simulink in the discrete-time domain with the parameters given in Table 3.2. Meantime, to better conform with the actual condition and to show the feasibility of the proposed AD stabilizer, digital control system delays consisting of the PWM and computational delays factors are also considered in the simulated model. In addition, three hardware prototypes of the cascaded systems with the configuration provided in Fig. 4.7 have been also built and tested to ensure applicability of the APVR-based stabilization approach in real-life (see Fig. 4.8) [16]. In the experimental implantation, real hardware controller-dSPACE 1202(Microlab Box) with a sampling rate of 10 kHz has been employed for

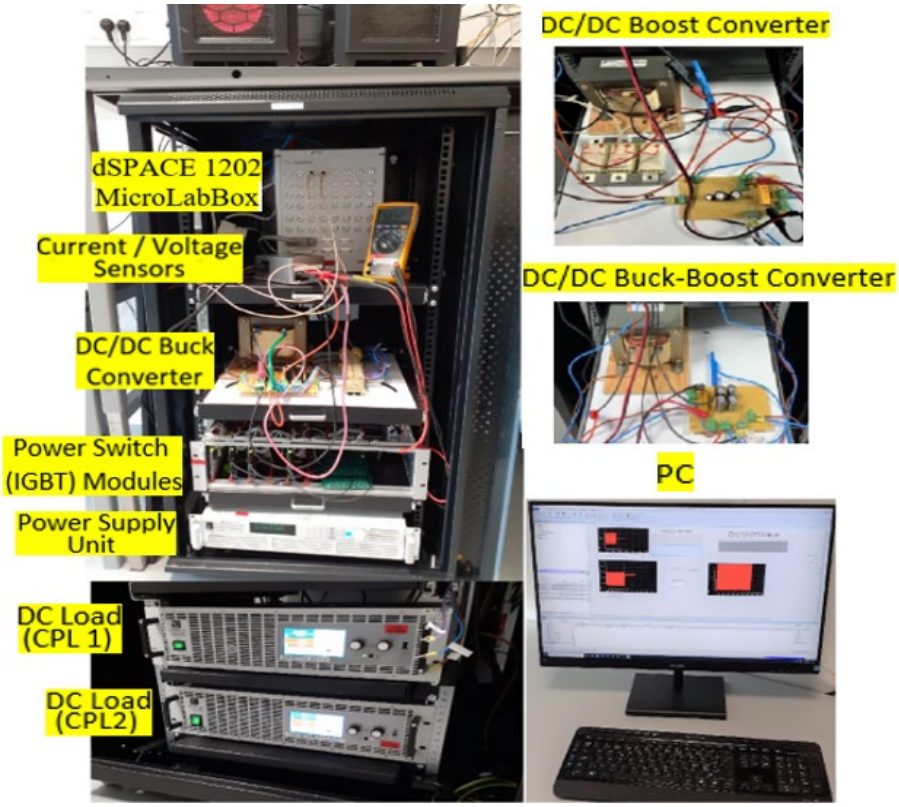


Fig. 4.8 Laboratory setup [16],

controlling of the source dc/dc converter. The switching frequency has been considered equal to the sampling rate of the control part. The system parameters are selected in the same simulations and experimental tests. For both implementations, three operational cases are considered as follows [16]:

***Case 1:*** System performance without and with the APVR control strategy.

***Case 2:*** Assessment of the transient stability and dynamic performance of the system in the presence of input voltage variations.

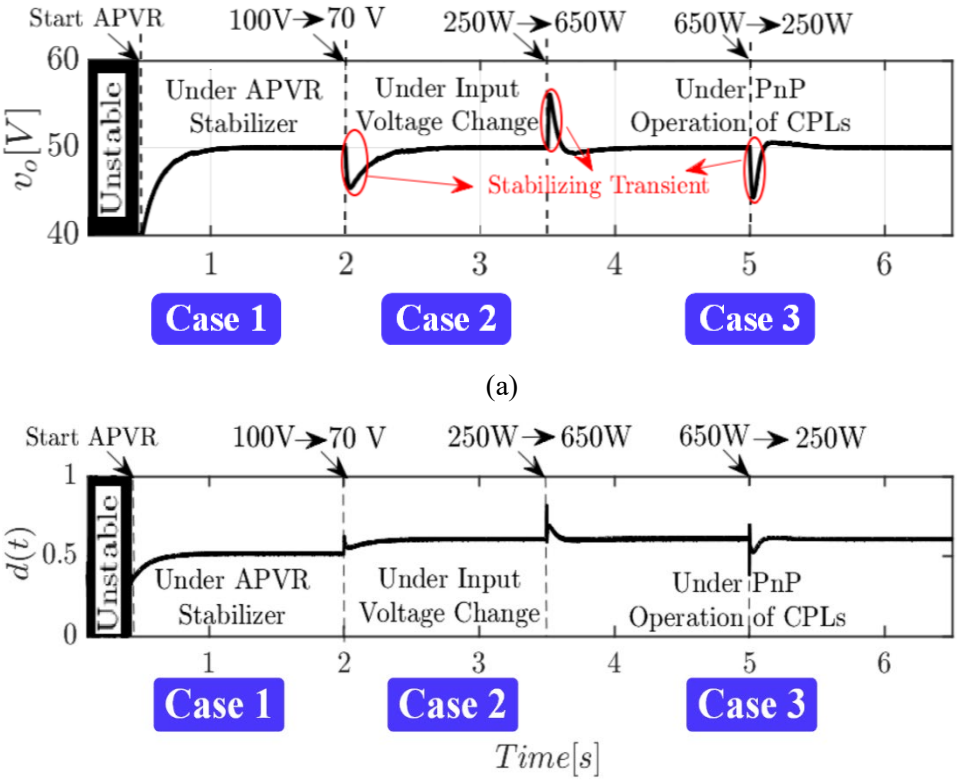



Fig. 4.9. Simulation results of the buck converter system with CPLs. (a) Output voltage. (b) Switch duty cycle.

***Case 3:*** Assessment of the transient stability and dynamic performance of the system under PnP of CPLs [16].

First, how to choose an effective $K_{AD}$ as per the design process described in the prior b subsection from the previous section is given numerically. In order to do so, the negative equivalent load resistance of the cascaded structure is calculated based on a certain desired output voltage as below:

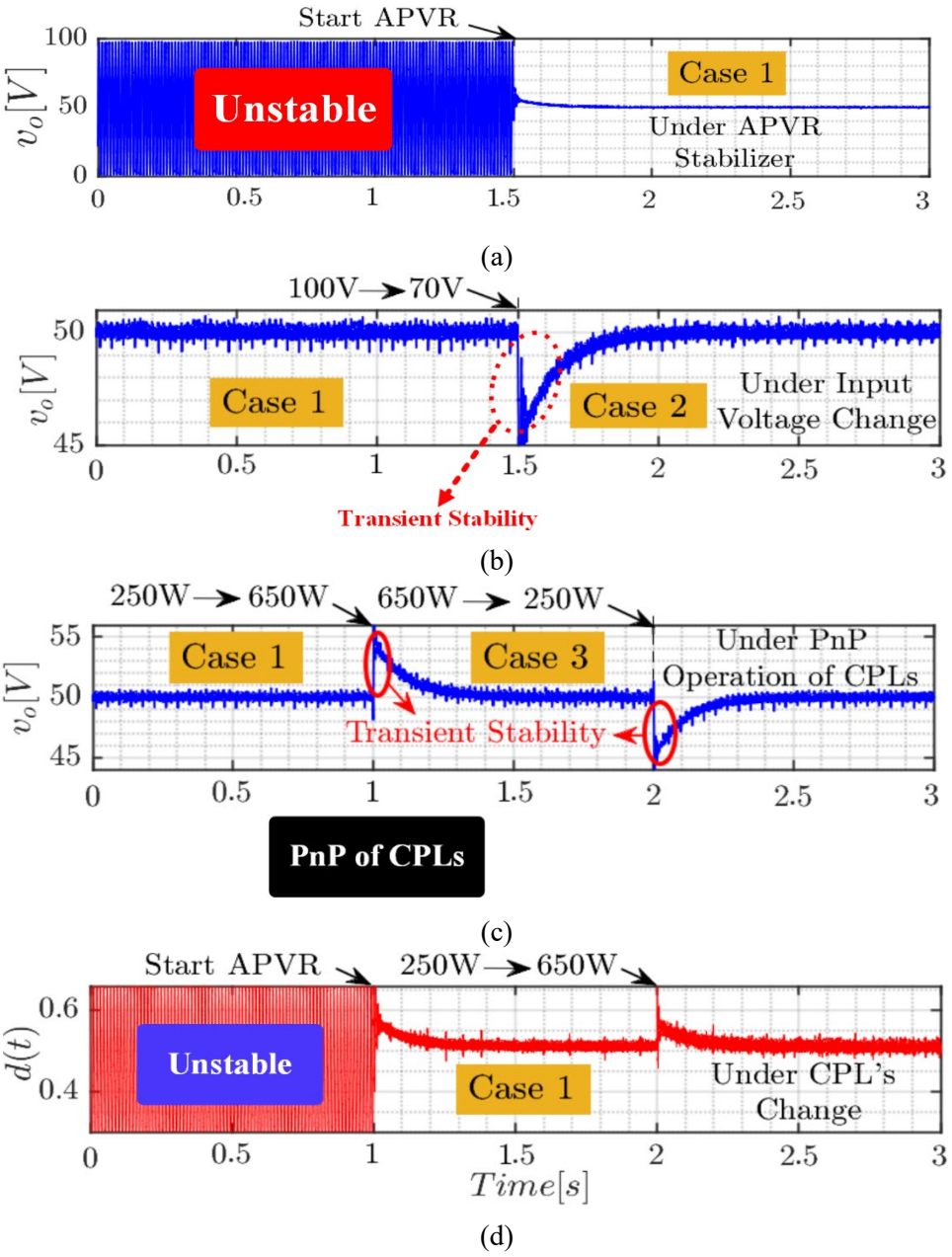



Fig. 4.10. Experimental results of the buck converter feeding CPLs. (a) Output voltage with and without APVR strategy. (b) Output voltage under input voltage change. (c) Output voltage under PnP of CPLs. (d) Switch duty cycle under CPL power rating change [16].

$$R_{eq} = R_{CPL} \left\| R_{Load} = -\frac{50^2}{250} \right\| 470 = -10.2\Omega \cdot \tag{4-6}$$

Then,

$$K_{AD,\min} = \frac{V_{Tr}}{V_{in}} = 0.01. \tag{4-7}$$

As previously explained, to obtain an efficient damping rate, rapid transient and dynamic performance as well as desirable robustness level against abrupt changes in input voltage amplitude, $K_{AD} = 0.2$ $(R_{APVR} = 510m\Omega)$ has been considered as an effective initial selection which is 20 times larger than the $K_{AD,\min}$. In case 1, as seen in Figs. 4.9(a) and 4.10(a), before the APVR stabilizer is activated, there are unstable oscillations in the DC bus voltage due to the active load instability effect. Once the presented AD stabilization is turned on, the very extreme fluctuations in the DC bus voltage are rapidly damped and then the system becomes stable with a minimum of transient recovery time and admissible dynamic response. The effective damping and stable performance of the cascaded system can also be verified in Figs. 4.9(b) and 4.10(d), due to the acceptable duty cycle realized by the proposed APVR based stabilization approach. To assess the robustness of this method, the transient stability and dynamic behavior of the system against possible changes in input voltage value and load level are also studied in cases 2 and 3. To reach this aim, first, a 30% decrease in the value of input voltage is applied to case 2 (see Figs. 4.9(a) and 4.10(b)). In Case 3, as shown in Figs. 4.9(a) and 4.10(c), to investigate the PnP operation of CPLs, the connection of the primary active load (CPL1) with a power rating of 250W under a $K_{AD,eff} = 0.2$ $(R_{APVR} = 510m\Omega)$ is decoupled and then a CPL2 with a power

value of 650W is connected into the DC bus. With the occurred change in the load set, the initial $K_{AD}$ is updated to its new value $K_{AD,eff} = 0.526$ ($R_{APVR} = 73.68m\Omega$) thanks to the load adaptive online self-tuning feature of the presented AD stabilization method. Then, by disconnecting CPL2 and reconnecting CPL1, $K_{AD}$ returns to its primary value automatically. As observed, after these unforeseen changes in the system, the bus voltage comes to its favorable value with stable transitions and very rapid dynamic responses. These results can also be confirmed by the Fig. 4.9(b) and 4.10 (d), which show the switch duty cycle based on the operational cases. In addition, it can be found that CPL instability is effectively compensated using the APVR-based active stabilizer method provided that $K_{AD}$ fulfilled the stability condition by virtual insertion of a suitable load adaptive pure resistive damper in parallel with the output of the source side circuit.

### 4.3.2 DC/DC Boost and Buck-Boost Converter feeding Resistive Load and CPLs

#### 4.3.2.1 Control Realization of the APVR Control Strategy

##### a) Circuit Physical Meaning

By applying the canonical model parameters determined in Table.3.1 to the configuration shown in Fig. 4.1 and neglecting the ac second-order terms, the small-signal averaged equivalent circuits of the boost and buck-boost systems supplying multiple CPLs are respectively achieved as Fig. 4.11(a) and (b). Then Fig. 4.12(a) and (b) respectively demonstrate a simplified small-signal model of these systems. Like the buck converter, after using the proposed AD stabilization scheme, Fig. 4.12(a) is modified as Fig. 4.13

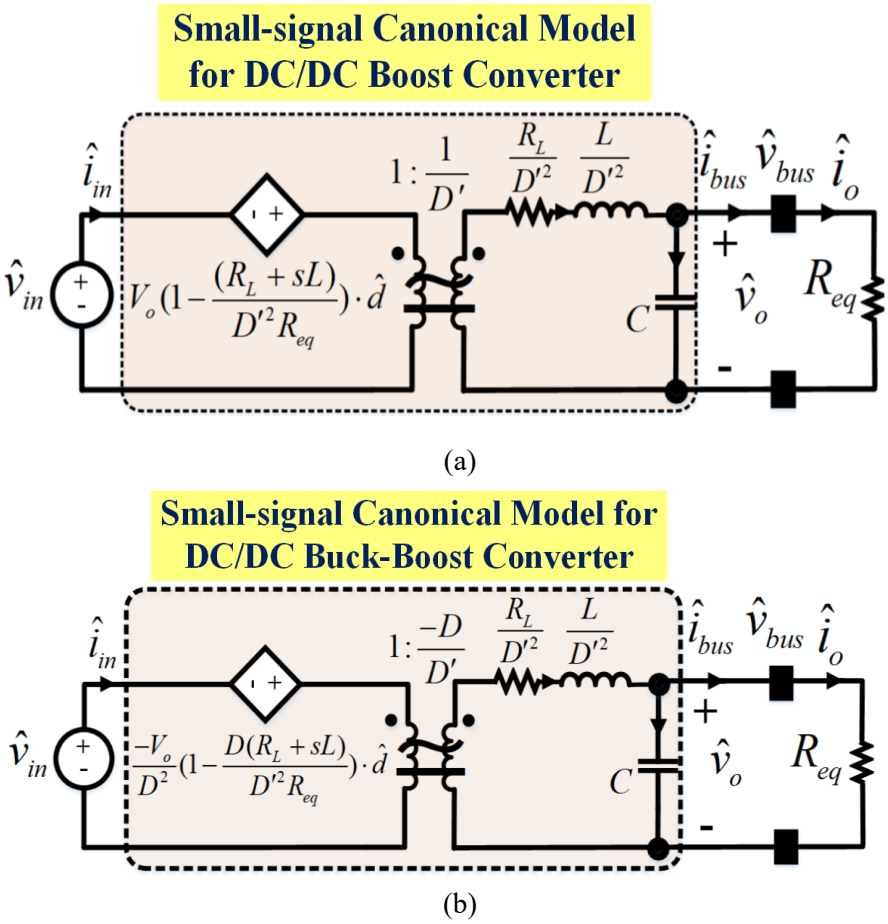



Fig. 4.11. Circuit schematic of small-signal averaged equivalent model of DC/DC converters feeding multiple CPLs. (a) boost converter. (b) buck-boost converter [16].

by replacing $\hat{d}_{new}=\hat{d}+\left[K_{AD}(R_L+sL)\hat{i}_o/V_{Tr}\right]$ instead of $\hat{d}$. As clearly shown in Fig.4.12, the APVR control strategy leads to the introduction of voltage and current dependent sources ($I_{AD}$ and $V_{AD}$) to the corresponding equivalent circuit. Fig.4.13 illustrates another analytical interoperation of Fig.4.12. According to the DC relationship governing DC/DC converters (inductor voltage-second balance),

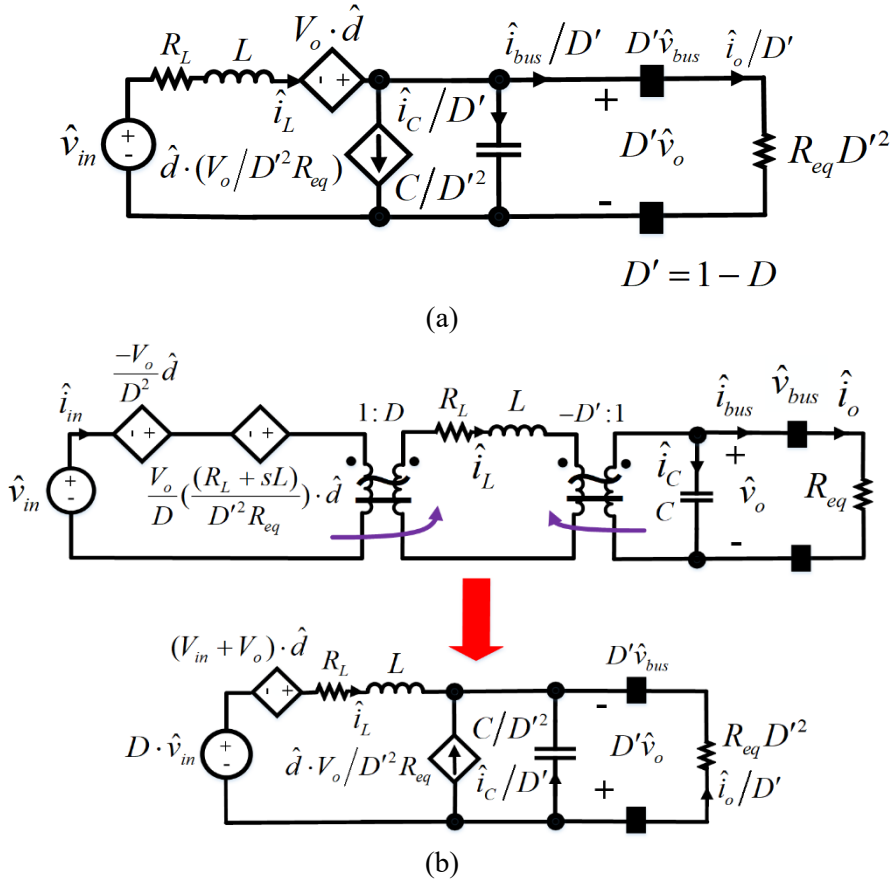



Fig. 4.12. Simplified small-signal averaged equivalent circuit. a) DC/DC boost converter. (b) DC/DC buck-boost converter [16].

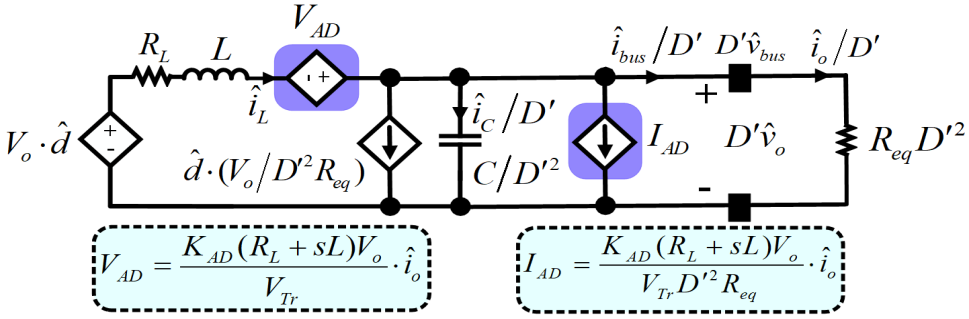



Fig. 4.13. A modified small-signal averaged equivalent circuit of Fig. 4.12(a) with applying APVR control strategy [16].

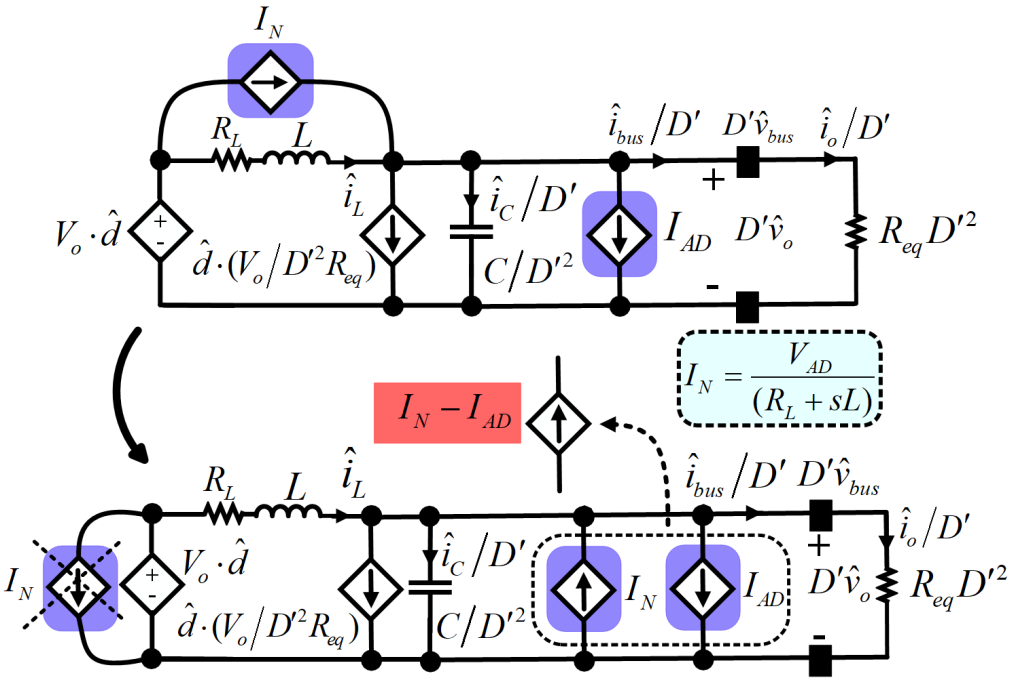



Fig. 4.14. Another analytical commentary of Fig. 4.13.

**Simplified Model for DC/DC Boost Converter**

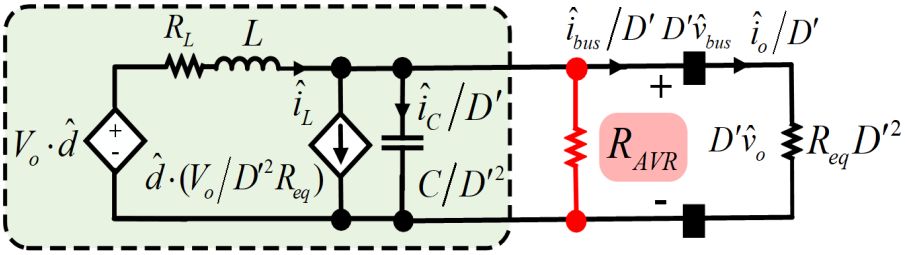



Fig. 4.15. The circuit physical concept of the APVR control strategy applied to Fig 4.12(a).

$$I_N - I_{AD} = \frac{K_{AD} V_o \hat{i}_o}{V_{Tr}} \cdot \left[ 1 - \frac{(R_L + sL)}{D'^2 R_{eq}} \right] \cong \frac{K_{AD} V_o \hat{i}_o}{V_{Tr}} \cdot \tag{4-8}$$

Since $\hat{i}_o = \frac{\hat{v}_o}{R_{eq}}$, $R_{APVR}$ can be derived as

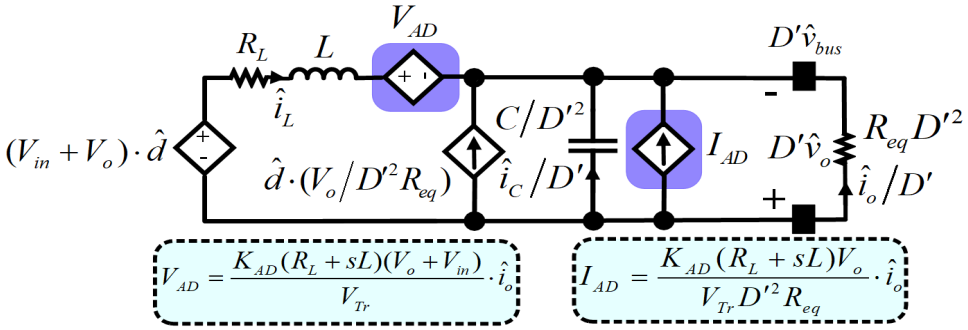



Fig. 4.16. A modified small-signal averaged equivalent circuit of Fig. 4.12 (b) with applying APVR control strategy.

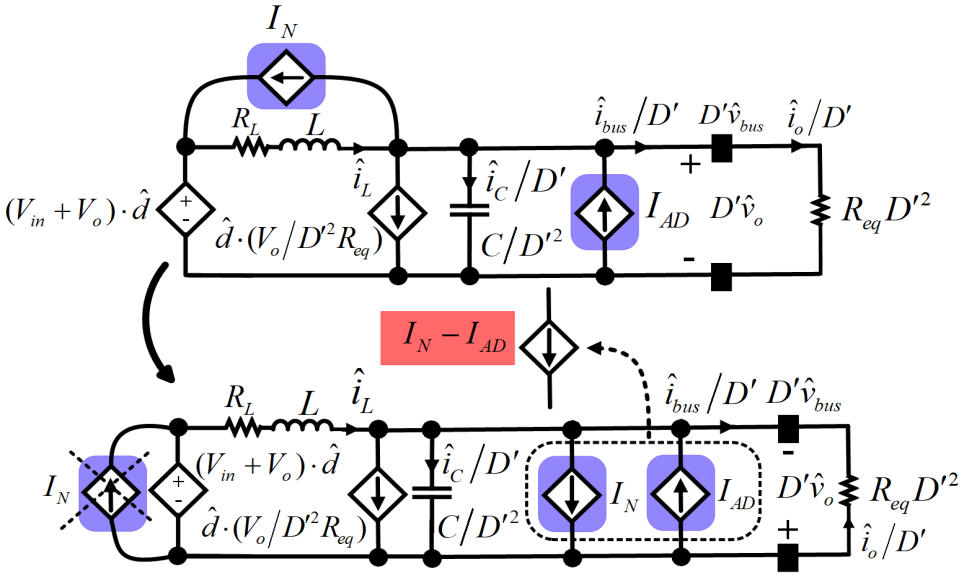



Fig. 4.17. Another analytical commentary of Fig. 4.16.

$$\frac{D'\hat{v}_o}{I_N-I_{AD}}=-\frac{D'V_{Tr}R_{eq}}{K_{AD}V_o}=R_{APVR}\cdot \tag{4-9}$$

Therefore, according to Fig. 4.15, this control approach presents an appealing circuit physical meaning that leads to the virtual modification of the equivalent circuit shown in Fig.4.12(a). Moreover, the realization process of APVR

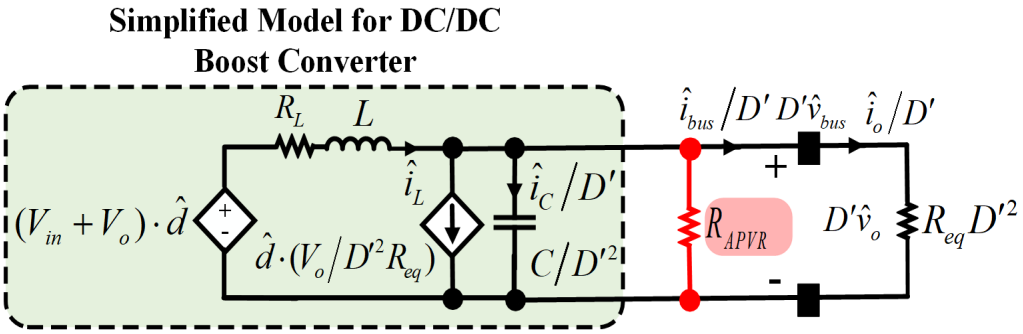



Fig. 4.18. The circuit physical concept of the APVR control strategy applied to Fig 4.12(b).

method on the buck-boost converter loaded with multiple CPLs has been displayed in Figs.4.16 to 4.18. After simplification, $I_N - I_{AD}$ can be achieved as follows;

$$I_N - I_{AD} = \frac{K_{AD} V_o \hat{i}_o}{V_{Tr}} \cdot \left[ (V_{in} + V_o) - \frac{V_o (R_L + sL)}{D'^2 R_{eq}} \right] \cong \frac{K_{AD} (V_{in} + V_o) \hat{i}_o}{V_{Tr}} \cdot \quad (4\text{-}10)$$

Consequently, the outcome of this process leads to a similar control realization as shown in Fig. 4.18, where $R_{APVR}$ can be obtained as

$$\frac{D'\hat{v}_o}{I_N - I_{AD}} = -\frac{D' V_{Tr} R_{eq}}{K_{AD} (V_{in} + V_o)} = R_{APVR} \cdot \quad (4\text{-}11)$$

b) Designing of Effective AD Control Coefficient

Based on (4-9) and (4-11), if $R_{APVR} \langle \left| D'^2 R_{eq} \right|$ is satisfied, the stability of the systems illustrated in Figs. 4.15 and 4.18 is guaranteed by actively overcoming for the CPL instability. Besides, it meets the Routh's stability criterion for (4-12) and (4-13).

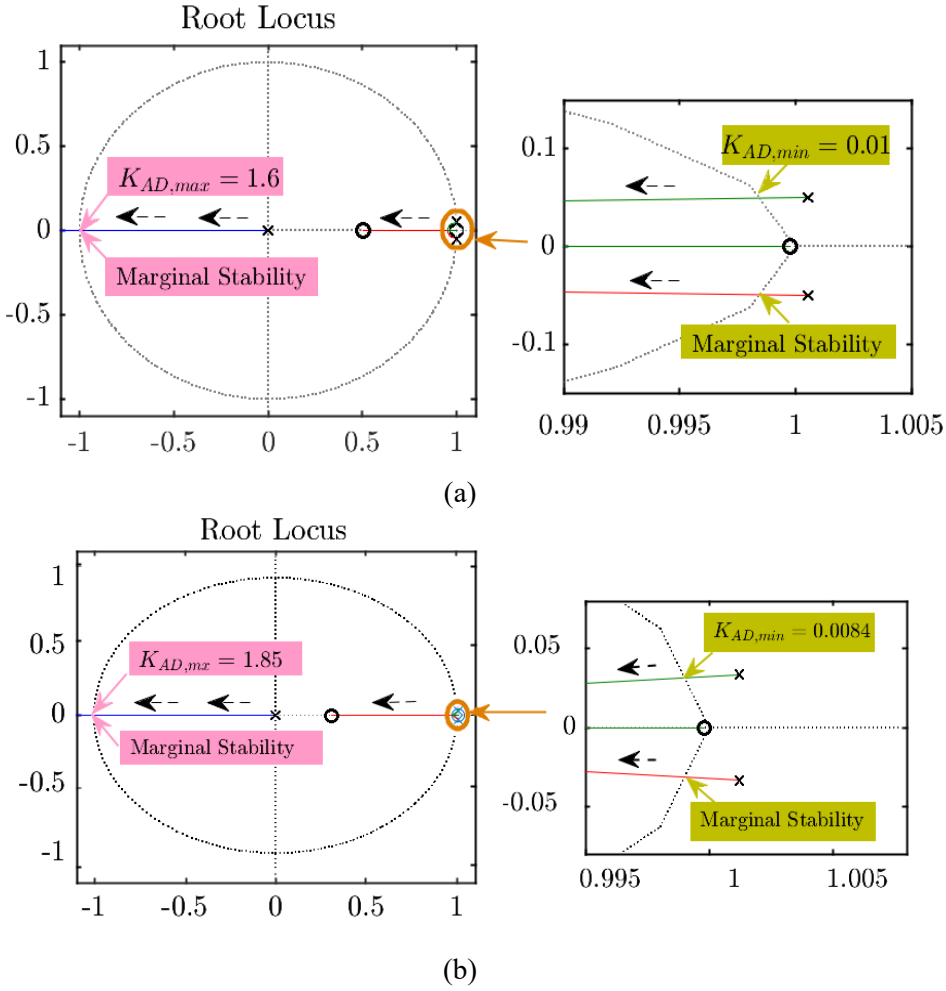



Fig. 4.19. Root locus of control-to-output transfer function based on KAD changes effect for DC/DC converters supplying CPLs. (a) boost. (b) buck-boost [16].

$$\text{(Boost)} \quad \frac{\hat{v}_o}{\hat{d}} = \frac{D'V_o - I_L(R_L + sL)}{LC.s^2 + (R_L C + \frac{L}{H}).s + (D'^2 + \frac{R_L}{H})}. \tag{4-12}$$

$$\text{(Buck-Boost)} \quad \frac{\hat{v}_o}{\hat{d}} = \frac{D'(V_{in} + V_o) - I_L(R_L + sL)}{LC.s^2 + (R_L C + \frac{L}{H}).s + (D'^2 + \frac{R_L}{H})}. \tag{4-13}$$

where,

- $H = R_{APVR} \| R_{eq}$ .
- (Boost) $I_L \cong \frac{V_o}{R_{eq} D'}$ .
- (Buck-Boost) $I_L \cong \frac{V_o}{R_{eq}} (\frac{D^2}{D'} + D)$ .

Consequently, the minimum $K_{AD}$ related to these systems are respectively attained by (4-14) and (4-15).

$$\text{(Boost)} \quad K_{AD,\min} = \frac{V_{Tr}}{D' V_o} \cong \frac{V_{Tr}}{V_{in}} . \tag{4-14}$$

$$\text{(Buck-Boost)} \quad K_{AD,\min} = \frac{V_{Tr}}{D'(V_{in} + V_o)} \cong \frac{V_{Tr}}{V_{in}} . \tag{4-15}$$

Afterwards, using a discrete root locus, stability analysis has been accomplished by considering the delays of the control system to examine the effect of $K_{AD}$ changes and also to determine the stability band (maximum permissible $K_{AD}$). According to the parameters given in Table 3.2, the root loci of (4-12) and (4-13) in accordance with are plotted in Figs. 4.19(a) and (b), respectively. It is obvious that without APVR control strategy, the system is initially unstable. By applying the AD stabilization technique, the unstable poles move to the inside of the unit circle by increasing the $K_{AD}$ $(K_{AD} \rangle K_{AD,\min})$, and then the stability of the systems are authenticated. Considering delays, the increase of $K_{AD}$ from a specified value, $K_{AD,\max}$ ((boost=1.6), (buck-boost=1.85)), result in a gradual reduction in

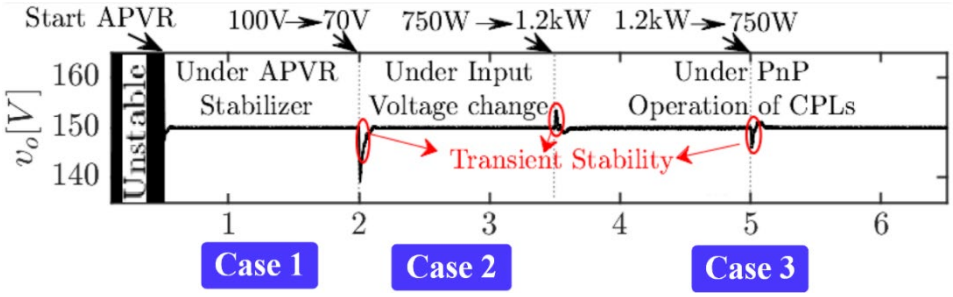



Fig. 4.20. Simulation result of output voltage for the boost converter feeding CPLs under three operation cases [16].

the damping rate and exit of the poles from the unit circle, and ultimately system instability. Finally, the allowable stability band for the cascaded systems demonstrated in Figs. 4.11(a) and (b) can be specified as [0.01,1.6] and [0.0084,1.85], respectively. Given that (4-14) and (4-15) are inversely dependent on the value of $V_{in}$, $K_{AD,eff}$ must be selected much bigger than $K_{AD,\min}$. In addition, since the proposed AD stabilization method inherently has load adaptive online self-tuning characteristic, robust stability will also be well achieved for these cascaded systems with optimal transient and dynamic responses.

### 4.3.3 Simulation and Experimental Results

The effectiveness of the APVR-based AD stabilization approach on the boost and buck-boost converters supplying multiple CPLs in DC MGs has been evaluated using discrete time-domain simulations in Matlab/Simulink and by considering the control system delays. Moreover, the feasibility and applicability of the presented APVR control strategy in the actual conditions have also been tested using the built laboratory rack (see Fig. 4.8). The system parameters given in Table 3.2 are considered for simulated models and laboratory implementations. Like the buck converter, the performance

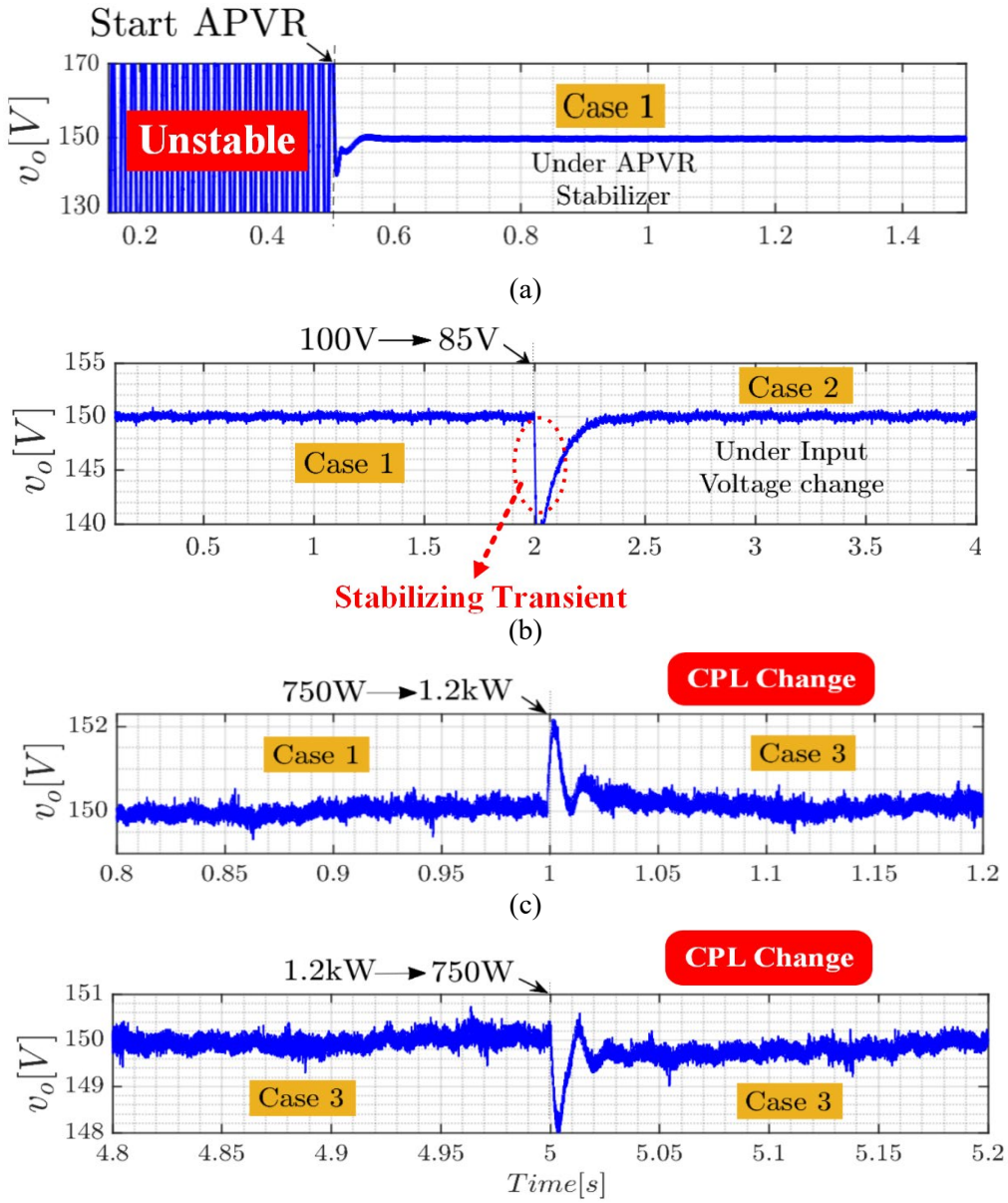



Fig. 4.21. Experimental results of the boost converter feeding CPLs. (a) Output voltage with and without APVR strategy. (b) Output voltage nder input voltage change. (c) Output voltage under PnP of CPLs. (d) Switch duty cycle under CPL power rating change [16].

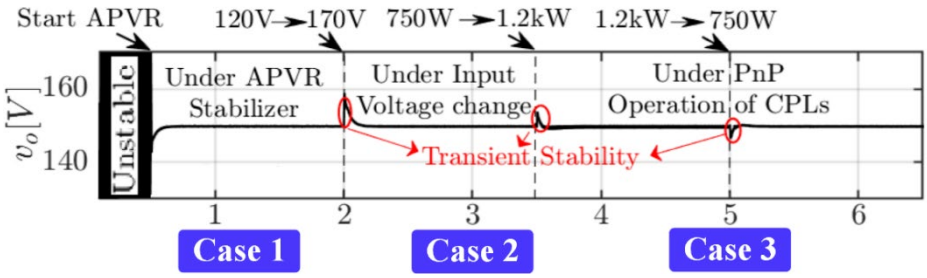
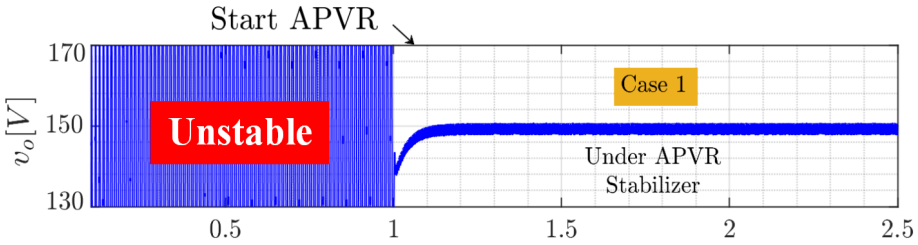
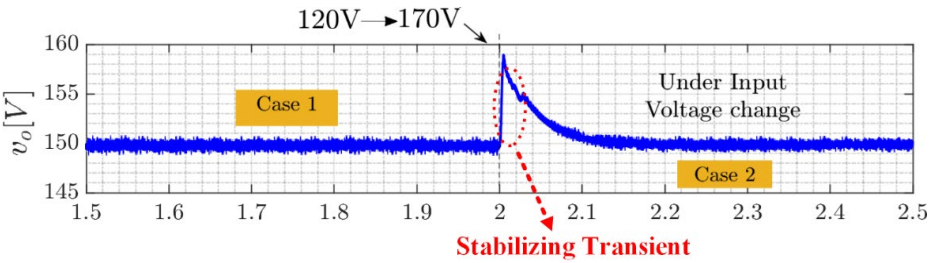



Fig. 4.22. Simulation result of output voltage for the buck-boost converter system supplying CPLs under three operation cases.

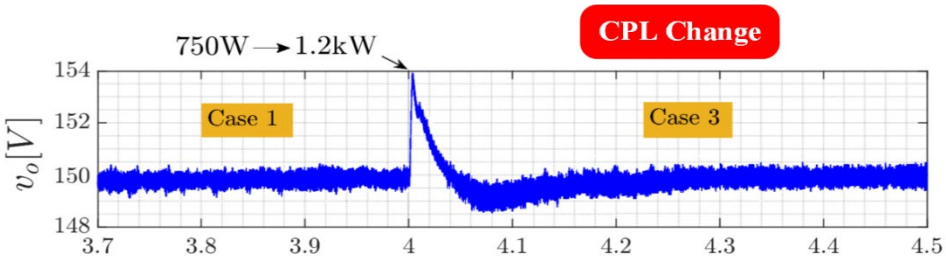
transient and dynamic of the system under three operational cases have studied in both simulation and experimental tests. In these assessments $K_{AD} = 0.2(R_{APVR} = 776.5\ m\Omega)$ and $K_{AD} = 0.17(R_{APVR} = 346\ m\Omega)$ have been respectively selected for the boost and buck-boost converters supplying CPLs. As seen from Figs. 4.20, 4.21(a), 4.22, and 4.23(a), in case 1, without applying the proposed AD stabilizer, instability fluctuations appear in the bus voltage due to the CPLs. Once the APVR control loop is activated, the sever oscillations of the output voltage are speedily reduced, leading to system stability. Then, to assess the robustness of the presented stabilization idea, the transient stability and dynamic performance of the cascaded systems are also investigated in cases 2 and 3. In this way, a 30% reduction in the input voltage level has been applied in Case 2 (see Figs. 4.20, 4.21(b), 4.22, and 4.23(b)). In Case 3, the PnP performance of the CPLs has been evaluated in Figs. 4.20, 4.21(c) and (d), 4.22, and 4.23(c) and (d). Under this anticipated variation in the load level, the controller automatically updates initial $K_{AD}$ (adaptive pure positive virtual resistance) for these systems to its new values. $K_{AD,new} = 0.34(R_{APVR,new} = 266.8\ m\Omega)$ and $K_{AD,new} = 0.29(R_{APVR,new} = 118.9\ m\Omega)$ respectively. Afterward, by disconnecting CPL2 and reconnecting CPL1 to the DC bus, damping gain is automatically returned to its primary value. Evidently, according to the results obtained from PnP operation of CPLs, the



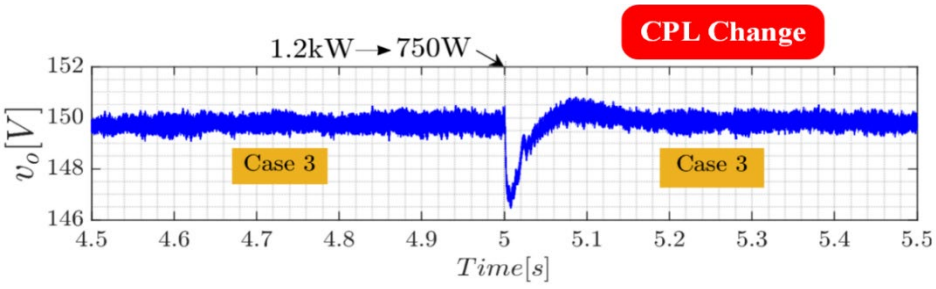

(a)




(b)




(c)




(d)

Fig. 4.23. Experimental results of the buck-boost converter. (a) Output voltage with and without APVR strategy. (b) Output voltage under input voltage change. (c and d) Output voltage under PnP of CPLs [16].

DC bus voltage reaches its desired level with stable transitions and very rapid dynamic responses. As a result, it can be concluded that CPL instability is effectively compensated for using the source-side APVR-based AD stabilization scheme, provided that $K_{AD}$ satisfies the stability conditions by inserting a well-designed load adaptive resistive damper.

## 4.4 Comparison with H∞-Robust Control Method

### 4.4.1 Methodology

In [14], we have been designed H∞ method-based robust controller for a buck converter system loaded with a CPL in DC MG, taking into account significant changes in load and input voltage levels. The simulation implementation was done based on the parameters determined in Table 4.3. In the first step, the small-signal averaged model of buck converter feeding CPL operating in continuous conduction mode was derived. According to the H∞ scheme, the cascaded system with perturbations are cumulated into a single perturbation block, $\Delta_m(s)$, which is known as an unstructured uncertainty.

Table. 4.3 system parameters [14]

| Description | Parameter | Value |
|---|---|---|
| Converter Filter Inductance | $L$ | $20mH$ |
| Converter Filter Capacitance | $C$ | $350\mu F$ |
| Inductance ESR,$r_L$ | $r_L$ | $45m\Omega$ |
| Capacitance ESR,$C$ | $r_C$ | $5m\Omega$ |
| Load Resistance | $R_{Load}$ | $470\Omega$ |
| CPL Power | $P_{CPL}$ | $3kw$ |
| DC Power Supply | $V_{in}$ | $100V$ |
| Desired Output Voltage | $V_O$ | $75V$ |
| Switching frequency | $f_{sw}$ | $10\ KHz$ |
| Average duty cycle | $D$ | 0.75 |

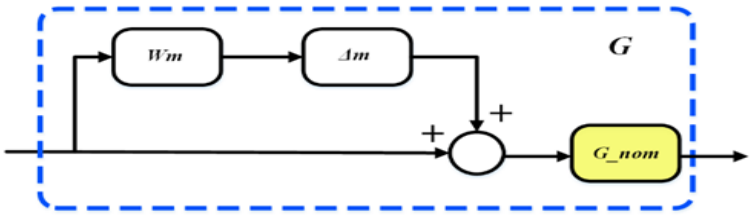



Fig. 4.24 Model with multiplicative uncertainty [14].

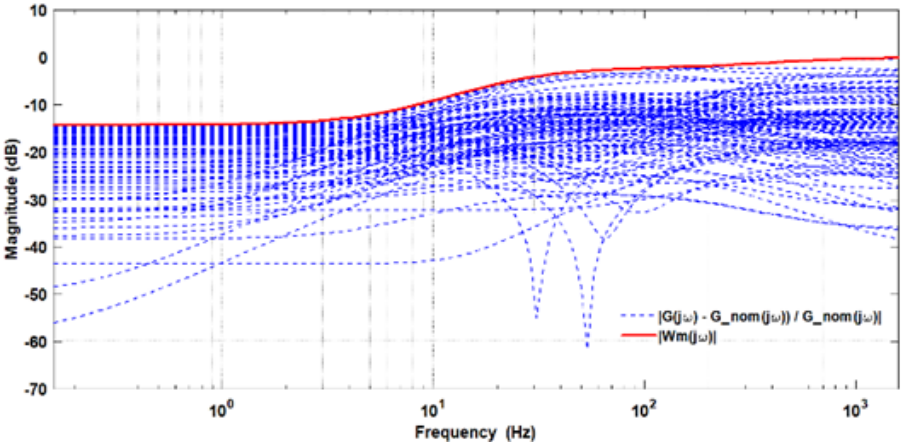



Fig. 4.25 Transfer function by the multiplicative uncertainty modeling [14].

To model uncertainty, a multiplicative perturbation technique is used in this work [14]. The block diagram of the plant with multiplicative uncertainty is illustrated in Fig. 4.24. Therefore, the system transfer function under uncertainty is achieved as

$$G = \left[1 + W_m(s) * \Delta_m(s)\right] + G_{nom}(s), \qquad \left|\Delta_m(jw)\right| \le 1 \cdot \tag{4-16}$$

In this model, $20\%$ variations in input voltage amplitude has been considered as uncertainty. According (4-17), $W_m(jw)$ can be obtained through calculating the upper limit of the relative error domain response (see Fig. 4.25). Hence, $W_m(s)$ can be derived as Generally, as depicted in Fig. 4.26, any system with the linear interconnection of inputs, outputs, system perturbations, and the

controller, can be adapted to the closed-loop model using linear fractional transformation (LFT) structure [14],[51].

$$W_m(s)=\frac{(1.004s^2+2996s+(8.388\times10^4)}{s^2+3025s+(4307\times10^5)}. \tag{4-17}$$

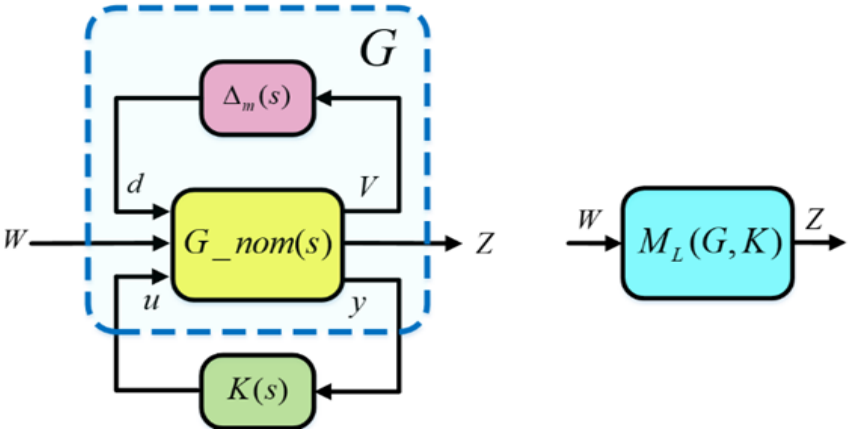



Fig. 4.26 LFT configuration [14].

$G_{nom}(s)$ is defined as the open-loop transfer function, and $K(s)$ is the controller. As a principle, the main aim of a robust controller design is minimizing the $M_L(G,K)$, i.e., satisfying $\|M_L(G,K)\|_\infty \langle 1$. According to Fig. 4.27, the matrix model of the closed-loop system can be obtained as

$$\begin{bmatrix} Z_1 \\ Z_2 \end{bmatrix}=\begin{bmatrix} GK(1+GK)^{-1} & (1+GK)^{-1} \\ -G(1+GK(1+GK)^{-1}) & 1-G(1+GK)^{-1} \end{bmatrix}\begin{bmatrix} W_1 \\ W_2 \end{bmatrix}. \tag{4-18}$$

where $Z=T_mW$.

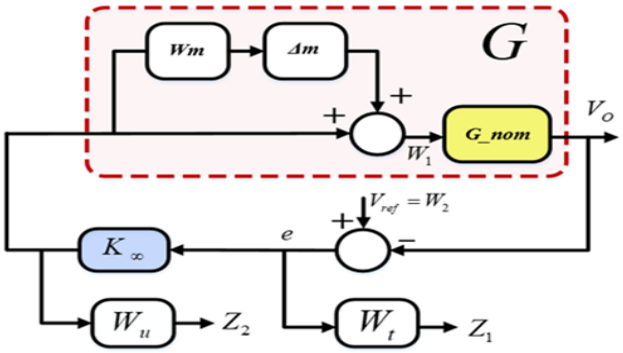


Fig. 4.27 The closed-loop system of the robust controller approach based on H infinity [14].

$W_t$ and $W_u$ are weight functions that represent the amount of the controller effort and penalty in the error tracking, respectively. Appropriate weight functions are selected as

$$\begin{cases} W_t = \dfrac{0.625(s+1040)}{s+2} \\ W_u = 0.01 \end{cases} \tag{4-19}$$

Using the robust control strategy provided in Fig. 4.27 and the choosing of the suitable weighting functions, $K_\infty$ can be obtained as (4-20) so that minimize $\|\cdot\|_\infty$ from $W$ to $Z$ [14],[52].

$$K_\infty(s) = \frac{((4.805\times10^6)s^2 + (1.789\times10^9)s + (1.716\times10^{11}))}{(s^3 + (2.906\times10^5)s^2 + (1.794\times10^{10})s + (3.588\times10^{10}))}. \tag{4-20}$$

### 4.4.2 Simulation Results and Comparison Study

According to the parameters specified in Table 4.3, this robust control scheme was conducted in the MATLAB/SimPowerSystems toolbox for the evaluation of dynamic and transient performances under sudden changes in the input voltage.

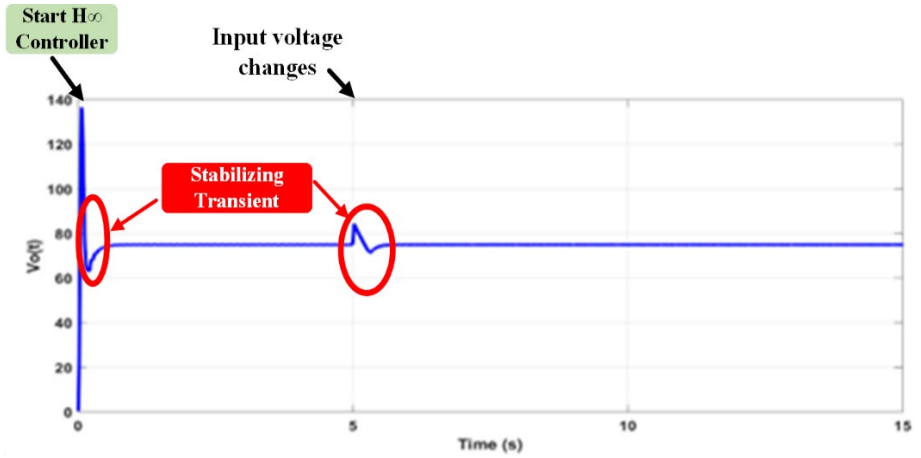



Fig. 4.28 Output voltage with applying H∞ controller under variations in input voltage.

In Fig. 4.28, the effectiveness of the H∞ method-based robust controller against a 20% change in the input voltage amplitude (t= 5 sec) is demonstrated. It can be concluded that under this technique in the presence of uncertainty in input voltage, system becomes stable with transient recovery time longer and more transient deviation compared with the proposed AD-based stabilization methods. It should be noted that the result is obtained under a specified CPL value. It means that the conventional H∞ controller design in the presence of severe variations in CPL power rating or PnP operation as well as step changes in voltage level of the output reference will not be practical. Therefore, to address this important issue, we will have to develop and enhance the design process of conventional H∞ control strategy under various performance scenarios. As a result, it will lead to complexity in the control structure and its design process. Moreover, under this strategy, there will be no guarantee of achieving a similar control structure applicable to all the basic DC/DC cascaded systems feeding multiple CPLs in different operating conditions, which is one of the main benefits of the proposed active stabilization schemes in Chapters 3 and 4.

# Chapter 5
# Conclusion and Future Work

*The conclusion and future works of this research based on papers are presented in this section*

## 5.1. Conclusion

Cascaded structures of source- and load-side circuits are known as the dominant configuration in multi- converter-based LVDC networks (e.g., DC MGs). Despite instability arising from interactions between the individually designed feedback-controlled converters, supplying active loads that are tightly-regulated such CPLs can yield system instability. Thus, this thesis studied the instability issues induced by CPLs in these types of networks, including modeling, stability analysis, active stabilization strategies and their control realization at the source-side level. In order to do so, in the first step, a novel virtual series *RC* damper-based source-side active stabilization scheme was proposed to suppress the CPL's instability effects of these configurations in DC MGs applications without affecting the dynamic performance of the load set. This active stabilization technique provides a design-oriented control strategy utilizes a easy control mechanism with simple parameter adjustment to achieve a reliable and robust stability level. In addition, a comparative study through experimental and simulation results was conducted to show the superiority and advantages of this technique's contributions over the stabilization methods that were close to our control idea. The results of these comparison studies indicated a significant improvement in the speed of the stabilizing transient and dynamic responses, as well as high robustness under

unforeseen changes in the system, including the variation in input voltage amplitude and changes at the load level by the proposed AD stabilization technique. However, although the *RC* damper-based AD strategy improves substantially damping rate and phase margin stability, and ultimately fixes the instability issue of these systems by further increasing capacitance value, it may adversely affect the speed of system dynamic responses under different operational cases. Therefore, in the next step, the aim was to overcome this limitation. Hence, the APVR control strategy-based stabilization scheme applied to the source side subsystem was proposed as a supplement of the presented technique in the first step. This approach has been achieved by a positive proportional-derivative feedback of the equivalent load current with an intrinsic self-tuning control parameter, which has provided the fast and desirable dynamic performance under different operating conditions. This is achieved by the virtual insertion of an adaptive positive resistance in parallel to the output of the source converter without disrupting the desirable dynamic performance of the load converter. The flexibility, compatibility, and modularity of the proposed stabilization methods were well-demonstrated by applying to the three cascaded systems consisting of the main DC/DC converters (Buck, Boost, and Buck-Boost) supplying multiple CPLs using only a similar and unique control structure but with different analytical concepts. The operational principles and control concepts achieved by the active stabilizers strategies proposed for the three cascaded systems were discussed analytically and individually. The obtained results confirmed the effectiveness and robustness of the proposed schemes with the fast and desired dynamic response for different operational scenarios including variation in input voltage amplitude, load changes, PnP of the CPLs, and step changes in output voltage reference. Eventually, transient stability and dynamic performance of the proposed AD control approaches were evaluated by

performing simulations in MATLAB/Simulink environment in the discrete-time domain, and the outcomes were verified experimentally by laboratory tests to validate the authenticity, applicability, and effectiveness of the proposed techniques in real life. These experimental implementations were accomplished on three cascaded systems (Buck, Boost, and Buck-Boost converter systems connected to programmable DC loads in constant power mode and resistive load) using IGBT power module PEB4050 and dSPACE real-time 1202 (Microlab Box) in the control part, separately.

The principle of the proposed novel AD -based stabilization schemes is well generalizable for more complex DC networks. However, since the cascading connection of the power converter systems is a predominant form in the DC MGs, addressing the instability problem in a typical DC cascaded system including one source converter feeding a resistive load and multiple CPLs can be considered as a necessary precondition to develop the proposed stabilization techniques for more complex DC networks with multiple sources. In the case of multiple source converters, by considering the entire source system configuration as the Thevenin equivalent circuit and applying the superposition theorem for each source, the stability analysis derived can be the same with cascaded structures except that the load equivalent resistance may be affected by the impedance interactions of other sources.

However, with the presence of multiple source converters in a more complex DC network, investigating the control interactions, proper interleaving, and desirable load sharing among the converters to achieve a generalized control scheme is an important issue. In this case, we will face challenges that exploring and resolving them in this thesis lead to the dispersal of the subject and the loss of the main focus in the present work. Therefore, the study and generalization of the proposed stabilization techniques for a

more complicated DC network with multiple source converters will be considered as one of the future research topics.

## 5.2. Future Work

- Investigate how to generalize the proposed active stabilization techniques for more complex DC MGs containing multiple source converters linked to the DC bus. However, on this path, we will face some challenges relating to source converters which are:

➢ Interactions between their control loops,

➢ Interleaving issues among the converters,

➢ load sharing and simultaneous startups.

- Investigate the stability issues for DC MGs in the simultaneous presence of dynamic loads and CPLs and design the developed active stabilization strategies for them.

- Design the data-driven (model-free)-based control strategies for cascaded systems in DC microgrids and their generalization into complex DC MGs containing multiple source converters.

- Investigate and design the developed schemes for stability and control of DC MGs based on Machine learning techniques.

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