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FROM COMPONENT TO CONVERTER

BY
UIMIN CHOI

DISSERTATION SUBMITTED 2016

AALBORG UNIVERSITY
DENMARK

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Uimin Choi

February, 2016

Aalborg, Denmark

ABSTRACT

As power electronic systems have gradually gained an important status in a wide range of industrial applications, there are increasing demands to improve the reliability and robustness of power electronic systems. The power electronic systems consist of various components, and among them, power semiconductor devices are one of the most fragile components. Thus, they play a key role in the robustness and reliability of the overall power electronic systems.

Insulated Gate Bipolar Transistor (IGBT) power modules are the most widely used of their kind and the temperature stress is a major stressor that kills IGBT modules. Therefore, in order to improve the reliability of power electronic systems, reliability research on reliability-critical components regarding the major critical stressors are needed. In this PhD project, various researches on reliability of the IGBT module are performed from component level to converter level.

It is divided into two main parts: the first part, which consists of Chapters 2 and 3, is reliability studies of the IGBT module regarding thermal stresses and the second part, composed of Chapters 4 and 5, discusses strategies to improve the reliability and availability of power electronic converters under IGBT failure conditions. The apparatus and methodology for an advanced accelerated power cycling test of IGBT modules are presented in Chapter 2. Further, an improved junction temperature estimation method is also proposed as well as power cycling test results are presented. Then, in Chapter 3, the effect of junction temperature swing duration $t_{\Delta Tj}$ on the lifetime of the transfer molded Intelligent Power IGBT Module is investigated and modeled based on the power cycling test results. In addition, the physics-of-failure analysis results of the tested modules are presented. Finally, in Chapters 4 and 5, open-circuit fault detection and fault-tolerant control methods are proposed for two kinds of neutral-point clamped three-level inverters T-type and NPC inverters.

One of main contributions in this project is the development of an apparatus and methodology for advanced accelerated power cycling test of IGBT modules. It allows performing the reliability test regarding temperature stresses under more realistic electrical conditions in an efficient way. Therefore, a more practical reliability assessment of power IGBT modules can be achieved with respect to lifetime as well as failure mechanisms. Furthermore, it introduces new control strategies to improve the reliability and availability of two types of the neutral-point clamped three-level converters under open-circuit fault conditions.

The feasibility and effectiveness of this project are verified by various experimental results.

DANSK RESUME

Effektelektroniske systemer har efterhånden fået en særdeles vigtig betydning i en lang række industrielle applikationer, og der er et stigende behov for at forbedre pålideligheden og robustheden af de effektelektroniske systemer. Sådanne systemer består af forskellige komponenter, og blandt dem, er effekthalvlederkomponenterne nogle af de mindst robuste komponenter. De har dermed en central rolle i robustheden og pålideligheden af de samlede effektelektroniske systemer.

Insulated Gate Bipolar Transistoren (IGBT) er den mest udbredte komponent-type og temperaturen er en stor stressfaktor for denne og er med til at reducere levetiden. IGBT'rne samles i moduler for at reducere produktions-omkostninger. For at forbedre pålideligheden af effektelektroniske systemer, er studier omkring de mest pålideligheds kritiske komponenter under de omtalte stressfaktorer nødvendige. I dette ph.d.-projekt er forskellige undersøgelser af pålideligheden af IGBT-moduler udført fra komponentniveau til effektkonverter niveau.

Afhandlingen er opdelt i to hoveddele: den første del, som består af kapitel 2 og 3, gennemfører pålideligheds undersøgelser af IGBT moduler, når de er udsat for termiske belastninger og den anden del, der er kapitel 4 og 5, diskuterer strategier til at forbedre pålideligheden og tilgængeligheden af effektelektroniske konvertere under fejltilstande i IGBT'erne. Test-system og metoder til at gennemføre en avanceret accelereret test af IGBT modulerne er præsenteret i kapitel 2, som indebærer termisk cycling af komponenterne. Endvidere er en forbedret estimering af IGBT krystal temperaturen også foreslået, og der er præsenteret testresultater i samme kapitel. I kapitel 3 er levetiden på støbte Intelligent Power IGBT Moduler undersøgt, hvor temperaturen og dens varighed $t_{\Delta Tj}$ er varieret og modelleret baseret på en række test-resultater på et udviklet test system. Desuden er physics-of-failure analyser af de testede moduler også fremlagt. I kapitel 4 og 5 foreslås intelligent fejlfinding og fejltolerante kontrol-metoder, når transistorerne fejler (er åbne og kan ikke lede strøm) for to slags tre-niveau invertere (T-type og NPC-type), som eksempelvis kan anvendes til at net-tilslutte solceller.

Et af de vigtigste bidrag i dette projekt er at udvikle et test-system og test metoder til avanceret accelereret temperatur cycling af IGBT moduler. Det gør det muligt at udføre pålideligheds-test i forhold til temperatur belastninger under meget realistiske elektriske forhold. Dermed kan en mere reel pålidelighedsvurdering af IGBT modulerne opnås med hensyn til at bestemme levetid, samt forstå hvilke brud-mekanismer, der opstår i IGBT modulerne, når de stresses termisk. Desuden foreslås nye kontrolstrategier til at forbedre pålideligheden og tilgængeligheden af to typer effekt-omformere, som har fejltilstande ved at være åbne. Projektet er samtidig underbygget via en række forskellige eksperimentelle resultater.

TABLE OF CONTENTS

CHAPTER 1. INTRODUCTION

This chapter presents the background and motivation of this research project followed by its objectives. Then, the thesis outline is presented. Finally, all publications related to this research work are listed at the end of the chapter.

1.1. RELIABILITY IN POWER ELECTRONICS

The power electronics play a still more important role in various applications such as renewable generation, automotive, motor drives, aerospace and railway transportation to achieve efficient conversion of electric energy from one stage to another stage and also achieve high performance of the systems [1-4]. In 1973, William E. Newell defined the scope of power electronics that is interstitial to all three of the major disciplines of electrical engineering: electronics, power, and control as shown in Fig. 1-1 (a) [5]. The field of power electronics has grown during the last few decades, especially in terms of efficiency and density, by taking advantage of innovative solutions in active and passive components, digital signal processor, circuit topologies, control strategies and systems integration [4, 6].

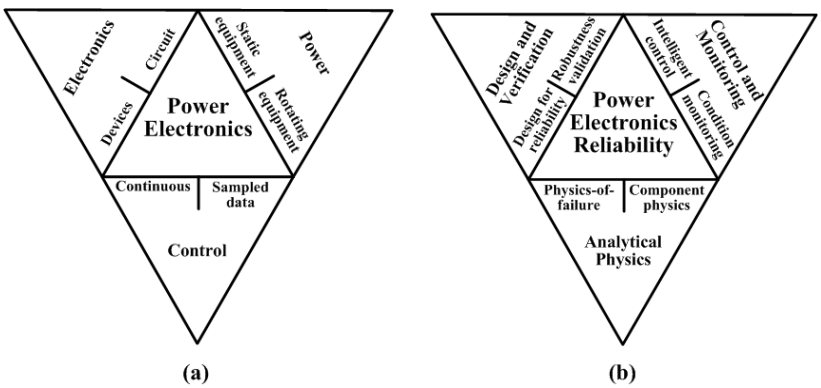

Fig. 1-1 Defined scopes of (a) power electronics by William E. Newell in 1973 (b) power electronics reliability by CORPE in 2010 [7].

As power electronics have gradually gained an important status in a wide range of industrial fields for power generation, distribution and consumption, recent research endeavors to improve the reliability of power electronic systems to comply with more stringent constraints on cost, safety and availability in various applications [7, 8]. Automotive and Aerospatiale industries have brought increasingly stringent reliability constraints into their power electronic systems because of their safety

requirements. Additionally, other industrial fields are also following the same trend that is improving the reliability of power electronics systems with cost-effective and sustainable solution [6].

Recently, the reliability research in power electronics has been defined by the Center of Reliable Power Electronics (CORPE) which is a strategic research center between industry and universities, led by Aalborg University, Denmark. It also includes multi-disciplinary knowledge as shown is Fig. 1-1 (b) [6, 7]. There are three major aspects to be able to concern:

- Analytical analysis based on physics-of failure in order to understand root cause of failure and failure mechanism of power electronic products.

- Design For Reliability (DFR) and robustness validation process in order to meet the expected lifetime and failure rate of products.

- Intelligent control and condition monitoring in field operation to improve the reliability and availability of products.

Nowadays, much research about reliability have been performed in the power electronics field considering the above aspects such as reliability tests and physics of failure analysis of failure root and failure mechanisms [9-11], lifetime modeling and prediction [12-15], active thermal control [16-18], condition monitoring [19-23], and fault-tolerant strategies [22-26], as examples of a dynamic research field.

1.1.1. FIELD EXPERIENCES OF FAILURES IN POWER ELECTRONIC SYSTEMS

Examples of field experiences in photovoltaic (PV) and wind power systems show that the power electronic converters are one of the most critical parts in terms of failure rate, lifetime and maintain cost [27-29].

Fig. 1-2 shows the unscheduled maintenance events and costs by the subsystems based on field experiences between 2001 and 2006 in a large utility-scale PV generation plant. The PV inverter covers 37 % of unscheduled maintenance events and make up 59 % of unscheduled maintenance costs [27]. Therefore, PV inverter is one of the important parts in respect of reliability in overall PV system and also to reduce the cost of operation.

In the case of wind turbine systems, around 350 wind turbines from multiple manufacturers have been investigated [28]. The downtime events have been analyzed for 10-minute average Supervisory Control and Data Acquisition

(SCADA) data, fault/alarm logs, work orders, service reports and operation and maintenance (O&M) reports. Totally, 35,000 downtime events have been considered to determine the distribution of failure rates and downtimes between the sub-assemblies.

Fig. 1-3 shows the contribution of subsystems and assemblies to the normalized failure rate and downtime of wind turbine. The power electronic frequency converter accounts for 13 % of the overall normalized failure rate and 18.3 % of the overall normalized downtime of the investigated wind turbines. It can be seen from the result that the power electronic converter is also one of the important parts in terms of reliability in wind turbine system. Another study has also been performed in [29] where more than 6000 onshore wind turbines and their subassemblies in Denmark and Germany have been investigated for 11 years. Similar results are derived that the power converter is one of the subassemblies, which have the highest failure rates in wind turbine system.

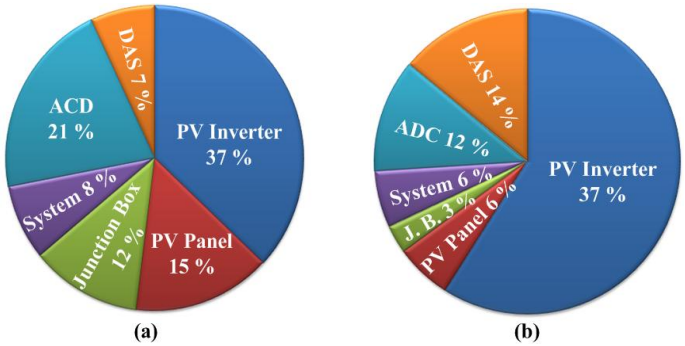

Fig. 1-2 Field experiences of system maintenance in PV generating plant [26]
(a) Unscheduled maintenance events by subsystem. (b) Unscheduled maintenance costs by subsystem.

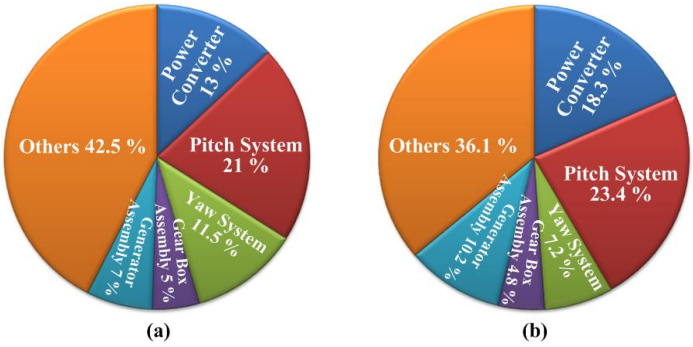

Fig. 1-3 Failure rate and downtime results of sub-systems and assemblies in wind turbine systems [27] (a) normalized failure rate (b) normalized downtime.

1.1.2. RELIABILITY CRITICAL COMPONENTS IN POWER ELECTRONICS

The power electronic systems consist of various components as shown in Fig. 1-4. Each component affects the reliability and robustness of the overall systems and, especially, reliability-critical components play a key role in the robustness and reliability of the overall power electronic systems.

Two surveys were performed to investigate the reliability critical component in microelectronics and power electronics systems [30, 31]. Fig. 1-5 shows the failure distribution in power electronic systems based on two surveys. It can be seen from the results that the power devices and the capacitor are the most fragile components in power electronic systems.

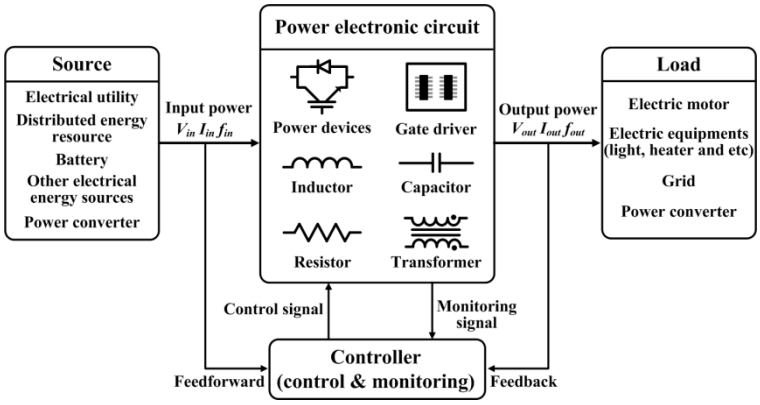

Fig. 1-4 General structure of power electronic systems connected to a source and load [29].

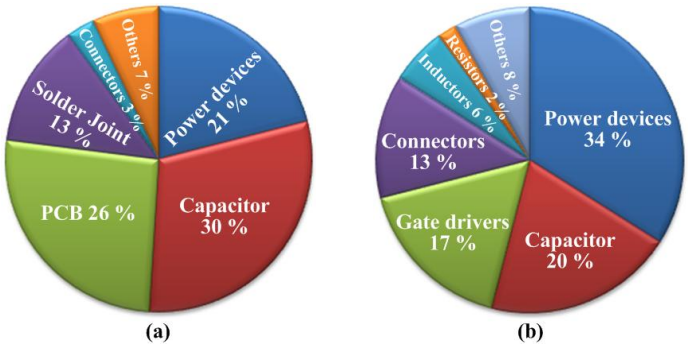

Fig. 1-5 Failure distribution in power electronic systems (a) survey is more on microelectronics products [30] (b) survey is more on power electronic products [31].

Each component in power electronic systems has the different critical stressors to affect the reliability. Table 1-1 shows the critical stressor for different components in power electronic systems [7]. It can be seen that the temperature swing, steady state temperature, humidity, voltage and vibration are the main stressors in the power electronics system and stressors have different levels of effect on each component in the power electronics system. Therefore, it could be helpful to focus on the critical stressor according to components when the various reliability researches are performed and the challenges are seen [32].

Table 1-1 Critical stressor of different components in power electronic systems [7]

Load			Elements									
Climate + Design => Stressor			Active power components			Passive power components		Control circuitry, IC, PCB, connector and etc				
Ambient	Product design	Stressor	Die	LASJ	Wire-bond	Cap.	Ind.	Solder Joint	MLCC	IC	PCB	Connectors
Relative humidity *-RH(t)* Temperature *-T(t)*	-thermal system -operation point -ON/OFF -power *P(t)*	Temperature swing $\triangle T$	●	●	●			●				
		Average Temperature *T*	◎	◎	◎	◐		◎	◎	○	○	○
		dT/dt	○	○	○	○						
		Water								●	●	○
		Relative Humidity	○	○	○	◎	○	○	○	◐	◐	○
Pollution	Tightness	Pollution						○			○	
Mains	Circuit	Voltage	○	○	○	◐	◎		○	○	○	○
Cosmic	Circuit	Voltage	○									
Mounting	Mechanical	Shock / vibration	○			○	○	○	○			○

LASJ – Large Area Solder Joint, MLCC – Multi Layer Ceramic Capacitor, IC – Integrated Circuit, PCB – Printed Circuit Board, Cap. – Capacitor, Ind. – Inductor, Level of effect (from high to low): ●-◐-◎-○

1.2. INSULATED GATE BIPOLAR TRANSISTOR (IGBT) MODULE

1.2.1. STRUCTURE OF IGBT MODULE

There are various kinds of power devices used in power electronic systems and different types of power devices are used according to the specification of the system like power range, blocking voltage switching frequency, and cost. Among the power devices, the IGBT is the one of the most used power device in various applications in the power range of from several hundred W to several MW due to their advantages like good power handling capabilities, high speed switching capability, relatively simple voltage controlled gate driver, short-circuit robustness and etc [33, 34].

In many practical applications, the power devices are used in a form of package, also called module, in order to [34]

- provide electrical connection between one or more semiconductor chips and the circuit.

- reduce costs for high power applications by connecting several chips with internal insulation of individual components.

- dissipate the heat generated during chip operation to a cooling system with electrical insulation.

- protect the semiconductor chip from harmful ambient influences.

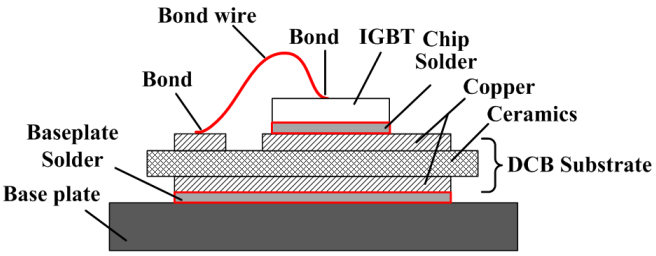

Fig. 1-6 Structure of standard Insulated Gate Bipolar Transistor (IGBT) module (weak connections that are relevant to reliability are marked red) [34].

Fig. 1-6 shows the structure of standard IGBT module [34]. A Direct Copper Bonded (DCB) substrate is soldered to a base-plate. The DCB provides electrical insulation between power components and cooling systems. Further, it conducts the current via copper track and provides also good thermal connection to cooling systems. In the lower power range, IGBT modules without the base-plate are more frequently used, while in medium and high power range, IGBT modules almost all have a base-plate. The base-plate provides thermal capacity and helps for the thermal spreading by increasing the contact area to a heat-sink. IGBT and diode chips are soldered to DCB. Bond wires are commonly used in order to connect the emitter of the silicon chips to a substrate and in order to connect the substrate to terminals. Finally, it is covered by silicone gel for insulation. Depending on packaging types, other materials like epoxy resin are also used.

1.2.2. SELECTED FAILURE MECHANISMS IN IGBT MODULES

Bond wire fatigue

Bond wire fatigue is one of the common failure mechanisms in power IGBT modules. As shown in Fig. 1-6, IGBT module consists of various materials and each material has the different Coefficient of Thermal Expansion (CTE) as listed in Table 1-2 [35]. The IGBT and diode produce the loss during switching and when conducting the electric currents and it appears as a heat source in the module. The converter load variation, the periodical commutation of power switching device and the ambient temperature change cause the temperature variation in the IGBT module. The large CTE mismatch between bond wires (Al) and chip (Si) under the temperature variation causes the thermo-mechanical stress in bond wires and it leads to the bond wire lift-off or crack failure [9, 33-38]. These failures occur at lots of electrical interconnection between chips and output pin of the IGBT.

To prevent bond wire related failures several strategies have been proposed such as bond wire geometry optimization [39, 40], replacement of Al bond wire to Cu bond wire for lower CTE mismatch [41, 42], Direct-Lead-Bonding (DLB) [43], and advanced packaging, where the bond wires are replaced with flexible circuit board [44].

Metallization reconstruction

To obtain direct electrical connection between semiconductor chips and substrate or output pin of module, a metallization layer is added to semiconductor chips [45]. Under the temperature variation, compressive and tensile stresses are introduced in the thin metallization layer due to the CTE mismatch between aluminum and silicon chip and the stresses can be far beyond the elastic limit. Under these conditions, the stress relaxation can occur by diffusion creep, grain boundary sliding or plastic deformation through dislocation glide depending on temperature and stress conditions [35, 36]. Depending on the texture of the metallization, it leads to either extrusion of the aluminum grain or voids formation at grain boundary. The reconstruction of aluminum metallization leads to an increase of the metal sheet resistance due to rough metallization surface, weakness of the connection between metallization layer and bond wire and non-uniform current distribution [46, 47].

To improve the emitter interconnection, a special emitter contact design called reinforced modules has been proposed [48]. The emitter contact includes a metal plate, which is Ag-sintered to the metallization and wire bonded on the top surface. Reinforced modules have comparably low current densities on the emitter contact of the IGBTs as well as lower von Mises stress at the bond interface, which makes them immune against bond wire lift-off and aging of the front metallization.

Table 1-2 Coefficient of Thermal Expansion (CTE) of different materials in IGBT module.

Material	**CTE ($10^{-6}K^{-1}$)**
$A1_2O_3$	6.8
AlN	4.7
Si_3N_4	2.7
BeO	9
Al	23.5
Cu	17.5
Mo	5.1
Si	2.6
AlSiC	7.5

Solder fatigue

Another dominant failure mechanism is solder fatigue. There are two solder joints in standard IGBT module between chip and DCB and between DCB and base-plate. Due to the CTE mismatch with temperature variation, the thermo-mechanical stresses are applied to the solder joints and cause the degradation of the solder interface like cracks, delamination and voids [36, 49, 50]. The solder joint fatigue increases the thermal impedance. Consequently, the junction temperature of power semiconductor devices may increase and it could accelerate other failure modes like bond wire fatigue [36, 51, 52]. Furthermore, the increased junction temperature could induce hot spots and thermal runaway in the affected areas of the module [53].

To improve the reliability of IGBT module, solder free packaging designs have been proposed [54-56]. The solder interface between chip and substrate and between substrate and base-plate are replaced by silver (Ag) sintering technology [55-57] or the soldered base-plate can be eliminated by pressure contact technology [54]. The advantages of Ag sinter layer compared with solder are that the thermal conductivity is more than a factor of three better than that of a tin–silver solder interface. This improves the transfer of heat together with the reduced layer thickness. The electrical conductivity is also enhanced. The mechanical characteristics such as CTE and tensile strength are favorable for the implementation in power electronic packages. Furthermore, it has higher meting temperature and thus has lower homologous temperature than solders at the same operating temperature [54]. Consequently, it has lower mechanical stresses.

Gate oxide failure

Gate oxide breakage of IGBT is caused by either an initial defect or deterioration of the oxide film. The former breakage is considered as an early failure, and the latter breakage is regarded as a long-term reliability failure [58]. If a high electric field which exceeds dielectric breakdown withstand voltage is applied, the oxide film

maybe broken. However, even if relatively low electric field is applied, continuous application of such a low electric field for a long time may also cause breakage as time elapses. This type of failure is referred to as a Time Dependent Dielectric Breakdown (TDDB) [58].

The electron is injected to the gate oxide by tunneling and it slowly degrades the quality of the oxide and over time, leads to failure of the oxide [59]. Once a dielectric breaks down, the current is able to flow more easily through the gate into source of an N-MOSFET completely destroying functionality. The evidence of TDDB is changes in the drain current as well as a large increase in the leakage current [60].

Another failure mechanism is the hot carrier injection. Hot carriers refer to either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor device [61]. Hot carrier is injected to the gate oxide because it has high kinetic energy to overcome the surface energy barrier. Hot carrier effects are mainly due to that the device dimensions are reduced without reduction of the operating voltage, resulting in high electric fields in the device [61]. Hot carrier injection usually results in higher circuit current densities. If hot carriers are injected into a gate oxide film, the gate oxide film is charged, or the $Si\text{-}SiO_2$ interface is damaged [58]. As a result, the transistor characteristic such as threshold voltage, leakage current and trans-conductance are changed [62].

The hot carrier injection is related to the channel lateral electric field and the TDDB in a thin gate dielectric is strongly dependent on vertical electric field. However, there seems to be similar electron and hole behaviors. Consequently, long-term hot carrier injection causes device breakdown which means that this effect might be related to the TDDB mechanism [63].

Burnout failure

Burnout failure may occur in the IGBT module as the final act of the wear-out. Furthermore, it is very closely associated with short-circuit condition under the operations in real applications where a high current is generated through the device while the device is handling a high voltage [36]. If the short-circuit condition is lasted for too long time, the IGBT chip is destroyed instantaneously. The repetitive tolerable short-circuit over long time interval may lead to thermal runaway conducting fast destruction of the devices [35, 64]. There are many causes of the short-circuit condition such as operations outside the safe operating area of the IGBT, malfunction of gate driver, inhomogeneous current sharing, dielectric breakdown and cosmic ray irradiation too [36, 65].

The selected failure mechanisms in the IGBT modules are summarized in Table 1-3.

Table 1-3 Selected failure mechanism in conventional IGBT module.

Failure mechanism	Failure site	Potential failure mode	Main failure cause	Parameter
Bond wire fatigue (lift-off, crack)	Bond wires (IGBT and diode)	Open circuit	ΔT, T	V_{CE_ON}, V_F
Metallization reconstruction	IGBT and diode	Open circuit	ΔT, T, J	V_{CE_ON}, V_F
Solder fatigue	Solder joints (between chip and DBC, DBC and base-plate)	Open circuit	ΔT, T	V_{CE_ON}, V_F, R_{th}
Gate oxide failure (TDBB, hot carrier injection)	IGBT oxide, oxide/substrate interface	Short circuit	T, V, E, J	V_{th}, I_D, I_{leak}
Burn-out failure	IGBT and diode	Short circuit	E, T, Overvoltage, Ionizing radiation	-

V_{CE_ON} : On-state collector emitter voltage of IGBT
V_F : Forward voltage of diode
R_{th} : Thermal impedance
V_{th} : Threshold voltage of IGBT
I_{leak} : Leakage current
I_D : Drain current
ΔT : Temperature swing
T : Temperature
E : Electric field
J : Curent density

1.2.3. POWER CYCLING (PC) TEST

As discussed above, the power devices are one of the most reliability-critical components in power electronic systems and the temperature swing and steady state temperature are the main causes of failure in power devices such as IGBT modules. Therefore, reliability researches about the effect of temperature stresses on power IGBT modules are one of the main concerns.

The accelerated power cycling test is an important method to investigate the reliability performance of power device modules regarding temperature stress [35, 56, 66-68]. By performing the power cycling test, failure mechanisms of the power device modules due to temperature stress can be studied [9, 49]. Further, new device packaging materials and designs can be evaluated [48, 55, 56, 69]. Finally, last but not least, a lifetime model can be developed based on the power cycling results [70-72] that will be used for lifetime estimation of power device modules under given mission profiles [12, 15, 73, 74].

Power cycling test has been performed under various temperature stress conditions with different temperature stress parameters such as ΔT_j and T_{jmean}. By investigating inside of tested modules with special equipment like Scanning Electron Microscope

(SEM), the effect of different temperature stress conditions on failure mechanisms and lifetime as well as the failure mechanism of the tested module can be studied.

Further, based on the number of cycles to failure results, the lifetime models in terms of the stress parameters are developed. The lifetime models play an important role in design for reliability. From the lifetime models, lifetime of power device modules in power converter can be estimated under given mission profiles. Further, the lifetime models can be used for converter design aspect to achieve lower development cost, manufacturing cost, operational and maintenance costs during the lifetime.

Most power cycling tests have been performed with simple designed test setup as shown in Fig. 1-7, where the load pulse with constant DC current source is applied to the device under test (DUT). The temperature of the tested module increases by the conduction loss. If the temperature is reached to the desired maximum temperature, the applied power is disconnected and the temperature is decreased by the external cooling system. This period (T_s) is defined as cycle and it is repeated until the tested module is failed. The duration and amplitude of the current pulse are changed in order to obtain the specific junction temperature swing ΔT_j (T_{jmax} - T_{jmin}) and mean junction temperature T_{jmean} [35, 56, 75, 76].

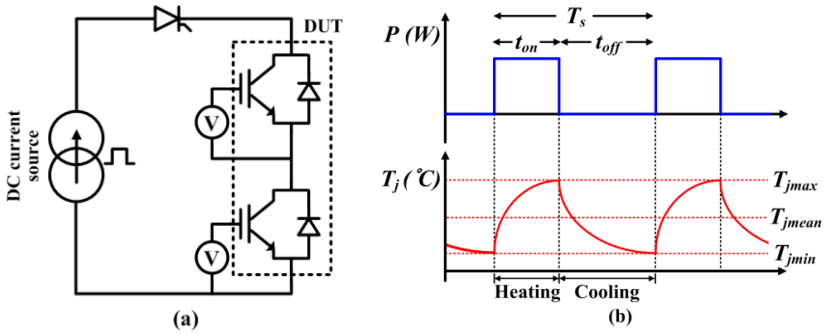

Fig. 1-7 Conventional DC power cycling test (a) configuration of DC power cycling test (b) temperature profile applied to Device Under Test (DUT).

However, in such test, the tested module is not operated under realistic electrical conditions. There are no switching, high DC-link voltage and etc. Further, an overload current may be required to apply high temperature swing in a short cycle period because the temperature is increased by only conduction loss. In addition, there is a lack of study on the effect of the operating conditions of the power modules on the failure mode and lifetime and thus this effect is still an open question [77-79].

In [9], the AC power cycling test has been performed. This circuit allows performing the power cycling test under more realistic converter operation compared with conventional DC test with small power losses. However, in this setup, some features such as on-line monitoring system are required for more advanced power cycling test. Further, there is lack of detailed information on control and configuration of test setup and test procedure. In other words, there is a still lack of study on AC power cycling test and test results in the prior-art test activities at the moment. Therefore, an advanced power cycling test setup and procedure are still needed in order to perform the power cycling test under the realistic operating condition in an efficient way and minimize the uncertainty which may be able to come from other parameters or test conditions and to affect test results.

1.2.4. IGBT MODULE FAILURE HANDLING METHODS IN POWER ELECTRONICS CONVERTER

Typically, failure mode in an IGBT module can be divided into two modes; short-circuit fault and open-circuit fault.

The short-circuit fault may occur because of abnormal operating conditions such as the wrong gate voltage, overvoltage, avalanche stress, temperature overshoot and etc. It is difficult to handle the short-circuit fault because it leads to the over-current which can cause serious damage to other components in power electronics converters. Therefore, most short-circuit fault detection and protection methods are based on hardware circuits. The de-saturation detection method, which measures the on-state collector-emitter voltage of IGBTs during turn-on state, is the common method to detect the short-circuit fault [85-87]. Further, electric fuses are also used to protect the power electronics circuit under the short-circuit current.

The open-circuit fault may occur due to the lifting of the bond-wire in power module. Gate drive fault may also be one of the common causes of the open-circuit fault. The open-circuit fault does not cause a serious damage, compared to the short-circuit fault, but reduces the system performance considerably. It leads to the distortion of the output phase currents, increase of the currents in the other normal phases and unbalance of the neutral-point voltage in the case of neutral-point clamped inverters. Further, it may cause secondary problems in other components or loads like transformer and motors by applying the distorted currents. If the open-circuit fault occurs, fault-tolerant control needs to be applied to maintain the converter system performance. The fault detection is performed before the fault-tolerant control, because the fault-tolerant strategies are typically different according to the specific faulty switch. In addition, identifying the faulty switch can give the advantage to know where the converter needs to be repaired.

The most of the open-circuit fault detection methods are based on characteristics of output currents [87-90]. These methods are cost-effective because they do not need any additional hardware but there are limitations in detection speed and accuracy under the small output current. On the other hand, the open-circuit detection methods based on the output voltage measurements [87, 91, 92] have advantages in terms of detection speed and accuracy but they need additional hardware to measure the output voltage. Therefore, they are not cost-effective.

After the faulty switch is detected, the fault-tolerant methods are applied in order to keep the operation of power electronics converter system for high availability. Generally, fault-tolerant methods are based on the topology modifications and thus require additional components in the form of silicon switches and/or fuses to provide continuous operation and minimize the effects of the fault [93-96]. Depending on the systems, there are also fault-tolerant methods based on the control strategies [97, 98].

It is worth to point out that there are no generalized fault-detection and fault-tolerant methods for various converters because they have different characteristic under the fault conditions. Therefore, specialized fault detection and fault-tolerant methods are needed for the different converters and applications.

1.3. THESIS OBJECTIVES

1.3.1. REASEARCH QUESTIONS AND OBJECTIVES

As power electronics have progressively gained an important status in a wide range of industrial fields, the reliability and robustness of power electronics are becoming one of the important topics. To improve the reliability of the power electronic system, more multidisciplinary reliability research which is defined as shown in Fig. 1-8 especially about the reliability-critical components is needed. Taking into account three respective aspects of reliability in power electronics, following research questions are raised:

1. How can the reliability test be performed under more realistic operating conditions in order better to analyze and understand the root cause of failure and failure mechanism?

2. How to develop the lifetime model under more realistic condition of real applications for an accurate lifetime prediction for an IGBT module?

3. How to improve the reliability and availability of a complete power electronic converter under the failure condition?

Based on the above research questions, various reliability studies on power IGBT module are performed as shown also in Fig. 1-8.

The main objectives of this project are

1. Development of apparatus and methodologies for an advanced accelerated power cycling test of power IGBT modules.

2. Development of a lifetime model of the IGBT module regarding thermal stresses under realistic electrical condition based on the advanced power cycling test.

3. Development of open-circuit fault detection and fault-tolerant control methods to improve the reliability and availability of the power converters.

In this thesis, a 600 V, 30 A transfer molded Intelligent Power IGBT Module (IPM) is used as target component for the first two objectives and two types of neutral-point clamped IGBT-based three-level inverters (NPC and T-type) are considered for the last objective.

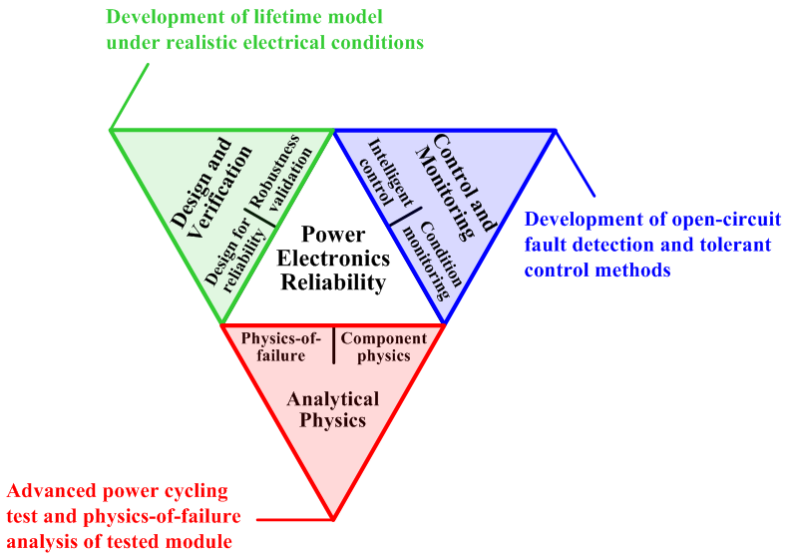

Fig. 1-8 The objectives of this project corresponding to the scope of power electronics reliability defined by CORPE in 2010 [7].

1.3.2. PROJECT LIMITATIONS AND ASSUMPTIONS

In this project, the power cycling tests were performed under limited temperature range and temperature cycle period, which are relatively higher temperature stress and shorter period because the lower temperature range, which is more similar with real conditions and longer cycle period, requires a long test time. This is the fundamental limitation in power cycling test as well as the limitation in this project.

Further, the accelerated power cycling tests were carried out with restricted number of samples and test conditions to make the lifetime model due to the limitations in the test time and cost. More test results obtained in the future might change the parameter values. Therefore, the model and the parameter fit should be considered as preliminary.

The open-circuit fault conditions for the verification of fault detection and fault-tolerant control methods were made by eliminating the gate signal of the IGBT because it is difficult to make the real open-circuit fault condition of the IGBT module.

1.4. OUTLINE OF THE THESIS

The PhD dissertation consists of six chapters and is organized as follows:

Chapter 1: Introduction

The background and motivation for the research project are presented. Based on the research questions, the objective of the project are described as well. Finally, the outline of each chapter is also given.

Chapter 2: Advanced Accelerated Power Cycling Test for Reliability Investigation of Power Device Modules

An apparatus and methodology for an advanced accelerated power cycling test are presented. A detailed explanation of apparatus such as configuration and control methods for the different functions of accelerated power cycling test setup is given. Then, an improved in-situ junction temperature estimation method using on-state collector-emitter voltage V_{CE_ON} and load current is proposed. Finally, a procedure of the advanced accelerated power cycling test and experimental results are presented in order to verify the validity and effectiveness of the proposed test setup and methodology.

Chapter 3: Lifetime Modeling of Power IGBT Module

A lifetime model of transfer molded Intelligent IGBT Power Module is developed based on the advanced power cycling test results. In the beginning of this chapter, the Weibull analysis, which is commonly used in lifetime data analysis, is presented. Then, the effect of junction temperature swing duration $t_{\Delta Tj}$ on lifetime of IGBT module is investigated. The detailed lifetime analysis under different lifetime definitions and confidence levels are provided and relevant lifetime factor is modeled based on the total 38 test results under the six different conditions. Finally, physics-of-failure analysis results of the tested modules are presented.

Chapter 4: Open-Circuit Fault Detection and Fault-Tolerant Control Methods for a T-type Three-Level Inverter

This chapter deals with an open-circuit fault detection and tolerant-control methods for the T-type inverter to improve their reliability and availability under open-circuit fault conditions. Firstly, the basic configuration and description of neutral-point clamped three-level inverters are discussed. In addition, the operation of T-type inverter under the open-circuit fault is presented. Then, the open-circuit fault-detection method for the T-type inverter is presented. Finally, fault-tolerant control methods are introduced, where two fault-tolerant control methods are proposed in the case of fault in the neutral-point switch.

Chapter 5: Open-circuit Fault Detection and Fault-Tolerant Control Methods for a Grid-Connected NPC Inverter

This chapter proposes open-circuit fault detection and fault-tolerant control methods for the grid-connected NPC inverter. The analysis of the grid-connected NPC inverter operation under open-circuit fault conditions is presented. Based on the analysis, a novel open-circuit fault detection method including fault in the clamping diode is proposed. Finally, a fault-tolerant control strategy under open-circuit fault in the clamping diode is proposed.

Chapter 6: Conclusions and Future Work

This chapter presents the summary, main findings and conclusion of this thesis. Topics for future research are also discussed.

In the end of the thesis, the published papers during the PhD study period are attached.

1.5. LIST OF PUBLICATIONS

A list of the papers, which are published or have been submitted during the PhD study, is given as follows:

Papers related to thesis

A. Journal paper

[J.1] **U. M. Choi**, S. Jørgensen and F. Blaabjerg, "Advanced Accelerated Power Cycling Test for Reliability Investigation of Power Device Modules,**"** *IEEE Transactions on Power Electronics*, to be published.

[J.2] **U. M. Choi**, F. Blaabjerg, F. Iannuzzo and S. Jørgensen, "Junction temperature estimation method for a 600 V, 30A IGBT module during converter operation," *Microelectronics reliability*, vol. 55, no. 9-10, pp. 2022-2026, Aug.-Sep. 2015. (also *in Proc. of EEREF 2015*).

[J.3] **U. M. Choi**, K. B. Lee and F. Blaabjerg, "Diagnosis and Tolerant Strategy of an Open-Switch Fault for T-Type Three-Level Inverter Systems," *IEEE Transactions on Industry Application*, vol. 50, no. 1, pp. 495-508, Jan.-Feb. 2014.

[J.4] **U. M. Choi**, F. Blaabjerg and K. B. Lee, "Reliability Improvement of a T-Type Three-Level Inverter With Fault-Tolerant Control Strategy," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2660-2673, May 2015.

[J.5] **U. M. Choi**, J. S. Lee, F. Blaabjerg and K. B. Lee, "Open-Circuit Fault Diagnosis and Fault-Tolerant Control for a Grid-Connected NPC Inverter," *IEEE Transactions on Power Electronics*, in press.

[J.6] **U. M. Choi**, F. Blaabjerg and K. B. Lee, "Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2517-2533, May 2015.

B. Conference

[C.1] **U. M. Choi**, I. Trintis, F. Blaabjerg, S. Jørgensen, and M. L. Svarre, "Advanced Power Cycling Test for Power Module with On-line On-state V_{CE} Measurement," *in Proc. of APEC 2015*, pp. 2919-2924, Mar. 2015.

[C.2] **U. M. Choi**, F. Blaabjerg, J. S. Lee, and K. B. Lee, "Open-circuit fault diagnosis for a grid-connected NPC inverter with unity Power Factor," *in Proc. of APEC 2015*, pp. 213-220, Mar. 2015.

[C.3] **U. M. Choi**, F. Blaabjerg, and S. Jørgensen, "Junction temperature estimation for an advanced active power cycling test," *in Proc. of ICPE-ECCE Asia 2015*, pp. 2994-2950, Jun. 2015.

[C.4] **U. M. Choi** and F. Blaabjerg, "Effect of Junction Temperature Swing Duration on Lifetime of Transfer Molded Intelligent Power IGBT Module," submitted to *ECCE 2016*.

Other Papers

[O.1] **U. M. Choi**, F. Blaabjerg and K. B. Lee, "Method to Minimize the Low-Frequency Neutral-Point Voltage Oscillations With Time-Offset Injection for Neutral-Point-Clamped Inverters," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1678-1691, Mar.-Apr. 2015. (also *in Proc. of ECCE 2013*)

[O.2] **U. M. Choi**, F. Blaabjerg and K. B. Lee, "Control Strategy of Two Capacitor Voltages for Separate MPPTs in Photovoltaic Systems Using Neutral-Point-Clamped Inverters," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3295-3303, Jul.-Aug. 2015 (also *in Proc. of APEC 2014*).

[O.3] J. S. Lee, **U. M. Choi**, and K. B. Lee, "Comparison of Tolerance Controls for Open-Switch Fault in a Grid-Connected T-Type Rectifier," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5810-5820, Oct. 2015.

CHAPTER 2. ADVANCED ACCELERATED POWER CYCLING TEST FOR RELIABILITY INVESTIGATION OF POWER DEVICE MODULES

This chapter presents an apparatus and methodology for an advanced accelerated power cycling test for IGBT modules. A detailed explanation of apparatus such as configuration and control methods for different functions of the advanced accelerated power cycling test setup is given. Then, an improved in-situ junction temperature estimation method using on-state collector-emitter voltage V_{CE_ON} and load current is proposed. Finally, a procedure of the advanced accelerated power cycling test and experimental results are presented.

2.1. ADVANCED ACCELERATED POWER CYCLING TEST SETUP

The most of the power cycling tests has been performed with the conventional DC power cycling test as mentioned in Chapter 1.2.3. However, in such test, the tested module is not operated under realistic electrical conditions. Further, an overload current may be required to apply high temperature swing in a short period because the temperature is increased by only conduction losses. There is a lack of study on the effect of the operating conditions of the power modules on the test results and thus this effect is still an open question [77-79]. Several accelerated reliability tests have been performed at product level with a real load such as motor [79-81]. However, power cycling tests with real loads are not cost-effective because the real load generates the large power losses during test. Further, it requires long test period. In the case of power cycling test with small load inductor, there are limitations to emulate the various operating conditions such as power factor, modulation index and etc.

Therefore, the power cycling test under more realistic operating condition in a cost-effective way is needed in order to minimize the uncertainty which may be able to come from other parameters or test conditions and to affect test results.

2.1.1. CONFIGURATION OF ACCELERATED POWER CYCLING TEST SETUP

Fig. 2-1 shows a configuration of an advanced accelerated power cycling test setup. Two three-phase converters are connected through load inductors. One is a test converter and the other one is a load converter. An IGBT module that will be tested is used for the test converter. In the load converter, an IGBT module which has a higher rated power than the tested module is used in order to reduce the effect of the thermal stresses on the load IGBT module during accelerated power cycling tests. By using a higher rated power module for the load converter, the load converter can run for a long time even though the tested IGBT modules are changed after a certain number of power cycling tests.

These two converters are connected with a DC source (V_{DC}) via an electric fuse (see Fig. 2-1). If there is an abnormal high current during the power cycling test, the electric fuse disconnects the two converters from the DC source in order to protect the overall system. The detailed information for the electric fuse can be obtained in [99].

The on-state collector-emitter voltages (V_{CE_ON}) of IGBTs and forward voltages (V_F) of the diodes are measured in real time by an on-line V_{CE_ON} measurement circuit to monitor the wear-out condition of the IGBT module under test [19]. V_{CE_ON} is a good indicator to determine the wear-out of the power device module regarding bond-wire lift-off, delamination of solder joints and chip metallization degradation [82]. Further, the junction temperature of the power devices can also be estimated by V_{CE_ON} because it is one of Temperature Sensitive Electrical Parameters (TSEPs) in the IGBT [83, 84].

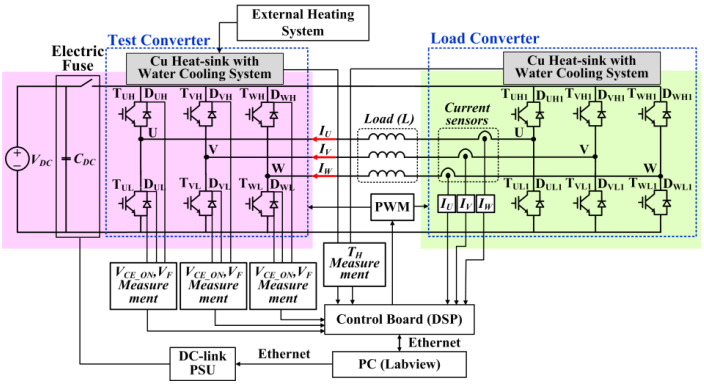

Fig. 2-1 Configuration of power cycling test setup.

The two converters are controlled by a control board with a Digital Signal Processor (DSP) and Labview interface communicates with the DSP to manage and monitor the overall system. A water cooling system and external temperature controllable heating system are used to change the heat-sink temperature according to the desired test condition and to keep the heat-sink temperature of the test module as a constant during the power cycling test.

Fig. 2-2 shows a prototype of the advanced accelerated power cycling test setup. A power circuit board consists of three parts; Test Converter board, Load Converter board and V_{CE_ON} Measurement circuit. In this system, A 600 V, 30A, 3-phase transfer molded Intelligent Power IGBT Module is used for the test converter and a 1200 V, 75A, 3-phase IGBT module is used for the load converter. The IGBT module for test is replaced with a new one after the power cycling test and the test converter board is also changed sometimes to a new one if the board is worn out. Therefore, the power circuit board has been designed by applying the plug-and-play concept. The boards can be separated from each other easily and components, which are put on the Test Converter board, are minimized to avoid unnecessary replacement of components.

In this topology, there are only power losses by the tested and load IGBT modules, which are switching and conduction losses and losses from the load inductors, because the current is circulated between the two converters. Further, only a small value of inductors is needed for the loads in order to get an acceptable current ripple. Therefore, although, the rated output currents are generated, the power losses by the test setup can be kept low.

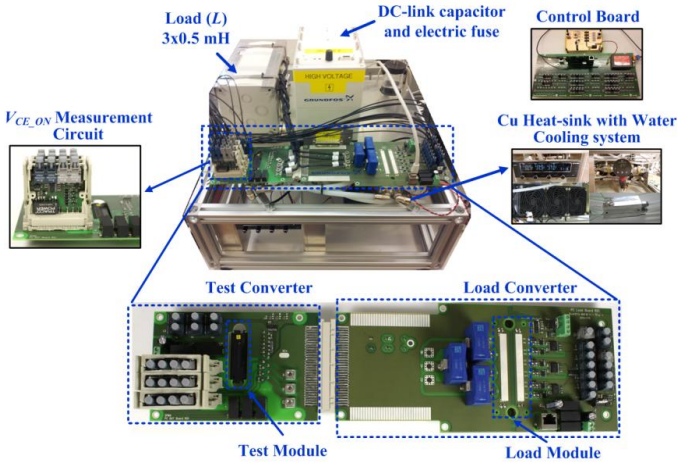

Fig. 2-2 Prototype of the advanced accelerated power cycling test setup.

2.1.2. OPERATING PRINCIPLE OF POWER CYCLING TEST SETUP

Output of each test converter leg and output of corresponding load converter leg are connected through each load inductor and the load inductors are not connected to each other as shown in Fig. 2-1. Therefore, this system is controlled like three single-phase half bridge converters. For example phase-U, the test converter generates the output voltage ($V_{U\_ref\_test}$) that fulfills required test conditions like magnitude, output frequency with a determined switching frequency and the load converter produces the output voltage in order to generate the current with desired magnitude, frequency and power factor.

The output phase current of the converter (I_U) is considered as the current in the d-axis in the stationary frame when it is controlled. The q-axis current in the stationary frame can be made by shifting the d-axis current in the stationary frame by 90 ˚ using an all-pass filter as shown in Fig. 2-3. The d- and q-axis currents in the stationary frame are converted to the currents in the synchronous frame with a phase angle. The real power is aligned to the d-axis and the imaginary power is aligned to the q-axis in the synchronous frame. Then, they become the input to Proportional-Integral (PI) current controllers, separately. The output of each current controller becomes the reference output voltages (V_{de_ref} and V_{qe_ref}) in the synchronous frame. By inverse transformation, the output reference voltages V_{de_ref} and V_{qe_ref} are converted to voltages in the stationary frame (V_{ds_ref} and V_{qs_ref}), where the d-axis reference voltage V_{ds_ref} becomes the reference voltage of the load converter ($V_{U\_ref\_load}$).

The output current is generated by the difference of the output voltages between the test and load converters, which is applied to the inductor as shown in Fig. 2-4. It means that the voltage is applied across the inductor during a short period. Therefore, small inductors are enough as loads of the converter in this test setup in order to obtain an acceptable low current ripple. In this specific system, 0.5 mH inductors are used. The power factor of output currents can be varied by changing the magnitude and polarity of the d-axis and q-axis currents. By changing the power factor, the focused device for the power cycling test can be chosen. For example, under PF=1 which is inverting mode, the losses in the IGBTs are dominant and thus they have the larger thermal stresses than diodes. On the contrast, under PF=-1, the diodes have the larger thermal stresses than IGBTs like converter and rectifier.

The controls for the other phases are the same as explained above but there are only 120 ˚ and 240 ˚ shifting in phase angle respectively to simulate a 3-phase converter system. The parameters like output frequency, modulation index, magnitude of the output current and voltage, power factor, switching frequency can be set to apply various thermal stresses on the test module and emulate the various operating conditions of the test converter. Fig. 2-5 shows the outputs of test setup under different operating conditions.

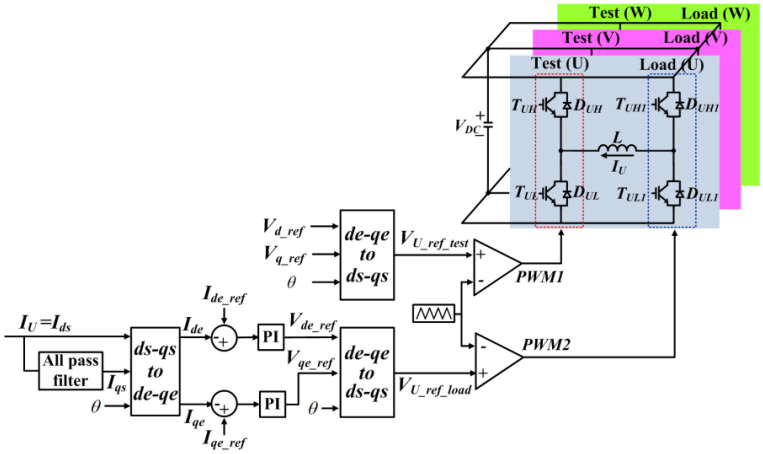

Fig. 2-3 Control block diagram of the advanced power cycling test setup.

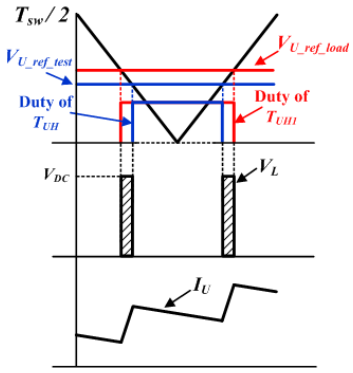

Fig. 2-4 Reference voltages for load and test converters and corresponded inductor voltage and output current.

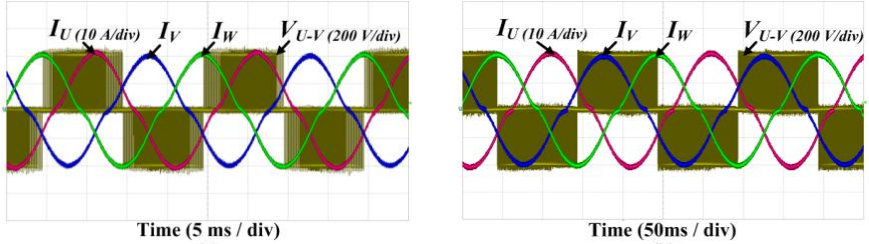

Fig. 2-5 Outputs under various operating conditions when I_{ref} = 20 A, V_{DC} = 400 V (a) f_{OUT} = 50 Hz, PF =1, (b) f_{OUT} = 5 Hz, PF = -1.

2.1.3. ON-LINE V_{CE_ON} AND V_F MEASUREMENTS

The on-state collector-emitter voltage (V_{CE_ON}) of IGBTs and forward voltage (V_F) of diodes are good indicators for determining the wear-out condition of power device modules regarding bond-wire degradation, delamination of the solder joints and chip metallization degradation. By measuring V_{CE_ON} and V_F, the degradation level of the tested module can be monitored during the accelerated power cycling test. Usually, 5% to 20 % increase of V_{CE_ON} and V_F from its initial values is considered as a wear-out failure of the power device modules [35]. Further, the junction temperature of the test module can be estimated.

Diode method

Fig. 2-6 shows the schematic of the V_{CE_ON} and V_F measurements circuit using diode which is described in [19].

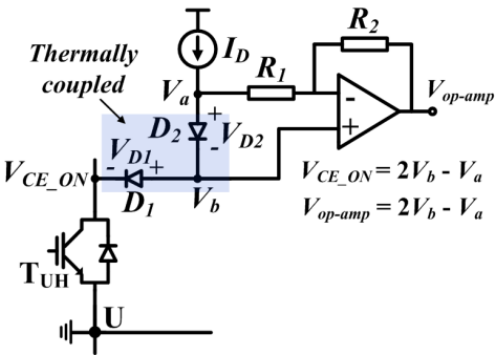

Fig. 2-6 Schematic of the on-line V_{CE_ON} and V_F measurement circuit using diode [19].

Two diodes D_1 and D_2 are connected in series and these diodes are forward-biased by the current source (I_D) when the transistor (T_{UH}) is turned on. If T_{UH} is turned off, D_1 blocks the high V_{CE} voltage, which comes from DC-link to protect the measurement circuitry. Assuming diodes D_1 and D_2 have the same characteristics, the forward voltage of D_1 and D_2 can be represented as given in (2.1)

$$V_{D1} = V_{D2} = V_a - V_b \tag{2.1}$$

For example T_{UH}, V_{CE_ON} can be expressed by the difference between the voltage potential V_b and V_{D1} as given below

$$V_{CE\_ON} = V_b - V_{D1} = V_b - (V_a - V_b) = 2V_b - V_a \tag{2.2}$$

The above result can be realized by choosing properly the gain of the amplifier. If $R_1 = R_2$, the output of the amplifier can be expressed as

$$V_{op\text{-}amp} = V_b - ((V_a - V_b) \cdot R_2 / R_1) = 2V_b - V_a = V_{CE\_ON} \quad (2.3)$$

The output of the amplifier is the same with V_{CE_ON} as described above.

MOSFET method

Fig. 2-7 shows V_{CE_ON} and V_F measurement circuit using MOSFET. The MOSFET used in this circuit is a depletion mode MOSFET. Therefore, it is turned on when the gate-source voltage V_{GS} = 0 V. Further, in this circuit, the magnitude of clamping voltage ($\pm V_{CC}$) should be bigger than on-state collector emitter voltage (V_{CE_ON}) and forward voltage (V_F).

When the IGBT (T_{UH}) is tuned-on, the current I_D does not flow through the MOSFET because V_{CE_ON} is smaller than V_{CC} and thus V_{GS} = 0. Consequently, the MOSFET is turned-on and V_{CE_ON} can be measured. As V_{CE} is increased above the clamping voltage V_{CC} by turning off T_{UH}, I_D starts to flow and makes the voltage drop in R_1. As I_D increases, V_{GS} becomes smaller than threshold voltage (V_T) of the MOSFET where V_T is negative voltage. Therefore, the MOSFET is turned off and the clamping voltage V_{CC} is measured during this period. The measurement of V_F also can be interpreted in a similar way.

V_{CE_ON} of the IGBT can be measured during the negative current and V_F of the diode can be measured during positive current where the current from the load converter to the test converter is positive.

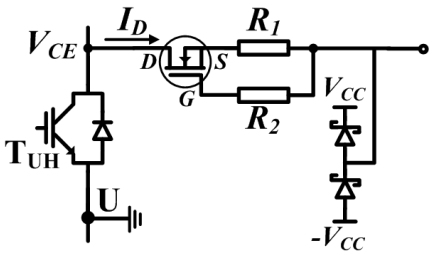

Fig. 2-7 Schematic of the on-line V_{CE_ON} and V_F measurement circuit using depletion mode MOSFET.

Fig. 2-8 shows a prototype of the V_{CE_ON} measurement circuit using MOSFET method which is used for this project. To improve the resolution of the measured data, an external 14 bit Analog to Digital Converter is used for this circuit. It is designed compactly and it can easily be separated from the power cycling test board.

Fig. 2-9 shows the measured V_{CE_ON} and V_F of the IGBTs and diodes of the phase-V according to the current under the inverter operation.

Fig. 2-8 Prototype of on-line V_{CE_ON} and V_F measurement circuit using MOSFET for the power cycling test.

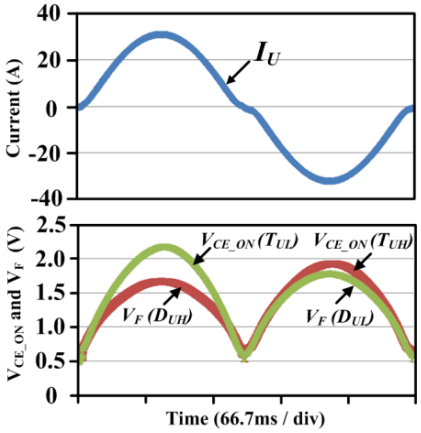

Fig. 2-9 V_{CE_ON} and V_F measurement of phase-V under the inverter operation when I_{peak} : 30 A, f_{SW}: 10 kHz, f_{OUT} : 3 Hz.

2.2. JUNCTION TEMPERATURE ESTIMATION

It is important to know the applied temperature stresses like junction temperature swing (ΔT_j), mean junction temperature (T_{jmean}) and temperature cycle period ($t_{\Delta Tj}$) when the power cycling test is performed. They are important factors when lifetime models of power device modules are developed. Further, they are also needed when the tested modules are investigated physically to study the failure mode and the effect of the different thermal stresses on the power device modules degradation.

A simple and correct method is to use an Infra-Red (IR) camera. In this test, the IR camera (FLIR X8400sc) is used to measure directly the applied temperature stresses and validate the proposed method. Using open IGBT module, covered by black paint, the junction temperature is measured under certain operating conditions. Then, the same operating conditions like output current, voltage, frequency, power factor and etc are applied to the tested power modules, which are the normal modules. However, even though the applied thermal stresses for power cycling test are known by the IR camera, it is also important to know the junction temperature variation as the tested module is worn-out in order to investigate the degradation effect of the power device modules. Furthermore, the junction temperature is the prime parameter to be concerned for the reliability analysis, when the converters are designed and operated. Therefore, the estimated junction temperature is an important parameter for monitoring. In this section, improved junction temperature estimation method using V_{CE_ON} and the load current is described.

2.2.1. PRELIMINARY I-V CHARATERIZATION

A preliminary calibration is necessary to estimate the junction temperature from V_{CE_ON} and V_F. The purpose is to obtain the dependence of temperature on the V_{CE_ON} and V_F for the IGBTs and diodes, under a given current level. Of course, data for the calibration can be obtained from the manufacturer's data sheet, but it is not accurate enough. Test equipment such as V/I curve tracer can be used to get more precise and various data. However, such equipment is considerably expensive. Further, the differences between the curve tracer and the V_{CE_ON} measurement circuit and between the current sensor of the curve tracer and the current sensor of the converter cannot be ignored. If there are some offset errors between them, it causes an error when the junction temperature is estimated using the measured V_{CE_ON} and current. However, if both I-V characterization and the measurement during operation are performed by the same V_{CE_ON} measurement circuit and current sensor, the error which comes from the different measurement methods (V/I curve tracer and V_{CE_ON} measurement circuit) and different current sensors can be eliminated.

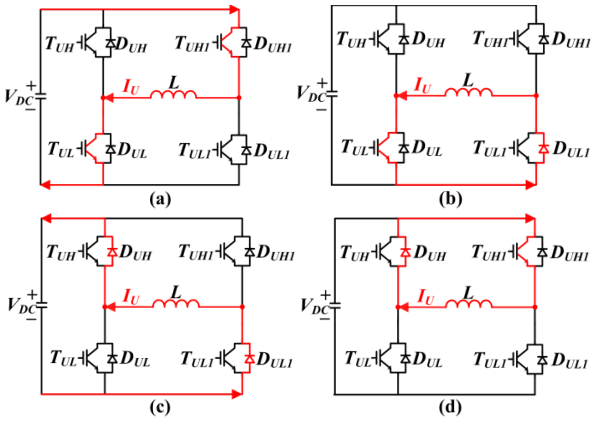

Fig. 2-10 Switching sequence for I-V characterization (a) switching for I_U increase (b) switching for freewheeling of I_U through T_{UL} (c) switching for I_U decrease (d) switching for freewheeling of I_U through D_{UH}.

In this section, an I-V characterization method of the power device module under test is presented. From the simple switching sequences with on-line V_{CE_ON} measurement, the I-V characterization curves for the junction temperature estimation can be obtained. The heat-sink temperature (T_H) is controlled by the external temperature controllable heating system. After a while, once the thermal steady-state condition is reached, the junction temperature becomes equal to T_H, and then T_{UL} and T_{UH1} are turned on as shown in Fig. 2-10 (a). The current level can be changed by varying the dwell time of turn-on state of T_{UL} and T_{UH1}. Then, T_{UH1} is turned off so that the current flows through T_{UL} and D_{UL1} as shown in Fig. 2-10 (b). V_{CE_ON} of T_{UL} and the current (I_U) are measured at this point. After V_{CE_ON} and I_U are measured, T_{UL} is turned off and I_U is reduced to zero as shown in Fig. 2-10 (c). In the case of measurement for D_{UH}, T_{UL} is turned off. I_U flows through D_{UH} and T_{UH1} as shown in Fig. 2-10 (d). The forward voltage V_F of D_{UH} and I_U are measured at this point and then T_{UH1} is turned off to make I_U zero. This switching sequence is performed by changing the current level from the minimum value to the rated value under the same temperature condition and then it is performed again at different temperature levels. Each switching sequence is performed in a short period (less than 3 switching periods). During this period, thermal impedance and the loss of the device are very small due to the short transient time. Therefore, the increase of the junction temperature during the switching sequence is negligible.

Fig. 2-11 shows the output current corresponding to the switching sequences for the I-V characterization.

Fig. 2-12 shows the I-V characterization curves for the low-side IGBT of the phase-V (T_{VL}) at different temperatures.

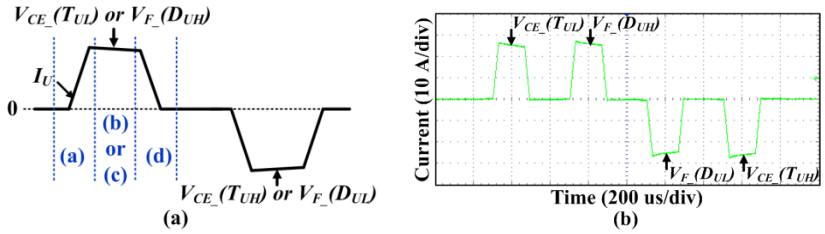

Fig. 2-11 Output current under switching sequence for I-V characterization (a) output current corresponding to the switching sequence (b) experimental result.

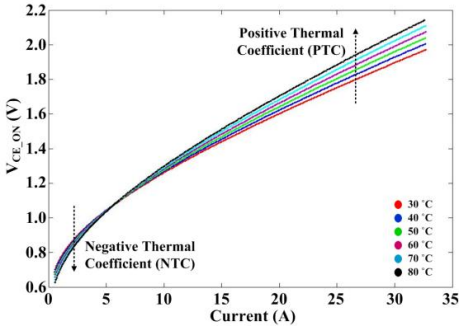

Fig. 2-12 I-V characteristic curves of low side IGBT of phase-V (T_{VL}) in IGBT power module at different temperatures.

2.2.2. T_J ESTIMATION FROM I-V CHARACTERIZATION CURVES

It is needed to derive V_{CE_ON} as a function of temperature at a given current level in order to estimate the junction temperature (T_j) from the obtained I-V characteristic curves in chapter 2.2.1. To derive the relation between V_{CE_ON} and T_j, V_{CE_ON} should be formularized as a function of current. This can be achieved by the polynomial fitting method. Then, T_j can be represented as the function of V_{CE_ON} at the given current as shown in Fig. 2-13. These relations can be represented by a Slope Factor (K) as shown in Fig. 2-14. From the above relations, T_j can be estimated from the measured current and V_{CE_ON} as follows

$$T_{j\_est} = K_{(I)} \cdot (V_{CE\_M} - V_{CE\_B(I)}) + T_B \tag{2.4}$$

where T_{j_est} is the estimated temperature, $K_{(I)}$ is the slope factor as a function of current, V_{CE_M} is the measured on-state V_{CE} in real time, $V_{CE\_B(I)}$ is the base V_{CE_ON} as a function of current, which can be chosen among the characterization curves. T_B is the base temperature corresponding to the base V_{CE_ON}.

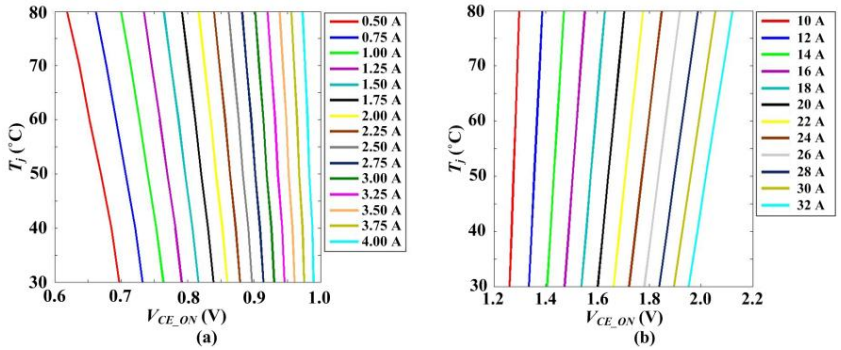

Fig. 2-13 Relation between V_{CE_ON} and T_j at different current levels (a) Negative Thermal Coefficient (NTC) region (b) Positive Thermal Coefficient (PTC) region.

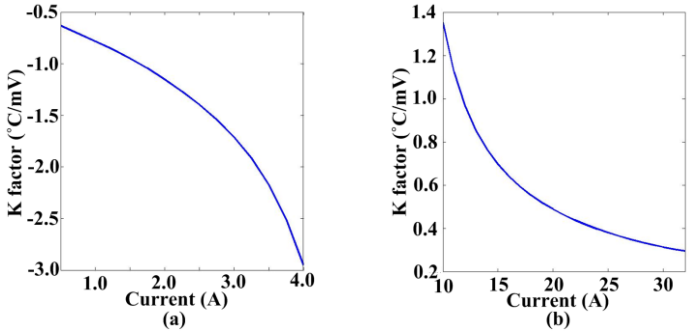

Fig. 2-14 Slope factors (K) as a function of current (a) in the NTC region (b) in the PTC region.

However, it is worth to note that packaged devices do not permit to solely measure V_{CE_ON}. In fact, each device is connected to output pins through a series of interconnections, like bond-wire and traces. Furthermore, in IPMs, control Integrated Circuits (ICs) with Printed Circuit Board (PCB) are embedded inside the module. Therefore, the measured V_{CE_ON} definitely includes the voltage drops on various interconnection elements as follows

$$V_{CE\_M} = V_{CE\_Chip} + R_{int} \cdot I_C \tag{2.5}$$

where V_{CE_Chip} is the real on-state collector-emitter voltage of the chip, R_{int} is the equivalent resistance of the interconnections elements and I_C is the collector current.

2.2.3. RESISTANCE VARIATION IN AN IGBT MODULE ACCORDING TO TEMPERATURE

To investigate the effect of temperature variation on the resistance in the IGBT module, the resistance of the interconnection materials in the IGBT module is measured using a four-point probing approach. An open module is used to contact the probe to the emitter and collector of the device.

Fig. 2-15 shows the four-point probing method to measure the interconnection resistance. The resistances from the negative DC-link input pin to emitter and collector to output pin of the low-side IGBT and from positive DC-link input pin to collector and emitter to output pin of the high side IGBT are measured by applying a DC current. Two different DC currents (1A and 5A) have been used to check the effect of self-heating during the measurement. Moreover, two IGBT modules have been used for measurements.

Fig. 2-16 (a) and (b) show the total parasitic package resistance values of the high- and low-sides IGBTs of two different modules. No big differences are observed in the resistances between the cases of 1 A and 5 A and between the two different modules.

From the results, it can be concluded that the self-heating effect by the applied DC current is negligible. Further, the Resistance Variation Factor (*RVF*) according to temperature can be obtained. Measurements of Fig. 2-15 yield 0.0359 mΩ/°C and 0.0234 mΩ/°C for the low-side and high-side IGBTs, respectively.

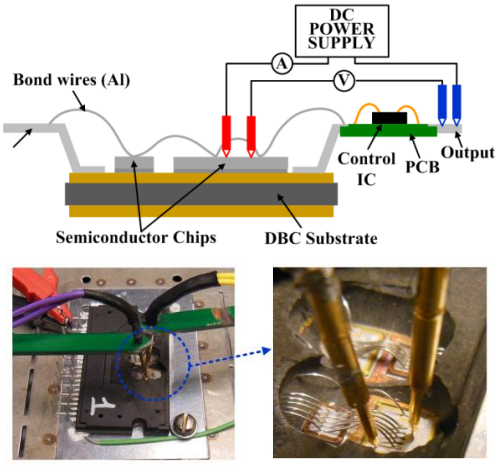

Fig. 2-15 Four-point probing method for the interconnection resistance measurement in an open-module.

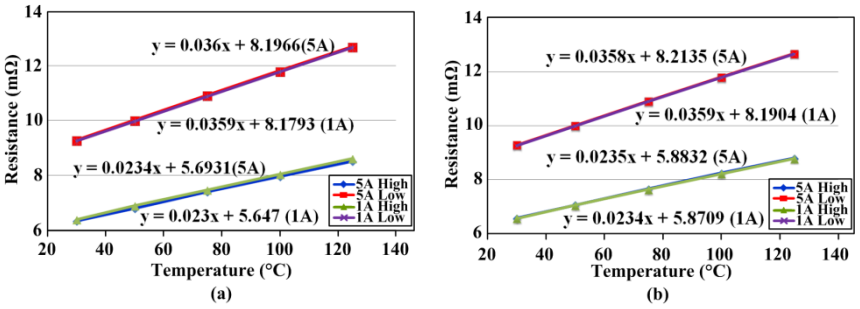

Fig. 2-16 Measured parasitic package resistances of high- and low-sides IGBTs in the open module as a function of temperature (a) module #1 (b) module #2.

2.2.4. COMPENSATION OF THE EFFECT OF INTERCONNECTION RESISTANCE ON T_J ESTIMATION

As analyzed above, the interconnection resistances are significantly changed by temperature variation and this change affects the measured voltage drop under the inverter operation.

Fig. 2-17 shows the simplified temperatures in the power module corresponding to an AC current, where T_{j_chip} is the real junction temperature of the device which means the average of temperature distribution on the chip surface, T_{j_est} is the estimated junction temperature using V_{CE_ON} and T_{Rint} is the average temperature of the interconnection materials in the module. The interconnection materials are represented by one equivalent resistor with an average temperature.

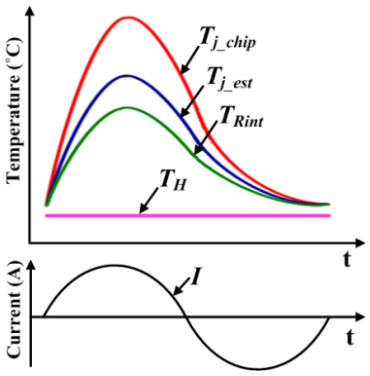

Fig. 2-17 Simplified temperatures in the power module according to an AC current.

If T_{Rint} is the same as T_{j_chip}, T_{j_est} would be the same as T_{j_chip}. However, T_{Rint} is not the same as T_{j_chip} under the converter operation and it leads to a lower V_{CE_ON} measurement than the one under the characterization condition, even though, the junction temperatures are the same. Consequently, the estimated junction temperature by V_{CE_ON} and the load current is smaller than the real one. Therefore, it is necessary to compensate for the voltage drop caused by the different temperature of the interconnection materials. However, it is challenging to know the temperature of each part of the interconnection materials during real operations.

A reasonable assumption, which has been further supported by the experimental observations, is that the temperature difference between T_{j_chip} and T_{Rint} during one fundamental period of the output current has the similar trend with the temperatures as shown in Fig. 2-17. Therefore, it can be expressed as (2.6) and the resistance variation can be represented as given in (2.7). Finally, the on-state voltage compensation V_{CE_comp} can be expressed as (2.8)

$$T_{j\_chip} - T_{Rint} = \alpha \cdot (T_{j\_est} - T_H) \tag{2.6}$$

$$\Delta R_{int} = \alpha \cdot (T_{j\_est} - T_H) \cdot RVF \tag{2.7}$$

$$V_{CE\_comp} = \Delta R_{int} \cdot I = \alpha \cdot (T_{j\_est} - T_H) \cdot RVF \cdot I \tag{2.8}$$

where T_H is the heat-sink temperature, α is the scaling factor, RVF is the Resistance Variation Factor and I is the output current.

Finally, the junction temperature can be corrected as

$$T_{j\_est\_comp} = K_{(I)} \cdot (V_{CE\_M} - V_{CE\_B(I)} + V_{CE\_comp}) + T_B \tag{2.9}$$

To find the scaling factor (α) of test modules, the IR (Infra-Red) camera and a black-painted open module have been used. By comparing the measured junction temperature by IR camera with the estimated one, the scaling factor α can be found. α and RVF factors are different according to the types of modules, because they have different resistances and structures. For this reason, it is difficult to generalize both factors for all modules. Therefore, efforts to find α and RVF are still needed. However, by the proposed approach, the junction temperature can be estimated more precisely under the converter operation. In addition, $V_{CE\_B(I)}$ and $K_{(I)}$ need to be updated repeatedly as V_{CE_ON} of the tested module increases during the power cycling test in order to exclude the effect of V_{CE_ON} increase due to the electrical degradation in the module on the junction temperature estimation.

2.2.5. EXPERIMENTS

Experiments have been carried out in order to verify the validity of the proposed method under 8 different operating conditions listed in Table 2-1 and Table 2-2. The low-side IGBT of phase-V is considered for the junction temperature estimation. *RVF* is 0.0359 mΩ/˚C and α is 0.93.

The junction temperature (T_j) has been measured by the IR camera in order to compare it with the estimated value. It is worth to point out that a non-uniform temperature distribution is typically observed in the chip surfaces [83, 84]. Therefore, an average temperature of the chip area has been used for comparison.

Fig. 2-18 shows comparison of the junction temperatures between IR camera and estimations using V_{CE_ON} and load current with and without compensation. The converter is operated under the operating condition 1 as listed in Table 2-1. The maximum T_{j_IR} measured by the IR camera is about 118.8 ˚C and the minimum is about 70 ˚C. The maximum estimated junction temperature T_{j_est} before the compensation is about 103 ˚C and the temperature difference with IR camera is about 15.8 ˚C. After the compensation, the maximum T_{j_est} is about 120.2 ˚C, yielding an error of less than 1.5 ˚C with respect to the measured temperature by the IR camera. The estimated temperature agrees well with the measured value.

The junction temperature estimations are also performed under the different operating Conditions 2, 3 and 4. Fig. 2-19 shows T_{j_IR} and T_{j_est} with compensation under the operating Condition 2. The maximum T_{j_est} is 140.2 ˚C and the maximum T_{j_IR} is about 142.3 ˚C. The temperature error between them is about 2 ˚C.

Table 2-1 Operating conditions for junction temperature estimation in IGBT module.

Parameters	Condition 1	Condition 2	Condition 3	Condition 4
DC-link voltage (V_{DC})	400 V	400 V	400 V	400 V
Output current (I_{peak})	30 A	30 A	25 A	25 A
Reference voltage (V_{ref})	140 V	140 V	140 V	145 V
Switching frequency (f_{SW})	10 kHz	10 kHz	10 kHz	10 kHz
Output frequency (f_{out})	3 Hz	1 Hz	5 Hz	0.5 Hz
Power factor (*PF*)	1	1	1	1
Heat-sink temperature (T_H)	50 ˚C	48 ˚C	50 ˚C	53 ˚C

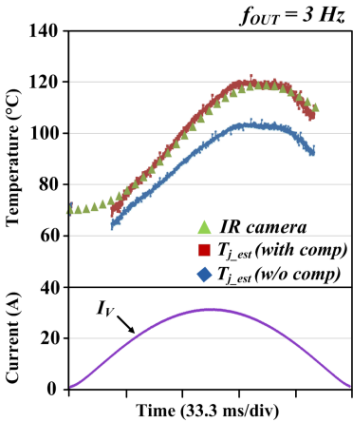

Fig. 2-18 Comparison of the junction temperature between IR camera and estimation using V_{CE_ON} and the load current with and without compensation.

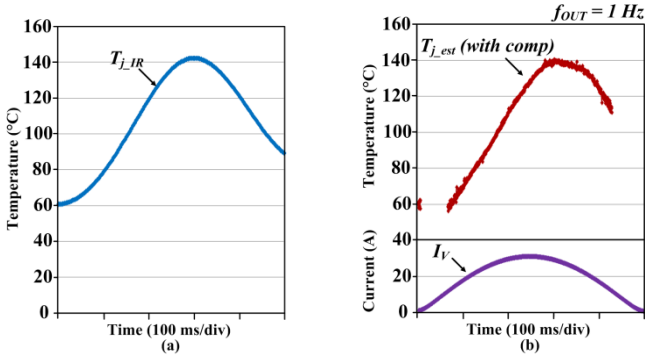

Fig. 2-19 Junction temperatures under the operating Condition 2
(a) IR camera measurement (b) estimation by the proposed method.

The junction temperatures under the operating Condition 3 are shown in Fig. 2-20. In this case, the temperature difference between maximum T_{j_est} and T_{j_IR} is about 0.5 ˚C. The estimated temperature is about 96.5 ˚C and measured one is 97 ˚C. Under the operating Condition 4, maximum T_{j_est} is about 139. 7 ˚C and T_{j_IR} is about 142 ˚C as shown in Fig. 2-21. The error is about 2.3 ˚C.

The junction temperature estimations under relatively fast output frequency conditions listed in Table 2-2 are also performed. In these cases, only the maximum junction temperature measured by the IR camera (T_{j_IR}) is presented for the comparison because the response of the IR camera is not fast enough to measure the temperature variation according to the output current.

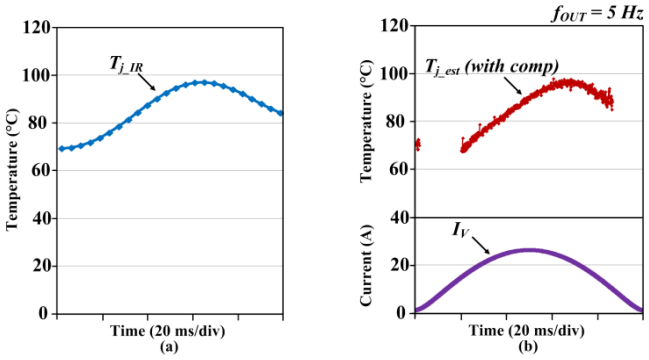

Fig. 2-20 Junction temperatures under the operating Condition 3
(a) IR camera measurement (b) estimation by the proposed method.

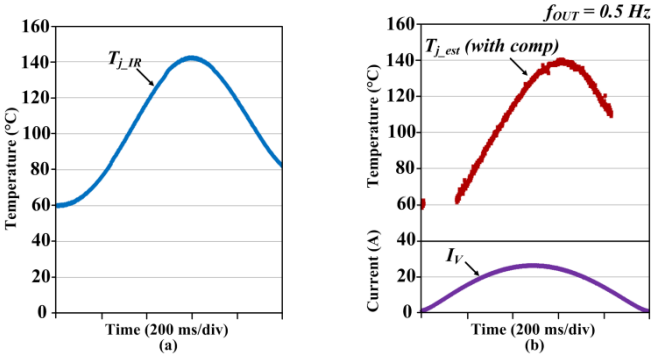

Fig. 2-21 Junction temperatures under the operating Condition 4
(a) IR camera measurement (b) estimation by the proposed method.

Fig. 2-22 (a) and (b) show the results of junction temperature estimation under the operating Conditions 5 and 6, respectively. The estimated temperature is about 100.7 ˚C and the measured value is 98.2 ˚C under the Condition 5. The junction temperature is a little bit over estimated in this case. The error is about 2.5 ˚C. In the case of 65 ˚C, the estimated value is also over estimated by 2.2 ˚C.

Fig. 2-23 (a) and (b) show the junction temperature estimation results when the cooperating Conditions are 7 and 8, separately. The estimation errors are about 2.7 ˚C and 1.9 ˚C when I_{peak} = 30 A and 25 A, respectively.

All estimation results are summarized in Table 2-3. As shown in Table 2-3, the estimated junction temperatures by the proposed method are in good agreement with the measured temperatures by the IR camera at various operating conditions.

Table 2-2 Operating conditions with relatively fast output frequencies.

Parameters	Condition 5	Condition 6	Condition 7	Condition 8
DC-link voltage (V_{DC})	400 V	400 V	400 V	400 V
Output current (I_{peak})	30 A	30 A	30 A	25 A
Reference voltage (V_{ref})	140 V	140 V	140 V	140 V
Switching frequency (f_{SW})	10 kHz	10 kHz	10 kHz	10 kHz
Output frequency (f_{out})	20 Hz	20 Hz	50 Hz	50 Hz
Power factor (PF)	1	1	1	1
Heat-sink temperature (T_H)	50 ˚C	65˚C	50 ˚C	50 ˚C

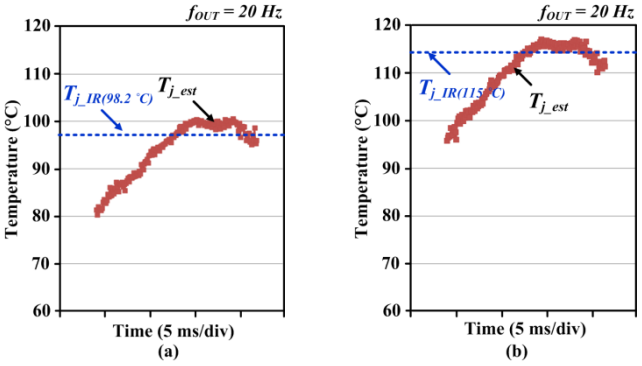

Fig. 2-22 Junction temperatures under the operating conditions (a) 5 (b) 6.

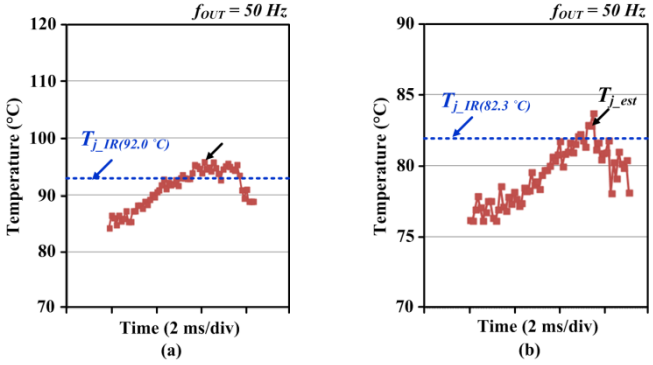

Fig. 2-23 Junction temperatures under the operating conditions (a) 7 (b) 8.

It is worth to point out that uncertainties come also from the IR measurement technique. First, the response of the IR camera is not fast enough to measure the correct maximum temperature when the output frequency goes beyond several tens of Hz. Therefore, the maximum temperatures under these conditions could be little bit higher than the measured values leading to smaller errors than the current values. Second, the measured temperatures by the IR camera are the average ones. For this reason, according to the area that is considered for the mean temperature, the measured value can be slightly changed. Furthermore, the black paint and the shading effect of the bond wire can also affect a little to the measured temperature value. Therefore, the error between estimation and measurement could be changed a bit but it is not significant.

It can be concluded from the results that the accuracy of the junction temperature estimation by using V_{CE_ON} and the load current is significantly improved by the proposed method.

Table 2-3 Comparison of T_j between estimation by the proposed method and measurement by the IR camera at different operating conditions.

	Method	***Tj* (˚C)**	**Error (˚C)**
Condition 1	IR Camera	118.8	1.4
	Estimation	120.2	
Condition 2	IR Camera	142.3	-2.1
	Estimation	140.2	
Condition 3	IR Camera	97.0	-0.5
	Estimation	96.5	
Condition 4	IR Camera	142	-2.3
	Estimation	139.7	
Condition 5	IR Camera	98.2	2.5
	Estimation	100.7	
Condition 6	IR Camera	115	2.2
	Estimation	117.2	
Condition 7	IR Camera	92.0	2.7
	Estimation	94.7	
Condition 8	IR Camera	82.3	1.9
	Estimation	84.2	

2.3. ADVANCED ACCELERATED POWER CYCLING TEST

2.3.1. IGBT POWER MODULE UNDER TEST

The power cycling tests have been performed with a 600 V, 30 A, 3-phase transfer molded Intelligent Power Module (IPM). Fig. 2-24 shows a vertical structure and configuration of the transfer molded IPM. The IPM consists of 6 IGBTs and 6 diodes and they are mounted on a Direct Bonded Copper (DBC) substrate with aluminum wire interconnection. The lead frame is connected to the DBC substrate by soldering and a copper surface of the DBC substrate is exposed to be contacted with an external heat-sink. Further, control Integrated Circuits (ICs) with Printed Circuit Board (PCB) are embedded inside the module too. This module is covered by Epoxy Molding Compound (EMC) instead of gel and there is no base-plate. Therefore, wear-out failure mainly occurs in bond-wire and chip solder joint due to thermo-mechanical stresses.

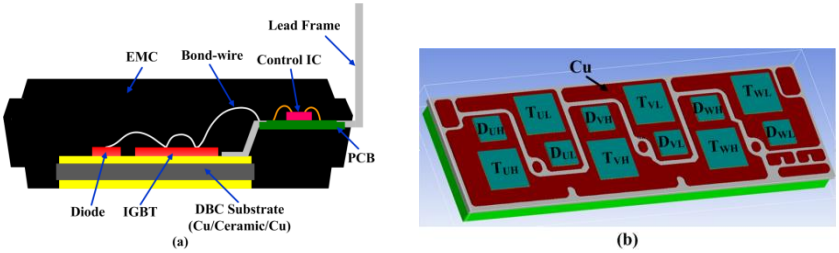

Fig. 2-24 Transfer Molded Intelligent Power IGBT Module
(a) vertical structure (b) configuration of power devices.

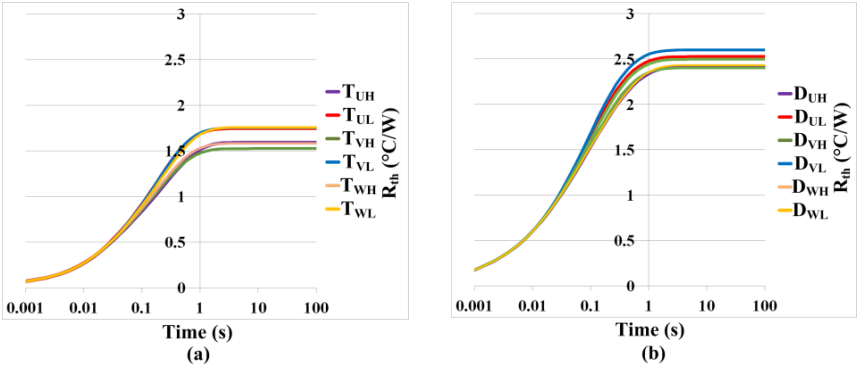

Fig. 2-25 Thermal impedances in transfer molded IPM by Finite Element Method simulation
(a) IGBTs (b) diodes.

Due to the asymmetric layout of the module, each device has a different thermal resistance as shown in Fig. 2-25 and the difference of the thermal resistance becomes larger as the transient time increases. Since this module is designed for inverter applications, the IGBT chip size is bigger than that of diode chip as shown in Fig. 2-24 (b). The diodes have higher thermal impedance than IGBTs. However, in this test, the tested IGBT module is operated under inverter mode with high power factor and thus the losses in IGBTs are dominant. Therefore, it leads to higher junction temperature and larger junction temperature variation than diodes. Besides the difference between the IGBTs and diodes, each IGBT and diode has different thermal impedance. For example IGBTs, the copper surface area around each IGBT is different as shown in Fig. 2-24 (b). In this module, the copper surface areas around the high side IGBTs are wider than the copper surface areas around the low-side IGBTs. A wider surface area means a smaller thermal resistance. Therefore, the low-side IGBTs have the larger thermal impedance than high side IGBTs as shown in Fig. 2-25 (a) and its difference between the high- and low-sides IGBT is bigger as the transition time is longer. From this result, it can be expected that the low-side IGBTs have a higher thermal stress during power cycling test and the failure may be expected to occur first among low side IGBTs.

2.3.2. ACCELERATED POWER CYCLING TEST

One of the important factors for the accelerated power cycling test is the test period. To get the results in the reasonable test time, proper temperature stresses and a temperature cycle period ($t_{\Delta Tj}$) should be chosen. Furthermore, the temperature cycle period is related to the failure mechanism of IGBT modules. Typically, short power cycling period leads to the failures in bond-wire, emitter metallization and chip solder joint but relatively long power cycling period (more than a few minute) also provokes the failure in base-plate solder joint [15]. As mentioned above, the target module of this project does not have the base-plate. In addition, in this test setup, it is possible to generate large temperature swing in a short period. Therefore, in this test, the power cycling period is chosen in the range from several hundred milliseconds to a few tens of seconds and it can be achieved by changing the output frequency f_{OUT}.

Further, control strategies of the test lead to the different number of cycles to failure. In [25], four control strategies are compared under the conventional power cycling tests. It concludes that the constant temperature swing and constant power losses are not suitable from a real application point of view, because both strategies compensate for the degradation effects. As the tested modules are degraded, the thermal impedance and power losses could be changed and it can lead to higher thermal stresses. This condition is more similar to the real applications. The compensations for the same temperature swing and power losses deliver a 3 times longer lifetime than the condition without compensations. Therefore, in this test methodology, the electrical test conditions are kept from its initial condition without

any compensation for the degradation of the tested modules during power cycling tests. Further, test conditions should be in the Safe Operating Area (SOA) of the test device in order to prevent the other failure mechanisms that could come from the operation outside of SOA.

The power cycling test has been performed under the operating condition 1 as listed in Table 2-4. Fig. 2-26 shows the temperature profile under the Condition 1 where T_{jmean} = (T_{jmax}+T_{jmin})/2. The power cycling test conditions are chosen based on the temperature of T_{VL}.

Table 2-4 Power cycling test conditions for Intelligent Power Module (IPM).

Parameters	Condition 1	Condition 2
DC-link voltage (V_{DC})	400 V	400 V
Output current (I_{peak})	30 A	21 A
output reference voltage (V_{ref})	140 V	113 V
switching frequency (f_{SW})	10 kHz	10 kHz
output frequency (f_{out})	1 Hz	0.1 Hz
power factor (PF)	1	1
Heat-sink temperature (T_H)	48 ˚C	59 ˚C
Junction temperature swing (ΔT_j)	81.6 ˚C	80.8 ˚C
Mean junction temperature (T_{jmean})	101.5 ˚C	102.3 ˚C

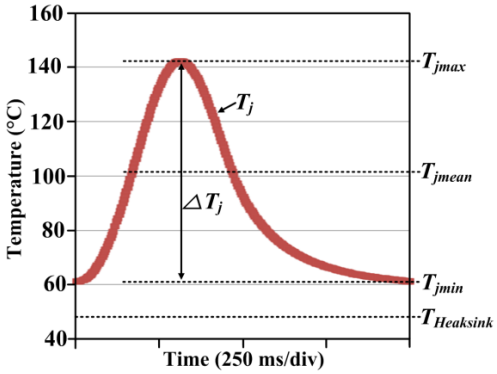

Fig. 2-26 Temperature profile measured by IR camera under the Condition 1.

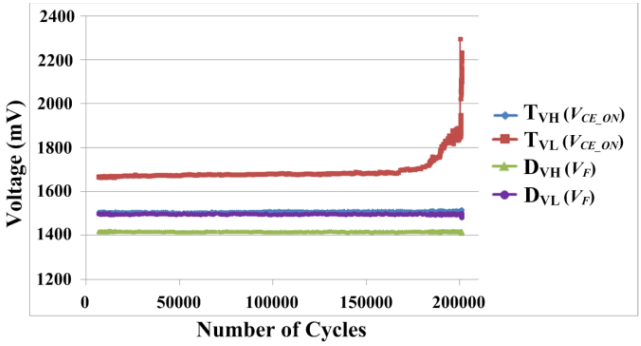

Fig. 2-27 Measured V_{CE_ON} and V_F of the IGBTs and diodes in phase-V during power cycling test under Condition 1 given in Table 2-4.

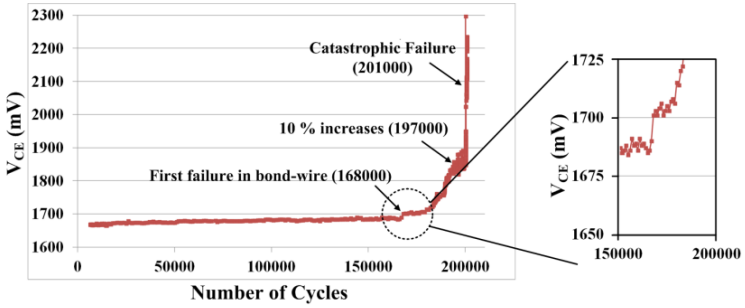

Fig. 2-28 V_{CE_ON} of low side IGBT of phase-V in detail from Fig. 2-27.

Fig. 2-27 shows the measured V_{CE_ON} and V_F of the IGBTs and diodes in the phase-V during the power cycling test. V_{CE_ON} and V_F are measured when the load current is 20 A_{peak}. As expected in Chapter 2.3.1, the failure occurs in the low-side IGBT first.

Fig. 2-28 shows V_{CE_ON} of the low-side IGBT of the phase-V in detail. It seems that the first failure occurs in bond-wire at about 168 K cycles, because there is a sudden increase of V_{CE_ON}. After 197 K cycles, V_{CE_ON} increases by 10 % from its initial value and a catastrophic failure occurs after 201 K cycles.

Fig. 2-29 shows the power cycling result of another module under the same operating condition. V_{CE_ON} is measured at 20 A_{peak} for all power devices. If V_{CE_ON} increases more than 10-15% from its initial value, the test is stopped to protect the tested module against catastrophic failure. The failure occurs in T_{VL} first. After 176 k cycles, there is a sudden increase in V_{CE_ON} of T_{VL} and then it increases by 10 %

after 216 k cycles. This test takes about 60 hours until it is finished. Even though test is stopped after V_{CE_ON} of T_{VL} increases above the set point, it can be expected that T_{UL} will be fail next because there is a sudden increase just before the test is stopped. This result also reflects well the previous analysis that the low-side IGBTs have the higher thermal stresses compared to the high-side IGBTs due to the different thermal impedance caused by asymmetric layout.

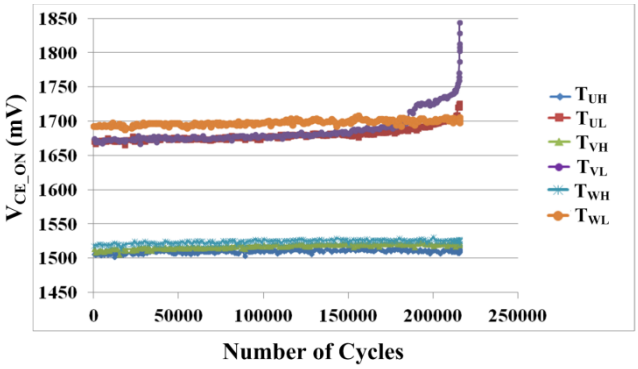

Fig. 2-29 Accelerated power cycling test result with another module under the operating Condition 1 specified in Table 2-4.

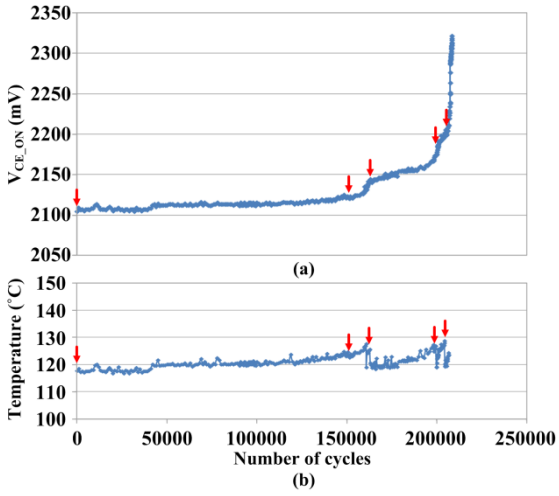

Fig. 2-30 Power cycling test results with junction temperature monitoring under the Condition 1 (a) on-state collector-emitter voltage (V_{CE_ON}) (b) estimated junction temperature at 29 A.

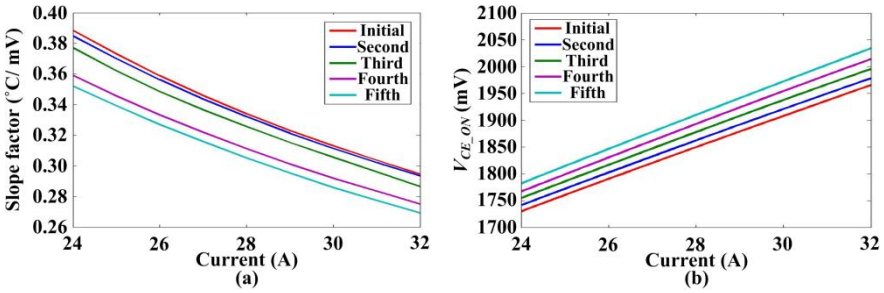

Fig. 2-31 Change of parameters for junction temperature estimation during power cycling test(a) slope factor (b) base V_{CE_ON} as a function of current ($V_{CE\_B(1)}$) at 30 °C (see eq. (9)).

Fig. 2-30 shows the power cycling test result with on-line junction temperature monitoring under the Condition 1 where red arrow indicates the re-characterization points. In this test, V_{CE_ON} is measured at 29 A and the junction temperature is estimated at this point. The I-V characterization is performed at initial stage and the estimated temperature is about 118 ℃. If the estimated junction temperature (T_j) increases by a certain level due to V_{CE_ON} increase, the I-V characterization needs to be performed again to eliminate the effect of the electrical degradation on T_j estimation and to determine V_{CE_ON} increase either due to bond-wire fatigue or due to solder joint fatigue. This point can be set properly within end-of-life criteria, for example, 20 % increases of thermal impedance, and can be checked in real time. As V_{CE_ON} increases during the test, the estimated T_j also increases as shown in Fig. 2-30. At 150000 and 163883 cycles where V_{CE_ON} increases by about 25 mV and 40 mV, respectively, the I-V re-characterization is performed and the estimated T_j decreases by its initial value. The I-V characterization is performed two times again at 199422 and 205238 cycles, separately until V_{CE_ON} increases by 5 %. As shown in the result, the estimated T_j decreases after re-characterization. It means that there is no thermal resistance increases during the test. Therefore, it can be expected that the main cause of V_{CE_ON} increases is not due to the solder joint fatigue but due to the bond-wire fatigue in this test condition. Fig. 2-31 shows the change of parameters for the junction temperature estimation during the power cycling test.

The power cycling test has been performed under the Condition 2 as given in Table 2-3 to investigate the effect of the temperature cycle period ($t_{\Delta Tj}$) (or temperature swing duration) on lifetime of the IGBT module. In this condition, the temperature stresses ΔT_j and T_{jmean} are almost the same with condition 1 but f_{OUT} is changed from 1 (1 s) to 0.1 Hz (10 s). This test is continued for about 370 hours. In this case, T_{UL} fails first as shown in Fig. 2-32 (a). After 133 K cycles, V_{CE_ON} *of* T_{UL} increases by more than 10 % from its initial value and the power cycling test is stopped. As shown in Fig. 2-32 (b), there is a significant difference in the number of cycles to failure between Condition 1 and Condition 2. This result shows that the temperature

swing duration is also one of the important factors to affect the lifetime and it should be considered when the power cycling test is performed and a lifetime model is developed from the test results. A more detailed investigation about this impact will be performed in chapter 3.

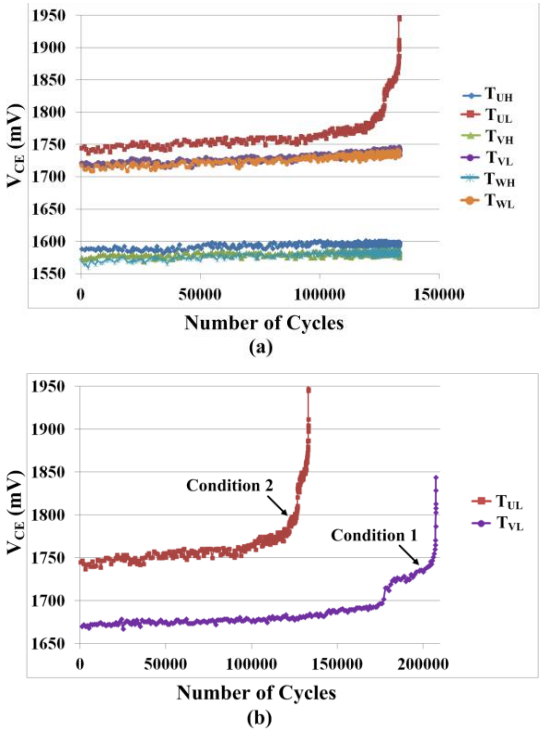

Fig. 2-32 Result of the accelerated power cycling test (a) under the operating Condition 2 (b) comparison of the number of cycles to failure between Condition 1 and Condition 2.

2.4. SUMMARY

This paper has presented a methodology and apparatus for an advanced accelerated power cycling test of power device modules. The detailed explanations of configuration, features and control methods for different functions of advanced accelerated power cycling test setup has been presented. Two on-line V_{CE_ON} measurement concepts also have been discussed. By applying the on-line V_{CE_ON} measurement circuit, the degradation of the tested power module can be monitored in real time which gives a convenience to perform the test.

An improved junction temperature estimation method has been proposed using V_{CE_ON} and load current. An I-V characterization curves for the tested devices are obtained by the proposed simple switching sequence with on-line V_{CE_ON} measurement. By means of the proposed method, the estimation error which comes from the different temperatures of the interconnection materials in the module is compensated and it leads to satisfactory estimated results. Further, it can be used to monitor the solder joint degradation.

In addition, accelerated power cycling tests with 600V, 30A Intelligent Power IGBT modules have been performed under two different test conditions in order to verify the validity and effectiveness of the proposed power cycling test concept. By the proposed concept of applying the temperature swing, it is possible to apply various magnitudes of temperature swing in a short cycle period and to change the temperature cycle period easily. Thanks to a short temperature cycle period, test results can be obtained in a reasonable test time.

The proposed accelerated power cycling concept is expected to be useful for developing lifetime models as well as investigating the reliability performance of power device modules under more realistic electrical operating conditions.

CHAPTER 3. LIFETIME MODELING OF POWER IGBT MODULE

3.1. WEIBULL ANALYSIS

Reliability is defined as the ability of an item to perform the required function under stated conditions for a certain period of time [100]. The reliability is typically represented by the probability of survival and failure rate because it is influenced by variability such as variations in manufacturing process, environments and any other varying factors. Therefore, in reliability modeling, the statistical data analysis is an essential in order to deal with uncertainty.

3.1.1. WEIBULL DISTRIBUTION

A Weibull distribution, especially suited for the description of end-of-life phenomena, is a popular distribution in reliability engineering for analyzing life data. The cumulative failure distribution function $F(t)$ is defined as [101, 102]

$$F(t) = 1 - exp\left[-\left(\frac{t - t_0}{\eta - t_0}\right)\right]^{\beta} \tag{3.1}$$

where F = probability of failure, t = test statistic (time or number of cycles), t_0 = minimum life (failure free period defined as $-\infty < t_0 < \infty$, often zero) time or number of cycles), β = Weibull slope or shape parameter, η = characteristic life (where F = 63.2% or also called scale parameter).

Small number of β indicates a distribution that is spread out. Large β number indicates that the tested items are more homogeneous. In addition, β also gives other information. If $\beta > 1$, it means increasing risk and thus tested items are worn-out. If $\beta = 1$, it indicates constant risk. Therefore, the failure occurs randomly in time. If $\beta < 1$, it denotes decreasing risk. It often occurs with a weak population or it means that the tested items are worn-in. Usually, larger β is desired as long as the characteristic lifetime is high enough [102].

Fig. 3-1 shows the plots of a cumulative distribution function and probability density function according to β as an example.

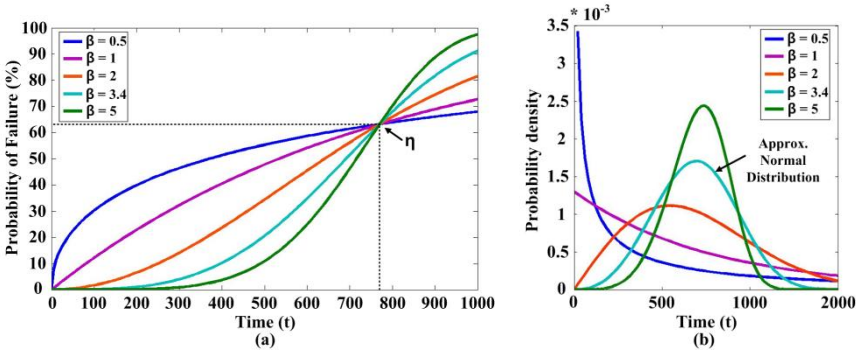

Fig. 3-1 Plots of a cumulative distribution function and probability density function according to β (a) cumulative distribution function (b) probability density function [101].

If $t_0 = 0$ which is called 2-parameter Weibull distribution, (3.1) can be rewritten as

$$\frac{1}{1-F(t)} = exp\left(\frac{t}{\eta}\right)^{\beta} \tag{3.2}$$

By taking two natural logarithms into (3.2), it will take the form of

$$ln\,ln\frac{1}{1-F(t)} = \beta(ln\,t) - (\beta\,ln\,\eta) \tag{3.3}$$

It can be seen that (3.3) has a linear form of $Y = \beta X + C$ where $X = ln(t)$, $Y = ln\,ln\frac{1}{1-F(t)}$ and $C = -\beta\,ln(\eta)$. Therefore, (3.3) can be represented as a straight line with a slope of β and intercept C on the Cartesian X, Y coordinates. Hence, if the data follows the 2-parameter Weibull distribution, the plot of $ln\,ln\frac{1}{1-F(t)}$ against $ln(t)$ will be a straight line with the slope of β in the Weibull probability plot [101].

3.1.2. MEDIAN RANK

As mentioned above, in reliability engineering, the statistical data is essential. As the sample size for the test is larger, more correct results can be obtained. However, there is limitation in sample size due to reasons such as cost and time for tests. In this situation, the data ranking is a good solution for the compensation of small sample size because it provides an estimate of what percentage of population is represented by the particular test sample [101].

Median rank is one of the most widely used methods for probability plotting in reliability engineering. It is defined as a cumulative percentage of the population represented by a particular sample with 50 % confidence level. It can be calculated simply by the Benard's approximation [101-103] as

$$MR(\%) = \left(\frac{j - 0.3}{N + 0.4} \right) \times 100 \tag{3.4}$$

where j = failure order number and N = sample size.

Table 3-1 shows the median rank of each sample according to the sample size. For example median rank of 2nd order sample out of six samples, those two samples represents the 26.56 % of the total population with 50 % confidence.

Table 3-1 Median rank of each sample according to sample size (value is given in percentage)

	Sample size									
Rank order	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
1	50.00	29.16	20.58	15.91	12.96	10.93	9.46	8.33	7.45	6.73
2		70.83	50.00	38.63	31.48	26.56	22.97	20.23	18.08	16.35
3			79.41	61.36	50.00	42.18	36.48	32.14	28.72	25.96
4				84.09	68.52	57.81	50.00	44.04	39.36	35.58
5					87.03	73.43	63.51	55.95	50.00	45.19
6						89.06	77.02	67.86	60.64	54.81
7							90.54	79.76	71.28	64.42
8								91.67	81.91	74.03
9									92.55	83.65
10										93.27

3.1.3. SAMPLE SIZE

The larger sample size gives better results but increases the cost and test time. On the contrary, the smaller sample size decreases the cost and test time, however, increases the uncertainty of results. Therefore, it is important to choose the proper sample size in reliability test considering above factors.

From the median rank, the uncertainty is calculated as

$$Uncertainty = 1 - (MR_{\_higest\ (\%)} - MR_{\_lowest\ (\%)}) \tag{3.5}$$

where $MR_{\_higest}$ = the highest median rank for given sample size, $MR_{\_lowest}$ = the lowest median rank for given sample size [104].

Fig. 3-2 shows the uncertainty according the sample size. A sample size of six is down in the knee of the curve and the sample size of twelve is beyond the knee of the curve. It can be seen that six to twelve samples would be appropriate for the test. Therefore, in this project, the sample size of six is chosen for the power cycling test.

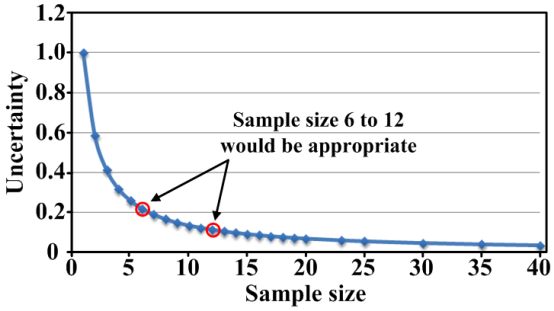

Fig. 3-2 Uncertainty according to sample size in Weibull plotting.

3.2. EFFECT OF TEMPERATURE SWING DURATION ON LIFETIME OF IGBT MODULE

The temperature stresses are the major stressors to kill the IGBT module. While the impacts of temperature swing (ΔT_j) and mean temperature (T_{jmean}) on the degradation of IGBT modules are well investigated, there is still lack of quantitative study on the impact of temperature swing duration ($t_{\Delta Tj}$).

Therefore, this test aims to investigate $t_{\Delta Tj}$ impact on lifetime and failure mechanism of tested modules under different $t_{\Delta Tj}$ conditions. The test results will be used when the lifetime model is developed considering $t_{\Delta Tj}$ impact.

3.2.1. TEST CONDITIONS

Six operating conditions are found using IR camera with an open module covered by black paint to investigate the $t_{\Delta Tj}$ impact. The low side IGBT of the phase-V (T_{VL}) is considered to standard device for finding the conditions.

Table 3-2 shows the six different operating conditions. They have almost the same ΔT_j and T_{jmean} (about 81 ˚C and 102 ˚C, respectively) but different $t_{\Delta Tj}$. Different $t_{\Delta Tj}$ is achieved by changing the output frequency from 0.1 to 1.7 Hz. In the cases of conditions 5 and 6, the switching frequencies are changed from 10 to 12 and 15 kHz, respectively to get the same ΔT_j in a short period. All conditions are in the Safe Operating Area (SOA) of the test device to prevent the other failure mechanisms that could come from the operation outside of SOA.

Fig. 3-3 shows the temperature profiles measured by IR camera under the six different operating conditions.

Table 3-2 Operating conditions to investigate the $t_{\Delta Tj}$ impact

Condition	$t_{\Delta Tj}$ (S)	f_{OUT} (Hz)	f_{SW} (kHz)	I (A)	V_{ref} (V)	T_H (˚C)	ΔT_j (˚C)	T_{jmean} (˚C)
1	10	0.1	10	21	113	59	80.8	102.3
2	5	0.2	10	22	115	57	80.6	102.5
3	2	0.5	10	25	145	53	82.0	101.3
4	1	1	10	30	140	48	81.6	101.5
5	0.8	1.25	12	30	140	50	81.8	102.4
6	0.59	1.7	15	30	143	48	80.8	102.0

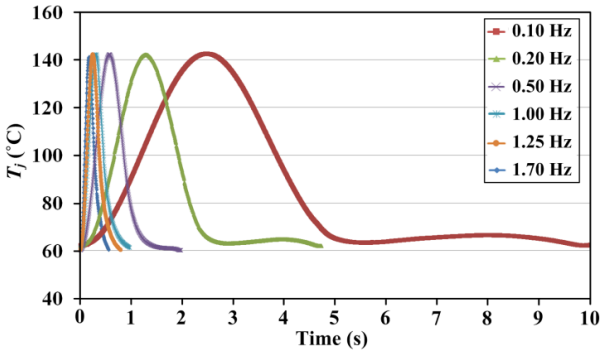

Fig. 3-3 Temperature profiles under the six operating conditions.

3.2.2. POWER CYCLING TEST RESULT

The accelerated power cycling test has been stopped if V_{CE_ON} increases by 10 - 15% from its initial value to protect tested devices against catastrophic failure.

Fig. 3-4 shows power cycling test results of the six samples under the six conditions. Depending on the testing samples and test conditions, the accelerated power cycling test has lasted for about 35 to 480 hours. For all cases, the wear-out failure occurs firstly in the low side IGBT. The minimum number of cycles to failure per condition is summarized in Table 3-3. 5% increase of V_{CE_ON} is considered as the end-of-life. As $t_{\Delta Tj}$ increases, the number of cycles to failure decreases. In the case of 0.1 Hz, it is about 128900 cycles and it is about 211201 when f_{OUT} is 1.7 Hz. Further, among the IGBT modules under the same test conditions, the number of cycles to failure are different each other from about 20000 to 45000 cycles.

As it can be seen from the results, $t_{\Delta Tj}$ has a significant impact on the lifetime of IGBT module. Further, the statistical analysis is required because each sample has the different lifetime even though they are tested under the same condition.

Table 3-3 The minimum number of cycles to failure per test condition

Condition	1	2	3	4	5	6
f_{OUT}	0.1	0.2	0.5	1.0	1.25	1.70
N of cycles	128900	159900	182441	190700	197500	211201
Test period (hours)	370	230	105	57	45	35

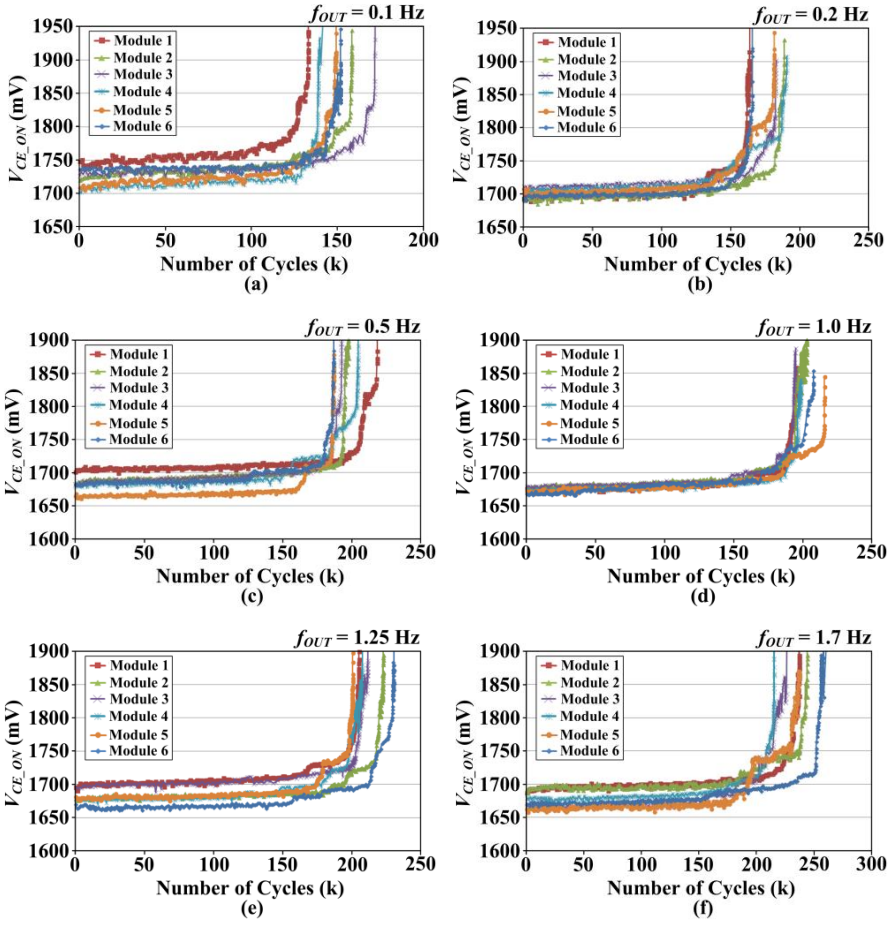

Fig. 3-4 Power cycling test results under six different conditions (a) Condition1 (b) Condition 2 (c) Condition 3 (d) Condition 4 (e) Condition 5 (f) Condition 6.

3.2.3. COMPARISON BASED ON DEFORMATION WORK

The degradation of a solder joint or a bond-wire may be able to be modeled by a uni-axial bimetallic approximation of the thermo-mechanical stress/strain which occurs at the interface between two different materials [105].

For example solder joint, the strain γ arising due to the Coefficient of Thermal Expansion (CTE) mismatch of two different materials under the temperature excursion can be described as follows

$$\gamma = L \cdot \Delta\alpha \cdot (T - T_0)/h \tag{3.6}$$

where L is the distance between the solder joint and the neutral point in the package, T is the immediate temperature, T_0 is the reference temperature, $\Delta\alpha$ is the difference of CTE of two materials and h is the solder joint height [106].

Three mechanical behaviors, elastic, plastic and creep behaviors can be observed in solder materials when the cyclic strain is applied and strain can be represented as a function of the applied stress σ.

The elastic strain γ_{el} is represented as

$$\gamma_{el} = \frac{\sigma}{G_0 - G_1 \cdot T(^\circ C)} \tag{3.7}$$

where G_0 is the modulus at 0 ˚C, G_1 is the temperature dependence, and T is the temperature in ˚C.

Further, the plastic strain is also expressed as

$$\gamma_{pl} = C_1 \left(\frac{\sigma}{G} \right)^m \tag{3.8}$$

where G is G_0 - G_1T, C_1 is the plastic strain coefficient, and m is the stress sensitivity of plastic strain.

Finally, the creep strain γ_{cr} is described as

$$\frac{d\gamma_s}{dt} = C_2 \frac{G}{T} \left[sinh\left(\alpha \frac{\sigma}{G} \right) \right]^n exp\left(\frac{-Q}{kT} \right) \tag{3.9}$$

$$\gamma_{cr} = \frac{d\gamma_s}{dt}t + \gamma_T\left(1 - exp\left(-B\frac{d\gamma_s}{dt}t\right)\right) \tag{3.10}$$

where $d\gamma_s/dt$ is the steady state creep rate, C_2 is a coefficient, α is the multiplier of stress, n is the stress sensitivity of steady-state creep rate, Q is activation energy, k is the Boltzmann's constant, γ_T is the transient creep strain, B is the transient creep coefficient and T is the temperature in Kelvin [107, 108].

Consequently, considering above three behaviors, the total strain γ_{total} can be obtained as a function of the applied stress σ as below

$$\begin{aligned}\gamma_{total} &= \gamma_{el} + \gamma_{pl} + \gamma_{cr} \\ &= \frac{\sigma}{G_0 - G_1 \cdot T(^\circ C)} + C_1\left(\frac{\sigma}{G}\right)^m \\ &\quad + C_2\frac{G}{T}\left[sinh\left(\alpha\frac{\sigma}{G}\right)\right]^n exp\left(\frac{-Q}{kT}\right)t \\ &\quad + \gamma_T\left(1 - exp\left(-BC_2\frac{G}{T}\left[sinh\left(\alpha\frac{\sigma}{G}\right)\right]^n exp\left(\frac{-Q}{kT}\right)t\right)\right)\end{aligned} \tag{3.11}$$

By putting (3.6) into (3.11), (3.11) can be solved and the solution of (3.11) for a temperature cycle can be represented as a stress-strain hysteresis loop as shown in Fig. 3-5 [109]. The loop area represents the deformation work (ΔW) or deformation energy that has been spent during a temperature cycle. If the accumulated deformation work is reached to deformation work to failure, the solder joint will fail [105].

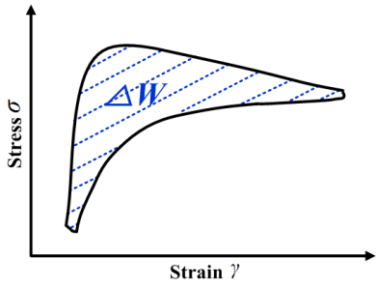

Fig. 3-5 Stress σ – strain γ loop of the solder joint for a temperature cycle [108].

The comparison of the stress-strain curves under the six power cycling test conditions listed in Table 3-2 is performed. The SnAg3.5 solder and Al_2O_3 are used for the case study and the related parameters for (3.6) and (3.11) are summarized in Table 3-4 [35, 107].

Fig. 3-6 shows the stress-strain curves under the six test conditions. As the output frequency decreases, the stress-strain curve area increases. In other word, longer $t_{\Delta Tj}$ has the larger deformation work during the temperature cycle. Therefore, the number of cycle to failure decreases as $t_{\Delta Tj}$ increases. This analysis can support the experimental results listed in Table 3-3 indirectly.

It should be noted that the hysteresis stress-strain loops in Fig. 3-6 are to show the different loops area under the six different conditions. The value of stress and strain does not mean real stress and strain values under the tested conditions because the *L*/*h* is normalized by 1.

Table 3-4 Parameters in (3.6) and (3.11) for SnAg3.5 solder [35, 106]

Parameter	G_0 (Mpa)	G_1 (Mpa)	***m***	***α***	C_2	C_1 (sec/Mpa)	***n***
Value	$1.93 \cdot 10^4$	$0.689 \cdot 10^2$	4.4	1300	$2.0 \cdot 10^{11}$	0.709	5.5
Parameter	***Q* (eV)**	***k***	***B***	γ_T	α_{Si} (ppm/˚C)	α_{Al2O3} (ppm/˚C)	***L/h***
Value	0.4	$1.3806 \cdot 10^{-23}$	147	0.086	2.6	6.8	1

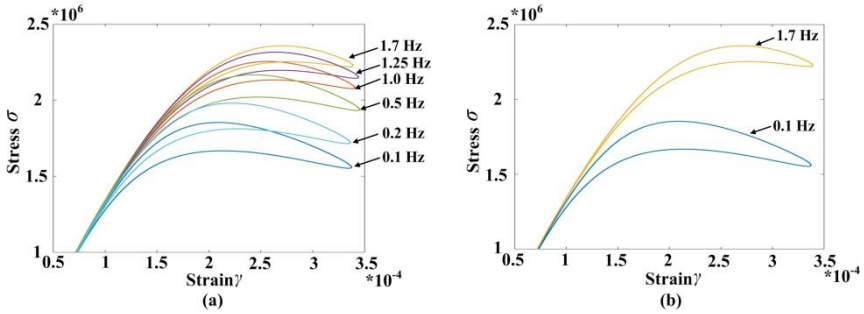

Fig. 3-6 Stress σ – strain γ loop of the solder joint (a) under the six different temperature cycles (b) selected conditions for comparison.

3.3. JUNCTION TEMPERAUTRE SWING DURATION DEPENDENT LIFETIME ANALYSIS BASED ON TEST DATA

In this chapter, the lifetime analysis according the power cycling test data is discussed. Typically, 5 to 20 % increase of V_{CE_ON} is considered as the end-of-life and the numbers of cycles until these periods are counted for the lifetime [35]. In this project, 5 % increase is considered as its end-of-life criteria for a lifetime model.

The time to failure of the tested IGBT modules under the six test conditions are presented by Weibull distribution [101]. The results shown in Fig. 3-4 are analyzed using the software tool Weibull ++ [110]. The lifetime of a population of IGBT modules can be defined with different criteria in terms of time to how much percentage of accumulated failure. Further, it is important to obtain the predicted lifetime range with a certain confidence Boundaries (CB) because the time to failure of each IGBT module varies.

Fig. 3-7 shows the Weibull plots under the six different conditions with 90 % CB and the lifetime under the different definitions and confidence levels is summarized in Table 3-5. In the case of B_{10} lifetime which is the time to 10 % of total population is fail, the nominal B_{10} lifetime of six conditions is 127800, 154767, 179000, 187694, 192225 and 205884 cycles, respectively. The lifetime of IGBT modules under the test condition 4 with 90 % confidence level is expected within 178500 to 197361 cycles. While with 99 % confidence level, the lifetime range is extended to from 173498 to 203051 cycles. The lifetime under the different definition can also be explained with a similar way. Totally, the lifetime with 4 different definitions with 2 different confidence levels is given in Table 3-4 where *MTTF* is Mean Time to Failure. The lifetime related to $t_{\Delta Tj}$ effect can be modeled by inverse power law [111] as (3.12)

$$N_f = A \cdot (t_{\Delta Tj})^{-n} \tag{3.12}$$

where N_f = the number of cycles to failure, $t_{\Delta Tj}$ = temperature swing duration, and A and n are fitting parameters.

For B_{10} lifetime model, A and n are obtained as 189866 and 0.148, respectively based on the nominal lifetime and the corresponding lifetime model for the studied IGBT module is plotted as shown in Fig. 3-8. However, it should be noted that values of parameters A and n could be varied according to different lifetime definition and confidence level because the IGBT modules have the different number of cycles to failure as analyzed above. For example, B_1 lifetime model, A and n are defined as 170385 and 0.16 respectively. Therefore, it is important to know specific lifetime definition of a lifetime model.

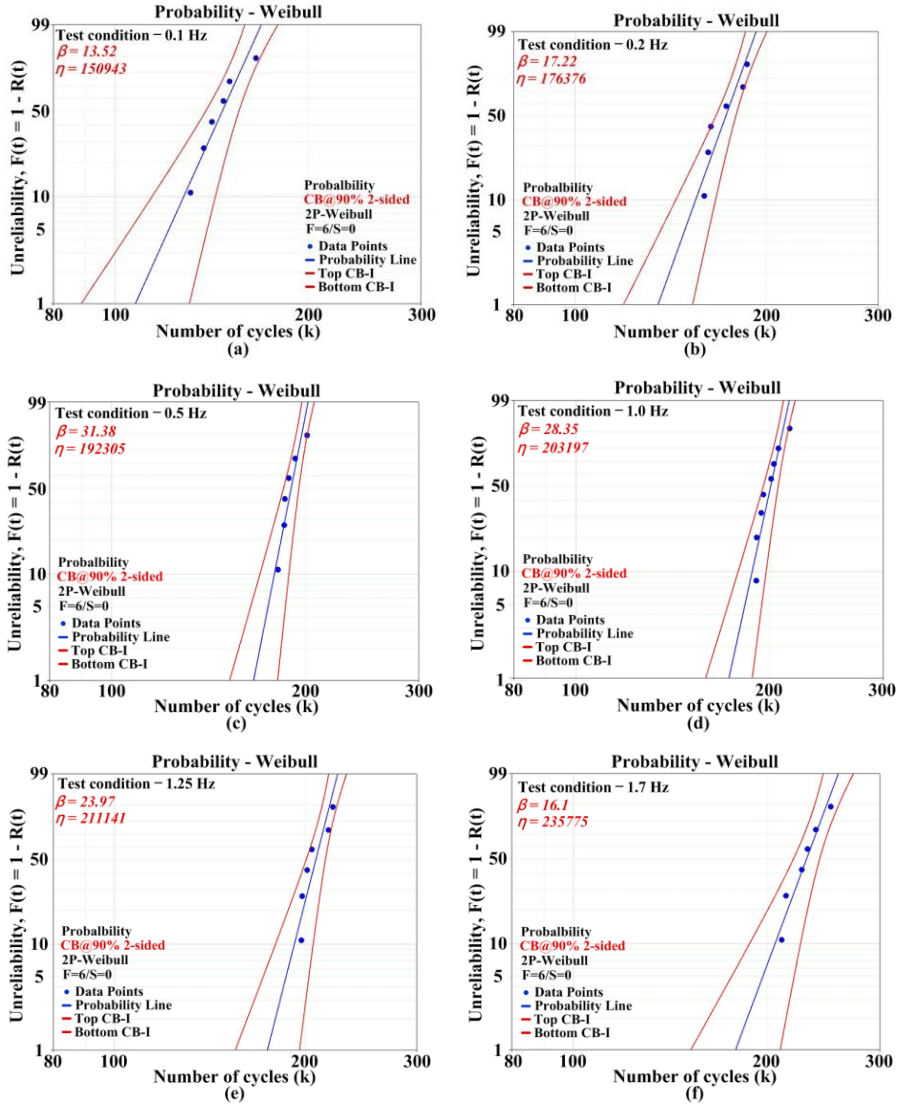

Fig. 3-7 Lifetime analysis based on power cycling test results in Weibull plots.

Table 3-5 Lifetime analysis with different definitions and confidence levels.

Condition		***Lifetime (cycles)***							
		B_1		***B_{10}***		***$B_{\eta\ (\eta=63.2)}$***		***MTTF***	
		Confidence level		Confidence level		Confidence level		Confidence level	
		99%	90%	99%	90%	99%	90%	99%	90%
0.1 Hz	Bottom CB	79188	88412	106906	114031	138888	143128	131599	136383
	Nominal value	107413		127800		150930		145264	
	Top CB	145697	130497	152777	143231	164036	159176	160348	154724
0.2 Hz	Bottom CB	104935	114946	133875	141079	165321	169233	158220	162732
	Nominal value	135025		154767		176372		171021	
	Top CB	173741	158610	178920	169784	188163	183813	184858	179733
0.5 Hz	Bottom CB	145126	152378	165053	169964	185204	187739	180412	183454
	Nominal value	166089		179000		192303		188956	
	Top CB	190079	181032	194126	188517	199675	196978	197904	194622
1.0 Hz	Bottom CB	151630	158953	173498	178500	195942	198533	190567	193679
	Nominal value	172767		187694		203194		199302	
	Top CB	196851	187782	203051	197361	210715	207965	208438	205088
1.25 Hz	Bottom CB	145099	155034	172652	179485	201303	204804	194635	198810
	Nominal value	174278		192225		211138		206407	
	Top CB	209323	195910	214015	205868	221454	217669	218892	214295
1.7 Hz	Bottom CB	138985	152205	178349	187848	220554	225937	211242	217282
	Nominal value	178710		205884		235770		228378	
	Top CB	229788	209830	237670	225652	252036	246031	246905	240042

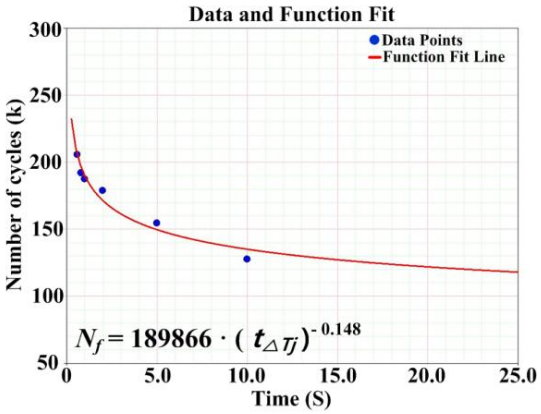

Fig. 3-8 B_{10} lifetime model under different junction temperature swing duration ($t_{\Delta Tj}$).

Table 3-6 shows the parameter values of (3.12) under different lifetime definitions.

The obtained model can be used together with impact of other parameters such as junction temperature swing (ΔT_j) and mean junction temperature (T_{jmean}). Therefore, the lifetime model can be extended from the widely used Coffin-Manson-Arrhenius lifetime model [112] as shown in (3.13)

$$N_f = \alpha \cdot (\Delta T_j)^{-n1} \cdot e^{E_a/(k \times T_{jmean})} \cdot A \cdot (t_{\Delta Tj})^{-n2} \tag{3.13}$$

The parameters α and n_1 can also be obtained from accelerated power cycling test. By including $t_{\Delta Tj}$ impact to lifetime model, lifetime prediction of the IGBT module regarding temperature stresses could be improved.

Table 3-6 Parameters of eq. (3.12) under different selected lifetime definitions

Lifetime	***A***	***n***
B_1	*170385*	*0.160*
B_{10}	*189866*	*0.148*
B_{20}	*196567*	*0.144*
B_{30}	*200000*	*0.135*
B_η	*200000*	*0.102*
MTTF	*200000*	*0.166*

3.4. PHYSICS-OF-FAILURE ANALYSIS OF TESTED IGBT MODULES

The physics-of-failure analysis of the tested modules is performed to investigate the failure mechanism of the IGBT module.

The tested modules under the Conditions 1 and 4 listed in Table 3-2 which have relatively long and short $t_{\Delta Tj}$ are considered for the failure mechanism investigation and compared with new one.

The tested modules are decapsulated by heated fuming nitric acid to investigate inside of the module since the target module is covered by Epoxy Molding Compound (EMC). The physical analysis has been done by Optical/ Scanning Electron Microscope (SEM) inspection.

Fig. 3-9 shows an analysis result of tested module under the Condition 4 in Table 3-2 as shown in Fig. 2-27. Abnormal high current flows at the end of test due to the catastrophic failure and thus metal, silicon and emitter bond-wires of low side IGBT of phase-V (T_{VL}) are fused. Under this condition, it is impossible to investigate the failure mechanism correctly and it is important to stop the power cycling test before the catastrophic failure occurs which is possible by the on-line V_{CE} measurement.

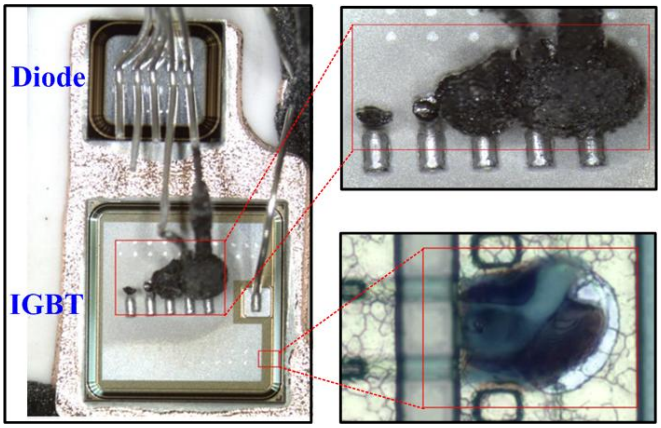

Fig. 3-9 Failure analysis of the tested module corresponding to Fig. 2-27 under the operating Condition 4 given in Table 3-2.

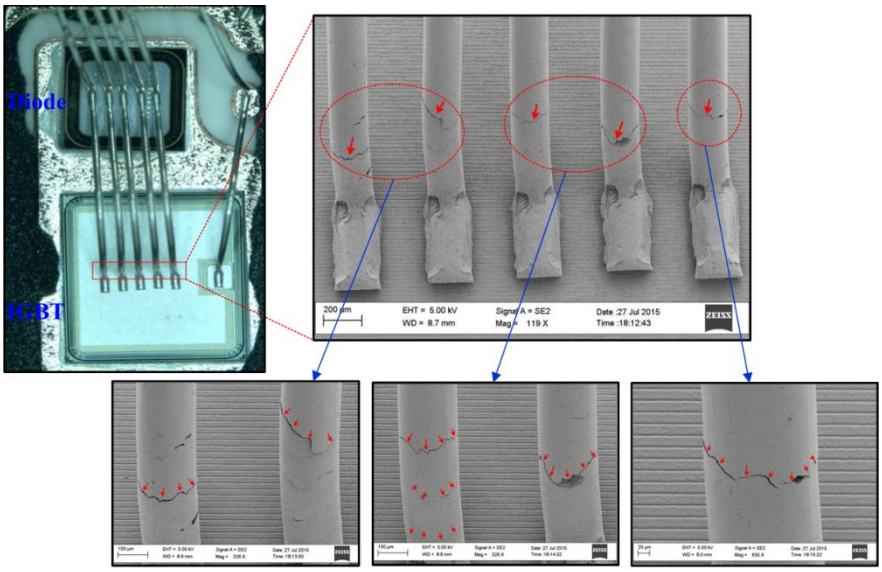

Fig. 3-10 Failure analysis of the tested module corresponding to Fig. 2-29 under the operating Condition 4 in Table 3-2 where the power cycling test was stopped before catastrophic failure occurs (cracked bond-wires – Red arrow).

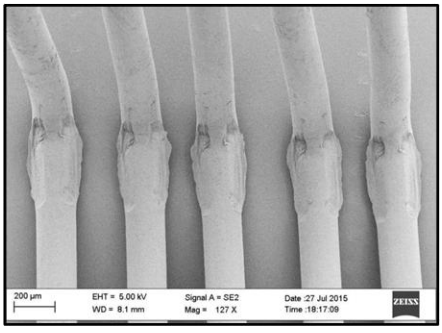

Fig. 3-11 SEM image of the diode D_{VL} of tested module under the operating Condition 4 in Table 3-2.

The physics-of-failure analysis of the second tested module under the same operating condition has been performed. In this case, the power cycling test was stopped when V_{CE_ON} increases by 10 - 15 % from its initial value as shown in Fig. 2-29. Fig. 3-10 shows the analysis results. The bond-wire cracks are observed in all 5 bond-wires of T_{VL}. This is the reason that V_{CE_ON} increases as shown in the power cycling test results.

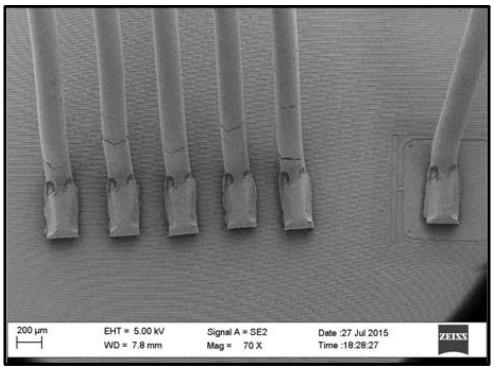

Fig. 3-12 Failure analysis of another tested module under the Condition 4.

There is no visible degradation in the diode D_{VL} as shown in Fig. 3-11. These results agree well with power cycling test result that V_{CE_ON} of T_{VL} is increased due to degradation. Fig. 3-12 shows another tested module under the Condition 4. There are cracks in all five bond wires of the IGBT.

In the case of the other tested modules under the Condition 1, the cracks are also observed in the bond wires of failed IGBTs.

Fig. 3-13 (a), (b) and (c) show SEM images of cross sectioned IGBTs before power cycling test and after the power cycling test under the Conditions 4 and 1, respectively. There is no visible degradation in chip solder joint compared with new one and no fracture in the interface between chip and bond-wire under the test Condition 4 as shown in Fig. 3-13 (b). In the case of the tested module under the Condition 1, there are also no degradation in chip solder joint compared with new one and no fracture in the interface between chip and bond-wire as shown in Fig. 3-13 (c). It is worth to note that the black spots in the solder and wire-bond shown in Fig. 3-13 are not the degradation due to power cycling test but remained material from the IGBT module such as epoxy.

It can be seen from the physics-of-failure analysis results that the bond-wire degradation is the predominant failure mechanism of this module. Further, there is no big difference in failure mechanism due to $t_{\Delta Tj}$ under the defined test conditions. However, the power cycling tests under more various temperature stress conditions with a number of samples per condition are still needed in order to investigate the effect of temperature stress conditions on the failure mechanisms with statistic results.

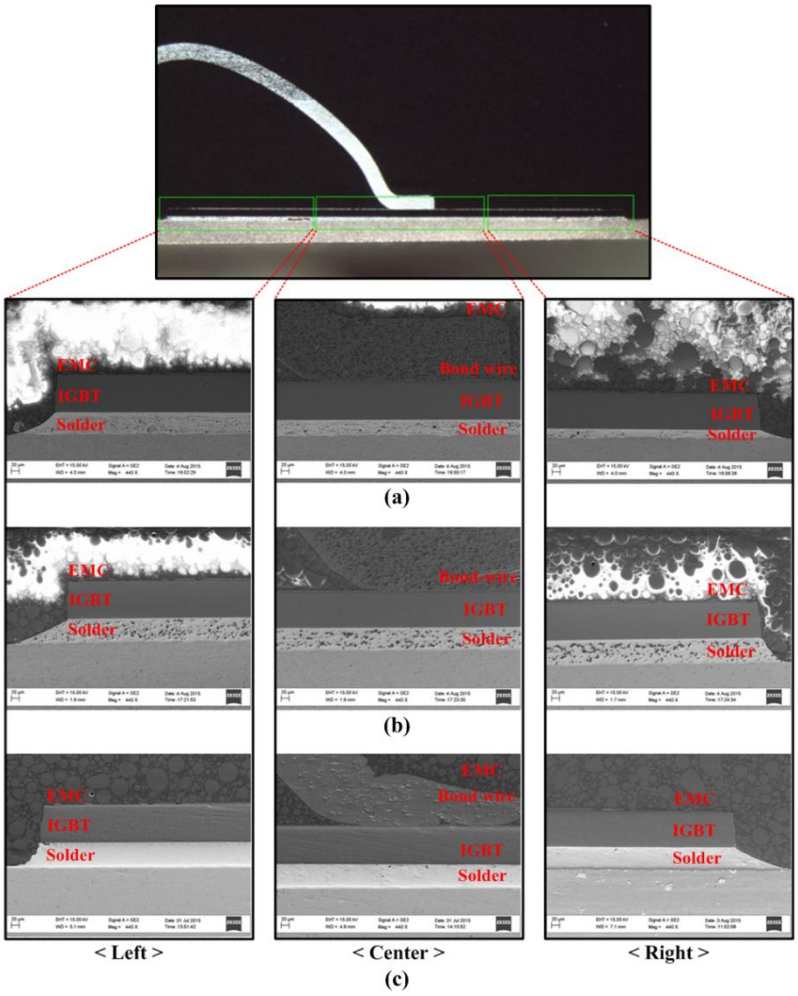

Fig. 3-13 SEM images of cross sectioned IGBTs for failure analysis (a) before power cycling test (b) after the power cycling test under the Condition 4 (1Hz) (c) after the power cycling test under the Condition 1 (0.1 Hz).

3.5. SUMMARY

An effect of the junction temperature swing duration ($t_{\Delta Tj}$) on the lifetime of an IGBT module has been investigated and its relevant lifetime factor has been modeled based on the test data. It can be seen from the result that $t_{\Delta Tj}$ has a significant effect on the lifetime and thus should be considered when lifetime models are developed and the lifetime of IGBT modules is estimated. Further, the junction temperature swing duration dependent lifetime factor is modeled based on a total of 38 accelerated power cycling test results under six different duration conditions. The different lifetime factor has been obtained for the specific type of IGBT modules under test with different lifetime definitions and confidence levels of a specific lifetime. The result shows the importance of the information about lifetime definition and confidence level for lifetime modeling. This study enables to include the junction temperature swing duration effect on IGBT modules for its lifetime estimation and it may result in improved lifetime prediction of IGBT modules under given mission profiles of converters.

Finally, the physics-of-failure analysis has been performed to investigate the failure mechanism of the tested device modules. The bond-wire cracks are observed in all tested modules and there are no visible degradation in the chip solder joint. Therefore, the bond-wire is the predominant failure mechanism in the tested modules under these conditions. However, the power cycling tests under more various temperature stress conditions with a number of samples per condition are still needed in order to investigate the effect of temperature stress conditions on the failure mechanisms with statistic results.

CHAPTER 4. OPEN-CIRCUIT FAULT DETECTION AND FAULT-TOLERANT CONTROL METHODS FOR A T-TYPE INVERTER

This chapter deals with the open-circuit fault detection and fault-tolerant control methods for a T-type three-level inverter to improve its reliability and general availability under open-circuit fault conditions. Experimental results verify the feasibility and effectiveness of the proposed open-circuit fault detection and fault-tolerant control methods.

4.1. NEUTRAL-POINT CLAMPED THREE-LEVEL INVERTERS

4.1.1. CONFIGURATION OF NEUTRAL-POINT CLAMPED THREE-LEVEL INVERTERS

Fig. 4-1 (a) shows the simplified circuit diagram of the 3-phase Neutral-Point Clamped (NPC) three-level inverter. The inverter leg is composed of four active switches (from $S_{x1(x=a,b,c)}$ to S_{x4}) like IGBT with four anti parallel diodes (from D_{x1} to D_{x4}). The DC-link capacitor is split into two capacitors for providing the neutral-point Z and it is connected with points between S_{x1} and S_{x2} and between S_{x3} and S_{x4} through clamping diodes D_{Cx1} and D_{Cx2}, respectively.

The NPC inverter is widely used in the medium-voltage range applications due to their advantages. Compared with conventional two-level inverter, it has lower *dv/dt* and reduced Total Harmonic Distortion (THD) in its output voltage. Therefore, the output filter size can be reduced. Furthermore, smaller capacity switches can be used because two active switches are connected in series to block the DC-link voltage [113].

The three-level inverters have also become promising topologies for low voltage applications because they can improve the efficiency compared with conventional two-level converters in certain switching frequency ranges [114]. Various three-level topologies have been suggested to achieve specific application requirements or to improve the system performances [114]-[116]. Recently, the T-type inverter has also been proposed to improve the efficiency in the medium switching frequency range [116].

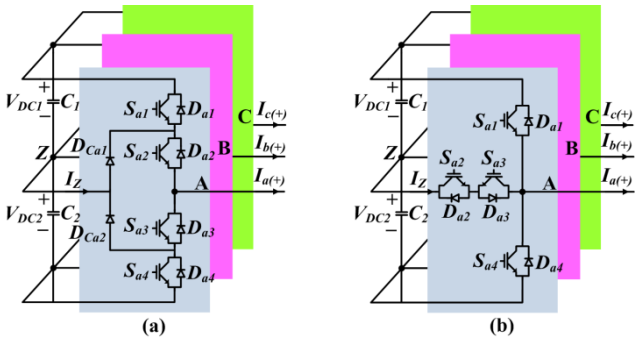

Fig. 4-1 Simplified circuit diagram of three-level neutral-point clamped inverters (a) NPC inverter (b) T-type inverter.

Fig. 4-1 (b) shows the simplified circuit diagram of the T-type inverter. In the half bridge (S_{x1} and S_{x4}), the T-type inverter uses the same switches as that used in conventional two-level inverters because these switches have to block the full DC-link voltage. A bidirectional switch is connected between the neutral-point and each output. Unlike half-bridge switches, bidirectional switches (S_{x2} and S_{x3}) have to block only half of the DC-link voltage. Therefore, it is possible to use devices having a lower voltage rating. On the contrary to the NPC inverter, the switches are not connected in series. Therefore, the conduction losses are considerably reduced. Further, due to the reduced blocking voltage, the neutral-switches have also lower switching losses. Therefore, the T-type inverter has the highest efficiency among the T-type, NPC, and conventional two-level inverter in the medium switching frequency (4~30 kHz) range [116].

4.1.2. DESCRIPTION OF NEUTRAL-POINT CLAMPED THREE-LEVEL INVERTERS

The operating status of each phase leg in three-level inverters can be represented by three switching states: [P], [O], and [N]. Switching state [P] indicates that the switches S_{x1} and S_{x2} are on and the output pole voltage which is the voltage of output with respect to the neutral-point Z is $+V_{DC}/2$. Switching state [O] means that the switches S_{x2} and S_{x3} are on and the output pole voltage is zero. Switching state [N] signifies that the switches S_{x3} and S_{x4} are on and the output pole voltage is $-V_{DC}/2$. Considering the three phases, the three-level inverters have 27 switching state combinations. These switching state combinations can be represented by space voltage vectors [117].

Fig. 4-2 shows the relationship between the switching state combination and the space voltage vector. Each space vector can be categorized into zero, small, medium, and large voltage vectors based on its magnitude.

Table 4-1 shows the space voltage vector, switching states and neutral-current of three-level inverters. The voltage vectors except for the large and zero voltage vectors affect the neutral-point voltage variation as shown in Fig. 4-3.

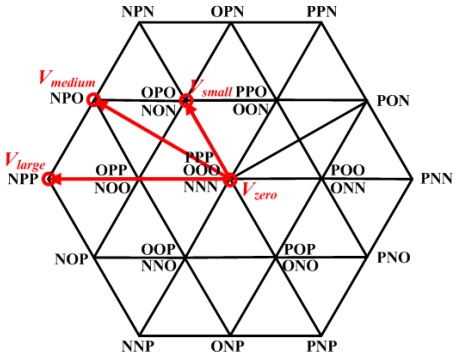

Fig. 4-2 Space vector diagram of three-level 3-phase inverter.

Table 4-1 Switching states, voltage vectors and neutral current for the three-level inverter.

Vector	**Magnitude**	**Switching State**		**Neutral Current**	
Zero vector	0	[PPP] [OOO] [NNN]		–	
Small vector	$\frac{1}{3}V_{dc}$	**P-type**	**N-type**	**P-type**	**N-type**
		[POO]	[ONN]	$I_b + I_c$	I_a
		[PPO]	[OON]	I_c	$I_a + I_b$
		[OPO]	[NON]	$I_a + I_c$	I_b
		[OPP]	[NOO]	I_a	$I_b + I_c$
		[POP]	[ONO]	I_b	$I_a + I_c$
		[OOP]	[NNO]	$I_a + I_b$	I_c
Medium vector	$\frac{\sqrt{3}}{3}V_{dc}$	[PON]		I_b	
		[OPN]		I_a	
		[NPO]		I_c	
		[NOP]		I_b	
		[ONP]		I_a	
		[PNO]		I_c	
Large vector	$\frac{2}{3}V_{dc}$	[PNN]		–	
		[PPN]		–	
		[NPN]		–	
		[NPP]		–	
		[NNP]		–	
		[PNP]		–	

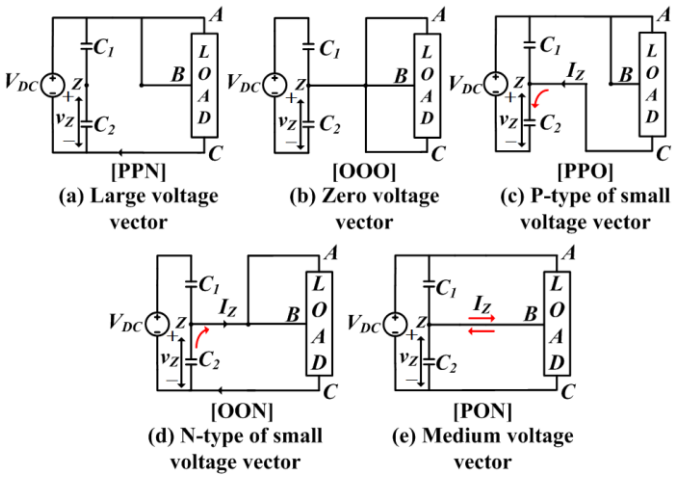

Fig. 4-3 Effect of voltage vectors on the neutral-point voltage variation.

Large voltage vectors do not affect the neutral-point voltage variation because the neutral-point *Z* is left unconnected as shown in Fig. 4-3 (a) and thus the neutral current I_Z is zero. Zero voltage vectors also do not affect the neutral-point voltage variation. Although, the switching state [OOO] of zero voltage vectors is connected to the neutral-point *Z* as shown in Fig. 4-3 (b), the total sum of three phase currents is zero in this case. Therefore, it does not affect the neutral-point variation. Fig. 4-3 (c) shows the inverter operation with the P-type switching state [POO] of the small voltage vectors. Because the P-type switching states are connected between the positive DC-link and neutral-point *Z*, the neutral current flows into the neutral-point *Z* and thus the neutral-point voltage is increased. On the other hand, the N-type switching states of small voltage vectors decrease the neutral-point voltage since the three phases are connected between the neutral-point and the negative DC-link as shown in Fig. 4-3 (d). Medium voltage vectors also affect the neutral-point voltage. Depending on the current direction of the phase connected to the neutral-point, the neutral-point voltage increases or decreases as shown in Fig. 4-3 (e) [117].

4.2. OPERATION OF T-TYPE INVERTER UNDER OPEN-CIRCUIT FAULT CONDITIONS

In this section, the operation of the T-type inverter under open-circuit fault conditions is analyzed considering the open-circuit fault in phase-A. The analysis is performed under the assumption that the inverter is in normal operating mode that the power is delivered from the inverter to loads. The positive current direction is defined as flowing out from the inverter to loads.

Open-circuit fault in S_{a1}

Under normal conditions, if the switching state is [P] and the phase current is positive, the phase current flows through the switch S_{a1} and the pole voltage becomes $+V_{DC}/2$.

If the open-fault occurs in the switch S_{a1}, the current flows through the switch S_{a2} and the diode D_{a3} instead of S_{a1} while the switching state is [P] and the phase current is positive. The phase output is connected to the neutral-point Z instead of the positive DC bus as shown in Fig 4-4 (a). The blue line indicates the current path under the normal condition and the red line denotes the current path under the fault condition. Therefore, the output-pole voltage becomes zero instead of $+V_{DC}/2$. This undesirable output pole voltage causes the distortion of the output phase currents, especially the positive current of faulty phase-A. In this instance, the switching states of P-type small voltage vectors [PPO], [POO], [POP], the switching states of medium vectors [PON], [PNO] and the switching states of large voltage vectors [PNN], [PPN] [PNP] are impossible because the switching state [P] is impossible in faulty phase-A. Some of the P-type switching states of small voltage vectors and switching states of medium voltage vectors are changed to N-type switching states. On the contrary, other switching states which contain the switching state [O] or [N] in faulty phase-A are possible. Therefore, the upper capacitor voltage V_{DC1} becomes larger than the lower capacitor voltage V_{DC2}.

Fig. 4-5 (a) shows the output phase current, pole voltage of phase-A and two capacitor voltages under the S_{a1} fault condition.

Open-circuit fault in S_{a2}

In the case of the S_{a2} fault, the current flows through the diode D_{a4} instead of S_{a2} and D_{a3} if the switching state is [O] and the phase current is positive. The pole voltage becomes $-V_{DC}/2$ instead of zero because the phase output is connected to the negative DC bus as shown in Fig 4-4 (b). The output currents are also distorted by the changed pole voltage.

When the open-circuit fault occurs in the switch S_{x2}, the switching state [O] in the faulty phase is impossible and this state is replaced by the switching state [N] if the current is positive. In the faulty phase-A case, the switching states [ONN], [OON], [ONO], [OPN], and [ONP] are impossible. These switching states are changed to the switching states, which includes [N] state in the faulty phase-A. Some of the N-type switching states of the small voltage vectors and the switching states of the medium voltage vector are changed to the switching states of the large vectors. The amount of the neutral-current flowing out from the neutral-point is smaller than under the normal condition. Therefore, the lower capacitor voltage V_{DC2} is higher than the upper capacitor voltage V_{DC1} as shown in Fig. 4-5 (b).

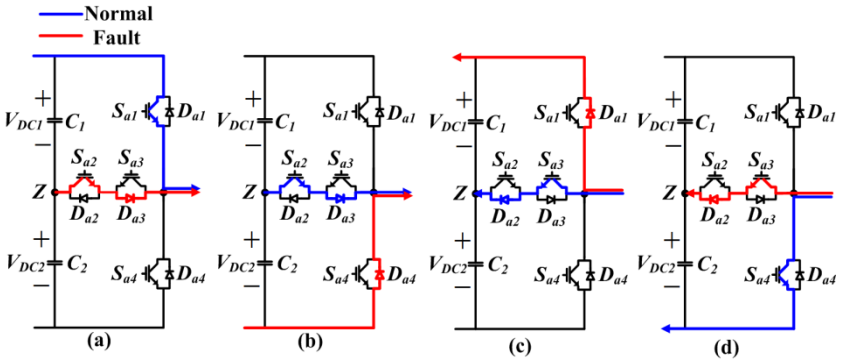

Fig. 4-4 Current paths (a) under normal and S_{a1} open-circuit fault condition when $I_a > 0$ with [P] (b) under normal and S_{a2} fault condition when $I_a > 0$ with [O] (c) under normal and S_{a3} fault condition when $I_a < 0$ with [O] (d) under normal and S_{a4} fault condition when $I_a < 0$ with [N].

Open-circuit fault in S_{a3}

If the open-circuit fault occurs in S_{a3}, the output pole voltage becomes $+V_{DC}/2$ instead of zero as shown in Fig. 4-4 (c) when the switching state is [O] and the phase current is negative.

In this case, the switching states [OPO], [OPP], [OOP], [OPN], and [ONP] are impossible. On the other hand, all N-type switching states and the medium switching states [OPN] and [ONP] are possible. Therefore, the upper capacitor voltage V_{DC1} is larger than the lower capacitor voltage V_{DC2}. The output phase currents, the pole voltage of phase-A and the two capacitor voltages under the S_{a3} faulty condition are shown in Fig. 4-5 (c).

Open-circuit fault in S_{a4}

If the current is negative during the switching state [N], the current flows through S_{a4} under the normal condition. However, if the open-circuit fault occurs in S_{a4}, the current flows through S_{a3} and D_{a2} and the pole voltage becomes zero rather than $-V_{DC}/2$ as shown in Fig. 4-4 (d). In this case, the switching states [NON], [NOO], [NNO], [NPO], [NOP], [NPN], [NPP] and [NNP] are impossible and these states are replaced with the switching states which contain the switching state [O] instead of [N] in the faulty phase-A. For example, the switching state [NPP] is replaced with the switching state [OPP]. The amount of the phase current which flows into the neutral-point is larger than the amount of the phase current which flows out from the neutral-point. Therefore, the lower capacitor voltage V_{DC2} becomes larger than the upper capacitor voltage as shown in Fig. 4-5 (d).

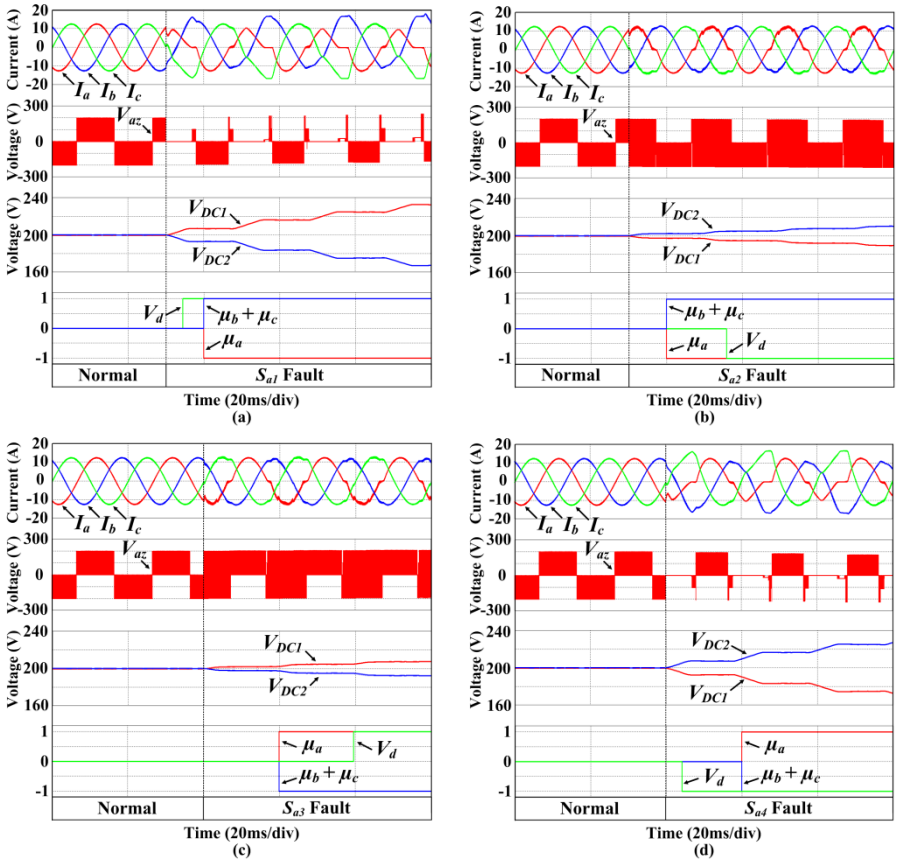

Fig 4-5 Phase currents, pole voltage and two capacitor voltages under (a) S_{a1} open-circuit fault (b) S_{a2} open-circuit fault (c) S_{a3} open-circuit fault (d) S_{a4} open-circuit fault conditions.

4.3. OPEN-CIRCUIT FAULT DETECTION METHOD

The phase currents are distorted and two capacitor voltages are unbalanced under the open-circuit fault conditions as shown in the previous analysis in Chapter 4.2.1. By these characteristics, the faulty switch can be identified. The proposed fault detection method is explained considering the open-circuit faults in phase-A.

The average value during one fundamental period of the phase current is defined by $I_{x\_ave(x=a,b,c)}$. Under the normal operating condition, the average of each phase current is zero. However, in the faulty cases, the output currents are distorted and the average of each phase current also has the different polarities according to faulty switches. If the open-switch fault occurs in the switch S_{a1} or switch S_{a2}, I_{a_ave} has the

negative value because the positive current of the phase-A is distorted. The total amount of the average values of the phase-A is the same with the summation of the average values of the other two phases if it is a three-phase balanced system. Thus, $I_{a\_ave} = -(I_{b\_ave} + I_{c\_ave})$. On the contrary, if the open-circuit fault occurs in S_{a3} or S_{a4}, I_{a_ave} has the positive value and the summation of the average values of the other two phases has a negative value. Therefore, using the polarities of I_{a_ave} and $I_{b\_ave} + I_{c\_ave}$, it is possible to identify whether the open-circuit fault occurs between S_{a1} and S_{a2} or between S_{a3} and S_{a4}. However, this direct average current method tends to be highly unreliable under varying operating conditions, especially during fast transient conditions, and may lead to a wrong diagnosis. Further, it is difficult to set the threshold value as a constant because it depends on the variations of the output currents. To improve the accuracy and set the threshold value as a constant, the normalized phase currents are used for the fault detection. The phase currents can be normalized as given below [118, 119]

$$|I_s| = \sqrt{(I_{ds})^2 + (I_{qs})^2} \tag{4.1}$$

$$I_{x\_N} = \frac{I_{x\,(x=a,b,c)}}{|I_s|} \times |I_{rated}| \tag{4.2}$$

where I_{ds} and I_{qs} are d- and q-axis currents in a stationary reference frame, respectively, I_{rated} is a magnitude of the rated current of a system and I_{x_N} is the normalized phase current.

The two capacitor voltages have also different characteristics according to the faulty switch. In the case of S_{a1} or S_{a3} fault, V_{DC1} becomes larger than V_{DC2}. Reversely, if the open-circuit fault occurs in S_{a2} or S_{a4}, V_{DC2} becomes larger than V_{DC1} as mentioned before. Therefore, the faulty switch can be identified by the characteristics of the current distortions and two capacitor voltages. The procedure of the proposed fault diagnosis method is as follows:

1) Calculate the average of each the normalized phase current (I_{xN_avg}) and check the polarity of the average value.

2) Identify whether the open-switch faults occurs in one of the two switches (S_{a1}, S_{a2}) or one of the two switches (S_{a3}, S_{a4}) using the polarities of the average current value.

3) Identify the location of the faulty switch between S_{a1} and S_{a2} or between S_{a3} and S_{a4}, using the change of the two capacitor voltages.

To improve the accuracy, the threshold values I_{thr} and V_{thr} are set. The diagnosis variables μ_x and V_d are defined by the following conditions:

$$\begin{aligned} I_{xN\_avg} > I_{thr} &\quad : \mu_x = 1 \\ I_{xN\_avg} < -I_{thr} &\quad : \mu_x = -1 \\ -I_{thr} < I_{xN\_avg} < I_{thr} &\quad : \mu_x = 0 \end{aligned} \qquad (4.3)$$

$$\begin{aligned} V_{DC1} - V_{DC2} > V_{thr} &\quad : V_d = 1 \\ V_{DC1} - V_{DC2} < -V_{thr} &\quad : V_d = -1 \\ -V_{thr} < V_{DC1} - V_{DC2} < V_{thr} &\quad : V_d = 0 \end{aligned}$$

where I_{xN_avg} is the average value of the normalized phase current, V_{DC1} and V_{DC2} are upper and lower capacitor voltages, respectively, I_{thr} is threshold value for the average value of the current and V_{thr} is threshold value for the voltage difference.

Table 4.2 shows the diagnosis variables for the faulty switch identification.

Fig. 4-5 shows the change of the diagnosis variables according to the faulty switch in phase-A.

Table 4-2 Values of diagnosis variables according to the faulty switch

	Diagnosis Variables						
Faulty Switch	μ_a	$\mu_b + \mu_c$	μ_b	$\mu_a + \mu_c$	μ_c	$\mu_a + \mu_b$	V_d
No fault	0	0	0	0	0	0	0
S_{a1}	-1	+1	-	-	-	-	+1
S_{a2}	-1	+1	-	-	-	-	-1
S_{a3}	+1	-1	-	-	-	-	+1
S_{a4}	+1	-1	-	-	-	-	-1
S_{b1}	-	-	-1	+1	-	-	+1
S_{b2}	-	-	-1	+1	-	-	-1
S_{b3}	-	-	+1	-1	-	-	+1
S_{b4}	-	-	+1	-1	-	-	-1
S_{c1}	-	-	-	-	-1	+1	+1
S_{c2}	-	-	-	-	-1	+1	-1
S_{c3}					+1	-1	+1
S_{c4}					+1	-1	-1

4.4. OPEN-CIRCUIT FAULT-TOLERANT CONTROL STRATEGY

In this section, a fault-tolerant control method for the open-circuit fault in half-bridge switches (S_{x1}, S_{x4}) is explained first and then the two fault-tolerant methods for the neutral-point switches (S_{x2}, S_{x3}) are explained. The fault in phase-A is considered for the case studies.

4.4.1. FAULT OCCURS IN THE HALF-BRIDGE SWITCH (S_{X1} OR S_{X4})

If the open-circuit fault occurs in the half-bridge switches, the output phase currents are considerably distorted and the neutral-point voltage is unbalanced as mentioned above. This is because it is impossible to generate the large and the medium voltage vectors which contain the switching state states [P] or [N] in the faulty phase. The S_{a1} fault for example, the large voltage vectors [PNN], [PNP], [PPN] and the medium voltage vectors [PNO], [PON] are impossible. To generate the output without theses vectors, the modulation index should be reduced so that the reference voltage is in inner hexagon as shown in Fig. 4-6. By the proposed fault-tolerant method, the inverter can be operated without output distortions and with reduced power at reduced output voltage. In other words, it means that the proposed fault-tolerant method for half-bridge switch fault cannot be used for the applications with fixed output voltage such as grid-connected inverter.

Although the modulation index is reduced, the output is still distorted because there are impossible P-type switching states [PPO], [POO] and [POP] of the small voltage vectors. These switching states should be replaced with N-type switching states that indicate the same small voltage vectors. This change is simply achieved by adding the shortest turn-on time (T_{short}) to three phase turn-on times (T_a, T_b, T_c). The turn-on time is a time that the switching state of each phase is changed from the current state to another state, T_{short} is the shortest turn-on time among T_a, T_b and T_c and T_{sw} is a switching period.

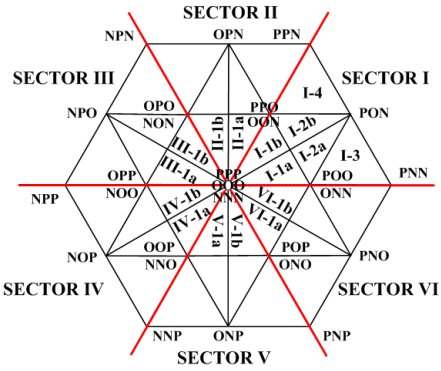

Fig. 4-6 Space vector diagram for fault-tolerant control when open-circuit fault occurs in half bridge switch (S_{x1} or S_{x4}).

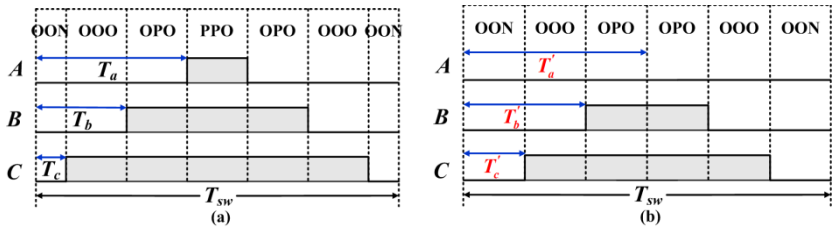

Fig. 4-7 The switching sequence in sector II-1a (a) under normal conditions (b) for fault-tolerant operation.

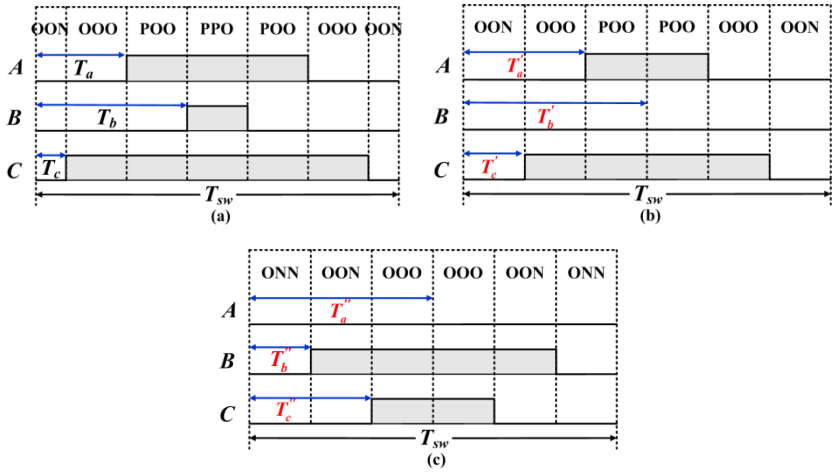

Fig. 4-8 The switching sequence in sector I-1b (a) under normal conditions (b) after T_{short} is added (c) after rearrangement.

Fig. 4-7 (a) shows the switching sequence when the reference voltage is in sector II-1a. After T_{short} is added, the P-type switching state [PPO] is replaced with the N-type switching state [OON] as shown in Fig. 4-7 (b). In this sequence, T_{short} is T_a. This change does not affect the output because the small switching states [OON] and [PPO] generate the same line-to-line AC output voltage. In the case of open-circuit fault in S_{a1}, T_{short} should be added to T_a, T_b and T_c in sectors I, II-1a, V-1b and VI, respectively.

However, in the sectors I-1b and VI-1b, the impossible switching state [POO] is still remained after T_{short} is added. This switching state should be replaced to [ONN]. In the sector I-1b, the switching sequence is [OON]-[OOO]-[POO]-[PPO]-[POO]-[OOO]-[OON] as shown in Fig. 4-8 (a). After T_{short} is added, the switching state [PPO] is changed to [OON] and the switching sequence is formed as [OON]-

[OOO]-[POO]-[OOO]-[OON] as shown in Fig. 4-8 (b). The remained impossible switching state [POO] should be replaced to [ONN] and the switching sequence should be rearranged as [ONN]-[OON]-[OOO]-[OON]-[ONN] to eliminate the output distortion and to minimize the number of switching as shown in Fig. 4-8 (c).

The replacement of the switching state and the rearrangement of the switching sequence are easily achieved by redefining three phase turn-on times (T_a, T_b, T_c). In the sector I-1b, dwell times of the switching states (T_{dwell}) after T_{short} is added can be expressed as

$$\begin{aligned} T_{dwell[OON]} &= 2(T_c + T_{short}) \\ T_{dwell[OOO]} &= 2(T_a - T_c) \\ T_{dwell[POO]} &= T_{dwell[ONN]} = 2(T_b - T_a) \end{aligned} \tag{4.4}$$

where T_{short} is T_c.

Using the dwell time of each switching state, the turn-on times for rearrangement are redefined as (4.5)

$$\begin{aligned} T_a^{"} &= T_{sw}/2 \\ T_b^{"} &= \frac{1}{2}T_{dwell[ONN]} = T_b - T_a \\ T_c^{"} &= \frac{1}{2}(T_{dwell[ONN]} + T_{dwell[OON]}) = 2T_c + T_b - T_a \end{aligned} \tag{4.5}$$

All impossible P-type switching states in the sectors I, II-1a, V-1b and VI are substituted to the N-type switching states for the fault-tolerant control. However, it means that the dwell times between N-type switching states and P-type switching states are not equal during the fundamental period. It makes the average of the neutral-current to be non-zero. Consequently, it causes the unbalance of two DC-link capacitor voltages. The P-type switching states increase the lower capacitor voltages and decrease the upper capacitor voltage. On the contrary, the N-type switching states decrease the lower capacitor voltage and increase the upper capacitor voltage. Therefore, the total dwell times of the P-type and N-type switching states during fundamental period should be equal so that the average of the neutral-current is zero resulting in balance of the two capacitor voltages. To make the neutral-current to be zero, the N-type switching states in the opposite sectors should be replaced with P-type switching states in their switching sequences.

The S_{a1} fault for instance, the P-type switching states in the sectors I, II-1a, V-1b and VI are replaced by the N-type switching states. Therefore, the N-type switching states in the opposite sectors II-1b, III, IV, and V-1a should be replaced with the P-

type switching states. The replacement of the N-type switching states with P-type switching states is easily implemented by subtracting T_{short} to T_a, T_b and T_c. After T_{short} is subtracted, the remained N-type switching states can be replaced and the switching sequences can also simply be rearranged by applying the above explained principle. The N-type switching state [NOO] is remained in the sectors III-1a and IV-1b. Therefore, [NOO] should be replaced with [OPP] and the switching sequences should be rearranged as [NPO]-[OPO]-[OPP]-[OPO]-[NPO] and [NOP]-[OOP]-[OPP]-[OOP]-[NOP] in the sectors III-1a and IV-1b, respectively.

The change of the switching states according to the faulty switch is arranged in Table 4-3. The procedure of the fault-tolerant control strategy for the S_{a4} fault is the same with that of the S_{a1} fault. Therefore, the redefined turn-on times for both S_{a1} and S_{a4} open-circuit faults are the same.

The redefined turn-on times for the fault-tolerant control, when the open-circuit fault occurs in the half-bridge switches of phase-A are arranged in Table 4-4. The redefined turn-on times for the fault-tolerant control of the other phases can be obtained using the same principle as explained above.

Table 4-3 Change of switching states according to fault switches (S_{x1}, S_{x4}).

<table>
<tr><td></td><td colspan="3">Faulty switch</td></tr>
<tr><td>Sector</td><td>Phase-A (S_{a1}, S_{a4})</td><td>Phase-B (S_{b1}, S_{b4})</td><td>Phase-C (S_{c1}, S_{c4})</td></tr>
<tr><td>I-1a</td><td rowspan="3">P ⇒ N</td><td>N ⇒ P</td><td rowspan="4">N ⇒ P</td></tr>
<tr><td>I-1b</td><td rowspan="5">P ⇒ N</td></tr>
<tr><td>II-1a</td></tr>
<tr><td>II-1b</td><td rowspan="6">N ⇒ P</td></tr>
<tr><td>III-1a</td></tr>
<tr><td>III-1b</td><td rowspan="5">P ⇒ N</td></tr>
<tr><td>IV-1a</td></tr>
<tr><td>IV-1b</td><td rowspan="4">N ⇒ P</td></tr>
<tr><td>V-1a</td></tr>
<tr><td>V-1b</td><td rowspan="3">P ⇒ N</td></tr>
<tr><td>VI-1a</td></tr>
<tr><td>VI-1b</td><td>N ⇒ P</td></tr>
</table>

P : P-type switching state of small voltage vectors

N : N-type switching state of small voltage vectors

Table 4-4 Redefined turn-on times for tolerant-control of switch S_{a1} or S_{a4} fault.

Sector	Turn-on times	Sector	Turn-on times	Sector	Turn-on times
I-1a	$T_a^{'} = T_a + T_{short}$ $T_b^{'} = T_b + T_{short}$ $T_c^{'} = T_c + T_{short}$	IV-1a	$T_a^{'} = T_a - T_{short}$ $T_b^{'} = T_b - T_{short}$ $T_c^{'} = T_c - T_{short}$	V-1a	$T_a^{'} = T_a - T_{short}$ $T_b^{'} = T_b - T_{short}$ $T_c^{'} = T_c - T_{short}$
I-1b	$T_a^{'} = T_s/2$ $T_b^{'} = T_b - T_a$ $T_c^{'} = 2T_c + T_b - T_a$	IV-1b	$T_a^{'} = T_s/2$ $T_b^{'} = T_s/2 + T_b - T_a$ $T_c^{'} = T_c - T_a$	V-1b	$T_a^{'} = T_a + T_{short}$ $T_b^{'} = T_b + T_{short}$ $T_c^{'} = T_c + T_{short}$
II-1a	$T_a^{'} = T_a + T_{short}$ $T_b^{'} = T_b + T_{short}$ $T_c^{'} = T_c + T_{short}$	III-1a	$T_a^{'} = T_s/2$ $T_b^{'} = T_b - T_a$ $T_c^{'} = T_s/2 - T_a + T_c$	VI-1a	$T_a^{'} = T_s/2$ $T_b^{'} = T_c + 2T_b - T_a$ $T_c^{'} = T_c - T_a$
II-1b	$T_a^{'} = T_a - T_{short}$ $T_b^{'} = T_b - T_{short}$ $T_c^{'} = T_c - T_{short}$	III-1b	$T_a^{'} = T_a - T_{short}$ $T_b^{'} = T_b - T_{short}$ $T_c^{'} = T_c - T_{short}$	VI-1b	$T_a^{'} = T_a + T_{short}$ $T_b^{'} = T_b + T_{short}$ $T_c^{'} = T_c + T_{short}$

4.4.2. FAULT OCCURS IN THE NEUTRAL-POINT SWITCH (S_{X2} OR S_{X3})

Two fault-tolerant control methods will be presented in the case of the neutral-point switch fault.

Method #1: Two-Level Switching Method (TLSM)

If the open-circuit fault occurs in S_{x2} or S_{x3}, the switching state [O] in the faulty phase is impossible. Therefore, if a reference voltage of the faulty phase is made using voltage vectors, which do not contain the switching state [O] in the faulty phase, the distortion of the outputs can be eliminated.

The proposed fault-tolerant control is simple. In a conventional SVM approach for three-level inverters, the positive output voltage is generated using the switching states [P] and [O], and the negative output voltage is generated using the switching states [O] and [N]. In the proposed method, the reference voltage of the faulty phase is made using [P] and [N] as in the case of the 2-level inverter. This method can easily be implemented by adding an offset time (T_{offset}) to the turn-on time of the faulty phase [120]. T_{offset} is defined as follows

$$\begin{aligned} T_{offset} &= -\frac{1}{2}T_x && (V_x^* > 0) \\ T_{offset} &= -\frac{1}{2}T_x + \frac{1}{4}T_{sw} && (V_x^* < 0) \end{aligned} \tag{4.6}$$

where V_x^* is the reference voltage of the faulty phase and T_{sw} is the switching period. Assuming that the open-circuit fault occurs in S_{a2} or S_{a3}, the turn-on time T_a is redefined as given below

$$\begin{aligned} T_a^{'} &= \frac{1}{2}T_a && (V_a^* > 0) \\ T_a^{'} &= \frac{1}{2}(T_a + \frac{1}{2}T_{sw}) && (V_a^* < 0) \end{aligned} \tag{4.7}$$

The reference voltage of the phase-A is made by the turn-on time $T_a^{'}$. S_{a1} is turned-on using the redefined turn-on time $T_a^{'}$ and S_{a4} is complementarily operated with S_{a1}.

Method #2: Hybrid Discontinuous Switching Method (HDSM)

As explained above, if the open-circuit fault occurs in the neutral-point switches, the switching state [O] is impossible in the faulty phase according to output current directions. It means that there are problems to make zero, small and medium voltage vectors which contains [O] in the faulty leg. If the open-circuit fault occurs in S_{a2}, it is impossible to generate the switching states of the small voltage vectors [OON], [ONN], [ONO] and the switching states of the medium voltage vectors [OPN], [ONP] when I_a is positive. The impossible switching states should be replaced with other switching states to generate the output without distortion. The impossible N-type switching states [OON], [ONN] and [ONO] can simply be replaced with the P-type switching states [PPO], [POO] and [POP] by subtracting T_{short} to the turn-on times of the three phases (T_a, T_b, T_c).

If the reference voltage is in the sector I-3 (See Fig. 4-6), the switching sequence is developed as [ONN]-[PNN]-[PON]-[POO]-[PON]-[PPN]-[ONN] as shown in Fig. 4-9 (a). Fig. 4-9 (b) shows the switching sequence after T_{short} is subtracted to the three-phase turn on times. The switching sequence is formed as [PNN]-[PON]-[POO]-[PON]-[PNN]. The switching state [ONN] is replaced with [POO] and the dwell time of [POO] becomes double.

The turn-on times for the fault-tolerant control is simply redefined as

$$\begin{aligned} T_a^{'} &= T_a - T_{short} \\ T_b^{'} &= T_b - T_{short} \\ T_c^{'} &= T_c - T_{short} \end{aligned} \tag{4.8}$$

where $T_{short} = T_a$.

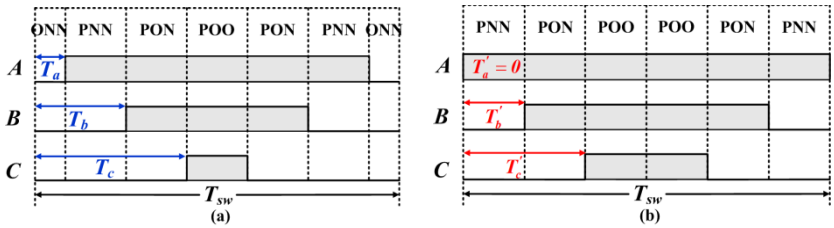

Fig. 4-9 The switching sequence in sector I-3 (a) under normal conditions (b) for the fault-tolerant operation.

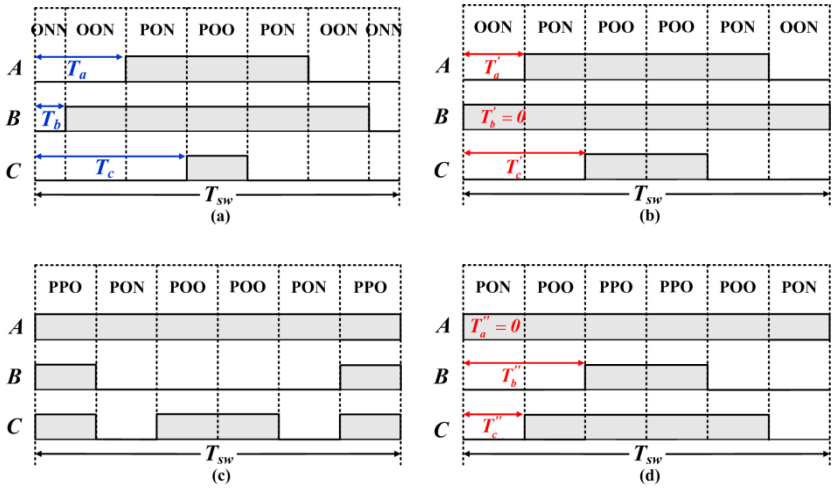

Fig. 4-10 The switching sequence in region 3-a of sector I for fault tolerant control (a) under normal conditions (b) after T_{short} is subtracted (c) before rearrangement (d) after rearrangement

.

If there is only one N-type switching state in the switching sequence, the impossible N-type switching state can be replaced by subtracting T_{short}. However, if there are two impossible N-type switching states in the switching sequence, it is impossible to get the switching sequence for the fault-tolerant control by only subtracting T_{short}. If the reference voltage is in sector I-2a, the switching sequence is formed as [ONN]-[OON]-[PON]-[POO]-[PON]-[OON]-[ONN] as shown in Fig. 4-10 (a). Fig. 4-10 (b) shows the switching sequence after T_{short} is subtracted to replace the N-type switching state [ONN] with [POO]. There is still impossible N-type switching state [OON] and it also should be substituted to the P-type switching state [PPO] as shown in Fig. 4-10 (c). In this switching sequence, phase-C changes its switching state twice. To reduce the number of switching, the switching sequence should be rearranged as [OON]-[PON]-[POO]-[PON]-[OON] as shown in Fig. 4-10 (d).

In order to rearrange the switching sequence, the dwell time of each switching state should be obtained.

The dwell time (T_{dwell}) can be expressed by the turn-on times as

$$\begin{aligned} T_{dwell[OON]} &= 2(T_a - T_b) \\ T_{dwell[PON]} &= 2(T_c - T_a) \\ T_{dwell[POO]} &= 2(T_{sw}/2 - T_c + T_b) = 4T_b \end{aligned} \tag{4.9}$$

From the dwell time of each switching state, the redefined turn-on times ($T_a^{"}, T_b^{"}, T_c^{"}$) for the switching sequence rearrangement are obtained as

$$\begin{aligned} T_a^{"} &= 0 \\ T_b^{"} &= \frac{1}{2}(T_{dwell[PON]} + T_{dwell[POO]}) = 2T_b + T_c - T_a \\ T_c^{"} &= \frac{1}{2}T_{dwell[PON]} = T_c - T_a \end{aligned} \tag{4.10}$$

All impossible N-type switching states in the sectors I and IV should be substituted to the P-type switching states for the fault-tolerant control. To make the neutral-current to be zero, the P-type switching states in the sectors III and IV should be replaced with the N-type switching states in their switching sequences. It can be achieved by adding T_{short} to the turn-on times. In the regions that have two P-type switching states, all P-type switching states should be replaced to the N-type switching states and the switching sequence should also be rearranged as explained above.

The impossible switching states of the small voltage vectors can be replaced with the other type of switching states. However, in the case of medium voltage vectors, there are no possibilities to replace the switching state with another one which indicate the same voltage vector. Therefore, the new switching sequence should be applied in the regions that have the impossible medium voltage vectors. In the case of the open-circuit fault in S_{a2}, the medium switching states [OPN] in sector II and [ONP] in sector V are impossible. The new switching sequence without these switching states can be achieved by applying the Two-Level Switching Method (TLSM) in the sectors II and V and the turn-on time $T_a^{'}$ is redefined as (4.7)

S_{a1} is turned on by the redefined turn-on time $T_a^{'}$ and S_{a4} is operated complementarily with S_{a1}.

The proposed fault-tolerant control for the neutral-point switch is arranged in Table 4-5. The redefined turn-on times in the sectors I and II for the tolerant-control of the S_{a2} or S_{a3} fault are also arranged in Table 4-6.

Fig. 4-11 shows the flow chart of the proposed open-circuit fault detection and fault-tolerant control methods considering the faults in the phase-A.

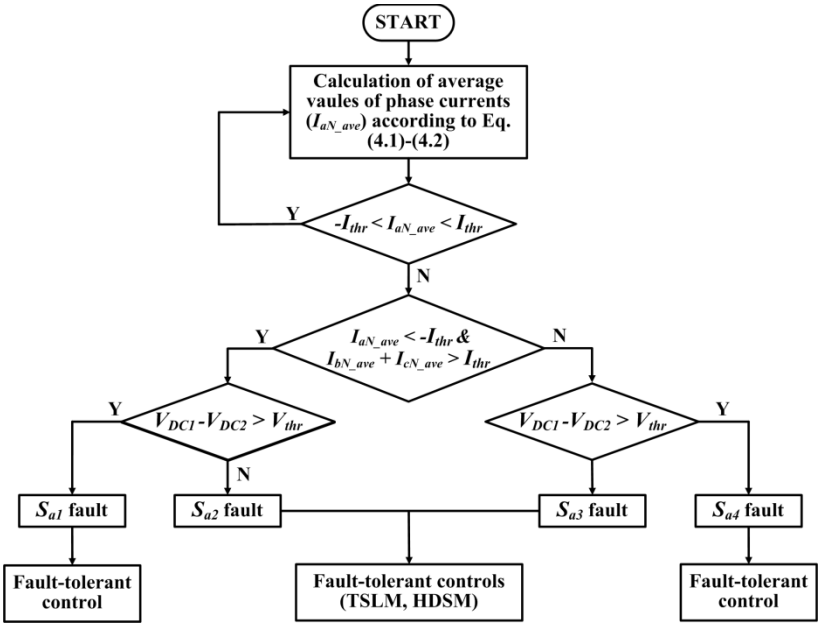

Fig. 4-11 Flow chart of the proposed open-circuit fault detection and fault-tolerant control method for T-type inverter considering the faults in phase-A.

Table 4-5 Fault-tolerant control HDSM for the open-circuit fault in the neutral-point switches.

	Faulty switch		
Sector	**Phase-A (S_{a2}, S_{a3})**	**Phase-B (S_{b2}, S_{b3})**	**Phase-C (S_{c2}, S_{c3})**
I	[OOO] ⇒ [PPP] N ⇒ P	TLSM	[OOO] ⇒ [NNN] P ⇒ N
II	TLSM	[OOO] ⇒ [PPP] N ⇒ P	[OOO] ⇒ [NNN] P ⇒ N
III	[OOO] ⇒ [NNN] P ⇒ N	[OOO] ⇒ [PPP] N ⇒ P	TLSM
IV	[OOO] ⇒ [NNN] P ⇒ N	TLSM	[OOO] ⇒ [PPP] N ⇒ P
V	TLSM	[OOO] ⇒ [NNN] P ⇒ N	[OOO] ⇒ [PPP] N ⇒ P
VI	[OOO] ⇒ [PPP] N ⇒ P	[OOO] ⇒ [NNN] P ⇒ N	TLSM

P : P-type switching state of small voltage vector

N : N-type switching state of small voltage vector

TLSM : Two-Level Switching Method

Table 4-6 Redefined turn-on times in sector I and II for tolerant-control, when the open-circuit fault occurs in S_{a2} or S_{a3}.

Sector	Turn-on times	Sector	Turn-on times	Sector	Turn-on times
I-1a	$T_a^{'}=0$ $T_b^{'}=2T_b$ $T_c^{'}=T_b+T_c$	I-3	$T_a^{'}=T_a-T_{short}$ $T_b^{'}=T_b-T_{short}$ $T_c^{'}=T_c-T_{short}$	II-2a	$T_a^{'}=\frac{1}{2}T_a$ $T_b^{'}=T_b$ $T_c^{'}=T_c$
I-1b	$T_a^{'}=0$ $T_b^{'}=T_b-T_a$ $T_c^{'}=T_b-T_a+2T_c$	I-4	$T_a^{'}=T_a-T_{short}$ $T_b^{'}=T_b-T_{short}$ $T_c^{'}=T_c-T_{short}$	II-2b	$T_a^{'}=\frac{1}{2}(T_a+\frac{1}{2}T_{sw})$ $T_b^{'}=T_b$ $T_c^{'}=T_c$
I-2a	$T_a^{'}=0$ $T_b^{'}=T_c-T_a+2T_b$ $T_c^{'}=T_c-T_a$	II-1a	$T_a^{'}=\frac{1}{2}T_a$ $T_b^{'}=T_b$ $T_c^{'}=T_c$	II-3	$T_a^{'}=\frac{1}{2}T_a$ $T_b^{'}=T_b$ $T_c^{'}=T_c$
I-2b	$T_a^{'}=T_a-T_{short}$ $T_b^{'}=T_b-T_{short}$ $T_c^{'}=T_c-T_{short}$	II-1b	$T_a^{'}=\frac{1}{2}(T_a+\frac{1}{2}T_{sw})$ $T_b^{'}=T_b$ $T_c^{'}=T_c$	II-4	$T_a^{'}=\frac{1}{2}(T_a+\frac{1}{2}T_{sw})$ $T_b^{'}=T_b$ $T_c^{'}=T_c$

4.5. EXPERIMENTAL RESULTS

Experiments have been carried out to verify the validity and effectiveness of the proposed fault detection and fault-tolerant control methods. A prototype of the T-type three-level inverter system has been built and used for the experiments as shown in Fig. 4-12. The parameters for the experiments are shown in Table 4-7.

Table 4-7 Parameters for the experiments of T-type inverter.

Parameter	Value
DC-link voltage	*150 V (200 V for Fig.4-16)*
Switching frequency	*10 kHz*
Control period	*100 μs*
Output frequency	*60 Hz*
Loads	*L: 10 mH, R: 10 Ω*
I_{thr}, V_{thr}	*0.08 A, 10 V*

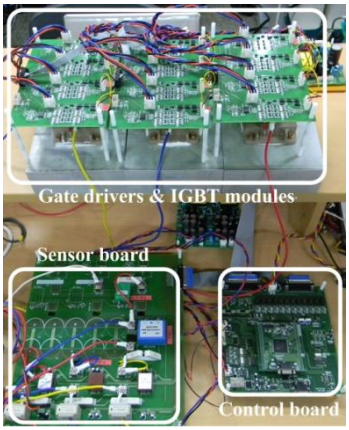

Fig. 4-12 Prototype of the T-type three-level inverter system.

Fig. 4-13 shows a comparison of the outputs of the T-type inverter between normal condition and different open-circuit fault conditions. Fig. 4-13 (a) shows the outputs under the normal condition. The current is sinusoidal and output pole voltage and line-to-line voltage have three levels and five levels, respectively. Fig. 4-13 (b) to (e) show the distortion of the outputs when the open-circuit fault occurs in S_{a1} to S_{a4}, respectively. In the case of the S_{a1} and S_{a2} faults, the positive phase current is distorted. The negative phase current is distorted when the open-circuit fault occurs in S_{a3} and S_{a4} as analyzed in Chapter 4.2.

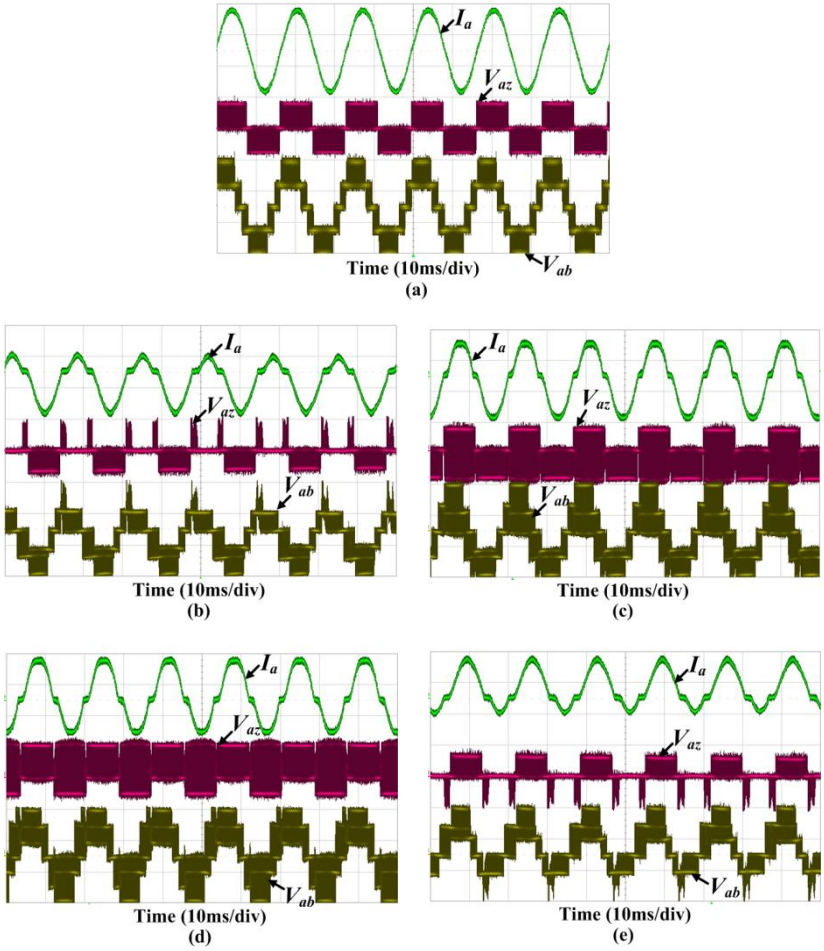

Fig. 4-13 Comparison of outputs of the T-type inverter (a) under the normal condition (b) S_{a1} open-circuit fault (c) S_{a2} open-circuit fault (d) S_{a3} open-circuit fault (e) S_{a4} open-circuit fault; I_a (5A/div), V_{az} (100V/div), V_{ab} (100V/div).

Fig. 4-14 (a) shows the experimental results of the proposed fault diagnosis method when the open-switch fault occurs in S_{a1}. After the fault occurs, the phase current, especially the positive phase current of the faulty phase is distorted and the upper capacitor voltage becomes larger than the lower capacitor voltage. The faulty switch is detected within 30 ms based on (4.3) and Table 4-2 and the identification number is measured to be 1 which means the open-circuit fault occurs in S_{a1}. Fig. 4-14 (b) to (d) also show experimental results when the open-circuit fault occurs in S_{a2}, S_{a3} and S_{a4}, respectively. The fault switch is identified within 40 ms in all cases and the identification number is also measured to be 2, 3 and 4, respectively.

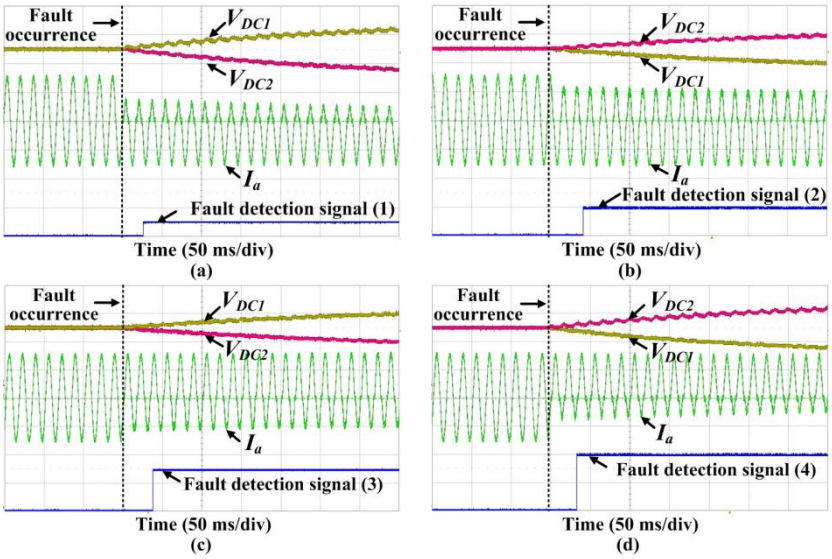

Fig. 4-14 Experimental results of the proposed fault detection method (a) open-circuit fault occurs in S_{a1} (b) open-circuit fault occurs in S_{a2} (c) open-circuit fault occurs in S_{a3} (d) open-circuit fault occurs in S_{a4}; I_a (5A/div), $V_{DC1,2}$ (50V/div).

It can be seen from the experimental results that the faulty switch is identified correctly by the proposed fault detection method. The diagnosis time can be varied according to operating and system conditions. As output current is higher and capacitance of DC-link capacitors is smaller, diagnosis time can be reduced because they affect the change of the capacitor voltages.

Fig. 4-15 (a) and (b) shows the experimental results of the proposed fault-tolerant control when the open-circuit faults occur in S_{a1} and S_{a4}, respectively. The output pole voltage is fixed to zero. It means that the half bridge switches of the faulty phase S_{a1} and S_{a4} are not used under the proposed fault-tolerant control. The magnitude of the output phase current decreases and the line-to-line voltage has three levels after the fault-tolerant method is applied because of the reduced modulation index. Although the output power is decreased, the distortion of the outputs is eliminated well.

Fig. 4-16 (a) and (b) shows the experimental results of the proposed Two-Level Switching Method (TLSM) when the open-circuit fault occurs in S_{a2} and S_{a3}, separately. After the proposed TLSM is applied, the distortion of the outputs disappears and the output pole voltage has two levels as in a conventional two-level inverter because, in the proposed TLSM, the switching state [O] in the faulty phase-A is not used.

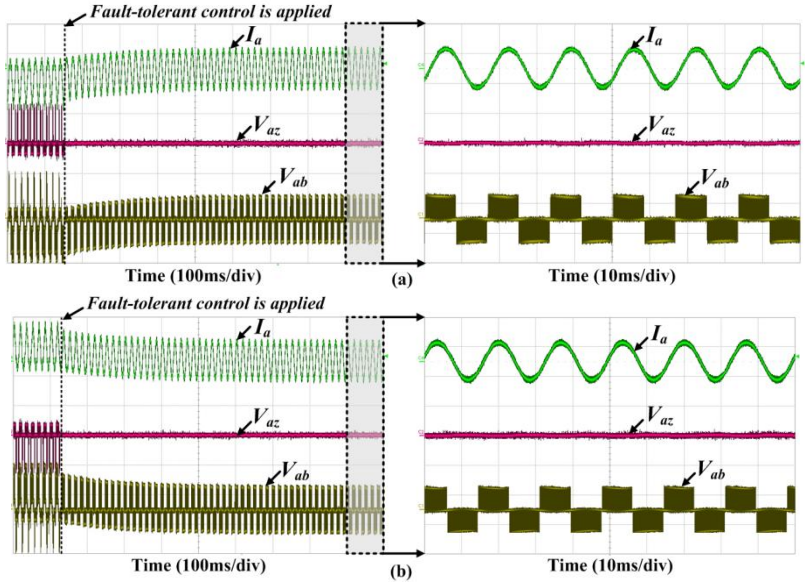

Fig. 4-15 Experimental results of the proposed fault-tolerant control (a) open-circuit fault occurs in S_{a1} (b) open-circuit fault occurs in S_{a4}; I_a (5A/div), V_{az} (100V/div), V_{ab} (100V/div).

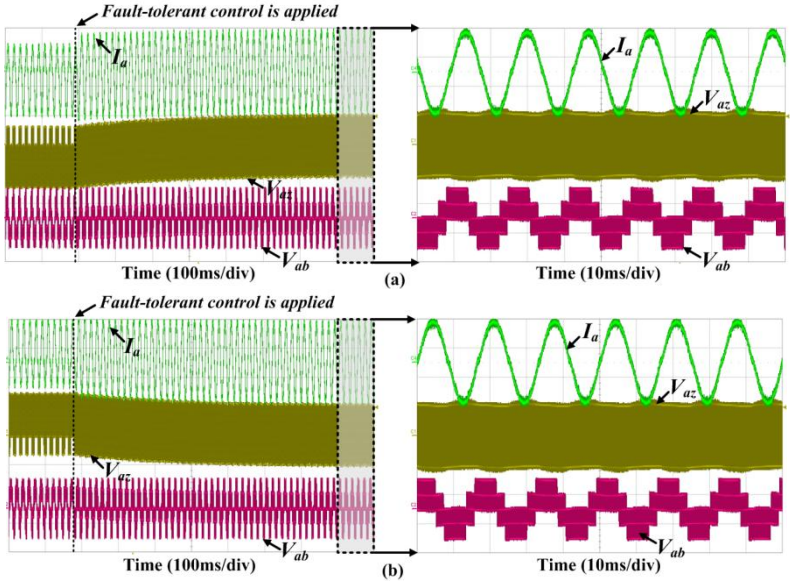

Fig. 4-16 Experimental results of the proposed fault-tolerant control TLSM (a) open-circuit fault occurs in S_{a2} (b) open-circuit fault occurs in S_{a3}; I_a (5A/div), V_{az} (100V/div), V_{ab} (200V/div).

In this case, the inverter can be operated without decrease of the output power because the proposed fault-tolerant control can be applied without reducing the modulation index.

The Total Harmonic Distortion (THD) is a little bit increased compared to the normal operating condition since this method does not use the switching state [O] in the faulty phase. Nevertheless, the experimental results demonstrate that the T-type inverter is operated with well-maintained performance by the TLSM when the neutral-point switch fails.

Fig. 4-17 (a) shows the experimental result of the proposed HDSM when the open-circuit fault occurs in S_{a2}. In the sectors I and VI, the switching state of the phase-A is kept to [P] and the switching state is kept to [N] in the sectors III and IV as Discontinuous Pulse Width Modulation (DPWM). In the sectors II and VI, TLSM is applied. Therefore, the phase-A has two switching states [P] and [N]. In the case of the S_{a4} fault, the control method is the same as the previous case and the result is shown in Fig. 4-17 (b). It can be seen from the experimental results that the inverter is operated without distortion in the outputs and de-rating of the output power after the proposed method is applied.

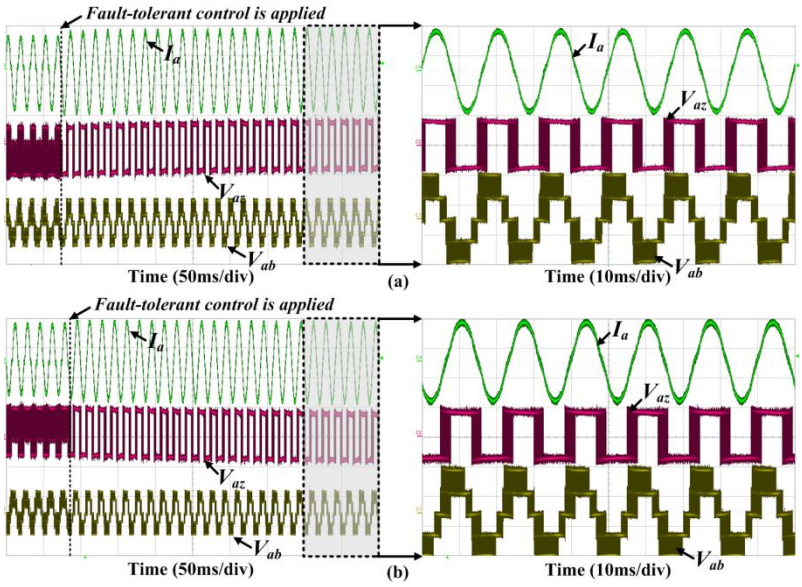

Fig. 4-17 Experimental results of the proposed fault-tolerant control Hybrid Discontinuous Switching Method (HDSM) (a) open-circuit fault occurs in S_{a2} (b) open-circuit fault occurs in S_{a3}; I_a (5A/div), V_{az} (100V/div), V_{ab_left} (200V/div), V_{ab_right} (100V/div).

4.6. SUMMARY

In this chapter, the open-circuit fault-detection and fault-tolerant control methods for the T-type three-level inverter has been proposed.

The operation of the T-type inverter under the open-circuit fault condition has been analyzed first and then the open-circuit fault detection method has been proposed. The location of the faulty switch can be identified based on the distortion of the phase currents and change of two DC-link capacitor voltages.

The fault-tolerant control methods have been explained by dividing the fault into two cases: the open-circuit fault occurring in the half-bridge switches and the open-circuit fault occurring in the neutral-point switches. In the first case, the modulation index should be reduced until the reference voltage is in the inner hexagon of the voltage vector diagram. In other words, the inverter operation without output distortions is possible with reduced power at reduced output voltage. It means that, the proposed fault-tolerant method for the half-bridge switch fault typically cannot be used for applications with fixed output voltage like grid-connected inverters. However, if the inverter system is allowed to increase the DC-link voltage so that the modulation index decreases, it is possible to apply the proposed fault-tolerant control method to the applications with fixed output voltage without output power de-rating. The proposed fault-tolerant control method can be helpful for several safety critical applications that need the continuous operation although the output power is reduced. In the second case, the two fault-tolerant controls have been proposed. By the proposed method, the T-type inverter can be operated with the acceptable output performance and no de-rating of the output power and voltages even though THDs of the outputs increase. Therefore, these two fault-tolerant methods can be applied for all kinds of applications and give higher system reliability.

The feasibility and effectiveness of the proposed open-circuit fault detection and fault-tolerant control methods have been verified by the experiments.

CHAPTER 5. OPEN-CIRCUIT FAULT DETECTION AND FAULT-TOLERANT CONTROL METHODS FOR A GRID-CONNECTED NPC INVERTER

There are many grid applications especially in renewable energy system such as PV and wind turbine systems and NPC inverter is one of the most widely used topology for the gird connection. Therefore, it is worth to investigate fault detection and fault-tolerant control methods for the grid-connected NPC inverter to improve their reliability and availability. This chapter presents open-circuit fault detection and fault-tolerant control methods for the grid-connected NPC inverter. Experimental results verify the feasibility and effectiveness of the proposed fault detection and fault-tolerant control methods.

5.1. OPERATION OF A GRID-CONNECTED NPC INVERTER UNDER OPEN-CIRCUIT FAULT CONDITIONS

In this section, the operation of the grid-connected NPC inverter under the open-circuit faults is analyzed considering the open-circuit faults in phase-A. For this study, simulations are performed under the conditions listed in Table 5-1.

Table 5-1 Simulation parameters of the grid-connected NPC inverter.

Parameter	**Value**
DC-link voltage	*700 V*
Switching frequency	*10 kHz*
Control period	*100 μs*
Output current	*10* A_{peak}
Output frequency	*50 Hz*
Grid voltage	*220* V_{rms}
Filter	*L: 3 mH*

Fig. 5-1 shows the grid-connected NPC inverter system. Two different kinds of the open-circuit faults within the NPC inverter are considered; one is when the open-circuit fault occurs in one of the switches (Type-A fault) and the other one is when the open-circuit fault occurs in one of the clamping diodes (Type-B fault). The current from the inverter to the grid is considered as being the positive direction.

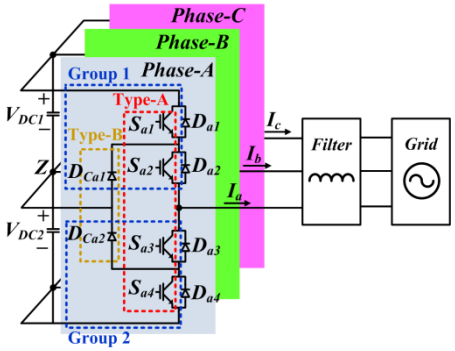

Fig. 5-1 Grid-connected Neutral-Point Clamped (NPC) inverter system.

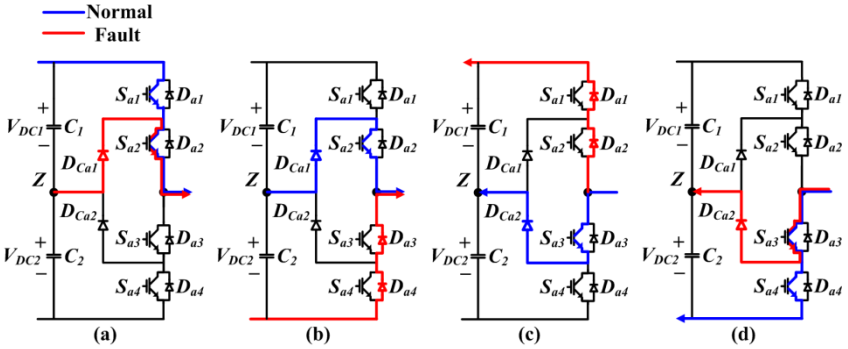

Fig. 5-2 Current paths (a) under normal and S_{a1} fault condition when $I_a > 0$ with [P] (b) under normal and S_{a2} or D_{Ca2} fault condition when $I_a > 0$ with [O] (c) under normal and S_{a3} or D_{Ca2} fault condition when $I_a < 0$ with [O] (d) under normal and S_{a4} fault condition when $I_a < 0$ with [N].

5.1.1. TYPE-A FAULT

Open-circuit fault in S_{a1}

Fig. 5-2 (a) shows a current path under the normal condition. The current path is formed through S_{a1} and S_{a2} when the switching state is [P] with a positive current. If the open-circuit fault occurs in S_{a1}, the switching state [P] is impossible but the switching state [O] is possible functionally. If the open-circuit fault occurs while the positive current flows, the current flows through D_{Ca1} and S_{a2} while the positive current is decreased to zero and then, if the current is reached to zero, D_{Ca1} is reverse biased due to the positive grid voltage. Consequently, there are no current paths and the positive current of the faulty phase does not flow as shown in Fig. 5-3 (a). The upper capacitor voltage V_{DC1} becomes larger than the lower capacitor voltage V_{DC2}, because of the distortion in the positive current.

Open-circuit fault in S_{a2}

Under the normal condition, the current path is formed through D_{Ca1} and S_{a2} when the switching state is [O] with the positive current as shown in Fig. 5-2 (b). However, if the open-circuit fault occurs in S_{a2}, the switching states [P] and [O] are impossible. The possible current path is only through D_{a3} and D_{a4}. If the open-circuit fault occurs in S_{a2} while the positive current flows, the current flows through D_{a3} and D_{a4} until it decreases to zero and then, D_{a3} and D_{a4} are reverse-biased due to the positive grid voltage. It means that there are no current paths and the positive current of the faulty phase does not flow as shown in Fig. 5-3 (b). In this case, the distorted outputs are the same with the outputs under the S_{a1} fault condition.

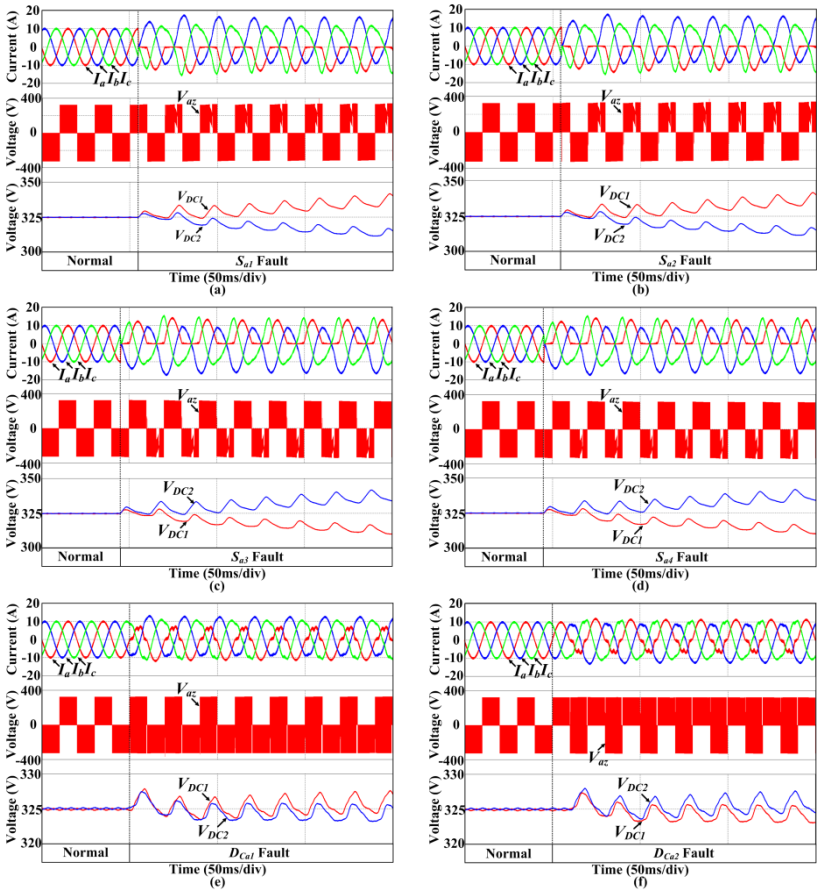

Fig. 5-3 Output currents, pole voltage and capacitor voltages of the grid-connected NPC inverter under the open-circuit fault conditions (a) S_{a1} fault (b) S_{a2} fault (c) S_{a3} fault (d) S_{a4} fault (e) D_{Ca1} fault (f) D_{Ca2} fault.

Open-circuit fault in S_{a3}

The overall analysis is almost the same with the previous case except for the current direction. Under the normal condition, the current path is formed through S_{a3} and D_{Ca2} while the switching state [O] with the negative current. In the case of the switching state [N], the current path is formed through the switches S_{a3} and S_{a4} as shown in Fig. 5-2 (d). If the open-circuit fault occurs in S_{a3} while the negative current flow, the current path is formed through the D_{a1} and D_{a2} until the current decreases to zero as shown in Fig. 5-2 (c). If it decreases to zero, D_{a1} and D_{a2} are reverse-biased due to the negative grid voltage. Therefore, the negative current does not flow because both switching state [O] and [N] are impossible and V_{DC2} becomes larger than V_{DC1} as shown in Fig. 5-3 (c).

Open-circuit fault in S_{a4}

Under the S_{a4} open-circuit fault condition, the switching state [N] is impossible but the switching state [O] is possible. If the open-circuit fault occurs in S_{a4} when the negative current flows, the current flow through D_{a1} and D_{a2} until it decreases to zero. After the current is reached to zero, however, the current path is not made in this case also because the diode D_{Ca2} is reverse-biased and the diodes D_{a1} and D_{a2} are also reverse-biased due to the negative grid voltage. Therefore, the negative phase current of the faulty phase does not flow and V_{DC2} becomes larger than V_{DC1} as shown in Fig. 5-3 (d). The distortion of the outputs under the S_{a4} fault is the same as the outputs under the S_{a3} fault condition.

5.1.2. TYPE-B FAULT

Open-circuit fault in D_{Ca1}

If the open-circuit fault occurs in the clamping diode D_{Ca1}, the switching state [P] is possible but the switching state [O] is impossible. Under the normal condition, the current path is formed through D_{Ca1} and S_{a2} when the switching state is [O] with the positive current. However, under the D_{Ca1} fault condition, the output is connected to the negative DC-link through D_{a3} and D_{a4} instead of D_{Ca1} and S_{a2} as shown in Fig. 5-2 (b) even though the negative voltages are applied across D_{a3} and D_{a4} by the negative grid voltage. This is because there is a positive current which is generated by the switching state [P]. Therefore, the output pole voltage becomes $-V_{DC}/2$ and this wrong output voltage causes the distortion of the positive phase current as shown in Fig. 5-3 (e). In this case, the current distortion is smaller than under Type-A fault because the output voltage is distorted only when the switching state is [O]. Therefore, the neutral-point voltage unbalance is also smaller than that of the Type-A fault case.

Open-circuit fault in D_{Ca2}

In the case of D_{Ca2} fault, the current path is formed through D_{a1} and D_{a2} instead of the S_{a3} and D_{Ca2} when the switching state is [O] with negative current as shown in Fig. 5-2 (c). Therefore, the output pole voltage becomes $V_{DC}/2$ instead of 0. This undesirable current path and pole voltage make the negative phase current to be distorted as shown in Fig. 5-3 (f).

Several methods to detect the open-circuit fault have been proposed such as the current pattern method, slope method and DC current method [121-122]. However, it is impossible to identify the faulty switch by the existing methods because the output distortions between $S_{x1(x=a,b,c)}$ fault and S_{x2} fault or between S_{x3} fault and S_{x4} fault are the same as illustrated in Fig. 5-3.

5.2. OPEN-CIRCUIT FAULT DETECTION METHOD

In this section, an open-circuit fault detection method is discussed. Firstly, the identification of the faulty leg and group is presented and then the classification of fault type is described. Finally, the fault switch detection method under the Type-A fault is proposed.

5.2.1. IDENTIFICATION OF THE FAULTY LEG AND GROUP

The proposed fault detection method is explained considering the open-circuit fault in phase-A. The faulty phase and group can be identified based on the characteristic of the distorted currents. The average value of the positive current of each phase is defined by $I_{x\_ave(+)}$ and the average value of the negative current is defined by $I_{x\_ave(-)}$. The average value during one fundamental period of the phase current is defined by $I_{x\_ave(all)}$ as shown in Fig. 5-4.

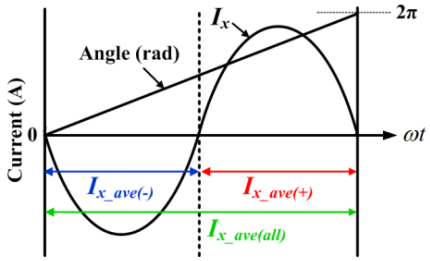

Fig. 5-4 Definition of variables for the fault detection method.

Each phase can be divided into two groups. For example phase-A, a group 1 consists of the two upper switches (S_{a1} and S_{a2}) and the diode D_{Ca1}. A group 2 is composed of the two lower switches (S_{a3} and S_{a4}) and the diode D_{Ca2}. Under the normal condition, the average of the phase current is zero. It means that the summation of $I_{x\_ave(+)}$ and $I_{x\_ave(-)}$ which is $I_{x\_ave(all)}$ is also zero. However, if the open-circuit fault occurs among the upper components (S_{a1} or S_{a2} or D_{Ca1}), $I_{a\_ave(all)}$ has a negative value because the positive current of the phase-A is distorted. The average values of the other phases have the positive values and the total amount of increasing average values is the same with the $I_{a\_ave(all)}$ if it is a three-phase balanced system. Thus, $I_{a\_ave(all)} = -(I_{b\_ave(all)} + I_{c\_ave(all)})$. On the contrary, if the open-circuit fault occurs in the lower component (S_{a3} or S_{a4} or D_{Ca2}) of the phase-A, $I_{a\_ave(all)}$ has a positive value and the other phases have negative values. Therefore, the faulty phase and group can be identified using the polarities of $I_{a\_ave(all)}$ and the summation of $I_{b\_ave(all)}$ and $I_{c\_ave(all)}$. However, as mentioned before, this direct average current method tends to be highly unreliable and it is difficult to set the threshold value to be a constant because it depends on the variations of the output currents. Therefore, the normalized phase currents are also used for the fault detection. The phase currents can be normalized by (4.1) and (4.2) as described in Chapter 4.3.

5.2.2. CLASSIFICATION OF THE FAULT TYPE

The fault type can be classified after the faulty phase and group are detected. The large difference between the Type-A fault, which is the open-circuit fault in the switches, and the Type-B fault, which is the open-circuit fault in the clamping diodes, is whether the current flows or not during the half cycle of the faulty phase current as illustrated in Fig. 5-3. For example, if the open-circuit fault occurs in D_{Ca1}, the positive phase current of the faulty phase is distorted, but it flows as shown in Fig. 5-3 (e). Thus, $I_{a\_ave(+)}$ has a positive value and $I_{a\_ave(all)}$ has a negative value. However, in the case of the Type-A fault (S_{a1} or S_{a2} fault), the positive phase current does not flow as shown in Fig. 5-3 (a). $I_{a\_ave(all)}$ has also the negative value but $I_{a\_ave(+)}$ has the zero value. Therefore, the Type-A and Type-B faults can be classified using different distortion characteristic of the output current. The identification of the group and fault type in the faulty phase-A is described in Table 5-2. The threshold value I_{thr1} is used to determine the polarity of the average current value to protect against a false alarm in the fault detection.

5.2.3. DIAGNOSIS OF THE FAULTY SWITCH UNDER THE TYPE-A FAULT

The remarkable difference between the open-circuit faults in the upper switches ($S_{x1(x=a,b,c)}$ and S_{x2}) or between the open-circuit faults in the lower switches (S_{x3} and S_{x4}) is the possibility of the switching state [O]. For instant phase-A, under the S_{a1} open-circuit fault, the switching state [P] is only impossible when the current is positive. In the case of S_{a2} open-circuit fault, both switching states [P] and [O] are

impossible. However, it is impossible to determine the possibility of the switching state [O] under the faulty condition due to the same distortion characteristic of the phase currents as shown in Fig. 5-3. To determine the possibility of the switching state [O], an underexcited reactive power may be injected.

Usually, the grid-connected inverter transfer electric power to the grid with a unity Power Factor (PF). Therefore, the polarities of the output phase current and the output voltage are almost the same as shown in Fig. 5-5 (a). If the underexcited reactive power is injected, the phase current leads the output voltage and the grid voltage and thus the regions which have the different polarities between the phase current and the output voltage occurs as shown in Fig. 5-5 (b). In this section, Region 1 means that the phase current is positive and the output voltage is negative and Region 2 means that the phase current is negative and the output voltage is positive. By making the Regions 1 and 2 through the underexcited reactive power injection, the possibility of the switching state [O] can be determined and the faulty switch also can be identified. Depending on the faulty switch, the current in the Region 1 or 2 flows or not.

The voltage space vector diagram of the NPC inverter can be divided into the sectors as shown in Fig. 5-6 to determine the region where the underexcited reactive power is injected for the identification of the faulty switch.

Table 5-2 Identification of faulty group and open-circuit fault type in phase-A

Fault (Fault Type)	$I_{a\_ave(+)}$	$I_{a\_ave(-)}$	$I_{a\_ave(all)}$	$I_{b\_ave(all)} + I_{c\_ave(all)}$
D_1 **(B)**	$> I_{thr1}$	$< -I_{thr1}$	$< -I_{thr1}$	$> I_{thr1}$
S_{a1} **or** S_{a2} **(A)**	$-I_{thr1} <, < I_{thr1}$	$< -I_{thr1}$	$< -I_{thr1}$	$> I_{thr1}$
D_2 **(B)**	$> I_{thr1}$	$< -I_{thr1}$	$> I_{thr1}$	$< -I_{thr1}$
S_{a3} **or** S_{a4} **(A)**	$> I_{thr1}$	$-I_{thr1} <, < I_{thr1}$	$> I_{thr1}$	$< -I_{thr1}$

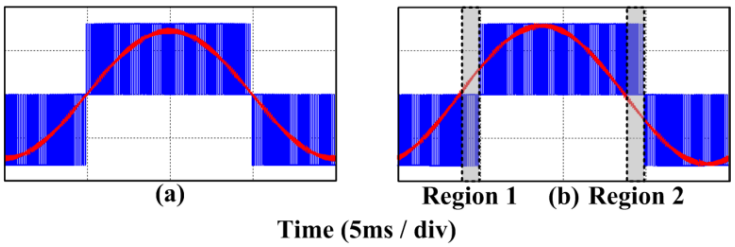

Fig. 5-5 Phase currents I_a (7.5A/div) and pole voltage V_{az} (200V/div) (a) before (b) after underexcited reactive current is injected from the grid.

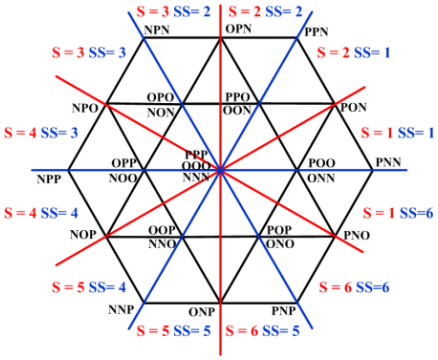

Fig. 5-6 Sectors of the space vector diagram for faulty switch detection.

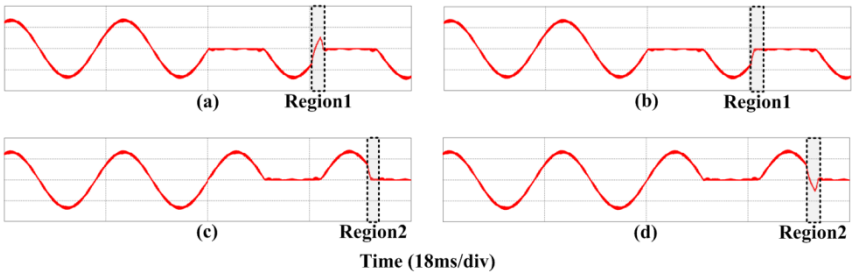

Fig. 5-7 Current of faulty phase with proposed fault detection method for faulty switch identification under Type-A fault (a) S_{a1} (b) S_{a2} (c) S_{a3} (d) S_{a4} open-circuit faults.

To identify the faulty switch between S_{a1} and S_{a2}, the underexcited power is injected when S = 5 and SS = 5 so that the Region 1 occurs. In the Region 1, the reference voltage is negative and thus it is made by the switching states [O] and [N]. All current paths by these switching states [O] and [N] are possible regardless of the open-circuit fault in S_{a1}. Therefore, the positive phase current flows in the Region 1 as shown in Fig. 5-7 (a). However, in the case of the open-circuit fault in S_{a2}, the positive phase current does not flow in the Region 1 as shown in Fig. 5-7 (b) because the switching state [O] is impossible. From this characteristic, the possibility of the switching state [O] is checked and the faulty switch between the upper switches (S_{a1} and S_{a2}) can be identified. In the case of the Type-A fault in the group 2, the underexcited reactive power is injected, when S = 2 and SS = 2 in order to make the Region 2. In this region, the positive reference voltage is made by the switching states [P] and [O] and all current paths by the switching states [P] and [O] are possible because the grid voltage is negative. Therefore, the negative phase current flows in the Region 2 as shown in Fig. 5-7 (d) regardless of the open-circuit fault in S_{a4}. On the contrary, if the open-circuit fault occurs in S_{a3}, the current path

when the switching state [O] is impossible. Therefore, the negative current does not flow in the Region 2 as shown in Fig. 5-7 (c). From this characteristic, the faulty switch between S_{a3} and S_{a4} can be determined.

The magnitude of the injected underexcited reactive current can be determined according to the magnitude of the output currents and the threshold value (I_{thr2}) of the current for the faulty switch identification.

To make the positive current flow above the threshold value in the Region 1 (S=5 and SS=5) or the negative current flow above the threshold value in the Region 2 (S=2 and SS=2) sufficiently, the power factor should be changed properly by injecting the underexcited reactive current. Further, underexcited reactive current to be injected should be larger than I_{thr2}. In this systme, the power factor is changed to 0.9 (leading) to make the regions 1 and 2 in sectors that are described in Table 5-3 and to make the current flow.

Table 5-3 shows the sectors where the underexcited reactive current is injected for the faulty switch identification. The minimum reactive current is set to $2*I_{thr2}$ by considering a margin. The underexcited reactive current is injected under the open-circuit fault condition, which is an abnormal condition. It means that, the produced current by the reference of the reactive current may not be guaranteed because the unbalanced capacitor voltages make a much smaller output pole voltage than that of under the normal condition. Therefore, the larger reference of the underexcited reactive current than the threshold value (I_{thr2}) should be set. The demanded underexcited reactive current can be defined as

$$\begin{aligned} I_{de\_ref(-)} &= -I_{qe} \cdot \cos^{-1}(0.9) \quad && (if\ I_{de\_ref(-)} < -2 \cdot I_{thr2}) \\ I_{de\_ref(-)} &= -2 \cdot I_{thr2} && (if\ I_{de\_ref(-)} \geq -2 \cdot I_{thr2}) \end{aligned} \tag{5.1}$$

Fig. 5-8 shows the flow chart of the proposed fault detection method considering the faults in the phase-A.

Table 5-3 Sectors of underexcited reactive current injection for faulty switch identification.

Faulty switch	***Sector***
$\boldsymbol{S_{a1}}$ **or** $\boldsymbol{S_{a2}}$	S = 5, SS = 5
$\boldsymbol{S_{a3}}$ **or** $\boldsymbol{S_{a4}}$	S = 2, SS = 2
$\boldsymbol{S_{b1}}$ **or** $\boldsymbol{S_{b2}}$	S = 1, SS = 1
$\boldsymbol{S_{b3}}$ **or** $\boldsymbol{S_{b4}}$	S = 4, SS = 4
$\boldsymbol{S_{c1}}$ **or** $\boldsymbol{S_{c2}}$	S = 3, SS = 3
$\boldsymbol{S_{c3}}$ **or** $\boldsymbol{S_{c4}}$	S = 6, SS = 6

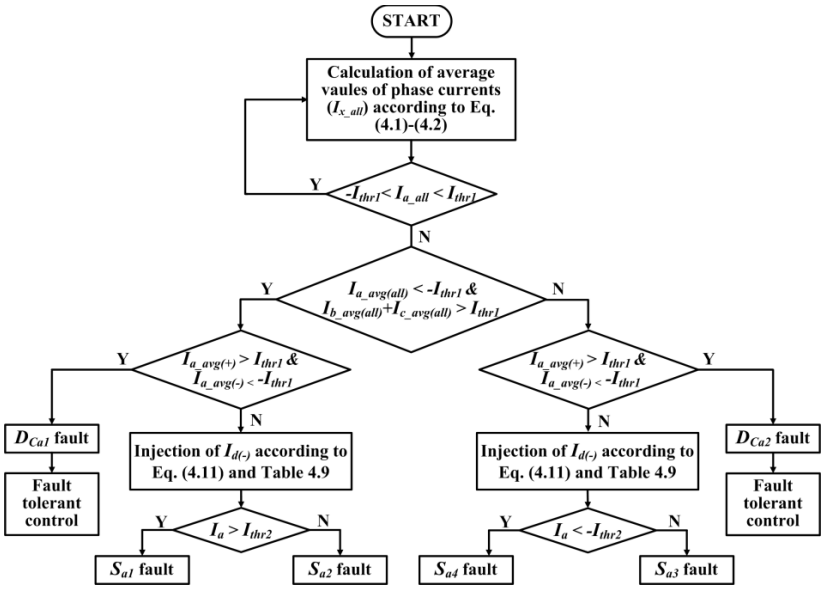

Fig. 5-8 Flow chart of the proposed fault detection method considering the faults in phase-A.

5.3. FAULT-TOLERANT CONTROL STRATEGY UNDER THE OPEN-CIRCUIT FAULT IN CLAMPING DIODE

If the open-circuit fault occurs in D_{Ca1}, it is impossible to generate the switching states of the small voltage vectors [OON], [ONN], [ONO] and the switching states of the medium voltage vectors [OPN], [ONP], when I_a is positive.

In the case of the open-circuit fault in D_{Ca2}, the switching states of the small voltage vectors [OPO], [OPP], [OOP] and the switching states of the medium voltage vectors [OPN], [ONP] cannot be produced when I_a is negative. These two results are the same when the open-circuit faults occur in S_{a2} and S_{a3} of the T-type inverter, respectively. It means that the fault-tolerant control methods (TLSM and HDSM) for the neutral-point switch in the T-type inverter, which are explained in chapter 4.4.2 can be directly applied to the NPC inverter when the open-circuit fault occurs in the clamping diodes.

Furthermore, if the NPC inverter is not operated for applications with fixed output voltage, it is also possible to use the fault-tolerant control method for the half-bridge switch in the T-type inverter, when the open-circuit fault occurs in S_{x1} and S_{x4} in the NPC inverter.

5.4. EXPERIMENTAL RESULTS

Experiments have been carried out to verify the validity and effectiveness of the proposed fault detection and fault-tolerant control methods. A prototype of the NPC inverter system has been built and used for the experiments as shown in Fig. 5-9. The design specifications and parameters used in the experiments are listed in Table 5-4.

Fig. 5-10 shows the output of the grid-connected NPC inverter under the normal condition. The phases of the output pole voltage, output current and grid voltage are almost the same, when it is operated with unity power factor.

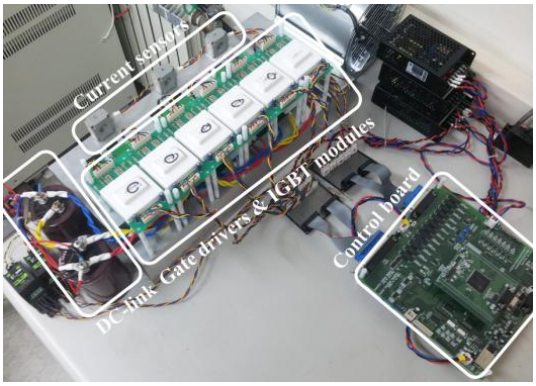

Fig. 5-9 Prototype of a grid-connected NPC inverter system.

Table 5-4 Parameters for the experiments of the proposed methods for NPC inverter.

Parameter	Value
DC-link voltage	*600 V*
Grid voltage	*300* V_{peak}
Switching frequency	*10 kHz*
Control period	*100* μs
Output frequency	*60 Hz*
L-filter	*3 mH*
I_{thr1}, I_{thr2}	*1.5 A, 2 A*

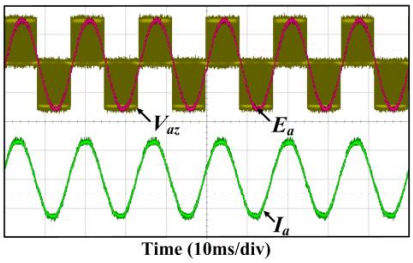

Fig. 5-10 Outputs of the grid-connected NPC inverter in normal operation; pole voltage (V_{az}), grid voltage (E_a) and phase current (I_a); I_a (5A/div), E_a (200V/div), V_{az} (200V/div).

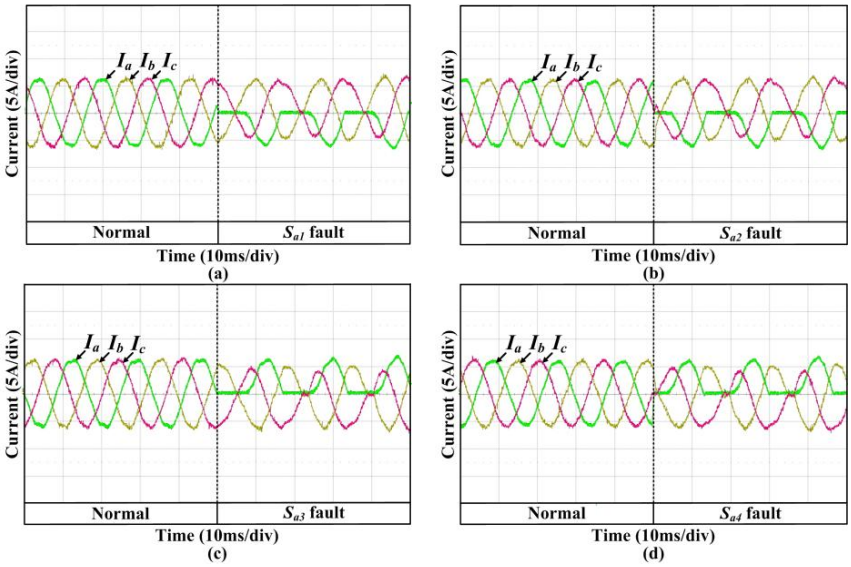

Fig. 5-11 Phase currents under the Type-A open-circuit fault (a) S_{a1} fault (b) S_{a2} fault (c) S_{a3} fault (d) S_{a4} fault.

Fig. 5-11 shows the experimental waveforms when the open-circuit fault has occurred in the switches of the phase-A (Type-A fault). If the open-circuit fault occurs, the positive or negative current of the faulty phase does not flow. Further, the distortion of the output currents between S_{a1} and S_{a2} open-circuit faults or between S_{a3} and S_{a4} open-circuit faults are the same as analyzed in chapter 5.1.1.

Fig. 5-12 shows the output currents when the Type-B open-circuit fault has occurred in phase-A. The output currents are distorted but both positive and negative currents of the faulty phase flow on the contrary of the Type-A open-circuit fault.

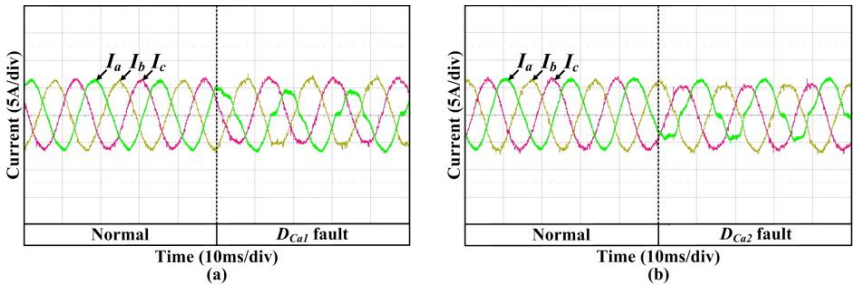

Fig. 5-12 Phase currents under the Type-B open-circuit fault (a) D_{ca1} fault (b) D_{ca2} fault.

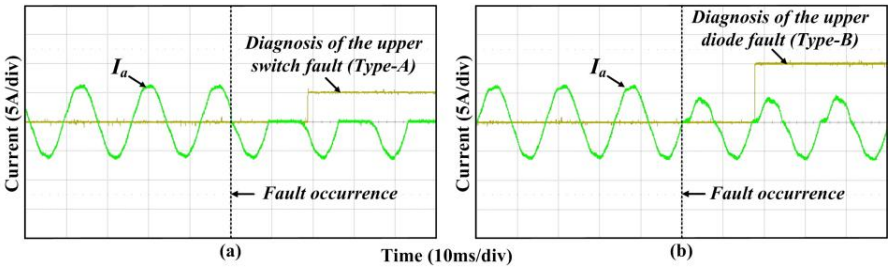

Fig. 5-13 Identification of fault type when (a) Type-A open-circuit fault occurs in S_{a1} (b) Type-B open-circuit fault occurs in D_{Ca1}.

Fig. 5-13 (a) shows the experimental result of the fault type identification when the Type-A open-circuit fault occurs in S_{a1}. $I_{a\_ave(all)}$ and $I_{a\_ave(-)}$ have the negative value and $I_{a\_ave(+)}$ is in the range of the threshold value which is ± 1.5A in this case because the positive phase current does not flow. The fault-type is identified within about one fundamental period and the identification number is to be 1 which means the Type-A fault. However, in the case of the Type-B fault, $I_{a\_ave\_(+)}$ has the positive value and it is larger than the positive threshold value because the positive current flows even though it is distorted. Fig. 5-13 (b) shows the fault type identification result when the open-circuit fault occurs in D_{Ca1}. It is also identified in about one fundamental period and the identification number is to be 2 which means the Type-B fault. As it can be seen in Fig. 5-13, the Type-A and Type-B faults can be identified precisely using the characteristics of the distorted output currents. After the fault type is determined, the faulty switch can be detected by the proposed method under the Type-A fault.

Fig. 5-14 (a) and (b) shows the experimental results of the proposed fault detection method when the Type-A open-circuit faults occur in S_{a1} and S_{a2}, respectively. The Type-A fault detection signal indicates the occurrence of the open-circuit fault and

whether the open-circuit-fault occurs in upper switches or in lower switches. The fault detection signal "1" means that the open-circuit fault occurs in one of two upper switches and "2" means that the open-circuit fault occurs in one of two lower switches. The fault switch identification signal denotes the location of the faulty switch in the faulty phase. After the fault type and group are detected by the detection signal as 1, the underexcited reactive current has been injected when S = 5 and SS = 5 to identify the faulty switch between S_{a1} and S_{a2}. In the case of the S_{a1} fault, the positive phase current flows in the region, where the underexcited current is injected as shown in Fig. 5-14 (a). However, if the open-circuit fault occurs in S_{a2}, the positive current does not flow as shown in Fig. 5-14 (b). Fig. 5-14 (c) and (d) show the experimental results of the proposed fault detection method when the Type-A open-circuit occurs in S_{a3} and S_{a4}, respectively. To separate the fault location between the two lower switches (S_{a3} and S_{a4}), the underexcited reactive current has been injected when S = 2 and SS = 2. The negative current does not flow under the open-circuit fault in S_{a3}, but the negative current flows in the case of open-circuit fault in S_{a4}. From the above results, it can be seen that the location of the faulty switch can be identified correctly by injecting the underexcited reactive current.

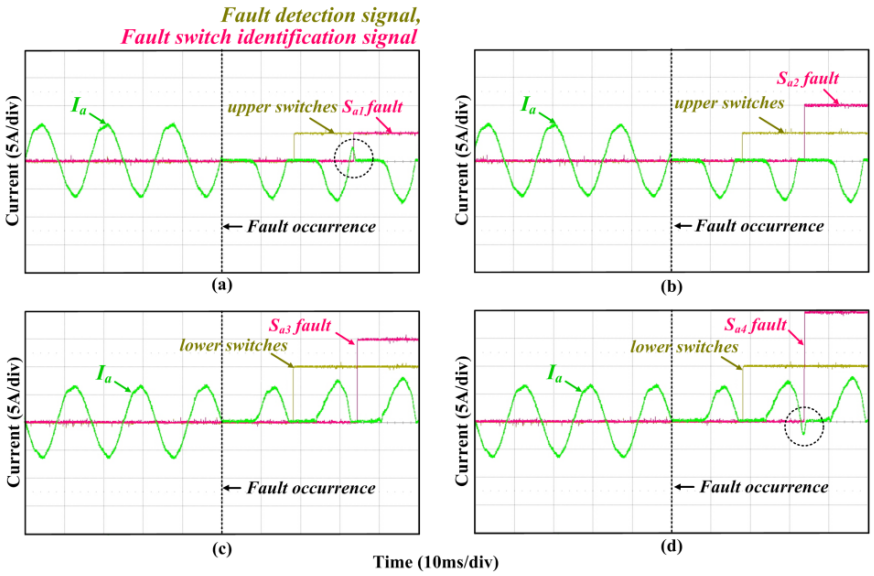

Fig. 5-14 Diagnosis of the faulty switch under the Type-A open-circuit fault by underexcited reactive current injection (a) S_{a1} fault (b) S_{a2} fault (c) S_{a3} fault (d) S_{a4} fault

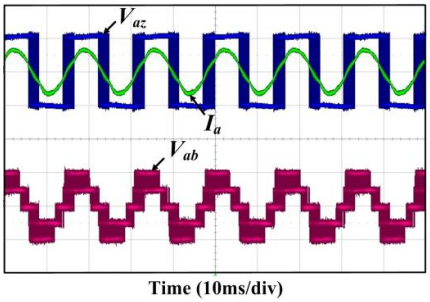

Fig. 5-15 Outputs of the grid-connected NPC inverter under the fault-tolerant control when the open-circuit fault occurs in D_{Ca1}; I_a (10A/div), V_{az} (300V/div), V_{ab} (600V/div).

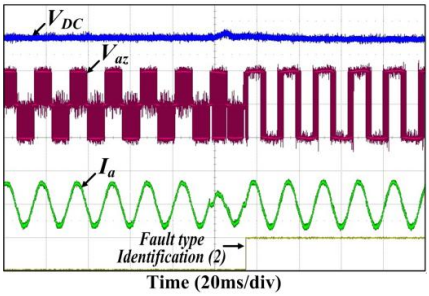

Fig. 5-16 Experimental result of the proposed methods from fault detection to fault-tolerant control when the open-circuit fault occurs in D_{Ca1}; I_a (10A/div), V_{az} (300V/div), V_{DC} (150V/div).

Fig. 5-15 shows the outputs of the grid-connected NPC inverter under the fault-tolerant control. The Total Harmonic Distortion (THD) of the output increases compared with the outputs under the normal condition since the two-level switching method is applied in some of the regions. Under the normal condition, a THD of the line-to-line voltage is 34%. If the proposed fault-tolerant control is applied, the line-to-line voltages (V_{ab} and V_{ac}) which contain the faulty leg are increased to 44 %. The other line-to-line voltage (V_{bc}) keeps the same THD under the normal condition. The most of world leading companies have designed their inverters with a margin of a THD of the current to be less than 2-3 % at the nominal power [123-124]. Therefore, even though the THD of the line-to-line voltages are increased, the inverter could comply with standards for the grid-connection. Further, the manufacturer can consider the fault-tolerant control mode when the output filter is designed to improve the reliability and availability of the NPC inverter under the open-circuit fault condition.

Fig. 5-16 shows the experimental results of the overall procedure from fault detection to fault-tolerant control when the open-circuit fault occurs in D_{Ca1}. Due to the distortion of the output currents, the DC-link voltage increases by about 20 V. After the fault type is identified by the identification signal which is measured to be 2 which means that Type-B fault occurs in group 1, the fault-tolerant control method HDSM is applied. The distortion of the output currents is eliminated and the DC-link voltage becomes stable. The experimental results demonstrate that the grid-connected NPC inverter is operated with well-maintained performance by the proposed fault-tolerant control method, when the open-circuit fault occurs in the clamping diodes.

5.5. SUMMARY

Open-circuit fault-detection and fault-tolerant control methods for the NPC inverter under the grid-connection have been proposed.

In the beginning of this part, the operation of the grid-connected NPC inverter under the open-circuit fault conditions has been studied. Then, the open-circuit fault detection and fault-tolerant control methods for the grid-connected NPC inverter system have been presented. Under the grid-connected condition, it is impossible to identify the fault switch by existing methods, which have been developed based on the outputs distortions for the conventional two-level inverter system. The fault between the switches and clamping diodes can be identified by checking whether the current flows or not during the half period of the output current of the faulty phase. The faulty switch between the upper two switches or between the lower two switches is classified by injecting an underexcited reactive current during short period. In the case of the open-circuit fault in the clamping diode, the fault-tolerant control method can be applied. Even though the THD of the output currents increase, the NPC inverter can be operated with acceptable output performance and without de-rating of the output power.

The feasibility and effectiveness of the proposed open-circuit fault detection and fault-tolerant control methods have been verified by experiments with prototype of the grid-connected NPC inverter system.

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

The purpose of this chapter is to summarize the results, which have been achieved throughout this PhD project and to emphasize the main contributions presented. Finally, topics for the future work are also discussed.

6.1. SUMMARY OF THESIS

This research project has performed studies on the power IGBT module from component level to converter level to improve the reliability of power electronics systems.

Accelerated power cycling test is an important method to investigate the reliability performance of power device modules regarding thermal stresses. In this kind of test, the test condition influences the results a lot. Therefore, it is important to perform the test under the realistic operating conditions to minimize the uncertainty. Furthermore, the test period and energy consumption during power cycling tests are also important factors. To perform the accelerated power cycling properly considering above aspects, the advanced accelerated power cycling test setup and methodology have been proposed. The feasibility and effectiveness of the proposed concept have been verified by building a prototype of the power cycling test setup and by performing the power cycling tests with a transfer molded IGBT module.

Furthermore, an improved junction temperature estimation method using an on-state collector-emitter voltage (V_{CE_ON}) and load current has been proposed. The proposed method compensates for an effect of different temperatures of the interconnection materials in an IGBT module on junction temperature estimation. Consequently, it leads to better estimation results. The experimental results have shown that the proposed method can reduce the junction temperature estimation error significantly which is useful in the power cycling test.

With the proposed concept, an effect of the junction temperature swing duration ($t_{\Delta Tj}$) on the lifetime of an IGBT module has been investigated and its relevant lifetime factor has been modeled. The different lifetime factor has been obtained for the specific type of IGBT modules under test with different lifetime definitions and confidence levels of a specific lifetime. The result shows the importance of the information about lifetime definition and confidence level for lifetime modeling. This study enables to include the junction temperature swing duration effect on IGBT modules for its lifetime estimation and it may result in improved lifetime prediction of IGBT modules under given mission profiles of converters. Further, the

physics-of failure analysis has been performed to investigate the failure mechanism of tested module. The bond-wire cracks are observed in all tested modules and there are no visible degradation in the chip solder joint. Therefore, the bond-wire crack is the predominant failure mechanism in the tested modules under these conditions. However, the power cycling tests under more various temperature stress conditions with a number of samples are still needed in order to investigate the effect of temperature stress conditions on the failure mechanisms with statistic results.

Finally, open-circuit fault detection and fault-tolerant control strategies for two kinds of neutral-point three-level inverters have been proposed to improve their reliability and availability under open-circuit fault conditions. Open-circuit fault detection and tolerant-control methods for a T-type inverter have been presented first. By investigating the characteristics of the output currents and two capacitor voltages, the faulty switches can be identified. Different fault-tolerant control methods have been proposed according to the faulty switch. Furthermore, an open-circuit fault detection method for a grid-connected NPC inverter has been proposed. By analyzing the distortion of the output currents and by injecting an underexcited reactive current, the faulty location in the grid-connected NPC inverter including clamping diodes can be identified precisely. In addition, a fault-tolerant control method has been proposed for the open-circuit fault in the clamping diodes. The feasibility and effectiveness of the proposed methods have been verified by the experiments.

6.2. CONTRIBUTIONS

The main contributions of this project from the author's point of view are highlighted in the following;

1. Development of apparatus and methodologies for advanced accelerated power cycling test

- Power cycling tests can be performed under realistic electrical operating conditions compared with a conventional method which injects DC current. Therefore, more accurate investigation of the reliability performance of IGBT modules is possible by the developed test setup.

- Various thermal stresses can be emulated in a short cycle period by changing various parameters such as switching frequency, output frequency, modulation index, power factor, magnitudes of output current and voltage. Therefore, the test results can be obtained in a reasonable test time as well as they are very much like real applications.

- Power losses during test can be kept small during the test. Therefore, it is also cost-effective solution.

- On-line V_{CE_ON} and V_F measurements are possible. Therefore, the condition of the tested modules during power cycling tests can be monitored in real time. Further, they can be used for junction temperature estimation.

2. Junction temperature estimation under converter operations

- An improved junction temperature estimation method using V_{CE_ON} and load current is made possible by compensating for the effect of different temperatures of the interconnection materials in the IGBT module under converter operation.

- Junction temperature estimation can be used for power cycling test and can also used for condition monitoring of IGBT modules to improve the reliability of converters.

3. Lifetime Modeling of an IGBT module regarding thermal stresses

- The effects of junction temperature swing duration on lifetime of the IGBT module is investigated with the advanced power cycling test setup.

- Also lifetime modeling procedure considering statistical analysis is presented with different definitions and confidence levels.

- A physics-of-failure analysis is performed to investigate the failure mechanism of tested modules.

4. Control strategies for NPC and T-type inverters under open-circuit faults

- New open-circuit fault detection and fault-tolerant control methods for the T-type three-level inverter are proposed.

- Also open-circuit fault detection and fault-tolerant control methods for the grid-connected NPC inverter are proposed.

- The proposed methods can improve the reliability and availability of the T-type and NPC inverters under the open-circuit fault conditions.

6.3. FUTURE WORK

Some other interesting and relevant topics are identified during the process of research work. The important research topics that could be considered for further investigation in the future are listed as follows.

1. Power cycling tests under more various thermal stress conditions

Power cycling tests regarding other parameters of temperature stress such as junction temperature swing and mean junction temperature could be performed to develop a complete lifetime model regarding temperature stress. Further, by performing the power cycling tests with more test samples and test conditions, more accurate lifetime model could be developed. Investigation of failure mechanisms based on the physic-of failure analysis according the different test conditions also could be performed. Finally, the power cycling tests with not fixed thermal stresses but more complex thermal stresses similar with real mission profile could be performed. This kind of tests could validate the lifetime estimation tools with developed lifetime model and Miner's rule.

2. Reliability investigation with different stress factors

Besides the thermal stresses, other stress factors like humidity, and vibration could affect the lifetime of IGBT modules. The effect of other stress factors on lifetime of IGBT module and the correlation between stress factors could be investigated. Further, failure mode of IGBT modules by different stress factors can be studied. Considering above aspects, the improved lifetime model including other factors could be developed. Reliability investigation under the short-circuit condition also could be an interesting topic.

3. Lifetime estimation and reliability assessment

The lifetime of IGBT module in power electronic applications under the given mission profile could be estimated with developed lifetime model based on power cycling tests. Reliability assessment of converters under different designs and control methods could be performed.

4. Reliability assessment of other kinds of modules

The interests in wide-band gap devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) for power electronic systems have been gradually increased. Therefore, investigation of the reliability performance of other kinds of modules like wide-band gap devices (SiC, GaN) could be an interesting topic.

5. Advanced controls and condition monitoring

Advanced control methods like modulation methods and power control strategies to relieve the stresses of reliability-critical components such as power devices and capacitors and their condition monitoring methods are worth to investigate from a reliability improvement point of view.

6. Advanced controls and topologies for fault tolerance

The proposed fault-tolerant control methods in this thesis degrade the output performance of the inverters and there are some limitations to use according to applications. Therefore, the developments of advanced controls and topologies that can keep the output performance same with the normal condition could be an interesting topic. Furthermore, multiple open-circuit fault and a short-circuit fault conditions could also be considered.

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