High power medium voltage DC/DC converter technology for DC wind turbines

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HIGH POWER MEDIUM VOLTAGE DC/DC CONVERTER TECHNOLOGY FOR DC WIND TURBINES

BY
CATALIN DINCAN

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High power medium voltage DC/DC converter technology for DC wind turbines

Ph.D. Dissertation

Catalin Dincan

Dissertation submitted month 07, 2018

To Lara-Maria, Luca and Andreea.

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Abstract

High voltage direct current (HVDC) connected wind farms promise reduced electrical losses, lower bill-of material cost and undiminished functionality with the condition the wind plant medium voltage (MV) collection network becomes DC, rather than MVAC. One dearly missed building block that would enable the transition to a DC voltage collection, is the DC/DC converter for high power & high voltage.

The main hypothesis of this thesis is that transition of MVAC connected wind turbines to MVDC (medium voltage direct current) output is conceivable with present and commercial technologies. Therefore, the main objective was investigation and development of proof of concept demonstrator for a high efficient, medium voltage (MV) converter topology, across relevant power (5 to 15 MW) and voltage range ($\pm$35 kV to $\pm$50 kV).

Research and concept demonstrators in DC/DC converters for high powers and voltages have emerged over the last decade, but none have become products yet, due to high cost, complexity or market volume.

With priority on availability, losses and power density, an analysis of a large catalogue led to favor a variant of the series resonant converter (entitled SRC#). As the DC turbine application does not require bidirectional power flow, forced commuated semiconductors on the $\pm$50 kVdc side are not required. A monolithic rectifier and transformer configuration was favoured for further robustness. With amorphous steel the transformer excitation frequency of 1 kHz was deemed achievable. Even more, at this frequency, line-frequency rectifier diodes are still feasible to use in series connected design, respecting their individual characteristics in recovery charge and recombination time, to balance losses and ratings.

During analysis, it was discovered that the transformer core size and losses could be significantly reduced by shifting the resonant inductor and capacitor to the transformer secondary, and operate the inverter (on the primary) with a modified pulse-pattern, entitled pulse removal technique. The new modulation scheme permits requlation of power from nominal level to zero, in presence of variable input and output DC voltage levels. Combination of variable switching frequency and phase-shift modulation, below

the resonant point of the LC tank, allows soft-switching commutation on all semiconductors and design of the medium frequency transformer for highest operating frequency.

Further on, substantial effort was invested to develop the analysis and design guide line tool, including a 10 kW, 5 kV laboratory test circuit. From this scaled power circuit - and simulation & design tools, the full-scale circuit performance was estimated to yield impressive 1-1.5% losses and transformer weight of less than 4 tonnes. This should be comparable to the present solution of some 2-2.5% losses and weight of 20 tones.

On a different medium voltage experimental setup, target 6.5 kV igbts and press-pack diodes have been exposed to similar voltage and current waveforms as in the target converter. The proposed soft-switching characterization setup allows generation of kilovolt and kiloamps pulses for a short time, without the need of bulky and expencive dc sources and loads. The semiconductor loss model was further validated and calibrated, while further works needs to address the validation of the monolithic transformer loss model.

Resumé

HVDC-tilsluttede vindmølleparker lover reducerede elektriske tab, lavere materielomkostninger og ufortyndet funktionalitet med den betingelse, at vindmølle spændingsnetværket bliver DC, snarere end MVAC. En meget savnet byggesten, der ville muliggøre overgangen til en DC-spændingsopsamling, er DC/DC-konverteren til høj effekt og højspænding.

Hovedopgaven af denne afhandling er, at overgangen af MVAC-tilsluttede vindmøller til MVDC-strøm (mellemspændingsstrøm) er tænkelig med nutidige og kommercielle teknologier. Derfor var hovedformålet at undersøge og udvikle bevis for konceptdemonstrator til en høj effektiv, mellemspænding (MV) konverter topologi på tværs af relevant effekt (5 til 15 MW) og spændingsområde ($\pm$35 kV til $\pm$50 kV).

Forsknings- og konceptdemonstratorer i DC/DC-omformere til høj spændinger og spændinger er opstået i løbet af det sidste årti, men ingen er blevet til produkter endnu på grund af høje omkostninger, kompleksitet eller markedsvolumen.

Med en prioritet om tilgængelighed, tab og strømtæthed førte en analyse af et stort katalog til fordel for en variant af serieresonantomformeren (med navnet SRC #). Da DC-turbineapplikationen ikke kræver tovejstrømstrøm, kræves der ingen tvungen, kommuterede halvledere på $\pm$50 kVdc-siden. En monolitisk ensretter og transformatorkonfiguration blev favoriseret for yderligere robusthed. Med amorft stål blev transformatorens eksitationsfrekvens på 1 kHz anset for opnåelig. Endnu mere, ved denne frekvens er line-frekvens ensretterdioder stadig mulige at anvende i serieforbundet design, idet de respekterer deres individuelle egenskaber ved genopretningsafgift og rekombinationstid for at balancere tab og ratings.

Under analysen blev det opdaget, at transformatorens kernestørrelse og tab kunne reduceres signifikant ved at skifte resonansspole og kondensator til transformatoren sekundært, og betjene inverteren (primært) med et modificeret pulsmønster, der har ret pulsfjernelsesteknik. Den nye modulationsplan gør det muligt at regulere strøm fra nominelt niveau til nul, i nærværelse af variable indgangs- og udgangsspændingsniveauer. Kombination af variabel koblingsfrekvens og faseforskydningsmodulering, under resonanspunk-

tet for LC-tanken, tillader soft-switching commutation på alle halvledere og design af mediumfrekvenstransformeren til højeste driftsfrekvens.

Endvidere blev der investeret betydelige anstrengelser for at udvikle analysen- og designstyringsværktøjet, herunder et 10 kW, 5 kV laboratorietestkredsløb. Fra dette målte kredsløbskredsløb - og simulerings- og designværktøjerne estimeres fuldskalaenhedens ydelse til imponerende 1-1.5% tab og transformatorvægt på mindre end 4 tons. Dette skal være sammenligneligt med den nuværende løsning på ca. 2-2.5% tab og vægt på 20 toner.

På en anden mellemspændings eksperimentelle opsætning er mål 6,5 kV igbts og press-pack diodes blevet udsat for tilsvarende spændings- og strømbølgeformer som i målkonverteren. Den foreslåede soft switching karakterisering opsætning giver mulighed for generering af kilovolt og kiloamps pulser i en kort tid, uden behov for omfangsrige og expencive DC kilder og belastninger. Halvleder tabet model blev yderligere valideret og kalibreret, mens yderligere værker skal adressere valideringen af den monolitiske transformator tabmodel.

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Preface

Foremost, I would like to thank my main supervisor, Prof. Philip Carne Kjær for giving me the opportunity to do research in the field of high power dc/dc converters, for his guidance, patience, professionalism and excellent feedback. I would also like to thank Prof. Stig Munk Nielsen and Prof. Claus Leth Bak for their feedback and help during my PhD studies. Also, my acknowledgements go to Prof. Drazen Dujic, Dr. Kazuhiro Imaie and Assoc. Prof. Michael Møller Bech for their effort, for being part of the examination committee and for the important contributions to the thesis. The financial support during my PhD study offered by the Department of Energy Technology is deeply appreciated.

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Catalin Dincan
Aalborg University, July 4, 2018

Nomenclature

ΔV	Voltage difference between V_g' and V_o
δ	Inverter legs phase displacement
γ	Normalized switching frequency
ω_r	Resonant angular frequency
ω_{sw}	Switching angular frequency
Φ	Inverter legs phase displacement in CCM mode
C_r	Resonant (tank) capacitor
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
F_r	Resonant frequency
F_{sw}	Switching frequency
$HVDC$	High voltage direct current
i_m	Transformer magnetizing current
i_{out}	Output current of the converter
i_{rp}	Primary resonant current
i_{rs}	Secondary resonant current
i_r	Rectified current
K	Constant
L_m	Transformer magnetizing inductance
L_r	Resonant (tank) inductor

$LVDC$ Low voltage direct current

M Voltage gain

$MVDC$ Medium voltage direct current

N Transformer turns ratio

P_{in} Input power

P_{out} Output power

Q Converter quality factor

q_s Resonant capacitor stored charge

SRC Series resonant converter

$SRC\#$ Series resonant converter sharp

T_r Resonant current pulse period

T_{rec} Rectifier diode reverse recovery time

T_{sw} Switching period

V_{Cr} Resonant capacitor voltage

V_g Inverter output voltage

V_g' Inverter reflected voltage on secondary

V_{in} Input voltage

V_{out} Output voltage

V_o Rectifier voltage

V_o' Rectifier voltage reflected on primary

V_t Resonant tank voltage

Z_c Resonant tank characteristic impedance

Chapter 1

Introduction

1.1 Background and motivation

1.1.1 A case for DC power collection

One of the main reason why DC power collection was not initially adopted as standard for electric power transmission and distribution was its inability to change voltage levels, meaning step-up at point of power generation for transport and step down again in the vicinity of the load. The equivalent of an ac transformer was missing and DC interrupters are inherently more difficult then AC. In the pioneering days of electro-technical development, DC power stations were able to supply customers within only a few km away from the plant, limited by the high power losses in the cables. On the other hand, the development of AC transformers, generators and polyphase induction motors facilitated the transmission of gigawatt power around the globe, powering factories and households with no storage required. This facilitated the interconnection of electric networks like Europe, China and US with more then 500 million consumers in synchronism. In the 20th century, AC has dominated the power industry for the right reasons at the time, becoming the status quo for electric power.

Moving fast forward to the 21^{st} century, the electric scenery is dramatically changed and it's no longer possible to depended on a century old and aging AC infrastructure. Power electronics technologies have started a new era, due to focus on continued improvements and higher efficiencies [1]. Classic AC energy sources (such as coal and gas power plants) will no longer dominate the energy mix, mainly due to the advent and increased shares of renewable energy. DC consumer devices (as data and computer centres, LED lighting, variable frequency drivers), high power energy storage, electric vehicles are all rapidly expanding.

In the last decade, *R&D* studies for high voltage direct current (HVDC) grids and micro DC grids have been under progress in all the major corporate research centers, universities and industries. HVDC is considered today as the optimal choice for bulk power transmission at high voltage level and over virtually unlimited distance for cables, which are limited for AC transmission systems due to reactive power loading. HVDC is the suitable solution for easy interface of asynchronous AC systems and are suited for weak AC network connection.

In the same manner, LVDC micro grid demonstrators have been built to prove their benefits and feasibility compared to AC solution. Higher efficiency, synchronization of distributed generators is not necessarily, loads are not affected by voltage disturbances and power quality is not impacted by inrush currents and single phase loads or generators.

If DC seems to be preferred at HVDC transmission and LVDC consumption, it's only logical that medium voltage direct current (MVDC) grids should

be investigated. There are a few strong arguments for this: the need of smart grid development and high penetration of distributed energy resources and energy storage favours DC connection point. Increased flexibility and reliability at a lower cost by sharing resources is offered. Synchronization between DC grids is no longer necessarily, while active and reactive power can be controlled through rapidly and independently between AC/DC or DC/DC converters and the AC grid. There is provision of reactive power support and enhanced fault ride through capability [2]. In theory, MVDC grids are the best technical solution for integration of renewable energy resources in distribution networks, as they have the benefits of higher efficiency and reliability, increase power transfer capability, while offering lower size, weight and bill of materials cost.

On the practical side, Europe's first MVDC link was recently commissioned, linking the Isle of Anglesey to North Wales AC collection grid , employing MV-VSC converters. The Angle-DC project aims to demonstrate a novel network reinforcement technique by converting an existing 33-kilovolt (kV) AC circuit to DC operation [3]. The reason of implementation was that uncontrolled power flows where putting the system at risk by exceeding thermal limits of the cables and overhead lines, while the MVDC link is expected to enable improved power flow and voltage control. Similar, commercial concepts from [4] have been introduced to the market, while offering efficient power transfer in the range of 30 MW to 150 MW.

1.1.2 HVDC wind farm with MVDC power collection

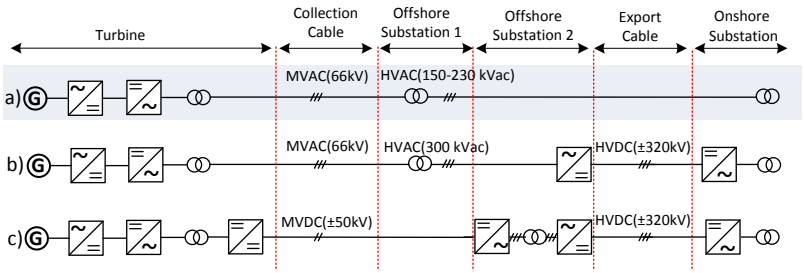


Fig. 1.1: Layouts of different configurations of electrical systems for offshore wind farms: a) MVAC collection and HVAC transport; b) MVAC collection and HVDC transmission; c) MVDC collection and HVDC transmission

A near term application of MVDC technology exists in the collector networks of large offshore wind farms with HVDC links to onshore AC grids.

The solution can offer savings on system level, only if new electrical solutions are introduced, meaning key components like the DC/DC converter: a mega-watt, high voltage, high frequency power electronic "transformer". Fig. 1.1 presents layouts of different types of electrical systems for offshore wind farms, which are: AC collection/AC transmission (1.1a), AC collection/DC transmission (1.1b) and the hypothetical DC collection/ DC transmission (1.1c).

All present onshore and offshore wind farms use an AC collection network, typically of 33kV or 66kV. Most of offshore wind farms use HVAC collection grids to transmit the energy collected from wind turbines to onshore (Fig. 1.1a). Other solutions use HVAC up to a large VSC rectifier station and then to the mainland, through high voltage DC (HVDC) transmission cables (Fig. 1.1b). But, as mentioned earlier this technique could be improved, by replacing the AC offshore collection grid with a medium voltage DC (MVDC) grid, as shown in Fig. 1.1c. It has been demonstrated in [5],[6] that wind farms could operate with higher efficiency when connected to MVDC collection grid. The motivation lays in the fact that the levelized cost of energy (LCOE) could be reduced by as much as 3%, by improving the efficiency with 2% and reducing the bill of materials (BoM) costs by at least 1%.

In a conventional offshore wind turbine,the generator output is connected through an AC/DC/AC converter, giving a constant frequency & voltage, which is elevated to 33kVac or 66kVac (medium voltage) for the collection network and secondly to 150-230 kVac (high voltage) for transmission. The MV/HV transformer is usually built on a separate platform from the offshore substation converter. Compared with AC and AC/DC layout configurations, in DC systems the line frequency transformers are replaced with high power dc/dc converters with medium frequency transformers, which could lead to significant reduction in the overall system size, weight, as well as the construction and installation cost of the wind turbines and substation platform (Fig. 1.1c). Up to this date, few active steps on realizing the paradigm shift have been implemented and there is no MVDC system commissioned for wind farms. There are no standards or design guidelines mentioning recommended MVDC levels where the system should operate and especially there are no high power DC/DC converters [1], [2]. The ambition of this work is therefore to update the state of the art and fill the gap regarding the DC/DC converter technologies.

A possible path-to-product route is illustrated in Fig. 1.2 and it proposes a series of intermediate stages within a controlled laboratory environment. An initial prof of principle needs to be selected from a myriad of DC/DC topologies and should fulfill all basic requirements regarding efficiency, power density and obtain initial characterization waveforms. To increase certainty in the design, a proof of concept at elevated voltage and power level should be

obtained increasing technology readiness level to TRL 6. At this level, the demonstrator experiments must provide results and confirm the design analysis and simulation, so confidence in the design guide line is built. Component losses and temperature rise would be characterized in a demonstrator with lower output voltage, while a 2nd demonstrator with higher voltage gain could evaluate static and dynamic voltage sharing on the rectifer side. Certainly, in both demonstrators, philosophies regarding power circulation should be discussed. The collected results will be further used to implement a third state of demonstrators, where a *thermal proof of concept* is implemented. Here the semiconductor components tested must be identical to those intended in the fully-rated product, while magnetics and capacitors are scaled down.

1.1.3 The high power DC/DC converter

The DC/DC converter for high power & high voltage (basically the equivalent of the ac transformer) is a missing building block for many applications spanning renewable energy, DC transmission & distribution, railway supply and traction. Its absence and low technology readiness level are the principle reasons of why MVDC collection networks have not been integrated on a large scale in wind farms. There are many arguments in favour of converting the wind turbine to DC output. For instance, in a wind turbine, the line frequency transformer and the DC/AC converter are replaced with a high power DC/DC converter, using a medium frequency transformer (Fig. 1.1c). This will lead to significant reduction in the overall turbine size and weight. But the area of applications for such a converter is larger: a cost efficient solution for medium voltage drives and traction, power supply to offshore oil/gas extraction platforms, grid connection of large PV plants or the replacement of large traditional power transformers with the so-called *solid state transformers.*

In the last decade, DC/DC converter research and concept demonstrators for smart grid and traction application at relevant power and voltage level have emerged, but no so many to collector networks for wind farms, which impose tougher specifications. Nevertheless, the design competence has grown, where circuit ratings, control, transformer electrical, magnetic and thermal performance have increased. It is mandatory therefore, to create a pool of knowledge that allows the design of demonstrators and should be extended to calculate the true cost and performance of the turbine DC/DC converter. Previous work has formulated many concepts for high power DC/DC converters related to DC wind turbines, but none have become products or even relevant demonstrators.

This thesis aims at increasing the technology readiness level (Fig. 1.2) for the wind turbine high power DC/DC converter, while employing existing

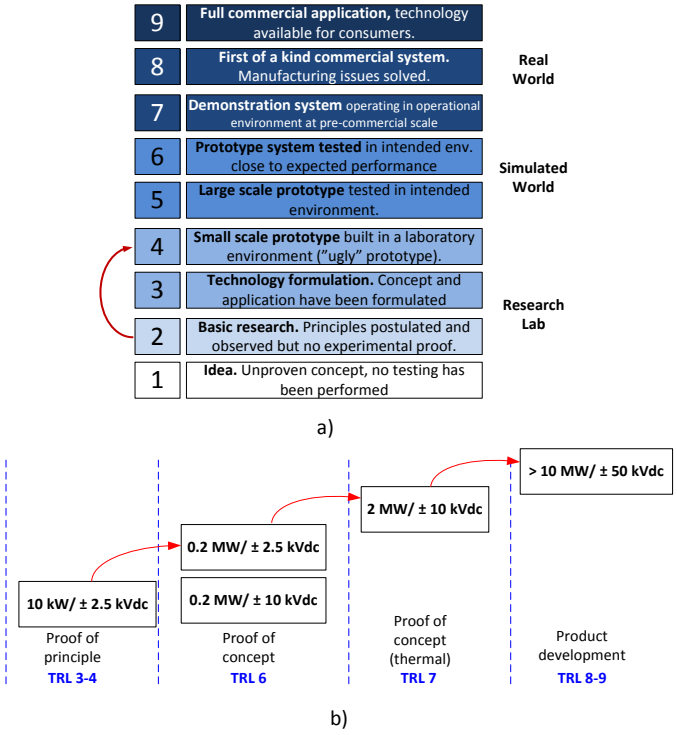


Fig. 1.2: Technology readiness level a) and path to technology b).

power electronics and transformer technology. The technologies of interest are resonant and soft-switching topologies that employ commercial silicon semiconductors and medium frequency transformers. Most of the circuit components are catalogue item-proven technology, but which where never integrated and engineered into the application of interest here. Off the shelf monolithic transformers are not available, but low loss core materials do exist as there are suppliers able to provide cores up to 2-3 MVA for line frequency distribution. Therefore a demonstration project that shows the feasibility and benefits of the comercial technology is a must to stimulate further R&D investments across the supply chain (cables, converters, transformers, control, OEMs) as many wind farm and wind turbine developers avoid the technology due to lack of low technology readiness level and field experience. The thesis suggests to bridge a proof of principle to a scaled laboratory prototype and build a foundation for future demonstrators at full ratings.

1.1.4 Terminology

The turbine DC/DC converter can be understood as a DC transformer that adapts voltages between LVDC and MVDC levels, while the substation DC/DC converter adapts voltage levels between MVDC and HVDC.

1.2 Principle hypotheses, objectives and limitations

1.2.1 Main hypotheses

The following hypotheses are formulated and their demonstration is confirmed (or infirmed) in the following chapters:

- The transition of SOA (state of the art) wind turbines to MVDC output is conceivable with present and commercial technologies, while having equal or greater efficiency and power density as compared to SOA MVAC connected wind turbines
- Low loss commutation of semiconductors at high power, medium voltage and medium frequency is achievable with soft-switching or resonant topologies
- High power density is conceivable as long as the transformer permits design for medium frequency operation (i.e losses are kep below Currie temp. point) and the semiconductors are highly utilized
- A medium frequency transformer with low core losses, suitable windings and insulation system can be designed for powers up to 15 MVA, by investigation of different core materials and structures
- Handling of medium voltage can be achieved through passive devices series connection rather than series connection of active devices or modular architecture that employs a large number of components

1.2.2 Main objectives

The main objective of this Phd thesis is to investigate and develop a proof of concept *demonstrator* for a high efficient, medium voltage (MV) converter topology, across relevant power (5 to 15 MW) and voltage range ($\pm 35kV$ to $\pm 50kV$). Expected outcome of the thesis will be:

- Survey of DC/DC converters for wind turbine and applications akin.
- Down selection of semiconductors and medium frequency transformer among multiple choices.

- Selection of suitable and later also optimal DC/DC topology.
- Analysis of selected converter topology, by means of simulation and preliminary loss investigation
- Design guide line and analysis tool for DC/DC converter.
- Build-up and testing of the prototype to validate the proposed design guide line.

1.2.3 Project Limitations

- Topologies that have ease of connection to the state of the art generators + active rectifiers will have the highest priority.
- The research on the circuits and their operation will focus only on commercially available Si-based semiconductors
- High detail design aspects of medium frequency transformer are not the main focus of the work and the outcome of the research is limited to core and windings material and layout selection, with preliminary study of losses
- Due to high costs, manufacturing time, logistics, number of researchers, complicated testing due to safety procedures, the initial demonstrator is limited to 5 kV and 100 kW, as this value allows sufficient value to extrapolate to $\pm 50kV$, $10MW$ or similar

Following areas will not be covered in the thesis and they are suggested for future work: protection schemes and strategies; isolation coordination; EMI (electromagnetic interference) impact and design of auxiliary supply.

1.3 Thesis outline

The thesis is presented as a monograph and is divided in nine chapters.

Chapter 1 - Introduction

Gives the background and motivation of this research. The main application of HVDC wind farms with MVDC power collection is introduced and it promises consistent advantages, with the key component being the DC/DC converter located in the turbines. The main objectives of the work are presented together with project limitations and a summary of the main contributions is given.

Chapter 2 - Investigation of current state of the art

Gives a review of DC wind farms, DC wind turbine concepts and DC/DC high power converters. A catalogue of circuits is organized to get a general picture of previous proposed topologies and a list of industrial and academic demonstrators is presented. The main goal is to guide towards the optimal topology.

Chapter 3 - DC/DC converter topology selection

This chapter presents the list of major challenges, list of studies to generate the nominal specifications and a methodology that helps to downsize the catalogue of circuits to only a few candidates, based on different design drivers and list of functionalities.

Chapter 4 - Series resonant converter - SRC#

Major focus is put on the applicability of the series resonant converter for DC wind turbines. General modes of operation and control methods are discussed, while a novel operating mode is introduced for a series resonant converter (entitled SRC#) with LV tank located on rectifier side.

Chapter 5 - Controller structure for SRC#

In this chapter the general structure of SRC# controller is evaluated and characteristic waveforms are presented for steady state, dynamic, fault ride through and short circuit operation.

Chapter 6 - Sensitivity studies of SRC#

LC tank, transformer and rectifier sensitivity studies are discussed. The selection of LC tank parameters has the strongest impact on delivered nominal power, peak current and voltage values, which impact the circuit ratings. Transformer magnetizing inductance has to be carefully selected and it is shown what impact it has on transformer size, semiconductor losses and primary resonant current waveforms. Discussions about rectifier voltage balancing across the series connected diodes are shown, while the impact of snubber/parallel RC circuit and valve stray parameters are presented.

Chapter 7 - Design guide line for SRC#

This chapter is showing a design guide line for the SRC# suitable for megawatt, kilovolt and kilohertz range. A general step by step methodology is illustrated and design example for a 10 MW specification is presented.

Chapter 8 - Experimental work

Shows two different experimental setups built during this research and a description and test method of each circuit is presented.

Chapter 9 - Conclusions and future work

This final chapter summarizes the performed work during this thesis and shows final conclusions and discusses future work.

1.4 List of publications

Certain parts of this PhD Thesis have been published or will be published in international scientific journals, conference proceedings, tutorials or are contained in patent applications. The list of publications is shown below:

Journal papers

- C. Dincan, P. C. Kjaer, Y. Chen, S.M. Nielsen, C. L. Bak, "Analysis of a high power, resonant DC-DC converter for DC wind turbines", IEEE Trans. Power Electron. and Appl, Nov. 2017 (early access). DOI: 10.1109/TPEL.2017.2770322.
- C. Dincan, P. C. Kjaer, Y. Chen, S.M. Nielsen, C. L. Bak, "High power, medium voltage, series resonant converter for DC wind turbines", IEEE Trans. Power Electron. and Appl, Nov. 2017 (early access). DOI: 10.1109/TPEL.2017.2770220.
- C. Dincan, P. C. Kjaer, Y. Chen, S.M. Nielsen, C. L. Bak, E. Sarra, V. Sriram,"Design of a high power, resonant converter for DC wind turbines", IEEE Trans. Power Electron. and Appl, under review.
- A. Tonellotto, E. Maccia, C. Dincan, P. Kjaer, S.M. Nielsen, C.L. Bak, "Control aspects for a high power, resonant converter for wind turbines", IEEE Trans. Power Electron. and Appl, under review.

Conference papers

- C. Dincan, P. Kjaer, S.M. Nielsen, C.L. Bak, " Soft-switching characterization of medium-voltage IGBT power modules and press-pack diodes in a 1 kHz mega-watt dc/dc resonant converter", Proc. IEEE Eur. Conf. Pow. Electron. and Appl. (EPE2018), under review
- C. Dincan, P. C. Kjaer, Y. Chen, S.M. Nielsen, C. L. Bak, "Analysis and design of a series resonant converter with wide operating range and

minimized transformer ratings", Proc. IEEE Eur. Conf. Pow. Electron. and Appl. (EPE2017), Sept. 2017. DOI: 10.23919/EPE17 ECCEEurope.2017.8099407

- C. Dincan, P. C. Kjaer, Y. Chen, S.M. Nielsen, C. L. Bak, "Selection of DC/DC converter for offshore wind farm with MVDC power collection", Proc. IEEE Eur. Conf. Pow. Electron. and Appl. (EPE2017), Sept. 2017. DOI: 10.23919/EPE17ECCEEurope.2017.8099408
- C. Dincan, P. C. Kjaer, Y. Chen, S.M. Nielsen, C. L. Bak, "Establishment of functional requirements to DC-connected wind turbine and their use in concept selection", Proc. IEEE Int. Conf. on DC Micro. (ICDCM), Jun. 2017. DOI: 10.1109/ICDCM.2017.8001021
- C. Dincan, P. C. Kjaer,"Characterization of diode valve in medium voltage dc/dc converter for wind turbines", Proc. IEEE Eur. Conf. Pow. Electron. and Appl. (EPE2016), Sept. 2016. DOI: 10.1109/EPE.2016.7695404.
- C. Dincan, P. C. Kjaer,"Control and modulation for loss minimization for dc/dc converter for wind turbines", Proc. PCIM, May. 2016.

Patent application

- C. Dincan, P. C. Kjaer, "DC-DC Converter and DC-DC conversion method". European Pat. Appli., no. 70059, Filed March. 2017.

Chapter 2

Investigation of current state of the art

Summary

This chapter presents an overview of DC wind farms configurations and DC wind turbine concepts. Afterwards, a catalogue of DC/DC converter topologies is built, categorizing the topologies from switching and isolation type. A survey of university and industrial demonstrators is presented and it illustrates the challenges, specifications and functionalities that the dc/dc converter located in the wind turbine will experience. The end goal of the chapter is to guide toward the optimal topology.

2.1 An overview of DC wind farms configurations

An overview of DC wind farms configurations is illustrated in Fig. 2.1. As discussed in [7] and [5], DC collector grids offer advantages regarding efficiency and investment costs. The DC collector grid layout can be realized through a two conversion stage (Fig. 2.1a) or a single conversion stage concept (Fig. 2.1b). In the two stage concept, the output of the turbine's active rectifier (responsible with the control of generator's power) is increased to medium voltage level, with the help of the dc/dc converter. Outside the turbine, power is collected and stepped up a second time through an offshore substation converter to HVDC level. The single stage concept assumes there is no LVDC/MVDC turbine dc/dc converter, and power is collected at a considerably lower medium voltage level (determined directly by the generator's nominal voltage level) and further stepped-up by substation converter to transmission level. The main disadvantages are increased collection network losses, due to higher currents and increased cables' diameter. The third farm layout (Fig. 2.1c) proposes turbine located dc/dc converters that step up voltage to medium voltage level close to transmission level ($\pm 100kV_{dc}$) and direct to on shore connection. The solution has the advantage of not requiring an offshore substation converter, but according to [8], the layout will have higher losses compared to the previous two for larger wind farms. The solution would be optimal for small size offshore wind farms and located close to the shore. The forth wind farm layout, discussed in [9]–[11] proposes a radical solution, where in order to reach high voltage transmission levels, without the need of an offshore substation and even no medium voltage turbine converter, it proposes series connection of the wind turbine output converter poles. The concept has been proposed in the early 2000's but presents technical challenges and risks. From technical point, efficiency and easiness of advancing the state of the art, the two stage concept is chosen as the main frame work of this research work.

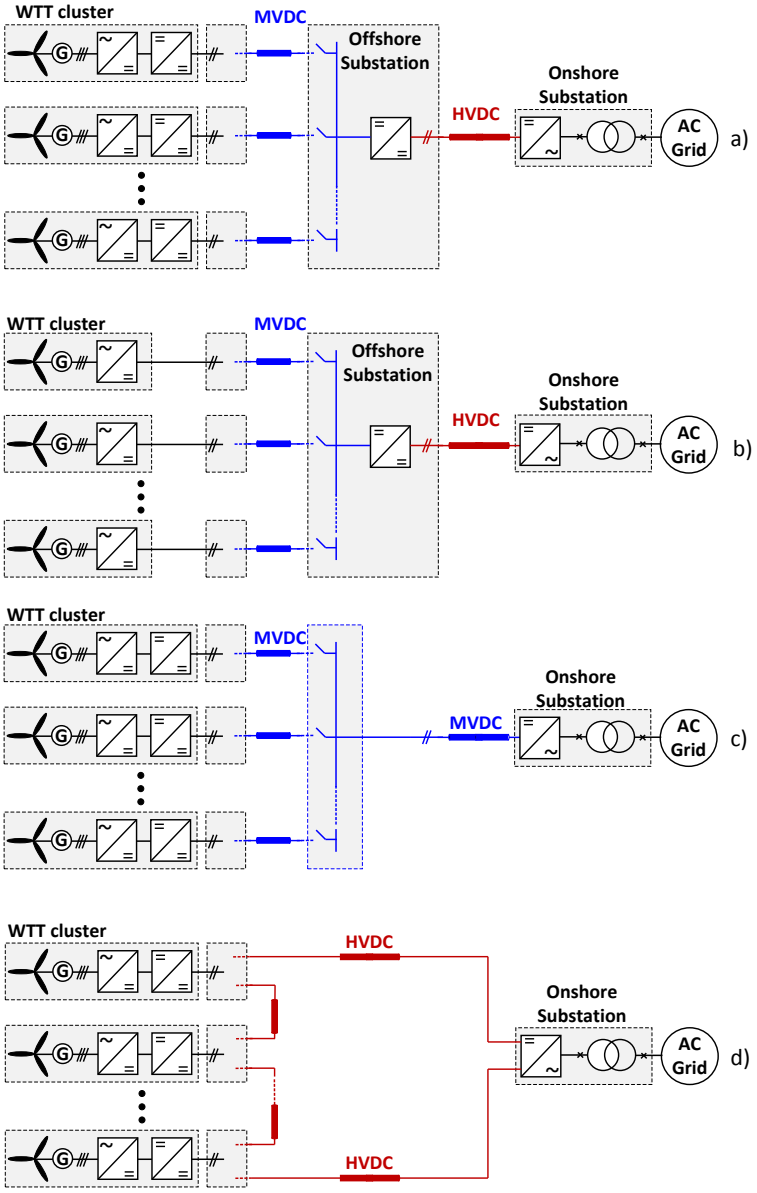


Fig. 2.1: Overview of dc wind farms configurations: a) Turbine with dc/dc converter, MVDC collection and HVDC transmission - two conversion stage concept; b) Turbine with no dc/dc converter, lower MVDC offshore substation and HVDC transmission - one stage concept; c) direct to shore MVDC transmission; d) Series connected wind turbines with HVDC transmission.

2.2 An overview of DC wind turbine concepts

Assuming that state of the art generators are employed, a number of dc wind turbines concepts classified by the number of power electronic stages was identified and shown in Fig. 2.14. This categorization is not considering modular generators [12] and series connected converters as in [13], even if the proposed solutions have some interesting advantages. The first concept (Fig. 2.14a), employing only 1 stage, that of an active rectifer was presented in [14] and has the advantage of low number of components and simplicity. The problem is that maximum output voltage is limited to the generator's nominal voltage level and it has no galvanic separation. Therefore, concept from Fig. 2.14b (presented in [15]) could alleviate this issue, by simply adding non-isolated dc/dc converter, to step up to medium voltage level. Another 2 stage concept ((Fig. 2.14c and presented in [16] suggests a low frequency transformer followed by a passive rectifier. Simplicity and low number of components are advantages, but fixed speed operation and transformer saturation risks are main disadvantages. Another interesting concept, composed of 3 stages ((Fig. 2.14d) was proposed by [9], [17] and employs a matrix converter (AC/AC). Another 3 stage concept (Fig. 2.14e), aims at limiting the disadvantages of (Fig. 2.14c), by incorporating a series connected front to front converter. Further on, a 4 stage concept (Fig.2.14f) that reuses the AC turbine's generator and active rectifie, followed by an isolated high power dc/dc converter. This approach would imply that the main research focus should be on the dc/dc converter, while the rest of components are off the shelf and present low technology risk. It also presents the lowest impact on AC turbine design to turn it into DC turbine. For these reasons it will be the main frame work of this research. A final turbine concept, with 5 converter stages (Fig. 2.14g) incorporates a boost converter between the active rectifier and the isolated dc/dc converter. The topology was suggested in [18], and it assumes that the boost converter is actively controlling the LV side DC link, while the DC/DC converter is operated in open loop in the manner of a DC/DC transformer.

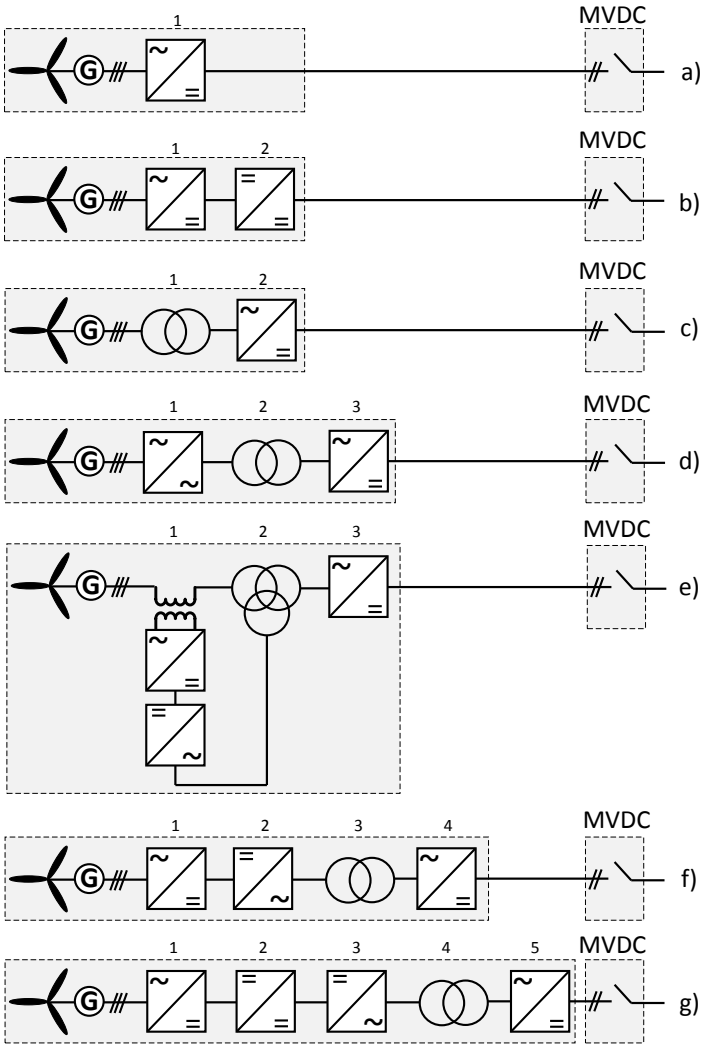


Fig. 2.2: Catalogue of dc wind turbine concepts: a) 1 stage concept with only active rectifier, no galvanic separation; b) 2 stage concept witch active rectifier and non-isolated dc/dc converter; c) 2 stage concept with transformer and passive rectifier; d) 3 stage concept with matrix converter, MF transformer and passive rectifier; e) 3 stage concept with V/Hz controller, medium frequency transformer and passive rectifer; f) 4 stage concept with active rectifier and galvanic isolated dc/dc converter; g) 5 stage concept employing a boost converter between the active rectifier and galvanic isolated dc/dc converter;

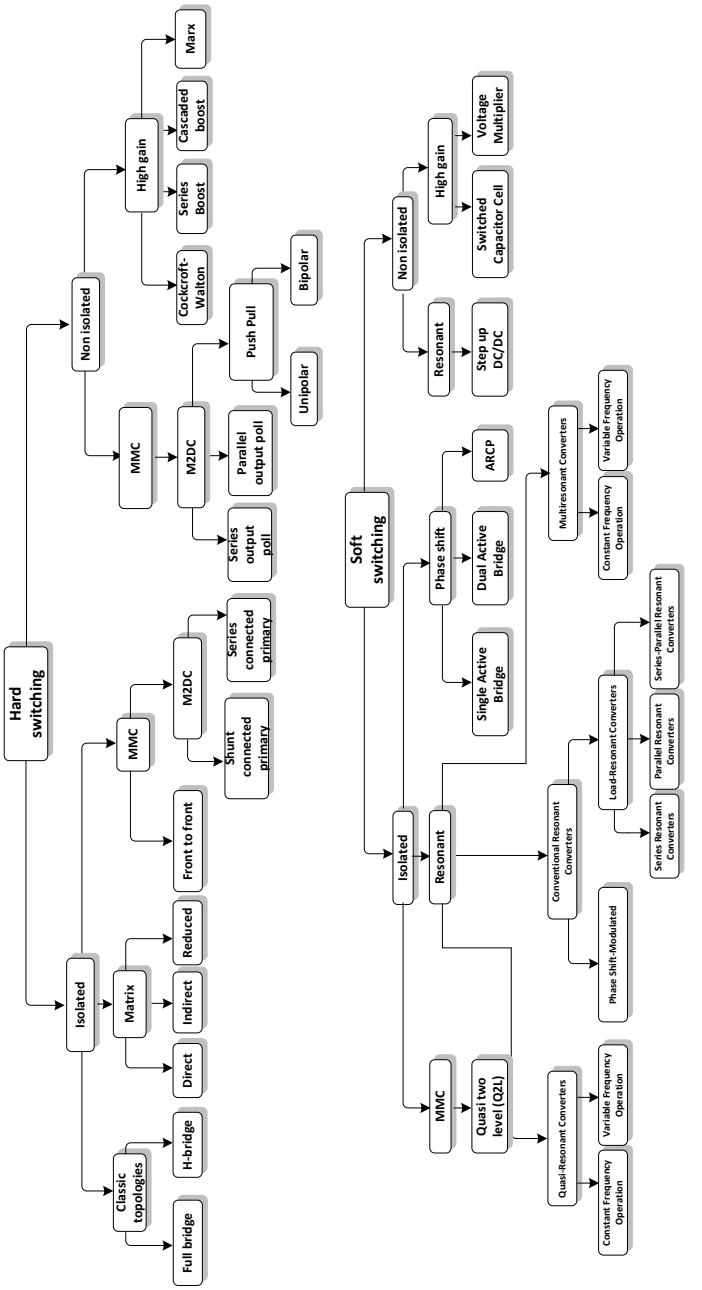


Fig. 2.3: Family tree of hard and soft-switching DC/DC converter topologies

2.3 A survey of DC/DC converter topologies

A multitude of DC/DC converter topologies exists, the vast majority being applied for low voltage and low power applications. Up to this point, there are no commercial high power, high voltage DC/DC converters. Nonetheless, corporate research centers, industry and universities have put effort in the last decade in research and demonstration of high power dc/dc converters and a few concepts have been proposed. A simple family tree illustrating the surveyed topologies and organized from switching point of view (hard vs. soft) and galvanic separation (isolated vs. non-isolated) is shown in Fig. 2.3.

2.3.1 Hard-switching topologies

Isolated: Half bridge and full bridge converter

The classic half and full bridge VSC-converter (2-level or 3-level) (Fig. 2.4) would be the most simple circuitry to be implemented: compared to the AC solution, they require the addition of a passive rectifier and MV-DC link stage. The topologies were investigated in a DC collection grid study in [6] and operation at constant frequency and variable duty cycle was employed. Compared to soft-switching topologies, they require no addition of inverter snubber components, with the penalty of hard-switching losses, turn-off voltage overshoot and high transformer dv/dt. Switching frequency and transformer design are limited, as stray parameters increase linearly with frequency, leading to oversized number of semiconductors only to accomodate voltage overshoots.

Isolated: Matrix converter

In order to remove the LV side DC-link capacitors, thus decreasing the number of stages, different AC/AC matrix topologies have been investigated in [9], [11], [19], [17] and [20] with the advantages of decreased cost, weight and volume compared to classic back-to-back topologies. In general, matrix topologies have been studied in applications that require small size and high reliability, such as motor drives, aircrafts, marine propulsion and lately offshore wind farms [9]. In [20], a multi-objective design of a modular power converter for DC wind turbines was performed. The direct matrix converter (Fig. 2.4c) is a direct three phase AC-AC converter that does not incorporate DC link capacitors. The indirect matrix converter (Fig. 2.4d) has a DC-link stage, but no capacitors. In both cases, a clamp circuit is required due to the lack of a natural freewheeling path like in the case of classic back-to-back topology. Bidirectional switches are employed in both converter types. Unlike these conventional matrix topologies, the reduced matrix converter was

analysed in [9] and the proposed topology is able to convert three-phase AC into a single phase AC. Also in this case, bidirectional switches with two reverse blocking IGBTs and without additional diodes are required.

The main advantages of incorporating a matrix topology are one less conversion stage, low switching losses and presumably a smaller transformer due to higher frequency.

According to the study from [17], compared to the conventional AC/DC/AC converter, it was found that for the range of transformer frequencies from 1 kHz to 20 kHz, the reduced matrix topology has the highest efficiency and the highest power density. On the other, the topology requires additional components for protection against overvoltages that might be destructive for semiconductors.

Isolated: Front to front modular multilevel converter

The modular multilevel converter (MMC) is commercially productified for HVC transmission converters and MV stations, being interfaced with the AC grid, where two MMC are connected at their DC transmission lines. Galvanic isolation and voltage step-up and step-down is performed through a power frequency (50 Hz/60 Hz) transformer. The conventional Modular Multilevel Converter (MMC, also known as M2C or M2LC) was proposed in a DC/DC configuration in [21]–[24], while incorporating a transformer designed for higher frequency and with the ability of handling short-circuit at the input and output without the need of additional DC or AC circuit breakers for protection. A three-phase solution is suggested in Fig. 2.5a.

A general conclusion of [21] was that the efficiency of the modulation method cannot be drawn because it depends on converter configuration, and depending on the nominal submodule voltage, different switches have to be chosen and this influences the loss calculation. Efficiencies higher than 98% (at 1 kHz) are achievable. On the other hand, the capacitors will occupy large fraction of the volume, motivating the use of the modular converter system for high voltage, high power specifications, such as the offshore substation converter. The large number of submodules will lead to an increase in power circuit and control complexity.

Isolated: M2DC - Shunt and series connected primary

Two other isolated-unidirectional variants of M2DC are shown in Fig. 2.5b and c, namely the Isolated Shunt connected primary and Isolated Series connected primary, both investigated in [25]. The topologies were introduced for HVDC interconnection links such as taps (defined as the interface between HVDC transmission line and local MVAC network) to inject/extract relatively small amounts of power. With the inclusion of a transformer and

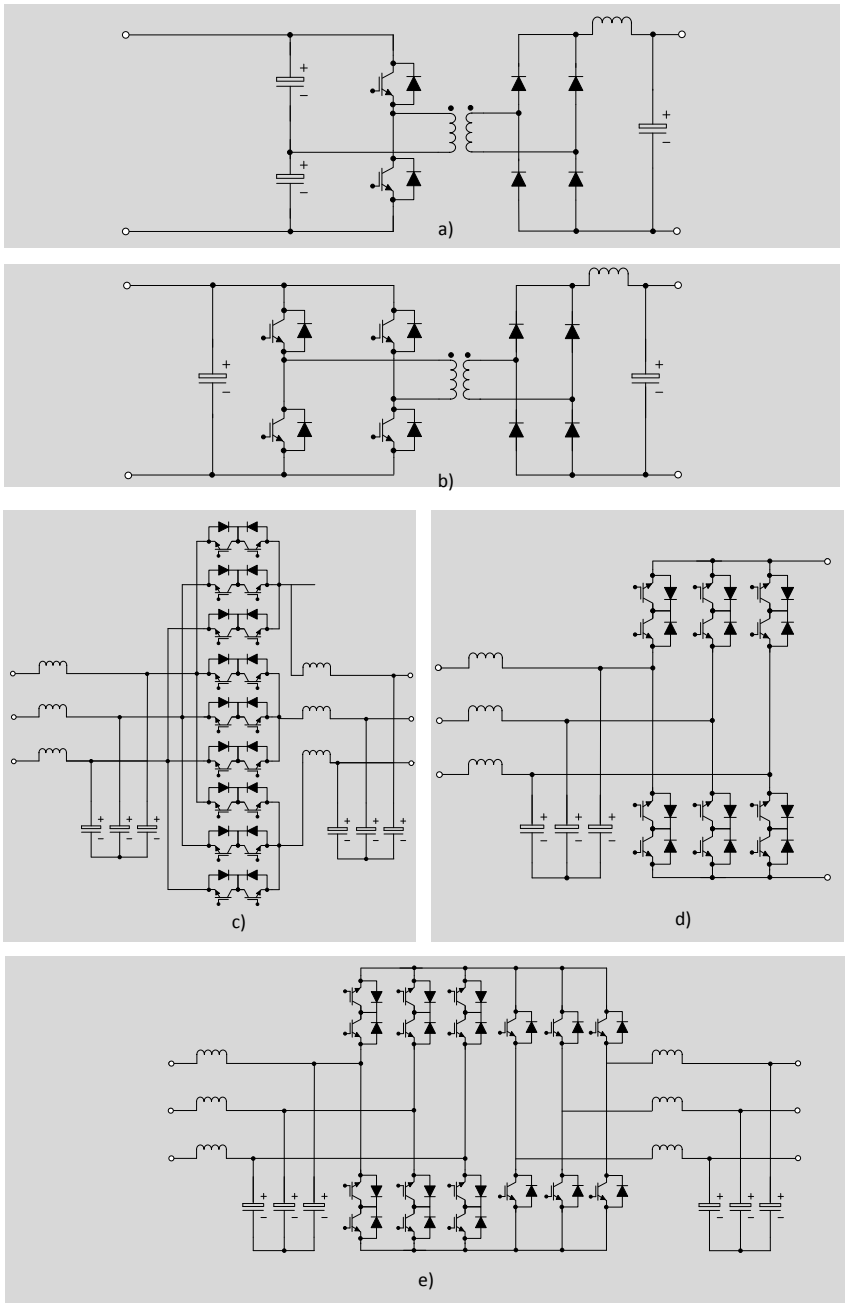


Fig. 2.4: Hard switching DC/DC converter topologies: a) Half bridge ; b) Full bridge; c) Direct matrix; d) Reduced matrix; e) Indirect matrix

square wave operation, taps with high voltage transformation ratios (such as 500 kV to 50 kV)are achievable. The circuit from Fig. 2.5b consists of a single phase leg with the transformer's primary connected between its midpoint and the midpoint of the split DC link capacitors. The Architecture from Fig. 2.5c is a variation of the shunt connected primary, where the transformer primary is connected between two arms and left floating. Other advantages worthy to mention are fault limitation due to galvanic separation, and AC frequency can be optimized to achieve a trade off between transformer size and switching losses.

Non-isolated: M2DC - Series Output pole and Parallel output pole

Two direct architectures of modular DC/DC converters for HVDC use were studied in [24] and are identified in Fig. 2.5d and e as the series output pole and the parallel output pole. The first topology consists of two phase legs connected in series with each other, while the midpoint of each phase leg connects to a lower DC voltage terminal. The parallel output pole architecture is seen as a DC version of the MMC, where each terminal of the lower DC voltage side is connected to the midpoint of a phase leg consisting of two arms. Because the cell arm has to provide the full DC step, the circuits suffer from an energy drift and require an internal AC rebalancing current to be circulated. The circuits have a poor capacity factor and are suitable for voltage gains up to 2:1, meaning they are more suitable for connecting HVDC links of adjacent voltage level.

Non-isolated: M2DC - Non-isolated Unipolar Push Pull

The M2DC - A non-isolated unipolar push pull topology was first introduced in [26], [27] and it is illustrated in Fig. 2.5f. The converter consists of four converter arms and two coupled inductors. The circuit was investigated in [28] for MVDC to HVDC connections and it was concluded that it requires a large number of semiconductors. Also, it was considered not to be suitable for high voltage ratios, as the circulating current in the converter becomes high, results in a poor efficiency of 95%. On the other hand, if primary and secondary voltages differ only by a few percent and no galvanic isolation is required, the maximum efficiency exceeds 99%.

Non-isolated: Cockcroft Walton

The Cockcroft Walton circuit from Fig. 2.6a is another topology suitable to achieve high voltage DC gains, while offering low weight and volume [29]. It has a simple control, simple structure, it can employ only diodes and it can offer ripple cancellation with symmetrical and double ladder. The topology

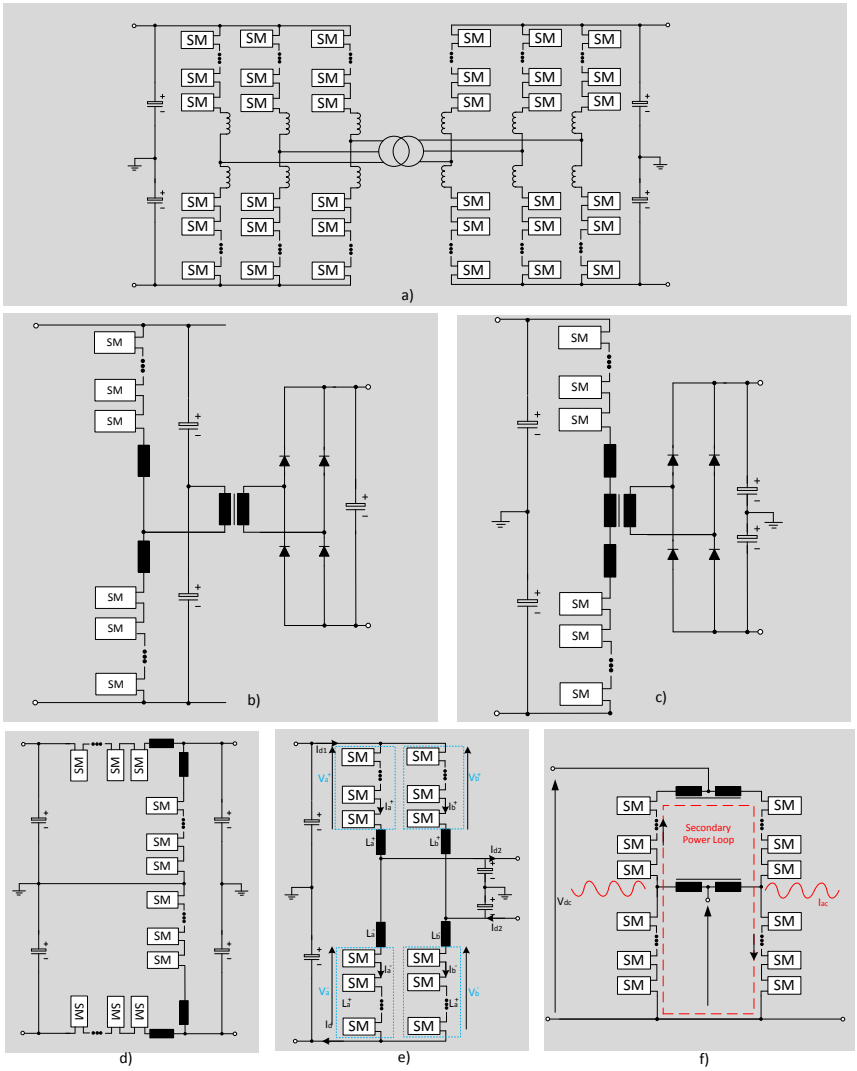


Fig. 2.5: MMC topologies: a) Isolated Front to front; b) M2SC Isolated Shunt connected primary; c) M2DC Isolated Series connected primary; d) M2DC Non-isolated Series output pole; e) M2DC Non-isolated Parallel output pole; f) M2DC Non-isolated Unipolar Push Pull

is suitable for high voltage and low power applications and has the disadvantages of poor voltage regulation and no galvanic separation.

Non-isolated: Cascaded and series boost converter

A multiple module high-gain and high-voltage DC-DC topology was proposed in [30] for offshore wind energy systems under the form of cascaded and series boost converter (Fig. 2.6b and c). Results for a low voltage-experimental prototype showed gains of up to 29 p.u. The cascaded configuration connects the output of the first boost converter to the input of the second one, while each converter is rated for the full input power. There are indeed potential for large gains due to the multiplicative effect, but the efficiency losses compound quickly for the same reason. Among other practical issues, the cascaded converter's components suffer from intermediate voltage stress and large current stresses. Control becomes difficult due to the interaction between the converters. The series boost converter configuration connects the input of the converter in parallel and the outputs in series. Both types were investigated for a theoretical 1 MW wind turbine with $1kV$ and boosted to 132 kV for HVDC transmission. The main issues are that due to the large switch duty ratio, required to achieve high voltage gain, and due to low switching frequency, conductions losses are high and size of passives is not decreased compared to low frequency magnetics. As every cell must be rated for entire output voltage and a fraction of input current, selection of semiconductor devices is not a straight-forward process.

Non-isolated: Marx converter

A variation of the Marx converter (Fig. 2.6d) was presented in [31], for a high-power application. The topology used IGBTs and diodes and was compared to the conventional boost converter. The main principle is based on charging capacitors in parallel followed by reconnection in series to create higher voltage. Output voltage regulation, high voltage stress and large number of semiconductors and passives are some of disadvantages that don't favour this choice of circuit.

2.3.2 Soft-switching topologies

Isolated: Phase-shift single active bridge

The single active bridge (single and three phase 2 level variant) are depicted in Fig. 2.7a and b. The three phase variant has been initially discussed in [5] and the small signal analysis was performed in [32]. The three phase variant has a simple mode of operation, meaning constant frequency operation, and 120 deg phase shift between each phase leg. The transformer windings will

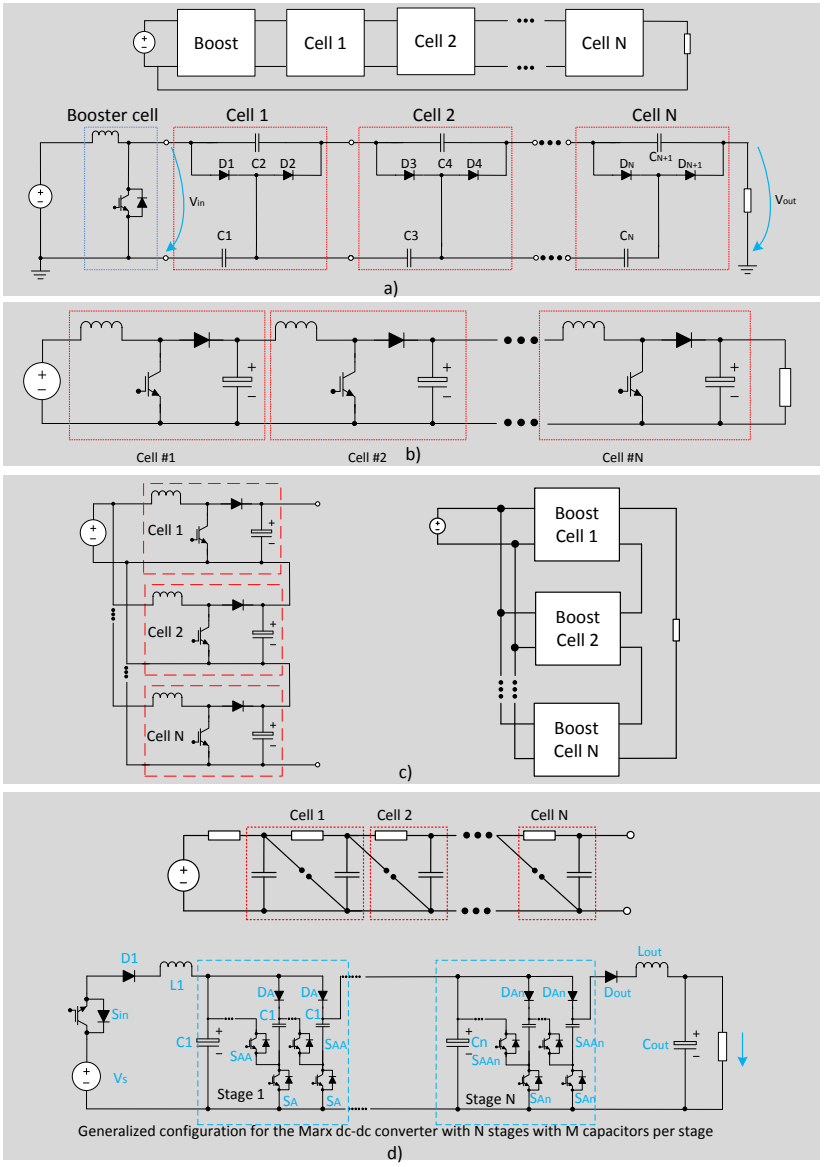


Fig. 2.6: Hard switching high gain topologies; a) Cockcroft Walton; b) Cascaded boost; c) Series boost; d) Marx converter

experience a square wave excitation and due to the presence of stray inductance or an individual series connected inductance, a phase shift between the primary and secondary windings will occur. A single phase interleaved variant was proposed in [33], [34], leading to lower current and voltage ripple on input and output side dc-link capacitors. According to [5] one disadvantage of the topology, is that it requires a very small stray inductance to transfer a large amount of power, leading to technical constraints on the transformer design. F.ex., to deliver a power level of 20 MVA, the total stray inductance should be below 0.1% of magnetizing inductance, which is hard to achieve in practice for a high power transformer. The topology exhibits a limited zero voltage switching (ZVS) range for the IGBT transistors and high turn-off currents for the rectifier diodes, leading to high losses due to reverse recovery.

Isolated: Phase-shift dual active bridge

To improve the drawbacks of the single active bridge, the dual active bridge is further discussed in [5], [35] and illustrated in Fig. 2.7c and d. The topology was initially introduced by [36] for aerospace application. Since then, the concept has gained wide acceptance, especially for high power applications, related to traction, solid-state transformer and commercial EV battery chargers. It consists of two full bridge converters and a medium frequency transformer with a turns ratio of 1:1. As explained in [7], both bridges are modulated in six-step voltage at the transformer terminals. The phase shift α between the input and output bridge voltages results in a voltage difference across the leakage inductance of the transformer. As the topology is able to achieve soft-switching at turn-on for the active semiconductors for a certain operating range (which can be increased by adding snubbers), it promises increased efficiency and the possibility of employing a three phase medium frequency transformer. To extend the soft-switching boundaries, the auxiliary resonant-commutated poles (ARCP) can be applied, as seen in Fig. 2.7. The auxiliary devices are rated for a fraction of the nominal power and are operated during hard-switching operational points, at low power ratings or unegual dc voltages [7].

Isolated: Resonant topologies

Resonant topologies get their name from the LC tank or variations of it, which is positioned on the inverter or rectifer side, depending on the application. Among the first to discuss resonant converters was [37] and it proposed an improved method of resonant current pulse modulation for power converters. Due to small size and high efficiency requirements for aerospace application, the interest in the philosophy of resonant topologies gained a lot of attention especially in the 80's. Nowadays, resonant converters find applications in a

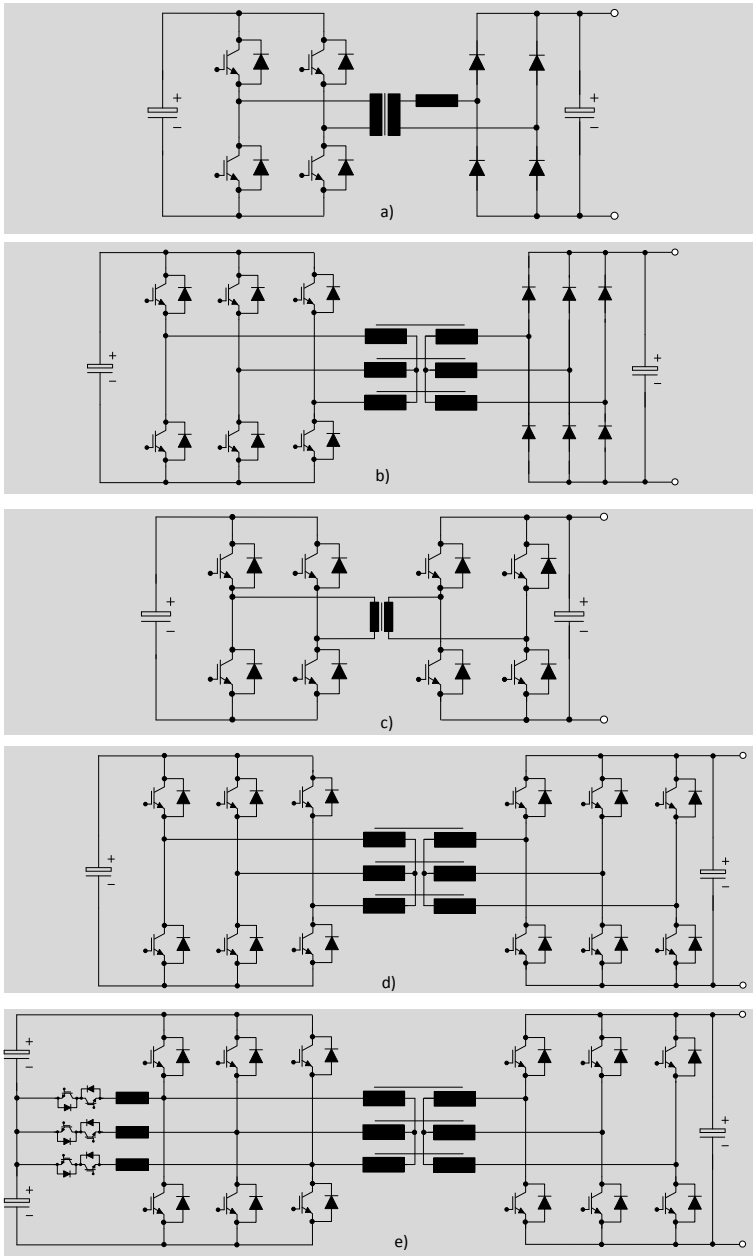


Fig. 2.7: Soft switching topologies: a) Phase shift single active bridge; b) Phase shift three phase active bridge; c) Single phase dual active bridge; d) Three phase dual active bridge; e) ARCP dual active bridge

range of exotic fields, like CO_2 lasers, radars, high voltage applications such as x-ray generators or electrostatic precipitators [38]. In order to reduce the size and volume of power supplies, one has to increase the switching frequency to reduce the size of magnetics and capacitors. At the same time, efficiency should remain high, by limiting the switching losses [39]. Further on, the topologies seem to be very well suited also for high-voltage applications, as they can incorporate the transformer non-idealities in the resonant tank [40]. This characteristic is usefull for high voltage applications, as the transformer non-idealities are dependent to the turns ratio. In classic hard-switch topologies, the transformer leakage inductance will lead to undesirable voltage spikes, while the winding capacitance will create current overshoots and slow rise time. Fig. 2.8 illustrates a number of resonant topology variants. Fig. 2.8a presents a three phase series resonant topology, investigated in [41], [42], while being operated at the resonant point. Amongst others, the solution offers in theory, ZVS at turn on and ZCS at turn-off, while limiting the input and output current ripple, due to three-phase operation. The single phase series resonant converter (Fig. 2.8a) has a wide range of applications, from telecommunications power supply, LED drivers and high voltage devices. Recently, the concept has attracted a lot of attention, especially for traction and solid-state transformers, where it is operated below resonant point, at constant frequency and it is called half-cycle discontinuous current mode (HC-DCM) SRC. Based on LC tank variations in configuration, the single phase parallel resonant converter (Fig. 2.8c), LCC converter (Fig. 2.8d) and LLC (Fig. 2.8e) can be formed. The parallel resonant converter has the ability to both step up and step down the DC voltage, exhibiting current-source characteristics near resonant point. One of the principle advantages are protection against short circuit current, but it suffers from high device current stress which is not load dependent. The series parallel resonant DC/DC converter in a LCC variant was proposed as a high voltage, low power topology for medical application in [38]. The LLC resonant topology has also been investigated for high-power application and proposed in traction application [43] It has the advantage of decreasing turn-off losses for IGBTs, while offering ZVS at turn-on, due to the incorporation of the magnetizing current in the resonant current waveform.

Non-isolated: High gain topologies

According to [44] and [15], the design of medium frequency transformers is not a trivial task, especially for large turns ratio, high cost of the magnetic core and dieletric losses. A number of soft-switching, non-isolated topologies that exhibit high gain characteristics are displayed in Fig. 2.9. A thyristor based topology, with similar characteristic of the parallel resonant converter is depicted in a single and three phase variant in Fig. 2.9 and is capable

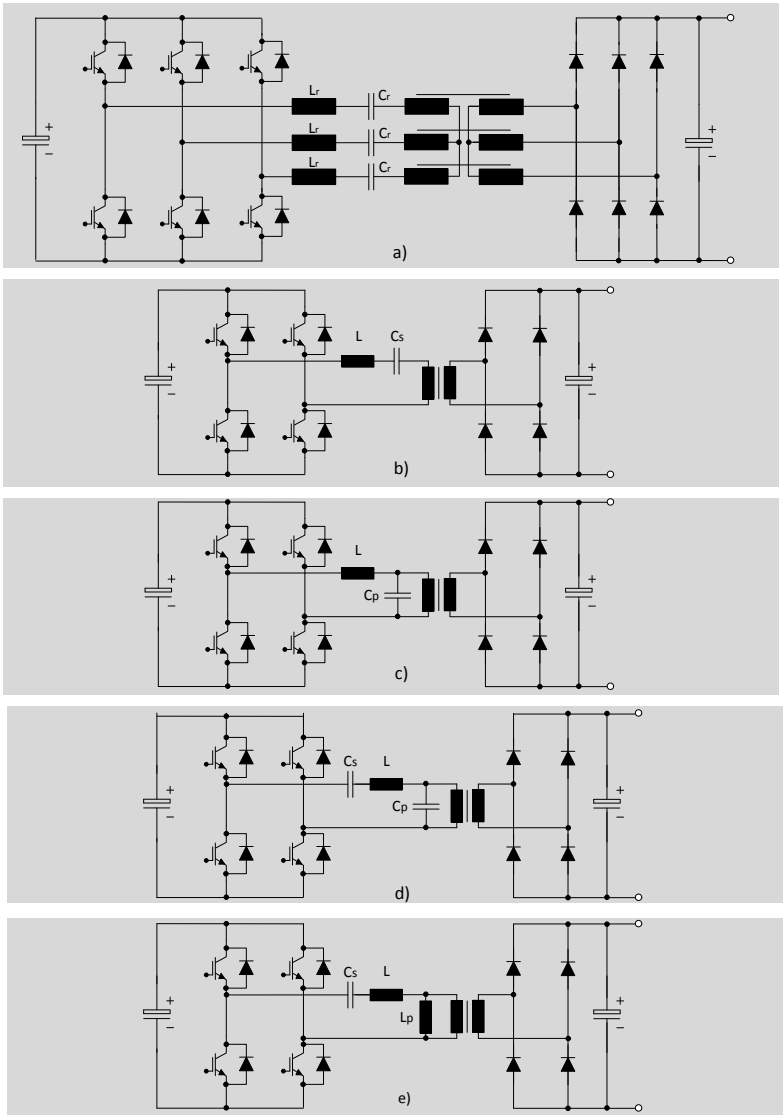


Fig. 2.8: Resonant topologies: a) Three phase series resonant converter; b) Single phase series resonant converter; c) Single phase parallel resonant converter; d) Single phase LCC converter; e) Single phase LLC converter.

of achieving very high step-up gains in voltage with megawatt level power transfers. Amongst simplicity and use of cheap and robust thyristors, it is also able to achieve soft-switching operation for e certain range. The circuit is operated with variable frequency control, but it has drawbacks such as high conduction losses and a high peak to peak voltage across the passive components. Switched capacitor or capacitor clamped DC/DC converters have attracted attention in the field of high power dc/dc converters, due to lack of a medium frequency transformer, high power density and control simplicity. Different cells topologies are depicted in Fig. 2.9c and d.

In Fig. 2.9e, a modular zero current switching resonant switched capacitor (ZCS RSC) is presented and its operational aspects are covered in [45]. The authors claim soft-switching characteristics for all switches and diodes, and a 24 kV, 17-level step up converter was built, with switching frequency of 8 kHz.

Another high gain RSC topology is shown in Fig. 2.9f and it's discussed in [44], [46], claiming improvements compared to the previously mentioned topology.

2.4 A survey of DC/DC converter demonstrators and technologies

A catalogue of circuits was presented in previous sub-chapters. To further down select to a few topologies and increase the confidence towards the optimal choice of topology, a survey of DC/DC converter demonstrators and technologies is necessary. The main interest is to understand which challenge appeared during design, integration and development of prototypes. Topics like topologies, semiconductors, magnetics or cooling are investigated.

During the process of survey, focus was mainly on assembled and tested high power medium voltage demonstrators, listed in Table. 2.1. Most of the relevant work was done on traction applications, with maximum power tested up to 1.2 MW (15 kV, 1750 Hz) [47], [48], while on medium voltage distribution SST (solid state transformer that replaces 50Hz/60Hz power transformer), valuable work is performed by [49], [50]. A 5 MW (5 kV, 1kHz) demonstrator was built on a three phase converter, and operating record was presented for a single phase 2.2 MW setup.

Regarding operating record for SST application, a number of university and industry demonstrators was presented: [51]–[53]. On the other hand, for DC offshore wind turbine applications, as expected, there is not so much practical work reported. There are indeed many proof of concept demonstrators of scaled power and voltage [5], [9], [21], [35], [54], [55], but there are no setups tested and assembled at powers beyond 100 kW. Most of the experimental work is focused on functionality assessment of different topologies

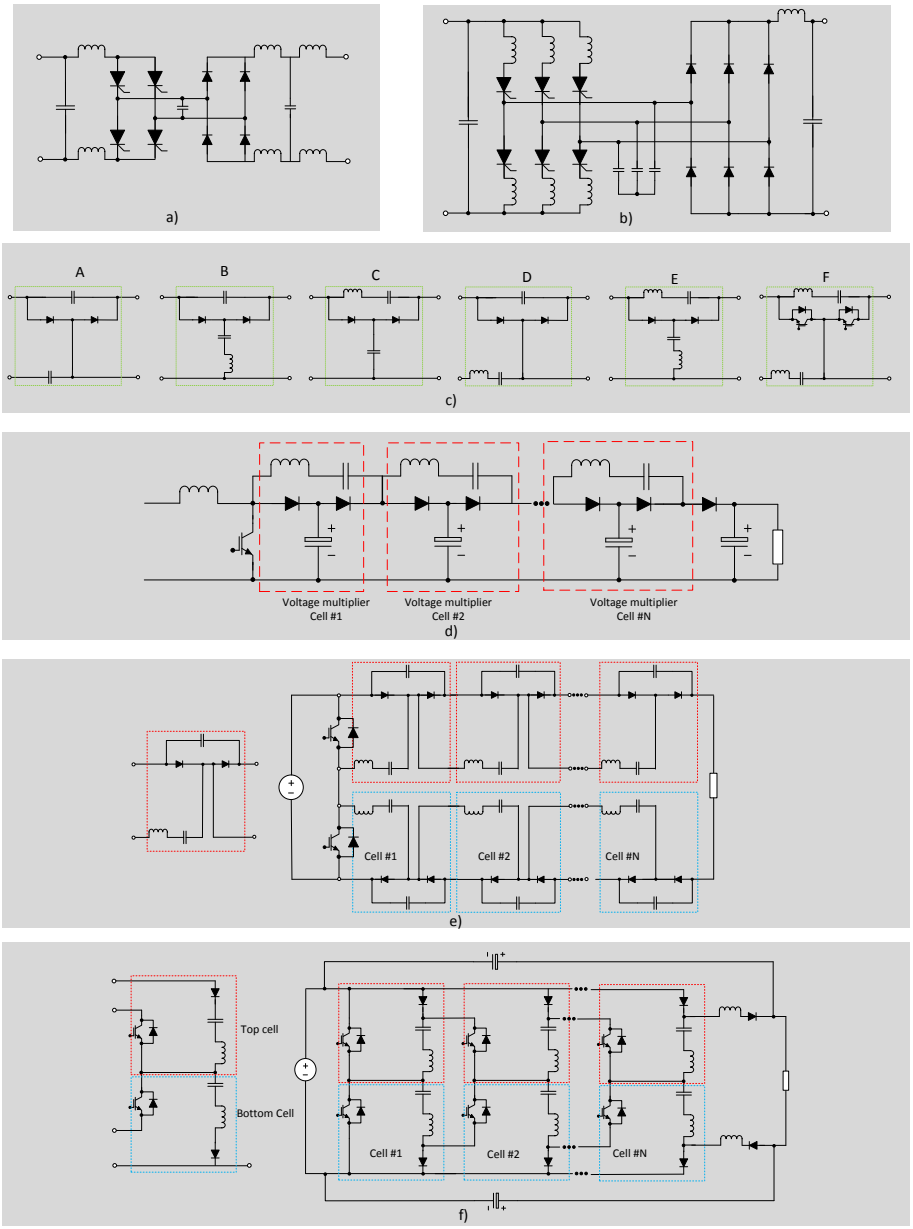


Fig. 2.9: Soft switching high gain topologies: a) Jovcic 1 phase high gain converter; b) Jovcic 3 phase high gain converter; c) Switched capacitor cells; d) Boost topology with voltage multiplier; e) ZCS RSC (zero current switching resonant switched capacitor; f) High gain RSC

and concepts, and some on efficiency and performance. Common challenges, output voltage, switching frequency and nominal power of studied demonstrators is shown in Fig. 2.10a, b and c.

One obvious conclusion is that different applications require different specifications, merely because of different requirements regarding availability, dimensions, climate, service, repairability or maintenance. In traction, the DC/DC converters will be connected to two different kind of single phase grids: 16 kV, 25 kV or 36 kV while the power range might goes up to 5-10 MW. A similar set of specifications is expected for medium voltage SSTs, where according to [45], [56], [57], the SST could connect to 30 kV grids and step down to LV level. Power levels are expected to go up to 10 MW. Traction will require high power density, so the converter will save space and weight in the locomotive.

Table 2.1: List of demonstrators in traction and solid state transformers

No	Entity	P_N [kW]	V_{in} [kV]	V_{out} [kV]	F_{sw} [kHz]	Application	Topology	Transformer type	Semiconductors	Cooling	Modules	Ref	Year
1	ABB	350	3	3	10	Traction	SRC	Amorphous	Different modules	De-ionized water	12	[58]	2002
2	ABB	75	1.8	1.8	0.4	Traction	Cycloconverter	Silicon Iron	3.3kV IGBT	Oil immersion	16	[59]	2007
3	Bombardier	400	3.6	2.8	8	Traction	SRC	Nanocrystalline	4.5kV IGBT	De-ionized water	8	[60]	2007
4	KTH	170	2.5	0.6	4	Traction	Cycloconverter	Amorphous	Different modules	Oil immersion/Heat sinks Natural convection	1	[61]	2009
5	Michigan University	70	0.3	0.7	13	Metro Aux Supply	Full bridge	Ferrie	Powerex CM600HU-24F	Aircooled	1	[62]	2009
6	DELFT University	50	0.75	0.6	25	-	ZVS, Quasi-ZCS DC/DC	Amorphous	Different modules	Water cooled	1	[63]	2009
7	Uniflex	300	3.3	3.3	2	SST	DAB+ Cycloconverter	Amorphous	Dynex 1700V/200A IGBT,	Oil immersion+forced cooling	16	[64]	2010
8	Siemens	450	3.6	3.6	5.6	Traction	SRC	Nanocrystalline	6.5kV IGBT	Internal cooled aluminium	8	[65]	2011
9	GE	1000	13.8	0.4	20	SST	DAB	Nanocrystalline	SiC Mosfets Schotky diodes	Aircooled	1	[51]	2011
10	FREEDM NCNU	20	3.8	0.4	3	SST	DAB	Amorphous	6.5kV SiC IGBT Powerex PM100CLA060	Heat sink-forced	3	[66]	2011
11	Ikerlan	400	3	0.75	1	Traction	DAB	Silicon Iron	6.5kV IGBT on High side 1.7kV on LV side	Aircooled	1	[67]	2012
12	Ikerlan	400	3	0.75	5	Traction	LLC	Nanocrystalline	6.5kV IGBT on High side 1.7kV on LV side	Aircooled	1	[67]	2012
13	ETH Zurich	166	2	0.4	20	Traction	DAB	Ferrite	1.7 kV IGBT on high side 600V on LV side	Aircooled	6	[68]	2013
14	ETH Zurich	166	2	0.4	20	Traction	SRC	Nanocrystalline	1.7 kV IGBT on high side 600V on LV side	Water cooled	6	[68]	2013
15	ABB	150	3.6	1.5	1.8	Traction	LLC	Nanocrystalline	6.5kV IGBT on high side 3.3kV on LV side	Oil cooled trafo, water cooled PEBB	9	[43]	2014
16	RWTH Aachen	5000	5	5	1	MVDC Distribution	DAB	Silicon Iron	IGCT(5SHY 3545L0001) antiparallel diode D1031SH45TS02	Water cooled	1	[50]	2014
17	ETH Zurich	25	5	0.7	50	SST	DAB	Ferrie	SiC JFET	Aircooled	1	[69]	2014

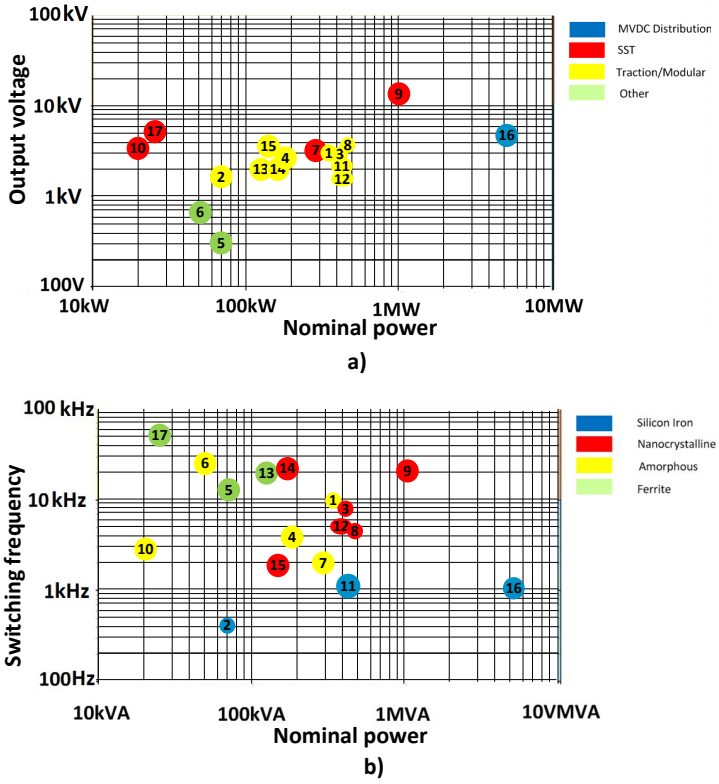


Fig. 2.10: a) Overview of demonstrators output voltage; b) Overview of demonstrators switching frequencies and type of transformers' cores.

As reported in [43], [58], [60], [61], [65], [68], [70] all demonstrators were built in a modular fashion, and N+1 redundancy is incorporated, with high power density as the main design driver. For medium voltage power distribution SSTs, the design driver for topology choice is bi-directionality. The SST converter will have to transfer power both ways and compete with standard 50 Hz/60 Hz power transformers on weight, volume and reliability.

For offshore wind turbines the requirements are different. Considering the rough environment, humidity levels, distance from shore, considerable smaller space and size, it is expected that the design specifications will be much tougher. The level of specifications and the study necessary to get them are elaborated in Chapter IV. Power levels are in the range of 5 MW to 15 MW, while MV side voltage are in between 50 kV to 100 kV. The converter will have to meet requirements as high efficiency, high power density, while offering good availability and access to maintenance.

2.4.1 Basic circuit concepts from demonstrators

From a wide range of possible topologies, only a few circuits have been prototyped at high power and a list of them is illustrated in Fig. 2.11, with three principle topologies: series resonant converter (in 2-level and 3-level half bridge and full bridge configuration), LLC resonant converter and the dual active bridge (in single and three phase variant).

In the case of traction and SSTs there is a trend on resonant and DAB converters used in modular topologies, having cascaded configurations. A lot of practical information regarding medium frequency transformer design and challenges can be obtained from traction demonstrators. The majority of demonstrators employ bi-directionality, meaning active switches on LV and MV side. For wind turbine applications, it is argued to use uni-directional topologies. For the medium voltage side, two different kinds of semiconductors were used, namely IGBTs and IGCTs, while for traction converters, 1.7kV, 3.3kV and 6.5kV were mainly used. For SST applications, SiC mosfets in single cell topologies are suggested, having breakdown voltages to 10kV and with very low current $\leq 30A$.

2.4.2 Traction demonstrators

A set of demonstrator setups for traction application are shown in Fig. 2.12. In majority of setups, the SRC is the preferred topology due to its soft-switching characteristics (meaning low semiconductor losses), while in some cases it evolved into the LLC topology. Module nominal power varies from 75 kW up to 450 kW in the reported prototypes. According to the authors, modular approach makes the DC/DC converter robust and fault tolerant. On the other hand, the high number of modules decreases reliability from FMEA (failure mode effect analysis) point of view, as the number of components increases. Efficiency is increased by disconnecting modules and so cancelling their losses during partial loading conditions. Among the important learnings from traction applications with respect to turbine applications, a few are listed here: transformers are design at elevated frequency; soft-switching of HV IGBT and IGCT is required to decrease losses; cooling aspects play a big role in evacuation of heat; control of resonant and soft-switching topologies; compact design for high power density is a design driver; insulation coordination is a key challenge; attention to manufacturers data sheet regarding transformer and the need of experience with certain core materials to estimate the losses correctly; control at light load and especially the commissioning of a MW setup.

The use of a 1.2 MW modular series resonant LC converters has been described in [47], [48]. In (Fig. 2.12a), a picture of world's first power electronic transformer for traction is illustrated.

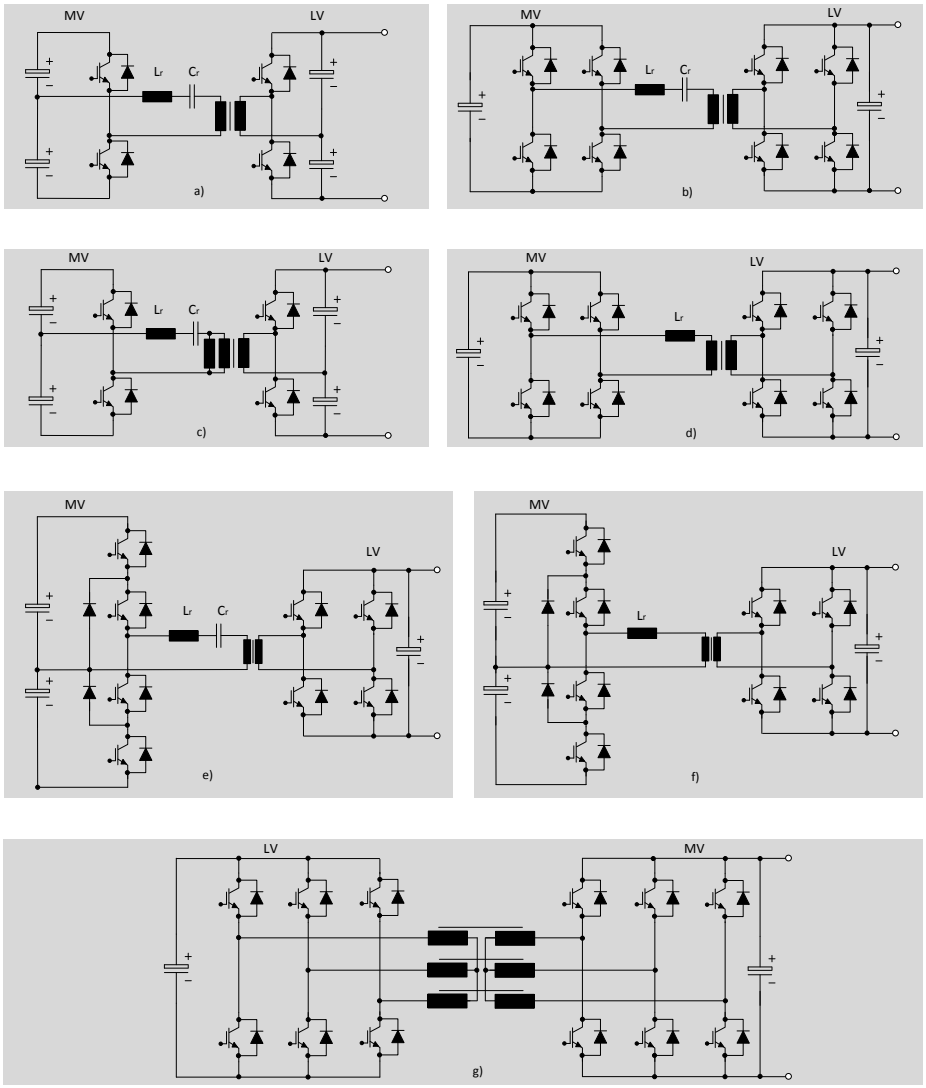


Fig. 2.11: Demonstrators common topologies: a) Half-bridge SRC; b) Full-bridge SRC; c) Half bridge LLC; d) Full-bridge DAB; e) NPC SRC; f) NPC DAB; g) Three phase DAB.

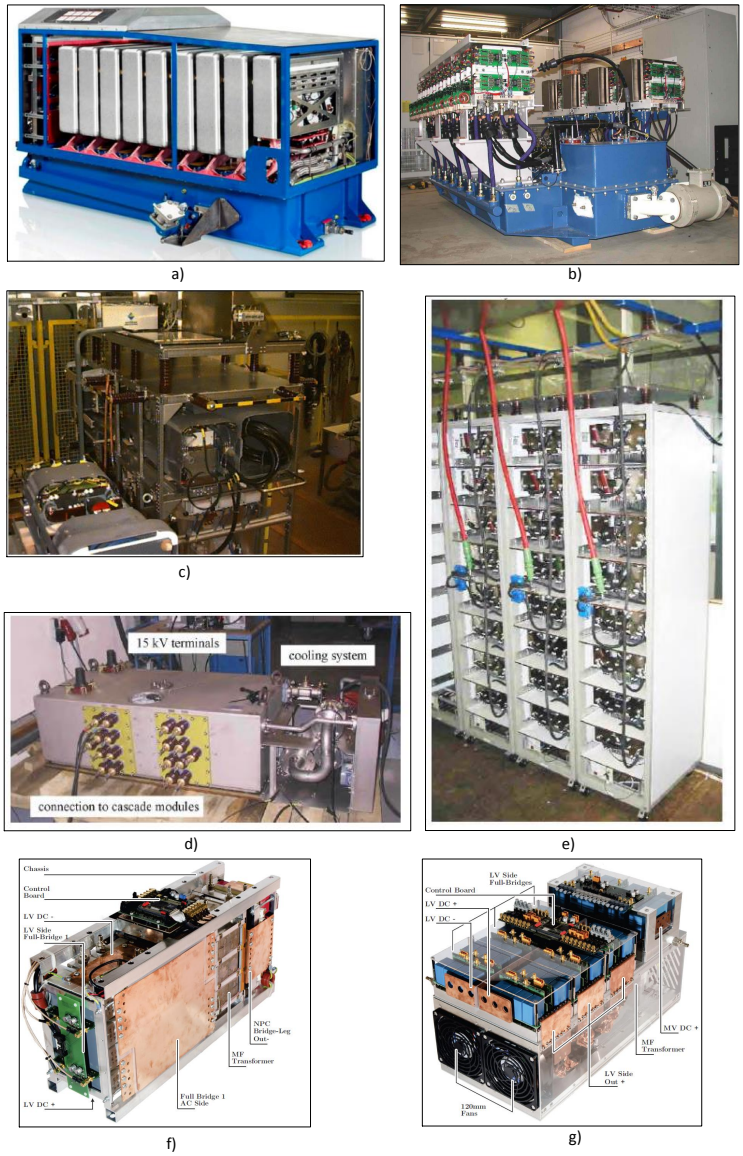


Fig. 2.12: a) 1.2 MW modular traction demonstrator [48]; b) Cycloconverter traction demonstrator [59]; c) Traction demonstrator [60]; d) Traction demonstrator [71] ; e) Traction demonstrator [72] ; f) 166 kW SRC with nanocrystalline transformer [73]; g) 166 kW DAB with ferrite transformer [73].

In [59], (Fig. 2.12b), the setup of 16 bidirectional cyclconverters (1.2 MW in total), connected in series to the catenary of 15 kV and 16.7 Hz was assembled. On the LV side, there were 16 four quadrant converters connected in parallel to a 1.8 kVDC link. The medium frequency transformers were designed for 400Hz, while using sillicon iron core and bar conductors. On both MV and LV side, 3.3 kV/2 x 400A IGBTs were used, for volume and cost purpose. In order to reduce costs, maintenance and size, oil was used for the converters (which had the IGBTs on cold plates) and the transformer was immersed in oil.

In [60], (Fig. 2.12c) a full bridge SRC based on 6.5 kV IGBT with a 1:1 medium frequency transformer and a switching frequency of 8 khZ has been described. Standard 6.5 kV IGBTs and modified 6.5 kV IGBTs (irradiated in order to reduce the carrier lifetime and thus lower turn-off losses) have been tested in [65]. It was reported that with the use of modified IGBTs, the switching frequency could be increased by 30 % compared to standard IGBTs, while the frequency of interest was 5-8 kHz.

A 15 kV/16.7 Hz energy supply system with 5 kHz medium frequency transformer and 6.5 kV IGBTs in resonant operation was reported in [71], (Fig.2.12c). The concept proposed eight cascaded modules, each consisting of a four-quadrant converter. The mechanical design was based on glass fiber reinforced plastic, suitable for good insulation and low weight, but lower structural strenght.

In [72], (Fig.2.12d), a M^2LC modular-multilevel converter is proposed with 2 MW power rating and 17-level output-voltage. 32 IGBTs are controlled per arm, while an example of the dynamic and steady state performance for single phase operation on the 25kV/50Hz power line is exemplified.

Two other concepts have been analyzed in [73], (Fig.2.12f and g), where the classic series resonant converter and dual active bridge have been proposed in a modular concept. Both concepts had a power rating per module of 166kW, while switching at 20kHz. Each module was adapting 2kV to 400V.

2.4.3 SST demonstrators

In [64], (Fig. 2.13a), a modular SST based on DAB topology was investigated. The structure allows the converter to be arranged in parallel and series combination to meet application power levels. Bidirectional power flow of 300kW was reachable with voltages up to 3.3kV. The medium frequency transformers were operated at 2kHz and employed amorphous cores and litz wires for the windings.

[74], (Fig. 2.13b) presents the design and development of a three phase 10kV / 400V of a 500 kVA SST. The power circuit is designed in a modular fashion, where each module has galvanic separation through a medium frequency transformer, assembled around an amorphous core material. The SST

was used to provide constant voltage and constant frequency for the nonlinear impact loads and prevent load harmonics from injecting into the utility grid.

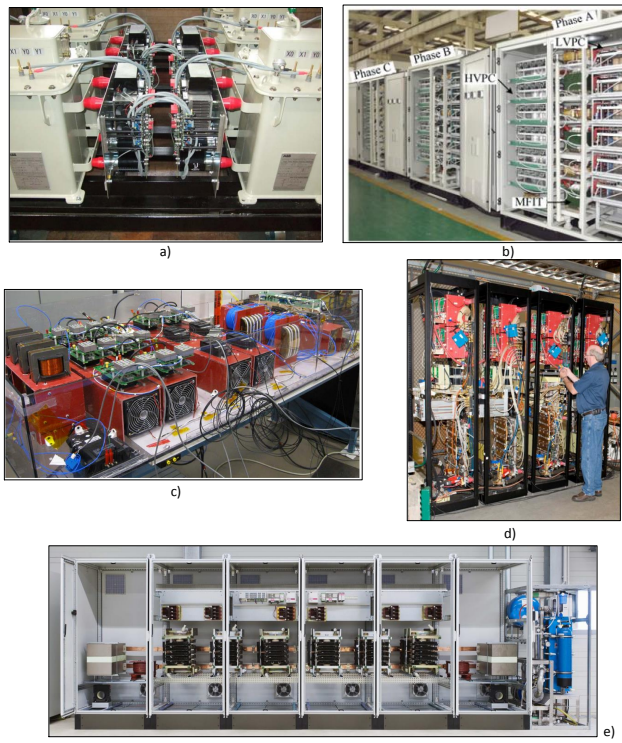


Fig. 2.13: SST demonstrators: a) 300 kW [64]; b)a 10 kV/ 400V 500 kVA SST[74]; c) 25 kVA prototype [66]; d) 10 kV, 855 kVA SST[51]; e) 5 MVA SST [50].

Another interesting demonstrator from [66] and shown in Fig. 2.13c, where a 20kVA SST was implemented. A topology of 7 level, cascaded H bridges was deployed for the high voltage rectifier stage. The rectifier stage had a switching frequency of 1kHz, while the employed DAB was operated at 3 kHz. The MF transformers had a turns ratio of 1:9 and were assembled around amorphous alloy cores.

In [51], another SST proof-of-concept, (Fig. 2.13d) was demonstrated with the help of 10kV SiC Mosfets modules, up to 855 kVA operation and 97%, efficiency. Soft switching at 20 kHz, in a bidirectional application (13.8kV to 465V), the SiC-enabled SST represents a 70% reduction in weight and 50% reduction size, compared to a 60Hz conventional transformer.

A 5MW demonstrator, (Fig. 2.13e) for a medium voltage DC/DC converter, intended for MVDC distribution was investigated in [50]. A three

phase dual active bridge, operated with IGCTs at 5kV DC link and 1kHz was the used topology. To commission the setup, initially only a single phase converter was operated at 2.2 MW, signalling that even a 3 phase transformer prototype for DAB is difficult to manufacture. The IGCTs and diode stacks were all water cooled, while the transformer was immersed in oil.

2.4.4 DC wind turbine demonstrators

A few scaled demonstrators of circuits proposed for DC wind turbine are illustrated in Fig. 2.14. Vast majority of setups are only proof of concepts, at scaled voltage and power levels.

In [75], a modular series connected converter suitable for transformerless offshore wind turbines is analysed (Fig. 2.14a). The main objective was to verify the proposed converters as a suitable interface between a modular axial flux ironless stator PMSG and a high voltage DC Link. The converter is composed of N x 3 phase VSC units, while each unit is connected to an independent 3-phase winding output from the modular generator. The concept was verified experimentally on a 45kW prototype.

In [55], a DC grid for offshore wind farms is investigated with focus on design and control. A parallel connected SAB dc/dc converter is proposed, and a demonstrator (Fig. 2.14b) rated at 1 kVA, with input voltage of 120V and output voltage of 600V, was tested. Switching frequency was around 10 kHz.

Aspects regarding wind park design and grid connection were treated in [10], with a demonstrator as seen in Fig. 2.14c. The concept was composed of 4 stages and proposed for series connected turbines. The downscaled converter was rated at 5.8kW, 300V input and output voltage.

A high efficient, high power step up resonant switched capacitor converter for offshore wind energy is proposed in [45]. This work presents a converter, which is characterized by soft-switching condition for all switches and diodes. The demonstrator from Fig. 2.14d is composed of 17 levels, 24kW with a switching frequency of 7.5kHz. Input voltage was 600V, while output voltage was 10.2 kV.

Fig. 2.14e shows a scaled down setup from [6], with a power rating of 9kW, built around a classic full bridge converter, and with 300V input and output voltage. In Fig. 2.14f, the reduced matrix topology discussed in [9] and proposed for series connected turbines is presented. The setup was rated at 10kW, with 10kHz switching frequency, 200Vrms input and 326Vdc output.

Another high gain topology, proposed in [46] and based on resonant switched capacitor cell is show in Fig. 2.14g. A 5kW prototype was evaluated, with switching frequency of 4.5kHz. Input voltage is 100V, while output voltage is 500V.

In [76], demonstration of a 30kW IGBT LCL dc/dc converter as a proof of

concept for interconnecting HVDC systems is performed. The setup picture is presented in Fig. 2.14h and proposes two active bridges with a resonant tank in between. Switching frequency is set to 5kHz, with 200V on input and 900V on the output.

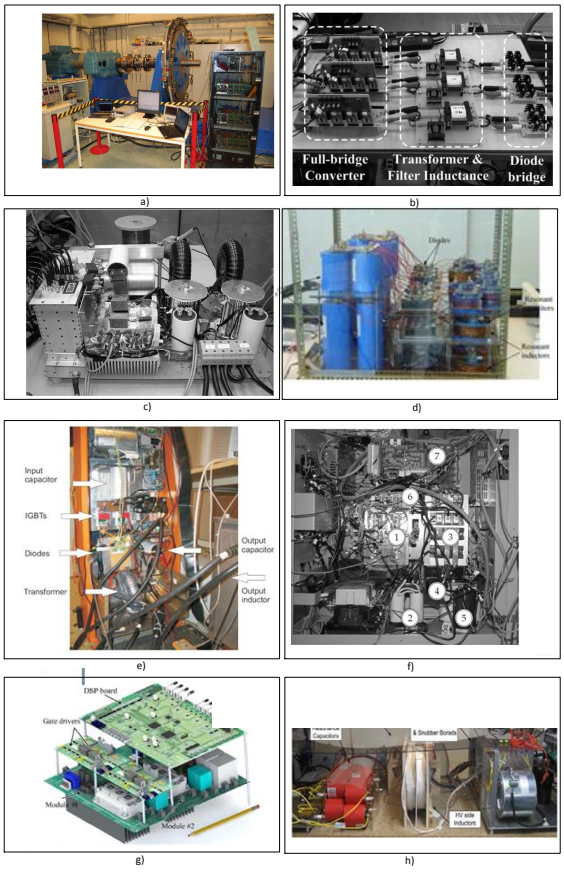


Fig. 2.14: DC/DC converter demonstrators for wind turbines:a) Modular series connected converter[75] b) Single active bridge prototype[33]; c) 11.2 kW prototype [10]; d) High gain converter [45]; e) Full bridge converter [6]; f) Matrix converter [9]; g) High gain converter [46]; h) 30 kVA, high gain converter [76]

2.4.5 Medium frequency transformer technologies

Low frequency transformer technologies have been known and improved since the beginning of last century. As for 50Hz and small power smps (switched mode power supply), medium frequency transformers are com-

posed from core and windings part. The challenges of mechanical assembly and heat removal are on the other hand, way more considerable at elevated voltage, frequency and power. The characterization of medium frequency transformers is presented in the literature, with different optimal design methodologies proposed in [67], [77], [78]. However, there are no standards (due to lack of global comparison and validity studies), making the design difficult.

A survey of different medium frequency transformer prototypes, proposed mainly in traction and solid state transformers is illustrated in Fig.2.16 and their characteristics presented in Table. 2.2.

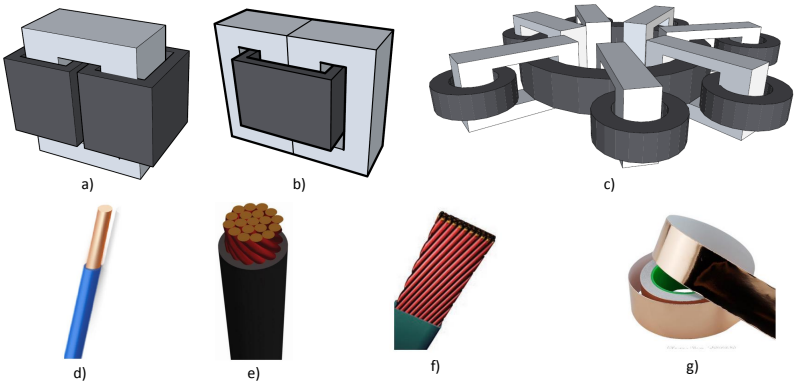


Fig. 2.15: Transformer core types: a) C-core; b) Shell core; c) Matrix core. Windings type: d) round wire; e) Circular Litz; f) Rectangular Litz and g) Foil windings.

In the converter topologies proposed for traction, SST and DC wind turbines, the transformers are exposed to non-sinusoidal current and voltage excitation, requiring more complex expressions to characterize the electromagnetic and thermal fields as compared to line frequency transformers.

To design an optimal medium-frequency transformer, one has to understand the frequency dependent behaviour of the magnetic material and the utilization of different conductor types at high switching frequency needs to be properly characterized. In low frequency operation, the typical core materials are silicon and nickel steel. Increasing the excitation frequency, the losses of these materials increase drastically. For a while, ferrite has dominated the world of magnetic cores for power electronics, but they have been limited to power and voltage because of the small saturation flux density B_{sat}, but also due to its manufacturing and brittle nature. To achieve operation at high power and voltage level, different materials like nanocrystalline and amorphous alloy, that exhibit low core losses, high saturation flux density and high continuous operating temperature are preffered. As seen in Table. 2.2, most of the demonstrator prototypes are using the previously mentioned

materials. Core configurations play a major role and according to the literature and as seen in Fig. 2.15, there are four concepts: C-core type, shell type, matrix and coaxial.

Fig. 2.16: Survey of medium frequency transformer prototypes: a) STS transformer prototype[79]; b) 400 kVA prototype for SRC[67]; c) 400 kVA prototype for DAB[67]; d) Traction transformer [58]; e) SST transformer prototype [66]; f) 166 kVA transformer ptotype[73]; g) 100 kVA transformer for DAB[35]; h) 168 kVA transformer for traction[80] ; i) Traction transformer[60]; j) SST transformer prototype[64]; k) Traction transformer[59]; l) Traction transformer [65]

Table 2.2: List of transformer prototypes

No	Center	Core Material	Core Type	Windings	Isolation	P_N[kW]	F_{sw}[kHz]	Cooling	Weight[kg]	Turns ratio	Ref
1	ABB	Si-Fe	C-core		For 15 kV	75	0.4	Oil	50% of PT	1:1	[59]
2	ABB	Nanocrystalline	Co-axial	L_m =25 mH L_{lk} =3 uH Al and Copper	38 kV	350	10	De-ionized water	$\leq$ 50	1:1	[48]
3	Siemens	Nanocrystalline	C-core	Al	Nomex, oil 25 kV	450	5.6	Core-oil De-ionized water for Al conductors	$\leq$ 60		[60]
4	ETH Zurich	Ferrite	Shell	Litz wires	PTFE	166	20	Air cooled	-	3:1	[68]
5	ETH Zurich	Nanocrystalline	Shell	Litz wires	Mica tape	166	20	Water	-	5:2	[68]
6	Bombardier	Nanocrystalline	Co-axial	L_{lk} =2.3 uH	Full line MV motors. Glass buble filled PV	400	8	Water	$\leq$ 20		[65]
7	Ikerlan	Si-Fe	Shell	L_{lk} =390 uH	18 kV	400	1	Dry	$\leq$ 460	4:1	[67]
8	Ikerlan	Nanocrystalline	C-core	L_{lk} =10 uH	18 kV	400	5	Dry	$\leq$ 60	4:1	[67]
9	KTH	Amorphous	Shell	Litz wires	Epoxy 30 kV Oil and nomex paper	170	4	Oil	$\leq$ 150	15:1	[61]
10	GE	Amorphous	-	-	-	1000	20	-	-	-	[51]
11	Freedm	Amorphous	C-core	L_m =235 mH	15 kV pfa	20	3	Dry	$\leq$ 13	9.5:1	[66]
12	UNIFLEX	Amorphous	-	-	-	300	2	Oil	-	-	[64]
13	RWTH Aachen	Si-Fe	C-core	Litz wires	12 kV	2200	1	-	600	1:1	[50]

From thermal point of view, the shell core exhibits the best performance, as for C-core, the windings are surrounding the core and because of poor thermal conductivity of the insulation it can lead to high core temperatures.

When selecting and designing the windings, one has to consider aspects like utilization area, good thermal behaviour and a proper electrical isolation. Due to elevated switching frequency, the impact of skin effect and proximity losses have to be considered when selecting the type of conductors. Eddy currents at high frequencies will force smaller diameters, suggesting in general the use of Litz wires, that have separately insulated wire strands twisted or braided together. To increase fill factor and to reduce eddy currents in low voltage windings, thin foil conducters are also an option, with the assumption that each turn of the foil conductor forms an entire winding layer.

Attention needs to be paid on insulation coordination and insulating materials, as they need to provide high voltage insulation between the windings and the core, while transferring dissipated heat. Characteristics like high dielectric strength, low loss and high maximum operating temperature are required for MF transformers. Common insulating materials are: epoxy, micare or pvc[81]. In the end, design criterias for an optimal transformer are based on weight, efficiency, cost, isolation and temperature rise, as it will decide the maximum allowed losses. Accurate thermal models are necessary during the design stage to predict final temperatures.

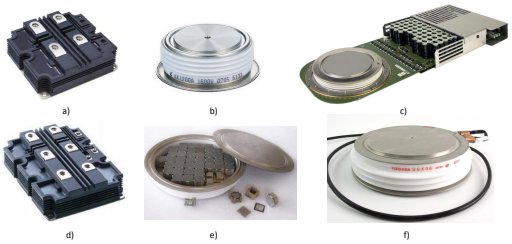


Fig. 2.17: Different semiconductor packages: a) Dual diode module; b) Press pack diode; c) Press pack IGCT; d) Single IGBT module; e) Press pack IGBT; f) Press pack IEGT.

2.4.6 Semiconductors overview

Relatiely, few high power, high voltage semiconductors exist and careful attentions is needed for device selection in a MVDC converter. According to [35], the selected device needs to have characteristics like: high voltage rating with acceptable conduction and switching property; current ratings of several kA; low integration effort for series connection of multiple devices; active fault protection without additional components and a low gate drive power

demand. As there are no commercial devices that meet all above features a trade off is needed.

Different semiconductor packages are illustrated in Fig. 2.17 with their general properties illustrated in Table. 2.3.

Table 2.3: List of semiconductor parameters

Device	Press pack IGCT	Press pack IEGT	Press pack IGBT	Power module IGBT	Power module Diode	Press pack Diode
Manufacturer	ABB	Toshiba	Westcode, IXYS	ABB	Infineon	Infineon
Code	5SHY 42L6500	ST2 100 GXH22A	T2400 GB45E	5SNA 0750G650300	DD750S65K3	D711N
Blocking Voltage [V]	6500	4500	4500	6500	6500	6500
Turn-off Current [A]	3800	2100/5500	2400/4800	750/1500	750	770
$V_{TO,max}$ [V]	1.88	3	1.49	2	3.5	0.84
$R_{t,max}[m\Omega]$	0.56	1	1.05	2.5	0.37	0.87
$E_{on,max}$ [J]	3.1	18.4	15	6.4		
$E_{off,max}$ [J]	44	17	14	5.3	3	
Meas.condition	4kV/3.8kA	3kV/2.1kA	2.8kV/2.4kA	3.6kV/0.75kA	3.6kV/0.75kA	1kV/1kA
$T_{j,max}$ [deg C]	125	125	125	125	125	125
$R_{th(j-c)}$	8.5	5.25	5.2	11	18.5	31.5
$R_{th(c-h)}$	3	3	3	9	16	6

2.5 Conclusions

A survey of DC wind farms configurations, DC wind turbine concepts and a catalogue of DC/DC converter topologies was presented. Regarding wind farm configuration, the two stage concept is chosen as main frame work and for the turbine concept, the 4 stage concept that reuses the AC turbines's generator and active rectifier followed by an isolated high power dc/dc converter. The catalogue of circuits mounts up to 37 different possible topologies, as presented in previous works and they are categorized from switching and galvanic isolation point of view. Topologies such as classic hard switched full bridge converter, matrix, mmmx, resonant, phase shifter or high gain have been addressed. To understand the challenges, specifications and functionalities required for the turbine DC/DC converter, a survey of university and industrial demonstrators was presented, to further down select to a few topologies and increase the confidence towards the optimal choice of topology. During the process of survey, focus was mainly on assembled and tested high power medium voltage demonstrators, with applications ranging from traction converters to solid state transformers. As it turns out, from a wide range of possible topologies, only a few circuits have been prototyped at high power, with three principle topologies: the series resonant converter, LLC resonant converter and the dual active bridge (in single and three phase variants). The knowledge gained from these surveys is used in the process of selection of a suitable and later optimal DC/DC topology, which are presented in the following chapter.

Chapter 3

DC/DC converter topology selection

Summary

The catalogue of circuits developed in chapter II from the survey of DC/DC converter topologies, suggests a large pool of circuits for DC wind turbine converters. However, majority are at an immature technology level, as no substantial experience from full scale detailed design exists, making the selection of the optimal converter difficult. A methodology is therefore suggested. First, a downselection of circuits is proposed based on a set of fundamental requirements, leading to the comparison of 5 topologies: the full bridge converter (FB), the single active bridge converter (SAB), LLC converter and two variants of the series resonant converter. Second, with the help of F-FMEA and a pugh matrix decision tool, a variation of the series resonant converter operated in a novel fashion is suggested as the more suitable topology for DC wind turbines. This chapter is based on works from publications [82] and [83].

3.1 Methodology to select circuits for comparison

It is expected from the mega-watt, high voltage, high-frequency DC/DC converter located inside the wind turbine, to employ state of the art commercial technologies. This fact is a driver in the process of topology selection. Electrical, cooling and control interfaces must be compatible with present turbine solutions, while physical size and weight should be smaller or equal to today's AC solutions [82].

As presented in previous chapters, there are many suggested topologies in the state of the art, but they are at an immature technology level, as no substantial experience from full-scale detailed design exists. A comparison of all proposed topologies for example efficiency and power density point of view will not answer which is the most suitable topology and technology. One reason is that efficiency studies require validation through scaled or full scale experiments. Thermal proof-of-concepts with the target devices need to be validaded first, so confidence is built in the topology and extrapolation of the results can be applied at higher specifications. A mature technology route (usually composed of different stages that increase technology readiness level) is required, as important knowledge is gained from prototype and field experience. Therefore, a downselection process based on fundamental requirements is employed, as exemplified in Fig. 3.1.

To reach the list of fundamental requirements for the turbine converter, the challenges that might occur in the choice and development of the circuits must be clarified. As mentioned in [84], any suggested MVDC collection solution must be possible to be characterized and evaluated through a series of case studies. That particular list of case studies will then determine

the suitable specifications and components ratings for the turbine converter. Knowing the ratings and the requirements for DC wind turbine allows the designer to downselect from the catalogue of circuits to only a few concepts, that are further compared with respect to different design drivers.

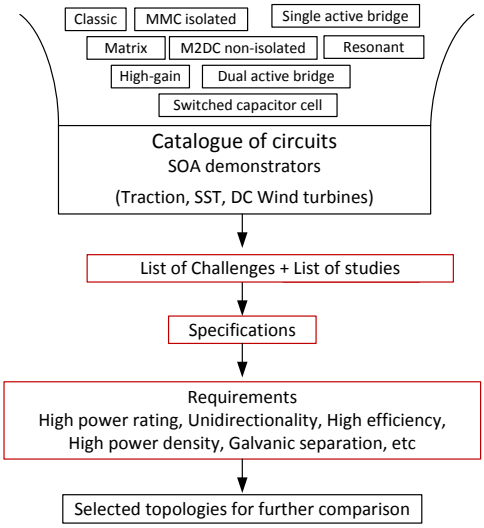


Fig. 3.1: Methodology to select circuits for comparison

3.1.1 List of challenges

Looking at Fig. 3.2, wind turbine DC/DC converters will need to be designed for higher power and voltage, as compared to traction and SST converters.

To understand the main challenges, the survey of demonstrators in traction, SSTs and DC wind turbines was arranged. As presented in [35], [85], [86], the main challenges that will be encountered are shown in Table. 3.1. The handling of medium voltage requirements, will have an impact on the converter's modularity philosophy. Galvanic separation is required mainly for safety reasons and lower insulation requirements for the turbine generator and nacelle as compared to non-isolated topologies. A high voltage transfer ratio is needed, in order to limit the collection grid cable losses.

Further on, isolation coordination is required so safe clearance and creepage distances are implemented. Electromagnetic interference is another area of interest that will impose challenges, as there are no standards for the MVDC voltage levels required in this application. Protection and control are two other areas that bring challenges and finally the construction and

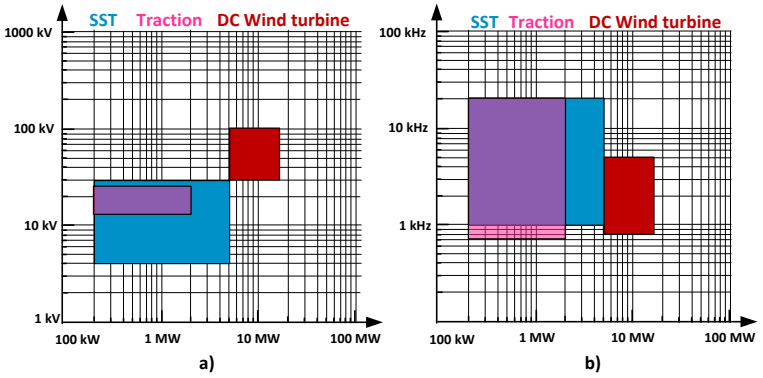


Fig. 3.2: Range of specifications from survey of demonstrators

Table 3.1: List of challenges

a	Handling of medium voltage (modular vs. series connec.)
b	Galvanic separation
c	High voltage transfer ratio
d	MF Transformer design and isolation
e	Isolation coordination
f	EMI
g	Protection
h	Control
i	Construction & testing

Table 3.2: List of studies

Study class		Study objective in turbine DC/DC converter	Detail level	Objective
I	Steady state operation	Determine converter ratings and boundary limits. Validate controller, ratings and losses.	Converter level	Determine converter specifications.
II	Dynamic operation	Validate controller, protection, ride through capability. Generate voltage, current, power waveforms. Calculate peak loadings for equipment.		
III	Voltage disturbance			
IV	Short circuit (dynamic)			
V	Harmonics and controller interaction	Calculate harmonic emissions. Calculate harmonic susceptability		
VI	Sensitivity study	Voltage distribution on MV converter/valve Impact on losses, transformer and controller behaviour	Device and converter level	Determine converter design.
VII	Thermal study	Semiconductor, transformer cooling temp.	Sub-assembly level	
VIII	Electromagnetic study	Distribution of electric and magnetic fields. Distribution of stray capacitances		

testing of a possible demonstrator will pose technical issues. One should enforce safety rules during testing period and also elaborate testing facilities that would not require a large number of experimental iterations or bulky loads.

3.1.2 List of necessary studies and specifications

A list of generic studies (inspired from established AC wind farm studies) for turbine DC/DC converter is presented in Table. 3.2, while Table. 3.3 indicates the fundamental DC/DC converter specifications. The proposed studies have the objective of determining components loads and ratings and predict performance, in order to facilitate design decisions. A similar methodology for characterization of electrical properties of DC collection systems in offshore wind farms was introduced in [84]. The goal of the steady state operation studies is to determine the converter ratings and evaluate the controller and losses. During dynamic operation studies, protection, ride through capability and generation of peak loading is obtained. Sensitivity studies are also required to characterize the behaviour of the medium-voltage converter, evaluation of voltage sharing and impact of non-idealities on the characteristic waveforms. Thermal studies are neccesary to evaluate semiconductors junction temperature, transformer core, windings and cooling liquid hot spots. They also determine the selection of a suitable cooling system. Finally, electromagnetic studies will evaluate the distribution of electric, magnetic fields and identification of equivalent circuit of stray parameters.

Table 3.3: Fundamental DC/DC converter specifications

Parameter	Range	Selected value
Nominal power, P_n	5 to 15 MW	10 MW
Input DC Voltage, V_{in}	$\pm$ 0.5 to $\pm$ 8.0 kV	$\pm$ 2.0 kV
Output DC Voltage, V_{out}	$\pm$ 35 to $\pm$ 50.0 kV	$\pm$ 50.0 kV
Switching frequency, F_{sw}	0.5 to 5 kHz	$\pm$ 1.0 kHz
Power overload	1.1 x P_n (short duration)	
V_{in} variation	$\pm$10%	
V_{out} variation	$\pm$10%	
$V_{out,max}$ transient	1.4 x V_{out}	
MV short circuit level	50 x I_{out}	
LV short circuit level	1.5 x I_{in}	
Insulation level	$\pm$ 1.0 to $\pm$ 1.5 p.u. x V_{out}	$\pm$ 75.0 kV

3.1.3 Fundamental requirements

The previously described list of challenges and the expected range of specifications have lead to a set of fundamental requirements as described in Table.3.4. Compared to traction and AC/AC solid state transformers, the DC wind turbine converter will have to face higher requirements, meaning

Table 3.4: Fundamental requirements

a	High power rating
b	Unidirectional power flow
c	High gain voltage transformation (LV to MV)
d	Efficiency equal or higher than AC solution
e	Power density equal or higher than AC solution
f	Galvanic separation through medium frequency transformer
g	Modular architecture that allows low number of components and a low risk priority number
h	Control philosophy similar to AC solution (LV side DC-Link Control)
i	Compatible electrical interface to classic PMSG and active rectifer

from the proposed catalogue of circuits, only a few topologies will meet the requirements.

3.1.4 Selected converter topologies

A set of fundamental requirements is proposed and illustrated in in Table.3.4. Applying these requirements, only a few set of topologies from the survey of circuits and demonstrators are suitable for further comparison. Looking at Table. 3.5, the single active bridge and some variants of resonant topologies are selected for comparison against the classic full bridge converter, which is seen as the reference point. The list of concepts for comparison is shown in Fig. 3.3 with their characteristic waveforms and with the specifications from Table. 3.3.

Full bridge converter (FB)

If one should implement a DC turbine, it could take a present AC solution; add a rectifier and an output filter, resulting in a full bridge topology (FB). For this reason, the FB (Fig. 3.3a) is chosen as a baseline for comparison of losses and power density, as it is the most simple and straight forward topology to implement. It is operated with constant frequency and variable duty cycle and has hardswitching losses on the semiconductors and high dv/dt on transformer windings. It has been proposed as a turbine solution in [6].

Single active bridge (SAB)

Similar to the FB converter, the single active bridge converter (SAB) (Fig. 3.3b) operates also at constant frequency and with variable duty cycle, being proposed as an alternative to the FB. It has been analyzed in [5], [41] as a three phase variant and in [33], [34] as a single phase interleaved topology. If operated in DCM mode for full operational range, the output filter inductance can be moved to the primary side, reducing the inductance by a factor

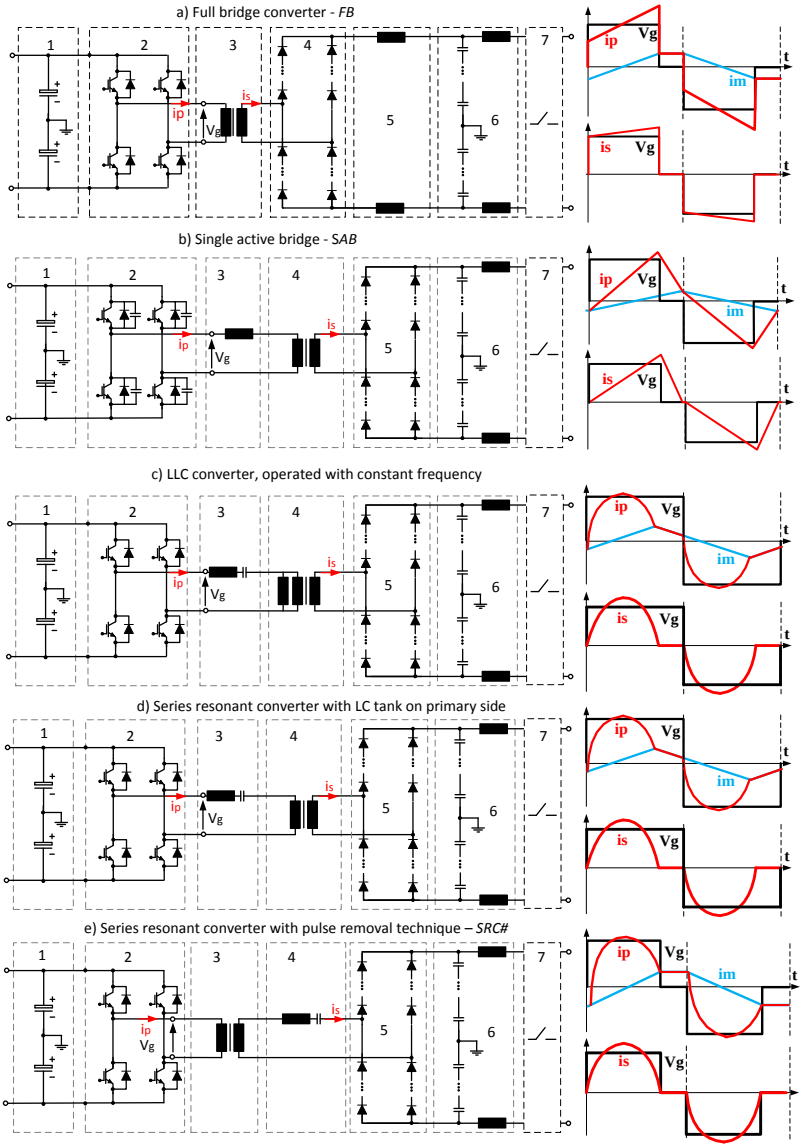


Fig. 3.3: List of concepts for comparison, divided in sub-systems: (a) full bridge converter; (b) single active bridge; (c) LLC converter operated at constant frequency; (d) SRC converter with tank on primary side; e) SRC converter operated with pulse removal technique - SRC#

Table 3.5: Selected topologies for comparison

Switching Type	Topologies	High power rating	Unidirectional power flow	High gain voltage ratio	High efficiency	High power density	Galvanic Separation	LPN Modularity	LV side DC Link Control	SOA Compatible
Hard switched	Classic Topologies	X	X	X		X	X	X	X	X
	Matrix Topologies	X	X	X	X	X	X	X		
	MMC Isolated	X	X		X		X		X	X
	M2DC Isolated	X	X	X	X		X		X	X
	M2DC Non-Isolated	X	X		X				X	X
	High-gain Cockroft Walton		X	X					X	X
	High gain Cascaded and Series		X	X					X	X
	High gain Marx		X	X					X	X
Soft switched	Single active Bridge	X	X	X	X	X	X	X	X	X
	Dual active Bridge	X		X	X	X	X	X	X	X
	ARCP	X		X	X	X	X	X	X	X
	Resonant Topologies	X	X	X	X	X	X	X	X	X
	High-gain Jovcic	X	X	X	X	X		X	X	X
	High gain Res. Boost	X	X	X		X			X	X
	High gain RSC	X	X	X	X	X			X	X

of the square of transformers turns-ratio n. The SAB can achieve ZVS (zero voltage switching) at turn-on on the inverter side semiconductors. One of the disadvantages of the topology is that it requires high current rating on both input and output DC-link capacitors, due to high current ripple.

LLC converter at constant frequency

The LLC converter (Fig. 3.3c) operated at constant frequency, was proposed in [87], for traction application, in a modular converter. As the name implies, a LLC resonant tank is used, consisting of two inductors Lr and Lm (with the option of integrating them in the transformer), with a resonant capacitor Cr in series. Normally, to control output power, variable frequency is used, with a 50% duty cycle. It can achieve ZVS at turn on and a low current at turn-off.

Series resonant converter : SRC and SRC#

The series resonant converter has been proposed as a promising DC/DC topology also in traction applications in [73], where its operated at constant frequency in sub resonant mode, and as a three phase variant in [42]. In both situations, the converter has no power control functionality and its operated in open loop. For a wind turbine application, it is mandatory to actively control the DC link. The classic series resonant converter (SRC) with LC tank on primary side (Fig. 3.3d) has the property, that if operated below

resonant point and in discontinuous mode, output power becomes a function of number of pulses sent to the load. The major drawback is the design of MF transformer for the lowest operating point, otherwise transformer saturation occurs. This option has beside the disadvantage of a generous transformer design, also limited range.

To avoid these two drawbacks, a new method of operation was proposed in [88], where a pulse removal technique is applied on a variant of the series resonant converter, with LC tank on secondary side, entitled SRC# (Fig. 3.3e). In summary, the converter is operated with variable frequency and phase shift in sub resonant mode and as soon as the resonant current reaches zero, the inverter voltage is clamped. This means there is a linear relation between output power and excitation frequency. Similar to the LLC topology, the converter has the benefits of ZVS at turn on and low current at turn off for LV side semiconductors, while offering ZCS for MV diodes at turn off.

3.2 Methodology to select suitable DC/DC converter

Regardless of the chosen topology, the turbine converter is subject to vital requirements and functionalities, that impact system availability, efficiency and cost. Considering the rough environment, humidity levels, distance from shore, finite space and size, the converter needs to be designed for a set of simultaneous functionalities and design drivers. The question is which are the fundamental functions and how to rank the design drivers? If a certain functionality failure occurs due to a certain cause, what is the severity level for different topologies? Answering this will help on identification of a suitable technology and critical system parts that present large uncertainties [82].

3.2.1 Functional failure mode and effect analysis

Typically, selecting one engineering solution from a suite of candidates makes use of some sort of comparison [89]. Each candidate gets evaluated (scored) on a series of selection criteria. This is also the case for the turbine dc/dc converter candidates, even if only at conceptual solution level, i.e before entering detailed design, as no substantial experience from full-scale detailed design exists for the relevant applications, i.e. the technology readiness level (TRL) is low. In the early stages it is helpful to identify the required functionality as well as any associated functional failure modes. This kind of scenario requires the generation of a functional failure mode and effects analysis (F-FMEA). This methodology is designed to identify and understand potential failure modes, their causes and the effects on the system for a certain product or process. Afterwards, a risk probability is assigned to the identi-

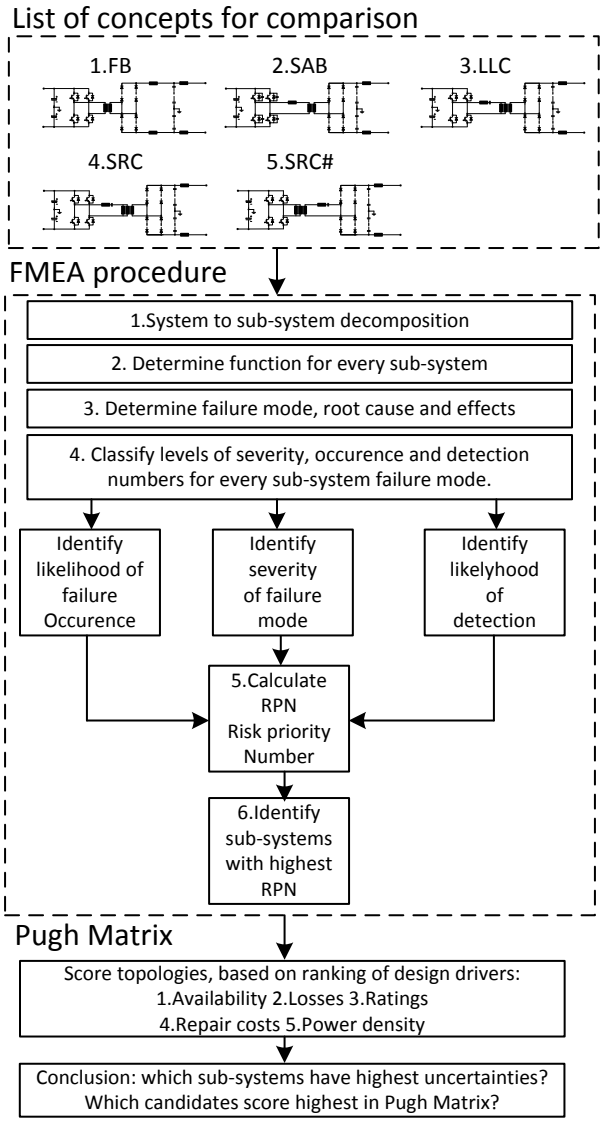


Fig. 3.4: Proposed methodology to select suitable DC/DC converter [82]

fied failure mode, followed by corrective actions to address the most serious concerns. The results from F-FMEA can be used together with a ranking of design drivers as weighted performance indices in a concept comparison (Pugh-Matrix [90]). A set of standards and rules exist in the literature for this topic, but in this approach the procedures from [91], are followed, with certain simplifications. A flow chart of the proposed method is shown in Fig. 3.4 and explained in the following paragraphs.

System-to-subsystem hierarchy

The first step is to establish a system-to-subsystem structure of each candidate circuit, obtaining a proper understanding of the DC/DC converter system and its main sub-systems. Looking at Fig. 3.5(a) and Fig. 3.5(b), the selected topologies can be divided in 3 levels. The dc/dc converter, seen as one system, can be categorized in 7 different sub-systems for every topology, into: inverter, rectifer, transformer, LV and MV dc-link, resonant tank/filter and disconnector. What differentiates the topologies is the sequence of these stages or absence, as seen in Fig. 3.5. Going to component level (system level 3), different components exist, such as: gate drivers, IGBTs, diodes, measurement circuits, control boards, snubbers, etc. Defining functionalities at this level, requires complex work and detailed knowledge of the system. For this reason, it is acceptable to define up to system level 2.

Determine system and sub-system functionalities

A function is defined as what the item or process is intended to do, usually to a given standard, performance or requirement. Functions can be decomposed in sub-functions, by asking how a certain function can be fulfilled? An example is given in Fig. 3.5(c). How can electrical energy be converted from low voltage DC to medium voltage DC? By converting it through different power stages, as inverter, transformer and rectifier. Thus, a set of sub-functions are needed to accomplish a top function. The list of fundamental DC/DC converter functionalities is established in Table 3.9. For further references, sub-system functionalities (inverter, rectifier, transformer, filter/resonant tank, disconnectors, LV and MV DC-link functionalties) are presented in [82].

Determine failure modes and root cause for every sub-system

Failure modes are described as ways in which a component may fail. There are numerous modes of failure. In this study, only the key failure modes, which can cause complete loss of power and major damage to the converter are considered. The causes of failure are said to be root causes and are defined as the mechanism that lead to the failure. Each cause has an effect that

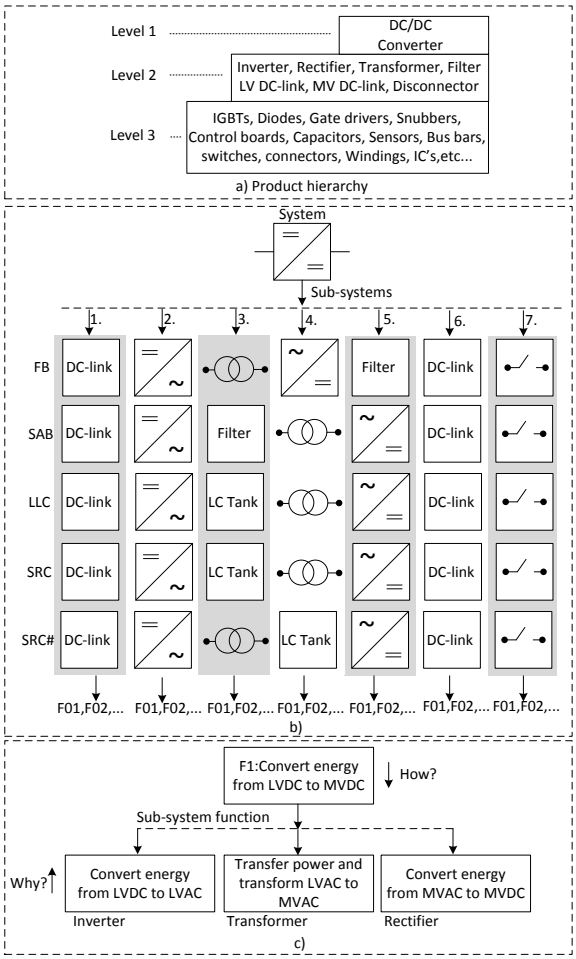


Fig. 3.5: System to sub-system decomposition [82]: a) product hierarchy; b) system decomposition; c) function derivation

influences the unctionalities. In this work, the most serious end effects are considered. A list of generic turbine failure modes were described in [92], and this work considers failures modes associated to the power converter, as seen in Table 3.6. In this study, a limited set of root causes have been considered.

Table 3.6: Generic Failure modes with possible root causes

No	Failure mode	Root cause
1	Electrical failure	High cycle fatigue
2	Electrical insulation failure	Insulation degradation
3	Thermal failure	Overheating
4	Output inaccuracy	Calibration error
5	Intermittent output	Installation defect

Determine levels of severity, occurrence and detection for root cause

The next step is to assign a numerical value for every failure mode, by using severity, occurrence and detection as metrics. Ranking of these is shown in Tables 3.7 and 3.8, with source reference from [93]. Severity level is scaled to the consequences of the end effect of a system failure, where a high value corresponds to a severe effect. Occurrence is defined as the likelihood of a root cause to occur, with the lowest rank for the least probable category. Detection is defined as the likelihood of detecting a root cause before a failure occurs. There are different ways of detecting a failure, the most common being through inspection or maintenance.

RPN: Risk priority number

Severity, occurrence and detection levels are multiplied to get the risk priority number (RPN), which is the final result of the F-FMEA. Summating the RPN for all functions builds the sub-system RPN. Sub-systems with high RPN are considered the most critical areas.

Table 3.7: Severity scale [93]

Rank	Category	Criteria
10	Failure to meet safety	Affects safe operation without warning
9	Failure to meet safety	Affects safe operation with warning
8	Loss of primary function	Loss of primary function
7	Loss of primary function	Degradation of primary function
6	Loss of secondary function	Loss of secondary function
5	Loss of secondary function	Degradation of secondary function
4	Annoyance	Item operable, noticed by 75% customers
3	Annoyance	Item operable, noticed by 50% customers
2	Annoyance	Item operable, noticed by 25% customers
1	No effect	1

Table 3.8: Occurence and detection scale [93]

Rank	Occurence		Detection	
	Likelihood of failure	Incidents per iterm	Likelihood of detection	Opportunity for detection
10	Very high	>1 in 10	Absolut uncertainty	No detection opportunity
9	Very high	>1 in 20	Very remote	Not likely to detect
8	High	>1 in 50	Remote	Post design freeze
7	High	>1 in 100	Very low	Post design freeze
6	Moderate	>1 in 200	Low	Post design freeze
5	Moderate	>1 in 500	Moderately	Prior to design freeze
4	Moderate	>1 in 1,000	Moderately high	Prior to design freeze
3	Low	>1 in 2,000	High	Prior to design freeze
2	Low	>1 in 10,000	Very high	Virtual analysis correlated
1	Very low	>1 in 100,000	Almost certain	Almost certain

3.2.2 Establishment and ranking of design drivers

Following the results from F-FMEA analysis, each topology should receive a weighted rank from +1 to +5, based on prioritized design drivers as explained in [83].

Availability (+5 rank)

The offshore wind turbine converter has to be designed for reliability, making availability the primary design driver. Even the smallest service for offshore installations immediately results in very high costs. Operation and maintenance (O&M) activities typically represent a big part of the total costs (e.g. 25–30% of the total lifecycle costs for offshore wind farms) [94].

Electrical losses (+4 rank)

Low percentage of losses will impact the total cost of operation and leverage the cost of energy. After availability, its considered as the second most important design driver. For example, one has to consider the LCOE (levelized cost of energy), defined as average total cost to build and operate a power-generating asset over its lifetime, divided by the total energy output of the asset over that lifetime [95]. Capital expenditure (CAPEX) and operational expenditure (OPEX) are the two fundamental costs for an offshore

Table 3.9: Converter (system level) functionalities [82]

No	Function
F1	Convert and transform electrical energy from LVDC to MVDC
F2	Deliver power with agreed quality
F3	Control power in full operational range
F4	Control power to agreed stationary and dynamic performance
F5	Control LVDC to agreed stationary and dynamic performance
F6	Operate converter in ± [XX]% MVDC voltage variation
F7	Withstand MVDC network voltage harmonics
F8	Withstand MVDC network harmonic impedance
F9	Withstand voltage levels on LVDC and MVDC sides (stationary and temporary)
F10	Withstand load current levels on LVDC and MVDC sides (stationary and temporary)
F11	Withstand MVDC short-circuit current contribution level
F12	Protect converter from excessive voltage / current from MVDC network
F13	Protect the MVDC network from excessive voltage / current from the converter
F14	Protect converter against MVDC polarity reversal
F15	Receive and respond to changes to MVDC network voltage by adjusting active power
F16	Receive and respond to setpoints for LVDC voltage
F17	Ensure galvanic insulation between LVDC and MVDC sides
F18	Ensure balanced voltage and current sharing on LV and MV semiconductors
F19	Ensure balanced bipolar output voltage
F20	Ensure proper operation with fast and stable recoveries after system faults and disturbances
F21	Ensure safe disconnect from DC collection network during internal and external short circuit scenario
F22	Ensure balanced capacitor voltage on LV and MV DC-link
F23	Ensure shielded cables for low voltage and measurement circuits
F24	Ensure local control through door panel
F25	Ensure remote control through other controller
F26	Ensure fiber optic communication between converter control board and power circuit
F27	Connect or disconnect converter to DC collection network when commanded to
F28	Connect or disconnect converter to generator / rectifier bus when commanded to
F29	Disconnect converter from DC collection network when voltage is too low for too long
F30	Disconnect converter from DC collection network when voltage is too high for too long
F31	Discriminate fault current from load current level
F32	Dissipate energy in LVDC when commanded to
F33	Limit EMC emissions (conducted, radiated) to agreed levels
F34	Withstand EMC imission
F35	Limit acoustic noise emission to agreed levels
F36	Sense converter health and feedback to main controller
F37	Energize LVDC bus from MVDC network
F38	De-energize LVDC / MVDC links for service

Table 3.10: Ranking of design drivers

No.	Design driver	Rank
a.	Availability (leading to loss generation [MW/h])	5
b.	Electrical losses (efficiency)	4
c.	Ratings (name plate power, voltage, temp.)	3
d.	Repair costs (excluding scheduled maintenance)	2
e.	Power density (volume and weight)	1

wind farm, while AEP_k represents the annual energy production. A turbine with high efficiency leads to high AEP_k and lower LCOE.

$$LCOE = \frac{\text{Total costs over life time}}{\text{Electricity produced over lifetime}} = \frac{CAPEX + OPEX}{\sum_{k=1}^{n} AEP_k} \tag{3.1}$$

Ratings / Bill of Material cost (+3 rank)

Considering the high voltage output, the medium voltage ratings will have a high impact on valve design and it will decide the number of series connected switches, which impact mechanical complexity and cooling.

Repair costs (+2 rank)

Important aspects of maintenance and service need to be addressed, so costs can be decreased. The components that need to be replaced should be transportable. Control hardware and software should allow remote access for off-site troubleshooting.

Power density (+1 rank)

Smaller size and weight at high power levels means high power density. High efficiency (above 98%) plus high power density will require a higher switching frequency for the semiconductors and transformer. This can be achieved only through soft-switching.

3.2.3 Pugh Matrix

In order to narrow down the list of options and increase confidence in which converter to proceed with, the Pugh Matrix is used to evaluate various alternatives against a baseline. In this case, the hard-switched full bridge converter (FB) is considered the base line and five criteria (which are actually the design drivers) are weighted. A 5-point scale is used (+2-much better than, +1-better than, 0-equal to, -1-worse than, -2-much worse than). As an

example, if a concept is much better than the base line on a 5 point weighted criteria, it will receive 10 points.

3.3 Selection results

3.3.1 F-FMEA results

Looking at the FMEA results from Table. 3.11, it is noticed that there are no differences between the topologies from the F-FMEA point of view. All sub-systems score the same RPN, as the topologies are very similar from components point of view. On the other hand, as the inverter has the highest number of functionalities, it scores the highest RPN number among the other sub-systems, followed by the rectifier, indicating that the designer should pay higher attention in this area, regardless of the selected topology.

Table 3.11: FMEA results

System Level	Topology normalized RPN *(SxOxD)*				
	FB	SAB	LLC	SRC	SRC#
Inverter/Ac-Ac*	42	42	42	42	42
Rectifier	35	**35**	35	35	35
LV DC-link/Clamp*	24	24	24	**24**	24
MV DC-link	21	21	21	21	21
Transformer	11	11	11	11	11
Disconnecter	11	11	11	11	11
Filter/Res.Tank	6	6	**6**	6	**6**

3.3.2 Comparison of availability

According to [96], availability for an offshore wind turbine is defined as the capability to operate from the technical point of view, without considering lack of wind, grid problems or ambient conditions such as gusts. One way of increasing availability and consequently energy production is through improvement of system reliability. In other words, prevention, correction and minimization of the number of failures should be the design philosophy of the DC/DC converter. One way of decreasing failure rates is through reduction of part count. This was one of the reasons of imposing a design constraint of the monolithic transformer, regardless of selected topology. At this point, due to low technology readiness level and the fact that there is no experience from full-scale designs, an empirical estimation for failure rate of the topologies proposed in this selection report is not possible. Nevertheless, the 5 topologies share exactly the same number of semiconductors (IGBTs and diodes) and identical transformer size, with the exception of the SRC, which has the transformer designed for 200 Hz. The FB and SAB each have

a filter inductor located on different positions, while the LLC and SRC# each have a LC tank in series with the transformer. Therefore, considering the same part number for each topology, in this study availability is considered to be the same.

3.3.3 Comparison of losses

The semiconductor and transformer loss model employed in this comparison is detailed in Appendix A.1 and A.2. Semiconductor losses are implemented on on-line simulation model, while transformer losses are calculated off-line. For IGBTs and diodes, conduction and switching losses are calculated according to methods proposed in [97], [98]. To calculate core losses P_v, the Improved Generalized Steinmetz Equation IGSE was employed. Simulated and calculated losses for the FB, SAB, LLC, SRC and SRC# are presented in Fig. 3.6(a, b, c, d and e).. Each figure shows total losses as a percentage of delivered power.

The FB converter has the highest amount of losses, close to 2.5% of delivered power, as seen in Fig. 3.6a. Due to hard turn on and turn off, switching losses represent the highest percentage of losses, ca. 2%. Transformer losses are only 0.2% at 1 pu output power. At low power, core losses are predominant, as they are a function of frequency Bmax and duty cycle, which varies between 33% and 44%.

In Fig. 3.6b, SAB losses show that conduction losses are similar to the FB, while there are no turn-on losses due to ZVS. Above 0.3 pu of nominal power, total losses drop below 2 % and stabilize around 1.5% at 1 pu. Transformer losses are 0.25% at 1 pu of output power. With a constant frequency of 1000 Hz, the duty cycle varies between 14% and 42%.

Further on, looking at Fig. 3.6c, LLC losses show a promising result, with losses below 1% for power above 0.2 pu. There are no turn-on losses, while turn-off losses are decreased compared to the FB and SAB. Regarding transformer losses, core losses are predominant, as compared to the SAB and FB, due to 50% duty cycle. On the other hand, exciting the transformer with 50% square wave voltage, means core losses are constant regardless of transmitted power, while the FB and SAB converters have core losses proportional to applied duty cycle.

Fig. 3.6d indicates the SRC total losses and it becomes clear that due to the generous transformer design, the SRC will pay a penalty on winding losses. Compared to Fig. 3.6c, it becomes clear that the semiconductor losses are similar to the LLC topology, but the difference in the transformer design plays a role. At elevated frequency, skin and proximity effects increase the winding ac resistance and impacts the transformer losses. For the frequency controlled SRC, this means winding losses are proportional to output power, increasing up to 6% at nominal power.

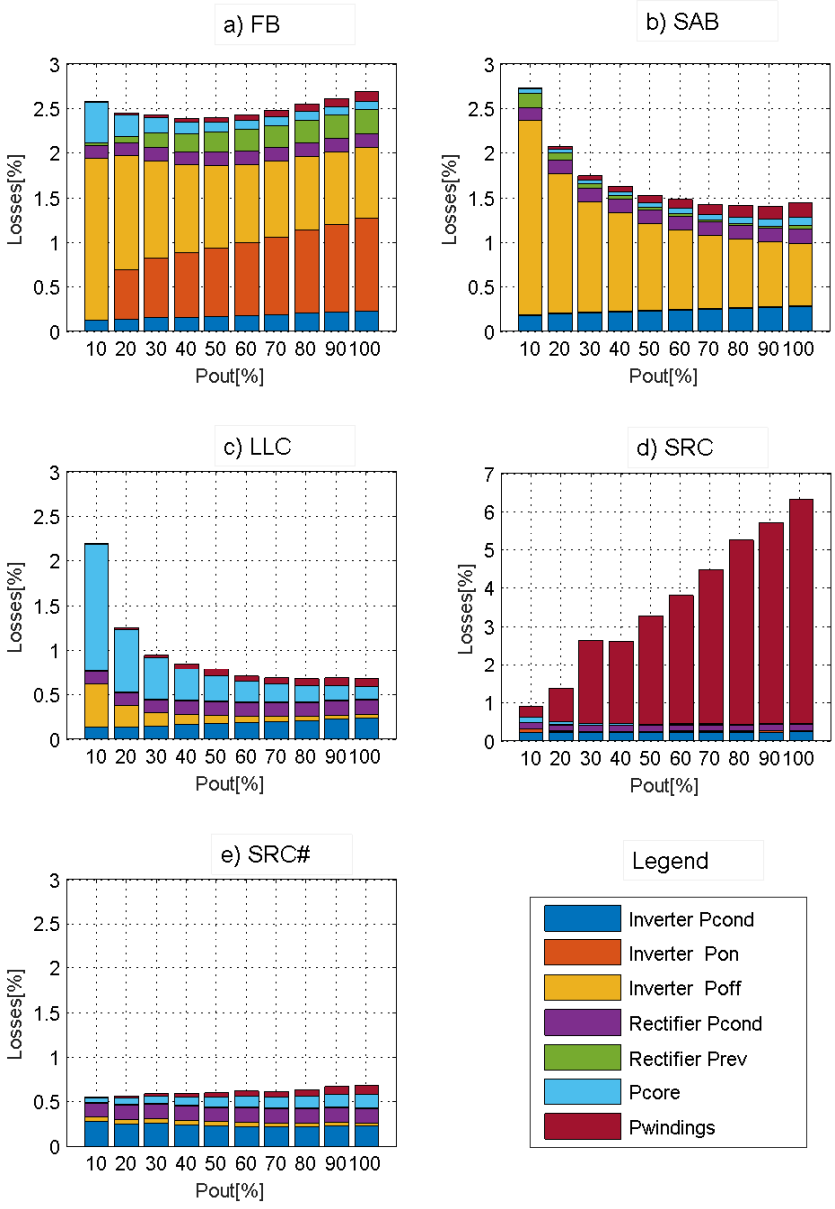


Fig. 3.6: Simulated electrical losses of selected topologies: a) FB; b) SAB; c) LLC; d) SRC; e) SRC#

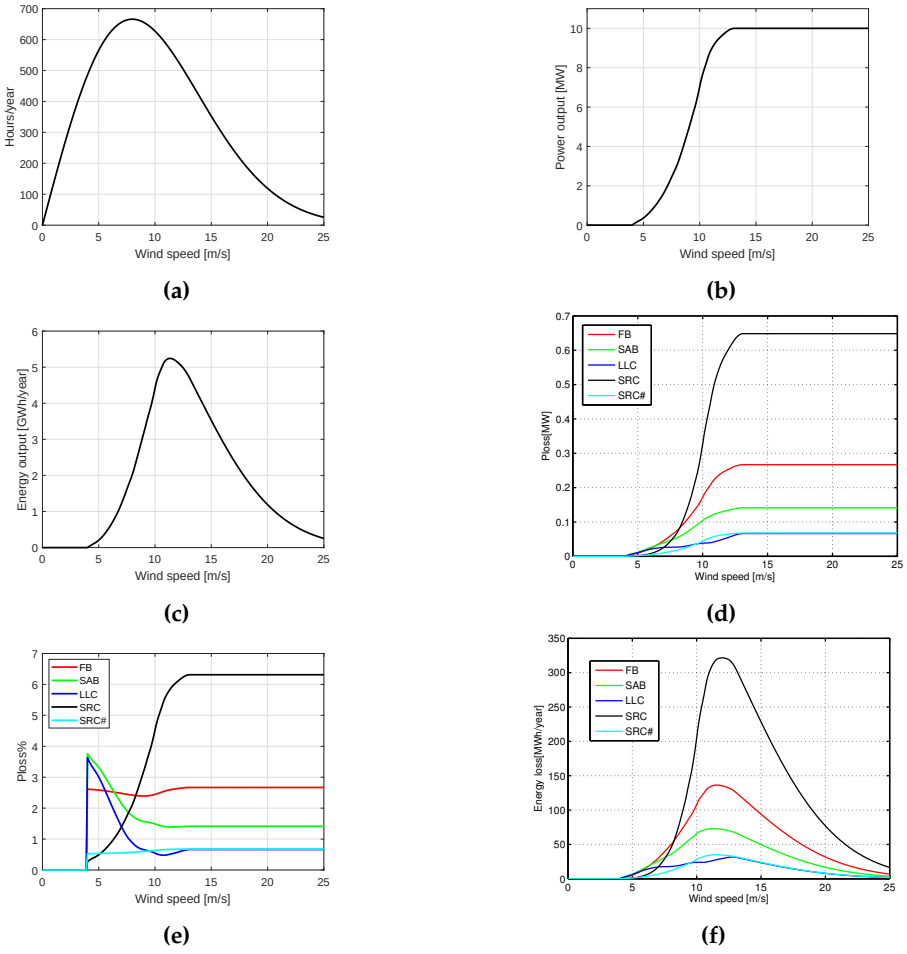
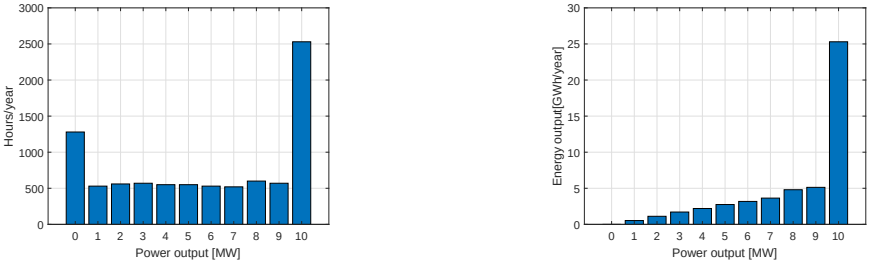
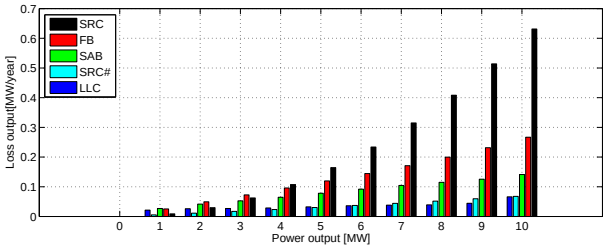


Fig. 3.7: a) Wind speed probability density of a typical offshore location; b) Power output curve for a 10 MW turbine; c) Energy output for a 10 MW turbine; d) Losses in absolut values; e) Losses in percentage; f); Annual energy loss distribution

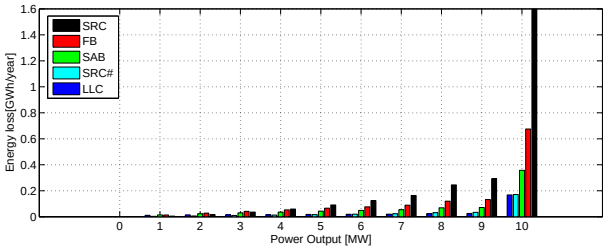


(a) **(b)**

Fig. 3.8: a) Power output vs. hours distribution; b) Annual energy output distribution



(a)



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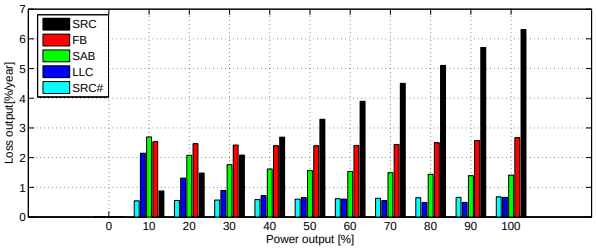

(c)

Fig. 3.9: a) Power output vs. losses; b) Power output vs. energy losses; c) Power output vs. energy losses%;

Fig. 3.6e shows SRC# losses, indicating losses below 1% for full operational range. Conduction losses are slightly higher than the other topologies, but due to no turn on losses and very low turn off losses, this topology shows the lowest amount of losses.

Considering the probability of the wind speed vs. number of hours per year of a typical offshore location (Fig. 3.7a) and the power output curve for a 10 MW turbine (Fig. 3.7b), the turbine energy output is then calculated in Fig. 3.7c. Further on, based on the specs from Table. 3.3, losses in absolut values and percentage are calculated for the 5 selected topologies in Fig. 3.7d and Fig. 3.7e.

As expected, due to the increased transformer size on the SRC, which are translated in windings losses, the proposes SRC has the highest amount of losses, regardless of wind speed. On the other hand, the LLC and the proposed SRC# have the lowest amount of losses regardless of wind speed. The interesting aspect of SRC# is that the percentage of losses are constant with respected to the wind speed. In the end, the total annual energy loss distribution with respect to the wind speed is plotted in Fig. 3.7f. Fig. 3.9a, 3.9b and 3.9c illustrate the power output vs. losses, energy losses and energy losses in percentage for the selected topologies.

3.3.4 Comparison of ratings

In Table 3.12, number of semiconductors, transformer weight, resonant/filter tank values and corresponding voltage and current stress are shown, indicating similar values. Due to this, it is considered that weighted rank for ratings and repair cost get same score for all topologies.

Table 3.12: Comparison of ratings

	FB	SAB	LLC	SRC	SRC#
IGBTs	4 x 3	4 x 3	4 x 3	4 x 3	4 x 3
Diodes	4 x 40	4 x 40	4 x 40	4 x 40	4 x 40
Vce_{pk}	1 pu	1 pu	1 pu	1 pu	1 pu
Ice_{pk}	0.44 pu	0.78 pu	0.6 pu	0.63 pu	0.63 pu
Vd_{pk}	0.68 pu	0.63 pu	0.63 pu	0.63 pu	0.63 pu
Id_{pk}	0.044 pu	0.078 pu	0.072 pu	0.072 pu	0.072 pu
Res/Fil.ind	200 mH	40 uH	250 uH	250 uH	78 mH
Res.cap	-	-	78 uF	78 uF	0.25 uF
L_m	5 mH	5 mH	5 mH	125 mH	5 mH
N_p	18	18	18	50	18
N_s	450	450	450	1225	450
M_{fe}	800 kg	800 kg	800 kg	880 kg	800 kg
M_{cu}	340 kg	340 kg	340 kg	2200 kg	340 kg

3.3.5 Comparison of power density

An initial strategy for comparison of weight and volume on selected topologies was to rank every unit with points. Final volume and weight are proportional to the number of points. The following assumptions have been considered, based on the fact that exactly same number of IGBTs and diodes were considered for every topology during loss analysis: inverter, rectifier, transformer and output filter have the same weight and volume for all topologies, and each is ranked with one point. One resonant component (inductor or capacitor) is ranked with one point. Based on Table. 3.13 scoring results, the SAB and FB converter should have the lowest weight and volume, while the resonant topologies the highest, as they need the resonant tank to have soft switching capability.

Table 3.13: Comparison of weight and volume

No	Topology	Inverter	Rectifier	MF Transformer	Inductor	Res.Cap	Score
1	FB	1	1	1	1	0	4
2	SAB	1	1	1	1	0	4
3	LLC	1	1	1	1	1	5
4	SRC#	1	1	1	1	1	5

3.3.6 Pugh matrix results

Looking at Table. 3.14, LLC and SRC# have the highest score, followed by SAB converter. Compared to the FB, they all have similar availability, ratings and repair costs, but the LLC and SRC# have much better efficiencies. The LLC and SRC# have very similar losses. LLC operates in open loop at constant frequency and 50% duty cycle. Even if this topology is proven in traction application, for dc wind turbines there are still high uncertainties. Finally the SRC# is able to deliver power in full operational range, with very small losses and minimized transformer size. The main disadvantage is the location of the resonant capacitor, which is subjected to high voltage transients and requires higher insulation, clearance and creapage. Therefore, considering the advantages and disadvantages, the SRC# is considered as preferred topology for dc wind turbines, followed by the LLC and SAB converters.

3.4 Conclusions

As no substantial experience from full scale detail design exists, the selection of the optimal DC/DC converter technology for DC wind turbines is difficult. A methodology was suggested, by downselection of circuits based on a set of fundamental requirements. 5 topologies (the full brige converter, the single

Table 3.14: Pugh matrix

Criteria	Base line FB	Weight	Concept			
			SAB	LLC	SRC	SRC#
Avail.	0	5	0	0	0	0
Losses	0	4	+4	+8	-8	+8
Ratings/Cost	0	3	0	0	-6	0
Repair costs	0	2	0	0	-2	0
Power density	0	1	+1	-1	-2	-1
Σ Total:			+5	+7	-18	+7

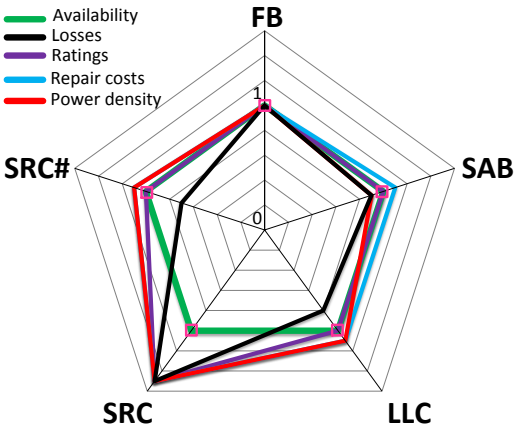

Fig. 3.10: Selected topologies for comparison.

active bridge, constant frequency LLC converter and two variants of the series resonant converter were commpared with respect to different design drivers, such as: availability, losses, ratings, repair costs and power density and. The functional failure mode and effect analysis (F-FMEA) and Pught Matrix have been proposed as tools of comparison. Finally, a variant of the series resonant converter, namely the SRC# was considered as the preferred topology.

The proposed circuit will be discussed in following chapters, with focus on its advantages and disadvantages, modes of operation, conduction modes, control architecture, sensitivity analysis and finally a design guide line is proposed.

Chapter 4

Series resonant converter - SRC#

Summary

This chapter discusses the series resonant converter as a good candidate for the high power dc/dc converter located in the wind turbine. A review of classic series resonant converter with possible modes of operation is given. Frequency controlled SRC in sub-resonant mode is attractive as it is able to control the input dc-link. But the main disadvantage lies in the design of transformer for lowest switching frequency. A novel modulation scheme is introduced, which permits regulation of power from nominal level to zero. The circuit is named SRC# and has the LC tank located on the rectifier side of the high-turns ratio transformer and it's controlled through variable frequency and phase shift modulation. Circuit operation, conduction modes, governing equations and steady state waveforms are illustrated. This chapter is based on work presented in [88], [99], [100].

4.1 Introduction

The offshore wind farm with MVDC collection (as seen in (Fig.7.7a) requires a turbine converter that employs a DC/DC converter with high availability, efficiency and power density as design targets, and considering the high voltage specifications, a transformer with high turns ratio should be employed. The problem of high frequency and high voltage transformers is that they suffer from the impact of leakage inductance and winding capacitance. This will lead to unwanted voltage spikes across circuit components, current overshoots and slow rise time [40]. These are strong arguments which favor the use of a series resonant converter as an optimal candidate, as through the use of a series resonant tank, the leakage inductance can now be incorporated in the resonant tank and help reduce switching losses. A candidate solution, entitled SRC# (as in series resonant converter sharp) is proposed in Fig.7.7b. The need of SRC# operated with a novel mode of operation, entitled pulse removal technique is presented in the following paragraphs.

According to [41], the initial use of the series resonant LC-circuits in power converters was in auxiliary commutation circuits for thyristors, as the auxiliary impulse-commutated inverter [101]. Afterwards, the first series resonant DC-to-DC converters was proposed in [37], while in [102] the advantages of reducing losses, increasing power density and power level are discussed. Further on, in the eighties the topology with bipolar transistors and mosfets was discussed in [39]. The use of variable switching frequency to control output voltage and a continuous and discontinuous DC characterization was performed in [103]. Afterwards a close form solution and a new approach to the analysis of the series resonant converter is presented in [104] and followed by a design of the series resonant converter for minimum com-

ponent stress [105]. State plane analysis is discussed in [106] and Optimal trajectory control is proposed in [107].

In high power operation, the topology has been investigated in traction applications [43], [58], [60], [108], [109] and in solid-state transformer applications [73], [110], [111]. In these applications, the topology was operated at constant frequency and in sub-resonant mode. The proposed SRC is known as the half cycle discontinuous-conduction-mode series-resonant converter (HC-DCM-SRC). For these particular applications, the converter couples two DC link voltages with a fixed voltage transfer ratio, but has no control possibilities (Fig.4.2a).

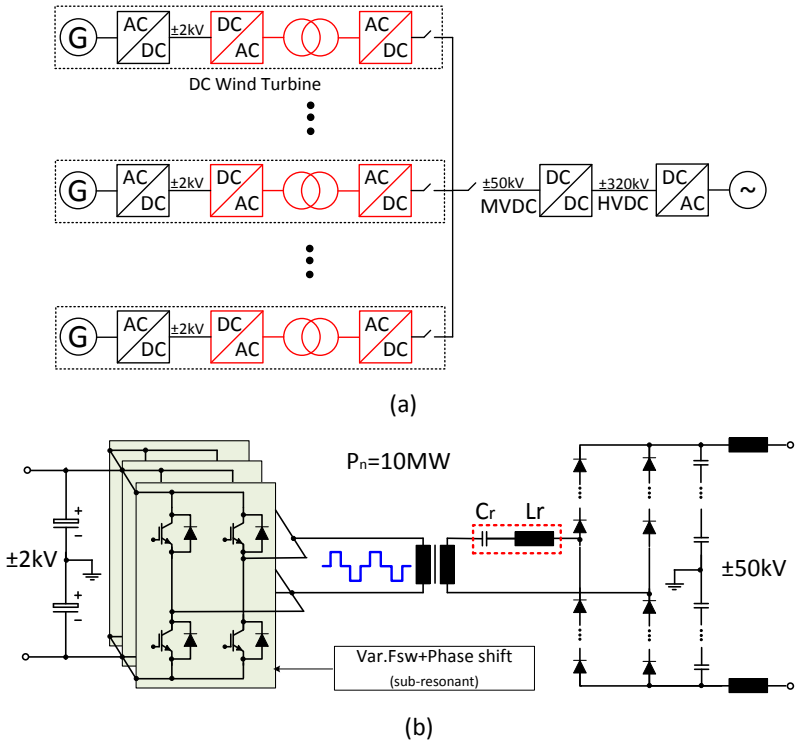

Fig. 4.1: (a) Single line diagram of DC wind farm; (b) Series resonant converter with new method of operation (SRC#), [99]

For a wind turbine on the other hand, the DC/DC converter must have the functionality of controlling the LV DC bus voltage, while offering galvanic separation and a high voltage gain. A candidate solution (cf. Fig. 4.2b) was proposed in [18] and it employs a SRC, operated at resonant mode and with constant frequency, while a front end boost converter controls the input DC-

link, increasing thus number of components, complexity and losses.

In [112] (Fig. 4.3), a per-phase configuration of the series resonant converter is proposed, with three single phase rectifier series-connected on the output. The topology is controlled through variable duty cycle and constant frequency, while being operated exclusively in super-resonant mode. The drawback of this mode are hard turn-off losses on both inverter and rectifier side switches. No efficiency analysis or measurement was reported and the circuit would appear to suffer from technical barriers on implementing 2-3 MVA, 10-kHz monolithic transformers. Non-isolated topologies have also been proposed in prior art: [15] and [113] propose a single and three phase topology, while employing low-cost thyristors. The topology is similar to a parallel resonant converter, but suffers from high voltage stress across the semiconductors and resonant tank. In a DC wind turbine application, galvanic separation is preferred for protection and safety reasons, by effectively decoupling the generator and its rectifier from that of the dc/dc converter.

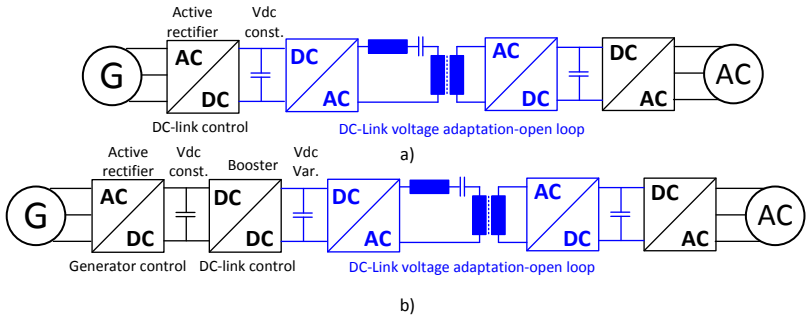

Fig. 4.2: a) Turbine converter with SRC operated in sub-resonant mode at constant frequency in open loop; b) Concept with DC/DC converter operated at resonant mode and constant frequency in open loop.

In order to control the LV DC bus voltage, a method of operation is proposed for the SRC, where variable frequency and phase shift control in sub-resonant mode are applied. The benefits and deficits of the method are discussed and compared to a SRC operated only with frequency control. The review of classic SRC is performed and it motivates the need for pulse removal technique, in order to avoid a bulky transformer. Four modes of operation (DCM1, DCM2, CCM1-hybrid and CCM1) are identified and analysed.

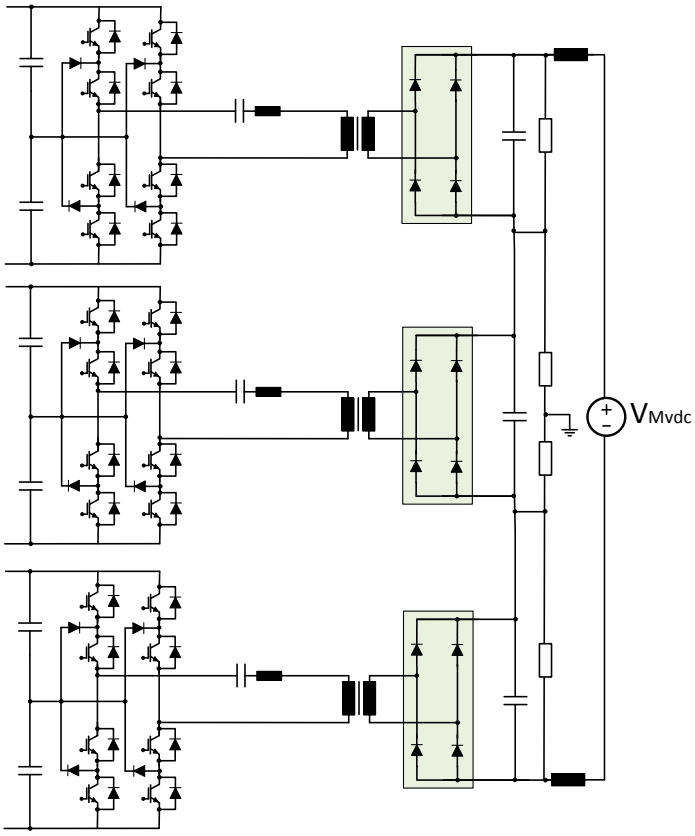

Fig. 4.3: Per-phase configuration of SRC proposed in [112].

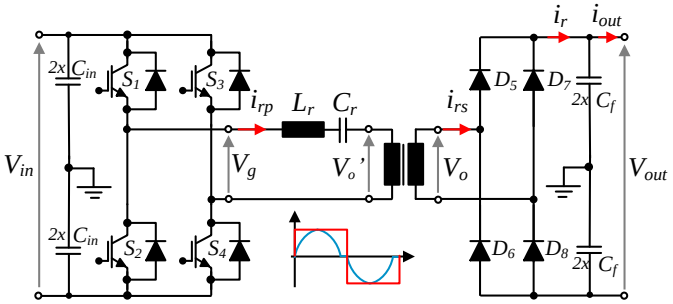

Fig. 4.4: Series resonant converter (SRC) with LC tank on primary side. [99]

4.2 Review of classic series resonant converter

4.2.1 Theory of operation

In order to fully comprehend pulse removal technique, a review of series resonant converter modes of operation and control is necessary. Therefore, consider the first SRC design, with tank on inverter side, as shown in Fig. 4.4, where initially the transformer magnetizing inductance L_m is neglected. When the two complementary switching pairs (S1, S2) and (S3, S4) are opened and closed alternately, a square wave voltage V_g of defined frequency F_{sw} and duty cycle D is applied to the resonant LC tank while on the rectifying bridge, the diodes are in operation. The resonant frequency F_r, resonant angular frequency ω_r and characteristic impedance of the tank are further defined in eq. (4.2), (4.3) and (4.3). V_g generates a resonant current i_{rp} in the tank circuit, which when rectified and filtered is fed into the output voltage network. The magnitude and shape of the output current is determined by the ratio between F_{sw} and F_r. This explanation is valid for all modes of operation [103]-[104].

$$F_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{4.1}$$

$$\omega_r = 2\pi F_r \tag{4.2}$$

$$Z_c = \sqrt{\frac{L_r}{C_r}} \tag{4.3}$$

4.2.2 Possible modes of operation

For a SRC, three modes of operation are possible: sub-resonant mode (Fig. 4.5a and Fig 4.5b), resonant mode (Fig. 4.5c) and super-resonant mode (Fig. 4.5d). In sub-resonant mode, F_{sw} is lower than F_r, while in super-resonant mode it's higher. In resonant mode F_{sw} is equal to that of the resonant tank, meaning switching occurs exactly at the zero crossing event of the current. For both sub-resonant and super-resonant modes, two states of conductions can exist: continuous and discontinuous. Discontinuous conduction mode (DCM-Fig. 4.5a) for sub-resonant mode is characterized by the presence of zero current sub-interval and further exemplified in the Appendix. In that period, all of the rectifier diodes are reversed biased, until V_g changes sign. Continuous conduction mode (CCM-Fig. 4.5b is characterized by the resonant tank current reversing polarity before the end of the inverter pulse ends/ transistor pair turns off. Regarding control methods, three different methods are identified in prior art for sub-resonant and super-resonant mode: frequency control (see Fig. 4.5 a, b, c, d), phase shift control (see Fig. 4.5 e, f) and

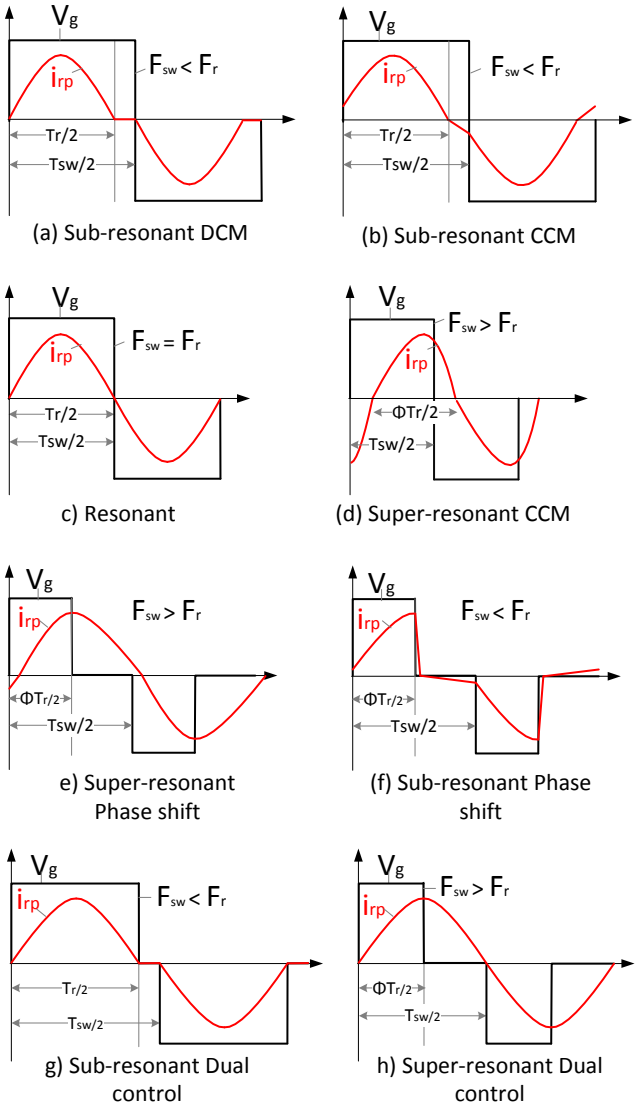

Fig. 4.5: SRC modes of operation and control methods: frequency control (a,b,c,d); phase shift control (e,f); dual control (g,h). [99]

Table 4.1: Inverter switching characteristics for SRC operating modes

	Turn on	Turn off
Frequency Control Sub-resonant DCM	ZVS	ZCS
Frequency Control Sub-resonant CCM	Hard	ZCS
Frequency Control super-resonant	ZVS	ZCS
Resonant mode	ZVS	ZCS
Phase shift sub-resonant	Hard	Hard
Phase shift super-resonant	ZVS	Hard
Dual control sub-resonant	ZVS	ZVS
Dual control super-resonant	ZVS	Hard

dual control (see Fig. 4.5 g, h). By frequency control of excitation voltage V_g, the effective resonant tank impedance varies with the switching frequency. The phase-shift method is controlling the excitation voltage to the resonant tank by changing the duty cycle of the inverter (square wave) voltage, with constant switching frequency . It can be applied in super-resonant mode (Fig. 4.5e) or sub-resonant mode (Fig. 4.5f). With dual control, a combination of variable frequency and phase-shift is applied in order to control transformer primary voltage and the switching current. Dual control in super resonant mode (Fig. 4.5h) has been published in prior art [114], while the dual control in sub-resonant mode (Fig. 4.5g) has not been investigated. Pulse removal technique belongs to this area. Switching characteristics at turn on and off for frequency, phase shift and dual control are listed in Table 4.1.

4.2.3 Selection of mode of operation and control method

The mode of operation and control method for the SRC are in general selected to suit the application. For example, at low power and high voltage, applications prefer super resonant and phase shift control [115]-[116] due to ZVS at turn-on (as mosfets are used) and control simplicity. A three phase variant of the SRC operated in resonant mode is described in [117] and [41] and promises efficiency above 99% but lacks controllability, meaning power is a function of input and output voltage levels. On the other hand, constant frequency and sub-resonant mode are applied in traction and solid state applications like [118].

Selection of operating mode and control method are based on inverter side device selection (mosfet vs. igbt) and application requirements (low power vs. high power). Considering the high power and medium voltage application in this case, 6.5 kV IGBTs are proposed on the inverter side, while 6.5kV line frequency diodes are used on rectifier side. Most of the available publications (and commercial products) which use a resonant topology are addressing low power and low voltage applications and are using mosfets

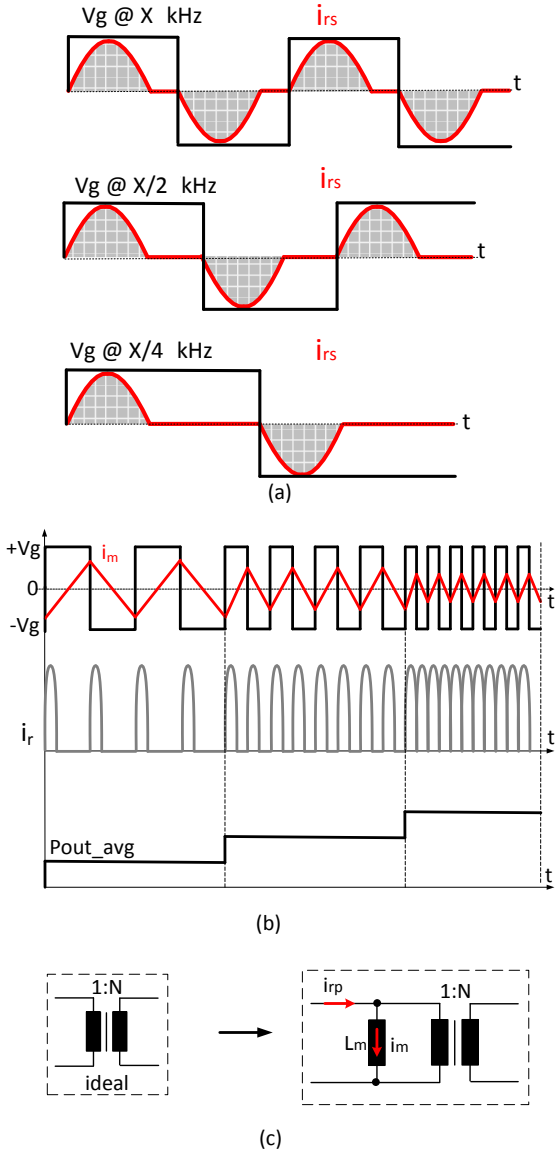

Fig. 4.6: Frequency control of SRC in sub-resonant DCM: operation with different F_{sw} (a); impact of variable F_{sw} on magnetizing current (b); ideal and non-ideal transformer (c). [99]

with switching frequencies in the range of hundreds of kilohertz. For those kind of applications, super-resonant mode is attractive, as it allows ZVS (zero voltage switching) at turn-on. But, as also stated in [87], the main contributors to the overall losses with igbt applications are the turn-off losses. According to [119] and [120] the main reason is that these semiconductors are characterized by a bipolar power stage, that, in order to block HV (high voltage), comprise a considerable large N-base region, which stores a large amount of charge during the conduction phase of the semiconductor. When the switch is turned off, this stored charge is evacuated from the semiconductor, causing tail currents that overlap with the blocking voltage, generating high switching losses. Therefore, a mode of operation that allows ZCS (zero current switching) or at least a low current at turn-off needs to be selected. The obvious mode of operation is therefore sub-resonant mode for IGBT applications. Another particular reason why sub-resonant operation is attractive and with reference to Fig. 4.6a is that regardless of switching frequency, during every switching period a full resonant pulse is sent to the load. This means if the converter operates in DCM mode, intervals of zero current will appear. Further on, if frequency control is implemented, output average power is a function of number of resonant current pulses transferred to the output, as seen in Fig. 4.6b. For an SRC operated in DCM mode, a current pulse is dependent on the resonant capacitor C_r and its voltage V_{Cr}, as it determines the stored charge q_s, shown in eq. (4.4), where $V_{Cr} = 2 \cdot V_{in}$.

$$q_s = C_r \cdot (2V_{Cr}) \tag{4.4}$$

The relation between output averaged current and stored charge is given by eq. (42):

$$i_{out} = \frac{2 \cdot q_s}{t_s} = 2 \cdot q_s \cdot F_{sw} \tag{4.5}$$

Combining eq. (4.4) into (4.5), will give (4.6):

$$i_{out} = 8 \cdot C_r \cdot F_{sw} \cdot V_{in} \tag{4.6}$$

Considering that $P_{out} = I_{out} \cdot V_{out}$ and $V'_{out} = \frac{V_{out}}{N}$ the previous mentioned relation between output power and switching frequency is determined in (43):

$$P_{out} = \frac{8 \cdot C_r \cdot F_{sw} \cdot V_{in} \cdot V_{out}}{N} \tag{4.7}$$

Thus, if an SRC should be operated only in DCM mode, eq. (43) provides a simple function, which could be implemented as a feedforward controller. Low frequency operation means low power output, while high frequency operation will deliver a high power output. On the other hand, the disadvantage of operating the SRC with resonant tank on inverter side in sub-resonant

mode and frequency control, is that the transformer needs to be designed for the lowest frequency point and the magnetizing inductance needs therefore to be considered, as seen in Fig. 4.6c and included in the schematic. Fig. 4.6b (top) shows how the magnetizing current i_m varies with frequency, in direct relation with applied volt-seconds. Below lowest operational frequency, saturation and transformer induced oscillations will occur [121], [122]. A means of avoiding this must be implemented, otherwise, designing medium frequency transformers with SRC operated in sub resonant mode is not possible.

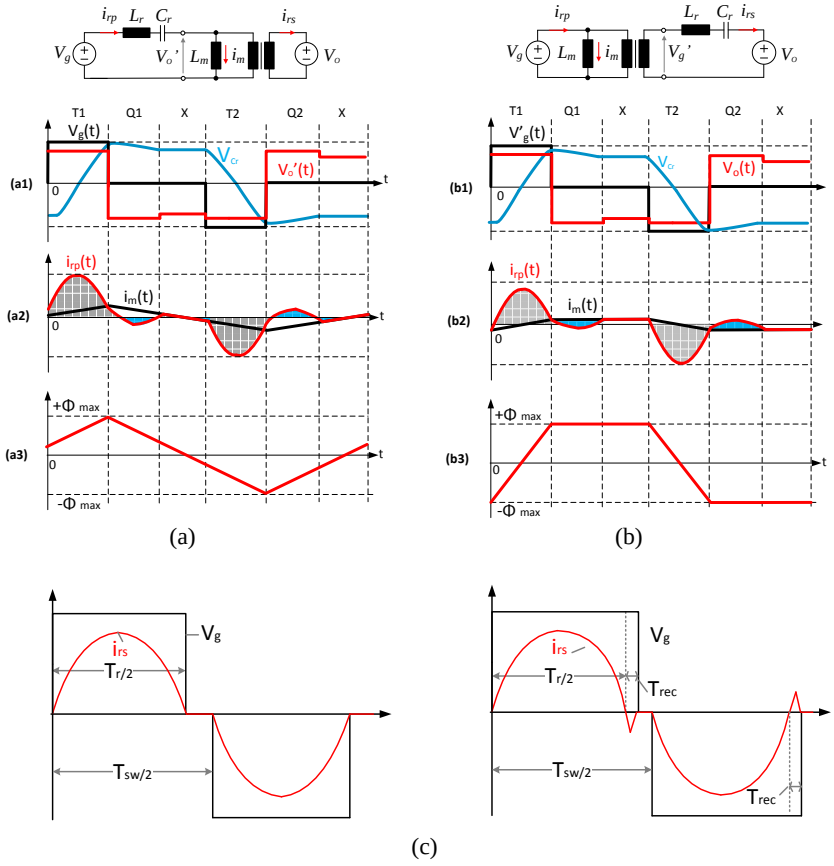

Fig. 4.7: Characteristic waveforms for SRC# with tank on inverter side (a) and rectifier side (b): (a1,b1) - inverter voltage V_g, rectifier voltage V_o, resonant capacitor voltage V_{cr}; (a2,b2) - primary resonant current i_{rp}, magnetizing current i_m; (a3,b3) - magnetic flux Φ; c) Impact of rectifier diode reverse recovery on length of V_g voltage pulse. [99]

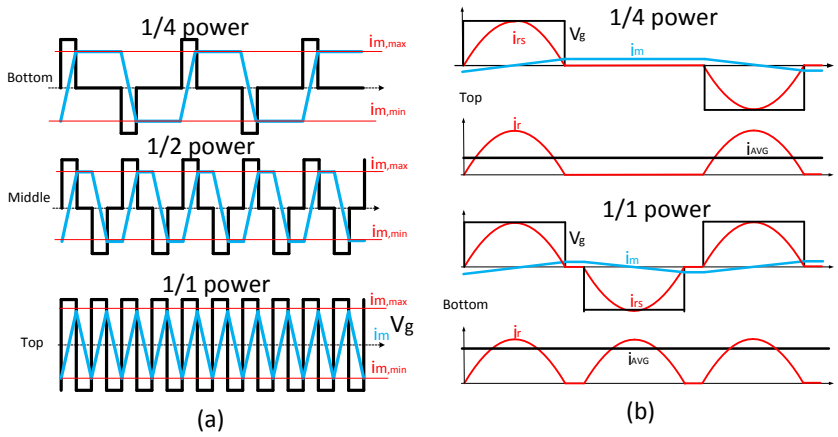

Fig. 4.8: Pulse removal technique (a); Operation of SRC# at low and high power (b). [99]

4.3 Operation principle of the SRC#

4.3.1 Pulse removal technique

Pulse removal technique was initially described in [88] and it is further explained in following paragraphs. As mentioned previously, sub-resonant operation and frequency control are optimal for IGBT applications as they allow soft-switching at turn-off and allow the SRC to control output power. The question is now, how can the transformer be operated with variable frequency and be designed at highest operating frequency, while avoiding saturation at lower frequency. One possible way and with reference to Fig. 4.8a, is V_g becomes a function of number of pulses, meaning a pulse with determined length is applied to the inverter, but the time between pulses varies as a function of desired power. As the temporal length of every voltage pulse is fixed, the amplitude of the magnetizing current i_m will be constant. Fig. 4.8a (bottom) shows the inverter voltage V_g operating at highest frequency, providing the maximum number of voltage pulses per unit time, while $\mid i_m \mid$ stays below the defined maximum value. Fig. 4.8a (middle) and (top) indicate that if variable zero voltage periods are inserted between the pulses, $\mid i_m \mid$ will not go above maximum values, but remain constant. Further on and with ref. to Fig. 4.8b, if the applied voltage V_g has the same duration as the resonant pulse i_{rs}, then frequency control in sub-resonant mode becomes possible, allowing the design of the transformer for highest operating point. In particular, Fig. 4.8b (top) relates to a lower power output (fewer current pulses) than Fig. 4.8b (bottom), which relates to higher power output. An-

other aspect worthy of mention is that the length of one V_g pulse needs to include the impact of rectifier diode reverse recovery time T_{rec}, as seen in Fig. 4.7c.

4.3.2 Resonant tank on inverter or rectifier side

Applying pulse removal technique is successful only if the resonant tank is placed on the rectifier side of the transformer, as explained in the following. When the LC tank is placed on the inverter side, V_g is the inverter voltage and V_o' is the rectifier voltage reflected on inverter side, the main goal is to achieve zero volts on transformer primary winding, as soon as the resonant current reaches zero, thus stopping any flux build-up. Consider the equivalent circuits and corresponding waveforms of SRC with tank on inverter side (Fig. 4.7a) and with tank on rectifier side (Fig. 4.7b). In the first case, transformer primary voltage is the rectifier reflected voltage on inverter side, namely V_o'. Looking at principle waveforms from Fig. 4.7a (a1), it is noticed that even if V_g is clamped to zero during Q1 sub-interval, the resonant capacitor voltage V_{C_r} is slowly discharged through the magnetizing inductance, preventing zero volts on the primary winding terminals. During sub-interval X, the transformer primary winding voltage is equal to the capacitor voltage, but with an opposite polarity. In other words, it is not possible to have zero volts on primary winding, even if V_g is zero. Fig. 4.7a (a2) and (a3) show the primary resonant current i_{rp}, magnetizing current i_m and the magnetic flux Φ, as a function of V_o' and time.

In the second case with LC tank on the rectifier side, (see Fig. 4.7b (b1), the transformer primary excitation voltage will be controlled directly through V_g, thus limiting the volt-seconds and allowing for lower magnetizing flux, as seen in Fig. 4.7b (b3). Comparing the shape of magnetizing current i_m from Fig. 4.7b (b2) to the one from Fig. 4.7a (middle), it becomes evident why pulse removal technique is efficient only with the LC tank on rectifier side. Another feature is that the tank needs to be designed for medium voltage levels, with impact on insulation, clearance and creepage specifications.

With this arrangement, operating in a sub-resonant mode permits a full resonant cycle of the LC circuit current to pass within a single switching cycle of the full bridge, allowing ZVS at turn-on and a low turn-off current for inverter switches, while the rectifier diodes will experience ZVS at turn-on and ZCS at turn-off.

4.3.3 Description of SRC#

The series resonant converter with the new method of operation (SRC#) is depicted in Fig. 4.9 and comprises a full bridge inverter, monolithic 1:N transformer, resonant tank and medium voltage rectifier. Power flows from

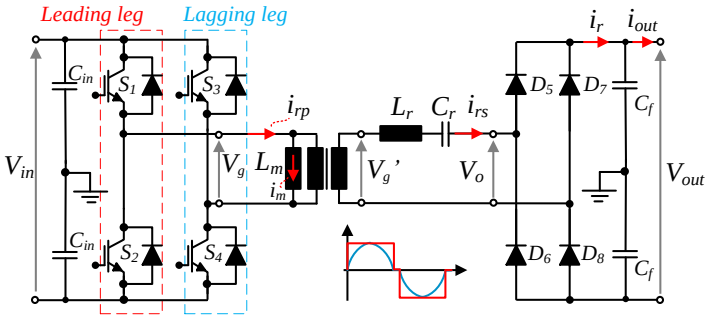

Fig. 4.9: Full bridge Series resonant converter with new method of operation: SRC# [99]

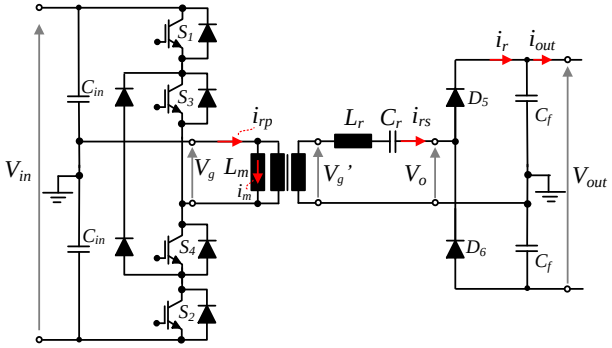

Fig. 4.10: NPC Series resonant converter with new method of operation: SRC#

V_{in} to V_{out}. A 3-level variation with half-bridge rectifier is also illustrated in Fig. 4.10.

The switch pairs (S1/S2) and (S3/S4) as indicated in Fig. 4.12a, operate at a 50% duty cycle. Determining (S1,S2) as leading leg, will generate Q1 and Q2 sub-intervals (Fig. 4.12b), while if (S3,S4) is the leading leg, will determine P1 or P2 sub-intervals (Fig. 4.12c). Q and P sub-intervales are explained later in the chapter. For simplicity, in the following paragraphs (S1, S2) is considered the leading leg. Commutation of switches on the leading leg is phase shifted with respect to the conduction of switches on the lagging leg, with a duration δ, equal to a resonant period, resulting in a quasi-square excitation voltage as seen in Fig. 4.12a. The applied square-wave voltage is scaled through the transformer (V_g referred to rectifier side is V_g') and excites the tank and a resonant tank current i_{rs} starts to flow. After rectification and

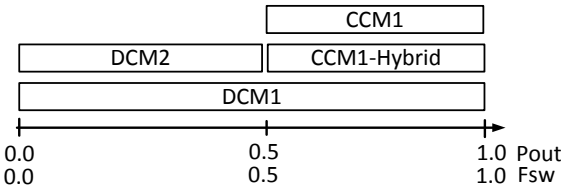

Fig. 4.11: Power to frequency relationship, for an SRC#

filtering it is fed into the medium voltage network, V_{out}. Up to this point there is no operational difference compared to a constant frequency phase shift control, which has been reported for operation in super resonant mode, to achieve ZVS at turn on. As igbts are employed, ZCS or at least a low current at turn off is highly sought, so the SRC# operates in sub-resonant mode. The particular case for SRC# is that the implemented phase shift temporal duration equals to the resonant pulse (Tr/2), as seen in Fig. 4.14a. This means that as soon as the secondary resonant current reaches zero, V_g' is switched to zero, i.e. the "pulsed voltage is removed". Now, because the converter needs to control output power, just like in the case of frequency control of the classical SRC, also here output power has a linear relation to the number of resonant pulses transferred per second, as depicted in Fig. 4.11. Therefore, the pulse pattern of the excitation voltage V_g, is determined by F_{sw} and phase shift δ. This means the zero voltage sub-interval has different lengths for different power levels.

4.3.4 SRC# conduction modes

Considering that SRC# is operating in sub resonant mode, four modes of conduction (two discontinuous and two continuous) will appear under steady state operation: DCM1, DCM2, CCM1-hybrid and CCM1. Switching frequency F_{sw} and voltage difference ΔV between inverter voltage reflected on rectifier side $V_g{}'$ (where $V_g{}' = V_g \cdot N$) and V_o will determine whether the converter operates in one conduction mode or another. A summary of these conditions is shown in Table 4.2. Discontinuous and continuous modes are characterized by the number of half resonant cycles that appear during a half switching period, with the difference that in DCM modes, a period of no conduction appears, while in CCM modes the current never ceases to flow. [103].

DCM1 can occur in the entire operating range (for frequencies from 0 to F_r) during transient states, when the resonant capacitor voltage is increasing or decreasing to certain values. DCM2 can occur only for frequencies below $F_r/2$, as two half resonant cycles followed by no conduction period are not

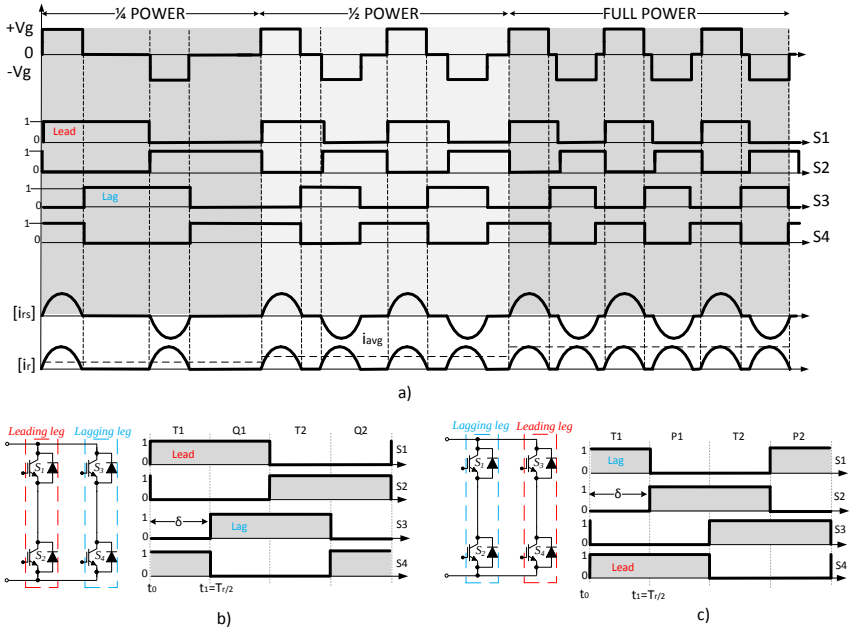

Fig. 4.12: SRC# switching pattern (a); Switching pattern with (S1,S2) as leading leg (b); Switching pattern as (S3,S4) leading leg (c). [99]

possible above half of F_r. Transition from DCM1 to DCM2 will occur, as soon as $V_{Cr} \geq V_o$, implying energy will flow towards output voltage network. Transition from DCM1 to CCM1-hybrid occurs when $F_{sw} \geq F_r/2$. As ΔV determines peak resonant current and voltage, when $V_{Cr} \geq (V'_g + V_o)$ and $F_{sw} \geq F_r/2$, transition to CCM1 mode will occur.

A one-cycle operation of SRC# is (regardless of conduction mode) composed of a sequence of linear circuits, each corresponding to a particular switching interval, as seen in Table 4.3. Every linear circuit is determined by switching certain switch pairs, as described in Fig. 4.13(a to i) and in Table 4.4. For even further clarification, Fig. 4.14 (a, b, c, d) presents secondary and primary resonant currents with their corresponding conductive devices per sub-intervals for every mode of operation.

4.3.5 Equations for subintervals

The time domain is used to investigate the behaviour of the SRC# operated with variable frequency and phase shift modulation. From the equivalent circuits, steady state equations of resonant inductor and capacitor voltage for every mode are derived by Laplace transform. Considering the half wave

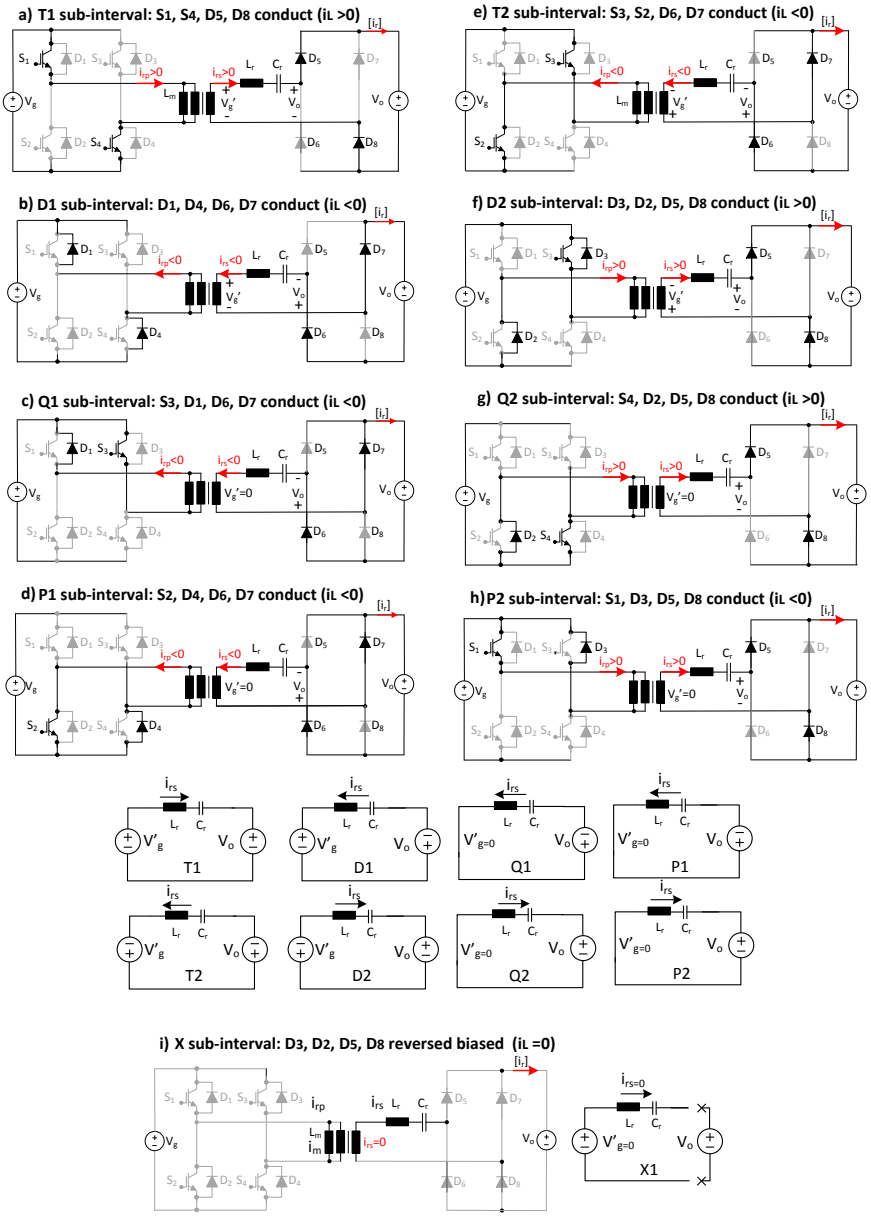

Fig. 4.13: Equivalent circuits for SRC# subintervals : T1 (a); D1 (b); Q1 (c); P1 (d); T2 (e); D2 (f); Q2 (g); P2 (h); X (i). [99]

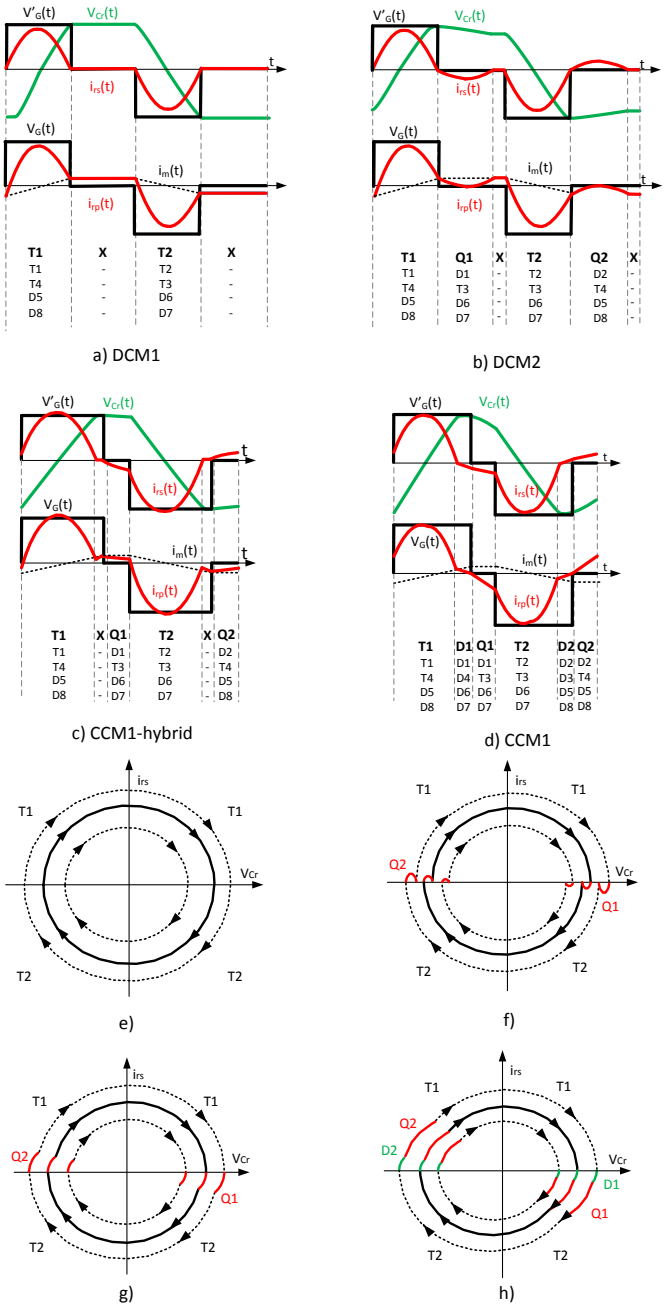

Fig. 4.14: Secondary (top) and primary (bottom) resonant currents with their respective conductive devices per sub-intervals in DCM1 (a); in DCM2 b); in CCM1-hybrid (c) and in CCM1 (d). State plane characteristic of resonant inductor i_{rs} vs. resonant capacitor voltage V_{Cr} in DCM1 (e); DCM2 (f) ; CCM1-Hybrid (g) and CCM1 (h). [99]

Table 4.2: SRC# conduction modes and boundary conditions

Mode of operation	Range of switching frequency	Cap. volt. condition
DCM1	$0 \rightarrow F_r$	$V_{Cr} < V_o$
DCM2	$0 \rightarrow F_r/2$	$V_{Cr} > V_o$
CCM1-hybrid	$F_r/2 \rightarrow F_r$	$V_{Cr} < V'_g + V_o$
CCM1	$F_r/2 \rightarrow F_r$	$V_{Cr} > V'_g + V_o$

Table 4.3: Sequence of subintervals for different modes

Mode of operation	Subinterval sequence
DCM1	T1-X-T2-X
DCM2	T1-Q1-X-T2-Q2-X
CCM1-Hybrid	T1-X-Q1-T2-X-Q2
CCM1	T1-D1-Q1-T2-D2-Q2

symmetry of tank variables, the analysis is performed for half cycle of switching period for every mode of operation. Similar to [115] the circuit behaviour of the SRC# under each topological mode can be described using the following differential equations, for subintervals T1, D1, T2, D2, Q1, Q2, P1, P2 and X, where V_t is the resonant tank voltage:

$$L_r \frac{di_{rs}}{dt} + V_{Cr} = V_t \tag{4.8}$$

$$C_r \frac{dV_{Cr}}{dt} = i_{rs} \tag{4.9}$$

$$V_t = \begin{cases} V'_g - V_o \text{ , for T1} \\ V'_g + V_o \text{ , for D1} \\ +V_o \text{ , for Q1} \\ -V'_g + V_o \text{ , for T2} \\ -V'_g - V_o \text{ , for D2} \\ -V_o \text{ , for Q2} \\ V_{Co} \text{, for X} \end{cases} \tag{4.10}$$

(4.11)

For subinterval X:

$$L_r \frac{di_{rs}}{dt} = 0 \tag{4.12}$$

$$C_r \frac{dV_{Cr}}{dt} = 0 \tag{4.13}$$

By solving equations eq. (4.8) and eq. (4.9), expressions for i_{rs} and V_{Cr} in each subinterval can be derived, with application of the consistent initial

Table 4.4: Conducting devices for different sub-intervals

Subinterval	$T1$	$D1$	$Q1$	$P1$	$T2$	$D2$	$Q2$	$P2$	X
Inverter	S1	D1	D1	S2	S2	D2	D2	S1	-
Side	S4	D4	S3	D4	S3	D3	S4	D3	-
Rectifier	D5	D6	D6	D6	D6	D5	D5	D5	-
Side	D8	D7	D7	D7	D7	D8	D8	D8	-
V_g' sign	+	+	0	0	-	-	0	0	0
V_o sign	+	-	-	-	-	+	+	+	0
V_t sign	+	+	+	+	-	-	-	-	0

conditions for each subinterval:

$$i_{rs} = \frac{V_t - V_{Cr}(t_0)}{Z_c} \sin \omega_r t + i_{rs}(t_0) \cos \omega_r t \tag{4.14}$$

$$V_{Cr} = V_t - (V_t - V_{Cr}(t_0)) \cos \omega_r t + i_{rs}(t_0) Z_c \sin \omega_r t \tag{4.15}$$

Considering that $V_t = V_g' - V_o$, the polarity of V_t is determined by the specific sub-intervals and conductive devices, as seen in Table. 4.4.

DCM1

With reference to Fig. 4.15, $DCM1$ mode can appear in the entire operational range and it Is possible only if $\Delta V \approx 0$ and $V_{Cr} \leq V_g'$. Fig. 4.15 shows on top the inverter voltage reflected on rectifier side V_g', rectifier voltage V_o and secondary resonant current i_{rs}. Middle graph describes resonant capacitor voltage V_{Cr}, while lower graph indicates the transistors (S1 to S4) switching pattern.

This mode of operation is composed of following sub-intervals: T1-X-T2-X. The sub-intervals equivalent circuits are shown in Fig. 4.13 (a), (e) and (i). Due to symmetry of operation over an entire switching interval, the analysis is performed over half the switching interval.

DCM1: Sub-interval T1

$t_0 \leq t \leq t_1$ This sub-interval starts when both S1 and S4 conduct, exciting the resonant tank with positive voltage V_g'. On the rectifier side, D5 and D8 are forward biased and the tank will be exposed to the rectifier voltage V_o. A positive inductor current rises from 0 with di/dt limited by the resonant tank elements, as long as $V_g' > V_o$. At $t_0 = 0$, the inductor current is zero due to the discontinuous nature of the inductor current in this mode. Resonant capacitor voltage rises from a negative V_{Cr} towards a positive value. So, both i_{rs} and V_{Cr} increase to positive values. This ensures ZVS turn-on on inverter side switches S1 and S4 and for rectifier side diodes. During this

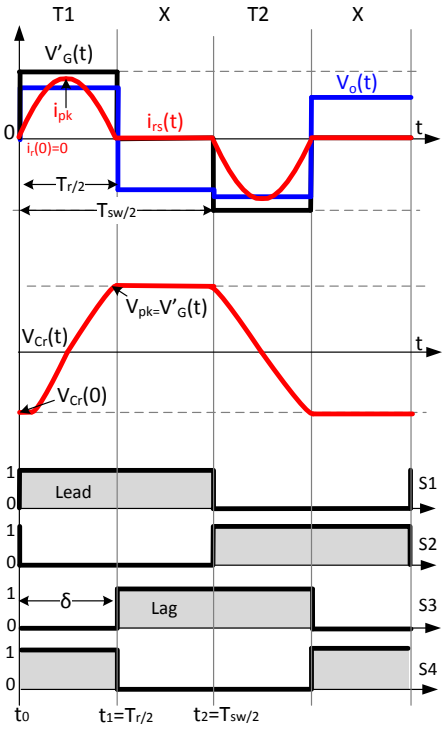

Fig. 4.15: DCM1 characteristic waveforms: top - inverter voltage reflected on rectifier side V_g', rectifier voltage V_o, resonant secondary current i_{rs}; middle - resonant capacitor voltage V_{Cr}; bottom - corresponding switching pattern. [99]

sub-interval a half resonant cycle (of duration $T_r/2$) is allowed to pass. T1 sub-interval finishes when S4 is blocked and S3 starts conducting. By this time, the resonant current has reached zero while capacitor voltage stabilizes at $+V_g'$ (considering the initial condition for $V_{Cr}(t_0) = -V_g' + 2\Delta V$ and $t = \pi$, see Fig. 4.16). Following equations are expressions for resonant current and voltage in DCM1 T1 sub-interval:

$$i_{rs}(t) = \frac{V_g' - V_o - V_{Cr}(t_0)}{Z_c} \sin \omega_r t \tag{4.16}$$

$$V_{Cr}(t) = (V_g' - V_o) - (V_g' - V_o - V_{Cr}(t_0)) \cos \omega_r t \tag{4.17}$$

As seen in Fig. 4.16, during transient state, capacitor voltage is increasing every switching interval with $2 \cdot \Delta V$ from 0 to $+V_g'$. As soon as $V_{Cr} \geq V_g'$, transition to DCM2 occurs.

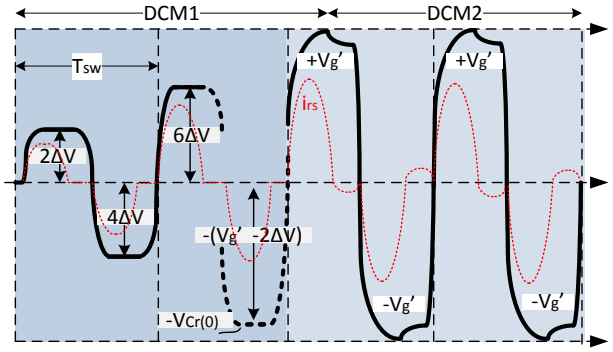

Fig. 4.16: Transition of capacitor voltge V_{Cr} from DCM1 to DCM2. [99]

DCM1: Sub-interval X

$t_1 \leq t \leq t_2$ X sub-interval begins when S1 and S3 are turned-on, while S2 and S4 are blocked. This means ${V_g}'$ is clamped to zero, inductor current remains at zero and all rectifier diodes are reversed biased. The equivalent circuit of this sub-interval can be seen as an open circuit resonant tank. In this time, V_o drops to V_{Cr} level. One half cycle is finished as soon as S1 is blocked, while S2 and S3 conduct. Following sub-intervals T2 and X are analysed with similar procedure.

$$i_{rs}(t) = 0 \tag{4.18}$$

$$V_{Cr}(t) = V_g' \tag{4.19}$$

Power flow

To evaluate how much power is delivered during DCM1, the average area of current waveforms i_{rs} during T1 and X sub-interval has to be calculated, following the steps from eq. (5.1) to eq. (5.1):

$$i_{out} = \langle i_{rs}(t) \rangle_{Tsw} = \frac{2}{T_{sw}} \int_{t_0}^{t_2} i_{rs}(t)dt \quad (4.20)$$

$$i_{out} = 2 \cdot F_{sw} \cdot q_s \quad (4.21)$$

$$q_s = 2 \cdot C_r \cdot V_{Cr} \quad (4.22)$$

$$i_{out} = 4 \cdot F_{sw} \cdot C_r \cdot V_{Cr} \quad (4.23)$$

$$P_{out} = V_{out} \cdot i_{out} \quad (4.24)$$

$$V_{Cr} = V_g{}' = V_{in} \cdot N \quad (4.25)$$

$$P_{out} = 4 \cdot F_{sw} \cdot N \cdot C_r \cdot V_{in} \cdot V_{out} \quad (4.26)$$

Comparing eq. (5.1) to eq. (4.6), they differ by a factor of 2. The main reason is that capacitor voltage on the "classic" SRC (with LC tank on inverter side) stabilizes at $2 \cdot V_g$. For the classic SRC, there are no Q1 or Q2 sub-intervals (no pulse removal), but only D1 or D2 sub-intervals. The transition from T1 to D1 will occur, only if $V_{Cr} \geq (V_g + V_o')$.

DCM2

With respect to Fig. 4.17, principle waveforms for DCM2 are shown. As the name implies two half resonant cycles will appear during a half switching period. This conduction mode can only appear in the interval [0 to $F_r/2$] and if $\Delta V > 0$. Being very similar to DCM1, DCM2 is a sequence of following sub-intervals: T1-Q1-X-T2-Q2-X, with Q1 and Q2 equivalent sub-circuits shown in Fig. 4.13(c) and (g). Due to half cycle symmetry only the first three sub-intervals will be analysed, as the other three are similar but with opposite voltage and current signs.

DCM2: Sub-interval T1

$t_0 \leq t \leq t_1$ As S4 is already conducting, S1 switch is turned on and a full resonant cycle is delivered to the load, while D5 and D8 are forward biased. During this interval, as the resonant current i_{rs} is increasing from 0, resonant capacitor voltage increases too from $-V_{Cr}$. At $t_1 = T_r/2$, T1 sub-interval is finished, having again a zero inductor current and maximum V_{Cr}. Resonant inductor current and capacitor voltage equations are similar to DCM1 mode.

DCM2: Sub-interval Q1

$t_1 \leq t \leq t_2$ During Q1 sub-interval, the inductor current resonates for another half cycle, until $t_2 = T_r$. During this period, S1 is still on, but S4 is blocked and S3 starts to conduct. Therefore, the negative current flows through D1 and T3 as seen in Fig. 4.13(c). On rectifier side, D6 and D7 are forward

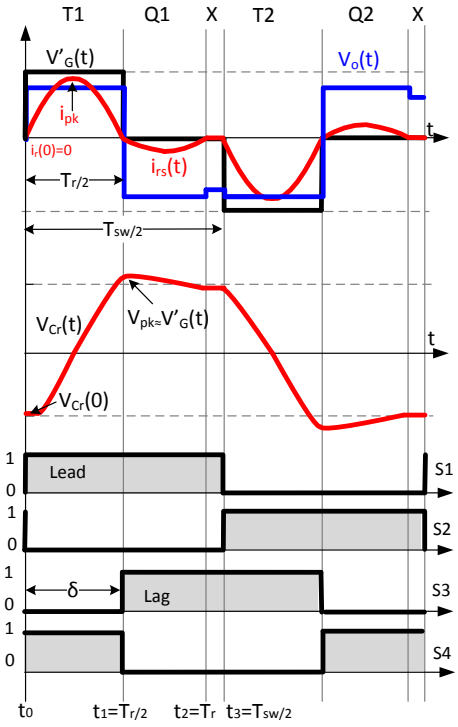

Fig. 4.17: DCM2 characteristic waveforms: top - inverter voltage reflected on rectifier side V_g', rectifier voltage V_o, resonant secondary current i_{rs}; middle - resonant capacitor voltage V_{Cr}; bottom - corresponding switching pattern. [99]

biased and due to this rectifer voltage V_o is negative. Capacitor voltage is slowly discharged, as $V_{Cr} > V_o$. Resonant current and capacitor voltage are given in Eq. (4.27) and (4.28). Eq. (4.29) shows where capacitor voltage will stabilize, when $t = t_2 = T_r$.

$$i_{rs}(t) = \frac{V_o - V_{Cr}(t_1)}{Z_c} \sin \omega_r (t - t_1) \tag{4.27}$$

$$V_{Cr}(t) = V_o - (V_o - V_{Cr}(t_1)) \cos \omega_r (t - t_1) \tag{4.28}$$

$$V_{Cr}(t) = V_o - (V_o - V_g')(+1) = V_o - \Delta V \tag{4.29}$$

DCM2: Sub-interval X

$t_2 \leq t \leq t_3$ When $V_{Cr} = V_o - \Delta V$, another X subinterval begins as resonant current is zero, while all rectifier diodes are reversed biased. At $t_3 = T_{sw}/2$, switch S1 is off and another half cycle begins. Similar to DCM1, in this sub-

interval, the resonant current is zero and capacitor voltage stays flat, meaning no power is delivered to V_{out}.

DCM1: Power flow and peak stress

Equation for power flow is exactly the same as in DCM1. As in DCM1 and also according to [103], the SRC# is operating similar to a frequency controlled current source in DCM2, implying a linear function between power and frequency. On the other hand, the slope of the function is slower as compared to DCM1, due to higher ΔV across the LC tank, In DCM2, $Vout$ is smaller then in DCM1. This means output power will also be less, but still proportional to the frequency. Looking at Fig. 6.1a, one notices the slope in DCM2 is proportional to ΔV and also impacts the resonant peak current (Fig. 6.1b).

Boundary condition

Transition from DCM1 to DCM2 is achieved when:

$$V_{Cr} > V_o \tag{4.30}$$

CCM1-Hybrid

CCM1-hybrid mode of conduction is described in Fig. 4.18. The name *hybrid* is used as very short X sub interval (characterized by zero resonant current) will appear. First of all, this mode can appear in the switching interval [$F_{r/2}$ to F_r] and if $\Delta V \approx 0$. It is composed of following subintervals:T1-X-Q1-T2-X-Q2. Similar to other modes of operation, only the first three sub-intervals will be analysed, as the other three are similar but with opposite voltage and current signs.

CCM1-Hybrid: Sub-interval T1

$t_0 \leq t \leq t_1$

During subinterval T1, resonant current i_{rs} will start at a low turn on current $i_r(t_0)$ and for a period equal to $\delta \cdot T_{sw}/2$ a resonant cycle is delivered to the load, as switches S1 and S4 conduct both. Capacitor voltage increases from a negative V_{C0} towards a positive value. Resonant current and capacitor voltage are determined as:

$$i_{rs} = \frac{V_g' - V_o - V_{Cr}(t_0)}{Z_c} \sin \omega_r t + i_{rs}(t_0) \cos \omega_r t \tag{4.31}$$

$$V_{Cr} = (V_g' - V_o) - (V_g' - V_o - V_{Cr}(t_0)) \cos \omega_r t + i_{rs}(t_0) Z_c \sin \omega_r t \tag{4.32}$$

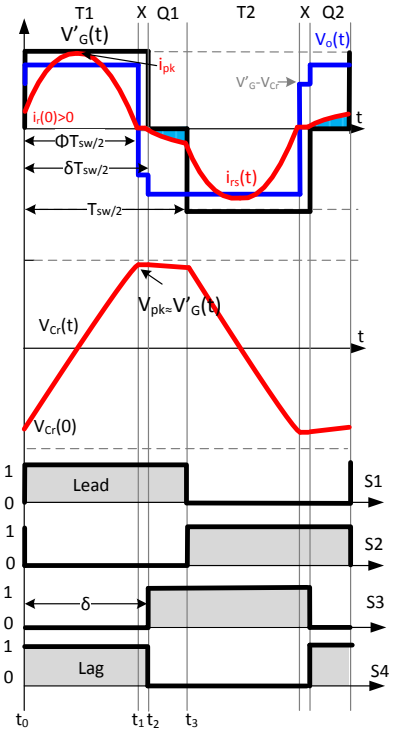

Fig. 4.18: CCM1-Hybrid characteristic waveforms: top - inverter voltage reflected on inverter side V'_g, rectifier voltage V_o, resonant secondary current i_{rs}; middle - resonant capacitor voltage V_{Cr}; bottom - corresponding switching pattern. [99]

The sub-interval ends at t_1, as for a very short period, V_{Cr} is equal to rectifier voltage V_o and no current is delivered to the load.

CCM1-Hybrid: Sub-interval X

$t_1 \leq t \leq t_2$

Next, a different kind of X subinterval appears, as V'_g is still applied. The reason for it is that $V_{Cr} \leq (V'_g + V_o)$. The length of T1 and X subintervals equals with $\delta \cdot T_{sw}/2$ which is the phase displacement between the inverter legs. The sub-interval ends at t_2, when switch S4 is blocked and switch S3 starts conducting.

$$i_{rs} = 0 \tag{4.33}$$

$$V_{Cr} = V_t \tag{4.34}$$

$$V_{out} = V'_g - V_{Cr} \tag{4.35}$$

CCM1-Hybrid: Sub-interval Q1

$t_2 \leq t \leq t_3$

Further on, as soon as phase displacement is implemented, a Q1 subinterval will begin and negative resonant current will start to flow. Here, V_g' is clamped to zero and tank voltage V_t equals V_o. From switching point of view, the inverter switches and rectifier diodes turn on at a low current and turn-off with ZCS. Resonant tank current and voltage are described in following equations.

$$i_{rs} = \frac{V_o - V_{Cr}(t_2)}{Z_c} \sin \omega_r(t - t_2) + i_{rs}(t_2) \cos \omega_r(t - t_2) \tag{4.36}$$

$$V_{Cr} = V_o - (V_o - V_{Cr}(t_2)) \cos \omega_r(t - t_2) + i_{rs}(t_2) Z_c \sin \omega_r(t - t_2) \tag{4.37}$$

Following T2, X and Q2 subintervals are complementary, but with opposite sign.

CCM1-Hybrid: Power flow

Compared to DCM1, the power to frequency relation in CCM1-hybrid is slightly non linear and described in Eq. 5.6. Derivation of power output equation is mentioned Appendix A.3 and it follows the procedure from [123].

$$M = \frac{V_o/N}{V_g} \tag{4.38}$$

$$\gamma = \frac{F_r \cdot \pi}{F_{sw}} \tag{4.39}$$

$$\Phi = 1 + \frac{2 \cdot atan(\frac{(V_g + \cos(\gamma) \cdot (2 \cdot V_o - V_g))}{(sin(\gamma) \cdot (2 \cdot V_o - V_g))})}{\gamma} \tag{4.40}$$

$$A = \frac{(1 - \cos(\Phi\gamma)) \cdot ((2M - 1) \cdot \cos(\gamma) + 1)}{\cos(\gamma) - \cos(\Phi\gamma)} \tag{4.41}$$

$$P_{out} = {V_g}^2 \cdot \omega_{sw} \cdot C_r \cdot \frac{1}{\pi} \cdot A \tag{4.42}$$

Boundary condition

Transition from CCM1-hybrid to CCM1 is achieved when:

$$V_{Cr} > V_g' + V_o \tag{4.43}$$

CCM1

Final mode of conduction is characterized by the waveforms from Fig. 4.19 and it is composed of following subintervals: T1-D1-Q1-T2-D2-Q2, with D1 and D2 equivalent circuits shown in Fig. 4.13(b) and (f). This mode appears only above $F_{r/2}$ and if $\Delta V >> 0$, showing a highly nonlinear relation between power and switching frequency and it should be avoided as it increases turn-on losses. Only first half cycle is analysed as the other half cycle is symmetric and complementary.

CCM1: Sub-interval T1

$t_0 \leq t \leq t_1$ Similar to CCM1-hybrid, T1 sub-interval starts at a current $i_{rs} > 0$, but with larger magnitude, impacting turn-on losses. Also in this sub-interval a resonant cycle is delivered to the load until $t = t_1$, when the resonant current reaches zero and capacitor voltage is reaching its peak value. Lower equations describes the two parameters.

$$i_{rs} = \frac{V_g' - V_o - V_{Cr}(t_0)}{Z_c} \sin \omega_r t + i_{rs}(t_0) \cos \omega_r t \tag{4.44}$$

$$V_{Cr} = (V_g' - V_o) - (V_g' - V_o - V_{Cr}(t_0)) \cos \omega_r t + i_{rs}(t0) Z_c \sin \omega_r t \tag{4.45}$$

CCM1: Sub-interval D1

$t_1 \leq t \leq t_2$

As a positive V_g' is still applied to transformer windings and $V_{Cr} > V_0$, a negative current flows through the resonant tank. This means on inverter side, diodes D1, D4 are conducting, while on rectifier side D6 and D7 are forward biased. The capacitor voltage is slowly discharing. Equations for resonant current and capacitor voltage are described as follows:

$$i_{rs} = \frac{V_g' + V_o - V_{Cr}(t_1)}{Z_c} \sin \omega_r (t - t_1) + i_{rs}(t_1) \cos \omega_r (t - t_1) \tag{4.46}$$

$$V_{Cr} = (V_g' + V_o) - (V_g' + V_o - V_{Cr}(t_1)) \cos \omega_r t + i_{rs}(t_1) Z_c \sin \omega_r (t - t_1) \tag{4.47}$$

Sub-interval D1 is ended at $t = t_2$, when switch S4 is turned off and S3 is turned on.

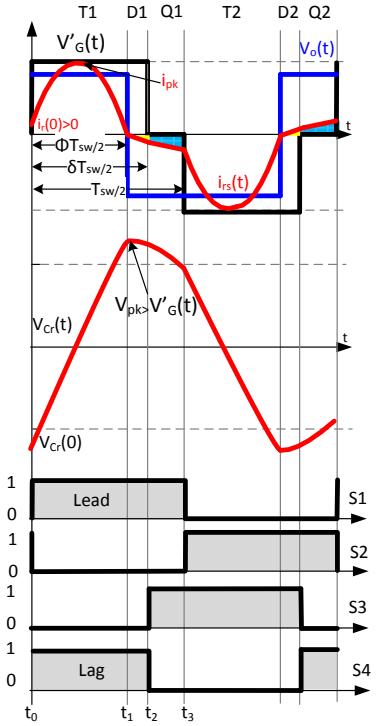

Fig. 4.19: CCM1 characteristic waveforms: top - inverter voltage reflected on inverter side V_g', rectifier voltage V_o, resonant secondary current i_{rs}; middle - resonant capacitor voltage V_{Cr}; bottom - corresponding switching pattern. [99]

Sub-interval Q1

$t_2 \leq t \leq t_3$ By turning off switch S4, applied inverter voltage V_g is clamped to zero. A negative current is still flowing, but through switch S3 and diode D1, while D6 and D7 are still forward biased. The capacitor voltage is still discharging. This sub-interval will end at $t = t_3$, when switch S1 is turned-off and S2 is turned-on. Equations for resonant current and capacitor voltage are given below:

$$i_{rs} = \frac{V_o - V_{Cr}(t_2)}{Z_c} \sin \omega_r (t - t_2) + i_{rs}(t_2) \cos \omega_r (t - t_2) \tag{4.48}$$

$$V_{Cr} = V_o - (V_o - V_{Cr}(t_2)) \cos \omega_r (t - t_2) + i_{rs}(t_2) Z_c \sin \omega_r (t - t_2) \tag{4.49}$$

CCM1: Power flow

Considering the power flow equation for CCM1 mode of operation, eg. (5.7) is derived. In CCM1, the relation between power and frequency is highly non-linear, making this mode of operation not favourable. Derivation of power output equation is mentioned in apendix A.4 and it follows the procedure from [123].

$$P_{out} = {V_g}^2 \cdot \omega_{sw} \cdot C_r \cdot M \cdot \frac{2}{\pi} \cdot B \tag{4.50}$$

$$B = [\frac{cos(\gamma) - 1 + 2M\cos(\gamma(1-\Phi))}{-\cos(\gamma(1-\Phi)) - cos(\gamma)}] \cdot \cos(\Phi\gamma) + M \cdot (\cos\Phi\gamma + 1) \tag{4.51}$$

$$\Phi = \frac{\delta}{2} + \frac{1}{\lambda} \cdot Q_s \cdot \sin M \tag{4.52}$$

4.3.6 Resonant tank stress

For proper component selection, the peak stress level has to be considered. The peak current level will occur in sub-interval T1 at $\pi/2$, while peak voltage at π. Considering Eq. (4.53) to (4.57), following parameters are defined: normalized output voltage M, converter quality factor Q_s, normalized switching frequency γ, constant K and load resistance R_{load}. The equations are valid for all modes of operation.

$$M = \frac{V_o/N}{V_g} \tag{4.53}$$

$$K = \frac{Q_s \cdot \gamma}{2} \tag{4.54}$$

$$Q_s = \frac{1}{\omega_r \cdot C_r \cdot R_{load}} \tag{4.55}$$

$$\gamma = \frac{F_r \cdot \pi}{F_{sw}} \tag{4.56}$$

$$R_{load} = \frac{V_{out}^2}{P_{out}} \tag{4.57}$$

Similar to [103] eq. (4.58) and (4.59) will predict the peak resonant tank voltage V_{pk} and current stress I_{pk} in all modes of operation.

$$I_{pk} = \omega_r \cdot C_r \cdot V_g \cdot (M(K+1) - 1) \tag{4.58}$$

$$V_{pk} = M \cdot K \cdot V_g \cdot N \tag{4.59}$$

4.4 Comparison of SRC vs. SRC#

This subchapter is based on the works from [124] and [125].

4.4.1 Ratings and characteristical waveforms

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The two variants of the series resonant converter with their operational principles and characteristic waveforms are illustrated in Fig. 4.20. The initial topology, the classic SRC operated in sub-resonant mode with variable frequency is in Fig. 4.20a, while the proposed topology SRC#, evolved from the SRC, is shown Fig. 4.20d. Both topologies are imagined for a 10MW turbine converter and their common ratings are presented in Table. 4.5, while the differences in ratings are shown in Table. 4.6. Comparing the conduction modes of SRC with SRC# between Fig. 4.20c and 4.20f, it's easy to see the addition of CCM1-hybrid for SRC#. Similar, comparing Fig. 4.20b with Fig. 4.20e, one of the main difference between the two topologies is the shape of the applied excitation voltage: for the SRC, V_g has a constant 50% duty cycle with variable period, while for the SRC#, the applied voltage pulse width is equal to one resonant cycle regardless of switching frequency, while the distance between the pulses is inverse proportional to the applied power.

Table 4.5: Common ratings for SRC and SRC#

Parameter	Value
Nominal power, P_n	10 MW
Nominal input voltage, V_{in}	$\pm$ 2kV
Nominal output voltage, V_{out}	$\pm$ 50kV
Insulation level	$\pm$ 75 kV
Inverter	4x3 in parallel IGBT(6500V-x-750A)
Rectifier	4x40 in series diode (6500V-x-750A)

Table 4.6: SRC and SRC# Comparison of ratings. I_{base} = 2500A, V_{base} = 4000V

Topology	Parameter	Value
Frequency range F_{sw}	200-1000 Hz	0-1000 Hz
Resonant capacitor C_r	78 uF	0.250 uF
Resonant inductor L_r	250 uH	78000 uH
Magnetizing inductance L_m	100 mH	10 mH
Transformer core weight Fe	880 kg	800 kg
Transformer winding weight Cu	2200 kg	340 kq
Resonant capacitor energy E_{cap}	10000 J	10000 J
Resonant inductor energy E_{ind}	10000 J	10000 J
Resonant tank voltage stress V_{pk}	2pu	25pu
Resonant tank current stress I_{pk}	2pu	0.2pu

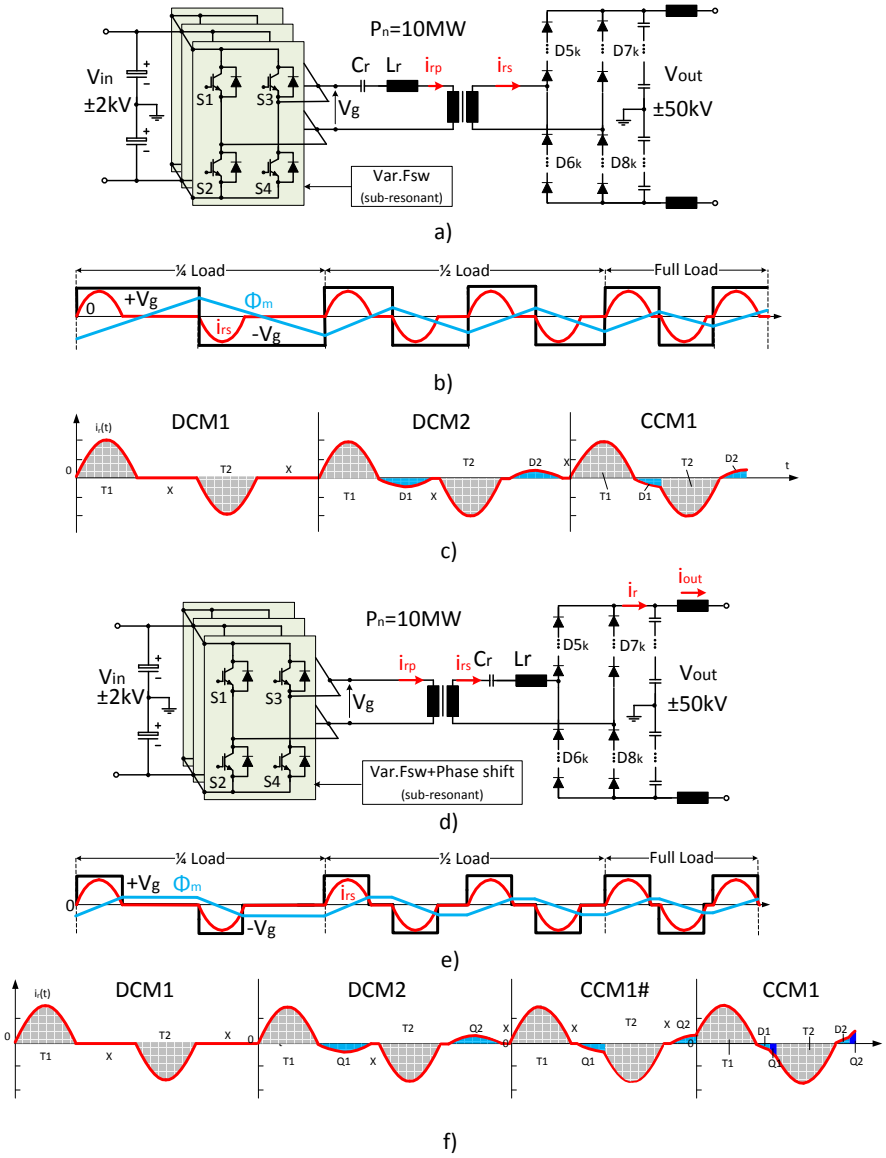


Fig. 4.20: SRC vs SRC# : a) classic SRC operated with variable frequency in sub-resonant mode and with LC tank on primary side; b) Example of variable frequency operation for SRC, with characteristical waveforms for inverter voltage V_g, secondary resonant current i_{rs} and transformer magnetix flux Φ_m; c) corresponding modes of operation of resonant current for SRC; d) SRC# with variable frequency and phase shift in sub-resonant mode and LC tank on secondary side; e)Example of variable frequency operation for SRC#, with characteristical waveforms for inverter voltage V_g, secondary resonant current i_{rs} and transformer magnetix flux Φ_m; f) corresponding modes of operation of resonant current for SRC#.

4.4.2 Transformer ratings

As also presented in [124], for the comparison of transformer ratings, a single phase transformer is suggested for both variants. Each transformer has a monolithic design, meaning only one primary and secondary winding as seen in Fig. 4.21a. A standard C-core structure, based on amorphous core material is preselected, for example [126]. Two design variants are proposed based on Table. 4.7 and shown in Fig. 4.21b. and c. As already seen, the major disadvantage of the SRC is that the transformer needs to be designed for the lowest operating frequency, which was selected to be 200 [Hz], impacting the transformer winding weight, increasing it almost 7x more then the SRC#. The other big disadvantage is that operation below 0.2 pu is not possible, limiting even more the ammount of annual energy production.

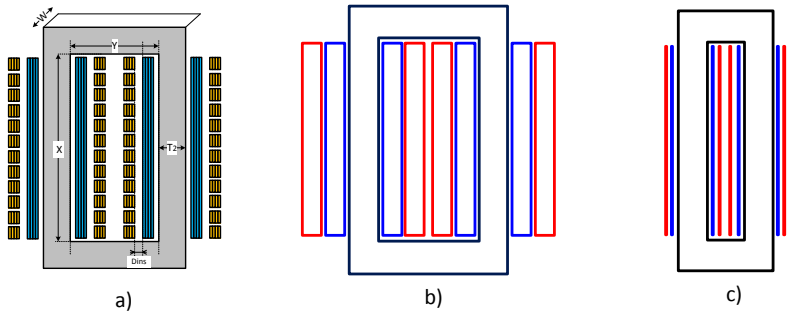


Fig. 4.21: Proposed transformer drawing a); SRC transformer b); SRC# transformer c).

Table 4.7: Transformer specifications for SRC and SRC#

Parameter	SRC	SRC#
N_p-Primary turns	92 (92 layers x 1 Turn),foil	20 (20 layers x 1 Turn), foil
N_s-Secondary turns	2300 (92 layers x 25 Turns),foil	500 (20 layers x 25 Turns), foil
B_{sat}-Saturation flux density	1.5 T	1.5 T
Foil thickness	0.001 m	0.001 m
Core material	Amorphous Metglas 2605SA1	Amorphous Metglas 2605SA1 [126]
Oil dielectric strength	10 kV/mm **midel**	10 kV/mm **midel**
Oil type	Ester based dielectric oil	Ester based dielectric oil
M_{Fe}-Core weight	880	$\approx$ 800 kg
M_{Cu}-Windings weight	2200	$\approx$ 380 kg
M_{Oil}-Oil weight	1200	$\approx$ 400 kg
X-Core window height	1 m	1 m
Y_D-Core window width	0.334	0.19 m
T_2-Core build	0.16 m	0.16 m
W-Core ribbon width	0.213	0.213 m
D_{ins} - primary to secondary distance	0.025 m	0.025 m
L_m - magnetizing inductance	125 mH	10 mH
Operational F_{sw}	200 - 1000 Hz	0 - 1000 Hz
Windings layout	1 primary + 1 secondary	1 primary + 1 secondary

4.4.3 Simulated efficiency

To compare the losses for SRC and SRC#, the semiconductor and transformer loss model detailed in the Appendices A.1 and A.2 were employed. Comparing Fig. 4.22a and Fig. 4.22b, it is noticed that the semiconductor losses are very similar between the SRC and SRC#. The major difference is in the transformer total losses, where the increased number of windings plays a major role. The increased winding losses exhibit higher losses due to the skin and proximity effects, which are increasing the windings ac resistance. In the case of the SRC, the winding losses are proportional to the output power, increasing up to 6% of nominal power at 1000 Hz. On the other hand, losses are kept below 1.5% for the whole operating range.

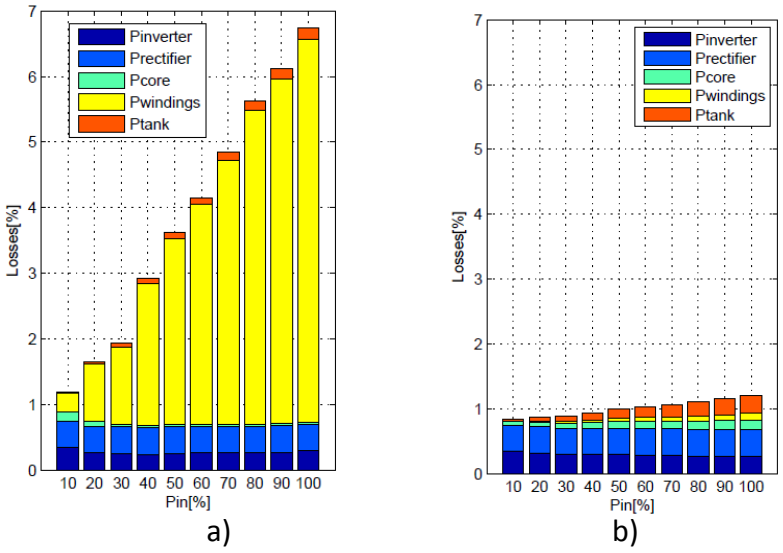


Fig. 4.22: a) SRC estimated losses; b) SRC# estimated losses

4.4.4 Operational range and resonant tank stress

In the first case of SRC, as the transformer was designed for 200Hz, meaning 0.2 pu operational frequency, the topology is not able to deliver power below this point, otherwise, the transformer will enter saturation mode. Assuming DCM mode of operation and the LC tank position on the primary side, both voltage and current peak levels will reach 2.0 pu, where the base values are referenced to the input side (V_{base} = 4000V, I_{base} = 2500A).

For the SRC#, the transformer will be designed for 1000 Hz, or 1.0pu, and due to pulse removal technique, the converter will be able to deliver power in full operational range. As the LC tank will be positioned on the rectifier side, the tank will experience the output network voltage, but the current stress will be minimized in proportion to the transformer turns ratio.

4.5 Conclusions

A variant of the single phase series resonant converter with LC tank located on the secondary side is proposed as a good candidate for the high power dc/dc converter. As the DC turbine converter does not require bidirectional power flow, the use of active switches on the $\pm 50kVdc$ side is removed. One monolithic rectifier with series connected diodes and one monolithic transformer configuration are proposed. The SRC# will excite the transformer primary winding with the so-called pulse removal technique. The modified pulse-pattern assumes variable frequency and phase-shift commutation on inverter side, allowing regulation of power from nominal level to zero. Two discontinuous and continuous mode have been identified, with DCM1 considered as the most favourable mode of operation, as it alows linear power to frequency operation. This attractive mode allows the control of LV side dc-link voltage control. Compared to a classic SRC operated in sub-resonant mode, the SRC# promises a flat efficiency of 98.5% in entire operational range and allows the design of the medium frequency transformer for the higher operating frequency, while on rectifier side, due to soft-switching and natural comutation, line frequency diodes are a feasible solution.

After basic analysis of the conduction modes and principle operation, a control architecture is proposed and discussed in following chapter.

Chapter 5

Controller structure for SRC#

Summary

Principle and control architecture are introduced for the SRC#. Two controller architectures are presented: the first one proposes a feedforward controller that acuratelly predicts for ideal models power to frequency relation, while a second architecture is based on a feedforward and gain scheduled PI controller, to compensate for the impact of non-idealities. Both controller have been investigated on a 10MW simulation model and experimentally validated on a 5000V, 10kW laboratory setup. The second architecture achieves low steady state error and good enough dynamics during power ramps and voltage steps.

5.1 Principle of control

5.1.1 AC wind turbine vs. DC wind turbine

There are fast and slow control dynamics involved in the control of a wind turbine, as the main goal is to maximize the power production based on the available wind power. The DC/DC converter will be the main buffer between the generator converter and the grid. For a state of the art-full-scale back to back converter, the main objective of the generator-side converter is to extract the maximum power from the wind, while the control of the grid side converter is mainly to keep the DC-link voltage constant [127]. Looking at Fig. 5.1a and b, the principle of control for grid side converters in an AC wind turbine and DC wind turbine are shown. The goal of the DC/DC converter will be to manage the LV side DC Link voltage, as it will experience transients due to the change of power produced by the generator. In other words, increase in produce power results in voltage overshoots, while its decrease results in voltage undershoot. These voltage variations due to power changes have to be compensated through charge and discharge of the DC link [127].

5.1.2 Functional requirements

Beside DC-link control, the DC/DC's controller needs to fulfill a set of functional requirements, as described in Table. 5.1.

5.2 Proposed controller structure

In the following paragraphs, open loop vs.closed loop operation for the SRC# are discussed. Two control architectures are presented and based on a feedforward controller obtained from power to frequency relation. Extensive

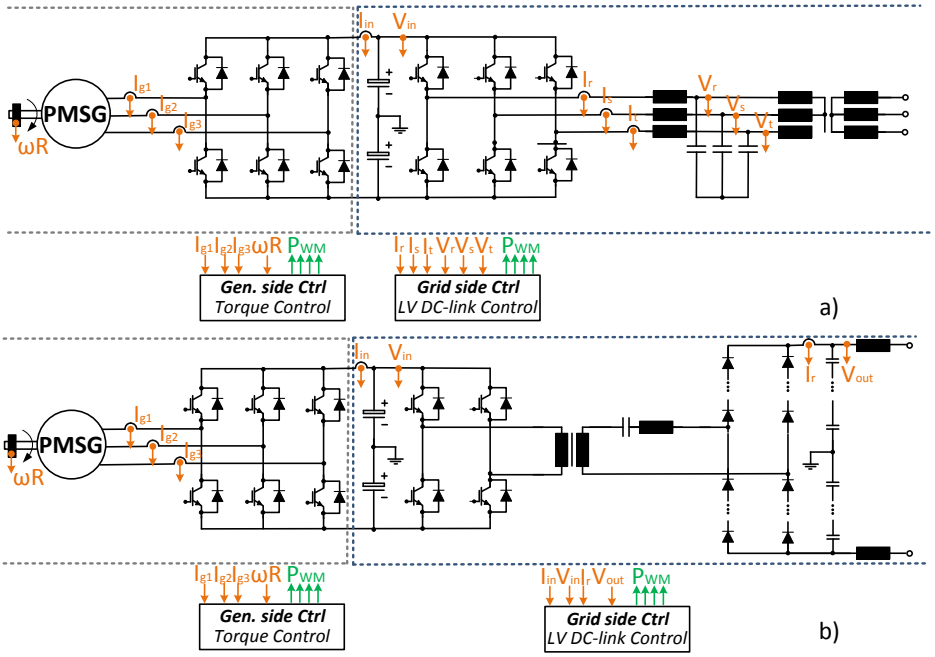


Fig. 5.1: Principle of control and sensor location : AC wind turbine a); DC wind turbine with SRC# b)

Table 5.1: Controller functional requirements

No	Function
1	Allow steady state generator across intended operating range
2	Ensure steady-state error in output power (current) is below specified value
3	Allow start-up from de-energized
4	Allow stop to de-energize
5	Allow large signal ramp-up/ramp-down of P_{ref} acc. to specified dP/dt value
6	Allow small-signal reference following of P_{ref} up to 3dB bandwith of XX Hz
7	Allow large-signal disturbance rejection (Change in V_{out}) acc. to spec. dV/dT and ΔV_{out} values
8	Allow small-signal disturbance rejection (Change in V_{out}) acc. to spec. of XX Hz
9	Allow automatic primary response (dP/dt) outside dead band
10	Allow fast run-back upon overvoltage
11	Allow detection of network fault (short circuit) by means of overcurrent & undervoltage detection
12	Allow protection by blocking & disconnecting upon relevant defects
13	Immunity to impressed harmonic in V_{out} (susceptibility)

work was performed in [128], [129] and the results obtained are further discussed.

5.2.1 Motivation for closed loop control

In [73] and [47], the SRC is proposed as an intermediate stage for a traction converter, with the main functionality of adapting two DC voltage levels. Operation in sub-resonant mode at constant frequency and open loop is proposed. The obvious question would be why not the same approach should be followed for a wind turbine application? One of the reasons is that any voltage disturbance on LV or MV side will impose a heavy CCM1 mode of operation, which translates to higher current and voltage stress. Further on, variations on MV side will be mirrored on LV side, thus increasing/decreasing the voltage level. This will impact the control of the active rectifier, which is using MPPT for maximum power extraction. Further on, even in steady state operation, it is expected that due to ohmic losses, the LV side DC-link will have variations. In the case of traction converters, the fron-end rectifier has the main goal of controlling the DC-link voltage, which is opposite for a wind turbine application.

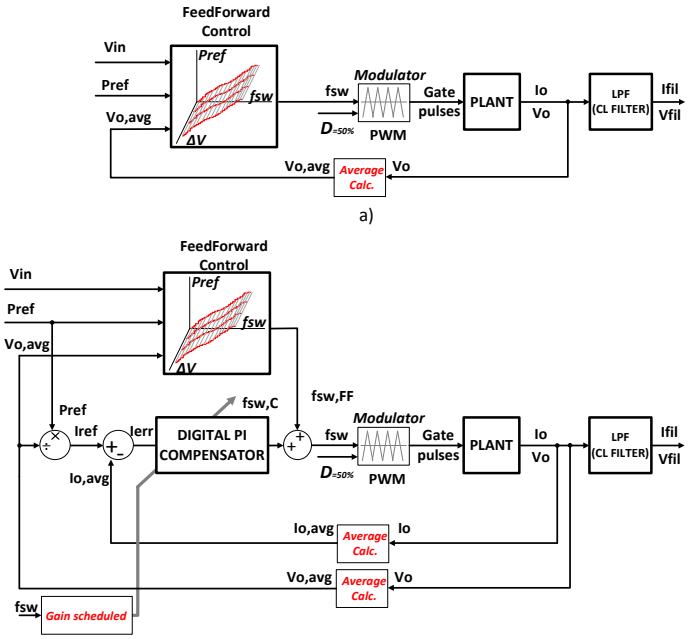


Fig. 5.2: Proposed controller architectures [128], [129]

5.2.2 Quasi-open loop operation and Feedforward controller

The first controller structure, based on quasi-open loop operation is illustrated in Fig. 5.2a and is implemented with a feedforward controller. As explained in Chapter IV, the SRC# will experience four different modes of operation, determined by the switching frequency and the voltage drop ΔV between input and output voltage levels. In each mode of operation, power is a function of number of pulses delivered to the MV grid. The feedforward controller emulates the power to frequency relation and it requires as input P_{ref}, measured V_{in} and V_{out}.

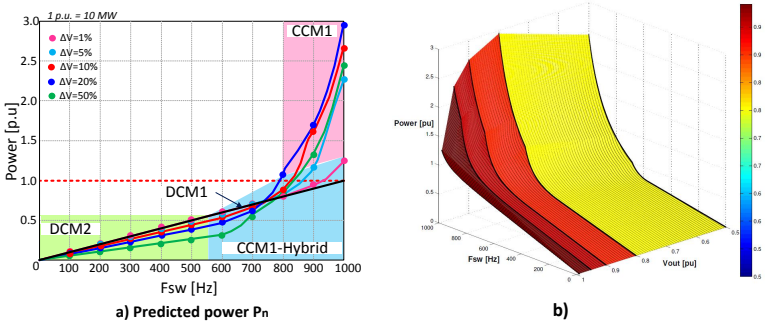


Fig. 5.3: Power to frequency relation a); 3d surface plot of power to frequency relation b).

Power to frequency relation

To properly implement the feedforward controller, the power to frequency relation in each mode of operation are identified and presented in Appendix A.3 and A.4.
Power flow in DCM1 and DCM 2:

$$P_{out} = 4 \cdot F_{sw} \cdot N \cdot C_r \cdot V_{in} \cdot V_{out} \tag{5.1}$$

Compared to DCM1, the power to frequency relation in CCM1-hybrid is slightly non linear and described in Eq. 5.6.

$$M = \frac{V_o/N}{V_g} \tag{5.2}$$

$$\gamma = \frac{F_r \cdot \pi}{F_{sw}} \tag{5.3}$$

$$\Phi = 1 + \frac{2 \cdot atan(\frac{(V_g + \cos(\gamma) \cdot (2 \cdot V_o - V_g))}{(sin(\gamma) \cdot (2 \cdot V_o - V_g))})}{\gamma} \tag{5.4}$$

$$A = \frac{(1 - \cos(\Phi\gamma)) \cdot ((2M - 1) \cdot \cos(\gamma) + 1)}{\cos(\gamma) - \cos(\Phi\gamma)} \tag{5.5}$$

$$P_{out} = {V_g}^2 \cdot \omega_{sw} \cdot C_r \cdot \frac{1}{\pi} \cdot A \tag{5.6}$$

Considering the power flow equation for CCM1 mode of operation, eg. (5.7) is derived. In CCM1, the relation between power and frequency is highly non-linear, making this mode of operation not favourable.

$$P_{out} = {V_g}^2 \cdot \omega_{sw} \cdot C_r \cdot M \cdot \frac{2}{\pi} \cdot B \tag{5.7}$$

$$B = [\frac{cos(\gamma) - 1 + 2M\cos(\gamma(1 - \Phi))}{-\cos(\gamma(1 - \Phi)) - cos(\gamma)}] \cdot \cos(\Phi\gamma) + M \cdot (\cos\Phi\gamma + 1) \tag{5.8}$$

$$\Phi = \frac{\delta}{2} + \frac{1}{\lambda} \cdot Q_s \cdot \sin M \tag{5.9}$$

The main goal of the feedforward controller is to apply the proper switching frequency to the modulator for power control. The operating point where P_{ref} is delivered to the grid is further defined by δV, which is the voltage difference between V_{in} and V_{out}. As mentioned previosuly, there's a linear characteristic between power and frequency, if operation in discontinuous mode is considered. On the other hand, voltage variations on input and output side could occur, impacting the power to frequency characteristic and giving it a non-linear shape.

Due to this fast, implementing an inverse function of the non-linear analytical equations during CCM1-hybrid and CCM1 is challenging. The method proposed in [128], [129], assumes linearization of the power curves obtained from the analytical equations. The power to frequency analytical curves are exposed in Fig. 5.3. A search algorithm is further described in [128] and employs a 2D look-up table, generated from the linearization of the non-linear power curves. In Fig. 5.3b, a 3D plot of the power curves with respect to switching frequency and the output voltage is depicted. The linearized map is composed by power curves at constant frequency and power curves at constant output voltage.

5.2.3 Closed loop operation with Feedforward controller

The previous control architecture based on the feedforward controller assumes operation with a lossless and ideal converter. Therefore, for a realistic approach, where non-idealities and ohmic losses are included, the feedforward controller should be modelled with analytic equations that incorporate

the previous. This is not a trivial task so to compensate for this, a gain scheduled PI controller is added in parallel and compensates for the error, as seen in Fig. 5.2b. The process of determining the SRC# transfer function and tuning of the PI are elaborated in [128] Experimental validation of both types of controllers is presented in Chapter 8.

5.3 Controller performance

To illustrate the steady state operation of the target converter, a PLECS simulation model was built and runned at different switching frequencies, in the range 0 to 1000 Hz, while voltage difference ΔV between input and output voltage was close to 0.1%, facilitating the operation in DCM1. The relevant experimental waveforms are further illustrated in Chapter 8.

Simulated results are shown in Fig. 5.4 and point out that output power is related to the applied switching frequency (cf. Fig. 5.4 a, b). As the converter operates in DCM1, peak resonant current and voltage are constant in the whole operating range. Fig. 5.4 b, c and d are zoomed in windows of the principle current and voltage waveforms (primary current i_{rp}, secondary current i_{rs}, inverter voltage V_g, capacitor voltage V_{Cr}, magnetizing current i_m) and they also demonstrate how pulse removal technique impacts the magnetizing current, keeping it constant, regardless of applied frequency. Another aspect worthy to mention is that at very low switching frequency $F_{sw} < 50$ Hz, the converter output current becomes discontinuous, as seen in Fig. 5.4a-(bottom). Looking at Fig. 5.5, ramp and step responses are shown. Fig. 5.6 illustrates a 10% step down in output voltage and the imediat impact on primary side current is seen. A jump from 1.8 pu to 5.0 pu is noticed, but the controller begins to decrease the switching frequency and the current decreases to $\approx$ 2.0pu. Further on, in Fig. 5.7 a 10% step in voltage implemented.

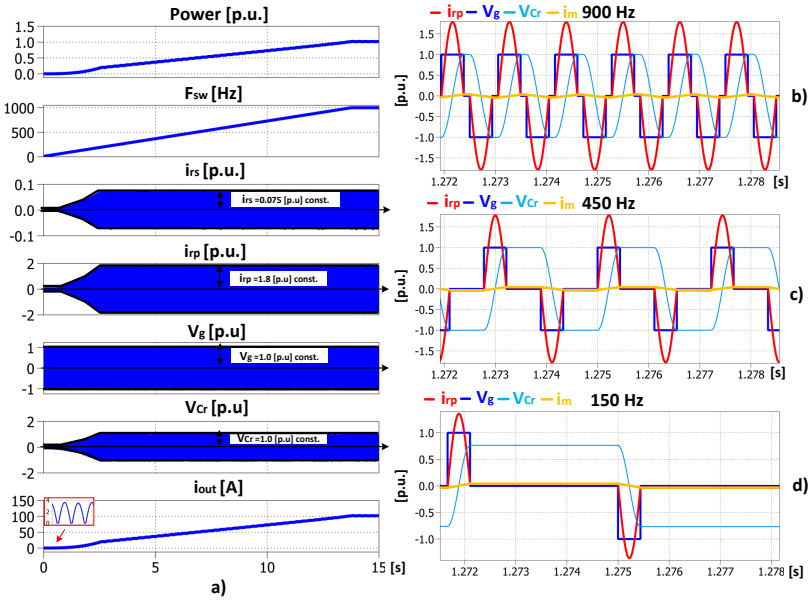


Fig. 5.4: Simulation results: steady state operation in DCM1 with steps in switching frequency (a); zoomed in windows of principle waveforms (primary resonant current i_{rp}, magnetizing current i_m, inverter voltage V_g and resonant capacitor voltage V_{cr} at 900 Hz (b), 450 Hz (c) and 150 Hz (d). [99]

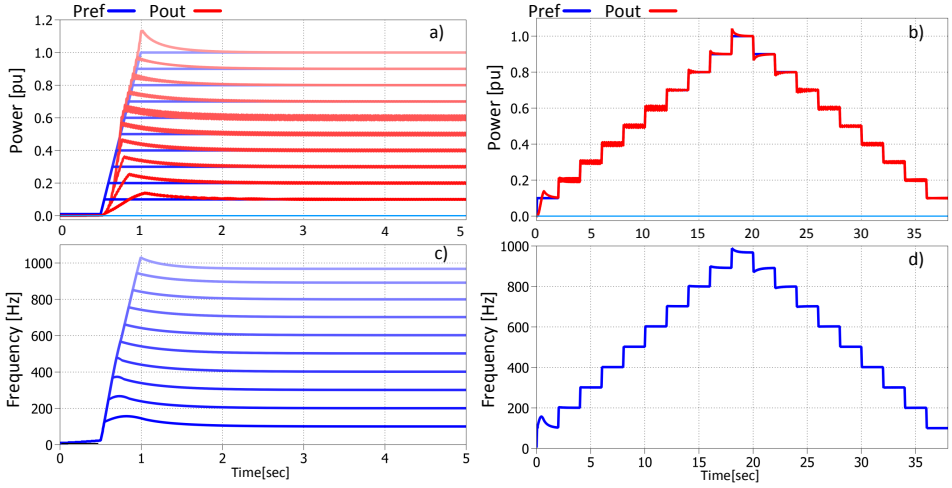


Fig. 5.5: Steady state operation: a)Ramps in reference power; b) Steps in reference power; c) Control frequency during ramps; d) Control frequency during steps.

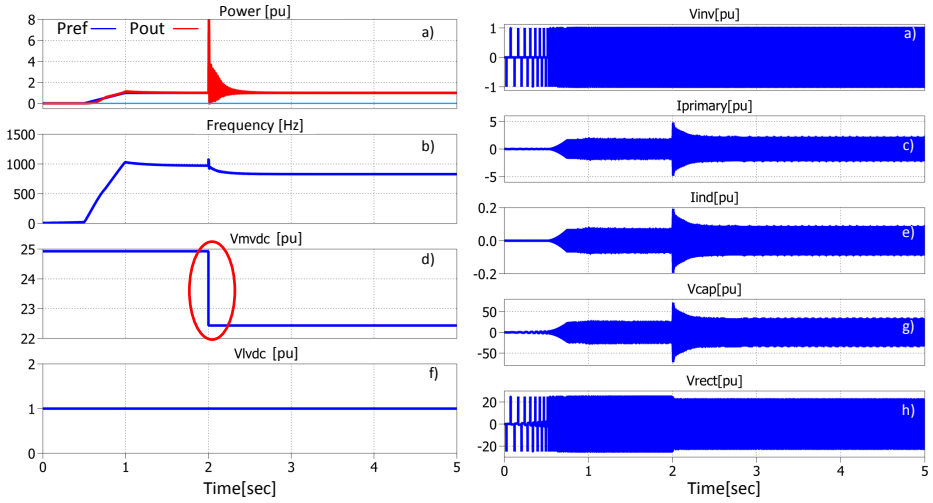


Fig. 5.6: Step down in output voltage: a) P_{out} vs. P_{ref}; b) F_{sw}; c) Output voltage; d) Input voltage; e) Inverter voltage; f) Primary side current; g) Resonant inductor current; h) Resonant capacitor voltage; i) Rectifier voltage

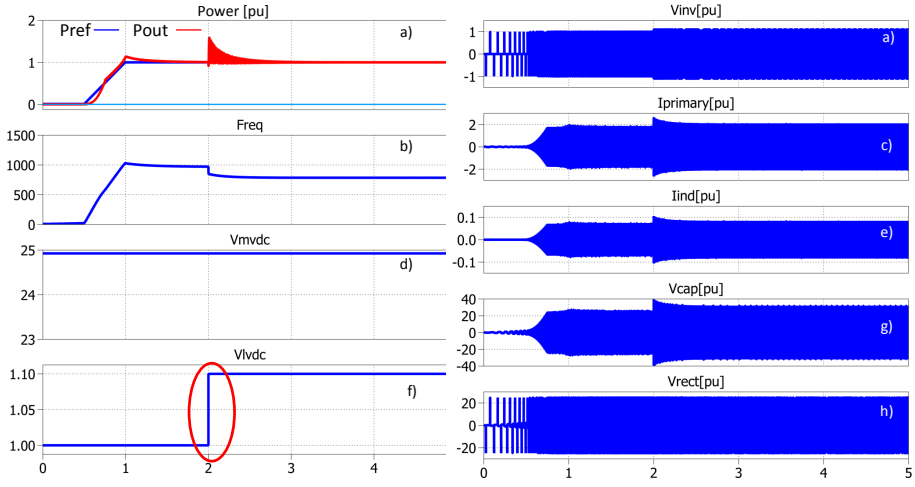


Fig. 5.7: Step up in input voltage: a) P_{out} vs. P_{ref}; b) F_{sw}; c) Output voltage; d) Input voltage; e) Inverter voltage; f) Primary side current; g) Resonant inductor current; h) Resonant capacitor voltage; i) Rectifier voltage

5.4 Conclusions

This chapter has discussed control aspects regarding the medium voltage, megawatt SRC#. Two controller architectures are identified: first approach assumes a feedforward controller that emulates the power to frequency relationship in 4 modes of operation (DCM1, DCM2, CCM1-Hybrid and CCM1), predicting accurately the necessary frequency for certain reference power. The second approach, proposes the addition of a gain scheduled PI controller that corects the deviations of the feedforward controller due to impact of non-idealities such as: ohmic losses, transformer stray capacitances and rectifier snubber circuits.

The impact of non-idealities on the circuit's characteristical waveforms and sensitivity studies are further illustrated in the following chapter.

Chapter 6

Sensitivity studies of SRC#

Summary

Peak resonant current and voltage stress variation to switching frequency are presented. LC tank, transformer and rectifier sensitivity to circuit parameters and specifications is performed. The choice of resonant capacitor and inductor has a direct impact on converter performance, selection of semiconductors and design of transformer. The impact of transformer magnetizing inductance on primary resonant current waveform and switching losses is investigated. The challenges in building a high voltage rectifier, with focus on diode voltage balancing, impact of snubber components and valve mechanical stray parameters are discussed and finally impact of non-idealities on the characteristic waveforms is shown.

6.1 Peak resonant current and voltage stress

The operation of SRC# in discontinuous conduction mode from 0 to maximum selected switching frequency, while the voltage difference between primary side reflected voltage and output voltage is ≈ 0, guarantees a linear function between switching frequency and power, a constant resonant capacitor peak voltage and resonant peak current. If input dc link voltage is considered constant and seen as an infinite power bus, voltage variation on output side will impact power to frequency function, presenting a non-linear characteristic. The reason is that the operation of SRC# cease to exist in DCM1 and transitions to CCM1-Hybrid or even CCM1.

As LC tank peak current and voltage will determine the specifications for semiconductors and resonant tank parameters, it is neccesary to establish which are the maximum accepted voltage drops on the output MVDC link and which are the maximum peak current and voltage stress. These parameters will serve as input variables for a design guide line. Evaluation of stress is determined through the analytical equations from previous Chapter IV. Fig. 6.1(a,b and c) shows the good agreement between analytical values and simulation results, within operation range of 0 to 1000 Hz and for different ΔV values (which is the voltage difference between reflected primary side voltage and rectifier voltage). Looking at Fig. 6.1a, a power to frequency characteristic in DCM1 is shown on the black line, with a linear characteristic.

As soon as a ΔV is increased, the $P(F_{sw})$ characteristic displays increasing nonlinearity above $F_{sw}/2$. In Fig. 6.1(b and c), if operation in DCM1 is considered, the peak current and voltage are the same in entire operational range. Increasing ΔV (meaning a larger output voltage difference between input and output voltage levels, compared to nominal specifications), will impact both peak current and voltage. It is observed in Fig. 6.1e, the resonant current's peak value is proportionaly increased with ΔV while the converter operates

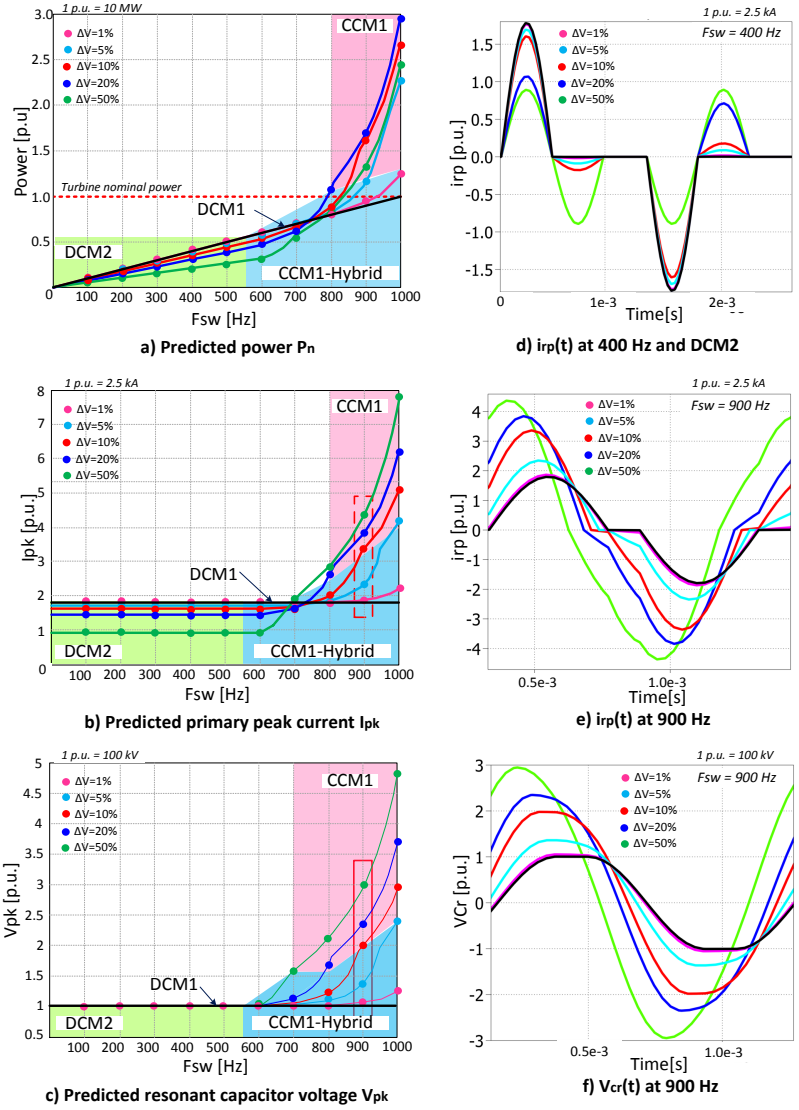
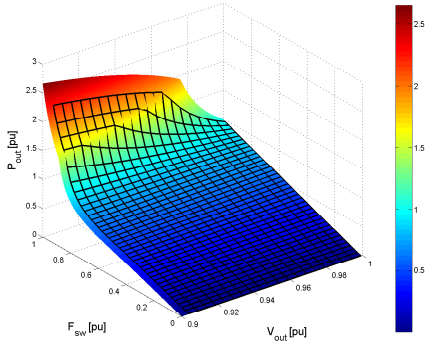
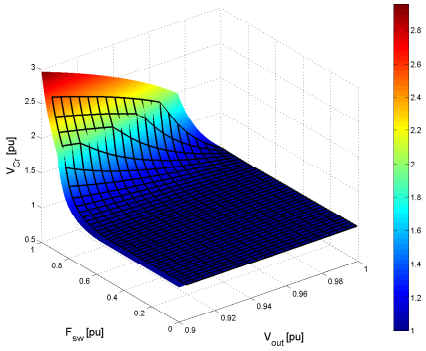


Fig. 6.1: Impact of ΔV (voltage difference between $V_g{}'$ and V_o) on: output power P_n (a); primary resonant current peak I_{pk} (b); resonant capacitor voltage peak V_{pk} (c); primary resonant current i_{rp} in DCM2 (e); primary resonant current i_{rp} at 900 Hz (f); resonant capacitor voltage waveform V_{cr} (g). [99]



(a)



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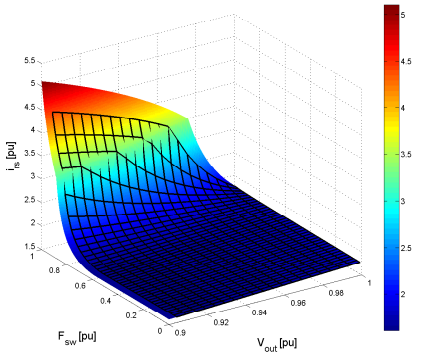


(c)

Fig. 6.2: 3D surfaces of : a) Power to frequency and output voltage characteristic; b) Resonant capacitor voltage to frequency and output voltage characteristic; c) Resonant inductor current to frequency and output voltage characteristic.

at the same frequency of 900 Hz. For this case, the converter can operate close to DCM1, with ΔV = 5%. Fig. 6.1f concludes the fact that capacitor voltage is output power dependent. Assuming a ΔV of 10%, with relation to Fig. 6.1a, nominal power is now being delivered at $\approx$ 825 Hz, rather then at 1000 Hz. At the same frequency, it is noticed that peak current has increased from 1.8 pu. to 2.1 pu, while capacitor voltage from 1.0 pu. to 1.25 pu. This means, when designing the converter LC tank, one has to consider a variation of +25% above nominal voltage and current specifications, to allow a safe margin with a 10% output voltage variation. Another aspect necessary to mention is that the converter efficiency will decrease for a ΔV higher than 5%. The 3D plots equivalent to Fig. 6.1(a,b and c) are shown in Fig. **??** a,b and c.

6.2 LC tank sensitivity to specifications

Converter's nominal specifications will determine the selection of LC tank parameters, namely the resonant capacitance C_r and resonant inductor L_r. The tank values will also determine peak ratings, that determine the selection of inverter and rectifier side semiconductors. As the position of the tank is located on rectifier side, meaning exposure to high voltage potential, a high resonant capacitance value and resonant inductor value could lead to technical challenges in building the resonant tank.

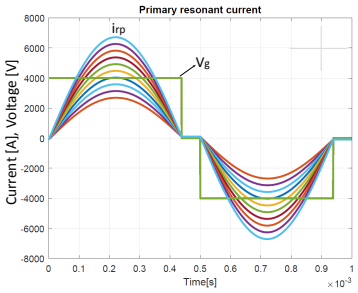


Fig. 6.3: Variation of primary peak current $i_{rp,pk}$ with nominal power level P_n

Variation of primary peak current $i_{rp,pk}$ to nominal power level P_n is presented in Fig. 6.3a. One could also say that a large characteristic impedance Z_c (present at the highest end of power and voltage specifications) will lead to a high peak current. This parameter is also crucial in determining the number of parallel modules on inverter side and selection heat sinks thermal impedance.

Looking at Fig. 6.5, variation of primary current i_{rp} and inverter voltage V_g with selected switching frequency, for the same power level, clearly shows

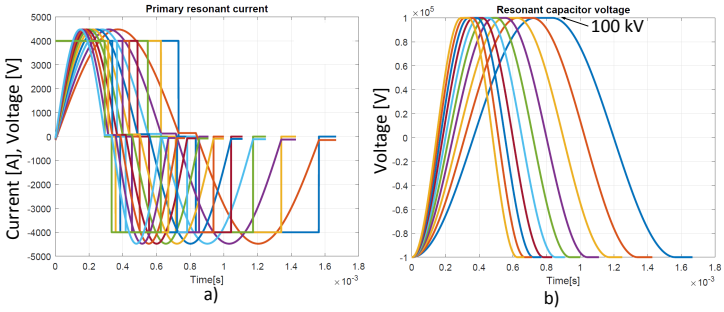


Fig. 6.4: a) Variation of primary current i_{rp} and inverter voltage V_g with switching frequency; b) Variation of resonant capacitor voltage V_{Cr} with switching frequency.C_r and L_r are recalculated for every step.

that in order to send the same power at low frequency, the pulse duration increases while the opposite occurs at higher frequency. The variation of resonant capacitor voltage V_{cr} with selected switching frequency is identified in Fig. 6.5b.

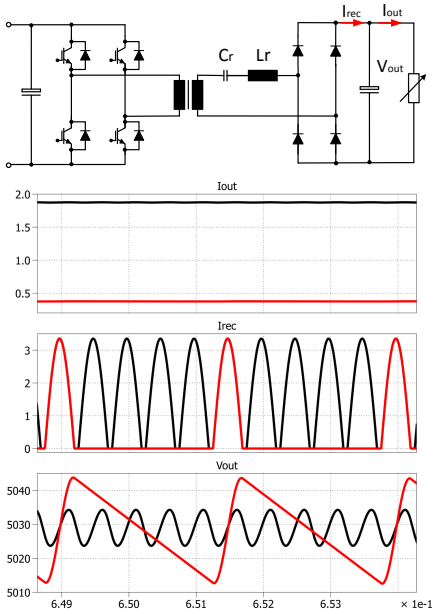


Fig. 6.5: Output capacitor voltage ripple, output filterd and rectified current for 1000 Hz and 100 Hz.

6.2.1 Output voltage ripple and current waveform

According to [130], operation with variable frequency in DCM mode will not be adversely affected by the wide range of switching frequency variation, as the low frequency operation coincides with the low output current, where less filtering is required. Therefore, the output capacitor value is determined by the maximum power point, which will occur at the highest frequency. Output capacitor voltage and rectified current waveform for two different frequencies are illustrated in Fig. 6.5.

6.2.2 Device waveforms

Igbts' and rectifier diodes' switching and conduction waveforms are presented in Fig. 6.6, while the switching characteristics per mode of operation are illustrated in Table.

Table 6.1: Device switching waveforms per mode of operation

Mode of operation	**Inverter**				**Rectifier**	
	Leading leg		Lagging leg			
	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off
DCM	ZVS	Low current	ZVS	Low current	ZVS	ZCS
CCM1-Hybrid	ZVS	Low current or ZCS	ZVS	Low current	ZVS	ZCS
CCM1	Hard SW	ZCS	ZVS	Low current	ZVS	ZCS

It is noticed that regardless of operating mode, the rectifier diodes have the same characteristics at turn-on and turn-off, meaning soft-switching is not sensitive to change in operating mode. For the IGBTs, CCM1 exibits hard switching at turn-on.

6.3 Transformer

6.3.1 Magnetizing inductance impact

One of the transformer's design drivers is high power density. This implies a small core geometry and copper volume (which is translated into low number of winding turns or a low magnetizing inductance). Looking at Fig. 6.7a and b the variation and impact of the magnetizing inductance L_m on primary resonant current i_{rp} indicates that for high L_m values, the total turn-off losses decrease considerably.

Understanding the relationship between the transformer's magnetizing inductance and turn off losses, helps the designer to impose a limit on L_m. In other words, if converter specifications are known, the maximum accepted ratio of magnetizing current to peak primary current determines the converter's figure of merit. With respect to Fig. 6.8, if the ratio i_m to i_{rp} is

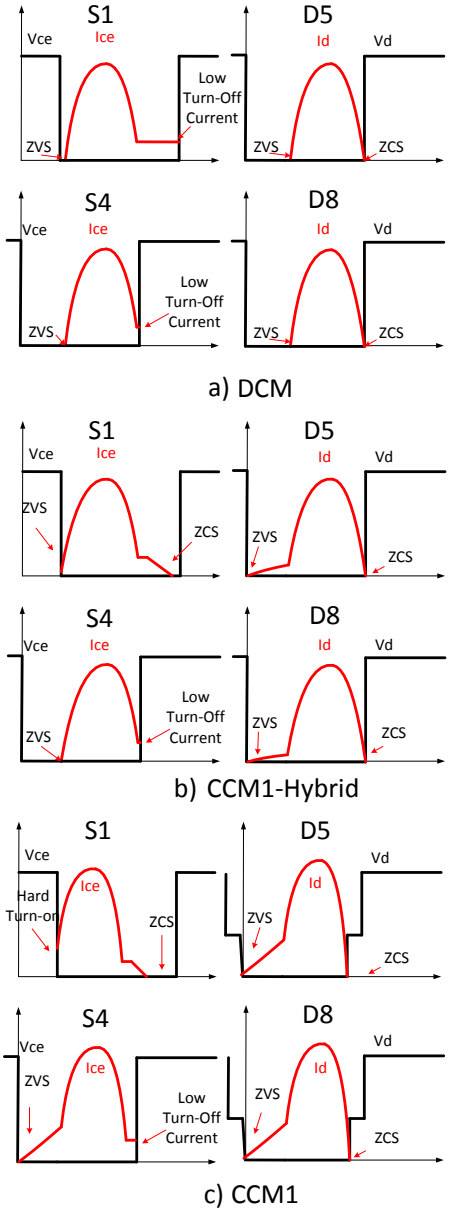


Fig. 6.6: IGBTs and rectifier diodes switching and conduction waveforms for different modes of operation: a) DCM; b) CCM1-Hybrid; c) CCM1.

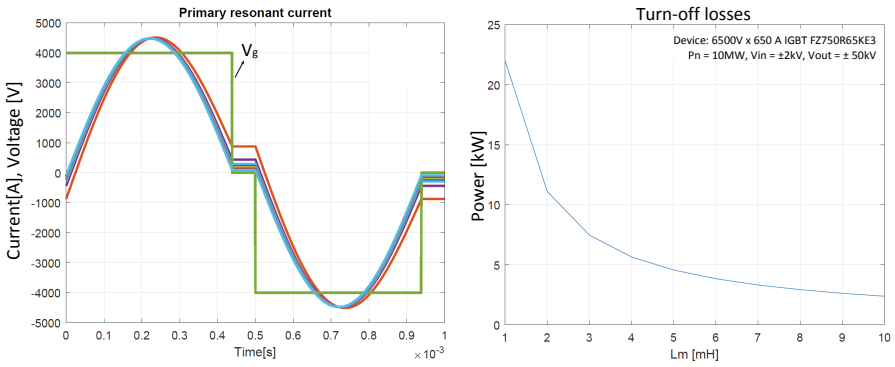


Fig. 6.7: a) Impact of L_m variation on primary resonant current i_{rp}; b) Impact of transformer magnetizing inductance on turn-off losses

selected to be 1%, L_m will have a variation from 15mH to aprox. 45mH, for a power range of 5 to 15MW. On the other hand, for 5% ratio, the range of variation will be 3mH to 10mH. Thus, the user pre-defined ratio or acceptable turn-off losses will also impact the transformer geometry.

Further on, as mentioned earlier, if the resonant inductor should be incorporated in the transformer's own leakage inductance, one notices from Fig. 6.8, that for 1% ratio of i_m to i_{rp}, the leakage inductance should not be higher then 0.55% of L_m. In practice, transformer's with 1 to 2% leakage inductance are considered to be very good designs, so one could say it would be challenging to incorporate the resonant inductor in the transformer and have low turn-off losses. But, if a ratio of 5% of i_m to i_{rp} is acceptable (meaning lower transformer volume and weight, but higher turn-off losses on the IGBTs), the leakage inductance should not be higher then $\approx 2.8\%$. Eq. for determining range of i_m and $L_{m,max}$ are shown in 6.2 and 6.2.

$$i_m = k_c \cdot i_{rp,pk},\ k_c \,\epsilon\, [1.0 - 5.0]\% \tag{6.1}$$

$$L_{m,max} = \frac{V_{in}}{4 \cdot k_c \cdot F_{sw} \cdot i_{rp,pk}} \tag{6.2}$$

6.3.2 Magnetizing current asymmetry

One important issue that needs to be addressed is the magnetizing current assymetry as seen in Fig. 6.9. The position of the LC tank on the rectifier side, implies that the inverter side current is susceptible to the non-ideal behavior of the semiconductor switches, meaning dc-voltage components can be applied to the transformer. This fact increases the risk of transformer saturation. Different methods have been proposed to alleviate this issue, one

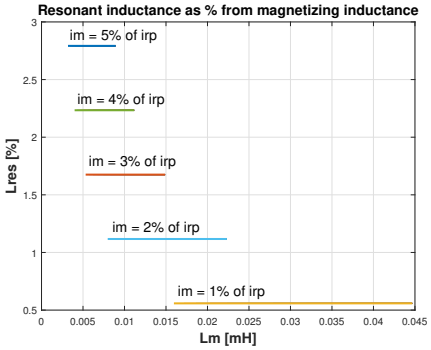


Fig. 6.8: Resonant inductance L_r as % from magnetizing inductance L_m. L_m is a function of nominal power P_n

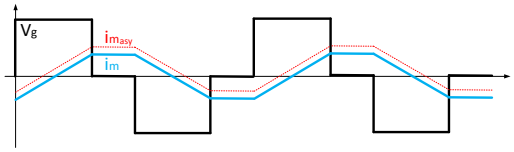


Fig. 6.9: Magnetizing current assymetry due to differences in IGBTs-R_{on}

of them being the "magnetic ear" proposed in [131], where a smaller size auxiliary core is attached to the transformer and shares the magnetic path. The particular transducer sense the flux through a non-invasive method and helps on balancing the transformer flux.

6.4 Rectifier

A methodology for characterization of medium voltage (MV), medium frequency (MF) rectifier valve was proposed in [132]. For a rectifier assembled with series connected diodes, static and dynamic voltage balancing are crucial and not just needed, and it is relevant to evaluate the sensitivity to the diode's parameter variation, snubber component tolerance, influence of temperature and the distributed stray capacitance of the mechanical system. The valve designer has to address this issues, before selecting the type of diode (fast or slow reverse recovery), type of cooling, valve orientation and to determine which parameter has the largest impact on sensitivity.

6.4.1 Fast vs. slow reverse recovery diodes

High voltage bipolar diodes are widely used in different converter applications, such as snubber diodes, blocking diodes or anti-parallel diodes. For applications requiring of 3.3 kV, 4.5 kV or 6.5 kV, the silicon bipolar diodes suffer from high switching losses at turn off due to the high reverse recovery current and recovery duration [132]. In a pwm converter with high di/dt, the diode losses will limit the operating (switching) frequency of the converter.

Looking at Fig. 6.10a, the current and voltage characteristic of the reverse recovery process for a soft-recovery diode are shown. As explained in [133], when turning from the conductive into the blocking state, the internal diode storage charge will be discharged, causing a current to flow in the opposite direction. The maximum possible peak reverse recovery current I_{RRM} is computed as acc. to eq. 6.3, while total charge Q_{rr} that flows from the diode to the outer circuit is calculated with eq. 6.4, by knowing the reverse recovery time t_{rr}

$$I_{RRM} \leq \sqrt{2 \cdot Q_{rr} \cdot -\frac{di_F}{dt}} \tag{6.3}$$

$$Q_{rr} = \frac{I_{RRM} \cdot t_{rr}}{2} \tag{6.4}$$

Reverse recovery and forward characteristic

Considering the forward voltage characteristics of a fast and slow diode from Fig. 6.10b and turn-off characteristics from Fig. 6.10c, it is proposed to employ slow recovery diodes at elevated frequency. This seems plausible as these devices are optimized for low conduction losses and low leakage current, while fast diodes are optimized for low reverse recovery, but suffer from increased conduction losses. With respect to Fig. 6.10d, reverse recovery for a 6.5kV slow diodes for soft and hard switching are presented. Further on, consider the soft-switching characteristics of the SRC# for rectifier diodes, meaning ZVS at turn-on and ZCS at turn-off, it is expected that for sinusoidal current waveform as in Fig. 6.10c, the diodes should experience a low reverse recovery.

6.4.2 Voltage balancing on series connected diodes

Voltage symmetry needs to be guaranteed in series connection of commutating semiconductors, mainly during (i) turn-on, (ii) turn-off and (iii) blocking state. The same applies for the rectifer diodes. Under quasi-static reverse voltage (blocking), the variation of leakage current (caused by manufacturing variation) may lead the devices with the lowest leakage current into avalanche

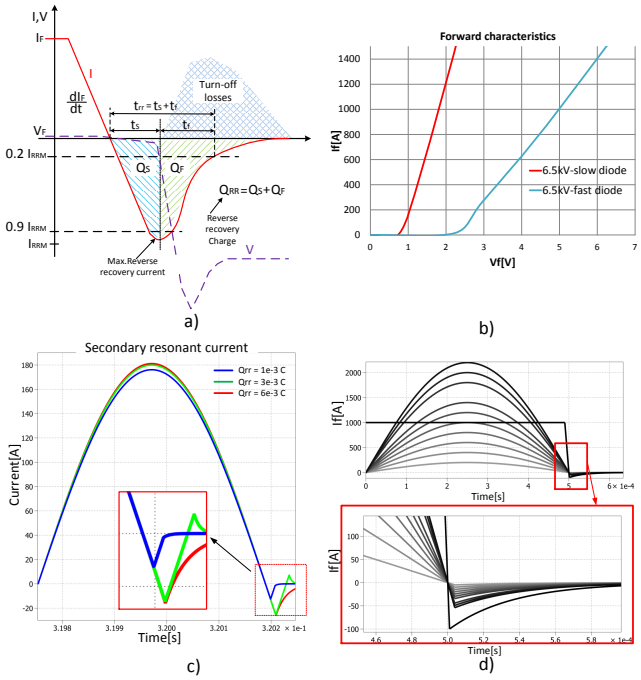


Fig. 6.10: a) Soft-diode turn-off reverse recover; b) Fast vs. slow reverse recovery press-pack diodes forward characteristic; c) Reverse recovery for different Q_{rr}; d) Slow diode reverse recovery for square and sinusoidal di/dt.

mode [133]. A common practice to ensure static and dynamic voltage balancing, is to connect parallel snubber and grading resistors, as shown in Fig. 6.11.

Static and dynamic imbalance

The example studied in [133], [134], a dispersion of only 10% in reverse current I_r is enough to provoke diode destruction for 600V diodes and 18% for 1.8 kV diodes. The divergence of reverse current is also temperature dependent. A balanced thermal management and selection of diodes from the same batch of manufacturers are proposed. But, in our application, it is considered that this asspect is not practical, and the most simple way of achieving static voltage sharing is through parallel grading resistors, despite added ohmic losses. In [132], it was shown that the largest impact on dynamic voltage distribution was given by variation in reverse recovery charge and temperature. A 5% variation in Q_{rr} caused a maximum overvoltage of 45%, while a difference of 10°K in temperature induced a 100% voltage difference. These issues

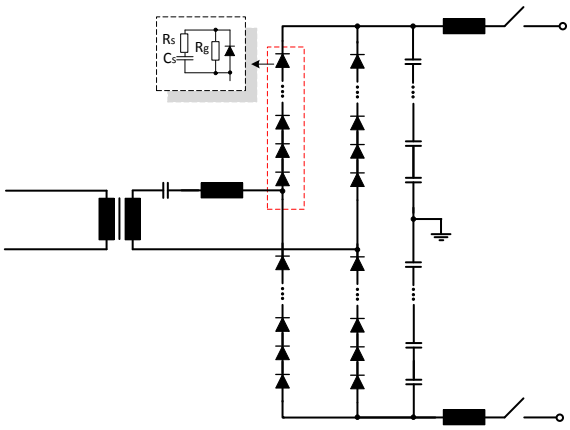


Fig. 6.11: MV rectifier with series connected diodes and RC parallel circuit for evenly shared static and dynamic voltages.

could be alleviated through the use of RC snubber circuits, where basically the parallel capacitor is added to the diode junction capacitance and through overdesign of diode voltage ratings up to 25% [134].

In Fig. 6.12a, b and c, the impact of diode reverse recovery charge Q_{rr} is evaluated. For instance, Fig. 6.12a shows that if one diode has 5% less charge than the other valve devices, it will block faster than all the other series conencted diodes and could experience nominal output voltage. By connecting a parallel 0.1nF capacitor to the same diode, the maximum voltage experience by the diode in blocking state drops to 0.7 pu, as seen in Fig. 6.12b. Further on, increasing the capacitor value to 1nF, diode blocking voltage drops now to 0.2pu, almost even with the other diodes. In correlation to Fig. 6.12g, one notices the correlation between one diode blocking voltage and snubber capacitor value.

Looking at Fig. 6.12d, e and f, the valve designer has to make a trade-off between maximum blocking voltage and impact on resonant current peak value. Low values of grading resistor combined with a parallel capacitor value, that is larger then the diode's own junction capacitance, the peak resonant current is clearly decreased as compared to the ideal case, as seen in Fig. 6.12d. Fig. 6.12h indicates the snubber impact on resonant current peak. Increasing the snubber capacitor value will decrease the peak of resonant current.

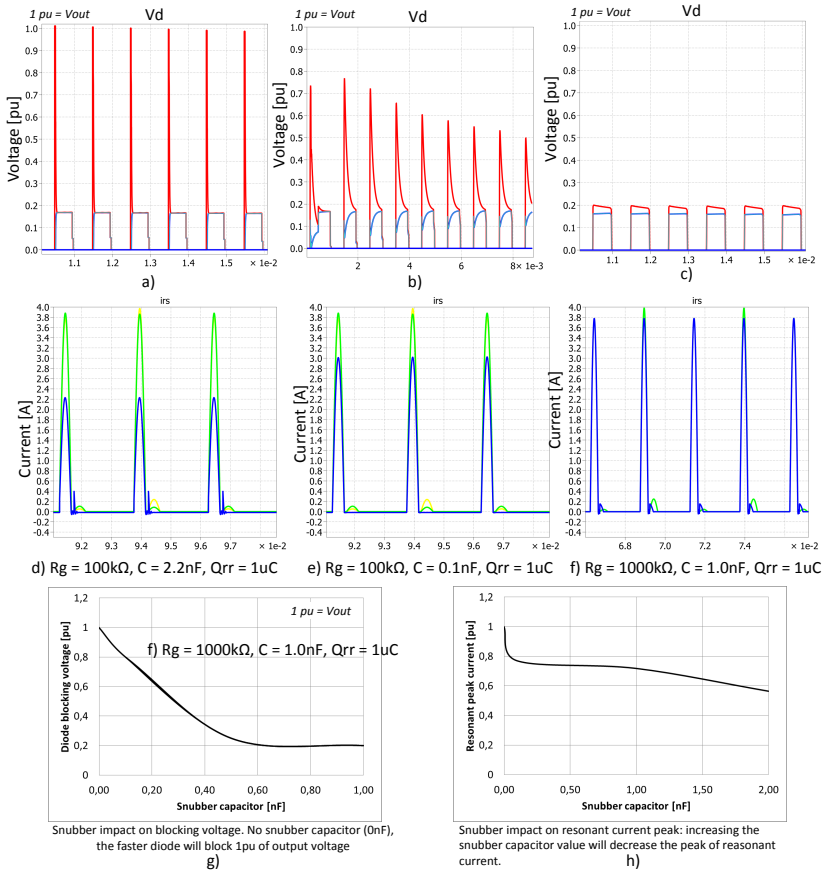


Fig. 6.12: Simulation observations on a valve composed of 12 series connected diodes (1600V,15A): a) 1 diode has 5% lower Qrr; b) 1 diode has 5% lower Qrr and a parallel 0.1nF capacitor; c) 1.nF capacitor connected in parallel to the faster diode; d) Comparison with ideal resonant current and Rg = 100$k\Omega$, C = 2.2nF; e) Rg = 100$k\Omega$, C = 0.1nF; f) Rg = 1000$k\Omega$, C = 1.0nF; g) Correlation between diode blocking voltage and snubber capacitor; h) Correlation between resonant peak current and snubber capacitor.

Experimental waveforms

The measured waveforms from Fig. 6.13 indicate how diode blocking voltage is impacted by the parallel RC circuit. In the experimental setup described in Chapter VIII, the snubber circuit (R = 50$k\Omega$, C = 1uF) was connected in parallel with each diode. One diode was experiencing 50% of nominal output voltage as seen in Fig. 6.13a, when the desired blocking voltage was supposed to be only 16%. With respect to Fig. 6.13b, by removing the series connected resistor and adding a parallel resistor (R = 250$k\Omega$), decreases the blocking

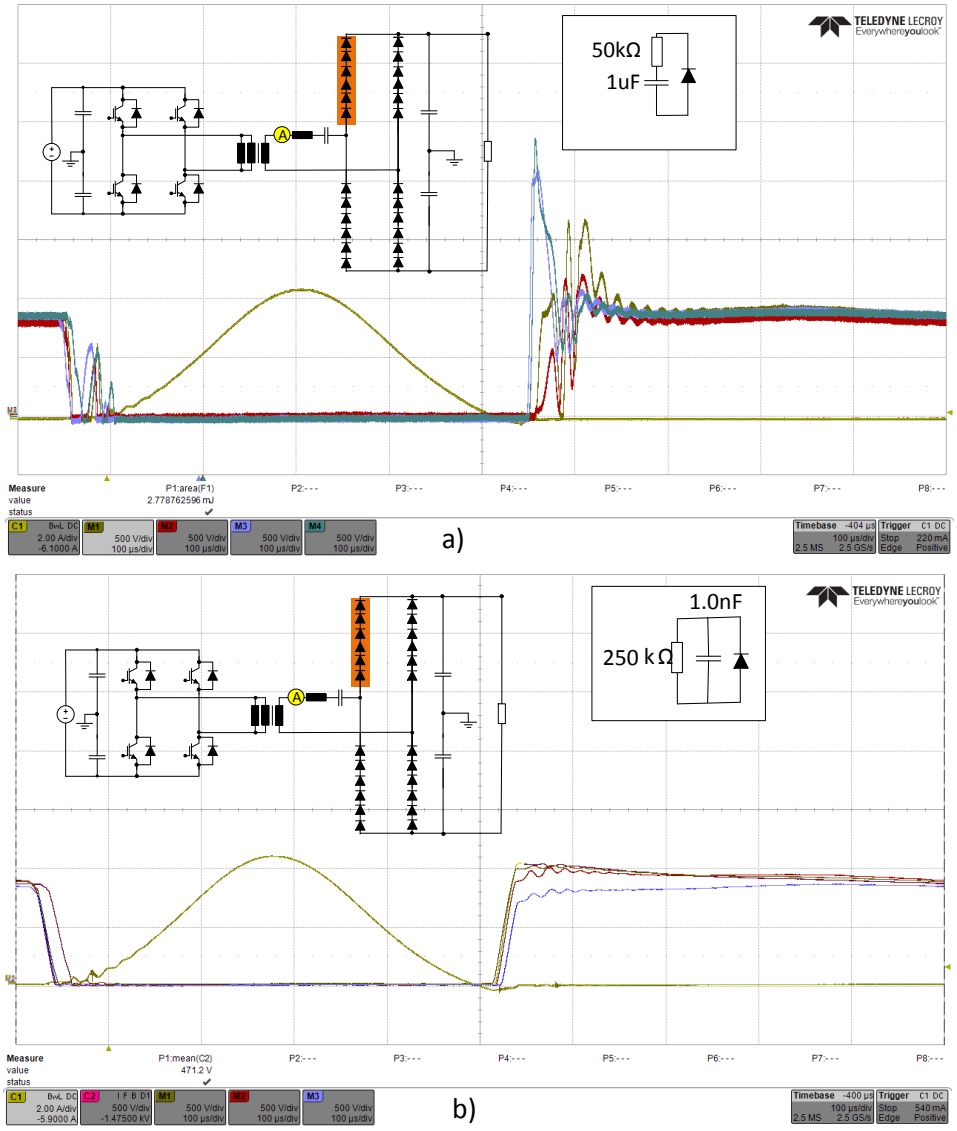


Fig. 6.13: a) Measured diodes blocking voltages, with snubber circuit connected in parallel: R = 50$k\Omega$, C = 1uF; b) Measured diodes blocking voltages, with parallel RC circuit: R = 250$k\Omega$, C = 1nF.

voltage per diode down to 16%. Observed oscillations at turn-off from Fig. 6.13a are generated by the interaction between the snubber capacitors and resonant inductance.

6.4.3 Valve mechanical structure and stray parameters

Valve structures

The development of valve technology has been significant since the first thyristor valve was commissioned in a converter station in 1967 [135]. Experience from previous thyristor valve designs could be followed in the development of the rectifier medium voltage valve. Different structures are exemplified in Fig. 6.14. The building block of the valve are the diodes (in press-pack package - Fig. 6.14a, b, c, d, or with power modules - Fig. 6.14e, f, g, h.)

The valve performance will be impacted by cooling technology, insulating medium and mechanical structure. Each diode will also require auxiliary equipment, like snubber circuits, grading resistors and heat sinks. The number of diodes is also relevant to reliability, cost and losses. The output voltage specification will impact the number of required diodes, and each valve has to withstand a certain overvoltage, calculated from the list of studies. The design of the voltage grading circuits should be as simple as possible [136]. Relevant work on high voltage valve designs, cooling techniques and power handling capabilities are discussed in [137], [138].

Valve equivalent circuit

Voltage sharing across the diodes is also impacted by the parasitic capacitances that exist between conductors, conductive framework, shielding, heatsinks and adjacent valve structures. Therefore, an electrostatic field analysis is neccesary to evaluate the stray capacitance parameters [139]. An equivalent diode valve circuit was established in [132] and presented in Fig. 6.15.

FEM investigation

In [132], a valve consisting of 10 diodes immersed in oil was modelled in FEM [140], as seen in Fig. 6.16c. In this particular analysis the stray capacitance between adjacent heatsinks C_{hh} and earth C_{he} are considered. The valve equivalent model of an arm is shown in Fig. 6.16b. During transient overvoltages, the diodes are blocked and can be modelled as a capacitor. The FEM and analytic values were then compared and used in the equivalent circuit. A standard impulse test ($1.2\mu s/50\mu s$) is modelled and applied to the valve circuit to evaluate voltage stress across the diodes. Fig. 6.16d shows device

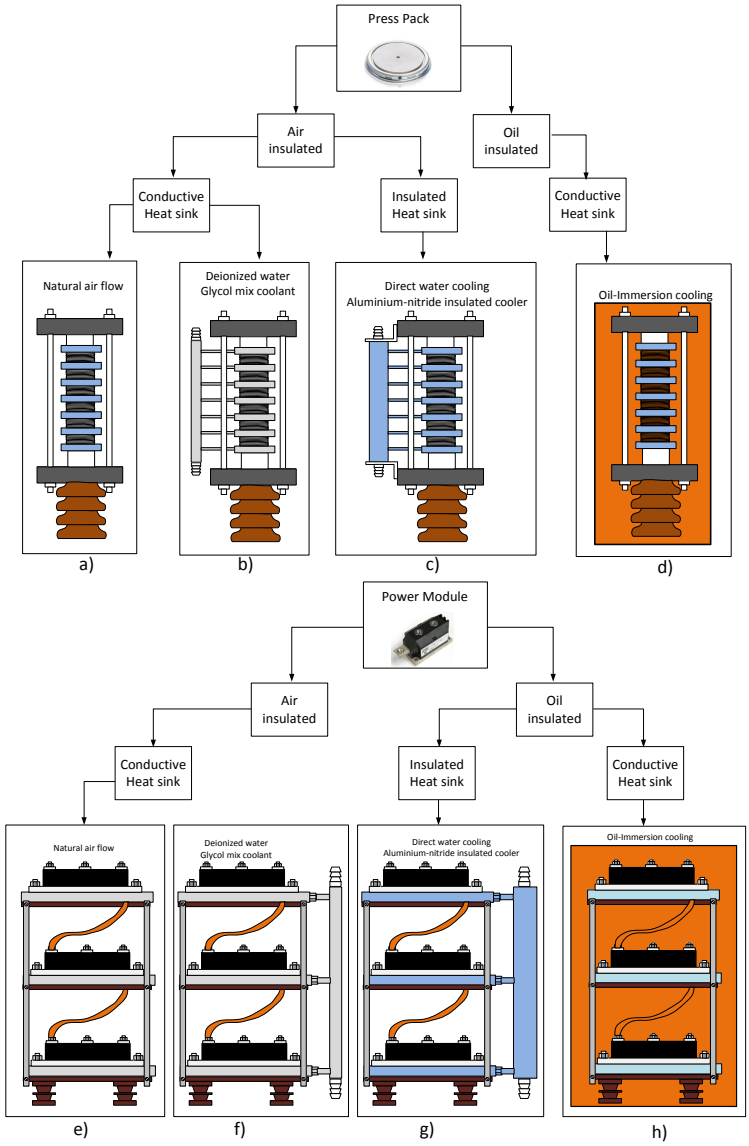


Fig. 6.14: Possible diode valve structures: a) Valve with press-pack diodes and natural air flow cooling; b) Valve with press-pack diodes and de-ionized water + glycol mix coolant; c) Valve with press-pack diodes and direct water cooling and aluminium nitride insulated cooler; d) Valve with press-pack diodes and oil immersion cooling; e) Valve with power module diodes and natural air flow cooling; f) Valve with power module diodes and deionized water+glycol mix coolant; g) Valve with power module diodes and aluminium-nitride insulated cooler; h) Valve with power module diodes and oil immersion;

stress for stray capacitance to earth in the range 10pF to 100pF. The observations indicate C_{he} has the largest impact from the stray circuit on device volage distribution, while C_{hh} has no impact.

6.5 Waveforms sensitivity to non-idealities

6.5.1 Transformer non-idealities

As exemplified in [40], [141], transformers with large turns ration amplify the effect of their nonidealities, meaning the leakage inductance and stray capacitance will affect the behaviour of the converter. Fig. 6.17 presents SRC# including the transformer equivalent circuits. To illustrate the effect of high leakage inductance and stray capacitance present in high voltage transformers, the waveforms from Fig. 6.18 are shown.

Transformer leakage inductance leads to voltage spikes, while stray capacitances lead to current spikes. The presence of non-idealities will lead in hard-switched converters to higher switching losses and reduced reliability, making this kind of topologies not suitable for high-frequency, high-voltage gains applications, without the presence of snubbers. On the other hand, resonant topologies are tolerant and well suited for high voltage DC applications, as the non-idealities are now part of the resonant LC tank. For resonant topologies, the effects of the windings stray capacitance can be overcome if the series stray capacitance is sufficiently larger then the reflected winding capacitance [40], while the leakage inductance is incorporated into the resonant inductor.

Minimize stray capacitance and maximize leakage inductance

According to [40], winding capacitances contribute substantial switching and snubber losses, as this capacitance needs to be charged or discharged every time the transformer voltage is changed. If the value of the capacitance is comparable to the one of the resonant capacitor present on the high voltage windings, an additional element is basically added to the tank circuit. Thus the expected ideal waveforms will deviate and an aditional subinterval is being added before each X sub-interval.

In [142] the development of a 100 kW and 30 kV insulated MFT is presented, with a few methods for minimizing the stray capacitance. The use of a low relative permittivity environment, such as ester oil is proposed.

The surface between primary and secondary coils needs to be decreased, by decreasing the winding diameter and winding height. Further on, the distance between primary and secondary coils has to be increased, also to minimize the potential of partial discharges.

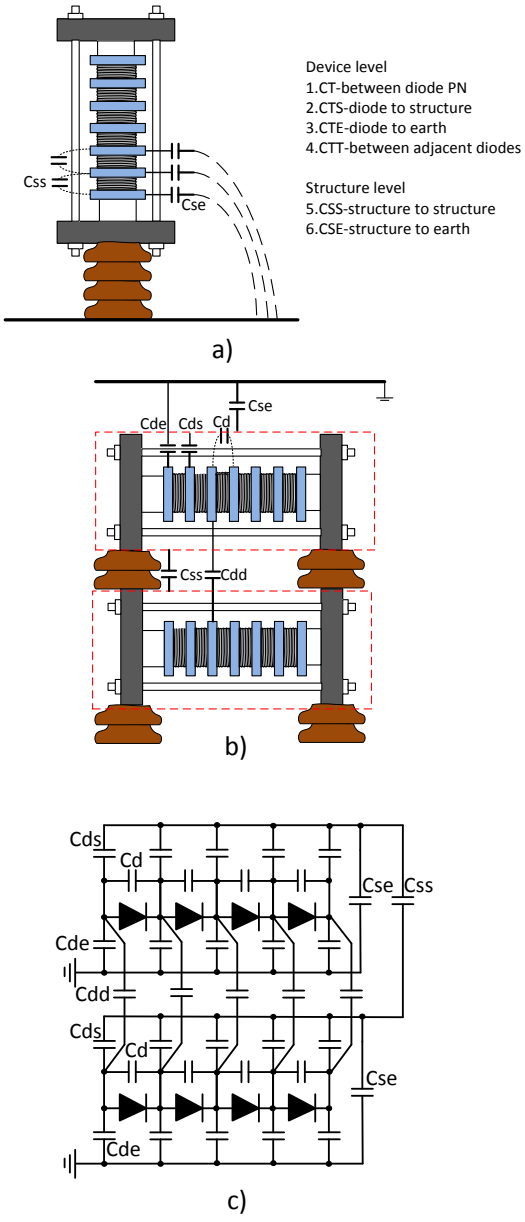


Fig. 6.15: a) One valve stray capacitance distribution; b) Stray capacitance distribution between two valves; c) Stray capacitance equivalent circuit between two valves of 4 diodes each. [132]

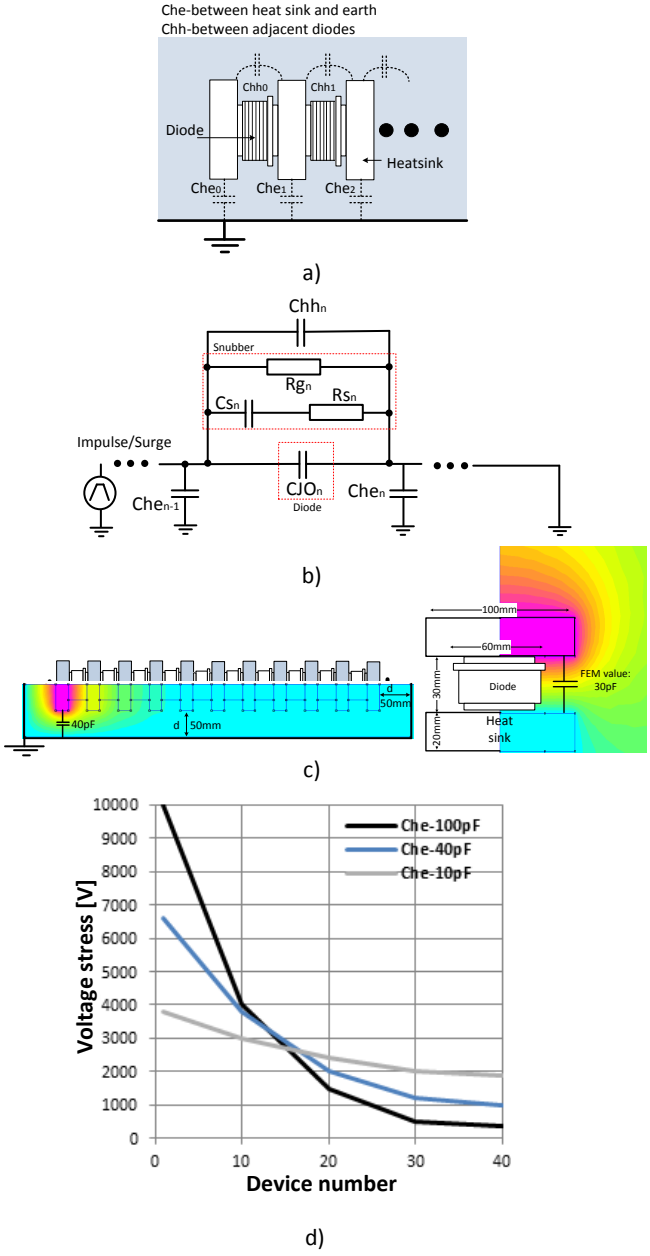


Fig. 6.16: Valve stray capacitance: a) Diode valve stray capacitance; b) valve section and equivalent circuit; c) FEM valve model; d) Voltage stress during impulse test. [132]

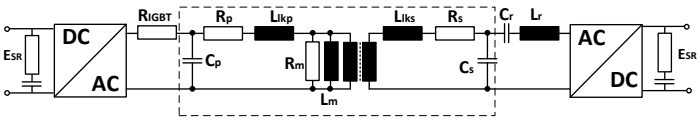


Fig. 6.17: SRC# Equivalent circuit

As the goal of the designer is to include as much as possible of the resonant inductor into the transformer, there are different methods proposed to increase the leakage inductance. Increasing the insulation distance between primary and secondary winding helps also on increasing the leakage inductance. In the end, a trafe-off between leakage and magnetizing inductance has to be addressed, as reducing the number of turns directly affects leakage inductance [134].

6.5.2 SRC# non-idealities

The impact on non-idealities on the primary resonant current of SRC# are illustrated in Fig. 6.19. To get a clear and simple picture of how each transformer, rectifier and RC circuit non-idealities are modifying the ideal shape, each non-ideality is added in step. In the ideal case (Fig. 6.19a), where $F_{sw} < F_r/2$, the shape of the current illustrates operation in DCM1, meaning the presence of T and X subintervals. The addition of transformer winding resistances (Fig. 6.19b), reduces the peak current in proportion to the value of the resistors. Larger winding resistances will require a larger input DC-link voltage and imply system losses.

Considering the winding leakage inductances L_{lkp} and L_{lks} in Fig. 6.19c would lead to a lower resonant frequency, as they are added in series to the resonant inductor. Therefore, L_r should be decreased, to allow L_{lkp}. The addition of magnetizing inductance L_m and core equivalent resistance R_m leads to a non-zero current during subintervals X.

In Fig. 6.19d, the rectifier diode reverse recovery charge Q_{rr} is added and reflected on primary side, while in Fig. 6.19e, the parallel RC circuit is further included. During the X subinterval, super-imposed on the DC component of the magnetizing current, oscillations generated by the diodes' parallel capacitances and the total resonant inductance are observed. The resonant frequency of the oscillations is shown in eq. 6.5 and given by L_r and C_{sn}, where C_{sn} is the parallel diode capacitor and N_{diodes} is the number of series connected diodes.

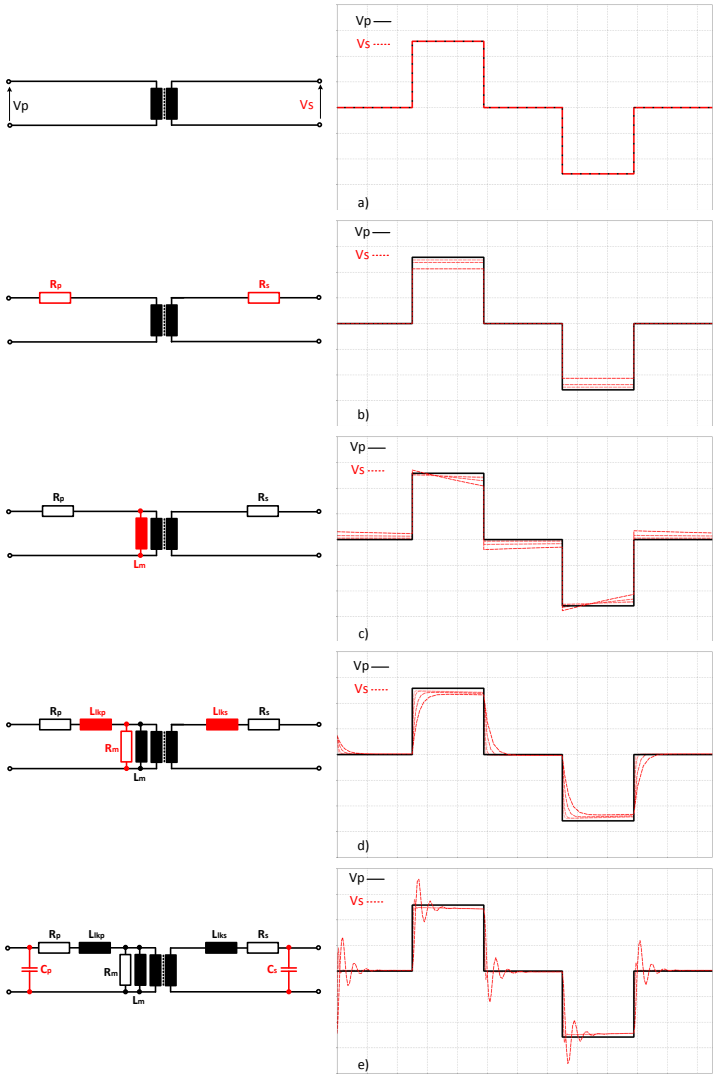


Fig. 6.18: Impact of non-idealities on transformer secondary voltage: a) ideal case; b) winding resistances; c) magnetizing inductance; d) leakage inductance and core equivalent resistance; e) windings stray capacitance.

$$F_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot \frac{C_{sn}}{N_{diodes}}}} \tag{6.5}$$

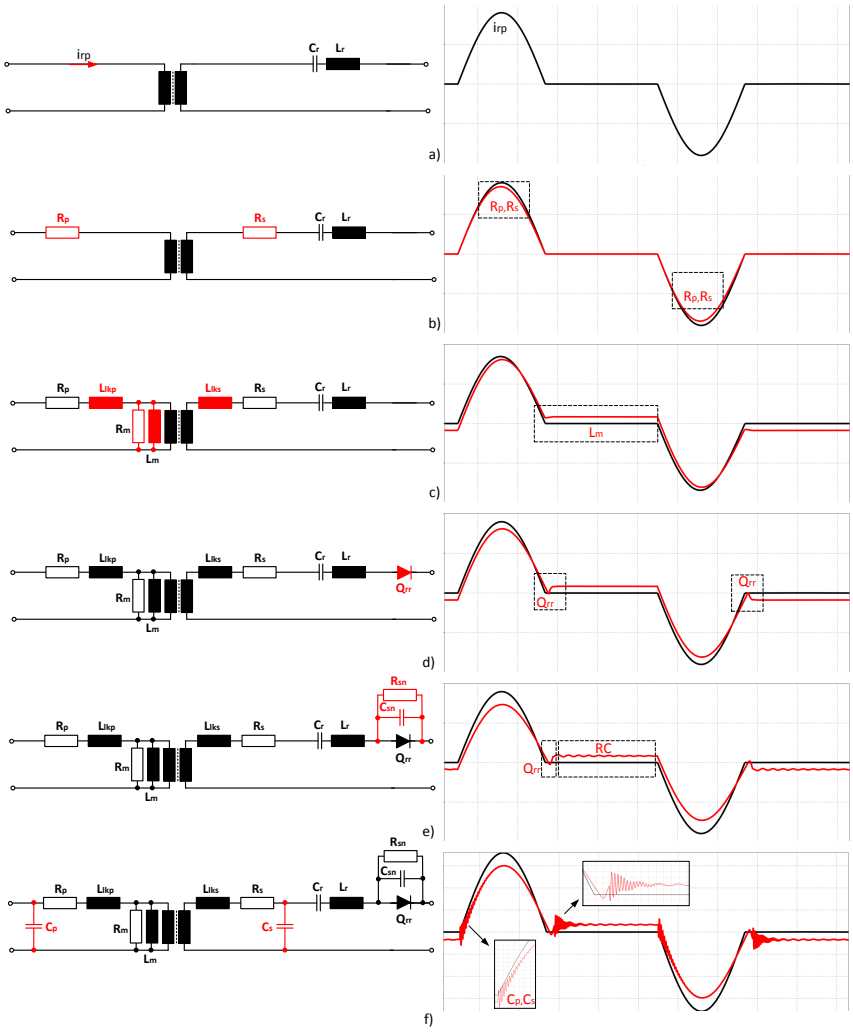


Fig. 6.19: Impact of non-idealities on primary resonant current: a) ideal case; b) transformer windings' resistances; c) transformer windings' leakage inductance, magnetizing inductance and core equivalent resistance; d) rectifier diode storage charge Q_{rr}; e) Parallel grading resistor R_{sn} and capacitor C_{sn}.

The final step is to include the windings stray capacitance, as displayed in Fig. 6.19f and current oscillations are noticed during the turn-on and turn-off period. The oscillations are generated by the transformer magnetizing inductance L_m and winding stray capacitance C_p and C_s and have the resonant frequency equal to eq. 6.6:

$$F_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_m \cdot (C_p \cdot N^2 + C_s)}} \tag{6.6}$$

6.6 Conclusions

The impact of switching frequency and voltage drop between input and output dc-link levels on peak resonant current and voltage stress have been discussed, as they will determine the specifications for semiconductors and resonant tank parameters. Operation in DCM1 mode leads to constant peak in resonant current and voltage waveforms in entire operating range, but as soon as ΔV increases, the peak values increase propotional. It is therefore critical for the designer to evaluate from the beginning the maximum acceptable voltage variations so the maximum acceptable stress is evaluated and selection of components is performed accordingly. Further on, device waveforms for each mode of operation have been introduced, and it has been shown that soft-switching capabilities are maintained in DCM1, DCM2 and CCM1-Hybrid, while in CCM1, switching losses increase as ZVS at turn-on is lost.

Voltage balancing across the series connected diodes has been investigated and concluded that only 5% variation in stored charge Q_{rr} can lead to a maximum overvoltage of 45%. Further on, when selecting the snubber capacitor value and grading resistance, the valve designer will need to make a tradeoff between maximum blocking voltage and impact on resonant current peak value.

Different valve mechanical structures have been discussed and proposed. Based on the valve equivalent circuit, it was concluded that voltage sharing across the diodes is impacted by the parasitic capacitances that exist between conductors and adjacent valve structures. In the end, the sensitivity studies discussed in Chapter VI are for the benefit of the designer that needs to evaluate worst case scenarios for determination of specifications, which will be used in the design guide line, proposed in Chapter 7. Further on, a careful selection of rectifier side diodes and balancing circuits will have an impact on total losses.

Chapter 7

Design guide line for SRC#

Summary

This chapter discusses a design guide line for the SRC# as presented in [125]. The guide line is suitable for a certain range of specifications, in the megawatt, kilovolt and kilohertz range, required by the application. Certain technology areas are predefined and a step by step methodology is given. Selection of switching frequency, determination of specifications for semiconductor and medium frequency transformer ratings, design of resonant tank and dc link banks are shown. Output results are volume, weight, losses and bill of materials. A 10MW design example is finally illustrated.

7.1 Methodology

A standard step by step design guide line methodology for SRC# similiar to [143] is proposed in Fig. 7.2 and detailed in Fig. 7.3. Selection of switching frequency, determination of specifications for semiconductors, medium frequency transformer, resonant tank components and dc link capacitors are discussed. Output results are volume, weight, losses and bill of materials cost, with a design example of 10 MW illustrated at the end of the chapter. Following assumptions are made: Nominal power, nominal input and output voltage are the fundamental converter specifications. They will determine the ratings of the transformer, semiconductors (igbts and diodes), LC tank, insulation, modularity, availability, input and output DC link capacitors and cooling system. The general methodology from Fig. 7.2 is explained as it follows:

- Step 1: determines based on input specifications, selected design parameters and technology selection the main circuit design. LC tank parameters are calculated and peak stress current and voltage are determined based on the SRC# model. Further on, analysis of worst case scenario is performed and maximum load operating point for semiconductor and transformer are determined based on performed studies (steady state, dynamic, faults, etc.). These values will define the worst case component loads and must be designed for as seen in Fig. 7.1. The transient use cases driving the worst loads must be steps in terminal voltages and steps in power command. The steady-state use cases driving the worst loads must be extreme ratios of V_{in}/V_{out} for any active power.
- Step 2: Sub-system design is performed, with device selection on inverter and rectifier side. Transformer geometry is selected with the condition of using the leakage inductance as part of the resonant inductance.

- Step 3: At this level, losses and temperature are estimated for all sub-systems, with the transformer thermal model parameters similar to [144].
- Step 4: Volume and mass is computed for all sub-systems.

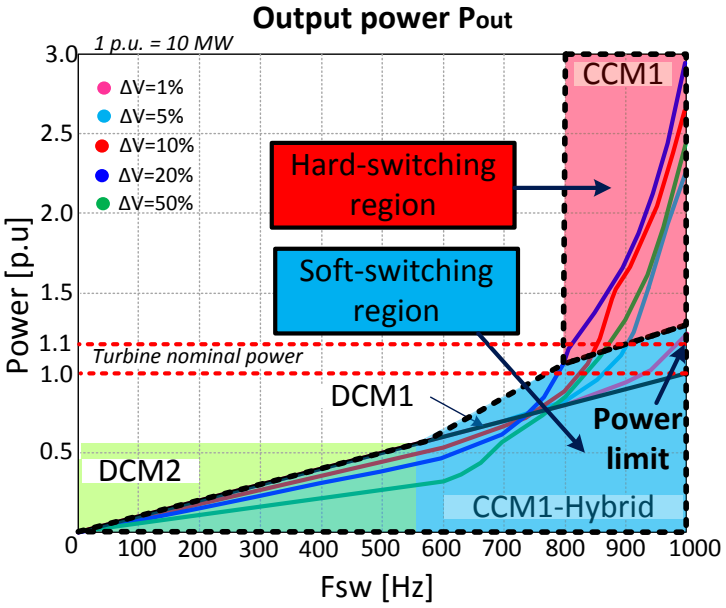


Fig. 7.1: Soft-switching operating boundaries

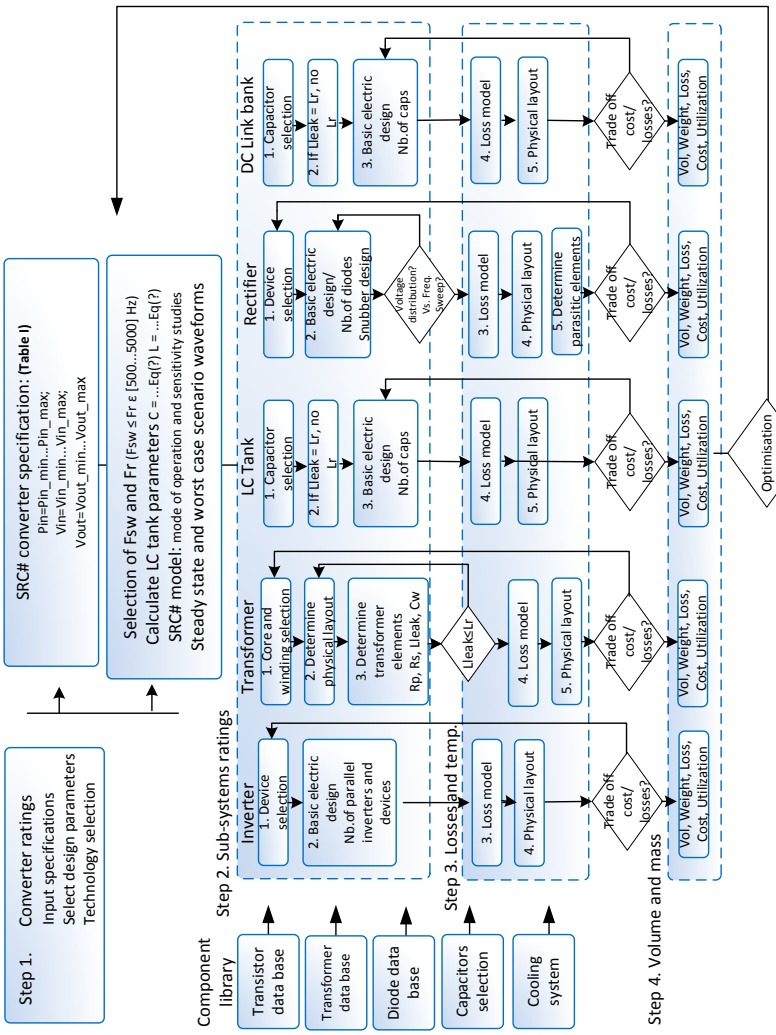


Fig. 7.2: Main flow chart

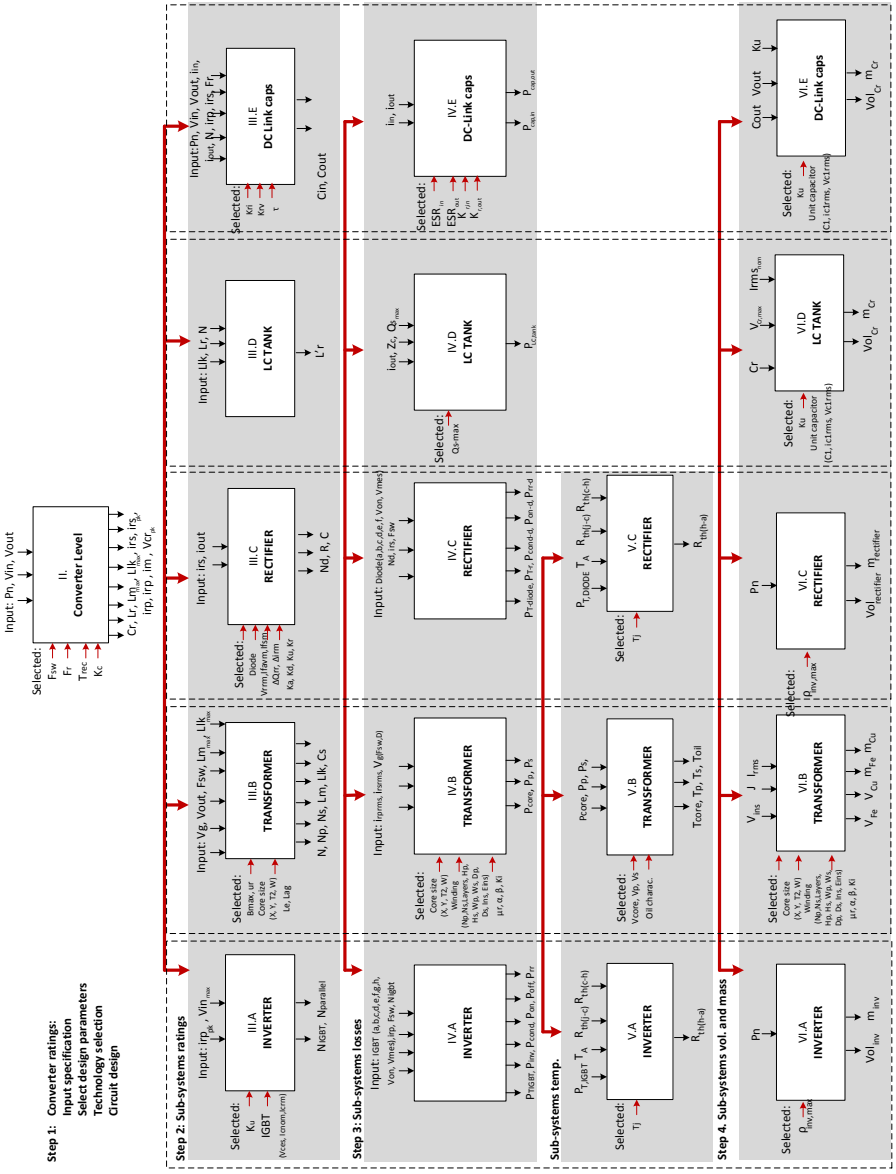


Fig. 7.3: Detailed flow chart

7.2 Converter ratings

7.2.1 Input specifications

In Table. 7.1, the list of fundamental input specifications is illustrated. Based on these, the converter design will perform the next steps.

Table 7.1: Input specifications

P_{in}	- Nominal power
$P_{in,max}$	- Nominal max. acc. power
V_{in}	- Input DC voltage
$V_{in,max}$	- Input max. acc. DC voltage
$V_{in,min}$	- Input min. acc. DC voltage
V_{out}	- Output DC voltage
$V_{out,max}$	- Output max. acc. DC voltage
$V_{out,min}$	- Output min. acc. DC voltage
η	- Min. acc. efficiency
ρ	- Min. acc. power density

Further on, Table. 7.2 presents a list of selected design parameters, where the designer has certain degress of freedom with pro's and con's. For instance, selection of maximum switching frequency is determined based on a trade-off between system losses, transformer size and the challenges in extracting the heat. The IGBTs utilization factor (defined as I_{Cnom}/I_C, transformer flux density, number of turns per layer, LC tank quality factor and so on, are all design parameters selected in the initial design phase.

7.2.2 Technology selection

The proposed design guide line has a validity range suitable for megawatt, kilohertz and kilovolt ratings. Following technology constraints are made on each sub-system level: IGBT power modules on rectifier side, line frequency press-pack diodes on rectifier side, amorphous c-core on transformer level.

1. Inverter:

- Semiconductors: Thyristors; IGCTs; IEGTs; IGBTs
- Packaging: power module; presspack
- Cooling type: Natural air; Forced air; Water/Glycol cooling

2. Transformer:

- Core type: C - core; Shell core; Nanocrystalline;
- Core material: Silicon iron; Ferrite; Amorphous;
- Cooling type: Natural air; Forced air; Water/Glycol cooling; Oil immersion

Table 7.2: Design parameters

F_{sw}	- Switching frequency
F_r	- Resonant frequency
T_{rec}	- Diode reverse recovery
K_c	- percentage of load current
K_u	- IGBT utilization factor
$IGBT_{(V_{CES},I_{CNOM},I_{CRM})}$	- IGBT parameters
B_{max}	- Transformer Flux density
$Core_{size(X,Y,T2,W)}$	- Core geometry
L_{ag}	- transformer max. air gap
μ_r	- core relative permeability
$Winding_{arrangement}$	- (Turns x Layers x Size)
$Q_{s,max}$	- LC tank quality factor
$T_{j,igbt}$	- IGBT junction temperature
$T_{j,diode}$	- Rectifier diode junction temperature
$T_{j,core}$	- Transformer core temperature
$T_{j,p}$	- Primary winding temperature
$T_{j,s}$	- Secondary winding temperature
$Power_{density,inv}$	- Inverter power density
$Power_{density,r}$	- Rectifier power density
Ku_{res}	- Utilization factor resonant unit capacitor
$Ku_{dc-link}$	- Utilization factor unit dc link capacitor
$Diode(V_{rrm}, I_{favm}, I_{fsm}$	- Rectifier diode parameters
ΔQ_{rr}	- Max. spread of stored charge
Δi_{rm}	- Max. spread of leakage current
K_a	- arrester utilization factor
K_d	- uneven voltage distribution factor
K_u	- Diode voltage utilization factor
K_r	- redundancy factor
$K_{r,v}$	- voltage ripple dc link
$K_{r,i}$	- current ripple dc link
τ	- time constant dc link

- Winding type: round wire; Litz wire; Foil windings;
- Insulation material: Nomex paper + Oil; Epoxy resin; etc.

3. Rectifier

- Semiconductors: Fast recovery diodes; Standard recovery diodes
- Packaging: Power modules; press-pack;
- Cooling type: Natural air; Forced air; Water/Glycol cooling;
- Insulating medium: air, SF6, oil.Oil immersion

4. Resonant capacitor tank

- Capacitor technology: Monolithic electrolytic; Modular Thin film; metallized polypropylene
- Cooling type: Natural air; Forced air; Water/Glycol cooling;
- Overload protection: fused; self-healing.

5. DC Link capacitor tank

- Unit capacitor: Electrolytic; Thin film; metallized polypropylene
- Cooling type: Natural air; Forced air; Water/Glycol cooling;
- Overload protection: fused; self-healing.

7.2.3 Circuit design

Table 7.3: Main circuit design parameters

F_{sw}	- switching frequency
F_r	- resonant frequency
C_r	- resonant capacitor
L_r	- resonant inductor
$L_{m,max}$	- max.acc. magnetizing inductance
$L_{lk,max}$	- max.acc. leakage inductance
i_{rp}	- primary side resonant current
i_{rs}	- secondary side resonant current
$i_{rp,pk}$	- primary side peak resonant current
$i_{rs,pk}$	- secondary side peak resonant current
V_{Cr}	- resonant capacitor voltage
$V_{Cr,pk}$	- resonant capacitor peak voltage
V_g	- inverter output voltage
T_{rec}	- rectifier diode reverse recovery time
N	- transformer turns ratio
V_t	- LC tank voltage
Z_c	- characteristic impedance
M	- normalized output voltage
Q_s	- normalized load parameter
λ	- normalized switching frequency
K	- constant parameter
K_c	- percentage parameter
ω_r	- resonant angular frequency

Selection of switching frequency

Selection of switching frequency is a crucial step, as it will determine transformer size, losses, acoustic noise and semiconductor losses, The DC/DC converter will operate with variable frequency and phase shift from 0 Hz to a maximum frequency. Therefore determining the maximum switching frequency will determine peak current, voltage and a resonant pulse duration. To avoid operation in resonant and super resonant mode, $F_{sw,max}$ needs to be lower then the resonant frequency. In the end, selection of F_{sw} will be a trade-off between transformer loss density and size, as seen in Fig. 7.4.
The benefit from increased frequency will be a smaller transformer core size, but a compact structure will be challenged by winding layout (parasitic capacitance will impact resonant waveforms), losses and heat removal. From various paper design studies, it is proposed to configure the maximum

switching frequency in the range of eq. (7.3):

$$F_{sw,max} \leq F_r \; \epsilon \; [0.5 - 5.0] \; kHz \tag{7.1}$$

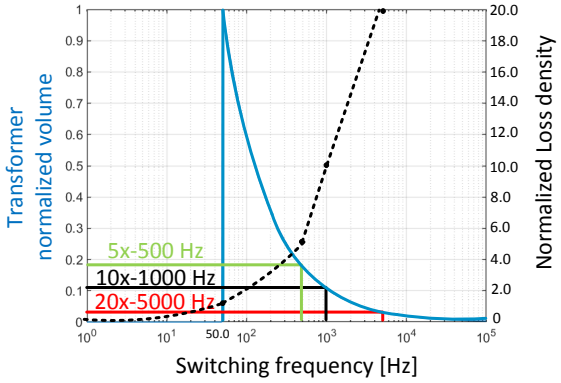


Fig. 7.4: Selection of maximum switching frequency

To further discuss the selected frequency range, for 6.5 kV IGBTs, switching frequencies of 10 kHz have been reported [120], while for monolithic transformers, [112] proposes a 3 MW transformer designed for 10 kHz. In the author's opinion, this is not a realistic target, as transformer's impact of parasitics elements are proportional to frequency and turns ratio. Further on, [112] suggests the design based on previous work from [73], where a modular approach for 100 kW was employed. It is also believed, that extracting the heat out will require a very small coolant to windings thermal resistance $R_{th,coolant}$. Based on this aspects, it was decided to limit the upper range of maximum switching frequency to 5 kHz. So, if maximum switching frequency is selected to be 5 kHz, the converter will operate from 0 to 5 kHz, meaning in the audible range (0.1-20 kHz). To limit the acoustic noise and vibration, important effort needs to be put in the design of transformer's enclosure and should be adressed in future work.

Resonant frequency

Selection of maximum switching frequency will determine the resonant frequency. Considering that the converter will deliver nominal power P_n at $F_{sw,max}$ then the resonant frequency F_r should be high enough to allocate an evacuation time T_{rec}, as seen in Fig. 7.5 and eq. (7.4):

$$F_r = F_r + \frac{1}{T_{rec}} \tag{7.2}$$

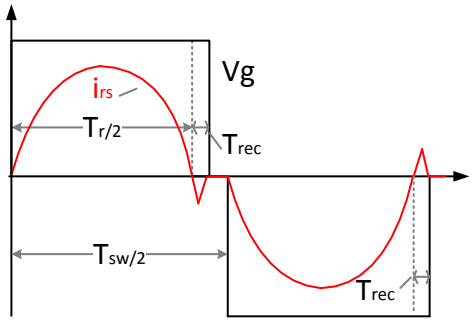


Fig. 7.5: Selection of resonant frequency

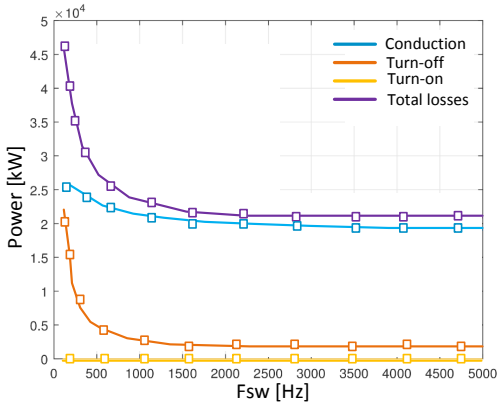


Fig. 7.6: Impact of switching frequency on conduction and switching losses

Another important aspect to discuss is the impact of selected switching frequency on the semiconductor conduction and switching losses, as seen in Fig. 7.6. In the range 500 to 5000 Hz, calculated inverter and rectifier losses remain constant. For example, if selected maximum switching frequency is 5000 Hz, one would expect the amount to total semiconductor losses to be the similar if the selected frequency would be 1000 Hz. The reason lies in the principle of operation and selection of the LC tank. As output power is dependent on number of pulses, it is expected that regardless of selected switching frequency, same amount of energy is delivered per second, the exception being the duration of 1 pulse of energy. At 5000 Hz, there are 5000 pulses of shorter duration, while at 1000 Hz, there are 1000 pulses but each pulse has 5 times longer time duration. As in both cases, the semiconductors

experience ZVS at turn-on, while the turn-off losses are only impacted by the magnetizing current. But again, in the higher range of switching frequency, the transformer will also have a lower magnetizing inductance, thus a lower magnetizing current.

1. Select switching frequency

$$F_{sw} \leq F_r \; \epsilon \; [0.5 - 5.0] \; kHz \tag{7.3}$$

2. Select resonant frequency

$$F_r = F_r + \frac{1}{T_{rec}} \tag{7.4}$$

3. Calculate resonant capacitor

$$C_r = \frac{P_{out}}{4 \cdot F_{sw} \cdot N \cdot V_{in} \cdot V_{out}} \tag{7.5}$$

4. Calculate resonant inductor

$$L_r = \frac{1}{C_r \cdot (2\pi \cdot F_r)^2} \tag{7.6}$$

$$L_{lk,max} \leq L_r \tag{7.7}$$

5. Calculate secondary side resonant current and voltage

$$i_{rs}(t) = \frac{V_t(t) - V_{Cr}(0)}{Z_c} \sin \omega_r(t) + i_{rs}(0) \cos \omega_r t \tag{7.8}$$

$$V_{Cr}(t) = V_t(t) - (V_t(t) - V_{Cr}(0)) \cos \omega_r(t) + i_{rs}(0) Z_c \sin \omega_r t \tag{7.9}$$

6. Calculate secondary side peak current and voltage

$$V_{Cr,pk} = \frac{M \cdot K \cdot V_g}{2} \tag{7.10}$$

$$i_{rs,pk} = \omega_r \cdot C_r \cdot V_g \cdot (M(K+1) - 1) \tag{7.11}$$

where M is the normalized output voltage and Q_s is the normalized load

parameter:

$$M = \frac{V_{out}}{V_g} \tag{7.12}$$

$$K = \frac{Q_s \cdot \lambda}{2} \tag{7.13}$$

$$Q_s = \frac{P_{out}}{\omega_r \cdot C_r \cdot V_{out}^2} \tag{7.14}$$

$$\gamma = \frac{F_r \cdot \pi}{F_{sw}} \tag{7.15}$$

7. Calculate primary side resonant current

$$i_{rp} = i_{rs} \cdot N \tag{7.16}$$

8. Calculate maximum accepted magnetizing inductance and current

$$i_m = k_c \cdot i_{rp,pk},\ k_c\ \epsilon\ [1.0 - 5.0]\% \tag{7.17}$$

$$L_{m,max} = \frac{V_{in}}{4 \cdot k_c \cdot F_{sw} \cdot i_{rp,pk}} \tag{7.18}$$

7.3 Sub-system ratings

7.3.1 Inverter

The main specifications for the inverter are the conducted peak primary side current $i_{rp,pk}$ and maximum allowed input voltage $V_{in,max}$.

Table 7.4: Inverter design parameters

$i_{rp,pk}$	- primary resonant peak current
$V_{in,max}$	- input max. acc. DC voltage
K_u	- voltage utilization factor
V_{CES}	- IGBT collector-emitter voltage
I_{CNOM}	- IGBT continuous DC collector current
I_{CRM}	- IGBT repetitive peak collector current
SOA	- safe operating area
$N_{parallel}$	- number of parallel inverters
N_{IGBT}	- total number of IGBTs

1. Select IGBT V_{ce} category

The final device is selected based on collector-emitter voltage V_{CES}, continuous DC current $I_{c,nom}$ and repetitive peak collector current $I_{C,RM}$ ratings.

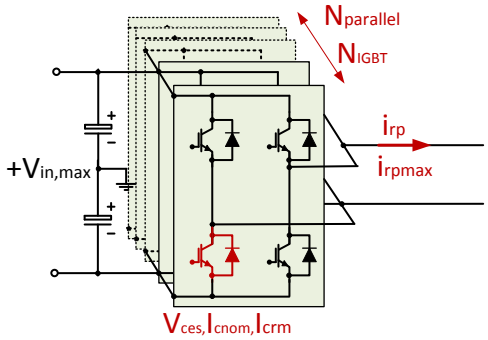


Fig. 7.7: Inverter main design parameters

$$V_{CES} \geq \frac{V_{in,max}}{K_u} \tag{7.19}$$

2. Select IGBT with highest $I_{C,nom}$ for selected voltage category

In order to be in the safe operating area, as stated in the device data sheet, the peak collector current should not exceed the SOA limits.

3. Calculate number of parallel inverters

$$N_{parallel} = \frac{i_{rp,pk}}{I_{CRM}} \tag{7.20}$$

4. Calculate number of discrete devices

$$N_{IGBT} = 4 \cdot N_{parallel} \tag{7.21}$$

7.3.2 Transformer

Preliminary design parameters for the medium frequency transformer are presented in Table. 7.5. Main specifications for design are: P_n, V_{in}, V_{out}, L_m, L_{lk}, maximum accepted air gap, insulation level, core and windings maximum accepted temperatures. As mentioned in Chapter IV, only one monolithic transformer with one primary and one secondary winding will be employed in the converter. Transformer geometry will be impacted by core selection, turns ratio and insulation levels. Turns ratio is selected based

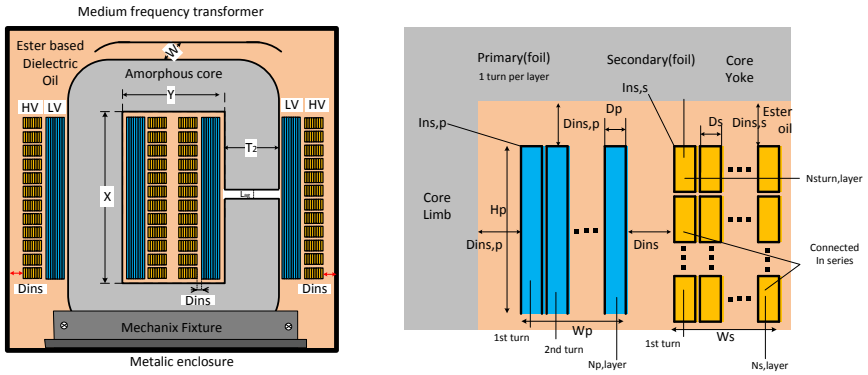


Fig. 7.8: Transformer core and windings section

Table 7.5: Transformer design parameters

V_{in}	- input DC voltage
V_{out}	- output DC voltage
F_{sw}	- switching frequency
B_{max}	- flux density
L_m	- magnetizing inductance
$L_{m,max}$	- max. acc. magnetizing inductance
L_{lk}	- leakage inductance
$L_{lk,max}$	- max. acc. leakage inductance
N	- transformer turns ratio
N_p	- primary number of turns
N_s	- secondary number of turns
A	- core area
A_p	- area product
μ_o	- absolut magnetic permeability
μ_r	- relative magnetic permeability
L_e	- mean magnetic path length
L_{ag}	- air gap magnetic path length
R_e	- ideal transformer reluctance
R_{ag}	- air gap reluctance
R_t	- total core reluctance

on DCM operation in full operational range of the converter, as seen in eq. 7.25. The proposed winding layout in this approach is shown in Fig. 7.8. Each core limb has a primary and secondary winding. Primary winding has a layered construction of N_p turns, while the secondary winding is divided in a number of layers with a certain number of turns.

1. Select core: geometry, material, size

$$V_c = (\frac{P_n}{4 \cdot J \cdot B_{max} \cdot F_{sw}})^{\frac{3}{4}} \quad (7.22)$$

$$V_c = K_{vol} \cdot A_{p,max}^{0.75} \quad (7.23)$$

$$A_p \geq A_{p,max} \quad (7.24)$$

2. Select wire: type and material

3. Calculate turns ratio N

$$N = \frac{V_{out}}{V_g} \quad (7.25)$$

4. Calculate primary and secondary turns

Further on, primary and secondary turns are calculated based on the selected maximum switching frequency F_{sw}:

$$N_p = \frac{Vg}{4 \cdot B_{max} \cdot A \cdot F_{sw}} \quad (7.26)$$

$$N_s = N \cdot N_p \quad (7.27)$$

5. Calculate mean magnetic path

$$L_e = 2 \cdot (X + Y) + 8 \cdot (\frac{T2}{2}) + L_{ag} \quad (7.28)$$

6. Calculate magnetic reluctance

$$R_e = \frac{Le}{\mu_0 \cdot \mu_r \cdot A} \quad (7.29)$$

$$R_{ag} = \frac{L_{ag}}{\mu_0 \cdot A} \quad (7.30)$$

$$R_t = R_e + R_{ag} \quad (7.31)$$

7. Calculate magnetizing inductance

$$L_m = \frac{N_p^2}{R_t} \quad (7.32)$$

8. Compare L_m with $L_{m,max}$

$$L_m \leq L_{m,max} \quad (7.33)$$

9. Calculate leakage inductance and stray capacitance

According to [141], the ratio of leakage inductance L_{ls} and windings stray capacitance C_d can be varied by the mechanical dimensions of the transformer, meaning the distances, heights and the lengths of the windings. Basically, the leakage inductance are calculated based on the stored energy in the magnetic and electric field.

$$L_{lk} = \mu \cdot \frac{{N_p}^2 \cdot l_w \cdot d_w}{h_k} \tag{7.34}$$

$$C_d = \frac{1}{3} \cdot \epsilon \cdot (\frac{N_s}{N_p})^2 \cdot (\frac{l_w \cdot h_w}{d_w}) \tag{7.35}$$

In eq. 7.34 and eq. 7.34, h_k represents the core height, h_w is the winding's height, d_w is the distance between the primary and secondary winding while l_w is the winding length.

Design procedures regarding transformer leakage inductance, stray capacitance and insulation are investigated in [141] and [145].

7.3.3 Rectifier

Design steps for the medium voltage rectifier are presented in the following steps. Design parameters are shown in Table. 7.6. The rectifier is implemented in a simple full bridge configuration, with series connected diodes, as seen in Fig. 7.9.

Table 7.6: Rectifier design parameters

i_{rs}	- secondary resonant current
i_{out}	- output DC current
V_{Cr}	- resonant capacitor voltage
R	- steady state blocking voltage resistor
C	- dynamic state blocking voltage resistor
I_{FSM}	- diode surge current
I_{FAVM}	- average on state current
V_{TOV}	- maximum valve blocking voltage
$V_{RRM,max}$	- maximum diode blocking voltage
K_A	- arrester utilization factor
K_D	- uneven voltage distribution factor
K_{UI}	- diode voltage utilization factor
K_R	- redundancy factor
N_d	- number of diodes per arm
ΔQ_{RR}	- max. spread of stored charge
ΔI_{RR}	- max. spread of leak. current

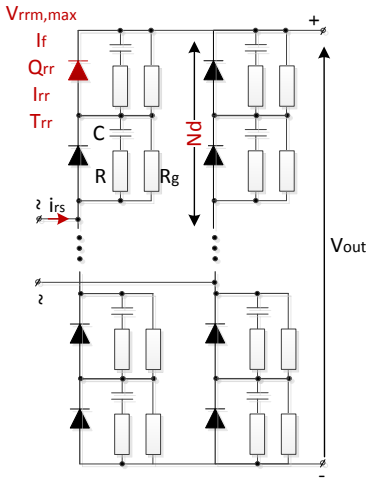


Fig. 7.9: Rectifier schematic

1. Select standard recovery diode

Line frequency press-pack diodes are pre-selected, with the challenge of kHz operating frequency. Diodes in power modules packages are also an alternative, but the issue of open circuit in case of fault per diode, does not leave space for redundancy. As high voltage bipolar diodes will be employed, and the important data sheet parameters are the repetitive reverse voltage V_{RRM}, continuous DC forward current I_{FAVM} and reverse recovered charge Q_r.

$$V_{RRM,MAX} \quad \epsilon \quad [2000V...6500V] \tag{7.36}$$

$$I_{FAVM} \quad \geq \quad i_{out} \tag{7.37}$$

$$I_{FSM} \quad \geq \quad 50 \cdot i_{out} \tag{7.38}$$

2. Maximum accepted Q_{rr}

The selected diode needs to fulfill the condition of having the reverse recovery charge smaller then a maximum threshold, that is determined from the list of studies.

$$Q_{rr} \leq Q_{rr.max} \tag{7.39}$$

3. Calculate number of diodes

The total number of series connected diodes is computed with eq. 7.40 and the parameters are described in Table. 7.6.

$$N_d = \frac{V_{TOV} \cdot K_A}{V_{RRM,max} \cdot K_V \cdot K_D \cdot K_R} \tag{7.40}$$

4. Calculate RC parameters

The goal of the snubber and parallel RC circuit is to achieve voltage symmetry across the diodes. Equations to calculate the resistance and capacitance values are:

$$R \leq \frac{N_d V_{rrm} - V_{TOV}}{(N_d - 1)\Delta I_{rm}} \tag{7.41}$$

$$C \geq \frac{(N_d - 1)\Delta Q_{RR}}{N_d V_{rrm} - V_{TOV}} \tag{7.42}$$

7.3.4 LC tank - resonant inductor

The designer will have to evaluate what percentage of the resonant inductor value can be incorporated as the transformers own leakage inductance and

Table 7.7: LC tank parameter

N	- transformer turns ratio
L_{lk}	- leakage inductance
L_r	- resonant inductor
$L_r{}'$	- updated resonant inductor

Fig. 7.10: LC tank parameters

1. Calculate updated resonant inductor

The updated resonant inductor L_r' is calculated in the situation where the leakage inductance of the transformer is smaller then the required theoretical

value.

$$L_r' = L_r - (L_{lk} \cdot N^2) \tag{7.43}$$

7.3.5 DC Link capacitors

Output and input dc-link capacitances are calculated in the following steps, with respect to Table. 7.8

Table 7.8: Design parameters for input and output dc-link banks

P_n	- nominal power
V_{in}	- input dc voltage
V_{out}	- output dc voltage
i_{in}	- input dc current
i_{out}	- output dc current
i_{rp}	- resonant primary current
i_{rs}	- resonant secondary current
N	- transformer turns ratio
C_{in}	- input dc-link capacitance
C_{out}	- output dc-link capacitnace
E_{cap}	- capacitor stored energy
τ	- time constant
$K_{r,i}$	- current ripple factor
$K_{r,v}$	- voltage ripple factor

1. Calculate output dc-link capacitance

Output capacitance value is determined by the maximum power point, which will occur at the highest frequency. Compared to the resonant tank values, the output filter has a large time constant and the filter elements are comparably larger.

$$C_{out} = \frac{2 \cdot E_{cap}}{V_{out}^2} = \frac{2 \cdot P_n \cdot \tau}{V_{out}^2} \tag{7.44}$$

$$\tag{7.45}$$

2. Calculate input dc-link capacitance

$$C_{in} = C_{out} \cdot N^2 \tag{7.46}$$

3. Calculate output dc-link capacitance based on current and voltage ripple

$$C_{out} = \frac{\sqrt{2} i_{rs} - K_{r,i} \cdot i_{out}}{2\pi F_r \cdot K_{r,v} \cdot V_{out}} \tag{7.47}$$

4. Calculate input dc-link capacitance based on current and voltage ripple

$$C_{in} = \frac{\sqrt{2} i_{rp} - K_{r,i} \cdot i_{in}}{2\pi F_r \cdot K_{r,v} \cdot V_{in}} \tag{7.48}$$

7.4 Sub-systems losses and temperature

7.4.1 Inverter

The strategy in calculating semiconductors loss model is described in detail in the Appendix and Table. 7.9 described all the parameters. Table. 7.10 shows loss model coefficients for 6.5 kV IGBTs.

Table 7.9: Inverter loss model parameters

a, b	- cond.loss parameters
c, d	- turn on loss parameters
e, f	- turn off loss parameters
g, h	- rev.rec. loss parameters
E_{on}	- turn on. loss energy
E_{off}	- turn off. loss energy
E_{rr}	- rev. rec. loss energy
i_{rp}	- primary resonant current
F_{sw}	- switching frequency
$P_{T,igbt}$	- Total IGBT loss
$P_{T,inv}$	- Total inverter loss
P_{cond}	- Cond. IGBT loss
P_{on}	- Turn on IGBT loss
P_{off}	- Turn off IGBT loss
$V_{on,mes}$	- Specification Turn-on Collector emitter voltage
$V_{on,nom}$	- Data sheet Turn-on Collector emitter voltage
$V_{off,mes}$	- Specification Turn-off Collector emitter voltage
$V_{off,nom}$	- Data sheet Turn-off Collector emitter voltage

Table 7.10: Loss model for 6.5 kV IGBTs

	P_{cond}		E_{on}		E_{off}		E_{rr}	
	a	b	c	d	e	f	g	h
Infineon	0.002	2.299	0.011	-0.361	0.0056	0.0638	0.0	0.0
ABB	0.0027	1.862	5e-6	0.0033	0.0067	0.5183	0.0	0.0

1. Calculate conduction losses

$$P_{Cond} = a \cdot {i_{rp}}^2 + b \cdot i_{rp} \tag{7.49}$$

(7.50)

2. Calculate turn on losses

$$E_{on} = c \cdot i_{rp} + d \tag{7.51}$$

$$P_{on} = E_{on} \cdot F_{sw} = \frac{V_{on,mes}}{V_{on,nom}} \cdot E_{on,nom} \cdot F_{sw} \tag{7.52}$$

3. Calculate turn off losses

$$E_{off} = e \cdot i_{rp} + f \tag{7.53}$$

$$P_{off} = E_{off} \cdot F_{sw} = \frac{V_{off,mes}}{V_{off,nom}} \cdot E_{off,nom} \cdot F_{sw} \tag{7.54}$$

4. Calculate diode turn off losses

$$E_{rr} = g \cdot i_{rp} + h \tag{7.55}$$

$$P_{rr} = E_{rr} \cdot F_{sw} = \frac{V_{rr,mes}}{V_{rr,nom}} \cdot E_{rr,nom} \cdot F_{sw} \tag{7.56}$$

5. Calculate total IGBT losses

$$P_{T,igbt} = P_{cond} + (E_{on} + E_{off} + E_{rr}) \cdot F_{sw} \tag{7.57}$$

6. Calculate total inverter losses

$$P_{T,inv} = N_{IGBT} \cdot P_{T,igbt} \tag{7.58}$$

Inverter temperature calculation

Calculation of IGBT junction temperature is performed based on input data from data sheet, by knowing R_{thJC} and Z_{thJC} (see Fig. 7.11), where the first parameter is suitable to estimate temperature for DC collector current, while for pulsed collector current the second parameter is employed [ref.IGBT calculation]. Thermal model parameters are presented in Table. 7.11.

1. IGBT junction temperature

$$T_j = P_{T,igbt} \cdot R_{th,igbt} + T_a \tag{7.59}$$

2. IGBT total thermal resistance

$$R_{th,igbt} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \tag{7.60}$$

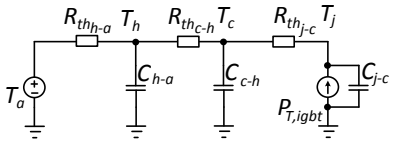


Fig. 7.11: IGBT thermal model

Table 7.11: IGBT thermal model parameters

T_j	- IGBT junction temperature
T_a	- Ambient temperature
$P_{T,igbt}$	- Total igbt loss
$R_{th,igbt}$	- Total igbt thermal resistance
$R_{th(j-c)}$	- IGBT junction to case thermal resistance
$R_{th(c-h)}$	- IGBT case to heat sink thermal resistance
$R_{th(h-a)}$	- Heat sink to ambient thermal resistance
$Z_{th,igbt}$	- Transient IGBT junction to case thermal impedance
t	- transient thermal impedance parameter
τ_i	- transient thermal impedance parameter

3. IGBT transient thermal impedance

$$Z_{th,igbt} = \sum_{i=1}^{n} R_{th(j-c),i}(1 - e^{\frac{-t}{\tau_i}}) \tag{7.61}$$

7.4.2 Transformer

The medium frequency transformer loss model is presented in the following steps, with the loss model parameters identified in Table. 7.13. Loss calculation was performed according to the works of [67], [77], [78]

1. Calculate primary skin depth

$$\delta_p = \sqrt{\frac{2}{2 \cdot \pi \cdot i_{rp,rms_N} \cdot \mu_{cu} \cdot \sigma_{cu}}} \tag{7.62}$$

$$\Delta_p = \frac{D_p}{\delta_p} \tag{7.63}$$

$$\tag{7.64}$$

2. Calculate primary winding mean length turn

$$MLT_p = 2 \cdot (T2 + W) + 4 \cdot (N_{p,layer} \cdot D_p + 2 \cdot D_{ins}) \tag{7.65}$$

Table 7.12: Transformer loss model parameters

α	-core loss calculation parameter
β	- core loss calculation parameter
K_i	- core loss calculation parameter
V_{Fe}	- Transformer core volume
δ_p	- primary winding skin penetration depth
δ_s	- secondary winding skin penetration depth
$R_{DC,p}$	- primary winding DC resistance
$R_{DC,s}$	- secondary winding DC resistance
D_p	- primary foil thickness
D_s	- secondary foil thickness
μ_{cu}	- copper permeability
σ_{cu}	- copper conductivity
i_{rp,rms_N}	- RMS of the N^{th} harmonic primary resonant current
i_{rs,rms_N}	- RMS of the N^{th} harmonic secondary resonant current
P_c	- Transformer core losses
P_p	- Transformer primary winding losses
P_s	- Transformer secondary winding losses
$N_{p,layer}$	- Primary winding number of layers
$N_{s,layer}$	- Secondary winding number of layers
$N_{pturn,layer}$	- Primary winding number of turns per layer
$N_{sturn,layer}$	- Secondary winding number of turns per layer
MLT_p	- Primary winding mean length turn
MLT_s	- Secondary winding mean length turn
H_p	- Primary winding height
H_s	- Secondary winding weight

3. Calculate primary winding DC resistance

$$R_{dc,p} = N_{p,layer} \cdot N_{pturn,layer} \cdot \frac{MLT_p}{\sigma_{cu}} \cdot D_p \cdot H_p \tag{7.66}$$

4. Primary winding loss

$$P_p = R_{DC} \cdot \Delta_p \cdot [A + \frac{2 \cdot ({N_{p,layer}}^2 - 1)}{3} + B] \cdot {i_{rp,rms_N}}^2 \tag{7.67}$$

$$A = \frac{\sinh(\Delta_p) + \sin(\Delta_p)}{\cosh(\Delta_p) - \cos(\Delta_p)} \tag{7.68}$$

$$B = \frac{\sinh(\Delta_p) - \sin(\Delta_p)}{\cosh(\Delta_p) - \cos(\Delta_p)} \tag{7.69}$$

5. Calculate secondary skin depth

$$\delta_s = \sqrt{\frac{2}{2 \cdot \pi \cdot i_{rs,rms_N} \cdot \mu_{cu} \cdot \sigma_{cu}}} \tag{7.70}$$

$$\Delta_s = \frac{D_s}{\delta_s} \tag{7.71}$$

$$\tag{7.72}$$

6. Calculate secondary winding mean length turn

$$MLT_s = 2 \cdot (T2 + W) + 4 \cdot (N_{s,layer} \cdot D_s + 2 \cdot D_{ins} + N_{p,layer} \cdot D_p + D_{ins}) \tag{7.73}$$

7. Calculate secondary winding DC resistance

$$R_{dc,s} = N_{s,layer} \cdot N_{sturn,layer} \cdot \frac{MLT_s}{\sigma_{cu}} \cdot D_s \cdot H_s \tag{7.74}$$

8. Secondary winding loss

$$P_s = R_{DC} \cdot \Delta_s \cdot [A + \frac{2 \cdot ({N_{s,layer}}^2 - 1)}{3} + B] \cdot {i_{rs,rms_N}}^2 \tag{7.75}$$

$$A = \frac{\sinh(\Delta_s) + \sin(\Delta_s)}{\cosh(\Delta_s) - \cos(\Delta_s)} \tag{7.76}$$

$$B = \frac{\sinh(\Delta_s) - \sin(\Delta_s)}{\cosh(\Delta_s) - \cos(\Delta_s)} \tag{7.77}$$

9. Core losses

$$P_{Core} = K_i \cdot 2^{\alpha+\beta} \cdot {F_{sw}}^{\alpha} \cdot B^{\beta} \cdot D^{1-\alpha} \cdot V_{Fe} \tag{7.78}$$

Transformer temperature calculation

The transformer thermal model (presented in [Vilar-trafo model]) is illustrated in Fig. 7.12 and the parameters in Table. 7.13.

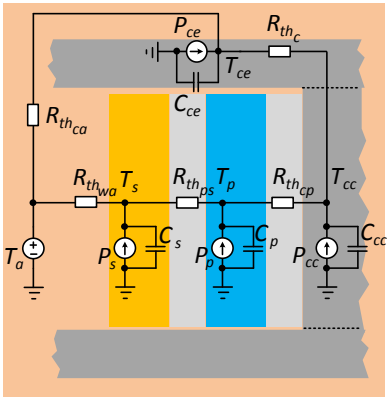


Fig. 7.12: Transformer thermal model

1. Energy balance equations

$$C_{cc}\frac{dT_{cc}}{dt} = \frac{1}{R_{thc}}(T_{ce} - T_{cc}) + \frac{1}{R_{thcp}}(T_p - T_{cc}) + P_{cc} \tag{7.79}$$

$$C_{ce}\frac{dT_{ce}}{dt} = \frac{1}{R_{thc}}(T_{cc} - T_{ce}) + \frac{1}{R_{thca}}(T_a - T_{ce}) + P_{ce} \tag{7.80}$$

$$C_p\frac{dT_p}{dt} = \frac{1}{R_{thcp}}(T_{cc} - T_p) + \frac{1}{R_{thps}}(T_s - T_p) + P_p \tag{7.81}$$

$$C_s\frac{dT_s}{dt} = \frac{1}{R_{thps}}(T_p - T_s) + \frac{1}{R_{thwa}}(T_a - T_s) + P_s \tag{7.82}$$

(7.83)

2. Calculate heat sources

$$P_{cc} = P_{Fe}V_{cc} \tag{7.84}$$

$$P_{ce} = P_{Fe}V_{ce} \tag{7.85}$$

$$P_p = P_{winding} \tag{7.86}$$

$$P_s = P_{winding} \tag{7.87}$$

Table 7.13: Transformer thermal model parameters

C_{cc}	- Core limb thermal capacitance
C_{ce}	- Core yoke thermal capacitance
C_p	- Primary winding thermal capacitance
C_s	- Secondary winding thermal capacitance
R_{thc}	- Core limb to yoke thermal resistance
R_{thcp}	- Core to primary winding thermal resistance
R_{thps}	- Primary to secondary winding thermal resistance
R_{thwa}	- Secondary winding to ambient thermal resistance
R_{thca}	- Core yoke to ambient thermal resistance
R_{theq}	- Equivalent thermal resistance of two nodes
P_{cc}	- Core limb power loss
P_{ce}	- Core yoke power loss
P_p	- Primary winding power loss
P_s	- Secondary winding power loss
P_{Fe}	- Total core power loss
T_{cc}	- Core limb temperature
T_{ce}	- Core yoke temperature
T_p	- Primary winding temperature
T_s	- Secondary winding temperature
T_a	- Ambient temperature
V_{cc}	- Core limb volume
V_{ce}	- Core yoke volume
m_{cc}	- Core limb mass
m_{ce}	- Core yoke mass
m_p	- Primary winding mass
m_s	- Secondary winding mass
m_i	- Insulating material mass
c_{p_c}	- Core limb heat capacity
c_{p_i}	- Insulating material heat capacity
$c_{p_{cu}}$	- Primary winding heat capacity
c_{scu}	- Secondary winding heat capacity
ρ_c	- Core mass density
A_i	- Area between two nodes
h_i	- Heat coefficient of element i
h_c	- Conduction heat transfer coefficient
h_{cc}	- Convection heat transfer coefficient
λ	- Fluid thermal conductivity
l	- length of considered element
D	- Surface characteristic length
Nu, G_r, P_r	- Dimensionless Nusselt, Grasshof and Prandtl number
ρ	- Fluid density
μ	- dynamic viscosity
β	- Volumetric expansion coefficient

3. Determine thermal capacitances

$$C_{cc} = c_{p_c}\, m_{cc} = c_{p_c}\, \rho_c\, V_{cc} \tag{7.88}$$

$$C_{ce} = c_{p_c}\, m_{ce} = c_{p_c}\, \rho_c\, V_{ce} \tag{7.89}$$

$$C_p = c_{p_i}\, m_i + c_{p_{cu}}\, \frac{m_p}{2} \tag{7.90}$$

$$C_s = c_{p_i}\, m_i + c_{p_{cu}}\, \frac{m_p}{2} + c_{scu}\, \frac{m_s}{2} \tag{7.91}$$

4. Determine thermal resistances

$$R_{theq} = \sum_{i=1}^{n} \frac{1}{h_i A_i} \tag{7.92}$$

$$h_c = \frac{\lambda}{l} \tag{7.93}$$

$$h_{cc} = Nu \frac{\lambda}{D} \tag{7.94}$$

$$Nu = 0.55(G_r P_r)^0.25 \tag{7.95}$$

$$G_r = \frac{\rho^2 g \beta D^3 \Delta T}{\mu^2} \tag{7.96}$$

$$P_r = c_p \frac{\mu}{\lambda} \tag{7.97}$$

7.4.3 Rectifier

The rectifier loss model parameters are illustrated in Table. 7.14 with coefficients example for 6.5kV diodes shown in Table. 7.15.

Table 7.14: rectifier_loss_model

a, b	- cond.loss parameters
c, d	- turn on loss parameters
e, f	- rev.rec. loss parameters
$E_{on,d}$	- turn on. loss energy
$E_{rr,d}$	- rev. rec. loss energy
i_{rs}	- secondary resonant current
F_{sw}	- switching frequency
$P_{T,diode}$	- Total Diode loss
$P_{T,r}$	- Total rectifier losses
$P_{cond,d}$	- Cond. Diode loss
$P_{rr,d}$	- Turn off Diode loss
$V_{on,d-mes}$	- Specification Turn-on Forward voltage
$V_{on,d-nom}$	- Data sheet Turn-on Forward voltage
$V_{rr,d-mes}$	- Specification Turn-off Forward voltage
$V_{rr,d-nom}$	- Data sheet Turn-off Forward voltage

Table 7.15: Loss model for 6.5 kV DIODEs

	$P_{cond,d}$		$E_{on,d}$		$E_{rr,d}$	
	a	b	c	d	e	f
Infineon	0.0016	1.7296	0.0	0.0	-2e-6	0.0055
ABB	0.0007	1.217	0.0	0.0	0.2e-6	0.005

1. Calculate diode conduction losses

$$P_{Cond,d} = a \cdot {i_{rs}}^2 + b \cdot i_{rs} \tag{7.98}$$

(7.99)

2. Calculate diode turn on losses

$$E_{on,d} = c \cdot i_{rs} + d \tag{7.100}$$

$$P_{on,d} = E_{on,d} \cdot F_{sw} = \frac{V_{on,d-mes}}{V_{on,d-nom}} \cdot E_{on,d-nom} \cdot F_{sw} \tag{7.101}$$

3. Calculate diode turn off losses

$$E_{rr,d} = e \cdot i_{rs} + f \tag{7.102}$$

$$P_{rr,d} = E_{rr,d} \cdot F_{sw} = \frac{V_{rr,d-mes}}{V_{rr,d-nom}} \cdot E_{rr,d-nom} \cdot F_{sw} \tag{7.103}$$

4. Calculate total diode losses

$$P_{T,diode} = P_{cond,d} + (E_{on,d} + E_{rr,d}) \cdot F_{sw} \tag{7.104}$$

5. Calculate total rectifier losses

$$P_{T,r} = N_d \cdot P_{T,diode} \tag{7.105}$$

Rectifier temperature calculation

Rectifier thermal model is shown in Fig. 7.13 and the parameters illustrated in Table. 7.16.

Table 7.16: Rectifier thermal model parameters

T_j	- Diode junction temperature
T_a	- Ambient temperature
$P_{T,diode}$	- Total diode loss
$R_{th,diode}$	- Total diode thermal resistance
$R_{th(j-c)}$	- Diode junction to case thermal resistance
$R_{th(c-h)}$	- Diode case to heat sink thermal resistance
$R_{th(h-a)}$	- Heat sink to ambient thermal resistance
$Z_{th,diode}$	- Transient diode junction to case thermal impedance
t	- transient thermal impedance parameter
τ_i	- transient thermal impedance parameter

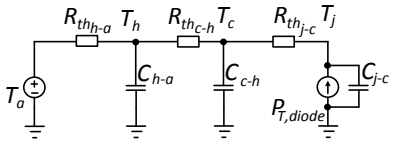


Fig. 7.13: Diode thermal model

1. Diode junction temperature

$$T_j = P_{T,diode} \cdot R_{th,diode} + T_a \tag{7.106}$$

2. Diode Total thermal resistance

$$R_{th,diode} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \tag{7.107}$$

3. Diode Transient thermal impedance

$$Z_{th,diode} = \sum_{i=1}^{n} R_{th(j-c),i}(1 - e^{\frac{-t}{\tau_i}}) \tag{7.108}$$

7.4.4 LC tank

Table 7.17: LC tank loss model

i_{out}	- output DC current
Z_c	- LC tank characteristic impedance
$Q_{s,max}$	- LC tank max. acc. quality factor
R_{LC}	- LC tank equivalent resistance
$P_{LC,tank}$	- LC tank losses

1. Calculate tank equivalent resistance

$$Q_{s,max} = 200 \tag{7.109}$$

$$R_{LC} = \frac{Z_c}{Q_{s,max}} \tag{7.110}$$

2. Calculate LC tank average losses

$$P_{LC,tank} = R_{LC} \cdot i_{out}^2 \tag{7.111}$$

Table 7.18: DC Link capacitors loss model

ESR_{in}	- equivalent series resistance of input dc link
ESR_{out}	- equivalent series resistance of output dc link
i_{in}	- input dc link current
i_{out}	- output dc link current
$P_{cap,in}$	- input dc link losses
$P_{cap,out}$	- output dc link losses
$K_{r,in}$	- input dc link current ripple
$K_{r,out}$	- output dc link current ripple

7.4.5 DC Link capacitors

1. Calculate inverter side DC Link losses

$$P_{cap,in} = ESR_{in} \cdot K_{r,in} \cdot i_{in}^2 \tag{7.112}$$

2. Calculate rectifier side DC Link losses

$$P_{cap,out} = ESR_{out} \cdot K_{r,out} \cdot i_{out}^2 \tag{7.113}$$

7.5 Sub-systems volume and mass

7.5.1 Inverter

Table 7.19: Inverter volume parameters

P_n	- Nominal power
$\rho_{inv,max}$	- Max. acc. power density
V_{inv}	- inverter volume
m_{inv}	- inverter mass
ρ_{mass}	- inverter mass density

1. Select minimum power density, based on commercial solution, $\rho_{inv,max}$

Power density is selected based on commercial solutions [133].

$$\rho_{inv,max} \; \epsilon \; [10...20] \; kW/dm^3 \tag{7.114}$$

2. Calculate total inverter volume and mass

$$V_{inv} = \frac{P_n}{\rho_{inv,max}} \tag{7.115}$$

$$m_{inv} = \rho_{mass} \cdot V_{inv} \tag{7.116}$$

7.5.2 Transformer

Table 7.20: Transformer volume and mass parameters

D_{ins}	- Insulation distance between primary and secondary winding
$D_{ins,p}$	- Primary winding clearance distance to core
$D_{ins,s}$	- Secondary winding clearance distance to core
V_{ins}	- Rated insulation voltage
λ	- safe margin parameter
E_{ins}	- Dielectric strength of the insulation material
X	- Core window height
Y	- Core window width
W	- Core ribbon widht
$T2$	- Core build
A	- Core area
ρ_{Fe}	- Core density
ρ_{Cu}	- Winding density
σ_{Cu}	- Copper conductivity
μ_{Cu}	- Copper permeability
$N_{p,layer}$	- Primary winding layers
$N_{s,layer}$	- Secondary winding layers
$N_{p,turns-layer}$	- Primary winding turns per layer
$N_{s,turns-layer}$	- Secondary winding turns per layer
H_p	- Primary winding height
H_s	- Secondary winding height
$H_s, layer$	- Secondary winding layer height
$I_{ns,p}$	- Primary winding insulation width
$I_{ns,s}$	- Secondary winding insulation widht
D_p	- Primary winding thickness
D_s	- Secondary winding thickness
$I_{rms,p}$	- Primary winding rms current
J	- Winding current density
W_p	- Primary winding width
W_s	- Secondary winding width
L_{ext}	- Exterior magnetic path
L_{int}	- Interior magnetic path
L_e	- Mean magnetic path
V_{core}	- Absolut core volume
V_{window}	- Window volume
V_{Fe}	- Core volume
m_{Fe}	- Core weight
V_p	- Primary winding volume
V_s	- Secondary winding volume
V_{cu}	- Total winding volume
$M_{cu,p}$, $M_{cu,s}$, M_{cu}	- Primary winding, secondary winding, total windings weight
M_{total}	- Total transformer weight, without oil

1. Insulation distance between primary and secondary winding

$$D_{ins} = \frac{V_{ins}}{\lambda \cdot E_{ins}} \tag{7.117}$$

2. Primary winding clearance to core

$$D_{ins,p} = D_{ins} \tag{7.118}$$

3. Secondary winding clearance to core

$$D_{ins,s} = D_{ins} \tag{7.119}$$

4. Initial dimensions based on Hitachi core data sheet

.
Following variables are required: X, $T2$, W, A_c, ρ_{Fe}, ρ_{Cu}, σ_{Cu}, μ_{Cu}.

5. Primary winding dimension

$$\begin{aligned}
N_{p,layer} &= N_p && (7.120)\\
N_{p,turns-layer} &= \frac{N_{p,layer}}{N_p} && (7.121)\\
H_p &= X - 2 \cdot D_{ins} && (7.122)\\
D_p &= \frac{I_{rms,p}}{J \cdot H_p} && (7.123)\\
I_{ns,p} &= 0.1 \cdot D_p && (7.124)\\
W_p &= N_{p,layer} \cdot (D_p + I_{ns,p}) && (7.125)\\
& && (7.126)
\end{aligned}$$

6. Secondary winding dimension

$$\begin{aligned}
H_s &= H_p && (7.127)\\
N_{s,layer} &= N_{p,layer} && (7.128)\\
N_{s,turns-layer} &= \frac{N_s}{N_{s,layer}} && (7.129)\\
H_{s,layer} &= \frac{H_s}{N_{s,turns-layer}} && (7.130)\\
D_s &= D_p && (7.131)\\
I_{ns,s} &= 0.1 \cdot D_s && (7.132)\\
W_s &= N_{s,layer} \cdot (D_s + I_{ns,s}) && (7.133)\\
& && (7.134)
\end{aligned}$$

7. Window area

$$\begin{aligned}
Y &= 2 \cdot (D_{ins,p} + W_p + D_{ins} + W_s) && (7.135)\\
L_{int} &= 2 \cdot (X + Y) && (7.136)\\
L_{ext} &= 2 \cdot (X + Y + 4 \cdot T_2) && (7.137)\\
L_e &= (L_{int} + L_{ext}) && (7.138)
\end{aligned}$$

8. Core volume and mass

$$\begin{aligned} V_{core} &= (X + 2 \cdot T_2) \cdot (Y + 2 \cdot T2) \cdot W && (7.139)\\ V_{window} &= X \cdot Y \cdot W && (7.140)\\ V_{Fe} &= V_{core} - V_{window} && (7.141)\\ M_{Fe} &= V_{Fe} \cdot \rho_{Fe} && (7.142) \end{aligned}$$

9. Primary winding volume and mass

$$\begin{aligned} V_{p1} &= H_p \cdot (T_2 + 2 \cdot D_{ins} + 2 \cdot W_p) \cdot (W + 2 \cdot D_{ins} + 2 \cdot W_p) && (7.143)\\ V_{p2} &= H_p \cdot (T_2 + 2 \cdot D_{ins}) \cdot (W + 2 \cdot D_{ins}); && (7.144)\\ V_p &= 2 \cdot (V_{p1} - V_{p2}); && (7.145)\\ M_{cu,p} &= V_p \cdot \rho_{cu}; && (7.146) \end{aligned}$$

10. Secondary winding volume and mass

$$\begin{aligned} V_{s1} = H_s \cdot (T_2 + 2 \cdot D_{ins} + 2 \cdot W_p + 2 \cdot D_{ins} + 2 \cdot W_s) \\ \cdot (W + 2 \cdot D_{ins} + 2 \cdot W_p + 2 \cdot D_{ins} + 2 \cdot W_s) \end{aligned} \quad (7.147)$$

$$V_{s2} = H_s \cdot (T_2 + 2 \cdot D_{ins} + 2 \cdot W_p + 2 \cdot D_{ins}) \cdot (W + 2 \cdot D_{ins} + 2 \cdot W_p + 2 \cdot D_{ins}) \quad (7.148)$$

$$\begin{aligned} V_s &= 2 \cdot (V_{s1} - V_{s2}); && (7.149)\\ M_{cu,s} &= V_s \cdot \rho_{cu}; && (7.150) \end{aligned}$$

11. Total transformer volume and mass

$$\begin{aligned} V_{cu} &= V_p + V_s && (7.151)\\ M_{cu} &= M_{cu,p} + M_{cu,s} && (7.152)\\ M_{total} &= M_{Fe} + M_{Cu} && (7.153) \end{aligned}$$

7.5.3 Rectifier

1. Select minimum power density, based on commercial solution, $\rho_{inv,max}$

$$\rho_{r,max} \, \epsilon \, [10...20] \; kW/dm^3 \quad (7.154)$$

Table 7.21: Rectifier volume and mass parameters

P_n	- Nominal power
$\rho_{r,max}$	- Max. acc. power density
V_r	- rectifier volume
m_r	- rectifier mass
ρ_{mass}	- rectifier mass density

2. Calculate total rectifier volume and mass

$$V_r = \frac{P_n}{\rho_{r,max}} \tag{7.155}$$

$$m_r = \rho_{mass} \cdot V_r \tag{7.156}$$

7.5.4 LC tank - resonant capacitor volume and mass

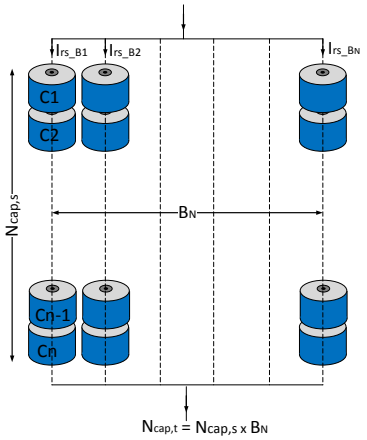


Fig. 7.14: Resonant capacitor volume estimation

1. Select volume utilization factor K_u

2. Select unit capacitor parameters

- Capacitance : C_1
- Rated DC voltage : V_{C1}
- Rated AC current : I_{rmsC1}

3. Calculate unit capacitor volume

$$Vol_{C1} = H_{C1} \cdot A_{C1} \tag{7.157}$$

Table 7.22: Resonant capacitor bank volume and mass parameters

C_1	- sub-unit capacitor
C_R	- resonant capacitor
V_{C1}	- Max. sub-unit capacitor voltage
V_{Cr}	- Max. acc. resonant capacitor voltage
I_{rmsC1}	- Max. sub-unit capacitor rms current
I_{rmsnom}	- Max. resonant rms current
K_u	- utilization factor
Vol_{Cr}	- Resonant capacitor volume
m_{Cr}	- Resonant capacitor mass
Vol_{C1}	- Sub-unit capacitor volume
B_N	- Number of capacitor branches
B_{Cap}	- Branch capacitance
$N_{cap,s}$	- Number of series capacitors per branch
$N_{cap,t}$	- Total number of capacitors

4. Calculate number of branches

$$B_N = \frac{I_{rms,nom}}{I_{rmsC1}} \tag{7.158}$$

5. Calculate branch capacitance

$$B_{Cap} = \frac{C_r}{B_N} \tag{7.159}$$

6. Calculate no. of capacitors per branch

$$N_{cap,s} = \frac{C_1}{B_{Cap}} \tag{7.160}$$

7. Verify voltage condition

$$V_{C1} \geq \frac{V_{Cr,max}}{N_{caps,s}} \tag{7.161}$$

8. Calculate total number of capacitors

$$N_{cap,t} = N_{cap,s} \cdot B_N \tag{7.162}$$

9. Calculate total active volume and mass

$$Vol_{Cr} = N_{cap,t} \cdot Vol_{C1} \tag{7.163}$$

$$M_{Cr} = \rho_{Cr} \cdot Vol_{Cr} \tag{7.164}$$

7.5.5 DC Link capacitors

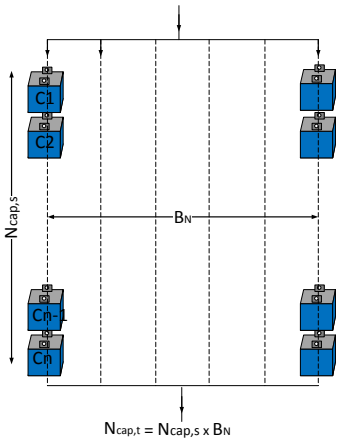


Fig. 7.15: DC Link capacitors volume estimation

Table 7.23: DC Link capacitors volume and mass parameters

C_1	- sub-unit capacitor
C_{out}	- output dc-link capacitor
V_{C1}	- Max. sub-unit capacitor voltage
I_{rmsC1}	- Max. sub-unit capacitor rms current
V_{outnom}	- output DC voltage
K_u	- utilization factor
Vol_{Cout}	- Output capacitor volume
m_{Cout}	- Output capacitor mass
Vol_{C1}	- Sub-unit capacitor volume
B_N	- Number of capacitor branches
B_{Cap}	- Branch capacitance
$N_{cap,s}$	- Number of series capacitors per branch
$N_{cap,t}$	- Total number of capacitors

1. Select volume utilization factor K_u

2. Select unit capacitor parameters

- Capacitance : C_1
- Rated DC voltage : V_{C1}
- Rated AC current : I_{rmsC1}

3. Calculate unit capacitor volume

$$Vol_{C1} = H_{C1} \cdot A_{C1} \tag{7.165}$$

4. Calculate no. of series capacitors

$$N_{cap,s} = \frac{V_{out}}{V_{C1}} \tag{7.166}$$

5. Calculate branch capacitance

$$B_{cap} = \frac{C_1}{N_{cap,s}} \tag{7.167}$$

6. Calculate no. of branches

$$B_N = \frac{C_{out}}{B_{cap}} \tag{7.168}$$

7. Calculate total number of capacitors

$$N_{cap,t} = N_{cap,s} \cdot B_N \tag{7.169}$$

10. Calculate total active volume and mass

$$Vol_{Cout} = N_{cap,t} \cdot Vol_{C1} \tag{7.170}$$

$$M_{Cout} = \rho_{Cout} \cdot Vol_{Cout} \tag{7.171}$$

7.6 10MW Design example

Table 7.24: Input specifications

Symbol	Parameter	Value	Unit
P_{in}	- Nominal power	10.0	MW
$P_{in,max}$	- Nominal max. acc. power	11.0	MW
V_{in}	- Input DC Voltage	±2.0	kV
$V_{in,max}$	- Input max. acc. DC Voltage	±2.2	kV
$V_{in,min}$	- Input min. acc. DC Voltage	±1.8	kV
V_{out}	- Output DC Voltage	±50.0	kV
$V_{out,max}$	- Output max. acc. DC Voltage	±55.0	kV
$V_{out,min}$	- Output min. acc. DC Voltage	±45.0	kV
η	- Min. acc. efficiency	98.5	%
ρ	- Min. acc. power density	10.0	kW/L

Using the proposed converter design guide line, a 10 MW design example is provided in the following tables as presented in [125]. Converter input

Table 7.25: Main circuit design parameters

Symbol	Parameter	Value	Unit
F_{sw}	- switching frequency	0 - 1000	Hz
F_r	- resonant frequency	1140	Hz
C_r	- resonant capacitor	0.250	uF
L_r	- resonant inductor	78.0	mH
$L_{m,max}$	- max. acc. magnetizing inductance	10.0	mH
$L_{lk,max}$	- max. acc. secondary leakage ind.	1.25	%
$i_{m,max}$	- max. acc. mag. current	5	%
i_{in}	- input DC. current	2.5	kA
$i_{rp,pk}$	- primary side peak current	4.9	kA
i_{out}	- output DC. current	0.1	kA
$i_{rs,pk}$	- secondary side peak current	0.2	kA
$V_{Cr,pk}$	- res. capacitor peak voltage	100	kV

Table 7.26: Inverter

Symbol	Parameter	Value	Unit
	- Semiconductor type	IGBT	-
	- Code	FZ750R65KE3	-
	- Packaging type	Power module	-
	- Cooling type	Water cooling	-
K_u	- utilization factor	60	%
V_{CES}	- Collector emitter voltage	6500	V
I_{CNOM}	- Continuous DC collector current	750	A
I_{CRM}	- Repetitive peak collector current	1500	A
ρ_{inv}	- Power density inverter	23	kW/L
$T_{j,IGBT}$	- Junction temperature	125	$^{\circ}C$
N_{IGBT}	- Number of IGBTs	12	-
$N_{parallel}$	- Number of parallel inverters	3	-
P_{IGBT}	- Total loss per IGBT	2250	W
P_{inv}	- Total loss per inverters	27000	W
$R_{th,igbt}$	- Total igbt thermal resistance	0.037	$^{\circ}C/W$
Vol_{inv}	- Total inverter volume	0.42	m^3
M_{inv}	- Total inverter mass	-	-

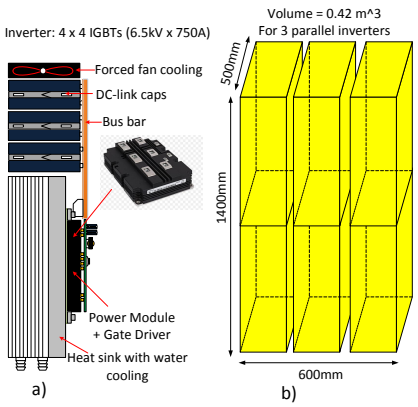


Fig. 7.16: Inverter power stacks. [125]

specifications are shown in Table. 7.24 and the main circuit design parameters are shown in Table. 7.25.

The inverter ratings, losses and volume are presented in Table. 7.26. Considering an utilization of 60% on the IGBTs, 3 paralell full bridge inverters are suggested with a total volume of 0.42 m^3.

Medium frequency transformer design aspects are presented in Table. 7.27 and the conceptual drawing in Fig. 7.17. The transformer is designed for a F_{sw} = 1000Hz.

Table 7.27: Transformer

Symbol	Parameter	Value	Unit
B_{max}	- Flux density	1.5	T
X	- Core window height	1	m
Y	- Core window width	0.19	m
T_2	- Core build	0.16	m
W	- Core ribbon width	0.213	m
L_{ag}	- Max. acc. air gap	1	mm
μ_r	- Core Rel. permeability	1000	$N \cdot A^{-2}$
N	- Turns ratio	25	-
N_p	- Primary turns	20	-
$N_{p,layer}$	- Primary wind. no. layers	20	-
$N_{pturn,layer}$	- Primary wind. no. turns per layer	1	-
D_p	Foil thickness	1	mm
N_s	Secondary turns	500	-
$N_{s,layer}$	- Secondary wind. no. layers	20	-
$N_{sturn,layer}$	- Secondary wind. no. turns per layer	25	-
D_s	- Foil thickness	1	mm
L_m	- Mag.inductance	10	mH
L_{lk}	- Leakage inductance reflec. on secondary side	78	mH
$T_{j,core}$	- Core max. temp.	-	-
$T_{j,p}$	- Primary wind. max. temp	-	-
$T_{j,s}$	- Secondary wind. max. temp	-	-
V_{Fe}	- Core volume	0.1	m^3
V_{cu}	- Windings volume	0.042	m^3
m_{Fe}	- Core mass	800	kg
m_{cu}	- Windings mass	380	kg
P_{core}	- Core losses	15000	W
P_p	- Primary winding loss	5000	W
P_s	- Secondary winding loss	5000	W

The medium voltage rectifier is implemented in a full bridge configuration with series connected diodes. Conceptual drawing of one diode valve is shown in Fig. 7.19. Rectifier design aspects, including volume, losses, number of series connected diodes and snubber components are shown in Table. 7.28

As explained in the main design guide line, the objective is to include the resonant inductor as part of the transformers own leakage inductance, by manipulating the distance between primary and secondary windings. In this manner, the focus can be only on implementing the resonant capacitor tank. Fig. 7.20 shows how based on a pre-selected sub-unit, the tank could be assembled and it's ratings, losses and volume are shwon in Table. 7.29.

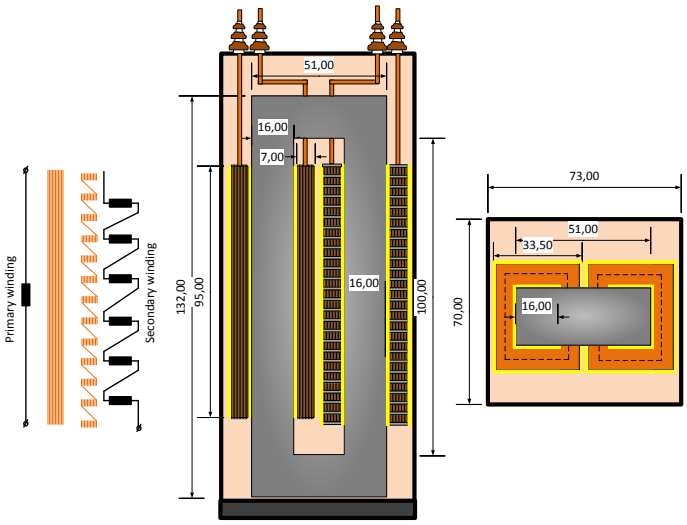


Fig. 7.17: Conceptual drawing of transformer with passive circulation of oil

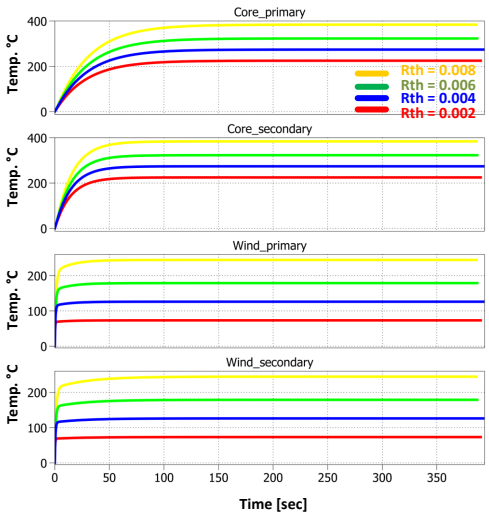


Fig. 7.18: Transformer core and windings temp. for different cooling thermal impedance

Table 7.28: Rectifier

Symbol	Parameter	Value	Unit
T_{rec}	- Reverse recovery time	60	s
$T_{j,diode}$	- Diode junction temperature	125	°C
ρ_r	- Rectifier power density	13.7	kW/L
V_{RRM}	- Repetitive peak reverse voltage	6500	V
I_{favm}	- Average on-state current	750	A
I_{fsm}	- Diode surge current	12500	A
Q_{rr}	- recovered charge	6.0	mC
ΔQ_{rr}	- Stored charge max.variation	1.0	%
Δi_{rm}	- Diode max. spread in leak.current	50	mA
K_a	- Valve arrester util. factor	1	1
K_d	- Uneven voltage distribution factor	1	-
K_u	- Diode voltage utilization factor	0.6	-
K_R	- Redundancy factor	1.025	-
R	- Grading resistor	50	$k\Omega$
C	- Snubber capacitor	10	nF
V_{TOV}	- Max. valve blocking voltage	140	kV
N_d	- Number of diodes per arm	40	-
$P_{T,diode}$	- Total diode loss	105	W
$P_{T,r}$	- Total rectifier loss	16800	W
$R_{th,diode}$	- Total diode thermal resistance	0.78	°C/W
V_r	- Total rectifier volume	0.73	m^3
m_r	- Total rectifier mass	-	-

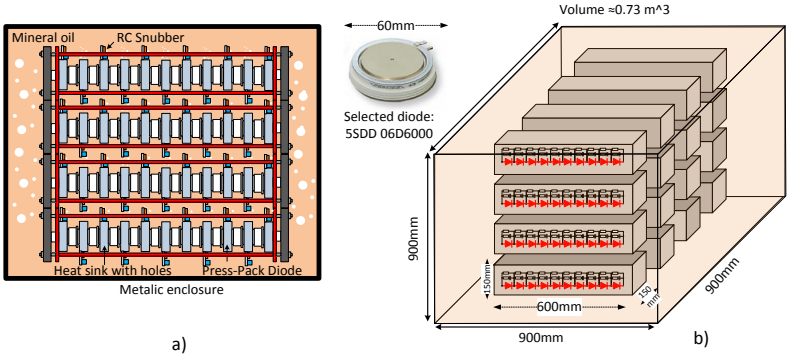


Fig. 7.19: Diode valve conceptual drawing. [125]

The sub-unit element is a metallized polypropylene capacitor, filled with dry resin.

A conceptul drawing of the output dc-link bank, assembled in a similar fashion as the resonant capacitor bank is illustrated in Fig. 7.21, with the calculated volume, losses and ratings shown in Table: 7.30. For input side, medium voltage electrolytic capacitors are selected, while for the output side, metallized polypropylene capacitors are suggested.

Table 7.29: LC tank

Symbol	Parameter	Value	Unit
Q_s	Quality factor	100	-
$L_r{}'$	Updated resonant inductor	0	mH
R_{LC}	Equivalent LC tank DC series resistance	10	$m\Omega$
$P_{LC,tank}$	LC tank losses	28000	W
C_1	Sub unit capacitance	15	uF
V_{C1}	Max. sub-unit cap. voltage	2200	V
$I_{rms,C1}$	Max. sub-unit cap. rms current	45	A
$K_{u,res}$	Utilization factor	1	-
Vol_{Cr}	Resonant capacitor bank volume	0.1	m^3
$N_{cap,t}$	Total number of capacitors	240	-
$E_{cap,res}$	-	-	-

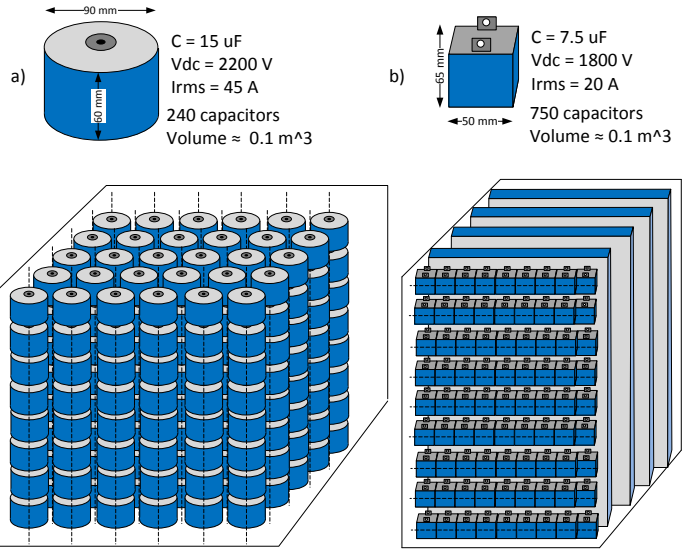


Fig. 7.20: Resonant capacitor bank. [125]

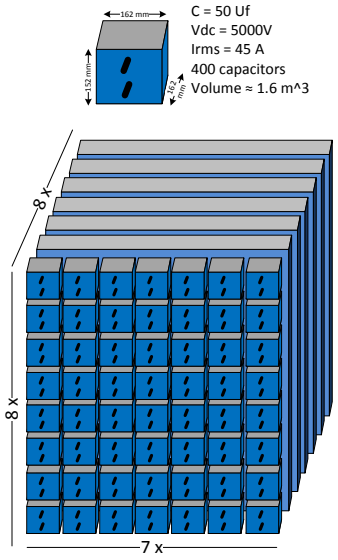


Fig. 7.21: Output dc link bank. [125]

Table 7.30: DC-link capacitors

Symbol	Parameter	Value	Unit
k_{u,dc_link}	Utilization factor	1	
$k_{r,v}$	Voltage ripple factor	1	%
$k_{r,i}$	Current ripple factor	1	%
τ	Output dc link time constant	25	ms
C_{in}	Input dc-link capacitance	30	mF
C_{out}	Output dc-link capacitnace	50	uF
ESR_{in}	Equiv.series resistance input dc-link	-	$m\Omega$
ESR_{out}	Equiv.series resistance output dc-link	-	$m\Omega$
$P_{cap,in}$	Power losses input dc-link	-	-
$P_{cap,out}$	Power losses output dc-linl	-	-
C_1	Output dc-link sub-unit capacitance	50	uF
V_{C1}	Output dc-link sub-unit capacitance voltage	5000	V
$I_{rms,C1}$	Output dc-link sub-unit capacitance rms current	45	A
Vol_{Cout}	Output dc-link capacitance volume	1.6	m^3
m_{Cout}	Output dc-link capacitance mass	-	-
$N_{cap,t}$	Total number of capacitors	400	-

7.7 Conclusions

A step by step design guide line methodology for SRC# has been introduced and detailed. The proposed range of validity of the guide line is for $P_n \ \epsilon$ $(5-10)$ MW, $V_{in} \ \epsilon \ \pm(0.5-8.0)$ kV, $V_{in} \ \epsilon \ \pm(35-50)$ kV and $F_{sw} \ \epsilon \ \pm(0.5-5.0)$ kHz. Selection of upper switching frequency of 5 kHz is due to challenges in designing the medium frequency transformer and heat evacuations, in addi-

tion o increased recovery losses on the line frequency diodes. In the end, a 10 MW design example is illustrated with commercially available technologies. To fulfill another objective of the thesis, the buil-up and testing of one proof of concept, that was arranged following the proposed design guide and validation of the semiconductor loss model are performed in two different medium voltage setups, discussed in the following chapter.

Chapter 8

Experimental work

Summary

A series of experiments has been performed during this project. Descriptions of the setups and verification method is illustrated in this chapter and is based on [125], [146]

One of the experiment was designed for 10 kW, 500V to 5000V and was performed for preliminary semiconductor loss model validation and rectifier diode voltage balancing. Another experiment performed soft-switching characterization of the target 6.5 kV IGBTs and Diodes on a setup that did not require bulky loads and sources.

8.1 Proof of concept: 10 kW SRC#

Experimental setup

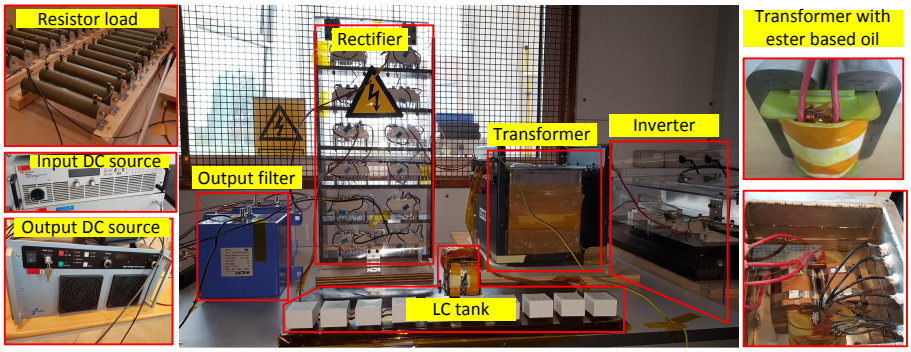


Fig. 8.1: Scaled proof of concept: experimental setup for SRC#. [125]

In order to evaluate the validity of the loss model, a scaled 10 kW prototype was built with specifications as shown in Table 4.5. The hypothesis was that if the 10 kW loss model (built in *Plecs*) is able to predict the scaled setup losses with low error, then there is higher confidence it will predict the losses also for the target 10 MW converter. The experimental circuit is pictured in Fig. 8.1 and it's diagram in Fig. 8.2. The medium frequency transformer is designed for a maximum switching frequency of 1000 Hz and a turns ratio of 1:10. The rectifier is assembled with 24 line frequency diodes, connected in series, each having a parallel RC circuit for voltage balancing. Resonant capacitor bank consists of 10 series connected thin film capacitors, while the resonant inductor was built around an amorphous core with round wires. Output dc link consists of metallized polypropylene capacitors, while on input side electrolytic capacitors are employed. For this study, the setup was

operated in open loop control up to 1.0 pu of nominal power. On the rectifier side, in order to emulate a medium voltage network, a 5 kV DC source is connected to a resistor load through three series connected diodes.

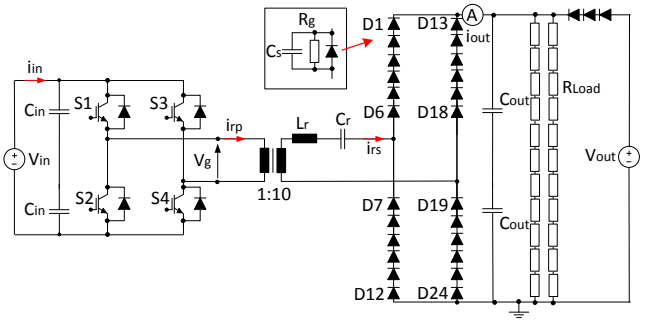


Fig. 8.2: Scaled proof of concept: experiment diagram. [125]

Table 8.1: Experimental SRC# Parameters

Parameter	Value
Input voltage - V_{in}	500 V
Output voltage - V_{out}	5000 V
Nominal power - P_n	10 kW
Resonant inductor - L_r	182 mH
Magnetizing inductance - L_m	10mH
Secondary Leakage inductance - L'_{Lk}	12.5 mH
Resonant capacitor C_r	0.1 uF
Snubber capacitor C_s	1.0 nF
Grading resistor R_g	300 kΩ
Load resistors R_{load}	2585 Ω
Primary resistance R_p	0.1 Ω
Secondary resistance R_s	5.0 Ω
Turns ratio N	1:10
Inverter IGBT	4 x SKM150GAR12T4
Rectifier diode	24 x SKKD16/46
Transformer core	4 x AMCC250-Metglas 2605
Windings type	Copper foil
Insulating material	Kepton tape and ester based oil

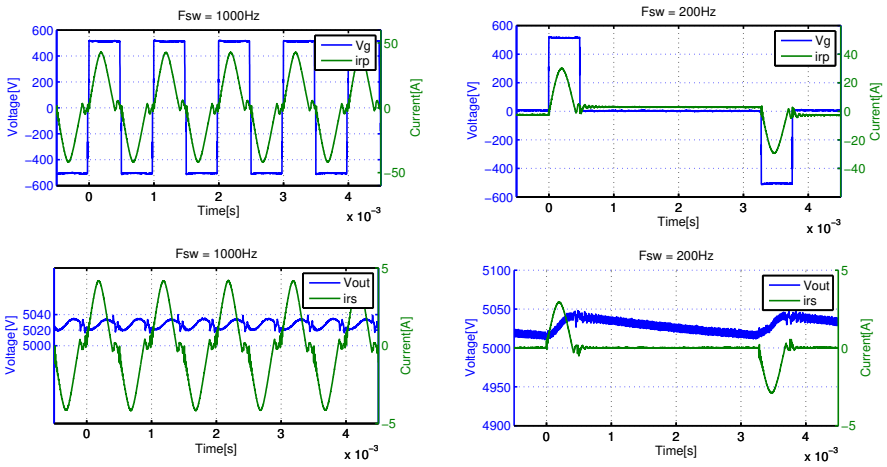


Fig. 8.3: SRC# characteristic waveforms at 1000Hz and 200Hz: inverter voltage V_g, out voltage V_{out}, primary resonant current i_{rp} and secondary resonant current i_{rs}. [125]

8.1.1 Characteristic waveforms

The principal characteristic waveforms for the experimental SRC# are presented in Fig. 8.3 for two different frequencies, corresponding to 1.0 pu and 0.2 pu of maximum switching frequency. As pulse removal technique is implemented, the distance between applied voltage pulses decreases with frequency, ensuring that the magnetizing current i_m stays constant during the zero voltage periods. Comparing the waveforms of primary and secondary currents, it's noticed that the only differences lay in the scaling factor and addition of magnetizing current on primary side. Another noticeable difference is that at lower frequency, the peak resonant current decreases as compared to higher frequency.

8.1.2 Devices waveforms

In order to understand how pulse removable technique is implemented, inverter and rectifer side devices waveforms are presented in Fig. 8.4 and Fig. 8.5.

Inverter IGBTs

Principle device waveforms for switches S1 and S4 are shown in Fig. 8.4, for 1000 Hz and 500 Hz, while for S2 and S3 they are symmetrical. As expected, both devices are experiencing ZVS at turn-on and a low current at turn-off. It's noticed how the delay between S1 and S4 turn-on is increasing at lower

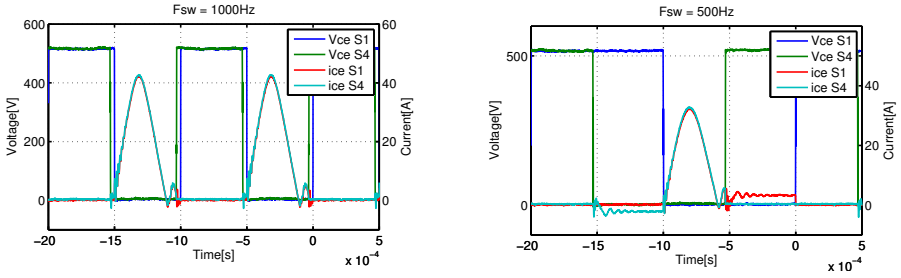


Fig. 8.4: S1 and S4 collector-emitter voltage and current at 1000 Hz and 500 Hz. [125]

frequencies. One big difference consists in longer conduction duration of the magnetizing current for S1. The same current will flow through D3 during positive intervals and S2, D4 pair during negative intervals. An important aspect is that the ratio between peak resonant current and magnetizing current has to be kept high, preferably above 10, in order to limit conduction and turn-off losses.

Rectifier diodes

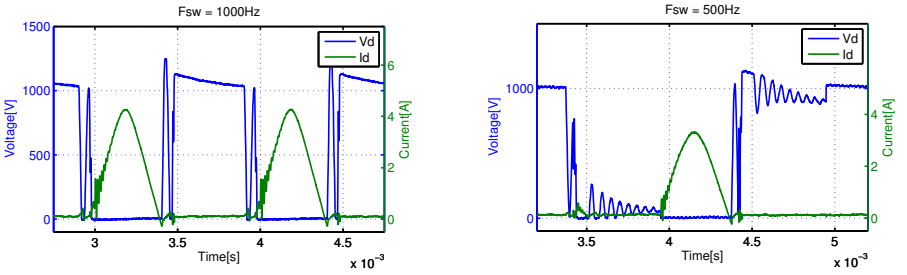


Fig. 8.5: Rectifier diode forward voltage V_d and current I_d. [125]

Characteristic diode waveforms are shown in Fig. 8.5 for 1000 Hz and 500 Hz. Each diode from the series connection chain will experience ZVS at turn-on and a low reverse recovery loss. The parallel RC circuit will cause on the other hand oscillations on V_d, but will not impact conduction losses.

8.1.3 Loss measurements

Total losses of the 10 kW prototype have been evaluated and presented in Fig. 8.6(a) and they range from $\approx$ 6% at 0.15 pu down to $\approx$ 4.5% at 0.15 pu of P_n. Looking at figures Fig. 8.6(b) and (c) it is noticed that the measured losses correspond with the simulated results.

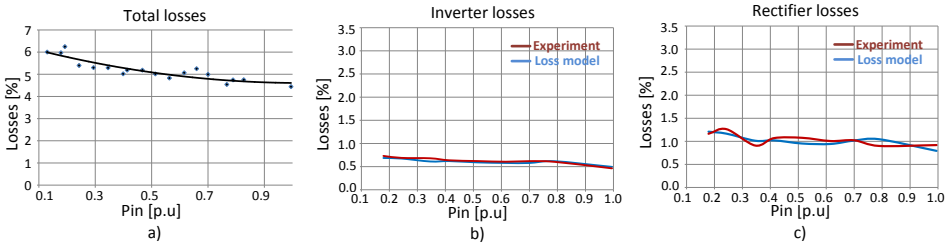


Fig. 8.6: Measured total losses (a); inverter losses (b); rectifier losses (c).

8.1.4 Loss segregation

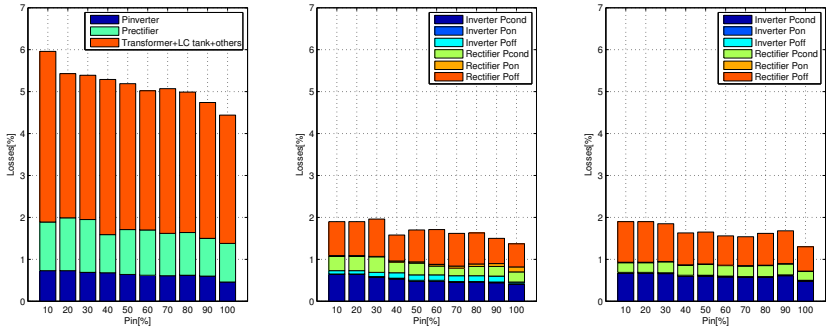


Fig. 8.7: Loss segregation of measured losses (a); loss segregation on measured (b) and simulated (c) semiconductor losses. [125]

After measuring the total losses, a segregation was performed and results shown in Fig. 8.7(a). It's noticed that the semiconductor losses are rather flat in the whole operating range. This was expected mainly because the turn-on and off energy losses are the same, regardless of switching frequency and should have the same percentage share. On the other hand, the remaining losses are not possible to segregate at this power level as no test facility was available for this (calorimeter setup or similar). Comparing figures Fig. 8.7(b) and (c), it's possible to understand why the experimental results match with the semiconductor loss models. It's should be noted that the measured results are also susceptible to errors due to voltage and current probes accuracy, ranging up to $\pm 2\%$ of reading.

8.1.5 Closed loop control

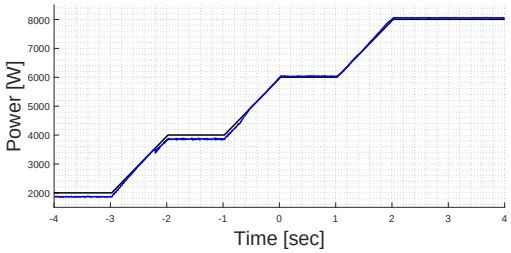
In Fig. 8.8a and b, power sweeps from 0.2 pu up to 0.8 pu are performed with two different control architectures, as described in Chapter 5. First controller

is based only on a feedforward controller (FF), built on linearized power to frequency equations, while the second architecture (FF+GSC) incorporates a gain scheduled PI controller that compensates for the error of the feedforward. The interesting aspect is that the FF controller starts to introduce a steady state error in the lower operating region (0.2 to 0.3) as the model is built based on empirical data and the effect of non-idealties is not included. To compensate for this, the help of the gain-scheduled PI is now clearly observed in Fig. 8.8b, where the steady state error is close to 0.1

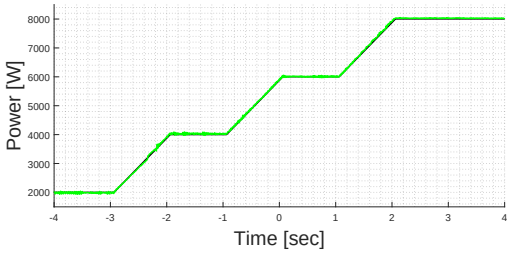
Power steps from 0.25 pu to 0.3 pu are observed in Fig. 8.8c, while steps from 0.8 pu to 0.85 pu are recorded in Fig. 8.8d. It needs to be mentioned that the recorded output power for these tests is the averaged measured power and the tests were performed withouth any output chocke inductor, otherwise the first order response of the filter would have been recorded, thus covering the natural response of the controllers. As in the power sweep tests, it's observed that in both power steps, the FF controller is reacting fast but it introduced a steady state error of 1-2%. On the other hand, the FF+GSC is reaching the steady state slightly slower then the FF, but the final steady state error is close to 0%.

8.1.6 Discussions

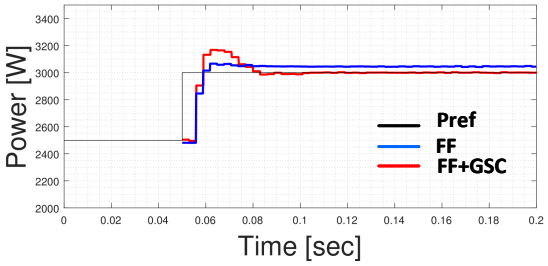
Some important aspects remain to be discussed, such as the relative low efficiency of the experimental demonstrator. First of all, looking only at the semiconductor losses, it's possible to conclude they remain rather constant in proportion to the load. Further on, it is expected that at this specifications, the transformer core losses have a higher percentage of total losses, as initially expected. But, the percentage of these losses should decrease as nominal power specifications will increase in the range of MWs. Next, the chosen semiconductors were only utilized at $\approx 25\%$ of their current ratings, as it was not possible to find single IGBT power modules for the setup specifications. Another topic of discussion is the high value of the resonant inductance, which lead to a rather bulky component. It's expected as the power and voltage level increase, such as 10 MW and 1:10 turns ratio, even a leakage inductance of 1 to 2% would be enough to replace the physical resonant inductor. As noticed in Fig. 8.3, the peak resonant current is lower at lower frequencies. These could be the impact of the RC parallel circuit, winding resistances and the emulated MVDC network.



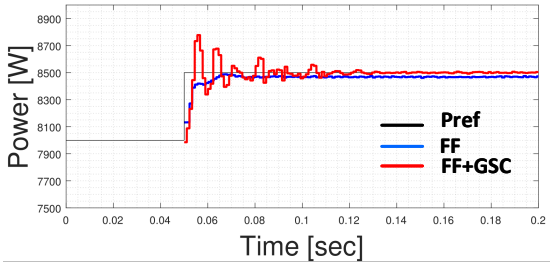
(a) Power sweep from 0.2 pu to 0.8 pu with FF controller.



(b) Power sweep from 0.2 pu to 0.8 pu with FF controller+GSC.



(c) Dynamic response during power step from 0.2 pu to 0.3 pu



(d) Dynamic response during power step from 0.8 pu to 0.85 pu

Fig. 8.8: Experimental waveforms. [128]

8.2 Soft-switching characterization of 6.5 kV IGBTs and diodes

6.5kV IGBT power modules and line frequency press-pack diodes are proposed for the turbine converter. The challenge of characterizing losses in soft-switching semiconductors - without building the full circuit - is overcome by a proposed test circuit and procedure that minimizes cost and complexity, yet subjects the device under test to similar use as in the target application. This sub-chapter is based on the work from [146] and describes the test method and results obtained with it. Semiconductor waveforms at kilovolt and kiloamps levels are recorded and compared with the loss models and preliminary evaluation of total efficiency is given.

8.2.1 Experimental test bench

A medium voltage experimental test bench has been assembled, by following the approach from [120] without the need of expensive dc loads and sources. The experimental diagram is presented in Fig. 8.9, the 1:1 medium frequency transformer in Fig. 8.10 and circuit parameters in Table. 8.2. A medium voltage DC source is used to pre-charge capacitors C_{in} and C_{out}, allowing a voltage difference ΔV between input and output. This particular voltages will determine the peak resonant current flowing from the inverter towards the rectifier.

Table 8.2: Circuit parameters of experimental setup

Parameter	Value
C_{in}	101 uF
C_{out}	106 uF
V_{in}	4000 V
V_{in}	1000-4000 V
L_m	55 mH
L_r	180 uF
C_r	100 uF
R	100 $k\Omega$
E_{pulse}	3000 J
IGBTs	6.5 kV/750A
Diodes	6.5 kV/750A

In [120], the operation of a (6.5kV/500A) IGBT module in a SRC is presented. A test bench (Fig. 8.11a) with novel mode of operation is proposed, which allows the investigation in quasi steady mode of semiconductors at low expense of power supplies. However, the principle of operation is for 1:1

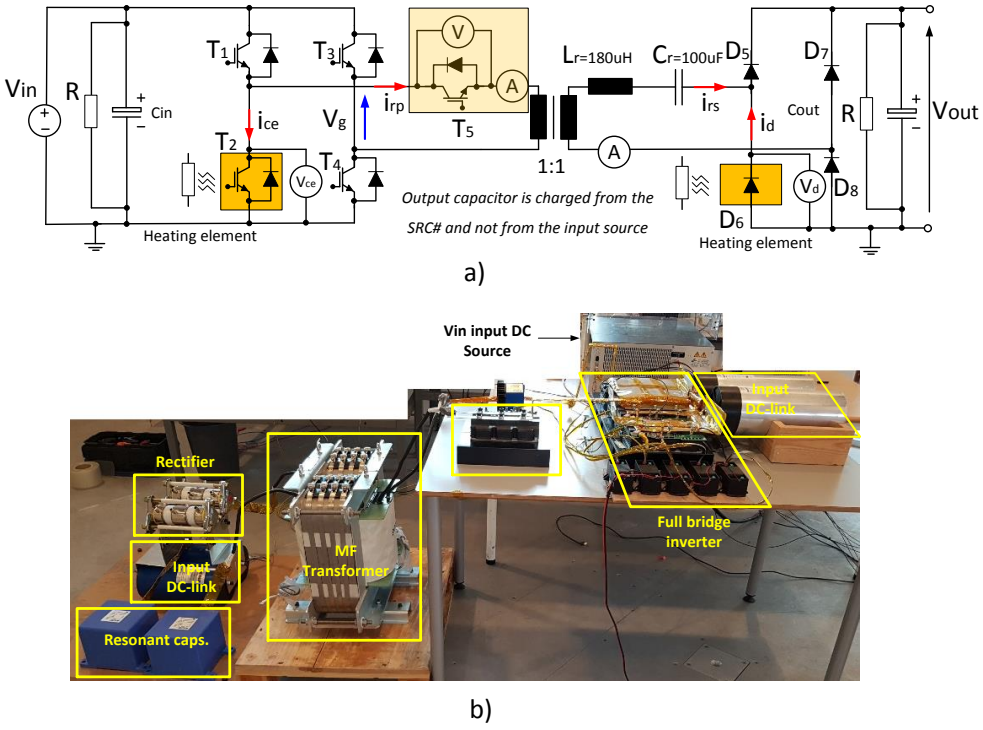


Fig. 8.9: a) Experimental diagram and b) experimental setup [146]

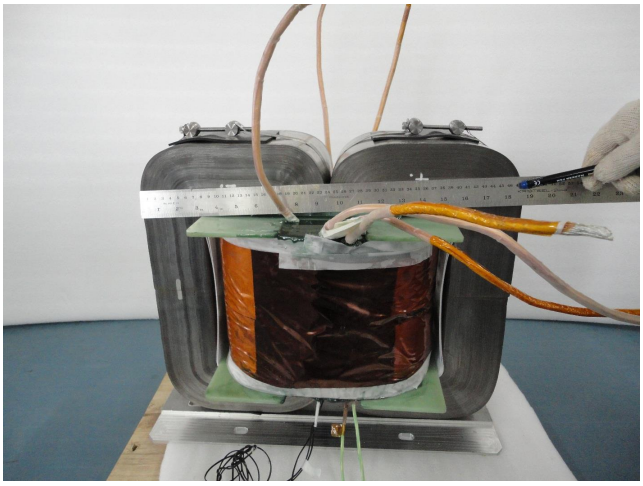


Fig. 8.10: Medium frequency transformer. [146]

topologies. The proposed test bench suggests a principle of operation that could be applied to 1:N topologies and does not use connectors for charging input and output capacitors. Principle waveforms are illustrated in Fig. 8.11b.

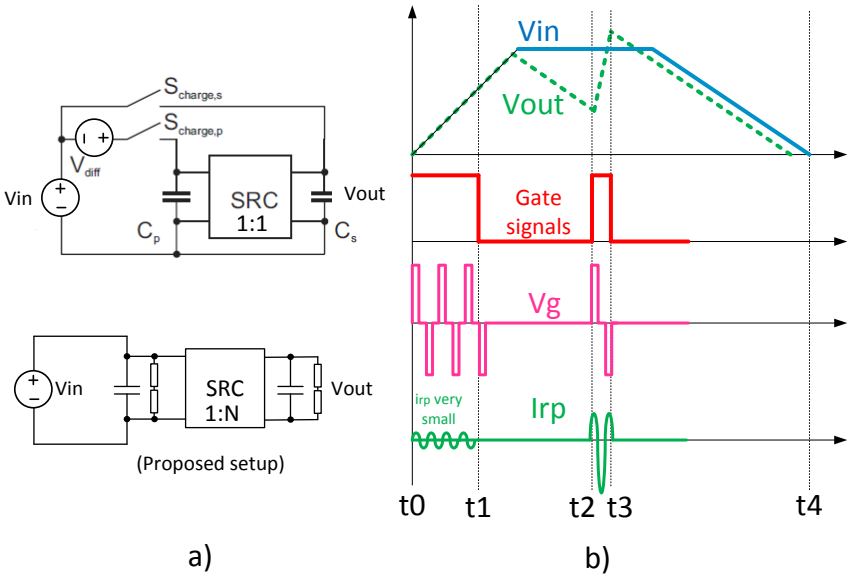


Fig. 8.11: Principle of operation [146]: a) Comparison of [120] setup with proposed setup; b) Characteristic waveforms. [146]

The switches pair T1/T2 and T3/T4 are operated with 50% duty cycle. Commutation of T1/T2 is phase shifted with respect to the conduction of T3/T4, with a duration equal to half of LC tank resonant period, resulting in a quasi-square excitation voltage. At the beginning of each test $t\epsilon[t0 - t1]$, pulses are applied to the igbts, while the input source is slowly charging C_{in}. In the same time, the converter itself is charging output capacitors C_{out}. During the charge up period $V_{in} \approx V_{out}$, meaning a very small sinusoidal resonant current is flowing. In the period $t\epsilon[t1 - t2]$, IGBT pulses are stopped, but V_{in} is still increased, while V_{out} begins to discharge through the parallel connected resistors array, thus achieving a certain between input and output voltages. Considering that this particular voltage difference will determine the maximum peak current, a predetermined number of pulses is applied in the period $t\epsilon[t2 - t3]$. Steady state principle waveforms for different excitation frequencies are shown in Fig. 8.12 and Fig. 8.13, while the characteristic waveforms for one igbt and rectifier diode are further illustrated in Fig. 8.14 and Fig. 8.15

Looking at Fig. 8.14, the same resonant current pulse is obtained for

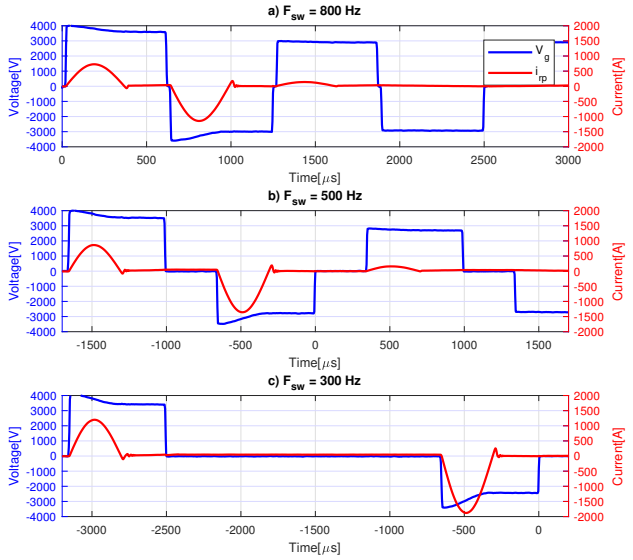


Fig. 8.12: Switching waveforms for: a) F_{sw} =800 Hz , b) F_{sw} =500 Hz and c) F_{sw} =300 Hz. [146]

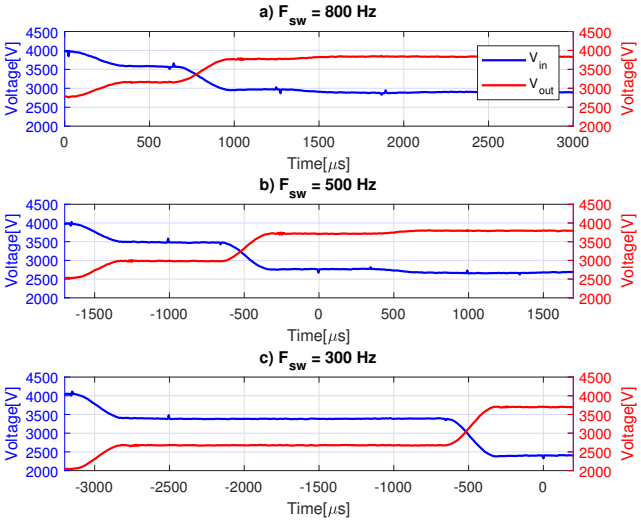


Fig. 8.13: Input and output dc link voltages. Waveforms are synchronized with waveforms from Fig. 8.12. [146]

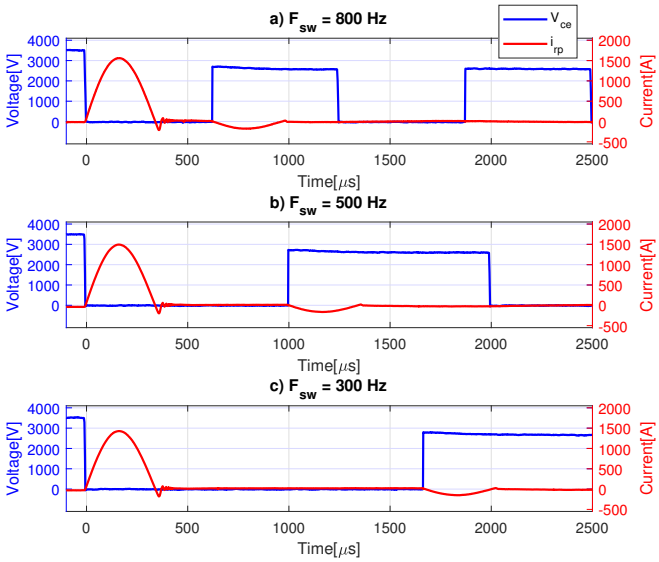


Fig. 8.14: Characteristic waveforms for one IGBT (T2) [146]

different switching frequencies, while the time duration between pulses is changed according to the output power. The recorded current waveform from Fig. 8.14 is the primary resonant current i_{rp}, while in Fig. 8.15 is the secondary resonant current i_{rs}. Coralated with igbt T2 and diode D6 conduction phases, the currents through the devices can be seen. It needs to be mentioned that during conduction phase of T2, when the current changes direction is for the IGBT's antiparallel diode.

8.2.2 Validation of loss model

In [124], an efficiency estimation for a 10 MW converter was performed and predicted a flat efficiency of 98.5% for entire operational range. One of the reasons for such high efficiency, is the ability to operate the inverter and rectifier devices with soft-switching. Thus, two hypothesis need to be demonstrated: (i) IGBT switching losses are decreased to low and very low values as compared to hard-switching topologies, due to ZVS at turn-on and a very low turn-off current; (ii) Due to soft-switching in full operational range and natural commutation, line frequency diodes can be used at elevated frequency. Therefore, it was important to recreate similar voltage and current waveforms on both IGBTs and diodes and compare the measured losses with the loss model. An example of comparison between experimental vs. simu-

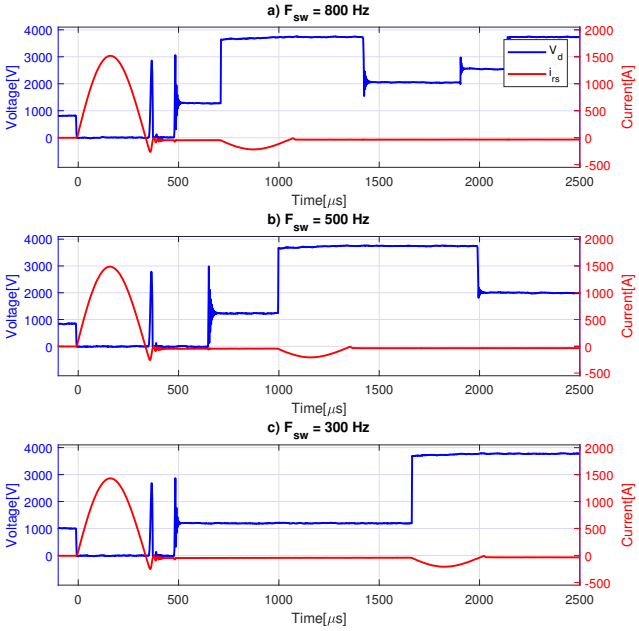


Fig. 8.15: Characteristic waveforms for one IGBT (D6)[146]

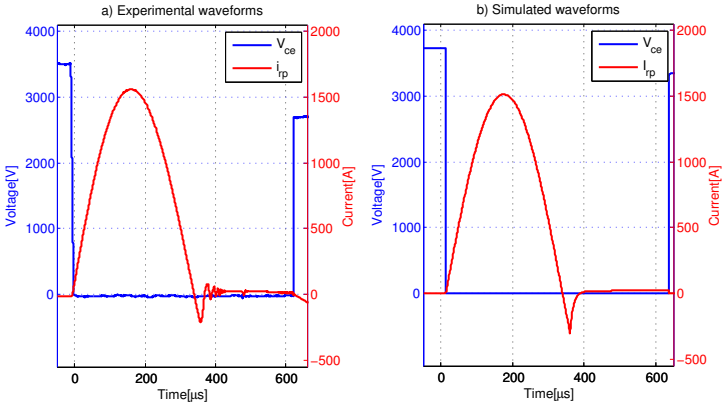


Fig. 8.16: Experimental vs. simulated igbt waveforms [146]

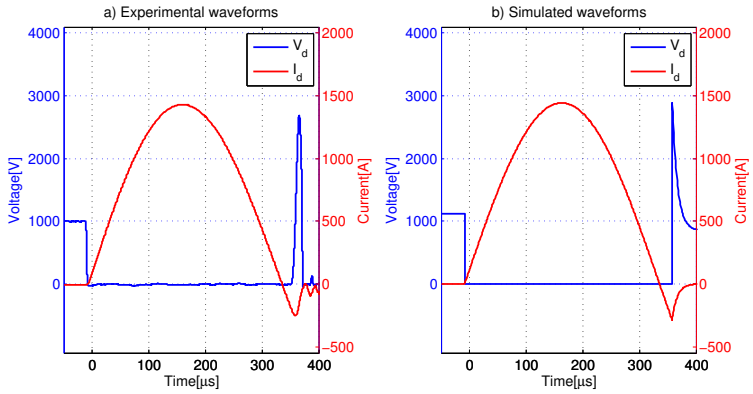


Fig. 8.17: Experimental vs. simulated diode waveforms [146]

lated waveforms are illustrated for one igbt in Fig. 8.16 and for one diode in Fig. 8.17.

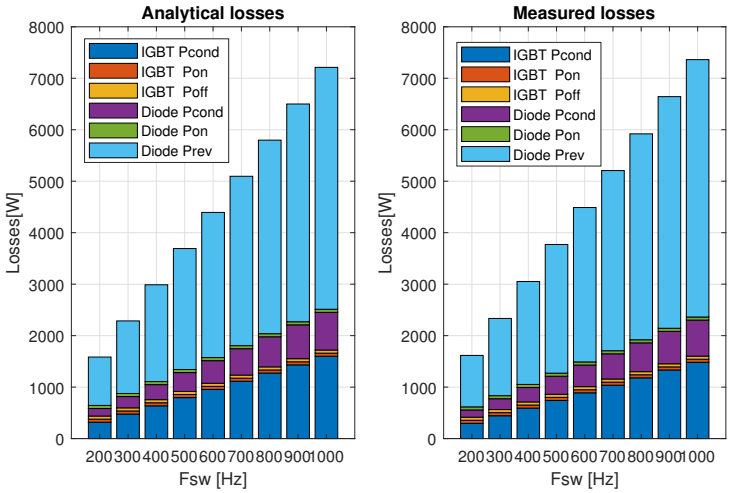


Fig. 8.18: Loss segregation on simulated semiconductor model a) and on measured semiconductor losses from exp b). [146]

Fig. 8.18a illustrates loss segregation on simulated waveforms, while Fig. 8.18a presents the measured semiconductor losses. It is noticed that igbt conduction, diode conduction and reverse recovery losses have the highest percentage, while the switching losses are insignificant. Regarding the diode reverse recovery losses, the model used in the experiment was PST-ZP750A/6500V, which is a general purpose high power avalanche rectifier

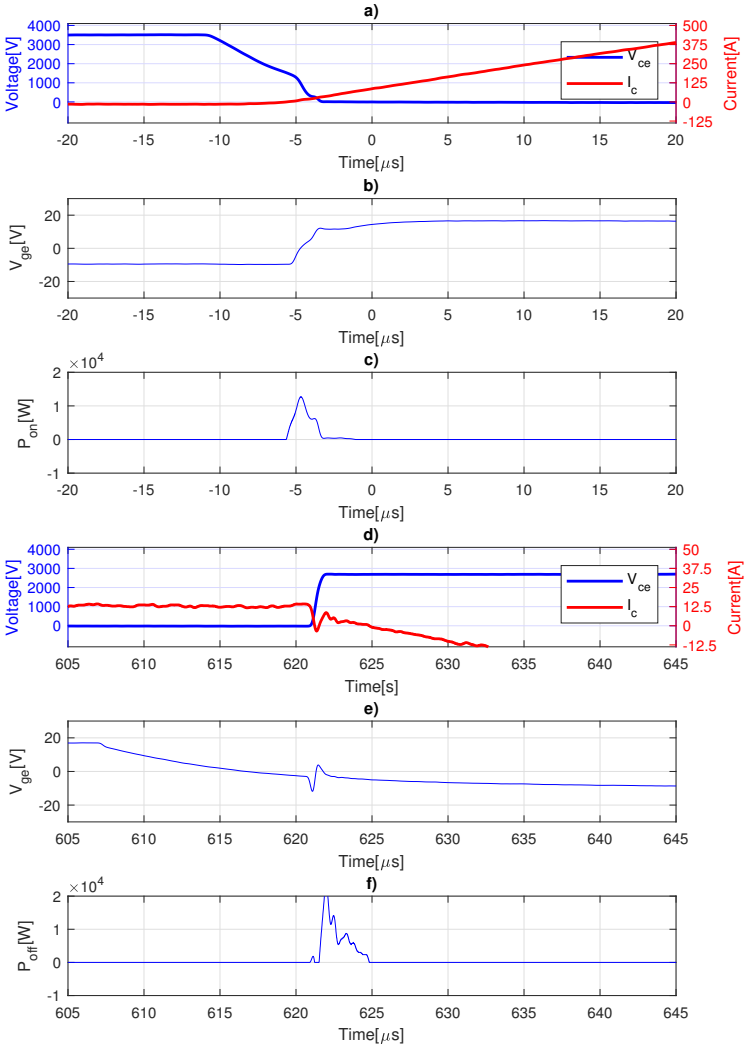


Fig. 8.19: IGBT switching waveforms: Turn-on process (a,b and c); Turn-off process (d,e and f). [146]

with a reverse recovery charge $Q_{rr} \approx 10000\mu C$. On the other hand, the target device is similar to 5SDD 06D6000, with $Q_{rr} \approx 2000\mu C$ and expected reverse recovery losses to be 5x smaller.

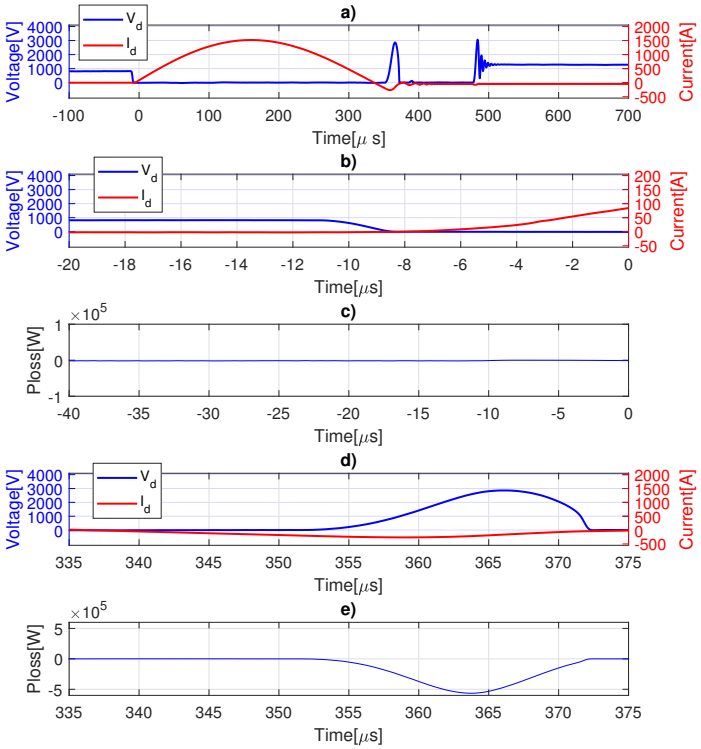


Fig. 8.20: Diode natural commutation: a) One conduction cycle; b) Turn-on Vd and Id; c) Turn-on losses; d) Vd and Id during reverse recovery; e) Reverse recovery losses [146]

Looking at Fig. 8.19, switching waveforms for one IGBT are presented, for a DC-link voltage of 4 kV and peak current reaching 1.5 kA. Fig. 8.19a presents the turn-on switching cycle and the equivalent turn-on losses in Fig. 8.19c. Quasi ZVS at turn on is observed with measured losses of $\approx 5W$ only. V_{ce} begins to drop befor the gate signal is applied, as the complementary IGBT is turned-off. Looking at Fig. 8.19c, the turn-off current is limited by the magnetizing current and losses are $\approx 27W$. Waveforms related to the rectifier diode are visualized in Fig. 8.20, with turn-on comutation in Fig. 8.20b and turn-off in Fig. 8.20d. As observed, turn-on losses are $\approx$0 W, while turn-off losses are close to 5000 W at F_{sw} = 1000Hz.

8.3 Conclusions

Two medium voltage setups have been built, each with different specifications and goals. One proof of concept of the SRC# was implemented in a 10 kW, 500V to 5000V laboratory prototype, while being operated with switching frequencies in the range as the target 10 MW example (0 to 1000 Hz). The main goal of the setup was to perform a preliminary semiconductor loss model validation, but also to evaluate the principle control architectures. The measured losses were ranging between 6% to 4.5%, while the measured inverter and rectifier losses correspond to that of the loss model, in the range from 2% to 1.5% of total losses. Confidence was built in the loss model and a second MV setup was implemented.

The second experimental setup was built with the intention of soft-switching characterization of 6.5 kV igbts and line frequency press-pack diodes. The proposed loss characterization philosophy required no expencive and bulky dc source or loads, as the principle of operation assumed recreation of a voltage drop across the LC tank. The semiconductor loss model was further compared with the measurements and was also fine-tuned. The error between igbts measured and simulated losses was between 6% to 7%, while on the diode model was ranging between 3% to 4%. Another preliminary efficiency measurement was done and during circulation of only a few resonant current pulses, 96% efficiency was recorded.

The conclusions of the experiments is that high confidence is built on the semiconductor loss model and more attention needs to be put on validation of the transformer loss model.

Chapter 9

Conclusions and future work

9.1 Summary

Offshore HVDC-connected wind farms promise reduced electrical losses, lower bill-of material cost and undiminished functionality with the condition the wind plant MV collection network becomes DC, rather than MVAC. One dearly missed building block that would enable the transition to a DC voltage collection, is the DC/DC converter for high power & high voltage (megawatss and kilovolts).

The main objective of this thesis was investigation and development of a turbine DC/DC converter proof of concept. To use as much as possible from the state of the art technology and philosophy, the target converter, needs to have electrical, cooling and control interfaces compatible with present turbine solutions. Physical size and weight should be smaller or equal, while efficiency and reliability must be higher or at least equal to today's AC turbine solution.

A survey of DC/DC converter topologies has been investigated. A multitude of variants exist, each with pluses and minuses and suitable for certain applications, but not all optimal for DC wind turbines. The surveyed topologies have been organized from switching point of view (hard and soft) and isolation type (isolated and non-isolated). As it required big effort to analyze and compare all possible topologies, a survey of industrial and university demonstrators (in traction, solid state transformers and DC wind turbines) was performed to further down select the number of possible variants. It was concluded that only a few topologies have been implemented on hundreds of kilowatts and megawatts demonstrators: the dual active-bridge (DAB) and the series resonant converter (SRC) topology. In both traction and SST, modularity on converter level is used, while the DAB is more suitable for bidirectional applications for hundreds of megawatt. Regardless of selected topologies, the turbine converter needs to fulfill a set of functionalities and establish which areas present larker riskcs as compared to the others. The F-FMEA and Pugh Matrix were used to establish the list of functionalities and main design drivers. Five different topologies were compared based on different design drivers, and from that list a variant of the classic series resonant converter, entitled SRC# was suggested as an option for the turbine converter.

From the survey of demonstrators, the classic SRC is used as a DC/DC transformer, adapting one DC-link voltage to another one with a low turns ratio, while other converter stages on the front and back side are controlling the DC-link voltage level. In a DC wind turbine converter, the SRC requires a form of control on LV DC link side. Further on, as the application itself imposes tough requirements as high distance to shore, high humidity and salty environment, a design that aims at a low number of components is neccesary. For this reason, it is suggested to have sub-system modularity on inverter

level and device modularity on rectifier level, while a monolithic transformer with one primary and one secondary winding should be employed.

9.2 Conclusions

It is considered that the transition of MVAC connected wind turbines to MVDC output is conceivable with present and commercial technologies, with efficiency and power density at least equal to present turbine configurations. Off the shelf igbts and line frequency diodes combined with monolithic amorphous cores designed for medium frequency transformer and LC tanks allow the adaptation of wind turbines to DC outputs. Therefore, a variant of the single phase series resonant converter, has been suggested as an optimal candidate.

The thesis suggested a new modulation scheme for a single-phase SRC, which permits requlation of power from nominal level to zero, in presence of variable input and output DC voltage levels. The circuit was rearranged so that the LC tank is located on the rectifier side of the high-turns ration transformer combined with frequency control and phase shifted inverter modulation. The modulation scheme was entitled pulse removal technique and it keeps the transformer flux constant from nominal frequency down to DC, always in sub-resonant continuous or discontinuous conduction mode.

The SRC operated with pulse removal technique was entitled SRC# (as in series resonant converter sharp) and it has the advantages of: compact and efficient transformer, as the transformer is designed for maximum operating frequency, validating the hypothesis that high power density is conceivable.

High efficiency is another advantage, due to the soft-switching nature of the converter: zero-voltage turn-on and low turn-off current on the inverter side, and zero-voltage turn-on and zero-current turn-on on the rectifier side diodes. With transformer excitation frequency in hundreds of Hz range, line-frequency diodes can be employed on the rectifier side, benefiting advantages of cheap and robust components. Therefore, the second hypothesis of the thesis, related to low loss commutation has been answered. Four modes of operation for the SRC# were identified (two continuous and two discontinuous), with the characterisctic voltage and current waveforms. Power flow equations were derived for each mode of operation.

The circuit was further characterized with respect to peak current and voltage stress and their variation to switching frequency. The impact of transformer magnetizing inductance on primary resonant waveforms and switching losses was investigated. One interesting aspect of semiconductor losses was their constant value in the range of 500 Hz to 5000 Hz of frequency specifications. The challenges of building a high voltage rectifier valve with focus on diode voltage balancing, impact of snubber components

and valve mechanical stray parameters were discussed and finally the impact of non-idealities on the characteristic waveforms was shown. The diodes' dynamic and static voltage balancing is heavily impacted by differences in diodes physical parameters (such as reverse recovery charge, leakage current), temperature differences and RC circuit tolerances. It was found that a trade-off between maximum permissible blocking voltage per diode and impact on resonant current waveforms is neccesary. Further on, by increasing the transformer nominal switching frequencies, the distances between primary and secondary windings are decreased, thus impacting the windings stray capacitances. The effect is noticeable especially on the hundreds of kiloherz range, but for a limited frequency range of 500 Hz to 5000 Hz, as in this application, the effect is considered to be diminished.

A design guide line for SRC#, suitable for a given range of specifications, in the megawatt (5 to 15 MW), kilovolt ($\pm$35 to $\pm$50 kV) and kilohertz (0.5 to 5.0 kHz) range was introduced. The guide line discusses selection of switching frequency and how the derivation of LC tank parameters impacts specifications for semiconductor and medium frequency transformer ratings. The output results are volume, weight, losses and bill of materials, with a 10 MW, $\pm$2 to $\pm$50 kV and 1 kHz design example illustrated.

Therefore, technology readiness level for DC/DC converters for wind turbines has been increased from TRL2 to TRL3. A proof of concept has been introduced on a 10 kW, 500V to 5000V scaled prototype. Characteristical waveforms, efficiency measurements and closed loop control were implemented, with the main goal of semiconductor loss model validation. Static and dynamic voltage sharing on the rectifier diodes increase confidence that this circuit can be built at elevated parameters.

It is considered that the proof of concept and principle demonstrators have provided sufficient results and confirm/calibrate the design analysis and simulation to an extent that allows extrapolation to further demonstrator with enough certainty in estimated performance and cost. The hypothesis have been proven and build confidence that this circuit could be extrapolated to 10MW/$\pm$50kV operation.

9.3 Criticality of SRC#

An overall critical discussions of the drawback of the SRC# is also required. During the experimental phases, the acoustic noise generated by the transformer's magnetostriction effect, as the switching frequency was in the audible range (0 to 1000 Hz) was clearly noticed. It is considered that this effect can be diminished through proper mechanical design of the transformer enclosure, and should filter the high pitch accoustic noice.

Another aspect the possibility of implementing the topology only in a

single phase options. The three phase variant was also investigated, but it was concluded that due to magnetic flux assymetry, a variant with a three phase transformer was not possible to be implemented. On the other hand, a variant with three single phase transformers, is possible as seen in Fig. **??**.

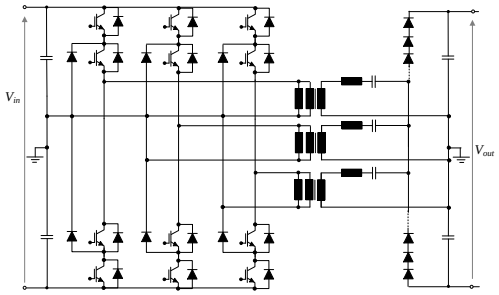


Fig. 9.1: Three phase SRC# with three single phase transformers

Further on, as medium voltage capacitors should be used on the high voltage side, questions regarding the degradation of their life time and even posibility of designing the capacitors for 25 years (as expected from turbine manufacturers) were raised. The capacitors have limited life time, can have explosive failure modes and depending on technology type, have a large foot print. But, as suggested in [147], self healing metallized hazy polypropylene are one possible solution. They offer 300.000 hour life time operation and were also proposed in a poly-phase resonant converter for generation of high voltage. They offer graceful degradation, have extremely high volumetric efficiency and a high safety factor.

Another aspect worthy to mention is the possibility of integrating the resonant inductor as the transformer leakage inductance, but also consistency in building transformers with a very low variation in the leakage inductance. This fact is considered to be a limiting factor of the technology and requires more attention.

9.4 Main contributions

- A new modulation scheme, entitled *pulse removal technique* has been introduced for a single-phase series-resonant converter, which permits continuous regulation of power from nominal level to zero, in presence of variable input and output dc voltage levels.
- A new converter philosophy for DC wind turbine application was proposed, consisting of modular inverters, one monolithic transformer with

one primary and secondary winding, LC tank located on rectifier side and rectifier assembled with line frequency diodes.

- Circuit conduction modes, output power, voltage and current stress for the novel scheme have been identified together
- Experimental validation of converter characteristic steady-state waveforms and semiconductors loss model
- Experimental investigation of static and dynamic voltage sharing across series connected devices on rectifier side
- Proposed a novel soft-switching characterization setup, that allows loss extraction of target devices for 1 to N voltage gains, allows voltage sharing investigation and requires no bulky components.
- A closed loop control architecture was proposed and validated
- A design guide line for SRC#, valid for mega-watt, kilo-volt and kilo-hertz range is proposed.

9.5 Outlook and future work challenges

This thesis has focused on delivering a proof of concept and due to project limitations only certain areas have been covered. For future work, it is recommended to increase the technology readiness level to TRL6-7 through the completion of a thermal concept, at elevated power and voltage (such as 0.2 MW and $\pm 10kV$) in continuous operation, while using the target igbts and rectifier diodes. The scaled transformer should be designed for similar switching frequencies as the target specifications and use similar technologies for cooling and oil immersion. Further works needs to address transformer loss model validation.

An automated design procedure with focus on addressing the extremes of the operating points - under assumption of well-working controls - which define worst case component loads, must be implemented.

A low stray capacitance medium voltage valve design has to be investigated, in order to avoid partial discharges and balanced voltage sharing acroos the rectifier diodes.

Focus on protection circuits, common mode currents, EMI, partial free design, isolation coordination and philosophy for auxiliary power supplie and measurement circuits needs to be further adressed.

Development of press pack devices with multiple series connected diodes inside should be adressed and investigation of opportunity to employ Si-Carbide diodes that have a safe to fail behaviour is needed.

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Appendices

A.1 Semiconductor loss model

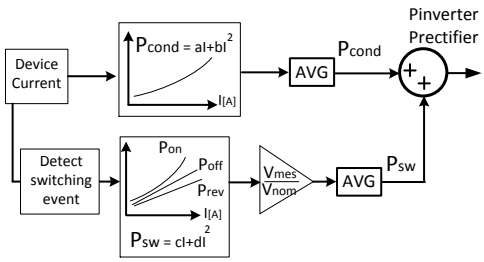


Fig. 2: Power semiconductor loss model

Power semiconductor loss model

Semiconductors loss model is presented in Fig. 2. The IGBTs T1 and T4 have both ZVS (zero voltage switching) at turn-on and a low turn off current, while rectifier diodes D5 and D8 exibit ZVS at turn on and ZCS at turn-off.

Conduction losses

Methodology proposed in [97], [98] is used for conduction loss modelling for both IGBTs and diodes. The current is multiplied with the according voltage directly from the data sheet for the highest acceptable temperature, e.g. T=125°C to extract conduction power loss. Afterwards, the curve is approximated with 2nd order polynomial fitting curves, as described in Eq. 1 which uses the current through the ideal switch as input and outputs conduction loss of the device during the simulation. The output is averaged for

Table 1: Transformer loss model parameters

Parameter	Value
D	Waveform duty cycle
MLT	Mean length turn
$Nturns$	Winding number of turns
m	Winding number of layers
R_{dc}	Winding dc resistance
R_{ac}	Winding ac resistance
δ	Foil winding skin depth
I_{rmsh}	RMS current per harmonic

1 switching cycle.

$$P_{Cond} = a \cdot I + b \cdot I^2 \tag{1}$$

$$P_{Sw} = c \cdot I + d \cdot I^2 \tag{2}$$

Switching losses

Switching losses are determined in similar way like in [14],[15]. Current dependent E_{ON}, E_{OFF} and E_{REC} are given in the device datasheet and are considered for a maximum junction temperature of T=125°C. This dependency is approximated with a second order polynomial fitting curve, as shown in Eq. 2 and multiplied with voltage factor V_{mes}/V_{nom}, where V_{nom} is datasheet parameter and V_{mes}, actual applied voltage. When a switching event occurs, losses are calculated and then averaged for 1 switching cycle.

A.2 Transformer and resonant tank loss model

The simplified transformer loss model is presented in Fig. 3 and it estimates core and winding losses.

Core losses

Different methods have been compared in [67],[78],[77],[144] for core losses. In the present loss model, the Improved Generalized Steinmetz Equation (IGSE) described in [67] was used with K_i, α and β determined from [35].

$$P_{Core} = K_i \cdot 2^{\alpha+\beta} \cdot {F_{sw}}^{\alpha} \cdot B^{\beta} \cdot D^{1-\alpha} \tag{3}$$

Winding losses

Foil winding losses are calculates, as according to [10],[11]. The expression from Eq. 4 is explained in [67]. The overall losses are calculated by summing

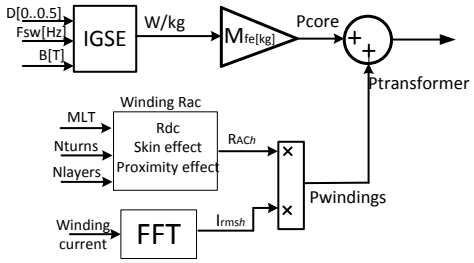


Fig. 3: Transformer loss model

the effect of every current harmonic. Skin effect losses are frequency dependent (Eq. 5), while proximity losses (Eq. 6) are influenced by the number of layers. D represents foil thickness, while δ is skin depth and m is the number of layers.

$$P_{Winding} = R_{DC} \cdot \frac{D}{\delta} \cdot [A + \frac{2 \cdot (m^2 - 1)}{3} + B] \cdot I_{rms}^2 \tag{4}$$

$$A = \frac{\sinh(\frac{D}{\delta}) + \sin(\frac{D}{\delta})}{\cosh(\frac{D}{\delta}) - \cos(\frac{D}{\delta})} \tag{5}$$

$$B = \frac{\sinh(\frac{D}{\delta}) - \sin(\frac{D}{\delta})}{\cosh(\frac{D}{\delta}) - \cos(\frac{D}{\delta})} \tag{6}$$

A.2.1 Resonant tank losses

To estimate the resonant tank losses, the simplest approach is to predefine the tank quality factor Q_s to a value of 200, and from it calculate the tank equivalent resistance, as shown in Eq. 7, and multiply it with the square of load current:

$$R_{LC} = \frac{Z_c}{Q_s} \tag{7}$$

$$LC_{loss} = R_{LC} \cdot I_{out}^2 \tag{8}$$

To keep resonant tank losses low, the Q_s should be higher than 100, meaning very low inductor resistance and capacitor ESR.

A.3 Derivation of power flow equation in CCM1-hybrid

Derivation of power flow equation is performed and similar to [123], [148], [149].

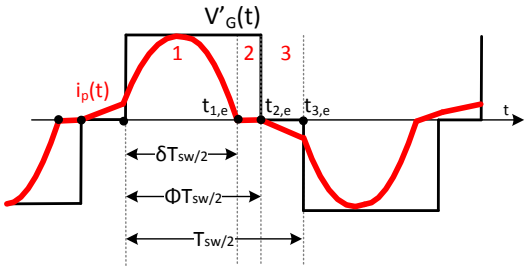


Fig. 4: CCM1 hybrid characteristic waveforms

A.3.1 Current continuity equations

$$i_{P1} = A_1 \cdot \sin(\omega_0 t_{1,e} + \alpha_1) \quad (9)$$
$$i_{P2} = A_2 \cdot \sin(\omega_0 t_{2,e} + \alpha_2) = 0 \quad (10)$$
$$i_{P3} = A_3 \cdot \sin(\omega_0 t_{3,e} + \alpha_3) \quad (11)$$

Where $\alpha_3 = 0$. In points $t_{1,e}$, $t_{2,e}$ and $t_{3,e}$: $i_{P(k)} = i_{P(k+1)}$, therefore:

$$A_1 \cdot \sin(\omega_0 t_{1,e} + \alpha_1) = 0 \quad (12)$$
$$A_2 \cdot \sin(\omega_0 t_{2,e}) = A_3 \cdot \sin(\alpha_3) = 0 \quad (13)$$
$$A_3 \cdot \sin(\omega_0 t_{3,e} + \alpha_3) = A_1 \cdot \sin(\alpha_1) \quad (14)$$

A.3.2 Voltage across capacitor continuity

derived from $V_t = V_{in} - V_{out}$.

$$\omega_0 L_r A_3 \cos(\omega_0 t_{3,e} + 0) + V_{out} = \omega_0 L_r A_1 \cos(\alpha_1) - V_{in} + V_{out} \quad (15)$$
$$\omega_0 L_r A_1 \cos(\omega_0 t_{1,e} + \alpha_1) - V_{in} + V_{out} = 0 - V_{Cr} \quad (16)$$
$$0 - V_{Cr} = \omega_0 L_r A_3 - V_{out} \quad (17)$$

Considering equations:

$$t_{1,e} = \frac{\delta \cdot T_{sw}}{2} \tag{18}$$

$$t_{2,e} = \frac{\Phi \cdot T_{sw}}{2} \tag{19}$$

$$t_{3,e} = \frac{T_{sw}}{2} \tag{20}$$

$$K = \frac{\omega_0 \cdot T_{sw}}{2} \tag{21}$$

$$Q = \omega_0 L_0 \tag{22}$$

A.3.3 Power balance equation

$$P_{in} = P_{out} \tag{23}$$

$$V_{in} I_{in} = V_{out} I_{out} \tag{24}$$

$$\frac{2}{T_{sw}} V_{in} \left(\int_0^{t_1} i_{P,1} dt_{1,e} = \frac{2}{T_{sw}} V_{out} \left(\int_0^{t_1} i_{P,1} dt_{1,e} + \int_{t_2}^{t_3} i_{P,3} dt_{3,e} \right) \right. \tag{25}$$

Where:

$$\int_0^{t_1} i_{P,1} dt_{1,e} = \frac{A_1}{\omega_0} (\cos \alpha_1 - \cos (\delta K + \alpha_1)) \tag{26}$$

$$\int_{t_2}^{t_3} i_{P,3} dt_{3,e} = \frac{A_3}{\omega_0} (\cos \phi K - \cos K) \tag{27}$$

After simplifications:

$$P_{in} = \frac{2}{T_{sw}} V_{in} \frac{1}{\omega_0} A_1 \cdot (1 - cos(\delta K)) \tag{28}$$

From eq. 16:

$$Q A_1 \cos(\delta K + \alpha_1) - V_{in} + V_{out} = -V_{Cr} \tag{29}$$

From eq. 12 and considering that $\alpha_1 = \pi - \delta K$

$$Q A_1 - V_{in} + V_{out} = -V_{Cr} \tag{30}$$

In eq. 14: Equating eq. 16 and eq. 17:

$$A_3 = -A_1 + \frac{2V_{out} - V_{in}}{Q} \tag{31}$$

Then replacing eq. 31 in eq. 14, A_1 is calculated as:

$$A_1 = \frac{(2V_{out} - V_{in}) \cdot \sin K}{Q(\sin \delta K + \sin K)} \tag{32}$$

Replacing again eq. 31 in eq. 15, A_1 is calculated as:

$$A_1 = \frac{(2V_{out} - V_{in}) \cdot \cos K + V_{in}}{Q(-\cos \delta K + \cos K)} \tag{33}$$

Equating eq. 32 and eq. 33, δ is calculated as:

$$\delta = 1 + \frac{2 \cdot atan(\frac{(V_{in} + \cos(K) \cdot (2 \cdot V_{out} - V_{in}))}{(sin(K) \cdot (2 \cdot V_{out} - V_{in}))})}{K} \tag{34}$$

A.3.4 Power equation for CCM1-Hybrid

Considering eq. 34, eq. 28 after simplifications becomes:

$$P_{in} = {V_{in}}^2 \cdot \omega_{sw} \cdot C_r \cdot \frac{1}{\pi} \cdot A \tag{35}$$

Where A is:

$$A = \frac{(1 - \cos(\delta)) \cdot ((2M - 1) \cdot \cos(K) + 1)}{\cos(K) - \cos(\delta K)} \tag{36}$$

A.4 Derivation of power flow equation in CCM1

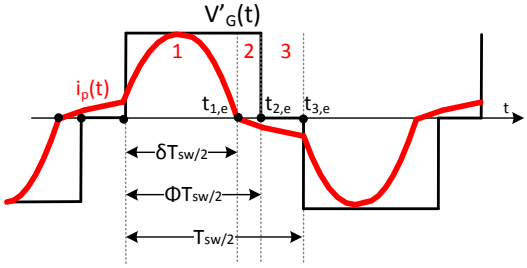


Fig. 5: CCM1 characteristic waveforms

A.4.1 Current continuity equations

$$i_{P1} = A_1 \cdot \sin(\omega_0 t_{1,e} + \alpha_1) \tag{37}$$
$$i_{P2} = A_2 \cdot \sin(\omega_0 t_{2,e} + \alpha_2) \tag{38}$$
$$i_{P3} = A_3 \cdot \sin(\omega_0 t_{3,e} + \alpha_3) \tag{39}$$

In points $t_{1,e}$, $t_{2,e}$ and $t_{3,e}$: $i_{P(k)} = i_{P(k+1)}$, therefore:

$$\begin{aligned} A_1 \cdot \sin(\omega_0 t_{1,e} + \alpha_1) &= 0 && (40)\\ A_2 \cdot \sin(\omega_0 t_{2,e} + \alpha_2) &= A_3 \cdot \sin(\alpha_3) && (41)\\ A_3 \cdot \sin(\omega_0 t_{3,e} + \alpha_3) &= A_1 \cdot \sin(\alpha_1) && (42) \end{aligned}$$

A.4.2 Voltage across capacitor continuity

derived from $V_t = V_{in} - V_{out}$.

$$\omega_0 L_r A_3 \cos(\omega_0 t_{3,e} + \alpha_3) + V_{out} = \omega_0 L_r A_1 \cos(\alpha_1) - V_{in} + V_{out} \quad (43)$$

$$\omega_0 L_r A_1 \cos(\omega_0 t_{1,e} + \alpha_1) - V_{in} + V_{out} = \omega_0 L_r A_2 - V_{in} - V_{out} \quad (44)$$

$$\omega_0 L_r A_2 \cos(\omega_0 t_{2,e} + \alpha_1) - V_{in} - V_{out} = \omega_0 L_r A_3 \cos(\alpha_3) - V_{out} \quad (45)$$

Considering equations:

$$\begin{aligned} t_{1,e} &= \frac{\delta \cdot T_{sw}}{2} && (46)\\ t_{2,e} &= \frac{(\Phi - \delta) \cdot T_{sw}}{2} && (47)\\ t_{3,e} &= \frac{T_{sw}}{2} && (48)\\ K &= \frac{\omega_0 \cdot T_{sw}}{2} && (49)\\ Q &= \omega_0 L_0 && (50) \end{aligned}$$

A.4.3 Power balance equation

$$\begin{aligned} P_{in} &= P_{out} && (51)\\ V_{in} I_{in} &= V_{out} I_{out} && (52) \end{aligned}$$

$$\frac{2}{T_{sw}} V_{in} \left(\int_0^{t_1} i_{P,1} dt_{1,e} - \int_{t_1}^{t_2} i_{P,2} dt_{2,e}\right) = \frac{2}{T_{sw}} V_{out} \left(\int_0^{t_1} i_{P,1} dt_{1,e} + \int_{t_1}^{t_2} i_{P,2} dt_{1,e} + \int_{t_2}^{t_3} i_{P,3} dt_{3,e}\right) \quad (53)$$

$$P_{in} = \frac{2}{T_{sw}} V_{in} \frac{1}{\omega_0} ((\cos(\alpha_1) - cos(\delta K + \alpha_1)) A_1 - (cos(\delta K) - cos(\Phi K)) A_2) \quad (54)$$

It's necessary to find $A_1, A_2, \alpha_1, \delta$: Considering eq. 44:

$$QA_1 \cos(\delta K + \alpha_1) + 2V_{out} = QA_2 \tag{55}$$

Considering eq. 40:

$$\alpha_1 = \pi - \delta K \tag{56}$$

From previous two equations:

$$A_2 = -A_1 + \frac{2V_{out}}{Q} \tag{57}$$

Considering eq. 41 and eq. 45

$$\sin \alpha_3 = \frac{A_2 \cdot \sin(\Phi - \delta)K}{A_3} \tag{58}$$

$$\cos \alpha_3 = \frac{A_2 \cdot \cos(\Phi - \delta)K - \frac{V_{in}}{Q}}{A_3} \tag{59}$$

The main goal now is to identify A_1. Looking at eq. 42:

$$A_3(\sin(K)\cos(\alpha_3) + \sin(\alpha_3)\cos(K)) = A_1 \sin(\delta K)$$

$$A_3(\sin(K)(\frac{A_2 \cos(\Phi - \delta)K - \frac{V_{in}}{Q}}{A_3}) + (\frac{A_2 sin(\Phi - \delta)}{A_3})\cos(K)) = A_1 \sin(\delta K)$$

$$A_2(\sin(K)\cos(\phi - \delta) + \sin(\phi - \delta)K) - A_1 \sin(\delta K) = \frac{V_{in}}{Q}\sin(K)$$

$$(\frac{2V_{out}}{Q} - A_1)(\sin(\Phi - \delta + 1)K) - A_1 \sin(\delta K) = \frac{V_{in}}{Q}\sin(K)$$

$$-A_1(\sin(\phi - \delta + 1)K + \sin(\delta K)) = \frac{-2V_{out}\sin(\phi - \delta + 1) + V_{in}\sin(K)}{Q}$$

In the end, A_1 is :

$$A_1 = \frac{V_{in}\sin(K) - 2V_{out}\sin(\phi - \delta + 1)}{-Q(\sin(\theta - \delta + 1)K + sin(\delta K))} \tag{60}$$

In following equation, A_1 is calculated again, from eq. 43:

$$QA_3(\cos K\cos\alpha_3 - \sin K\sin\alpha_3) = -QA_1\cos(\delta K) - \frac{V_{in}}{Q}$$

$$A_3(\cos K(\frac{A_2\cos(\phi-\delta) - \frac{V_{in}}{Q}}{A_3}) - \frac{\sin K\sin(\phi-\delta)K}{A_3}) = -A_1\cos(\delta K) - \frac{V_{in}}{Q}$$

$$A_2(\cos K\cos(\phi-\delta) - \sin K\sin(\phi-\delta)K) + A_1\cos(\delta K) = \frac{V_{in}}{Q}(\cos K - 1)$$

$$A_2\cos(\phi-\delta+1)K + A_1\cos\delta K = \frac{V_{in}}{Q}(\cos K - 1)$$

$$(-A_1 + \frac{2V_{out}}{Q})\cos(\phi-\delta+1)K + A_1\cos\delta K = \frac{V_{in}}{Q}(\cos K - 1)$$

$$A_1(\cos\delta K - \cos(\phi-\delta+1)) = \frac{V_{in}(\cos K - 1) - 2V_{out}\cos(\phi-\delta+1)}{Q}$$

In following equation, A_1 is calculated as:

$$A_1 = \frac{V_{in}(\cos K - 1) - 2V_{out}\cos(\phi-\delta+1)K}{-Q(\cos(\phi-\delta+1) - \cos(\delta K))} \tag{61}$$

By equating eq. 60 and 61, δ is found:

A.4.4 Power equation for CCM1

$$P_{in} = \frac{2}{T_{sw}}V_{in}\frac{1}{\omega_0}(A_1\cos(\alpha_1) - \cos(\delta K + \alpha_1) - A_2(\cos(\delta K) - cos(\phi K))) \tag{62}$$

$$\alpha_1 = \pi - \delta K \tag{63}$$

$$A_1 = \frac{V_{in}\sin(K) - 2V_{out}\sin(\phi-\delta+1)}{-Q(\sin(\theta-\delta+1)K + sin(\delta K))} \tag{64}$$

$$A_2 = -A_1 + \frac{2V_{out}}{Q} \tag{65}$$

$$\delta = \frac{\phi}{2} + \frac{1}{K}\arcsin(\frac{-M}{2}\frac{\sin(\phi+1)K}{\sin(\frac{(\phi+1)K}{2})\sin(\frac{K}{2})}) \tag{66}$$

After simplifications ($\phi K = \pi$):

$$P_{in} = \frac{2}{T_{sw}} V_{in} \frac{1}{\omega_0} (A_1(1 - \cos(\delta K)) - A_2(1 + \cos(\delta K))) \quad (67)$$

$$A_1 = \frac{V_{in} \sin(K) + 2V_{out} \sin(1 - \delta)k}{-Q(\sin(\delta K) - sin(1 - \delta)K)} \quad (68)$$

$$\delta = \frac{\phi}{2} + \frac{1}{K} \arcsin(M \frac{\cos(\frac{K}{2})}{\sin(\frac{(\phi+1)K}{2})}) \quad (69)$$

A.5 FB, SAB, LLC, SRC and SRC# waveforms

A.5.1 Full bridge (FB) converter

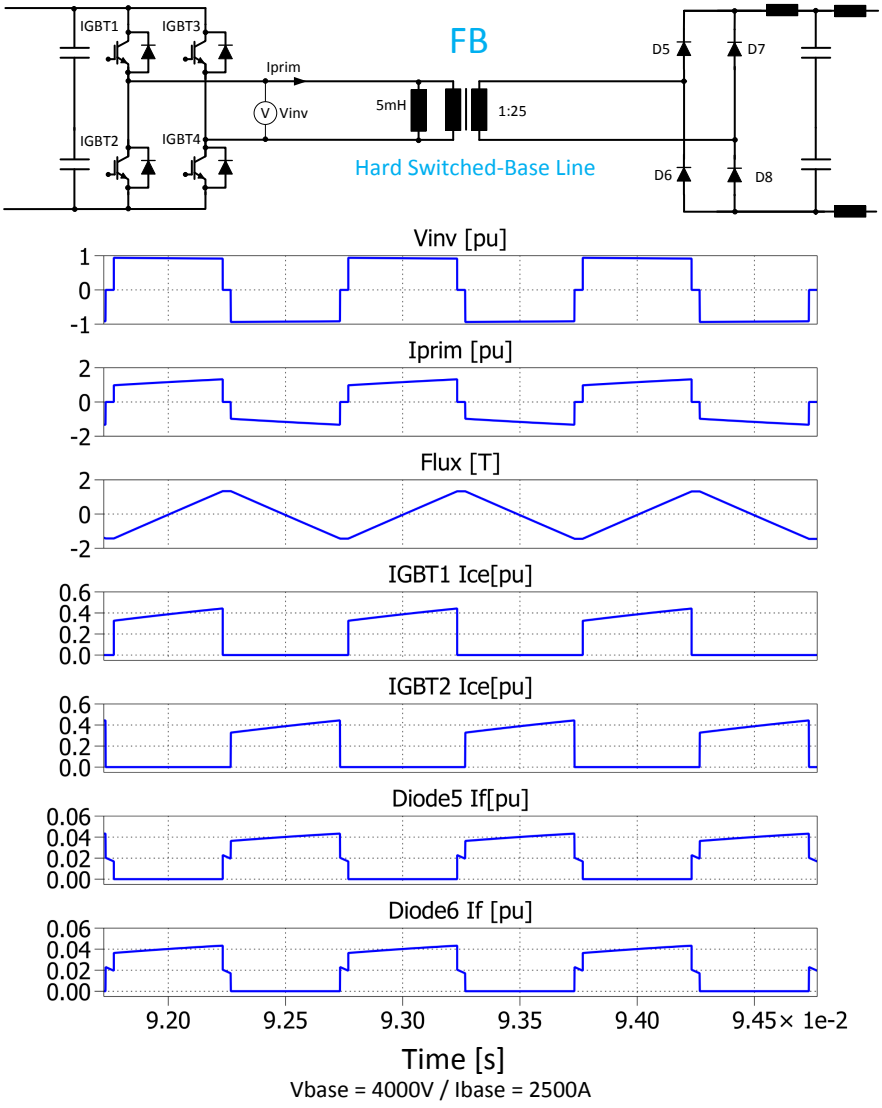


Fig. 6: Full bridge characteristic waveforms

A.5.2 Single active bridge (SAB) converter

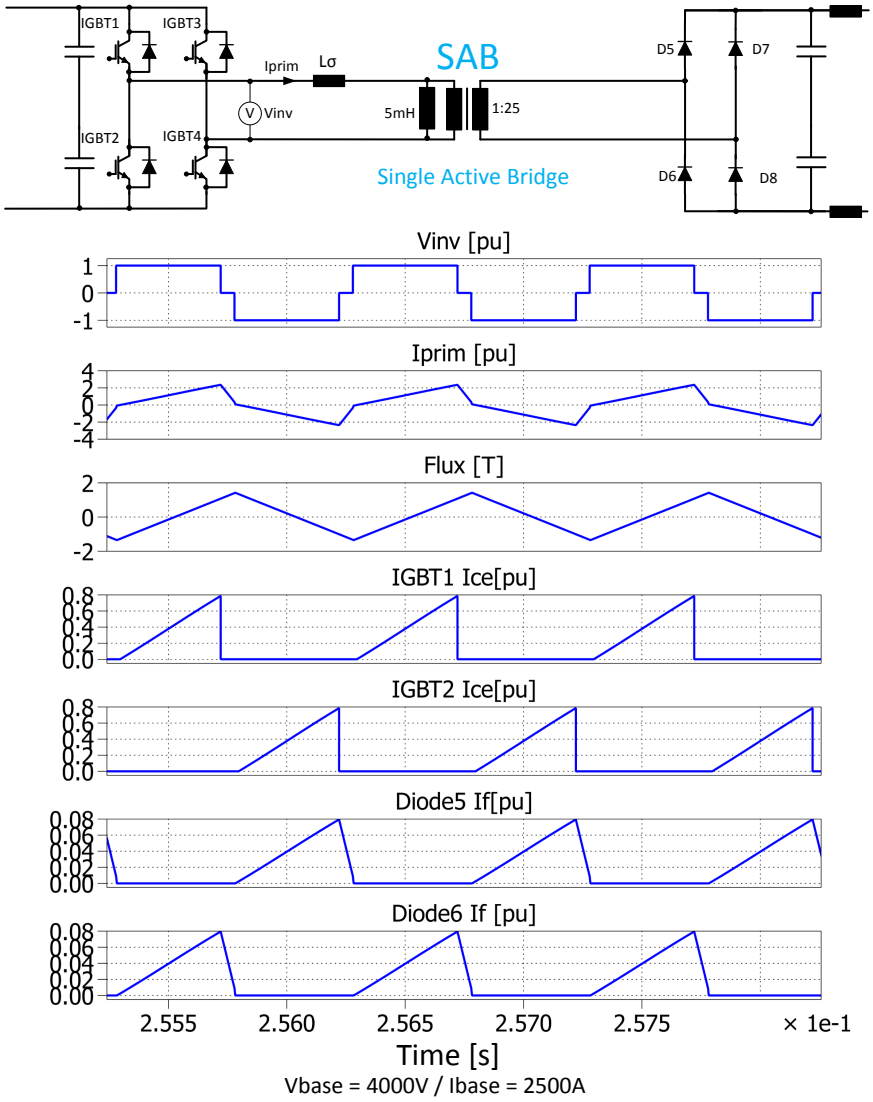


Fig. 7: Single active bridge characteristic waveforms

A.5.3 LLC converter

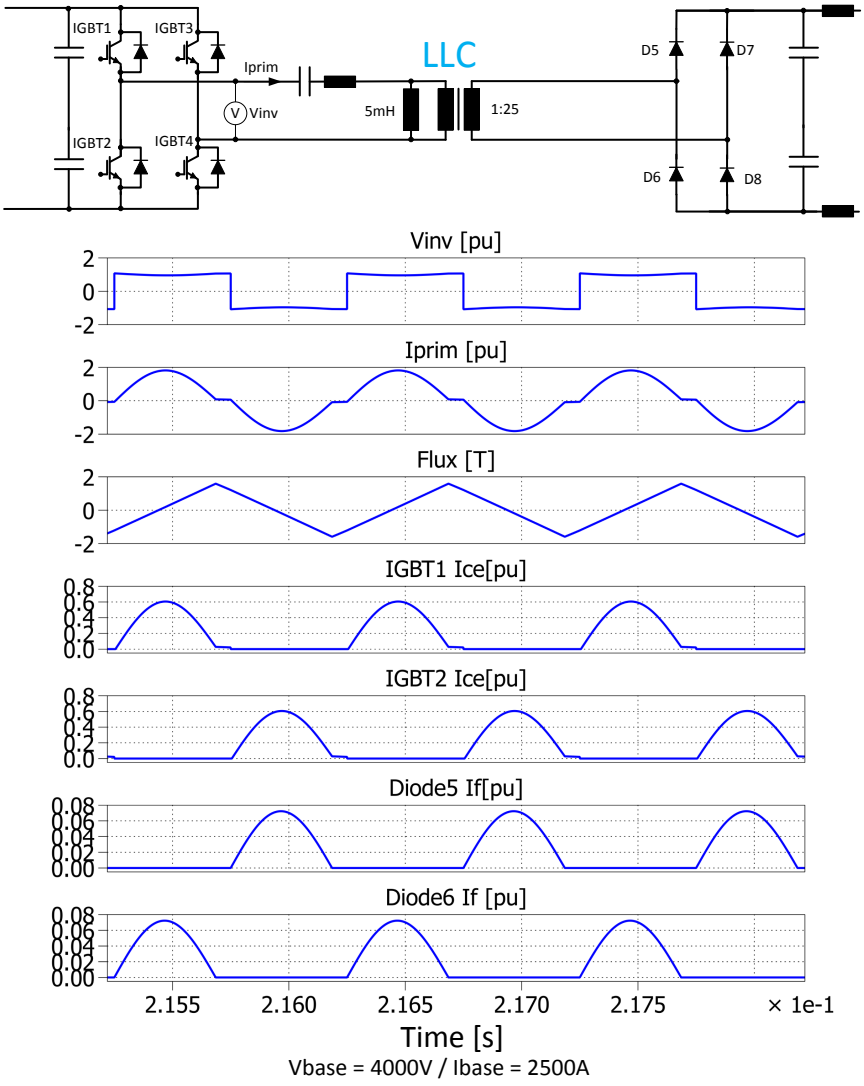


Fig. 8: LLC characteristic waveforms

A.5.4 Series resonant converter (SRC) with generous transformer design

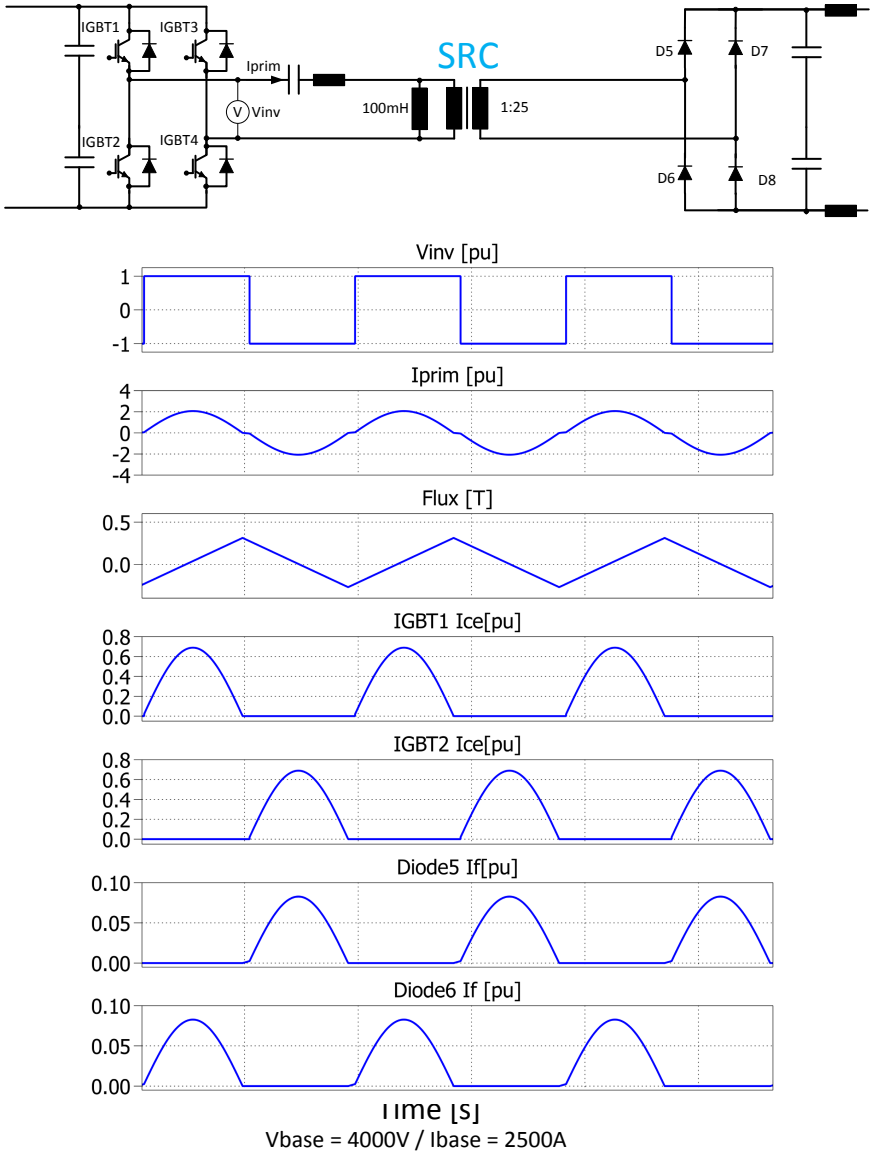


Fig. 9: SRC characteristic waveforms

A.5.5 Series resonant converter (SRC#) with LC tank on secondary side and pulse removal technique

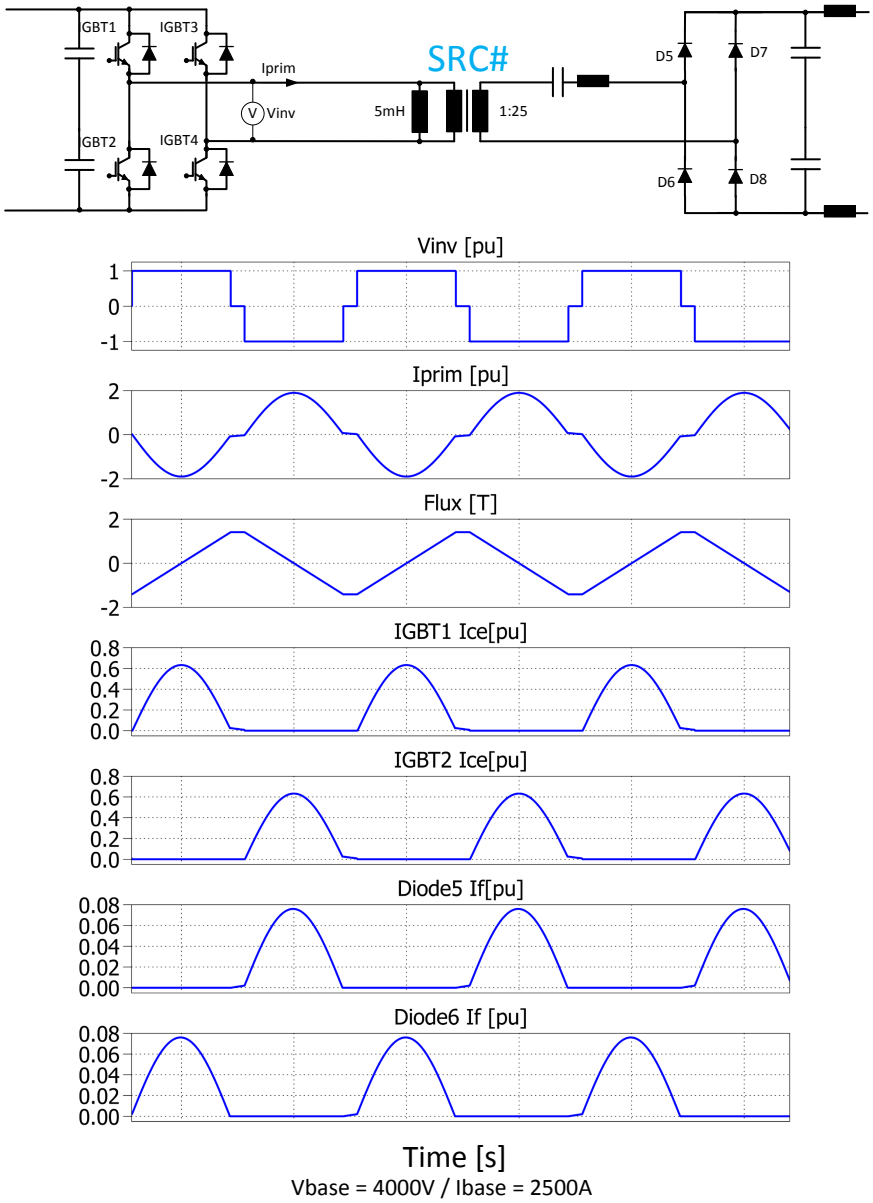


Fig. 10: SRC# characteristic waveforms

A.6 Classic SRC

LC Tank is located on primary side and only frequency control is employed.

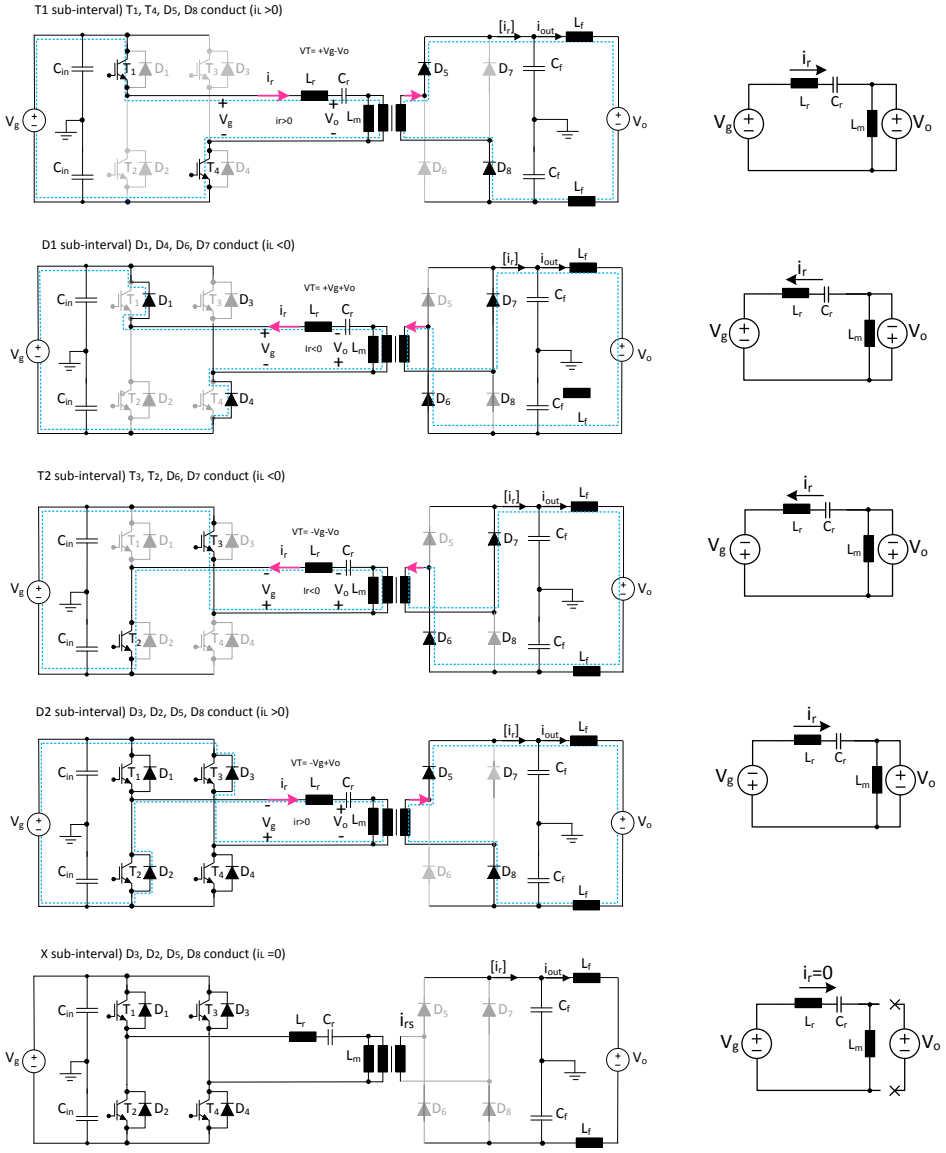
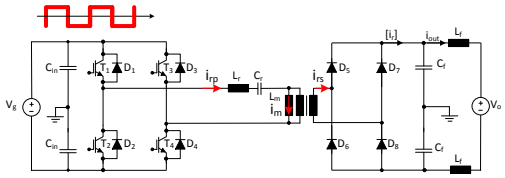


Fig. 11: Classic SRC equivalent circuits



DCM1:T1-X-T2-X

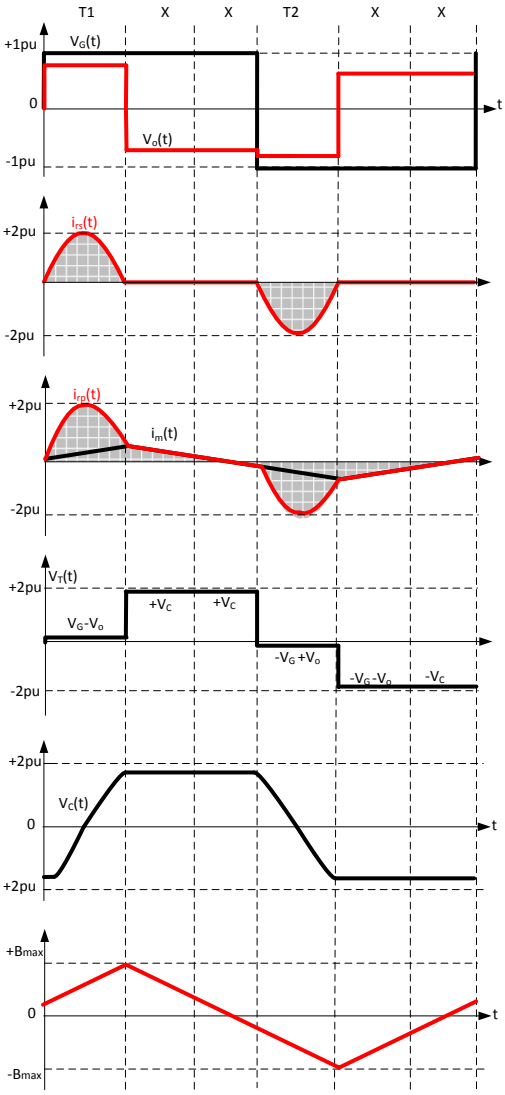
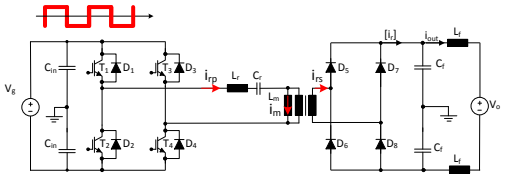


Fig. 12: Classic SRC DCM1 waveforms



DCM2:T1-D1-X-T2-D2-X

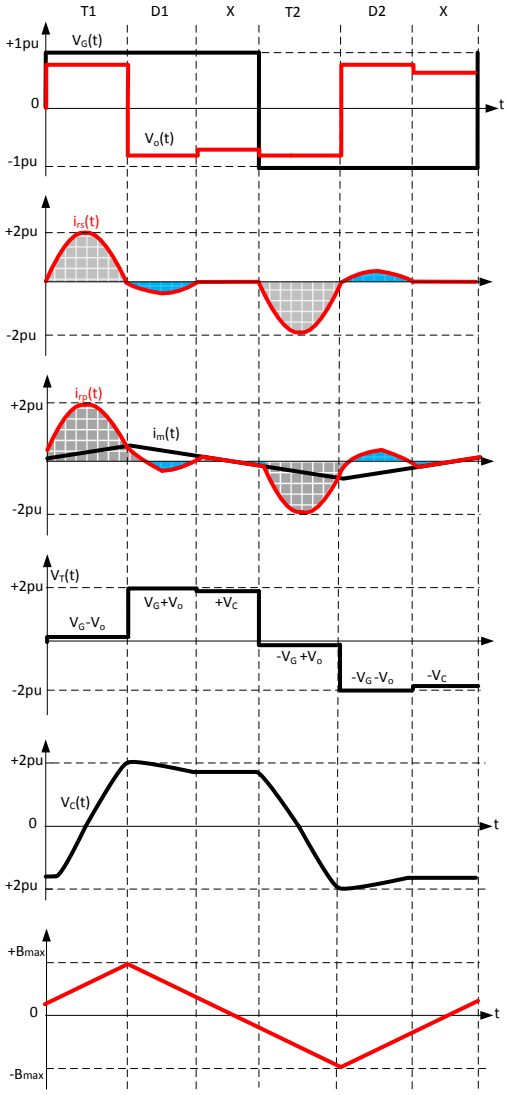
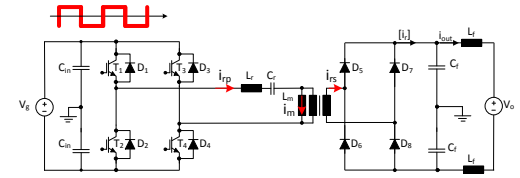


Fig. 13: Classic SRC DCM2 waveforms



CCM1:T1-D1-T2-D2

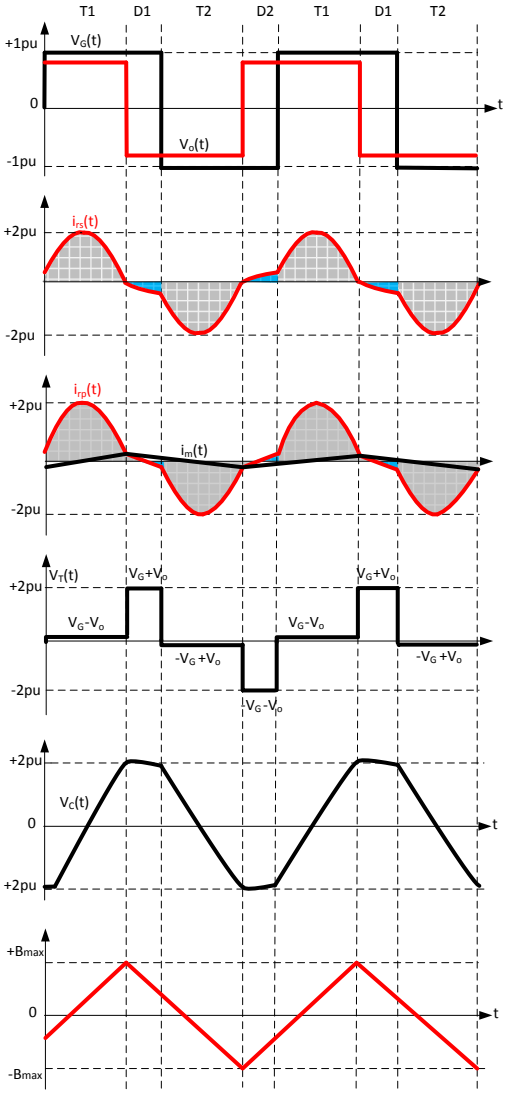


Fig. 14: Classic SRC CCM1 waveforms

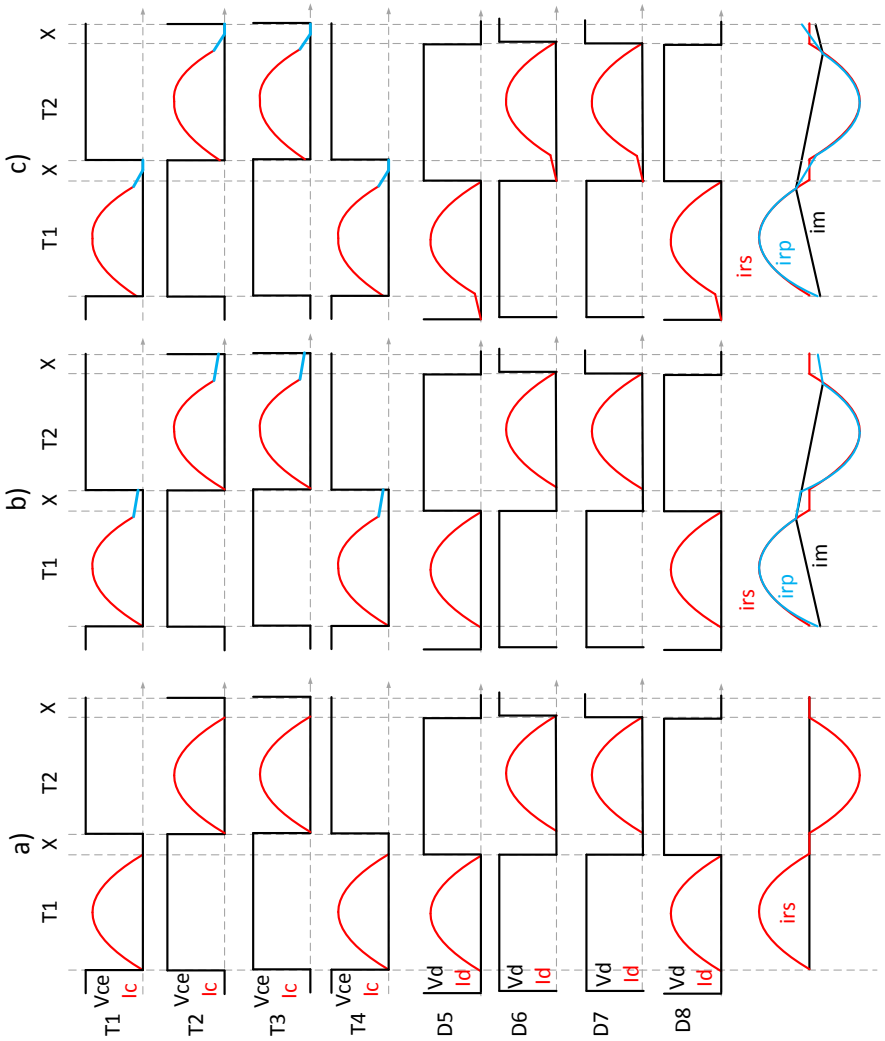


Fig. 15: Classic SRC device waveforms: a) Ideal waveforms, $L_m = inf$, $V_g - V_o = 0$, DCM1; b) Non-Ideal waveforms, $L_m = 50e-3$, $V_g - V_o = 0$, DCM1; c) Non-Ideal waveforms, $L_m = 50e-3$, $V_g \geq V_o = 0$, DCM1;

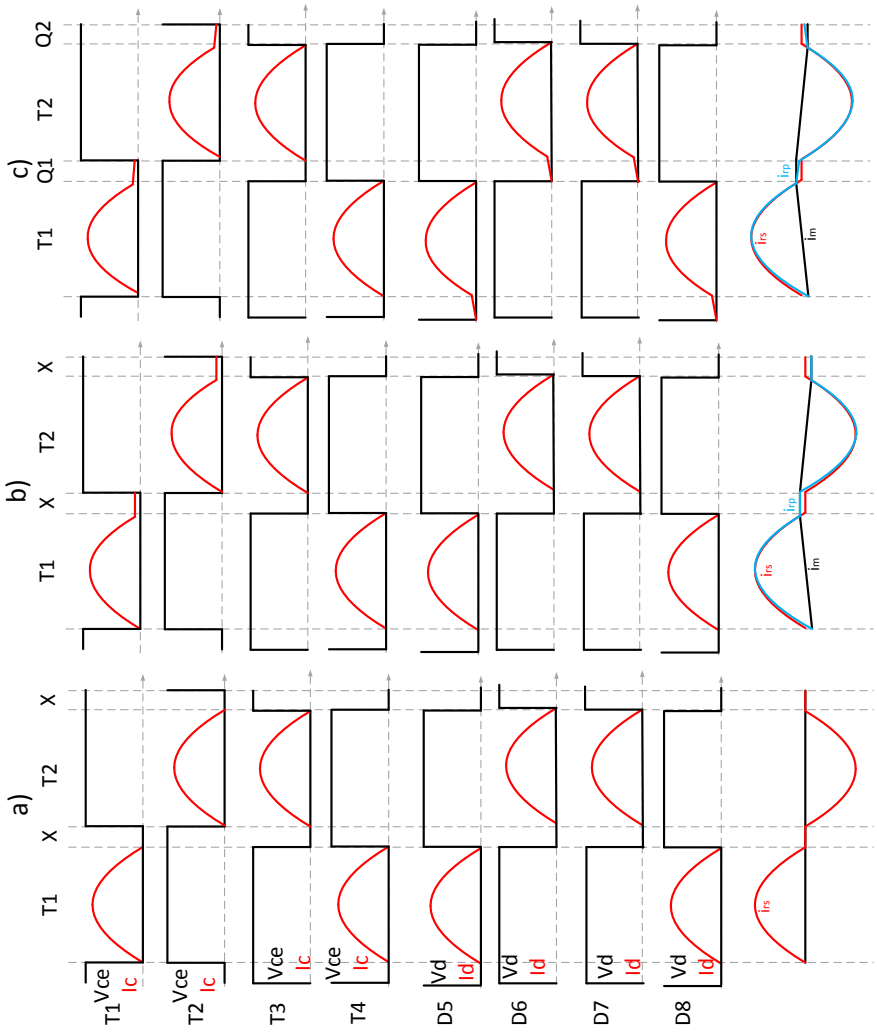


Fig. 16: SRC# device waveforms: a) Ideal waveforms, $L_m = inf$, $V_g - V_o = 0$, DCM1; b) Non-Ideal waveforms, $L_m = 10e-3$, $V_g - V_o = 0$, DCM1; c) Non-Ideal waveforms, $L_m = 10e-3$, $V_g \geq V_o = 0$, CCM1-Hybrid;

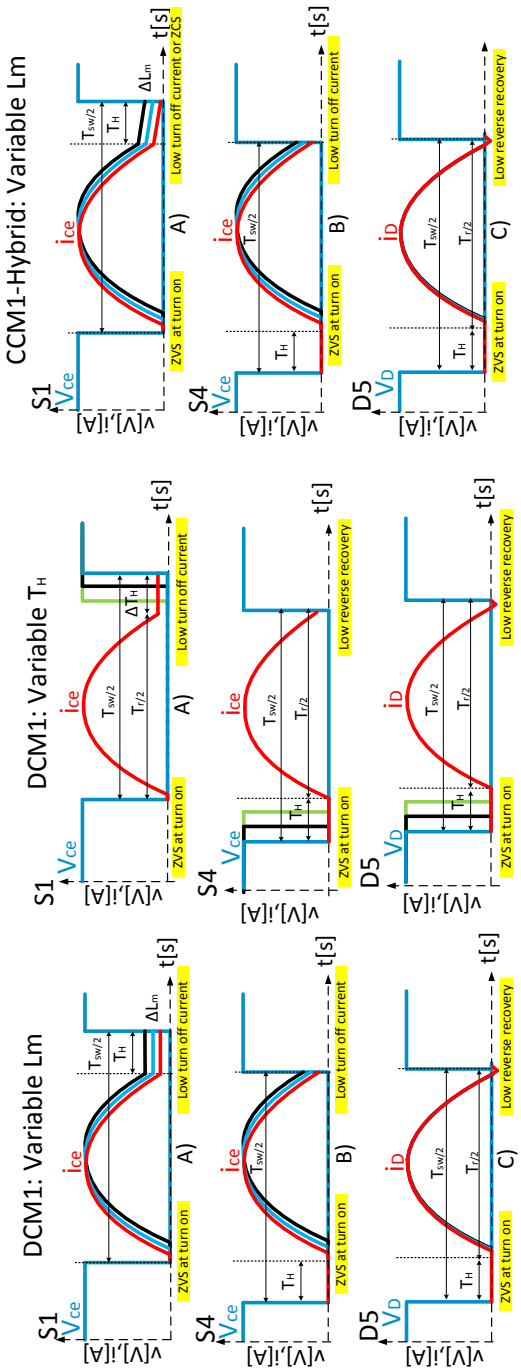


Fig. 17: SRC# device waveforms

SUMMARY

Offshore HVDC-connected wind farms promise reduced electrical losses, lower bill-of material cost and undiminished functionality with the condition the wind plant MV collection network becomes DC, rather than MVAC. One dearly missed building block that would enable the transition to a DC voltage collection, is the DC/DC converter for high power & high voltage (megawatss and kilovolts).The main objective of this thesis was investigation and development of a turbine DC/DC converter proof of concept. The selected topology is based on a single phase series resonant converter, operated with a new modulation scheme, which permits regulation of power from nominal level to zero, in presence of variable input and output DC voltage levels. The circuit was rearranged so that the LC tank is located on the rectifier side of the high-turns ration transformer combined with frequency control and phase shifted inverter modulation. The modulation scheme was entitled pulse removal technique and it keeps the transformer flux constant from nominal frequency down to DC, always in sub-resonant continuous or discontinuous conduction mode. A design guide line, suitable for a given range of specifications, in the megawatt (5 to 15 MW), kilovolt ($\pm$35 to $\pm$50 kV) and kilohertz (0.5 to 5.0 kHz) range is introduced, while medium voltage experimental setups are implemented for characterization of losses, control and voltage sharing.

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