Improved Design Methods for Robust Single- and Three-Phase ac-dc-ac Power Converters

Qin, Zian

Publication date:
2015

Document Version
Accepted author manuscript, peer reviewed version

Improved design methods for robust single- and three-phase ac-dc-ac power converters

by

Zian Qin

A Dissertation Submitted to
the Faculty of Engineering and Science at Aalborg University
for the Degree of Doctor of Philosophy in Electrical Engineering

May 2015
Aalborg, Denmark

Aalborg University
Department of Energy Technology
Pontoppidanstraede 101
Aalborg East, DK-9220
Denmark
Phone: +45 29 63 22 04
Fax: +45 98 15 14 11
http://www.et.aau.dk

Printed in Denmark by Uniprint

ISBN: 978-87-92846-57-0

Public Defence of PhD Dissertation

Thesis Title:

Improved design methods for robust single- and three-phase ac-dc-ac power converters

Ph.D. Defendant:

Zian Qin

Supervisor:

Prof. Frede Blaabjerg

Co-supervisor:

Prof. Poh Chiang Loh

Assessment Committee:

Prof. Zhe Chen (Chairman)

Department of Energy Technology
Aalborg University
Pontoppidanstraede 101
9220 Aalborg, Denmark

Prof. K. Gopakumar

Department of Electronic Systems Engineering
Indian Institute of Science
560012 Bangalore, India

Prof. Jinjun Liu

School of Electrical Engineering
Xi'an Jiaotong University
710049 Xi'an, China

Defence Date and Place:

Thursday, August 6, 2015
Pontoppidanstraede 101, Room 23, Aalborg University

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Thesis Title: Improved Design Methods for Robust Single- and Three-phase AC-DC-AC Power Converters

Name of the PhD student: Zian Qin

Name of supervisors: Prof. Frede Blaabjerg

Name of co-supervisors: Prof. Poh Chiang Loh

List of publication: Listed in § 1.5

This present report combined with scientific papers which are listed in § 1.5 has been submitted for assessment in partial fulfilment for the Degree of Doctor of Philosophy (Ph.D.) in Electrical Engineering. The scientific papers are not included in this version due to copyright issues. Detailed publication information is provided in § 1.5 and the interested reader is referred to the original published papers. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty of Engineering and Science, Aalborg University

Preface

This thesis is a summary of PhD project "Improved Design Methods for Robust Single- and Three-Phase AC-DC-AC Power Converters". The research work is supported mainly by China Scholarship Council (CSC) and partially by the Department of Energy Technology, Aalborg University, Denmark. Acknowledgements are given to these institutions, as well as the Center Of Reliable Power Electronics (CORPE) and Otto Mønsteds Fond, who supported me for test platform establishment and conference participation.

This research project was done under the supervision of Prof. Frede Blaabjerg and Prof. Poh Chiang Loh from the Department of Energy Technology, Aalborg University, Denmark. First and foremost, I would like to show my deepest gratitude to my supervisor, Prof. Frede Blaabjerg, for his professional and constructive guidance with his open-mindedness and earnestness during the PhD project. His encouragement supported me to get through the difficulties during the project one by one. His guidance not only help me to complete my PhD project but also deeply influence my research style, which I do believe will continuously support me in my career and through my future life. I would also show my appreciation to my co-supervisor, Prof. Poh Chiang Loh, for his patient guidance, his time to discuss the details with me and correct the papers for me. His guidance made the time of PhD much easier for me. Besides, I would thank my previous co-supervisor, Prof. Marco Liserre from Christian-Albrechts-Universität zu Kiel, for his guidance in the first year of my PhD, although short but helpful.

I would take this opportunity to also thank Prof. Rik De Doncker for his support during my study abroad in Institute for Power Generation and Storage Systems (PGS), RWTH Aachen University. The thanks will also go to the colleagues in PGS, especially Dipl.-Ing. Marco Stieneker, for their kind assistance.

I also want to thank all my colleagues from the Department of Energy Technology for the warm environment. Thank Dr. Yi Tang. His research spirit is impressive. The collaboration with him was although short but enjoyable. Thank Dr. Huai Wang for his constructive advice to my project. Thank Dr. Ke Ma for his passionate care to my project. Thank Dr. Xiongfei Wang, Dr. Yongheng Yang, and Dr. Dao Zhou for their kind help to my project. Best wishes to my friends - Helong Li, Yanjun Tian, Yanbo Wang, Cam Pham, Fan Zhou, Hui Liu, Rui Wu, Lexuan Meng, Tushar Batra, Min Huang, and all the other friends. We enjoyed the parties, the football matches, and even carnivals together. The life hence became more interesting and colorful. My appreciations are extended to John K. Pedersen, Tina Larsen, Corina Busk Gregersen, Eva Janik, Casper Jørgensen and Walter Neumayr for their assistance in different ways.

The sincerest gratitude goes to my parents and my sister for their endless love and support. Finally and most importantly, I would like to acknowledge my girlfriend Dan Wu for her support, concern and understanding.

Zian Qin

May, 2015
Aalborg Øst, Denmark

Abstract

After a century of fast developing, the society is facing energy issues again, e.g. the exhaustion of fossil fuel, emission caused air pollution, radiation leakage of nuclear generation, and so on. How to produce and use electricity in a more sustainable, efficient, and cost-effective way thus becomes a emerging challenge. Accordingly, installation of sustainable power generators like wind turbines and solar panels has experienced a large increase during the last decades. Meanwhile, power electronics converters, as interfaces in electrical system, are delivering approximately 80 % electricity to users. Their performances including cost, efficiency, reliability, and so on, therefore are more important concerns than they were. The objective of this thesis is to study and propose advanced design methods for robust ac-dc-ac converters, which are widely used interfaces in energy conversion system. The approaches for improving their performance, in terms of the voltage stress, efficiency, power density, cost, loss distribution, and temperature, will be studied. The structure of the thesis is as follows,

Chapter 1 presents the introduction and motivation of the whole project as well as the background, the emerging challenges, and the structure of the thesis. The main content of the thesis starts with single-phase converters: Chapter 2 and Chapter 3 propose new modulation methods for single-phase B6 and H6 converters, respectively, in order to retain the same dc-link voltage with two full-bridges connected back-to-back, and meanwhile improve the harmonics, control flexibility, and thermal distribution between the switches. Afterwards, active power decoupling methods for single-phase inverters or rectifiers that are similar to the single-phase ac-dc-ac converter, are studied in Chapter 4. With the proposed new active power decoupling method, the ripple power in the converter can be compensated in a more efficient and more compact way. Then, Chapter 5 changes the scope of the thesis to three-phase converters, and the nine-switch converter, as a reduced switch version of two three-phase full-bridges connected back-to-back, is studied. Application criteria of the nine-switch converter are investigated for reducing the relatively high stress introduced by the less number of switches. In Chapter 6 a rotating speed controller design method is proposed for improving the thermal loading of the three-phase wind power converter in a system level. The thesis is finally concluded in Chapter 7, before the proposal for the future research plan.

The contributions of this project include several approaches proposed for improved performance of ac-dc-ac power converters, and they can be categorized into three aspects as: control methods, auxiliary circuits, and application criteria. The details are as follows: 1. new modulation schemes of single-phase B6 and H6 converters for improved performance, 2. an optimal active power decoupling approach for kW-scale single-phase converters to achieve high power

density and high efficiency, 3. application criteria of nine-switch converters for improved performance in terms of loss and temperature, 4. a new rotating speed controller design method for power levelling of wind power converters.

Danske Abstrakt

Efter et århundrede med hurtig udvikling, er det samfund står over for energispørgsmål igen, f.eks konsumption af fossile brændstoffer, emission forårsagede luftforurening, stråling lækage af kernekraft, og så videre. Hvordan man producerer og bruger energi på en mere bæredygtig, effektiv og omkostningseffektiv måde bliver således en spirende udfordring. I overensstemmelse hermed har installation af bæredygtige el-generatorer som vindmøller og solpaneler oplevet en stor stigning i de seneste årtier. I mellemtiden, power elektronik omformere, som grænseflader i elektriske system, der leverer ca. 80 % elektricitet til brugerne. Deres præstationer, herunder omkostninger, effektivitet, pålidelighed, og så videre, er derfor mere vigtige bekymringer, end de var. Formålet med denne afhandling er at undersøge og foreslå avanceret design metoder til robuste AC-DC-AC omformere, der er almindeligt anvendt grænseflader i energi konvertering system. De metoder til at forbedre deres resultater med hensyn til spændingen stress, effektivitet, effekttæthed, omkostninger, fordelingen af tab samt temperatur, vil blive undersøgt. Strukturen i afhandlingen er som følger,

Kapitel 1 præsenterer indførelse og motivation af hele projektet samt baggrunden, de nye udfordringer, og strukturen af afhandlingen. Hovedindholdet af afhandlingen starter med enfasede omformere: kapitel 2 og kapitel 3 foreslå nye graduering metoder til enfasede B6 og H6 omformere henholdsvis for at bevare den samme DC-link spænding med to fulde broer forbundet tilbage -til-back, og i mellemtiden forbedre harmoniske, kontrollerer fleksibilitet og termisk fordeling mellem kontakterne. Bagefter er aktive magt afkobling metoder til enfasede invertere eller ensrettere, der ligner den enfaset AC-DC-AC konverter, undersøgt i kapitel 4. Med den foreslåede nye aktive effekt afkobling metode, rippeleffekten i konverteren kan kompenseres på en mere effektiv og mere kompakt måde. Derefter kapitel 5 ændrer omfanget af afhandlingen til trefasede konvertere, og ni-switch-konverter, som en reduceret switch-version af to trefasede fuld broer tilsluttet back-to-back, der er undersøgt. Anvendelseskriterier i de ni-switch konverter undersøges for at reducere den relativt høje spænding indført ved mindre antal omskiftere. I kapitel 6 foreslås en roterende hastighed controller design fremgangsmåde til forbedring af den termiske belastning af den trefasede vindkraft konverter i et system-niveau. Specialet er endeligt afsluttet i kapitel 7, før forslaget til den fremtidige forskning planen.

Bidragene fra dette projekt omfatter flere tilgange foreslået til forbedret ydeevne af AC-DC-AC strøm omformere, og de kan kategoriseres i tre aspekter som: kontrolmetoder, ekstra kredsløb, og anvendelse kriterier. Detaljerne er som følger: 1. nye graduering ordninger af enfasede B6 og H6 konvertere til forbedret ydeevne, 2. en optimal aktiv magt afkobling tilgang til kW-skala-fasede omformere at opnå høj effekttæthed og høj effektivitet, 3. anvendelseskri-

terier af ni-switch konvertere til forbedret ydeevne i form af tab og temperatur, 4. en ny rotationshastighed controller design metode til magt nivellering af vindkraft omformere.

Contents

Part I

Preamble

1 Introduction

1.1 Background and motivation

Due to the fast development of society, the demand for energy is growing more and more prominent. The fossil fuel resource may still afford for consumption in the future centuries, as the shale gas technology matures. However, the requirement of a low Cost Of Energy (COE) is becoming more and more urgent, especially considering the by-product of energy utilizaiton like the air pollution or nuclear leak. More renewable and clean energy production in power generation system is thus required. Ambitious targets have been set, e.g. the *DANISH ENERGY AGREEMENT* [1], where 50 % of electricity consumption will be from wind power production in 2020, and the *EUROPE 2020* [2], where in 2020 the greenhouse gas emissions will be 20% lower than 1990, 20% of energy will be from renewables, and energy efficiency will be increased by 20%.

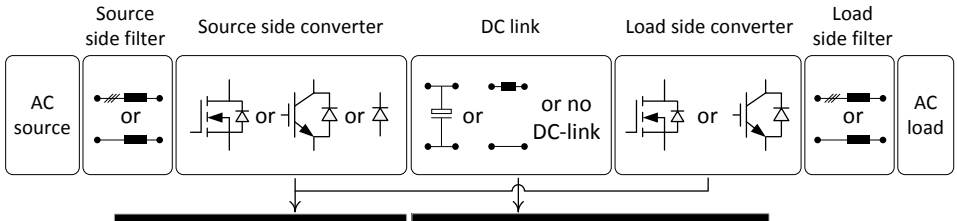
Meanwhile, power electronics, as the interface between the source and load in the electrical system, enable efficient and flexible conversion of the electrical power by taking advantage of the innovations in active and passive components, circuit topologies, control strategies, control circuits, and system integrations [3–10]. As a result, more than 70% of electricity is processed through power electronics in the modern society, which is likely to get to 80 % in 2015 [11]. Therefore, power electronics play a very important role in reducing COE. As interfaces, the COE introduced by the power converters can be generally illustrated as following,

$$COE_{PE} = \frac{Price_{energy} \times \int_0^{T_{life}} P_{in}(t) \times (1-\eta(t))dt + Cost_{installation} + Cost_{maintenance}}{\int_0^{T_{life}} P_{in}(t) \times \eta(t)dt} \tag{1.1}$$

where T_{life}, $P_{in}(t)$, and $\eta(t)$ are the service life, input power, and efficiency of the converter, respectively. As seen, from the power electronics point of view, the cost of energy can be reduced based on some traditional concerns like reducing the installation cost and increasing the efficiency of the converters. Besides, there are some new concerns in terms of the maintenance, the service life, and the aging of the converter. The service life is supposed to be prolonged to dilute the installation and maintenance cost in COE. The aging of the converter means degradation of performance including efficiency, which should be relieved in order to guarantee a high efficiency through the whole service life of the power converter. All these concerns require a robust design of the power converter. Therefore, this project will study and propose new methods to develop robust power converters, and the focus will be put on single- and three-phase ac-dc-ac power converters, which are widely used in applications like in wind power generation, motor drives, UPS, power conditioners, and so on [12–20].

1.2 State of the art

1.2.1 Main challenges



Active components	Passive components
1. Switch count	1. Voltage and current stress (capacitor)
2. Voltage and current stress	2. Loss (inductor)
3. Loss	3. Lifetime (capacitor)
4. Temperature/cooling/lifetime	4. Volume (capacitor, inductor)
5. Control flexibility	
a. amplitude	
b. phase	
c. frequency	

Figure 1.1: *Main concerns in ac-dc-ac power converter design.*

An ac-dc-ac power converter is composed of the source and load side converters, the source and load side filters, and dc-link, as shown in Fig. 1.1. Accordingly, the main concerns in the design phase can be categorized into two parts, in terms of the challenges in active and passive components. More details are illustrated as follows,

Power switches:

a. switch count

The number of switches will influence not only the complexity of the topology but also the number of gate drivers, and thereby the failure possibility, cost, and volume of the gate drivers.

b. voltage and current stresses

Voltage and current stresses determine the rating of the power switches and also the circuit topology, where high voltage or current applications may require multi-level or multi-phase topologies. Besides, the voltage and current stresses have impact on the power losses and current ripples of the converter.

c. losses

The total power loss will directly affect the efficiency of the power converter, and thereby the cost of energy, as illustrated in (1.1). Moreover, power losses are the main challenge to the cooling system design including the type, complexity, cost and volume of the cooling system.

d. temperature

The temperature of the converter closely relates to its power losses and its thermal design, but their concerns are different. From a temperature point of view, its distribution, the highest value and cycling are normally considered instead of its total value. Because the temperature cycling will accelarate the aging of the power switches, the temperature distribution will influence the consistency of the power switches' aging, while the highest temperature will affect the design capacity of the power switches including the cooling system.

e. control flexibility

The control flexibility includes the control of the three parameters of the ac side voltage or current, in terms of its amplitude, phase and frequency. Such control flexibility is required by some applications like in Power Factor Correction (PFC) circuits, variable-speed drives, and so on. The cost of the converter may increase in order to achieve a high control flexibility, but on the other hand the power source is better used and the load is better fed by the generated power.

DC link:

a. voltage and current stresses

The capacity of the dc-link capacitor is normally designed according to the power imbalance between the source and load. Despite that, in high power applications, the dc-link electrolytic capacitors are normally overdesigned to handle the high current ripple. Thus, the current stress will affect the capacity of the dc-link capacitor. The current stress can also affect the capacity

of the dc-link inductor if used. In contrast, the voltage will influence the voltage rating of the dc-link capacitor.

b. losses

The losses of the dc link are normally negligible unless a dc-link inductor is used. In that case, the circuit topology becomes a current source converter instead of a voltage source converter with only a dc-link capacitor. The current source converters have been studied for high power applications, but the voltage source converters are still the dominant choice.

c. lifetime

The electrolytic capacitor in the dc-link is a weak point of the converter, which may encounter failure earlier than the other components. The dc-link capacitor is normally overrated in order to reduce the stress for each unit. Another solution is to use film capacitor to replace the electrolytic capacitor. But, both of them will increase the cost and volume of the dc link, and therefore lead to a lower power density.

d. volume

The wide-band gap power switches are developing fast e.g. SiC and GaN, which can achieve lower losses and higher switching frequency. Volumes of the heatsink and ac-side power filter can hence be shrinked in the design. However, the dc-link typically does not benefit from it, and the dc-link still keeps the volume and becomes the barrier to achieve a high power density.

1.2.2 Circuit topologies

In ac-dc-ac converters, the diode rectifiers are normally applied as the front-end converter to passively convert the ac voltage to a dc voltage. An inverter connected to the dc link is then used to generate the ac voltage or current with specific amplitude, phase, and frequency. The circuit is cost-efficient and with less control complexity. However, the bidirectional power flow and front-end control flexibility cannot be realized, which are required by most of the high power applications and even some advanced applications with low power. To meet the requirements of these applications, Full-Bridge Back-To-Back converters (FB-BTB) can be utilized, as illustrated in Fig. 1.2(a) (single-phase) and Fig. 1.3(a) (three-phase). The FB-BTB converters have a symmetrical topology, which thus allows the input and output converters to be modulated independently. Such independence introduces the following advantages including evenly shared thermal distribution among switches, minimum dc-link voltage, and independent frequency control between the input and output converters. However, these superiorities do not stop the study of the other derived topologies [16, 21–34].

a. Single-phase converters

The B6 converter, which is normally used for the three-phase rectifier or inverter, has been used as a single-phase ac-dc-ac converter [16, 17, 35], as seen in Fig. 1.2(b). Two of the three ac terminals are connected to the ac source and load, respectively. The last one is then shared

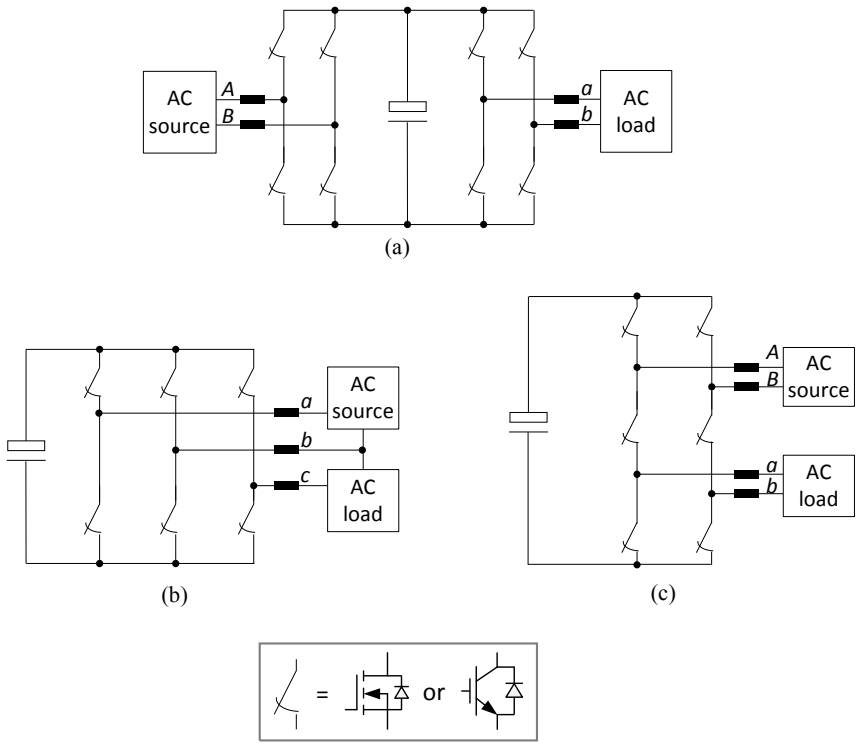


Figure 1.2: *Single-phase ac-dc-ac converters. (a) full-bridge back-to-back converter (b) B6 converter (c) H6 converter*

by both of them. With such a configuration, the number of switches is two less than the single-phase FB-BTB. Thus, the cost, volume, power density, and failure rate are expected to be improved. However this is not always correct unless some criteria are followed. One of them relates to the dc-link voltage. Because a common leg is shared between the source and load, the dc-link voltage needs to be increased or even doubled if the source and load operate with different fundamental frequencies. Since a double dc-link voltage will introduce significantly increased voltage stress, thereby also power loss, and current ripple, the different frequency mode is better to be avoided. In other words, UPS and voltage regulators, where the input and output have the same frequency, are more appropriate applications for the B6 ac-dc-ac converter [16,17]. Besides, the voltage stress, current stress, efficiency, and thermal distribution may be improved by following some criteria, to be evaluated in this thesis.

Another switch-reduced single-phase ac-dc-ac converter is also composed of six power

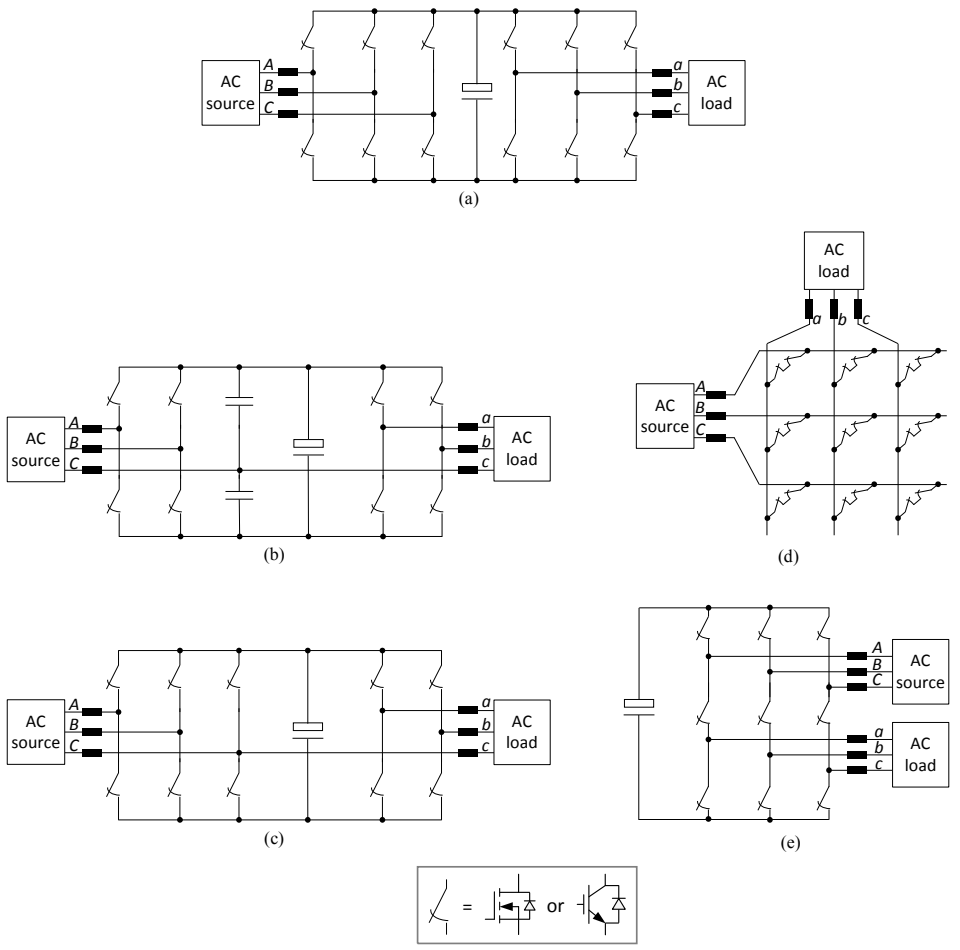


Figure 1.3: *Three-phase ac-dc-ac converters. (a) full-bridge back-to-back converter (b) with a common flying capacitor leg (c) with a common half-bridge leg (d) matrix converter (e) nine-switch converter*

switches, as shown in Fig. 1.2(c). As these switches are located in two legs, forming the shape of the letter 'H', it is referred to as the 'H6' converter in this thesis. The H6 converter is a derived topology of the nine-switch converter proposed recently [13, 15, 36, 37]. Instead of sharing a common leg between the input and output, the nine-switch converter puts the input on the top of the output and thus a switch is omitted in each phase-leg. Totally, there are only

six switches instead of eight forming a single phase (see Fig. 1.2(c)) and nine switches instead of twelve forming three phases (see Fig. 1.3(e)). The expected advantages are similar to those of the B6 ac-dc-ac converter as mentioned above, but some constraints cannot be avoided, and the dc-link voltage utilization is again a critical one. The operation of the H6 converter requires that the reference of the upper terminal is always above the reference of the lower one. Thus, a common frequency between the upper and lower terminals is necessary in order to achieve a high utilization of the dc-link voltage. Besides, the upper and lower terminals are required to be in-phase or to have only small phase displacement in order to avoid a significant increase of the dc-link voltage. Further, with the control methods described in the literature, the middle switch has much higher temperature than the upper and lower ones [13, 38] as more current is flowing through it. These constraints will significantly shadow the advantages of the H6 converter due to its reduced switch count. Part of the thesis is therefore directed at breaking or relieving these constraints and introducing more flexibility to the H6 converter.

b. Three-phase converters

The three-phase FB-BTB has more legs than the single-phase case, and thus has more derived possibilities, as seen in Fig. 1.3(b), (c), (d) and (e). Two legs from the input and output are merged together as a common-leg with only two switches in [40]. The common-leg can also be replaced by two flying capacitors [39]. Sharing of the common leg between the input and output will introduce a constraint to the dc-link voltage and also form a highly asymmetrical structure, as experienced by the single-phase B6 converter. Uneven loss and thermal distribution among the switches will then result. The matrix converter is another derived topology of the three-phase FB-BTB, which instead of reducing the number of power switches, gets rid of the bulky electrolytic capacitors placed at the dc-link [41,42]. The reliability and power density are thus claimed to be enhanced. However, due to the elimination of the dc-link capacitor, which can be considered as an energy buffer, the interference between the input and output becomes more significant and the fault tolerant ability is thus reduced. Further, the nine switches used by the matrix converter are bidirectionally controlled power switches, which with the current technology, need two IGBTs or Mosfets connected in series with either a common collector or emitter. The total number of unidirectional switches is thus increased from twelve to eighteen. All these constraints form a large challenge hindering the development of matrix converters.

The nine-switch converter looks like the matrix converter (see Fig. 1.3(e)), which is also composed of nine but unidirectionally controlled switches [12,13,15,36–38,43–45]. Besides, the dc-link capacitor is retained, which in turn allows independent control of the input and output. The same operational principle applies to the nine-switch converters, where the references of the upper terminals must be always above the lower ones. The constraint related to the dc-link voltage is also similar to that faced by the H6 converter: a common frequency and a small phase

displacement between the input and output are required if a lower dc-link voltage is demanded. Besides, a higher temperature is experienced by the middle switch in this configuration. How to relieve these constraints and highlight the advantages of the nine-switch converter thus becomes an important issue covered by the scope of this thesis.

1.2.3 The potential approaches

a. Modulation strategies

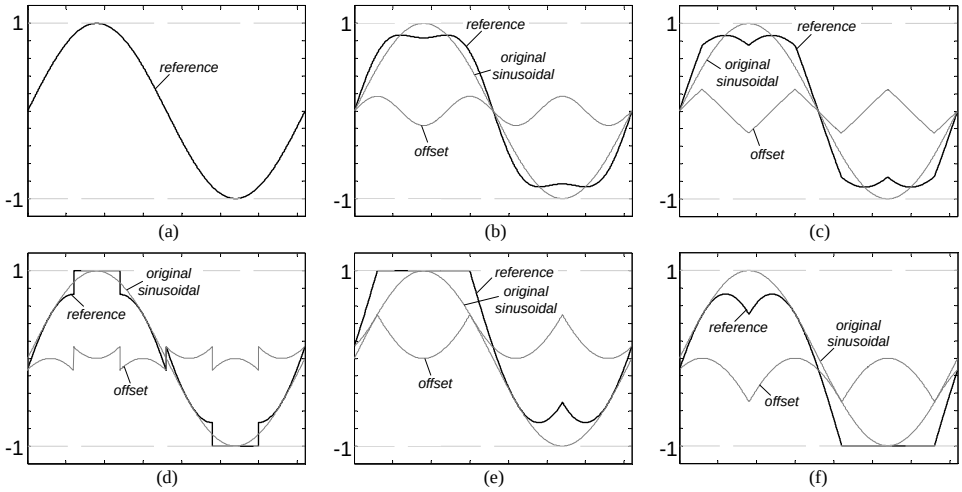


Figure 1.4: *Modulation schemes for three-phase converters [46, 47]. (a) SPWM (b) third hamonics injection PWM (THIPWM) (c) SVPWM (d) DPWM1 (e) DPWMMAX (f) DPWMMIN*

Different modulation schemes applied to a converter are known to produce different performance features in terms of harmonics, power loss and maximum modulation indexes [38,46–54]. They are thus potential approaches that can lead to robust ac-dc-ac converters. Despite their differences, most modulation schemes are, to a great extent, inter-related since they are derived from the same basic sine-triangle comparison, which is also known as carrier-based or sinusoidal pulse-width modulation (SPWM). The derivations are almost always done by adding a common offset to the modulating sine references used by the basic SPWM [46, 47], as seen in Fig. 1.4. These schemes can alternatively be analyzed by using explicit space vectors [50, 51], which if implemented by using built-in timers of digital signal processors, are not greatly different from sine-triangle comparison. The same sine-triangle comparison and adding of common offset can also be applied to a single-phase dc-ac or ac-dc system, but are comparably less studied since

the choices for offset are not many. The performance advantages expected from modulation modifications for a single-phase system are therefore not as wide ranging as for a three-phase system. Although this is generally true, there may be an exception with single-phase ac-dc-ac systems implemented using reduced-switch topologies, e.g. single-phase B6 and H6 converters. Less switches in these topologies usually lead to interdependencies between their ac inputs and outputs, and hence gives a different set of performance requirements, which is presently not thoroughly discussed and thus will be studied in this thesis.

b. Active power decoupling methods

Active power decoupling (APD) is another potential approach for improving the design of a single-phase system. In general, APD uses inductors or film capacitors with smaller capacitance, instead of the bulky and unreliable dc-link electrolytic capacitors, for compensating power oscillation between input and ouput of the converter, as illustrated in Fig. 1.5. High power density and reliability can then be achieved [27–29, 55–69]. Although it is mostly studied for single-phase ac-dc or dc-ac systems in the literature, it can also be used with a single-phase ac-dc-ac system [25], where power oscillation may also exist when the second-order items of the input and ouput power are not in phase.

APD, when implemented, will also involve usually an auxiliary circuit composed of power switches and energy storage devices like capacitors or inductors. Its efficiency is therefore poorer and hence a main concern in real applications. In particular, the inductor-based APD loses its competitiveness because of its sizable volume and inherent high losses, including core and copper losses [56, 57]. The film-capacitor-based APD is more attractive from an efficiency and power density point of view. Most of them in the literature are of the shunt type [27–29, 59–69], and can broadly be categorized as dc decoupling [59–65] and ac decoupling [27, 29, 66–69] according to the polarity of the decoupling capacitor voltage, as illustrated in Fig. 1.5. However, the above mentioned literatures did not discuss the performance of APD circuits in terms of power density and efficiency. The minimum capacitance required for APD was subsequently analyzed in [66], but the volume of film capacitors used for APD is not discussed, even though it is an important indicator for determing power density. Thus, the scope of this thesis also aims to provide a benchmark evaluation of existing APD circuits. The evaluation considers commercially available film capacitors, various auxiliary circuit topologies, and control strategies adopted for power decoupling.

c. Energy storage methods

The three-phase FB-BTB becomes mature in applications, but some emerging challenges like power and thermal cycling when used in wind power application are drawing renewed attention [70–76]. Wind power has achieved a large penetration of the electricity consumption in some countries after fast development for many decades [3, 5, 77], e.g., 53% is experienced in Spain [78] and more than 40% in Denmark. As a result, the fluctuation of wind power becomes

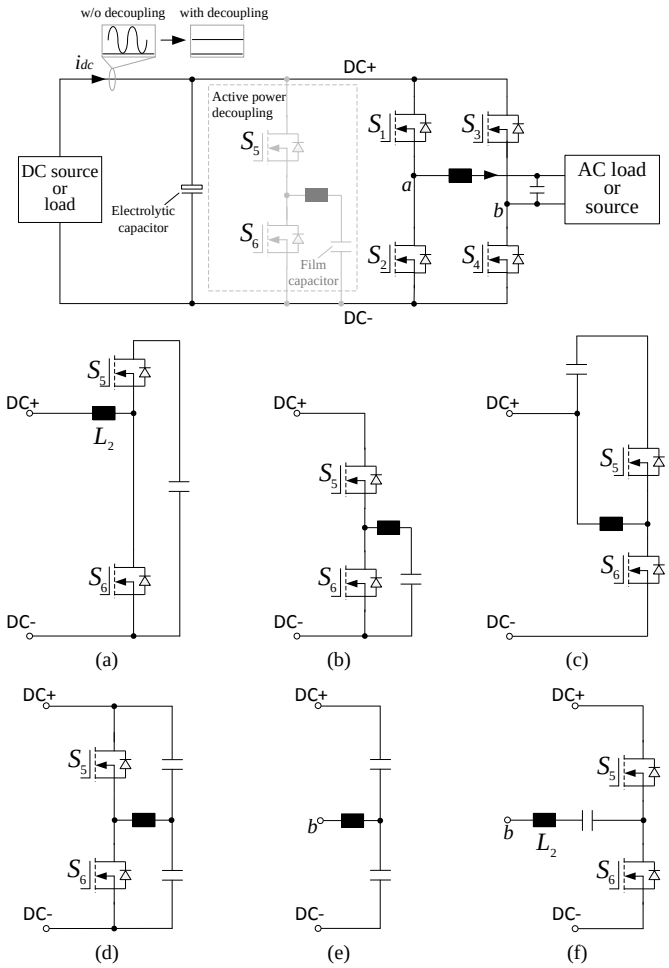


Figure 1.5: *The basic active power decoupling scheme in single-phase converters with the typical (a) boost-type (b) buck-type (c) buck-boost type dc decoupling methods and (d) symmetrical H-bridge (e) symmetrical passive half-bridge (f) symmetrical active half-bridge ac decoupling methods.*

an important issue, because it will not only influence the stability of the power system, but will also reduce the reliability of the wind power converter as the load fluctuates [79–83].

To smooth the power fluctuations, addition of Energy Storage Systems (ESSs) like flywheels, supercapacitors, and batteries [70,84–86] to the wind power converters has been proposed. The

main efforts in this method are put into the topologies, control strategies, and size evaluation of the ESS [71,72,87]. The high power generation efficiency is retained and the power fluctuation can be mitigated significantly as long as a large enough ESS is introduced. A wind turbine with ESS integrated is already commercially available [88]. Despite, there exist some drawbacks, e.g. the power fluctuations and thermal excursions in the generator side converter cannot be improved by the ESS connected to the dc-link, and the cost of ESS for large-scale wind turbines is still very high [89].

Pitch angle control and dc-link voltage control have thus been studied for power levelling [73, 90, 91]. However, changing the pitch angle below the nominal wind speed will lose power generation considerably. Controlling the dc-link voltage could be an effective approach for low-voltage-ride-through operation, but its impact on power levelling is normally negligible. Another possibility for power levelling in large-scale wind power systems is the rotor, which has a large inertia of moment for storing a large amount of energy like in an ESS [92–98]. This inertia energy is indirectly controlled by regulating the rotating speed of the wind turbine. The related control strategies were roughly studied in [92,93], before more advanced control methods like Fuzzy Control and Model Predictive Control were applied for power levelling [94, 95] to improve the performance and maintain stability of the rotor speed. In [99], a transfer function from the wind speed to the electrical power was derived to illustrate the power filtering effect and analyze the stability of the controllers. The transfer function in the frequency domain made the filtering effect much easier to be understood and the conclusion that the power levelling was a matter to design the slope between the electrical power and rotating speed was very valuable. Nevertheless, an optimal design of the rotating speed control in the frequency domain was not given. Some details were also ignored in the derivation of the transfer function, in terms of the MPPT controller, and the impact of the rotor inertia. Moreover, influence on the torque was not considered, which may be significantly changed by the power levelling strategies. It is therefore another important topic investigated in the thesis.

d. Application criteria

The reduced-switch converters, e.g. nine-switch converters, H6 converters, and single-phase B6 converters, inevitably encounter constraints. Since they have common legs and thereby modulation interference between their input and ouput, a higher dc-link voltage is required, which in the worst case is doubled that of the full-bridge converter. In order to achieve a lower dc-link voltage, these converters are suggested to be used in their common-frequency mode with a small phase displacement between their input and output, e.g. on-line UPS [13,17], and ac-ac power conditioners [12,16]. Even operating in this relatively more appropriate mode, the reduced-switch converters will still suffer uneven shared loss distribution, which may lead to inconsistent aging of the power devices in the converter and thereby reduction of the converter reliability [101–104]. Application criteria of these reduced-switch converters for

improved performance are therefore formulated in this thesis as another contribution.

1.2.4 Thesis hypothesis and objectives

As ac-dc-ac converters are widely used as interfaces in energy conversion system, they play an important role in reducing the cost of energy. Therefore, the objective of this thesis is to study and propose advanced design for robust ac-dc-ac converters, where the voltge stress, efficiency, energy density, cost, loss distribution, and thermal performance of the converters are all taken into account. Procedurally, this objective will be achieved by dealing with several research questions listed as follows:

- *What are the application criteria for ac-dc-ac converters in order to achieve relatively low stresses and better performance?*
- *How to generate advanced control strategies for further improving the performance of ac-dc-ac converters?*
- *How to use auxiliary circuits for improving the performance of ac-dc-ac converters in a cost-effective manner?*

1.3 Project limitations

Besides the single- and three-phase ac-dc-ac converters considered in the thesis, there are many other topologies that are not possible to be included in the scope of this thesis. Further, the proposed methods in this thesis are analyzed based on general ac-dc-ac power converters. Although appropriate applications are suggested, like the UPS, voltage regulators, and power conditioners, the proposed methods have not been tested under a real mission profile of a specific application. Besides, the performance of the converters with the proposed methods under fault conditions have not been studied, even though they can occur in real applications. Reliability of the converters is another aspect that is not studied thoroughly in the thesis.

1.4 Thesis outline

This thesis is divided into two sections: Section I – Report and Section II – Publications. Section I is a summary report of the work done throughout the research, it contains 4 parts and 7 chapters. Fig. 1.6 gives an overview of the thesis.

The first part - *"Preamble"* contains only *Chapter 1*, which presents the introduction and motivation of the whole project as well as the background, emerging challenges, and structure of the thesis.

The second part - *"Single-Phase AC-DC-AC converters"* covers three chapters. *Chapter 2* and *Chapter 3* propose new modulation methods for single-phase B6 and H6 converters,

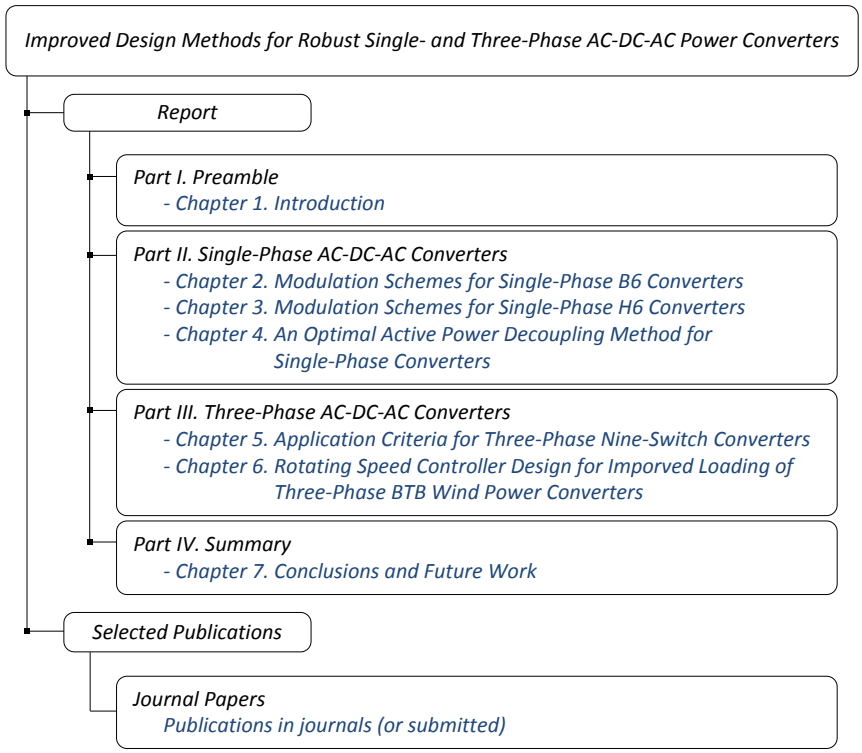


Figure 1.6: *Thesis structure and covered topics.*

respectively, to retain the same dc-link voltage as the HB-BTB. At the same time, thermal distribution between switches, harmonics, and control flexibility are also considered. *Chapter 4* studies various active power decoupling methods for the circuits similar to the single-phase ac-dc-ac converter, with which the ripple power in the converter can be compensated in a more efficient and higher power density way.

The third part - *"Three-Phase AC-DC-AC Converters"* is composed of two chapters. *Chapter 5* studies the nine-switch converter, which is a reduced-switch version of the FB-BTB. Because of its less components compared to the FB-BTB, the nine-switch converter encounters higher stresses if existing control schemes in the literature are applied. Application criteria of the nine-switch converter are thus investigated to reduce the stresses. Afterwards, *Chapter 6* proposes a rotating speed controller design method for improved loading in the FB-BTB wind power converter.

The fourth part - *"Summary"* has only *Chapter 7*, which gives the conclusions and contri-

butions documented in the thesis as well as some proposals for future research.

1.5 List of publications

The obtained results of this thesis are disseminated via a number papers, which are published or submitted in journals. A list of the papers is given below:

Journal Papers

J1. **Z. Qin**, P.C. Loh and F. Blaabjerg, "Application Criteria for Nine-Switch Power Conversion Systems with Improved Thermal Performance," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4608-4620, Aug. 2015

J2. **Z. Qin**, P.C. Loh, A.S. Bahman and F. Blaabjerg, "Evaluation of current stresses in nine-switch energy conversion systems," *IET Power Electron.*, vol. 7, no. 11, pp. 2877-2886, 2014.

J3. **Z. Qin**, F. Blaabjerg, and P.C. Loh, "A Rotating Speed Controller Design Method for Power Levelling by Means of Inertia Energy in Wind Power Systems," *IEEE Trans. Energy Convers.*, vol. 30, No. 3, pp. 1052-1060, 2015.

J4. **Z. Qin**, P.C. Loh, and F. Blaabjerg, "Modulation Schemes with Enhanced Switch Thermal Distribution for Single-Phase AC-DC-AC Reduced-Switch Converters," *IEEE Trans. Power Electron.*, early access, DOI: 10.1109/TPEL.2015.2451733, 2015.

J5. **Z. Qin**, P.C. Loh, and F. Blaabjerg, "Modulation Schemes for Single-Phase B6 Converter with Two Asymmetrical Terminal Voltages," *IEEE Trans. Industrial Electron.*, early access, DOI: 10.1109/TIE.2015.2464296.

J6. **Z. Qin**, Y. Tang, P.C. Loh and F. Blaabjerg, "Benchmark of AC and DC Active Power Decoupling Circuits for Second Order Harmonic Mitigation in Single-Phase Inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, under review.

Since these papers provide technical explanations and validation results for the ***Report*** of this thesis, the relationship between the publications listed above and the chapters of this thesis is summarized in Table 1.1, in order to give a better understanding of the research project.

Table 1.1: *Relationship between publications and chapters of the report.*

Chapter No.	Chapter Title	Relevant Publications
1	**Introduction**	-
2	**Modulation Schemes for Single-Phase B6 Converters**	J4,J5
3	**Modulation Schemes for Single-Phase H6 Converters**	J4
4	**Benchmark Design of Active Power Decoupling for Single-Phase Converters**	J6
5	**Application Criteria for Three-Phase Nine-Switch Converters**	J1,J2
6	**Rotating Speed Controller Design for Improved Loading of Three-Phase BTB Wind Power Converters**	J3
7	**Summary and Outlook**	-

Part II

Single-phase ac-dc-ac converters

The intention of this part is to study two promising single-phase ac-dc-ac converters using reduced switches. They are the B6 converters in *Chapter 2* and H6 converters in *Chapter 3*. New modulation schemes will also be subsequently proposed for them. The proposed schemes help the converters to retain their low dc-link voltages, reduce their current ripples, and achieve better thermal spread among their switches. Besides, the circuits similar to single-phase ac-dc-ac converter, normally named as active power decoupling, are investigated in *Chapter 4*. The second-order power ripple inherently exists in single-phase inverters. To compensate it and at the same time achieve high power density and efficiency, an improved design is necessary, and it is comprehensively studied. Simulation and experimental results have demonstrated the intended performances, hence verifying the analyses presented in the chapters.

2 Modulation schemes for single-phase B6 converters

Modulation methods can be used to effectively improve the performance of the power converters, e.g. the DC link voltage utilization, the harmonics, the power loss and so on. Modulation methods of B6 converters operating in three-phase balance mode have been well stuided, like the widely used SPWM, SVPWM, and 60^o-DPWM, while the single-phase mode still misses comprehensive investigation and it is studied in this chapter as following.

2.1 B6 converter

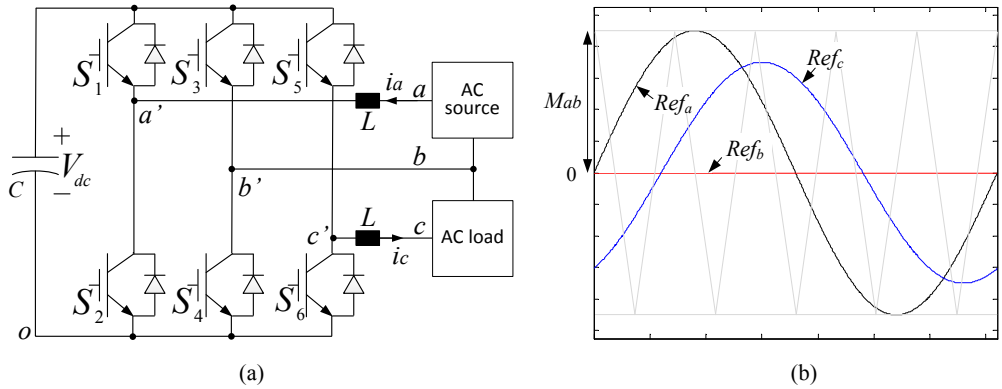


Figure 2.1: *Illustrations of (a) single-phase B6 converter and (b) its simple reference-carrier arrangement.*

The single-phase B6 converter is shown in Fig. 2.1(a), where a shared phase-leg between the source and load can clearly be seen. Thus the number of power devices is shrinked from eight to six compared with the two full-bridges connected back-to-back. The current flowing through this phase-leg is given by the sum of return currents from the source and load, which in most cases, will cancel each other prominently. This cancellation is an advantage of the B6 converter, which must usually be present before the B6 converter will be considered for single-phase applications. As a single-phase converter, the B6 converter must be modulated accordingly. The simplest reference-carrier arrangement that can be used is shown in Fig. 2.1(b). Expressions for the references (Ref_a, Ref_b, and Ref_c) and their generated voltages

(v_{ab} and v_{cb}) at the converter terminals are given in (2.1),

$$\begin{aligned} &Ref_a = M_{ab}sin(\omega_1 t), \quad Ref_b = 0, \quad Ref_c = M_{cb}sin(\omega_1 t + \varphi_1) \\ &v_{ab} = 0.5V_{dc} \times M_{ab}sin(\omega_1 t), \quad v_{cb} = 0.5V_{dc} \times M_{cb}sin(\omega_1 t + \varphi_1) \end{aligned} \tag{2.1}$$

where M_{ab} and M_{cb} are the modulation indexes, ω_1 is the angular fundamental frequency, and φ_1 is the phase between the two generated voltages. The main feature of the arrangement is a simple zero reference assigned to the shared phase-leg, which will certainly help if the input and output frequencies are different. The zero reference will however burden the converter unnecessarily if the two frequencies are similar like assumed in (2.1). More specifically, the dc-link voltage needed by the B6 converter will be doubled compared with what is needed by two full-bridge converters connected back-to-back, if the arrangement shown in Fig. 2.1(b) is used for modulation. This doubled dc-link voltage and its accompanied higher stresses will usually render the B6 converter as an unattractive converter even though it uses two less switches than the two full-bridges. The reference-carrier arrangement shown in Fig. 2.1(b) is therefore not recommended, if the B6 converter operates with a single common frequency.

2.2 Continuous modulation

2.2.1 Centered modulation

Referring to (2.1) and Fig. 2.1(b), the relative placement of the three references, treated as a whole, within the carrier band does not have to be fixed so long as their vertical spacing and sequence produce the desired ac voltages v_{ab} and v_{cb} in (2.1). Their relative placement can hence be varied to create different performance advantages for the B6 converter. This is similar to the addition of triplen offset to a three-phase converter, but with an asymmetry introduced. The modulation objectives expected from a single-phase B6 converter may therefore differ, even though some like keeping the converter dc-link voltage low remains unchanged. The converter dc-link voltage can indeed be minimized by centering the three references, treated as a whole, along the vertical axis. In other words, it means the maximum and minimum references must have the same absolute magnitude, but of opposite polarities. Such placement can be realized by adding a common offset $M_{off,C1}$ to (2.1), in order to give those modified references Ref_a^C, Ref_b^C and Ref_c^C in (2.2).

$$\begin{aligned} &Ref_a^C = Ref_a + M_{off,C1}, \quad Ref_b^C = M_{off,C1}, \quad Ref_c^C = Ref_c + M_{off,C1} \\ &M_{off,C1} = -\frac{1}{2}[max(Ref_a, Ref_b, Ref_c) + min(Ref_a, Ref_b, Ref_c)] \end{aligned} \tag{2.2}$$

Although $M_{off,C1}$ in (2.2) is similar to that used for three-phase balanced modulation,

its significance is more prominent here in terms of determining the minimum dc-link voltage needed. This is unlike the three-phase balanced modulation, where the minimum dc-link voltage needed is pretty obvious. To illustrate how the minimum dc-link voltage needed by the single-phase B6 converter can be determined, variations of (2.2) are drawn in Fig. 2.2, where the largest peak among the three modified references is notated as $M_{PK,max}$. The value for $M_{PK,max}$ can generally be determined by using (2.3).

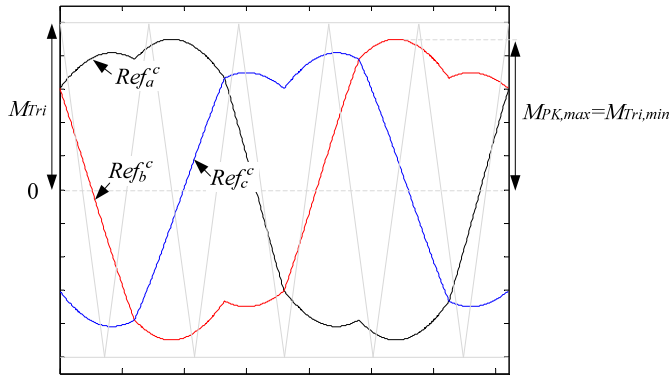


Figure 2.2: *Reference-carrier arrangement obtained with centered scheme.*

$$M_{PK,max} = max(M_{ab}, M_{cb}, M_{ac})/2 \tag{2.3}$$

where $\frac{1}{2}V_{dc} \times M_{ac}$ is the magnitude of $v_{ac} = v_{ab} - v_{cb}$ computed using ac terminal voltages defined in (2.1). The value of M_{ac} can further be computed using (2.4) based on simple geometry.

$$M_{ac} = \sqrt{M_{ab}^2 + M_{cb}^2 - 2M_{ab}M_{cb}cos\varphi_1} \tag{2.4}$$

To retain its linear characteristics, the carrier M_{Tri} used for comparison with the references in (2.2) must hence be either equal or larger than $M_{PK,max}$, which is given in (2.5).

$$M_{Tri} \geq M_{Tri,min} = M_{PK,max} = max(M_{ab}, M_{cb}, M_{ac})/2 \tag{2.5}$$

where $M_{Tri,min}$ is the smallest carrier peak necessary, which in terms of basic modulation principle, also is the smallest normalized dc-link voltage needed without causing over-modulation. Therefore, centering of all three references therefore has the advantage of identifying the smallest dc-link voltage easily, which if followed can reduce the voltage stress and switching loss of the power devices.

2.2.2 Partially centered modulation

The centered modulation scheme in Section 2.1.1 places the three references centrally within the carrier band, which for a three-phase balanced converter is attractive since current ripples from all three phases are reduced uniformly. However, for an asymmetrical single-phase B6 converter, reducing the current ripples uniformly may not be necessary. For example, with the ac load of the single-phase B6 converter as shown in Fig. 2.1(a) replaced by a film capacitor for power ripple decoupling, current flowing through the ac source may demand lower ripple than current flowing through the film capacitor. In that case, the references for the two phase-legs tied to the source should be centered, rather than centering all three references. Such two-reference centering can be implemented by dividing the source voltage v_{ab} equally between the two references. The modified references $Ref_a^{C'}$, $Ref_b^{C'}$ and $Ref_c^{C'}$ then become (2.6), after adding the common offset $M_{off,C2}$ to (2.1).

$$\begin{aligned} &Ref_a^{C'} = Ref_a + M_{off,C2}, \quad Ref_b^{C'} = Ref_b + M_{off,C2}, \quad Ref_c^{C'} + M_{off,C2} \\ &M_{off,C2} = -\frac{1}{2} \times (Ref_a + Ref_b) \end{aligned} \tag{2.6}$$

For the considered example, $M_{off,C2} = -\frac{1}{2}Ref_a = -\frac{1}{2}M_{ab}sin(\omega_1 t)$, which when substituted to (2.6), results in those two possible reference-carrier arrangements shown in Fig. 2.3(a) and (b). In both figures, the carrier peak is marked as M_{Tri}, which in practice has a small safety margin added to $M_{Tri,min}$ from (2.5). This carrier peak is obviously large enough in Fig. 2.3(a) for confining all references within the carrier band. Fig. 2.3(a) therefore does not require any further modification. The left diagram in Fig. 2.3(b), on the other hand, has a reference $Ref_c^{C'}$ exceeding the carrier band during T_1 and T_2. It is therefore not immediately applicable. Instead, the three references during T_1 must be shifted down equally until the modified $Ref_c^{C''}$ clamps to the carrier peak like shown in the right diagram of Fig. 2.3(b). Further downward shifting is also possible, but will worsen the centering of the modified $Ref_a^{C''}$ and $Ref_b^{C''}$ within the carrier band. It is therefore not encouraged to do so if the objective is to minimize the current ripple from those phase-legs modulated by $Ref_a^{C''}$ and $Ref_b^{C''}$. The same shifting must be applied during T_2, but instead of shifting down, the references must be shifted up until $Ref_c^{C''}$ clamps to the carrier trough. With the shifting included, (2.6) is changed to

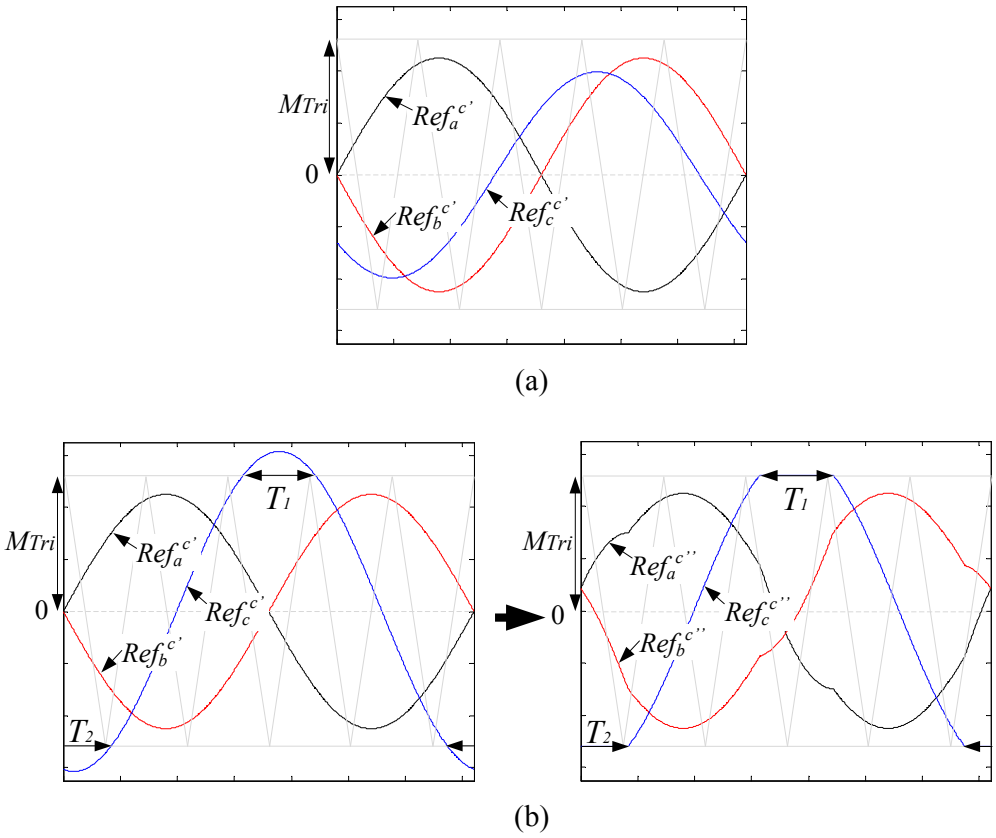


Figure 2.3: *Reference-carrier arrangement obtained with partially centered scheme with (a) $Ref_c^{C'} \leq M_{Tri}$ and (b) $Ref_c^{C'} > M_{Tri}$.*

(2.7), where the additional offset introduced for shifting is notated as $M_{off,C3}$.

$$Ref_a^{C''} = Ref_a^{C'} + M_{off,C3}, \quad Ref_b^{C''} = Ref_b^{C'} + M_{off,C3}, \quad Ref_c^{C''} + M_{off,C3}$$

$$M_{off,C3} = \begin{cases} 0, & if(Ref_a^{C'}, Ref_b^{C'}, Ref_c^{C'}) \leq M_{Tri} \\ sgn(Ref_c^{C'}) * M_{Tri} - Ref_c^{C'}, & if|Ref_c^{C'}| > M_{Tri} \end{cases}$$

$$M_{Tri} \geq M_{Tri,min} \tag{2.7}$$

where $sgn()$ is a function for returning the polarity of parameter enclosed by its parentheses.

To demonstrate the reduction of current ripple, a mathematical formulation can be derived

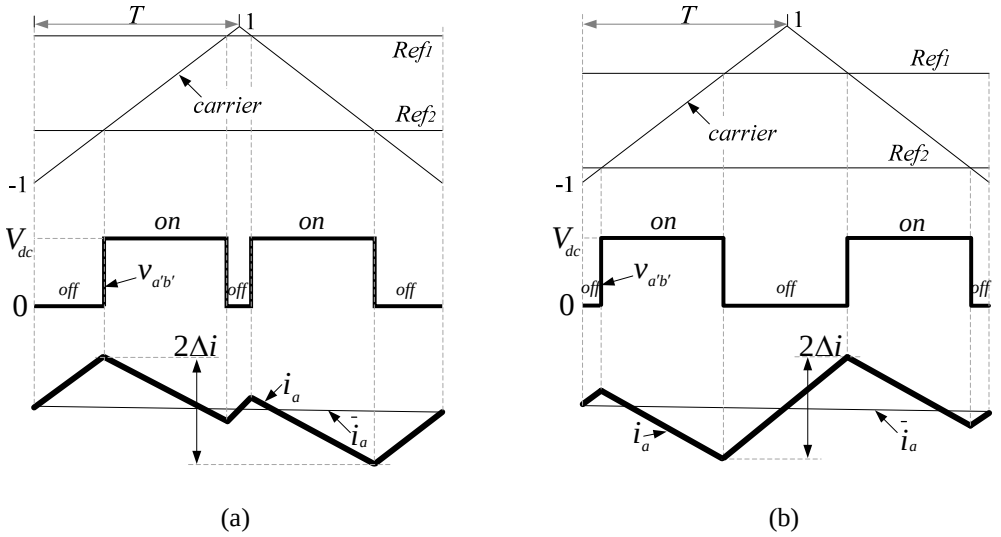


Figure 2.4: *Reference placements in a carrier cycle during (a) T_2 and (b) T_1.*

from those terminal pulse voltage and current waveforms as shown in Fig. 2.4(a) and (b) for the assumed example. In those figures, Ref_1 and Ref_2 are for representing either $Ref_a^{C''}$ or $Ref_b^{C''}$, depending on which is higher at the instant of consideration. They are shifted up like in Fig. 2.4(a) when in interval T_2, and shifted down like in Fig. 2.4(b) when in interval T_1. Their respective peak current ripple Δi expressions can also be derived as (2.8) and (2.9), where T and L represent the half carrier period and ac filter inductance, respectively.

$$L \times 2|\Delta i| = \frac{Ref_2 + 1}{2} \times 2T \times |v_{ab}| \tag{2.8}$$

$$L \times 2|\Delta i| = \frac{1 - Ref_1}{2} \times 2T \times |v_{ab}| \tag{2.9}$$

Noting further that $Ref_1 \geq Ref_2$, (2.8) and (2.9) can be combined in order to give the general current ripple expression in (2.10).

$$|\Delta i| = max[min(Ref_a^{C''}, Ref_b^{C''}) + 1, 1 - max(Ref_a^{C''}, Ref_b^{C''})] \times \frac{T}{2L} \times |v_{ab}| \tag{2.10}$$

References from (2.2) can subsequently be substituted into (2.10) for computing the peak

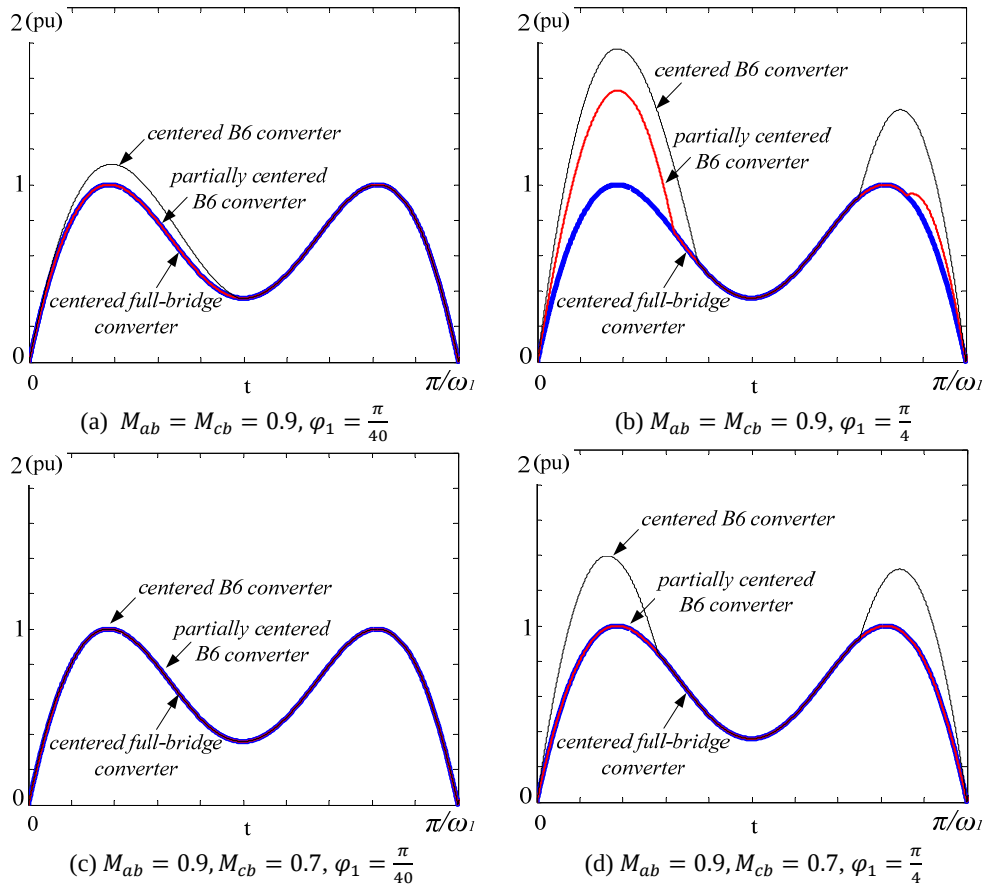


Figure 2.5: *Comparison of current ripples imposed on i_a by different modulation schemes (1 pu = $(\frac{V_{dc}T}{8L})$).*

current ripple expected from the partially centered scheme. The same expression in (2.10) can be used for calculating the current ripple expected from the centered scheme by simply replacing $Ref_a^{C''}$ and $Ref_b^{C''}$ with Ref_a^C and Ref_b^C from (2.2). The obtained current ripples are plotted in Fig. 2.5, together with ripple expected from a full-bridge converter, operating under the same ac and dc conditions. A comparison with the full-bridge converter is meaningful since the single-phase B6 converter has always been cited as the reduced-switch version of two full-bridge converters connected back-to-back. It's ripple value is therefore included in Fig. 2.5, which is clearly the lowest since the condition like $Ref_c^{C'}$ exceeding the carrier in Fig. 2.3(b)

will not occur.

The condition in Fig. 2.3(b) must however be corrected when used with the partially centered B6 converter. Its current ripple drawn from the ac source is therefore higher than the full-bridge converter during an interval of the fundamental cycle. Length of this interval and difference in ripple magnitude depend on the relative magnitude ($M_{ab} : M_{cb}$) and phase-shift φ_1 of the two ac voltages v_{ab} and v_{cb}. For example, in Fig. 2.5(a) and (c), where a comparably small $\varphi_1 = \pi/40$ is used, both partially centered B6 and full-bridge converters are noted to have the same ripple throughout the whole fundamental cycle. The same observation applies to Fig. 2.5(d), where a larger M_{ab} than M_{cb} has been used. The current ripple of the partially centered B6 converter will in fact only be higher when φ_1, M_{cb} or both are comparably high like shown in Fig. 2.5(b). The higher ripple is, as explained, attributed to the lengthened T_1 and T_2 in Fig. 2.3(b) as φ_1 and M_{cb} increase. Regardless of that, the ripple from the partially centered scheme is still smaller than that of the centered scheme discussed in Section 2.1.2(A). The centered scheme will, in fact, match the partially centered scheme only when both φ_1 and M_{cb} are small like shown in Fig. 2.5(c).

2.3 Discontinuous modulation

Discontinuous modulation has been proposed for the B6 converter when it is used as a three-phase converter. Under balanced conditions, all three phases share the clamping equally, which means each phase will be clamped to either the upper or lower dc rail for 120^o. Reduction in power losses will then be spread among the three phases evenly. However, such even spreading may not be necessary when the B6 converter is used as an asymmetrical single-phase converter with a shared phase-leg. This phase-leg usually carries the return currents from the other two non-shared phase-legs, which should cancel each other significantly. Else, the B6 converter may not be as attractive as two back-to-back full-bridges even though it uses two lesser switches. It is therefore reasonable to assume that the current flowing through the shared phase-leg is much smaller with significantly lower power losses generated. The clamping objective should hence move towards reducing losses from the two non-shared phase-legs rather than the shared phase-leg. Such clamping can be ensured by using an offset and modulating references given in (2.11).

$$Ref_a^D = Ref_a + M_{off,D1}, \quad Ref_b^D = Ref_b + M_{off,D1}, \quad Ref_c^D = Ref_c + M_{off,D1}$$
$$M_{off,D1} = \begin{cases} sgn(Ref_a) * M_{Tri} - Ref_a, & if |Ref_a| \geq |Ref_c| \\ sgn(Ref_c) * M_{Tri} - Ref_c, & if |Ref_a| < |Ref_c| \end{cases}, M_{Tri} \geq M_{Tri,min} \tag{2.11}$$

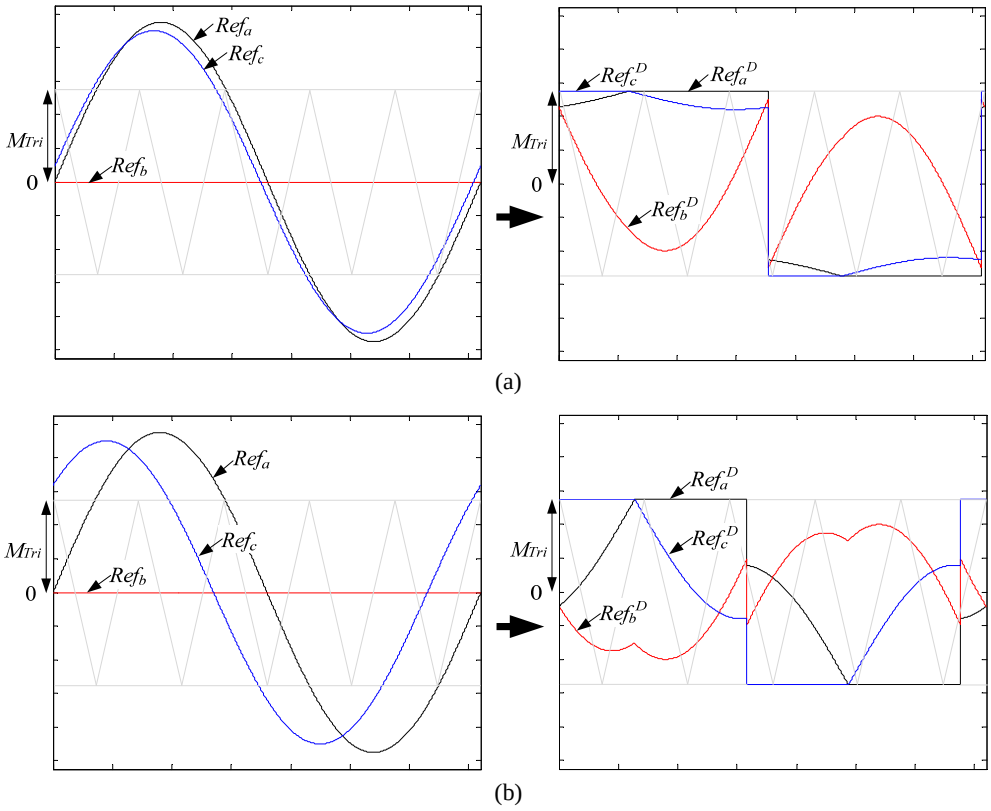


Figure 2.6: *Reference-carrier arrangements obtained with the discontinuous scheme when (a) v_{ab} and v_{cb} are close in magnitude and phase, and (b) $\varphi_1 = \pi/4$.*

Considering an UPS with very close v_{ab} and v_{cb} [17], and a power ripple decoupling converter with v_{ab} and v_{cb} shifted by $\pi/4$ [29], applying (2.11) to them results in Fig. 2.6(a) and (b), respectively. These figures clearly exhibit positive and negative clamping by the non-shared phase-legs only, which certainly is anticipated. Their intervals of clamping for the two non-shared phase-legs are also not always evenly distributed, and will vary with a magnitude ratio ($M_{ab} : M_{cb}$) and phase-shift φ_1 between v_{ab} and v_{cb}. Expressions for computing them can be derived after determining t_1 and t_2, which according to Fig. 2.6(a) and (b), can be expressed

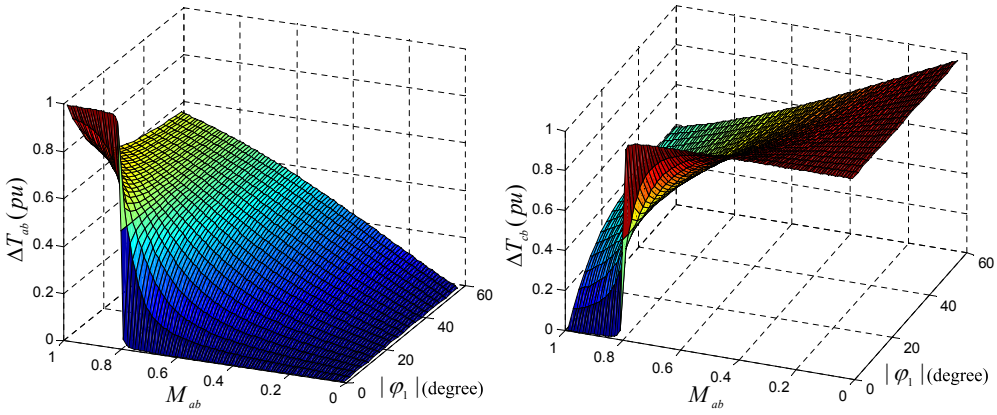


Figure 2.7: *Clamping intervals (a) ΔT_{ab} and (b) ΔT_{cb} of the non-shared phase-legs as M_{ab} and φ_1 vary while keeping $M_{cb} = 0.8$.*

as (2.12).

$$M_{ab}sin(\omega_1 t_1) = -M_{cb}sin(\omega_1 t_1 + \varphi_1) \Rightarrow \omega_1 t_1 = tan^{-1}(\frac{-M_{cb}sin\varphi_1}{M_{ab} + M_{cb}cos\varphi_1})$$
$$M_{ab}sin(\omega_1 t_2) = M_{cb}sin(\omega_1 t_2 + \varphi_1) \Rightarrow \omega_1 t_2 = tan^{-1}(\frac{M_{cb}sin\varphi_1}{M_{ab} - M_{cb}cos\varphi_1}) \tag{2.12}$$

The total positive and negative clamping time for the non-shared phase-leg linked to v_{ab} is then given by ΔT_{ab} in (2.13), which when subtracted from the fundamental period, gives the total clamping time ΔT_{cb} for the other non-shared phase-leg linked to v_{cb}.

$$\Delta T_{ab} = \begin{cases} 2(t_1 - t_2), & if t_1 \geq t_2 \\ 2(t_1 - t_2) + \frac{2\pi}{\omega_1}, & if t_1 < t_2 \end{cases} \Rightarrow$$
$$\Delta T_{ab} = \begin{cases} \frac{2}{\omega_1}\left(tan^{-1}(\frac{-M_{cb}sin\varphi_1}{M_{ab}+M_{cb}cos\varphi_1}) - tan^{-1}(\frac{M_{cb}sin\varphi_1}{M_{ab}-M_{cb}cos\varphi_1})\right), if M_{ab} \leq M_{cb}|cos\varphi_1|, \varphi_1 \in [0,\pi] \\ \frac{2}{\omega_1}\left(tan^{-1}(\frac{-M_{cb}sin\varphi_1}{M_{ab}+M_{cb}cos\varphi_1}) - tan^{-1}(\frac{M_{cb}sin\varphi_1}{M_{ab}-M_{cb}cos\varphi_1})\right) + \frac{2\pi}{\omega_1}, if M_{ab} > M_{cb}|cos\varphi_1|, \varphi_1 \in [0,\pi] \end{cases}$$
$$\Delta T_{cb} = \frac{2\pi}{\omega_1} - \Delta T_{ab} \tag{2.13}$$

Variations of ΔT_{ab} and ΔT_{cb} are plotted in Fig. 2.7 by varying $(M_{ab} : M_{cb})$ and φ_1, where $1\ pu = \frac{2\pi}{\omega_1}$. They will mostly be different except when $M_{ab} \approx M_{cb}$, at which ΔT_{ab} and ΔT_{cb} are approximately equal regardless of how φ_1 varies.

2.4 Simulation and experimental results

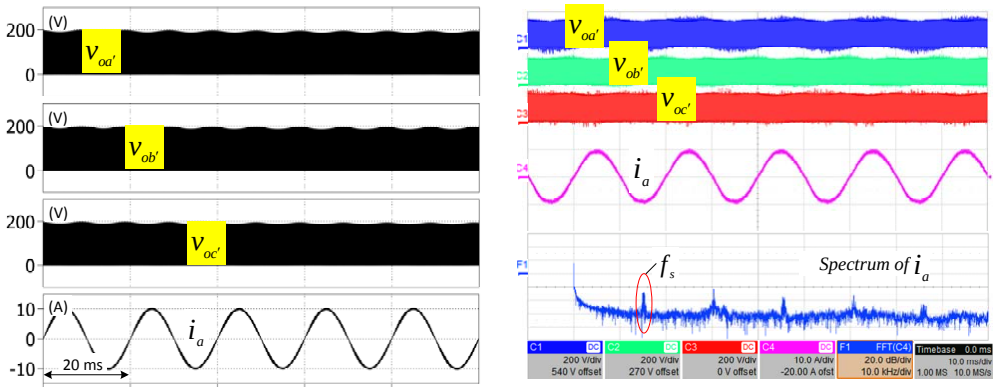
Using the parameters listed in Table 2.1, simulations of the single-phase B6 converter shown in Fig. 2.1(a) have been performed with the three proposed modulation schemes applied in turn. An experimental prototype was also built for verifying the practicalities of the schemes. The obtained results are described as follows.

Table 2.1: *PARAMETERS USED FOR SIMULATIONS AND EXPERIMENTS.*

Parameters	Values
Nominal power	800 W
DC-link voltage V_{dc}	190 V
Source voltage v_{ab}	110 V(RMS)
Load voltage v_{cb}	110 V(RMS) (Resistive load)
Phase shift φ_1	$\pi/4$
Switching frequency f_s	15.2 kHz
DC link capaciotr C	1800 uF
AC filter inductor L	4.1 mH
Power swithes	IXGH30N120B3D1

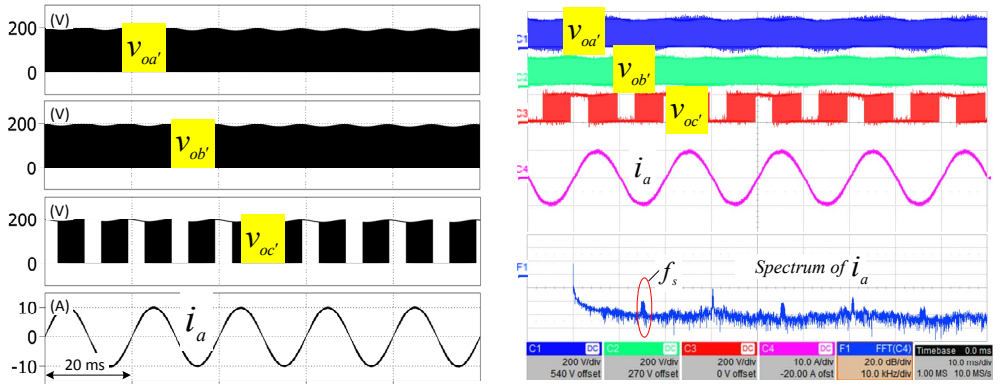
2.4.1 Continuous modulation

Results obtained with the centered scheme from (2.2) and partially centered scheme from (2.7) are presented in Fig. 2.8 and Fig. 2.9, respectively. The centered scheme obviously switches all phase-legs continuously with all three modulating references centered within the carrier band. Its accompanied current spectrum for i_a is plotted at the bottom of Fig. 2.8(b), which has a prominent harmonic cluster centered at the switching frequency of 15.2 kHz. This cluster leads to a total harmonic distortion (THD) value of 2.9 % computed for i_a when modulated by the centered scheme from (2.2). In contrast, the partially centered scheme has its harmonic cluster at 15.2 kHz reduced, which in terms of THD for i_a, gives a smaller value of 2.5 %. As explained, this improvement is introduced by centering the two preferred references rather than all three references. Such centering may however lead to discontinuous clamping of the phase-leg modulated by the non-centered reference, which in Fig. 2.3(b), is $Ref_c^{C''}$. This clamping can clearly be seen in Fig. 2.9(a) and (b), which according to the loss distribution plots in Fig. 2.10, has helped to reduce switching losses from the clamped phase-leg. The clamping is however not always introduced, and will, in fact, reduce to zero when the magnitude of $Ref_c^{C'}$ in Fig. 2.3(b) falls below the carrier peak.



(a) Simulated (b) Experimental

Figure 2.8: *Waveforms of the B6 converter in Fig. 2.1(a) obtained with the centered scheme from (2.2) and $\varphi_1 = \pi/4$. (Experimental results: $v_{oa'}$, $v_{ob'}$ and $v_{oc'}$: 200 V/div, i_a: 10 A/div, Spectrum of i_a: 20 dB/div 10 kHz/div, Timebase: 10 ms)*



(a) Simulated (b) Experimental

Figure 2.9: *Waveforms of the B6 converter in Fig. 2.1(a) obtained with the partially centered scheme from (2.7) and $\varphi_1 = \pi/4$. (Experimental results: $v_{oa'}$, $v_{ob'}$ and $v_{oc'}$: 200 V/div, i_a: 10 A/div, Spectrum of i_a: 20 dB/div 10 kHz/div, Timebase: 10 ms)*

2.4.2 Discontinuous modulation

For an easier comparison, simulations and experiments with the discontinuous scheme expressed in (2.11) were performed with the same parameters from Table 2.1. Its captured results are

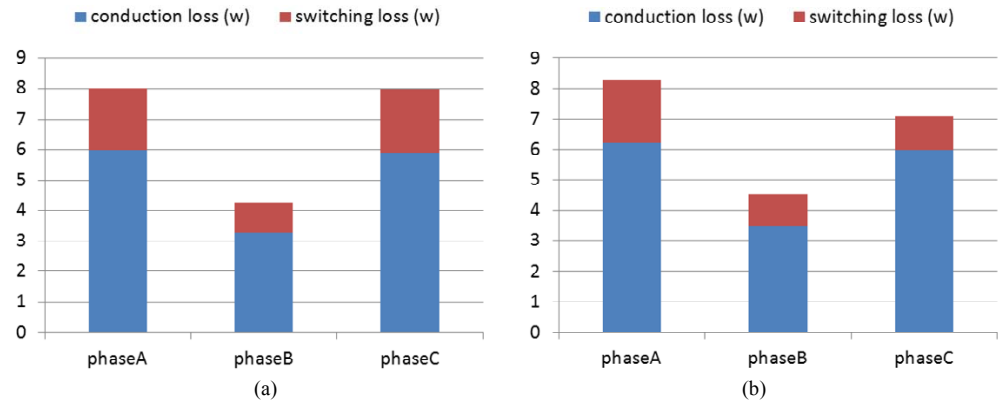


Figure 2.10: *Experimental loss distributions of B6 converter when modulated by the (a) centered scheme from (2.2) and (b) partially centered scheme from (2.7).*

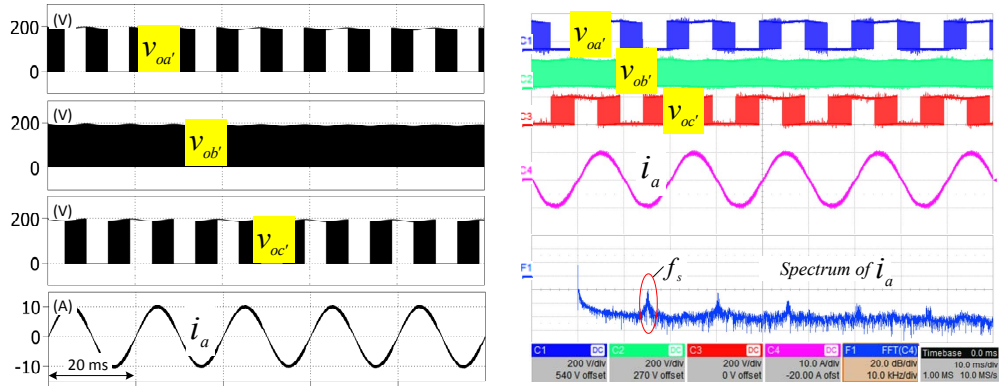


Figure 2.11: *Waveforms of the B6 converter in Fig. 2.1(a) obtained with the discontinuous scheme from (2.11) and $\varphi_1 = \pi/4$.(Experimental results: $v_{oa'}$, $v_{ob'}$ and $v_{oc'}$: 200 V/div, i_a: 10 A/div, Spectrum of i_a: 20 dB/div 10 kHz/div, Timebase: 10 ms)*

shown in Fig. 2.11, where the clamping of only two non-shared phase-legs can clearly be seen. Such clamping shifts the modulating references away from the center of the carrier band, and hence a poorer THD of 3.9 % for i_a. The first harmonic cluster of i_a is placed at 15.2 kHz, whose amplitude is the largest among the three proposed modulation methods. Its accompanied loss distribution in Fig. 2.12 is however improved when compared with those in Fig. 2.10 for the

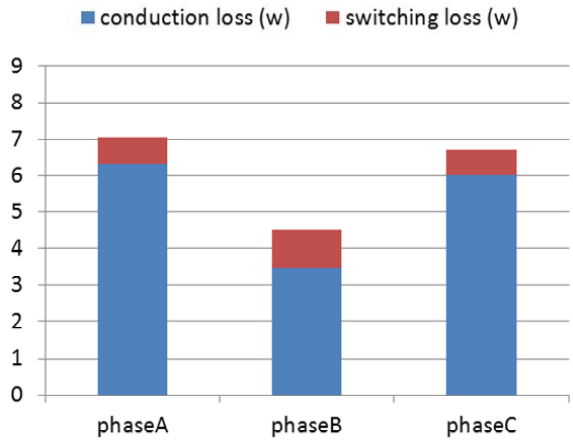


Figure 2.12: *Experimental loss distribution of B6 converter when modulated by the discontinuous scheme from (2.11).*

continuous schemes. The poorer i_a spectrum is therefore a tradeoff introduced by the lower total loss and improved loss distribution brought by the proposed discontinuous scheme.

2.5 Summary

New continuous and discontinuous modulation schemes have been proposed for the B6 converter when used as a single-phase converter with two sets of ac terminals. The continuous centered scheme, in particular, helps to identify the minimum carrier peak needed for linear modulation, and hence the minimum dc-link voltage needed by the converter. The same minimum dc-link voltage can be ensured by the partially centered scheme, which instead of all modulating references, centers only two chosen references. The current flowing through the phase-legs modulated by these two references will then have better spectral quality. On the other hand, the discontinuous scheme has its loss distribution improved by clamping only the two non-shared phase-legs with higher losses. Losses of the three phase-legs are therefore brought closer at the expense of a poorer current quality when compared with the other two modulation schemes. These performance features have been observed in simulations and experiments in accordance with the expectations.

3 Modulation schemes for single-phase H6 converters

Besides single-phase B6 converter, the H6 converter is another reduced switch converter, which has the same number of power devices and is appropriate for single-phase applications as well. Some studies about the H6 converter have been done in literatures in terms of control strategies and applications, but it is still a new topology and large potential still exists to further improve its performance and make it more attractive. It is thus stuided in this chapter as following.

3.1 H6 converter

The H6 converter has two sets of ac terminals, and four PWM references in total are thus needed to generate the terminal voltages, where the two references for one leg are illustrated in Fig. 3.1(b) and (c). As known, sinusoidal references located in the center of the carrier is the simplest modulation scheme, as indicated in (3.1), and they are also shown in the left part of Fig. 3.1(b) and (c), where V_{dc} is the DC link voltage, Ref_U, Ref'_U, Ref_D, and Ref'_D are the PWM references for terminals U, U', D, and D', respectively, M_U and M_D are the modulation indexes, v_U and v_D are the ac voltages, ω_1 is the angular frequency, and φ_1 is the phase displacement between the upper and lower references. However, this scheme cannot meet the modulation constraint of the H6 converter that the upper reference should always be above the lower one [34]. In the literature, positive and negative DC offsets are added to the upper and lower references respectively in order to respect the constraint, which unfortunately is only effective when the modulation index is low (at least one of the upper and lower modulation index is low, as illustrated in Fig. 3.1(b)), but when both of the two modulation indexes are high the references added by the DC offsets may get beyond the carrier (Fig. 3.1(c)) or the DC link voltage is essential to be increased. To retain the relatively low DC link voltage and at the same time get the modulation constraint met, a cluster of modulation schemes are proposed is this chapter, which will then be illustrated by categorizing into continuous and discontinuous schemes as following.

$$
\begin{aligned}
&Ref_U = M_U sin(\omega_1 t), \quad Ref_{U'} = -M_U sin(\omega_1 t) \\
&Ref_D = M_D sin(\omega_1 t + \varphi_1), \quad Ref_{D'} = -M_D sin(\omega_1 t + \varphi_1) \\
&v_U = V_{dc} \times M_U sin(\omega_1 t), \quad v_D = V_{dc} \times M_D sin(\omega_1 t + \varphi_1)
\end{aligned} \tag{3.1}
$$

3.2 Continuous modulation

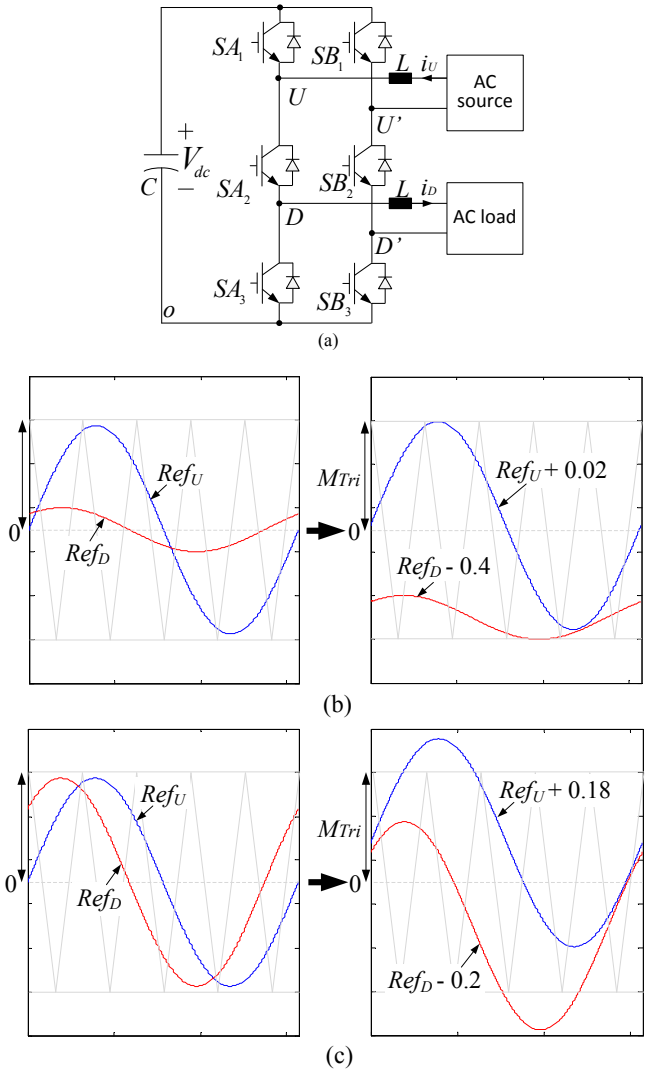


Figure 3.1: *Illustrations of (a) H6 converter and its simple reference-carrier arrangement (b) $M_U = 0.95$, $M_D = 0.2$ (c) $M_U = M_D = 0.95$.*

3.2.1 Centered modulation

In the centered scheme, the minimum offset is first added to the sinusoidal references in (3.1) to meet the modulation constraint, and the inter references are obtained, as shown in the left

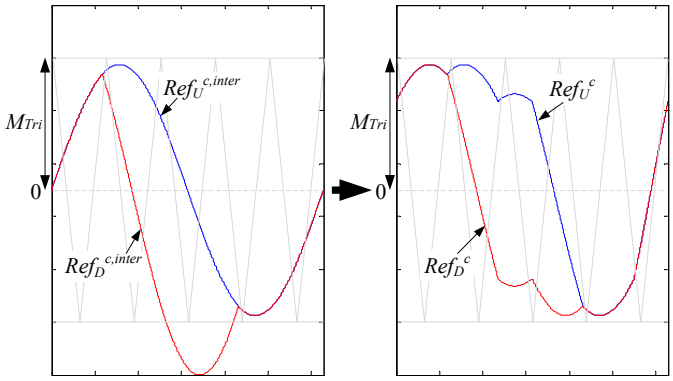


Figure 3.2: *Reference-carrier arrangement obtained with a centered scheme for the H6 converter.*

part of Fig. 3.2. Since the modulation constraint requires upper references above the lower one, the minimum offset needed $M_{offX,c,inter}(X = U, D)$ can be calculated as given in (3.2). The inter-references $Ref_X^{c,inter}(X = U, D, U', D')$ are then obtained by adding the offsets to the references in 3.1, as following.

$$
\begin{aligned}
&Ref_U^{c,inter} = Ref_U + M_{offU,c,inter}, \quad Ref_{U'}^{c,inter} = Ref_{U'} + M_{offU,c,inter} \\
&Ref_D^{c,inter} = Ref_D + M_{offD,c,inter}, \quad Ref_{D'}^{c,inter} = Ref_{D'} + M_{offD,c,inter} \\
&M_{offU,c,inter} = 0, \quad M_{offD,c,inter} = min(Ref_U - Ref_D, Ref_{U'} - Ref_{D'})
\end{aligned} \tag{3.2}
$$

Note that shifting only the upper or lower references or both of them does not make difference for the purpose to meet the modulation constraint. The upper references in (3.1) are thus retained for simplicity. Despite, the inter references $Ref_X^{c,inter}(X = U, D)$ shown in the left part of Fig. 3.2 are still beyond the carrier boundary because of a large bias relative to the center of the carrier. An offset $M_{offX,c}(X = U, D)$ is then added to the inter references in (3.2) to shift them to the center of the carrier band, as expressed in 3.3. The centered PWM references are thus obtained, and they are also shown in the right part of Fig. 3.2.

$$
\begin{aligned}
&Ref_U^{c} = Ref_U^{c,inter} + M_{offU,c}, \quad Ref_{U'}^{c} = Ref_{U'}^{c,inter} + M_{offU,c} \\
&Ref_D^{c} = Ref_D^{c,inter} + M_{offD,c}, \quad Ref_{D'}^{c} = Ref_{D'}^{c,inter} + M_{offD,c} \\
&M_{offU,c} = 0, \quad M_{offD,c} = -\frac{max(Ref_X^{c,inter}) + min(Ref_X^{c,inter})}{2} \quad (X = U, U', D, D')
\end{aligned} \tag{3.3}
$$

3.2.2 Partially centered modulation

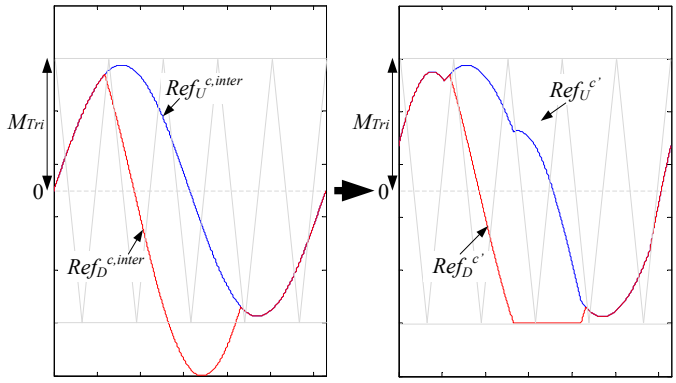
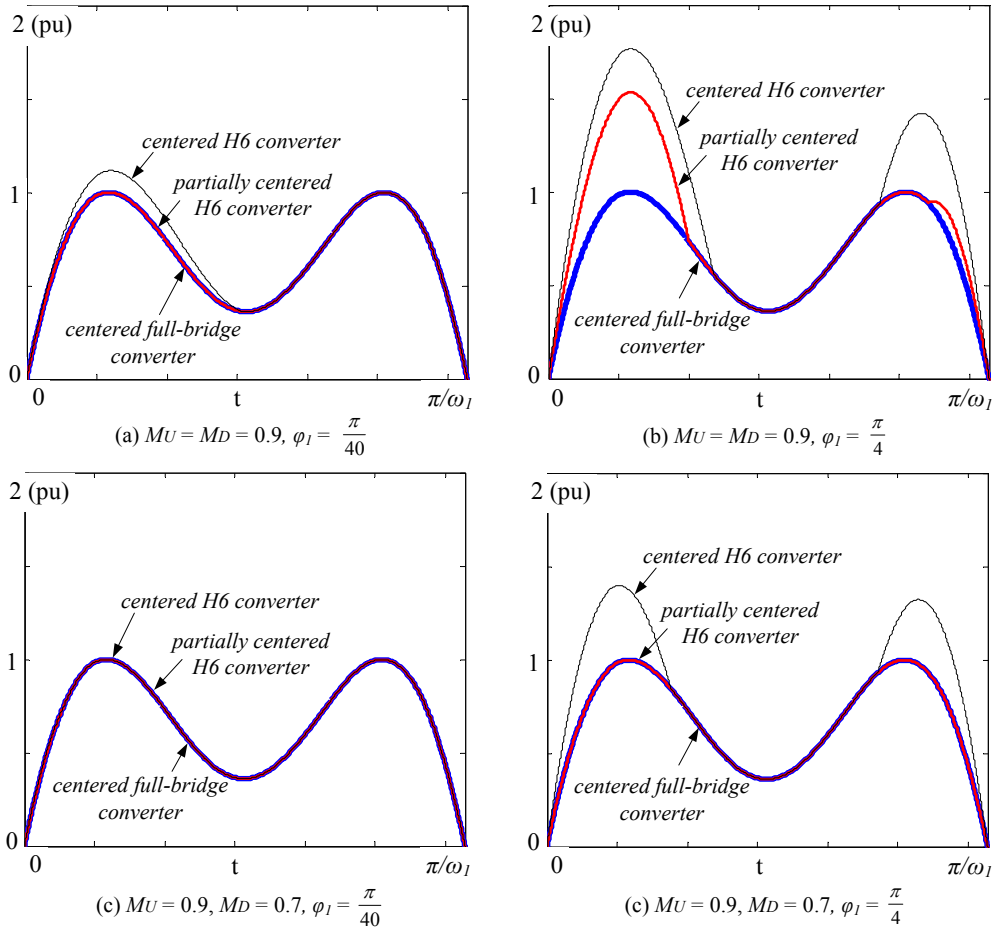


Figure 3.3: *Reference-carrier arrangement obtained with partially centered scheme for H6 converter.*

With the centered scheme the references group including the upper and lower references are located in the center of the carrier band, so the over modulation can be avoided as much as possible like in the SVPWM. On the other hand, both the upper and lower current ripples are reduced, which means neither the upper nor the lower current ripple is minimized since the upper and lower references together share the center of the carrier and thus both of them have bias relative to the center of the carrier wave. For applications, where only one set of terminals are connected to the grid, e.g. online UPS and voltage regulator, the current ripple reduction of the grid side is more required. The corresponding two references instead of the four are therefore more necessary to be located in the center of the carrier, which will then be referred to as the partially centered scheme.

Assuming the upper terminals are tied to the grid, with the inter references given in (3.2), the upper references are already in the center of the carrier, as shown in the left part of Fig. 3.3. In order to make the references applicable, an offset $M_{offX,c'}(X = U, D)$ is needed to shift the part of the references that beyond the carrier boundary back to the inside and it can be calculated as in (3.4). Then, by adding the offset to the inter-references, the partially centered references $Ref_X^{c'}(X = U, D, U', D')$ are obtained, as demonstrated in 3.4 and the right part of Fig. 3.3, where the part of the references that beyond the carrier boundary is clamped to the bottom of the carrier while other part is still retained. Meanwhile, the low DC link voltage is



(a) $M_U = M_D = 0.9$, $\varphi_1 = \frac{\pi}{40}$ (b) $M_U = M_D = 0.9$, $\varphi_1 = \frac{\pi}{4}$

(c) $M_U = 0.9$, $M_D = 0.7$, $\varphi_1 = \frac{\pi}{40}$ (c) $M_U = 0.9$, $M_D = 0.7$, $\varphi_1 = \frac{\pi}{4}$

Figure 3.4: *Comparison of current ripples imposed on i_U by different modulation schemes in H6 converters. ($1\ pu = \frac{V_{dc}T}{8L}$)*

still retained.

$$
\begin{aligned}
&Ref_U^{c'} = Ref_U^{c,inter} + M_{offU,c'}, \quad Ref_{U'}^{c'} = Ref_{U'}^{c,inter} + M_{offU,c'} \\
&Ref_D^{c'} = Ref_D^{c,inter} + M_{offD,c'}, \quad Ref_{D'}^{c'} = Ref_{D'}^{c,inter} + M_{offD,c'} \\
&M_{offU,c'} = M_{offD,c'}, \quad M_{offD,c'} = [-1 - min(Ref_x^{c,inter})] \cdot [min(Ref_x^{c,inter}) < -1] \quad (x = D, D')
\end{aligned}
\tag{3.4}
$$

Similar to the derivation of the current ripple in B6 converters which is illustrated in Fig. 2.4, and (2.8)-(2.10), the current ripple of i_U in H6 converters can be obtained as in (3.5) and it is also demonstrated in Fig. 3.4.

$$|\Delta i| = max[min(Ref_U^y, Ref_{U'}^y) + 1, 1 - max(Ref_U^y, Ref_{U'}^y)] \times \frac{T}{2L} \times |v_U| \quad (y = null, c, c') \tag{3.5}$$

Fist of all, from a current ripple point of view, the H6 converter has the same performance with B6 converter no matter the partially centered or the centered PWM is used, if the same dc link voltage, modulation index, and phase displacement are applied. So the same conclusion of the current ripple comparison with B6 converter is obtained. In detail, the centered full-bridge converter always has the lowest current ripple. The partially centered H6 converter can achieve the same lowest current ripple except in the toughest condition, where both the two terminal voltages have high modulation index and the phase displacement between them is large. The centered H6 converter has the highest current ripple, and the difference increases as the modulation index of the other voltage or the phase displacement increases. Thus, the better performance of partially centered PWM in the current ripple perspective is well verified.

3.3 Discontinuous modulation

Another critical concern besides the DC link voltage and the current ripple in the H6 converter is its uneven loss distribution among the three switches in each leg, where the middle switch is normally the most stressful. It was found in literatures that the loss of the middle switch can be shifted to the upper and lower ones by increasing the gap between the upper and lower references [38]. The idea of the discontinuous scheme is thus to push the upper and lower references upward and downward, respectively. The discontinuous PWM references can be obtained by first calculating the offsets needed, as indicated in (3.6), with which the references in (3.1) then are reshaped to the discontinuous references as shown in the right part of Fig. 3.5.

$$\begin{aligned}
&Ref_U^D = Ref_U + M_{offU,D}, \quad Ref_{U'}^D = Ref_{U'} + M_{offU,D} \\
&Ref_D^D = Ref_D + M_{offD,D}, \quad Ref_{D'}^D = Ref_{D'} + M_{offD,D} \\
&M_{offU,D} = 1 - max(Ref_U, Ref_{U'}), \quad M_{offD,D} = -1 - min(Ref_D, Ref_{D'})
\end{aligned} \tag{3.6}$$

The valid range of the phase displacement between the upper and lower references with the discontinuous scheme can be calculated by solving the equation $Ref_U^D \geq Ref_D^D$. As seen in the right part of Fig. 3.5, the first 'touching point' should appear in the dashed circle when the

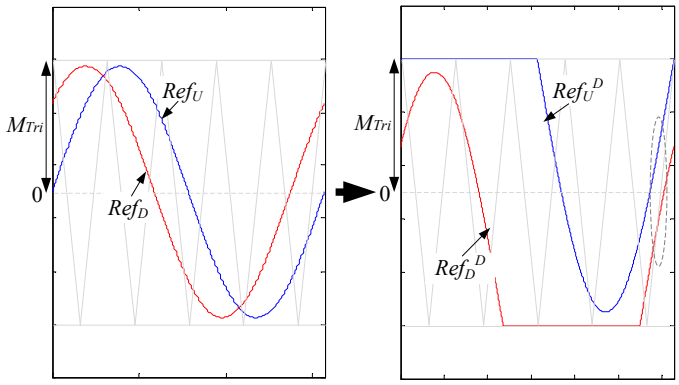


Figure 3.5: *Reference-carrier arrangement obtained with discontinuous scheme for H6 converter.*

two references are getting close to each other by increasing the phase displacement φ_1. Thus the conditions as given by (3.7) can be obtained as,

$$Ref_{U'}^D = 1, \quad Ref_{D'}^D = -1 \tag{3.7}$$

According to (3.7), (3.1), and (3.6), the inequation $Ref_U^D \geq Ref_D^D$ can be represented as follows,

$$2M_U sin(\omega t) + 1 \geq 2M_D sin(\omega t + \varphi_1) - 1 \tag{3.8}$$

The constraint of the phase displacement is then obtained as (3.9).

$$|\varphi_1| \leq acos(\frac{M_D^2 + M_U^2 - 1}{2M_D M_U}), \varphi_1 \in [-\pi, \pi] \tag{3.9}$$

The phase displacement with the conventional modulation scheme shown in the right part of Fig. 3.1 is analyzed as well for comparison, where the constraint for the phase displacement becomes,

$$Ref_U + 1 - M_U \geq Ref_D - (1 - M_D) \tag{3.10}$$

Substituting (3.1) into (3.10), the constraint of the phase displacement with the conventional modulation scheme can be obtained as the following,

$$|\varphi_1| \leq acos(\frac{2M_U + 2M_D - M_U M_D - 2}{M_U M_D}), \quad \varphi_1 \in [-\pi, \pi] \tag{3.11}$$

The maximum phase displacement with the conventional modulation and proposed discontinuous modulation scheme are indicated in Fig. 3.6. As seen, with the discontinuous scheme the phase displacement can become 60^o even both of the upper and lower references have a unity modulation index, which introduces much more flexibility into H6 converters compared with the conventional modulation scheme. Moreover, since the discontinuous scheme pushes the upper and lower references to be attached to the top and bottom rails of the carrier, respectively, while centered and partially centered scheme pushes the upper and lower references to touch with each other. Therefore all the three schemes can maximize the DC link voltage utilization and then can achieve the same maximum value of the phase displacement as given in (3.9) and illustrated in Fig. 3.6.

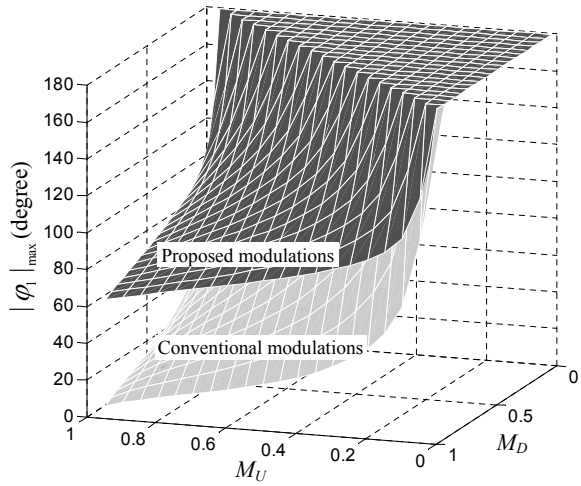


Figure 3.6: *The maximum phase displacement between the upper and the lower references with the conventional and proposed modulation schemes for the H6 converter.*

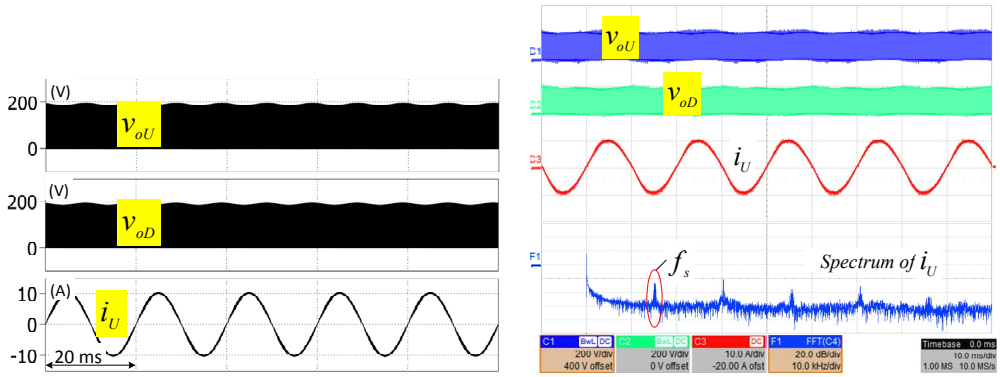
3.4 Simluation and experimental results

Simulations of the H6 converter which is illustrated in Fig. 3.1 have been performed with the three proposed modulation schemes applied, by using the parameters listed in Table 3.1. A prototype was also built to verify the feasibility of the proposed modulation schemes. The results are given in the following.

Table 3.1: *PARAMETERS USED FOR SIMULATIONS AND EXPERIMENTS.*

Parameters	Values
Nominal power	800 W
DC-link voltage V_{dc}	190 V
Source voltage v_U	110 V(RMS)
Load voltage v_D	110 V(RMS) (Resistive load)
Phase shift φ_1	$\pi/4$
Switching frequency f_s	15.2 kHz
DC link capacitor C	1800 uF
AC filter inductor L	4.1 mH
Power switches	IXGH30N120B3D1

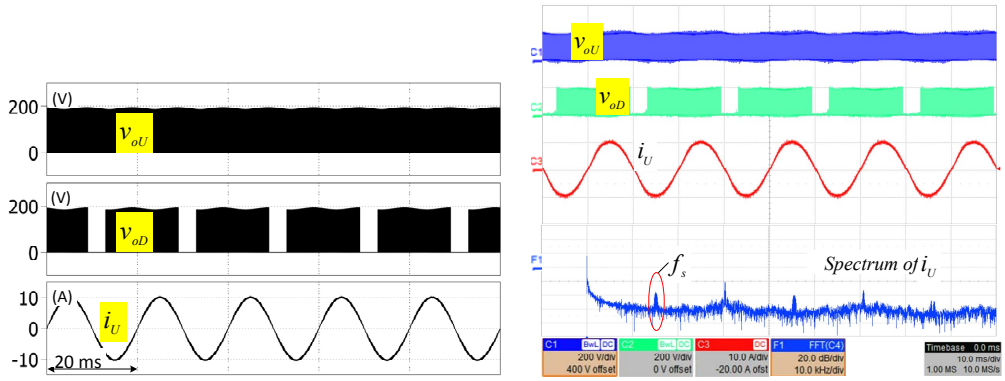
3.4.1 Continuous modulation



(a) Simulated (b) Experimental

Figure 3.7: *Waveforms of the H6 converter in Fig. 3.1(a) obtained with the centered scheme from (3.3) and* $\varphi_1 = \frac{\pi}{4}$*. (Experimental results:* v_{oU} *and* v_{oD}*: 200 V/div,* i_U*: 10 A/div, Spectrum of* i_U*: 20 dB/div 10 kHz/div, Timebase: 10 ms)*

Simulation and experimental results of the H6 converter with the centered scheme from (3.3) and partially centered scheme from (3.4) are presented in Fig. 3.7 and Fig. 3.8, respectively. Similar to the single-phase B6 converter, the partially centered scheme can reduce the first harmonic cluster of the corresponding current, which is i_U in the H6 converter. In terms of the THD of i_U, it is reduced from 2.9% to 2.5% by using the partially centered scheme to replace



(a) Simulated (b) Experimental

Figure 3.8: *Waveforms of the H6 converter in Fig. 3.1(a) obtained with the partially centered scheme from (3.4) and* $\varphi_1 = \frac{\pi}{4}$*. (Experimental results:* v_{oU} *and* v_{oD}*: 200 V/div,* i_U*: 10 A/div, Spectrum of* i_U*: 20 dB/div 10 kHz/div, Timebase: 10 ms)*

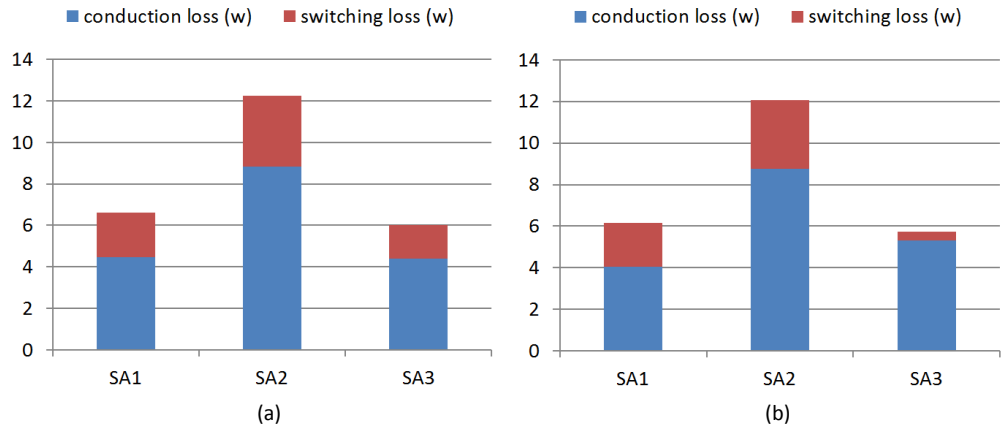
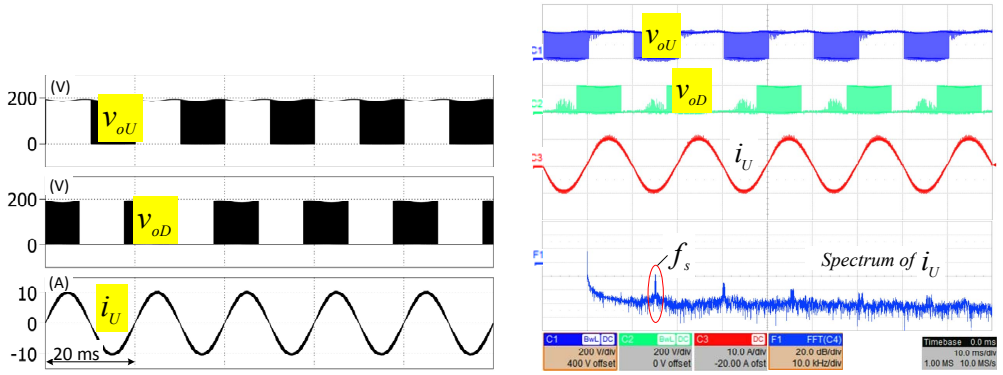


Figure 3.9: *Experimental loss distributions of H6 converter when modulated by the (a) centered scheme from (3.3) and (b) partially centered scheme from (3.4).*

the centered scheme. Furthermore, the partially centered scheme may introduce clamping to the terminal voltage (see Fig. 3.7(a)), and thereby reduce the corresponding switching loss (see Fig. 3.9). The clamping however may disappear, when the amplitude of v_U or v_D gets lower or the phase displacement between v_U and v_D decreases, as indicated in Fig. 3.3.

3.4.2 Discontinuous modulation

In contrast, with the discontinuous scheme from (3.6) the terminal voltages are always clamped in half a fundamental period, as seen in Fig. 3.10. Thus, the first harmonic cluster of i_U is the highest among the three proposed modulation schemes, and the THD of i_U is 4.7%. In terms of the loss distribution, the discontinuous scheme can increase the loss of SA1 and SA3 but decrease it of SA2 compared with the centered and partially centered schemes. Because SA2 is the most stressed device when the centered or partially centered scheme is applied, the loss distribution is improved by using the proposed discontinuous scheme.



(a) Simulated (b) Experimental

Figure 3.10: *Waveforms of the H6 converter shown in Fig. 3.1(a) obtained with the discontinuous scheme from (3.6) and a phase displacement $\varphi_1 = \frac{\pi}{4}$. (Experimental results: v_{oU} and v_{oD}: 200 V/div, i_U: 10 A/div, Spectrum of i_U: 20 dB/div 10 kHz/div, Timebase: 10 ms)*

3.5 Summary

Continuous and discontinuous modulation schemes are proposed for the single-phase H6 converter. The continuous centered scheme locates the reference group in the center of the carrier band, in order to achieve a maximum dc link voltage utilization and thereby a minimum dc link voltage. In fact, the same dc link voltage can be obtained by the partially centered scheme, which only centers a pair of the references instead of all of them. As a result, the corresponding current ripple can be further reduced. The discontinuous scheme can reduce the loading of the most stressed device in the H6 converter at the expense of a poorer terminal current quality compared with the continuous scheme. All these conclusions can be observed in both the simulation and experimental results.

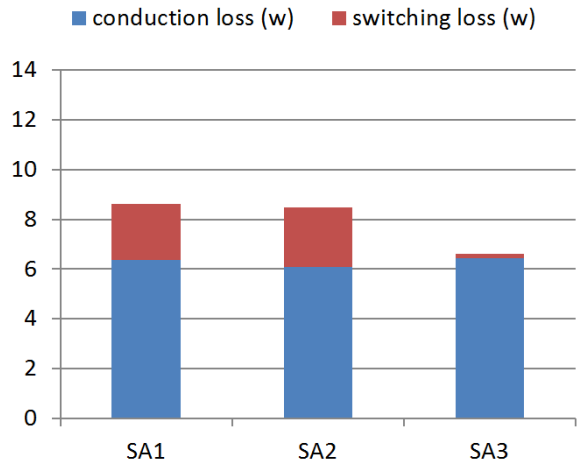


Figure 3.11: *Experimental loss distribution of B6 converter when modulated by the discontinuous scheme from (3.6).*

4 An optimal active power decoupling method for single-phase converters

In Chapter 2 and 3, the performances of the reduced switch single-phase ac-dc-ac converters are studied and new modulation schemes are proposed to improve the performances. Another issue in the single-phase system is the ripple power caused by the unequal instantaneous power between the source and the load, especially in single-phase inverters or rectifiers. The ripple power can be compensated passively by using large electrolytic capacitors on the DC-link, which has been used for decades. However, under the emerging requirement of the high power density and high relaiblity of power converters, the active power decoupling method, where the film capacitor will smaller size and longer lifetime is used to replace the DC-link electrolytic capacitor, is becoming more and more attractive [27–29,55–69]. Thus, an optimal active power decoupling method is proposed and presented in this chapter for single-phase converters to further improve the power density and efficiency.

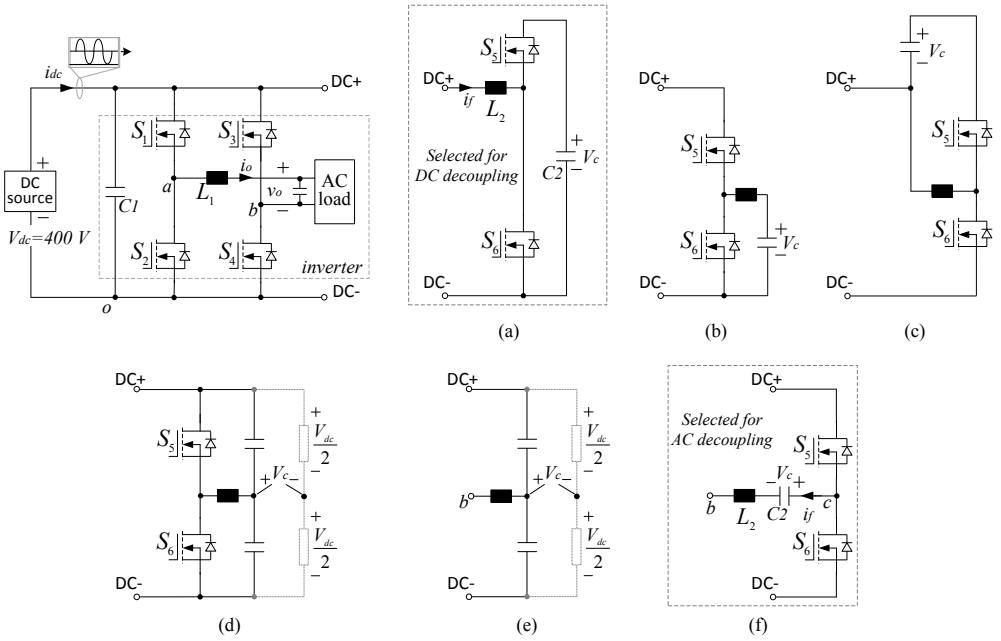


Figure 4.1: *A single-phase voltage source inverter with (a) boost-type, (b) buck-type, (c) buck-boost-type dc active power decoupling and (d) half bridge + flying capacitors, (e) flying capacitors, (f) half bridge ac active power decoupling.*

4.1 Selection of the decoupling capacitors and the auxiliary circuits

The basic circuit diagram of the studied single-phase inverter is illustrated in Fig. 4.1, and its specifications are partially refered to the Little Box Challenge [105], where the dc bus voltage V_{dc} is 450 V connected in series with a 10 Ω resistor as the impedance, the ac output voltage v_o is 240 Vrms with its fundamental frequency ω_n being fixed at $2\pi \times 60$ rad/s. The nominal output power P_n is 2 kW, and the design constraint is that the input dc bus peak-to-peak current and voltage ripples should be less than 20% and 3% of the nominal values, respectively. In order to avoid unnecessary power losses, the 10 Ω resistor is removed in the design, and the dc bus voltage V_{dc} is purposely dropped from 450 V to 400 V. It should be noted that the topology of the inverter is optional and can be other ones than a full-bridge. The following equations can be easily derived for its ac output,

$$v_o = \sqrt{2}V_o sin(\omega_n t), \quad i_o = \sqrt{2}I_o sin(\omega_n t + \varphi) \tag{4.1}$$

$$p_o = v_o i_o = \underbrace{V_o I_o cos\varphi}_{\overline{p_o}} + \underbrace{[-V_o I_o cos(2\omega_n t + \varphi)]}_{\widetilde{p_o}} \tag{4.2}$$

where i_o is the ac output current and only linear loads are considered in this case. φ is the load phase angle. Capital letters are used to represent the rms values. In order to keep the peak-to-peak ripple current to be less than 20%, the following equation should be satisfied.

$$(1 - \frac{20\%}{2})P_r = V_{dc} \cdot I_{r1} \tag{4.3}$$

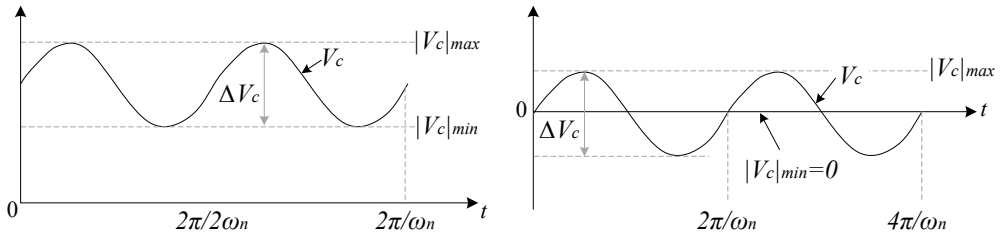
where I_{r1} is the current ripple of capacitor C_1 in the passive power decoupling, and P_r is the second order ripple power in P_o under nominal load. According to the constraint of the dc bus voltage ripple V_{r1}, it can be obtained as following,

$$I_{r1} = 2\omega_n C_1 V_{r1} = 2\omega_n C_1 \frac{3\%}{2} V_{dc} \tag{4.4}$$

According to (4.3) and (4.4), the capacitance of C_1 needed for passive power decoupling is 0.99 mF. In order to have enough design margins, a 450 V E-caps cannot directly be used, and two E-caps with a lower voltage value, e.g. 350 V should be connected in series in the dc bus. Moreover, the E-caps should normally be over-designed in order to have satisfactory lifetime. Therefore, the size of the required E-caps could be considerable, and it will be very difficult to simultaneously meet the compact design and low input current ripple requirements. The active power decoupling methods, which can significantly reduce the capacitance requirement

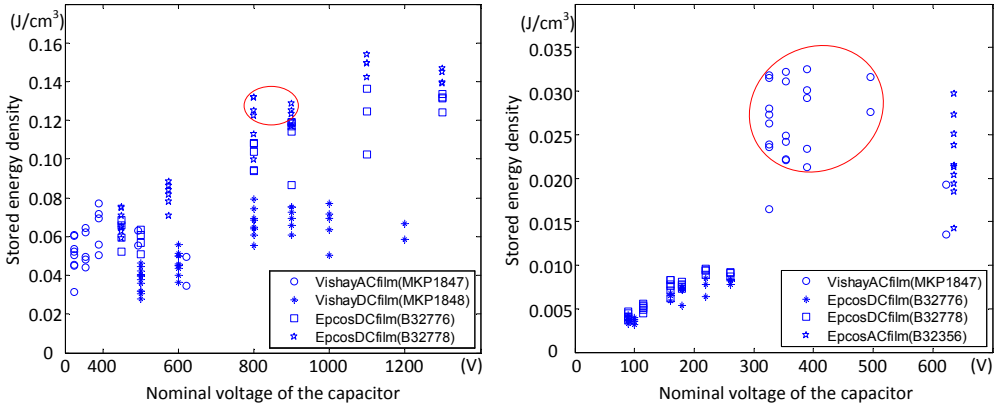
in single-phase systems thus become a promising solution.

A. Decoupling capacitors



(a) dc decoupling (b) ac decoupling

Figure 4.2: *Typical voltage profiles of the decoupling capacitors.*



(a) dc decoupling (b) ac decoupling

Figure 4.3: *Stored energy density versus nominal voltage of the film capacitors.*

The auxiliary circuits for active power decoupling are composed of power switches, chokes, and film capacitors. For power switches and chokes, their volume can be shrinked by using wide band gap devices operating with high switching frequency, while for film capacitors, they may dominate the volume of the overall system due to the requirement for ripple power compensation. The operation modes of the active power decoupling can be classified into dc decoupling and ac decoupling, depending on whether the decoupling capacitor voltage will change its polarity or not as shown in Fig. 4.2. The stored energy of the capacitor in dc decoupling is obviously higher than ac decoupling according to definition of the capacitor's

stored energy shown in (4.5).

$$\Delta E = \frac{1}{2} C_2 (|V_C|^2_{max} - |V_C|^2_{min}) \tag{4.5}$$

where C_2 is the capacitance of the decoupling capacitor, and $|V_C|_{max}$ and $|V_C|_{min}$ are respectively the maximum and minimum values of v_C during operation.

In order to evaluate the performance of the film capacitors used for power decoupling, some state-of-the-art film capacitors are studied and compared, and their stored energy densities, i.e. the ratio between the stored energy in (4.5) and the volume of the capacitor, are presented in Fig. 4.3. For dc decoupling, the dc voltage offset and voltage variation of the capacitors are pushed to the nominal values, and the specifications of the capacitors are obtained from the datasheets [106–108]. As seen in Fig. 4.3(a), the EPCOS dc film capacitors (B32778) have always the best performance even the nominal voltage changes from 400 V to 1300 V. Moreover, the stored energy density generally increases as the nominal voltage rises. The 800 V EPCOS dc film capacitors (B32778) are deemed as the best candidate for dc decoupling, because in this case 1200 V SiC MOSFET can be used with certain margins. However, there are very few types of B32778 film capacitors commercially available in the market, and 800 V B32776 series capacitors are finally chosen for dc decoupling and the power density will be slightly compromised. In contrast, the stored energy density of capacitors in ac decoupling is much lower, as seen in Fig. 4.3(b). Despite, Vishay ac film capacitors (MKP 1847) are found to be the best choice with the highest energy density, where the nominal voltage is around 350 V (or 250 Vrms). This can be easily achieved by using a buck-type decoupling method as the dc bus voltage is 400 V. Vishay ac film capacitors (MKP 1847) are thus chosen for ac decoupling.

B. Circuit topologies

Generally, there are buck (Fig. 4.1(b)), boost (Fig. 4.1(a)), and buck-boost type (Fig. 1(c)) topologies available for implementing the dc power decoupling. The buck type auxiliary circuit is not considered, because it may require at least two conversion stages in order to have a high dc offset voltage. The buck-boost-type topology "seems" to be a good choice, because it can output a high dc offset as well as a wide voltage variation so that the volume of the decoupling capacitor can be minimized. Unfortunately, the voltage stress of the switches in the auxiliary circuit is the sum of the decoupling capacitor voltage and the dc bus voltage as shown in Fig. 4.1(c), and thereby it will significantly increase the switching loss and even make the voltage stress of the auxiliary circuit go beyond 1200 V (800 V + 400 V). The boost-type topology shown in Fig. 4.1(a) is finally chosen and the required decoupling capacitance can be approximated to be,

$$C_{2_{dc}} = \frac{P_r}{2\omega_n V_{r2}(V_{C_max} - V_{r2})} = \frac{2000}{2 \times 377 \times 160 \times (800 - 160)} uF \approx 25.9uF \tag{4.6}$$

where V_{r2} is the allowed voltage ripple of the decoupling capacitor C_2, which is 0.2 $V_{c,max}$ for the EPCOS B32776 series. A single 30 uF/ 800 V film capacitor (B32776E8306K) is used together with the boost-type dc power decoupling circuit to mitigate the second-order ripple power. The volume of this capacitor is only $30mm \times 45mm \times 42mm = 56.7cm^3$.

The ac power decoupling is normally of a buck type, as shown in Fig. 4.1(d), (e) and (f). The maximum value of the peak voltage Vac of the ac decoupling capacitor can only be realized with the circuit in Fig. 4.1(f), where the required capacitance can be calculated to be,

$$C_{2_ac} = \frac{P_r}{\frac{1}{2}\omega_n V_{ac}^2} = \frac{2000}{\frac{1}{2} \times 377 \times 400^2} \approx 66.3uF \tag{4.7}$$

In this case, three 25 uF/ 250 Vrms AC film capacitors (MKP1847635314Y5) should be used, whose volume is $3 \times 30mm \times 45mm \times 42mm = 170.1cm^3$, and it is two times larger than the dc decoupling design. Actually, in addition to the larger volume, the ac decoupling circuit may have lower efficiencies, especially under light load conditions. This is because the current stress of the decoupling switches does not linearly decrease with the load power, and this will be explained in the following section.

4.2 Control strategies of the auxiliary circuits

A. DC decoupling

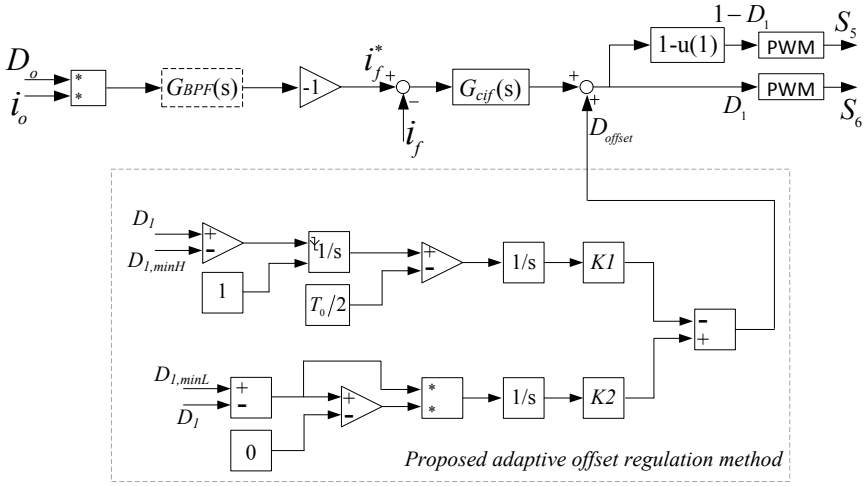
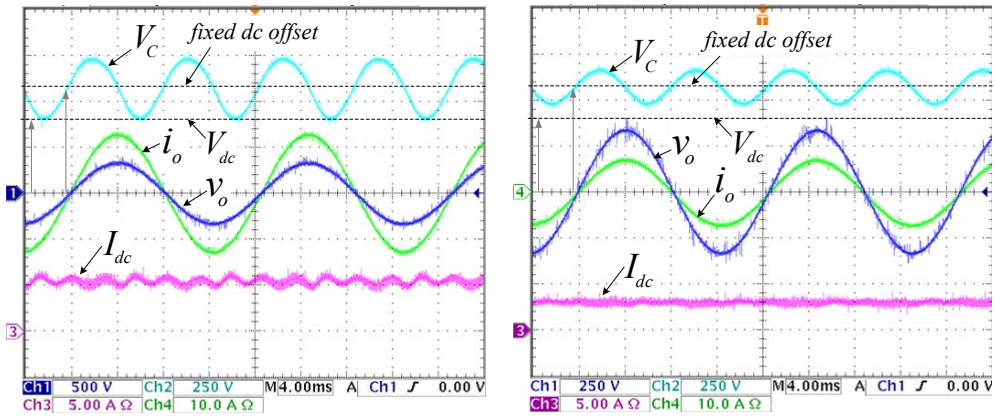


Figure 4.4: *Control strategy of the boost-type auxiliary circuit with proposed adaptive offset voltage control for the dc decoupling.*



(a) full load (b) half load

Figure 4.5: *Experimental results showing the decoupling capacitor voltage, output voltage and current, and dc link current with fixed dc offset in the decoupling capacitor voltage.*

According to (4.2) and Fig. 4.1(a), with the boost-type dc decoupling circuit, the ripple power can be compensated by regulating the decoupling current i_f to be a sinusoidal with the frequency $2\omega_n$ as following,

$$i_f^\star = \frac{-\widetilde{P_o}}{V_{dc}} = \frac{V_o I_o cos(2\omega_n t + \varphi)}{V_{dc}} = \frac{\overline{P_o}}{V_{dc}} - \frac{v_o i_o}{V_{dc}} \tag{4.8}$$

where $i_f^\star$ is the decoupling current reference. $\frac{\overline{P_o}}{V_{dc}}$ is actually used to cancel the dc component in $\frac{v_o i_o}{V_{dc}}$, which can also be realized by applying a band pass filter $G_{BPF}(s)$, as shown in Fig. 4.4. Thus $i_f^\star$ can be expressed as,

$$i_f^\star(s) = -\frac{v_o i_o}{V_{dc}} G_{BPF}(s) = -D_o i_o G_{BPF}(s) \tag{4.9}$$

$$G_{BPF}(s) = \frac{2 \times 0.33 \times 2\omega_n s}{s^2 + 2 \times 0.33 \times 2\omega_n s + (2\omega_n)^2} \tag{4.10}$$

where $D_o = \frac{v_o}{V_{dc}}$ is the instantaneous duty ratio of the inverter. The error of the decoupling current is then input into a Proportional Resonance (PR) Controller $G_{cif}(s)$ as (4.11) to obtain

the duty ratio of the boost converter, as illustrated in Fig. 4.4.

$$G_{cif}(s) = 0.02 + \frac{5s}{s^2 + (2\omega_n)^2} + \frac{5s}{s^2 + (4\omega_n)^2} + \frac{5s}{s^2 + (6\omega_n)^2} \tag{4.11}$$

It should be noted that the dc offset of v_C is a parameter that can be freely tuned. In [63], the decoupling capacitor is fed by the ac output voltage via a transformer and a rectifier in order to maintain $v_C > V_{dc}$. A relatively simpler and more cost-effective method is to set a fixed dc offset voltage for the decoupling capacitor to guarantee $v_C > V_{dc}$ for any load condition as done in [64,65]. However, with a fixed dc offset voltage, the ac component in v_C gets smaller under light load, and v_C becomes unnecessarily high as shown in Fig. 4.5(a) (full load) and Fig. 4.5(b) (half load). This directly translates into higher switching losses of S_5 and S_6 as well as faster lifetime consuming of the capacitor C_2. In order to solve these issues and meanwhile maintain a simple circuit configuration, this paper proposes an adaptive offset regulation to optimize V_C as much as possible, and the implemented control algorithm can be illustrated in the dashed box in Fig. 4.4. As seen, instead of having a fixed dc offset voltage, the idea is to maintain a fixed minimum value of v_C which is always slightly higher than the dc bus voltage regardless of load changes. In order to avoid adding another voltage sensor for measuring and controlling of v_C, an adaptive offset regulation method is realized by applying a hysteresis controller to keep the bottom value of D_1 into a small interval $[D_{1,minL}, D_{1,minH}]$, because D_1 has a one-to-one mapping with v_C as simply indicated by (4.12). The interval is very small so that the bottom value of D_1 and v_C can be considered as fixed.

$$v_C = \frac{1}{1 - D_1} V_{dc} \tag{4.12}$$

- Hysteresis controller

In order to keep the minimum value of D_1 into $[D_{1,minL}, D_{1,minH}]$, D_1 is compared with the upper and lower boundary values, as seen in Fig. 4.4. Once $D_1 < D_{1,minL}$ is detected, the D_{offset} will be increased to push D_1 up, thus $D_1 \geq D_{1,minL}$ can be simply guaranteed. To maintain the upper boundary of minimum D_1 is relatively more complicated, which cannot be directly implemented by comparing D_1 with $D_{1,minH}$. Instead, the duration of the continuous interval $D_1 \geq D_{1,minH}$ is detected, and it will be referred to as $T_{D_1 \geq D_{1,minH}}$. Once $T_{D_1 \geq D_{1,minH}} \geq \frac{T_0}{2} = \frac{\omega_n}{\pi}$ (T_0 is a fundamental period of the inverter) is detected, the bottom value of D_1 larger than $D_{1,minH}$ can be confirmed, so the D_{offset} will be decreased to pull the bottom value of D_1 back into the interval. The timer for the duration of the continuous interval $D_1 \geq D_{1,minH}$ will be reset as long as $D_1 < D_{1,minH}$ is detected. The two coefficients $K_1 = 3$ and $K_2 = 2000$ are used to adjust the dynamic response of the adaptive offset regulator. It should be noted that, the dc component in $D_o i_o$ will finally cause an offset in the duty ratio, because there is only a proportional gain for the dc component in the forward path of the con-

troller (Fig. 4.4), and the effect of this offset can be automatically cancelled by the adaptive offset regulation. Therefore, the band pass filter $G_{BPF}(s)$ used to mitigate the dc component in $D_o i_o$ can be avoided, and it is eliminated in the simulation and experimental test.

B. AC decoupling

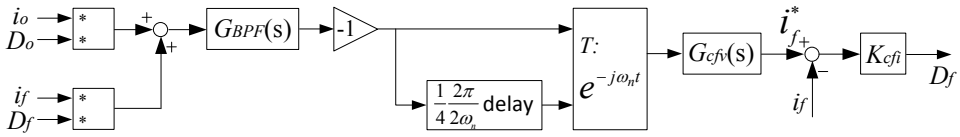


Figure 4.6: *Control diagram of the auxiliary circuit for the ac decoupling.*

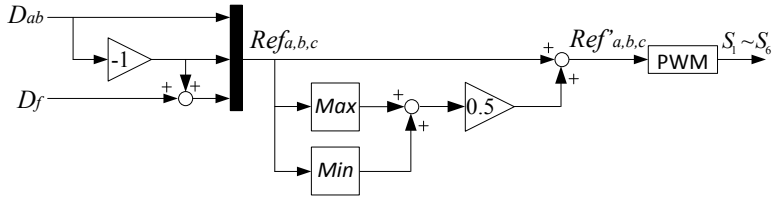


Figure 4.7: *Modulation strategy for B6 converter with ac decoupling to maximum the dc link voltage utilization.*

In ac decoupling, the terminal voltage of the decoupling capacitor is theoretically a sinusoidal as defined by (4.13). For the ripple power cancellation purpose, the decoupling capacitor voltage is necessary to be $\frac{\pi}{4}$ ahead of the inverter output voltage if the load is assumed to be resistive [29]. However in reality, the phase displacement may need a small change θ_c, because the load could be non-resistive and the ripple power caused by the filtering inductor or capacitor should also be considered. Similarly based on the instantaneous power balancing, the required voltage and current for the ac decoupling can be depicted by the following equation.

$$v_C = \sqrt{2}V_C sin(\omega_n t + \frac{\pi}{4} + \theta_C), \quad i_f = \sqrt{2}I_f sin(\omega_n t + \frac{3\pi}{4} + \theta_C) \tag{4.13}$$

where V_C and I_f are the rms voltage and current values of the coupling capacitor. The above equation shows that, being different with the dc decoupling case, the inductor current here does not linearly decrease with the load power, and therefore higher current stress and lower system efficiency may be expected for the ac decoupling under light load conditions.

Instead of using open loop power decoupling, which is simple but has relatively poor decoupling performance especially under load changes, a close loop decoupling method is designed in this chapter according to the one proposed in [68]. Since the inverter is fed by a constant dc

source, the duty ratios of the converter D_o and D_f can be regarded as the normalized output voltages. In this case, the output power and the decoupling capacitor power can be estimated from the duty ratios and the inductor currents as shown in Fig. 4.6. The sum of these two powers is then processed by the same band pass filter $G_{BPF}(s)$ as shown in (4.10) to cancel the dc component introduced by the output power and thereby derive only the ripple power. A minus one gain is then applied to obtain the error of the ripple power because the reference of the ripple power is simply zero. Since the ripple power is of second order, while in the inner current control loop, the inductor current is a fundamental component, a transformation matrix defined by (4.14) is required to assist in the reference frame transformation. As seen in Fig. 4.6, the ripple power together with a quarter cycle delay of itself are input to the matrix T, so the fundamental frequency is reduced from $2\omega_n$ to ω_n. Afterwards, a proportional resonant controller $G_{cfv}(s)$ is used to ensure a zero error tracking of the ripple power. The decoupling capacitor current is not necessary to be sinusoidal and a fast dynamic performance is more preferred. Thus, only a proportional controller $K_{cfi} = 0.02$ is used.

$$T = [cos(\omega_n t) \qquad sin(\omega_n t)] \tag{4.14}$$

$$G_{cfv}(s) = 3 + \frac{750s}{s^2 + \omega_n^2} \tag{4.15}$$

For the ac decoupling circuit presented in Fig. 4.1(f), another concern is the modulation method adopted for the B6 converter. A unipolar modulation method is normally used for the full bridge of the inverter, and the reference of phase C is obtained by adding the duty ratio of the decoupling capacitor D_f to the reference of phase B [27], as the $Ref_{a,b,c}$ in Fig. 4.7. The drawback is that the modulation indexes of the output voltage v_o and the decoupling capacitor voltage V_C cannot achieve unity at the same time, and therefore the utilization of the dc link voltage or the reduction of the decoupling capacitor cannot be optimized. In order to solve this problem, a Space Vector PWM (SVPWM) method has been proposed in [29], which is effective, but a little complicated due to the sector selection and dwell time calculation. Instead of using the space vectors a reference offset injection is applied for simplification, and it is illustrated in Fig. 4.7. The reference offset injection method is the same with the carrier-based SVPWM method, where the only difference is that the former is an unbalanced PWM method, while the latter is a balanced one.

4.3 Simulation results

In order to verify the feasibility of the proposed solution for power decoupling, simulations of the inverter circuits shown in Fig. 4.1(a) and Fig. 4.1(f) have been carried out with PLECS,

and the parameters are listed in Table 4.1.

Table 4.1: *SPECIFICATIONS OF THE SIMULATIONS AND EXPERIMENTS.*

Parameters	**Values**	
	dc decoupling	**ac decoupling**
Nominal power	$2kW$	
DC-link voltage	$400V$	
AC output voltage v_{ab}	$240Vrms/60Hz$ (resistive load)	
Switching frequency f_s	$30kHz$	
AC filter inductor L_1, L_2	$1mH$	
DC link capacitor C_1	$30uF$	
Decoupling capacitor C_2	$30uF/800V$ B32776E8306K	$3 \times 25uF/250Vrms$ MKP1847635314Y5
Boundary of the hysteresis controller $[D_{1,minL}, D_{1,minH}]$	—	$[0.01, 0.05]$ $(V_{C,min} \in [404V, 421V])$
Power switches $S_1 \sim S_6$	$C2M0080120D$	

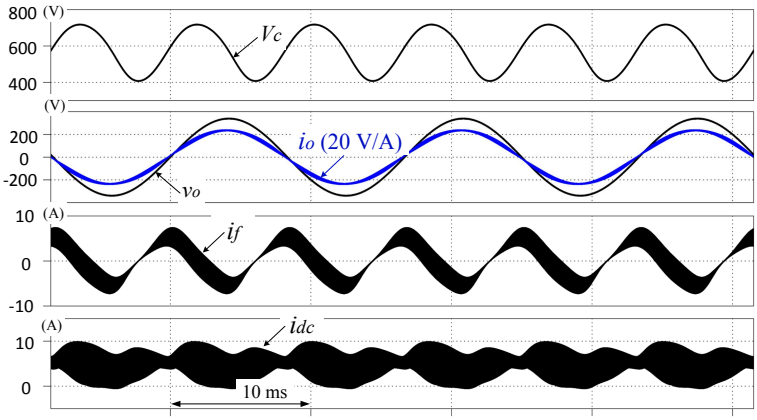


Figure 4.8: *Simulation results with dc decoupling during steady state at full load condition.*

The simulation results are presented in Fig. 4.8 to Fig. 4.11. As seen, the second order harmonic in the dc link current is significantly mitigated by both dc decoupling (Fig. 4.8) and ac decoupling (Fig. 4.10) circuits. Furthermore, with dc decoupling the voltage of the

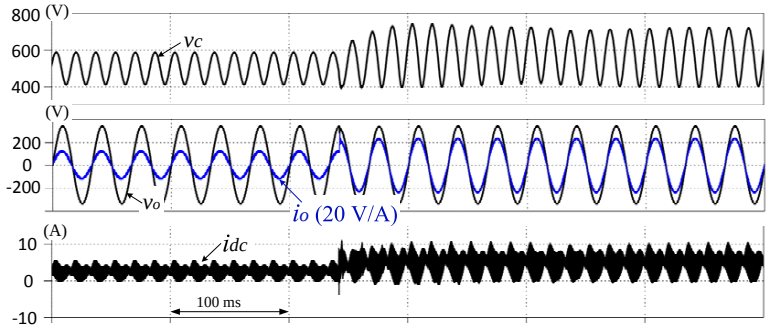


Figure 4.9: *Simulation results with dc decoupling during load step-up at full load condition.*

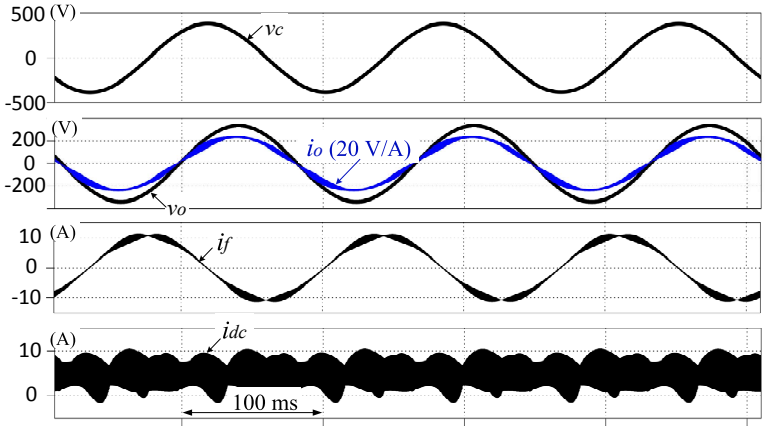


Figure 4.10: *Simulation results with ac decoupling during steady state at full load condition.*

decoupling capacitor V_C is higher than the dc link voltage due to the boost operation, and its ac component is dominated by the second order. While for the ac decoupling, the circuit still operates in the buck mode and v_C is between $[-V_{dc}, V_{dc}]$, and it is a sinusoidal with the fundamental frequency. Moreover, the decoupling current i_f in the ac decoupling is higher than that in dc decoupling, and thus the efficiency reduction caused by ac decoupling might be higher than the dc decoupling case, which will later be proved by the experimental results in Section 4.3. In addition to the steady-state operation, the dynamic performances of the two power decoupling solutions are verified by the simulations as well, and they are shown in Fig.

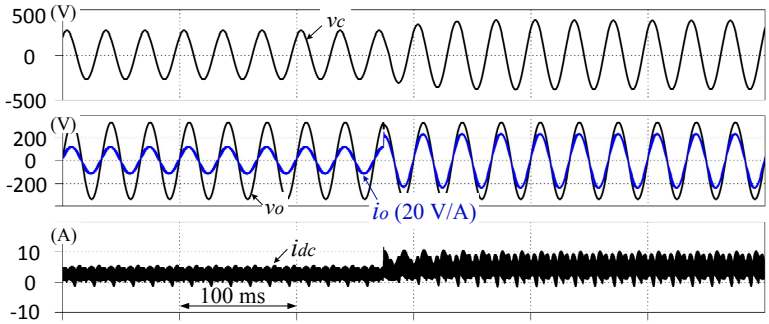


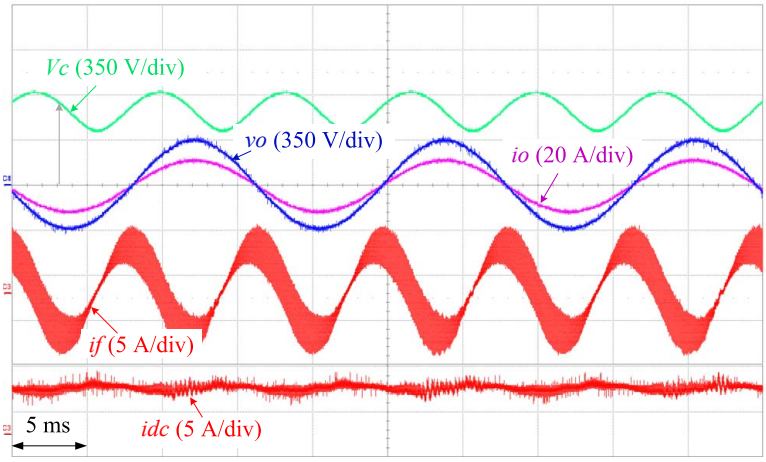
Figure 4.11: *Simulation results with ac decoupling during load step-up at full load condition.*

4.9 and Fig. 4.11, respectively. As seen from Fig. 4.9, with dc decoupling, a fixed bottom value is ensured for the decoupling capacitor voltage v_C by using the proposed adaptive offset regulation. In this case, the voltage stress of the decoupling switches S_5 and S_6 will always be lower than the case, when a fixed dc offset is applied to V_C. Therefore, the switching losses can be reduced. It is also noted that with both decoupling circuits, the reduction of the second order harmonics in the dc current can be always realized regardless of the load condition, which demonstrates the effectiveness of the closed loop control.

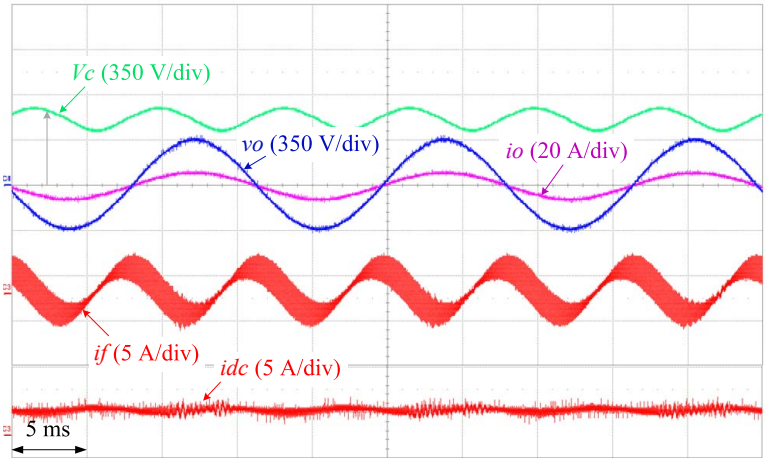
4.4 Experimental results

The proposed active power decoupling solution was also verified on a 2 kW prototype, whose parameters are the same with those used for simulations in Section 4.3. The final experimental results are presented in Fig. 4.12 to Fig. 4.15. The steady state performances of the dc and ac decoupling are shown respectively in Fig. 4.12 and Fig. 4.14, where the second order harmonic in the dc link current i_{dc} is well mitigated no matter if it is in half or full load condition. Fig. 4.13 and Fig. 4.15 show the transient responses of the dc and ac decoupling during decoupling function enabling and load change, respectively, which as seen are smooth and fast. Moreover, a fixed minimum voltage of the decoupling capacitor can be observed during the load step-up in Fig. 4.13 (b), and this matches well with the simulation results presented in Fig. 4.9. The efficiency of the system and the lifetime of the decoupling capacitor are expected to be improved as compared with the case shown in Fig. 4.5, where a fixed dc offset $D_{offset} = 0.3$ is used and the corresponding dc component of v_C is $V_{dc} \times \frac{1}{1-0.3} = 575V$.

The efficiency curves of the system under different control schemes and decoupling circuits were also measured by a Voltech PM3000A Universal Power Analyzer, and the results are



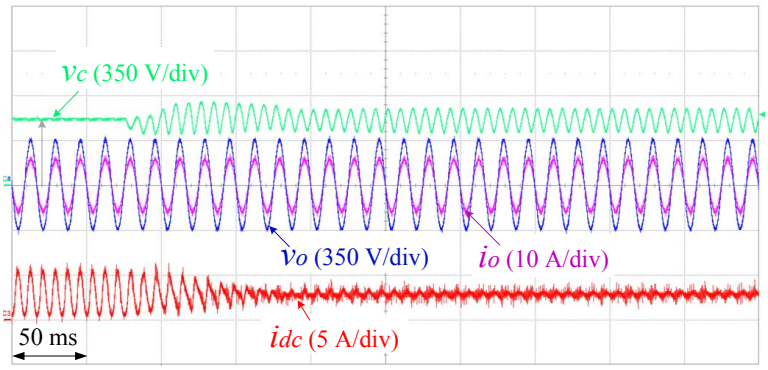
(a) full load



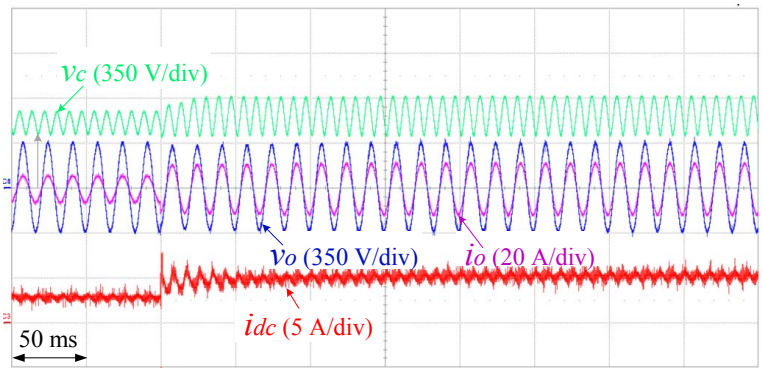
(b) half load

Figure 4.12: *Experimental results showing the steady state performance of dc decoupling at full load condition.*

summarized and presented in Fig. 4.16. It is clear that the proposed adaptive decoupling control method will stand out because its efficiency reduction is the lowest as compared to the other two decoupling solutions. Thanks to the adaptive decoupling voltage control, under light load conditions, the current and voltage stresses of the decoupling circuit are low and the



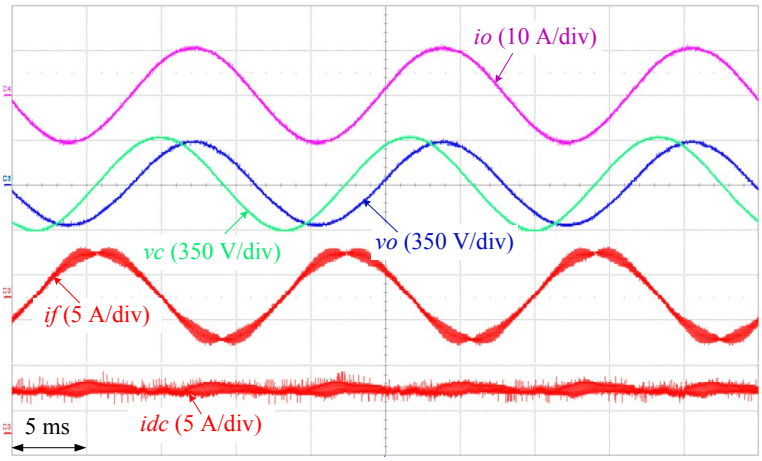
(a) enabling decoupling control



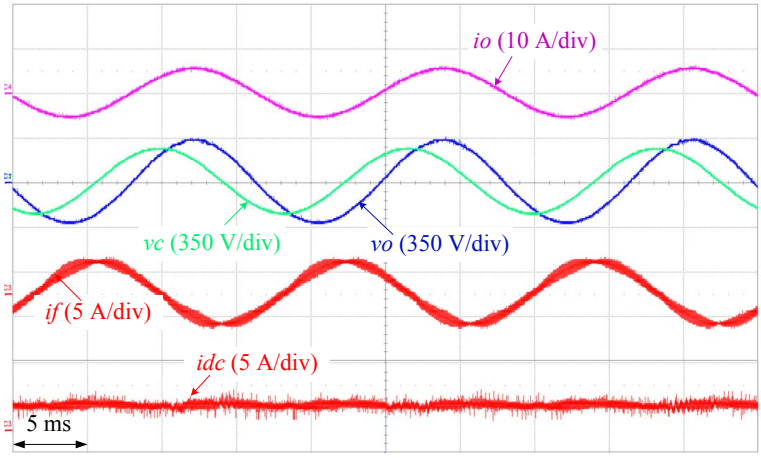
(b) load step-up

Figure 4.13: *Experimental results showing the transient responses of dc decoupling at full load condition.*

efficiency reduction is basically negligible. Under high load conditions, approximately 0.5% efficiency drop is observed because the boost decoupling circuit may need to handle a relatively high ripple power. When the proposed adaptive control is disabled and the decoupling voltage is fixed at 575 V, the efficiency reduction under light load conditions becomes more significant because of the higher voltage stress, and it is more than 1% when $\frac{1}{8}$ of the nominal load is applied to the system. In addition to the dc decoupling tests, the efficiency of the ac decoupling circuit shown in Fig. 4.1(f) was also tested and presented in Fig. 4.16 for comparison. As seen, it is much lower than the dc decoupling case no matter the proposed adaptive offset regulation is activated or not. The efficiency reduction is more than 1% at full load condition and about



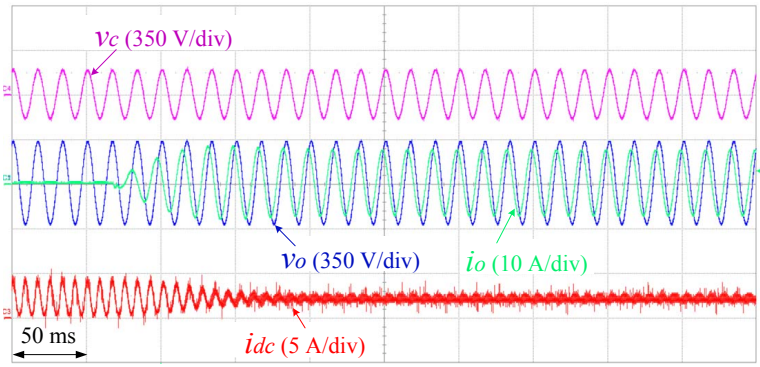
(a) full load



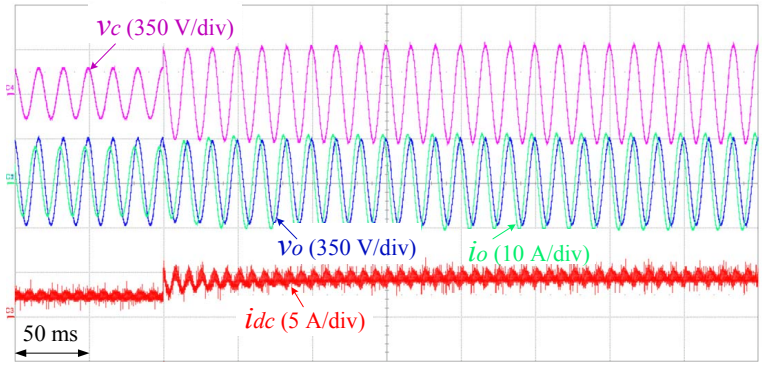
(b) half load

Figure 4.14: *Experimental results showing the steady state performance of ac decoupling at full load condition.*

2% $\sim$ 3% under light load condition. As mentioned, this is mainly because the current in the ac decoupling circuit does not linearly decrease with the load power. The physical dimensions of the capacitors used for dc and ac decoupling, which is another critical concern related to the power density, are shown in Fig. 4.17. As seen, the volume of the capacitor for dc decoupling



(a) enabling decoupling control



(b) load step-up

Figure 4.15: *Experimental results showing the transient responses of ac decoupling at full load condition.*

is only about $\frac{1}{3}$ of the total volume of the three capacitors for ac decoupling. This is in consistence with the investigations shown in Fig. 4.3, where the stored energy density of dc decoupling is about 3 times of the ac decoupling case. Note that, the prototype shown in Fig. 4.17 has a volume larger than 40 in^3, which is the maximum value required by the *Little Box Challenge*, but its volume is not optimized. The prototype is built only to verify the feasibility and effectiveness of the active power decoupling auxiliary circuit. In fact, the heatsink can be significantly shrinked and the overall converter can be made more compact.

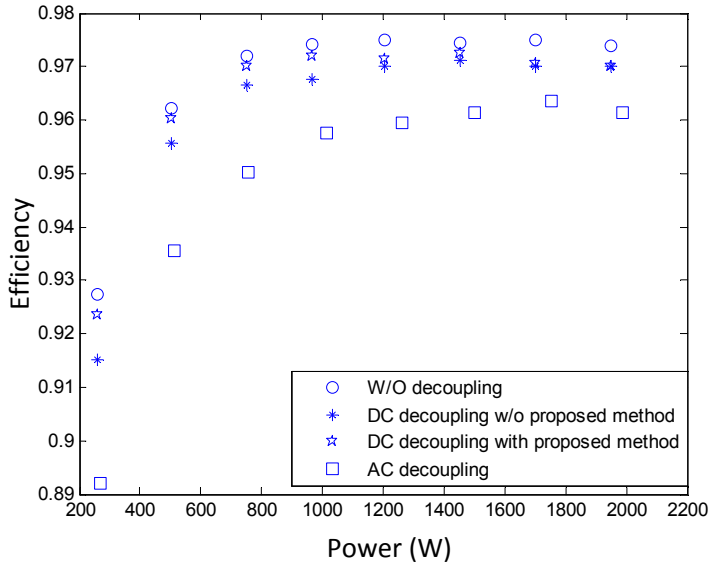


Figure 4.16: *Efficiency of the inverter versus the load power.*

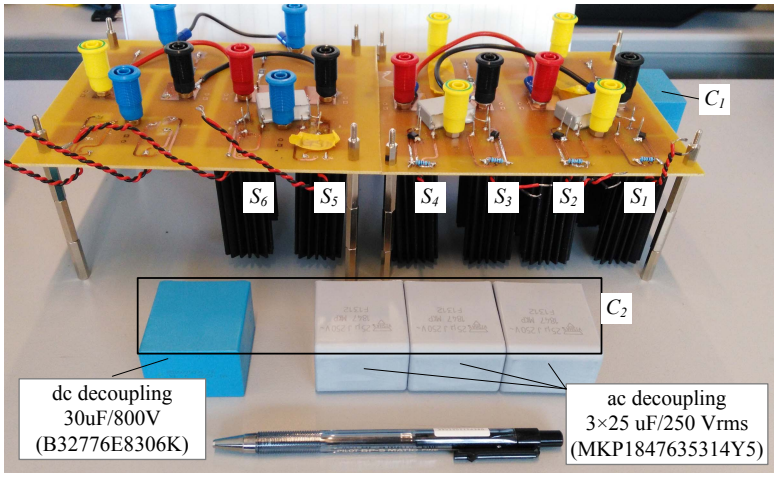


Figure 4.17: *Film capacitors used for dc and ac decoupling together with the 2 kW single-phase power converter prototype.*

4.5 Summary

In this chapter, an optimal design of ac and dc APD circuits for kW scale single-phase inverters is presented in order to achieve high power density and high efficiency. Different active power

decoupling topologies are evaluated and compared, among which, the boost-type dc power decoupling circuit is found to be best suited for this specific application. The results show that with the proposed solution, the dc bus current ripple of a 2 kW prototype can be significantly reduced by utilizing only a single 30 uF/800 V film capacitor in dc decoupling, instead of a large electrolytic capacitor bank. Moreover, the efficiency drop caused by the auxiliary circuit is sizably reduced under light load conditions by implementing an improved adaptive control strategy. The ac decoupling circuit is also studied for a detailed comparison, where the best solution is to use three 25 uF/250 Vrms film capacitors in parallel. However, the capacitor volume for the ac decoupling is about 3 times of that for the dc decoupling, and the efficiency of the former is significantly lower as well.

Part III

Three-phase ac-dc-ac converters

After studying single-phase converters in Part II, this part moves the focus to three-phase converters. Unlike single-phase converters, which have several topological options, the three-phase converters are dominated by the B6 converters. Their control has also mature after many decades of application. Despite that, there is still possibilities for other topologies as well as control strategies to be developed with enhanced performance for certain specific applications. Therefore, the nine-switch converter, as a reduced-switch version of two B6 converters connected back-to-back, will be studied in Chapter 5, where its appropriate application area with better performance has been identified. In chapter 6, a new design method for the rotating speed controller of wind turbines will also be presented for improving thermal loading in the wind power converter.

5 Application criteria for three-phase nine-switch converters

The nine-switch topology is derived from two B6 converters connected back-to-back (BTB). As seen in Fig. 5.1, two phase legs from converter #1 and #2, respectively, are merged together to compose one phase leg of the nine switch converter, and meanwhile one switch is dismissed. Thus nine-switch converters have only three phase legs and each of them has only three switches. With such a topology, nine-switch converters retain the DC-link and can achieve all the functions of twelve-switch BTB even with three switches less. However, like the other reduced switch topologies, the introduced constraint cannot be easily eliminated, e.g. the upper reference should always be above the lower one, as shown in Fig. 5.2, so the DC-link voltage of nine-switch covnerters needs to be doubled when the upper and lower terminals have different frequencies. The application criteria, where these constraints can be relieved, are thus studied in this chapter as following.

5.1 Instantaneous switch currents

Instantaneous switch currents flowing in the nine-switch converter have a one-to-one map with the BTB converter according to Fig. 5.1(a) and (b). The only exception is $SA2$ of the nine-switch converter, which instead of a single equivalence, is mapped to $SA2'$ and $SA2''$ of the BTB converter. The instantaneous currents flowing through these switches can then be derived for a typical half-carrier period like shown in Fig. 5.3 based on current directions indicated in Fig. 5.1(a) and (b). Unlike the switches of the BTB converter, which carry one terminal current (i_U or i_D) each, the switches $SA1$ and $SA3$ of the nine-switch converter carry both terminal currents simultaneously ($\pm(i_U + i_D)$). Their combined currents can hence be either higher or lower than the individual currents depending on their relative frequency, phase and amplitude.

5.2 Loss comparison

Referring to Fig. 5.3, the following observations can be summarized.

• At the end of T_1, $SA1$ and $SA1'$ switch on the same current $-i_U$. The same applies to $SA2$ and $SA2'$, which switch off the same current i_U. The other switches do not commutate at this instant.

• At the beginning of T_3, $SA3$ and $SA3'$ switch off the same i_D, while $SA2$ and $SA2''$ switch on the same $-i_D$. The other switches do not commutate at this instant.

The switching losses of the nine-switch and BTB converters are therefore close with the

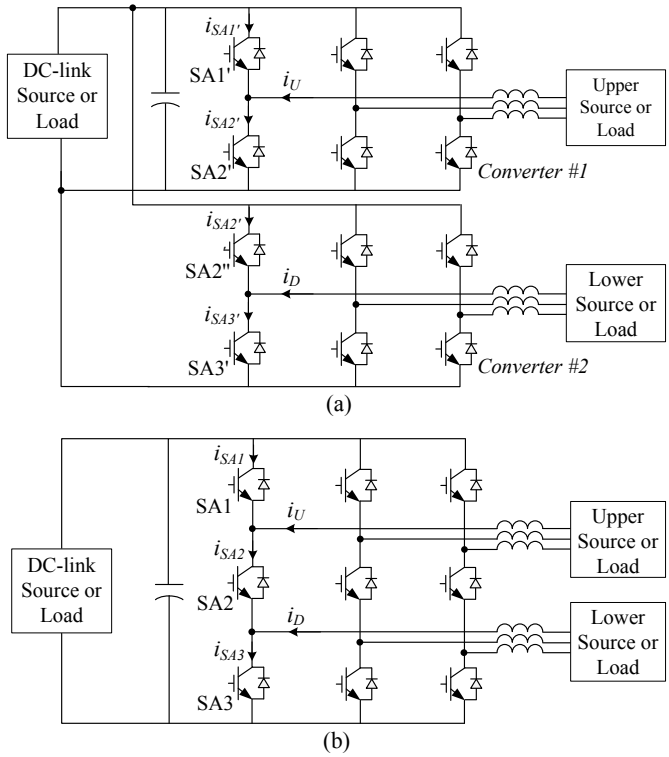


Figure 5.1: *Illustration of (a) twelve-switch BTB and (b) nine-switch power converters.*

same DC-link voltage enforced by following the recommendations provided in [12] and [100]. However, conduction losses of the two converters are different, caused by the different switch currents during T_1 and T_3. These losses are either proportional to the average or root-mean-square (RMS) switch currents depending on the types of devices used. A loss comparison between the two converters can thus be performed by computing their average and Root-Mean-Square (RMS) switch current differences during T_1 and T_3, like given in (5.1) and (5.2).

$$\Delta|i|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left[(|i_U + i_D| - |i_U|) \times \frac{T_3}{T} + (|i_U + i_D| - |i_D|) \times \frac{T_1}{T}\right] dt \tag{5.1}$$

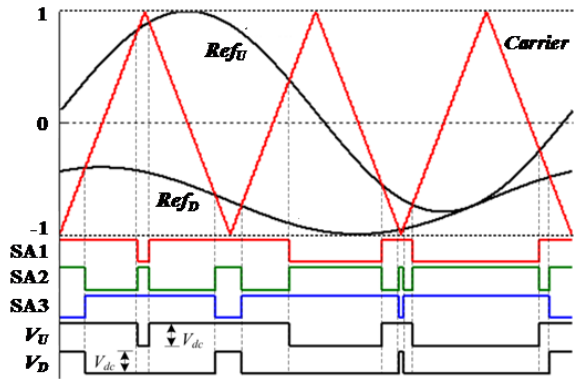
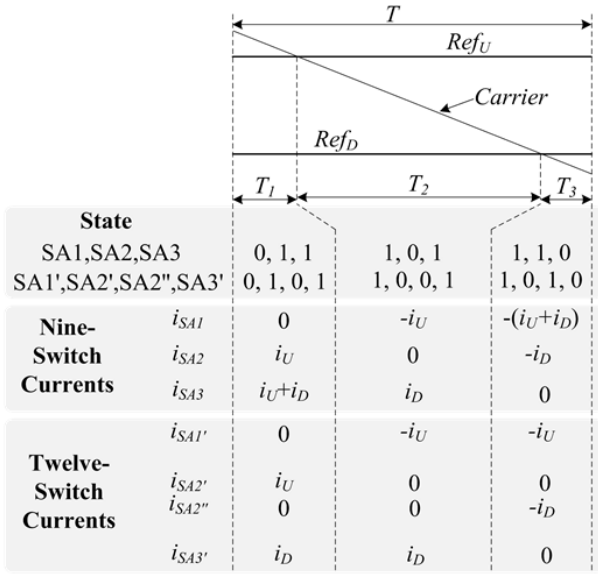


Figure 5.2: *Modulation of nine-switch converter.*



State				
SA1,SA2,SA3		0, 1, 1	1, 0, 1	1, 1, 0
SA1',SA2',SA2'',SA3'		0, 1, 0, 1	1, 0, 0, 1	1, 0, 1, 0
Nine-Switch Currents	i_{SA1}	0	$-i_U$	$-(i_U+i_D)$
	i_{SA2}	i_U	0	$-i_D$
	i_{SA3}	i_U+i_D	i_D	0
Twelve-Switch Currents	$i_{SA1'}$	0	$-i_U$	$-i_U$
	$i_{SA2'}$	i_U	0	0
	$i_{SA2''}$	0	0	$-i_D$
	$i_{SA3'}$	i_D	i_D	0

Figure 5.3: *Instantaneous switch currents of nine-switch and BTB converters when in a half-carrier period.*

$$\Delta i_{RMS}^2 = \frac{\omega}{2\pi}\int_0^{2T}\left\{[(i_U+i_D)^2 - i_U^2]\times\frac{T_3}{T} + [(i_U+i_D)^2 - i_D^2]\times\frac{T_1}{T}\right\}dt \tag{5.2}$$

where ω is the angular frequency of the integration period, T is half of the switching period,

and $\Delta|i|_{Av} < 0$ and/or $\Delta i^2_{RMS} < 0$ indicate lower conduction, and hence total (since switching losses are the same for both converters), losses for the nine-switch converter. Expressions for the three time intervals per half-carrier period can also be derived as (5.3) upon applying a basic geometry to Fig. 5.3.

$$\begin{cases} T_1 = 0.5T(1 - Ref_U) \\ T_2 = T - T_1 - T_3 \\ T_3 = 0.5T(1 + Ref_D) \end{cases} \tag{5.3}$$

Other expressions are needed for solving (5.1) and (5.2) depending on the types of energy conversions considered. In this chapter, both the ac-ac common-frequency conversion found in UPSs [13] and ac-dc different-frequency conversion found in a hybrid renewable energy system [100] will be considered since they have earlier been demonstrated to require a low DC-link voltage. Upon being proven efficient, they may hence be attractive applications for the nine-switch converter.

5.2.1 AC-AC common-frequency mode

In this mode, the two modulating references shown in Fig. 5.3 can be expressed as:

$$\begin{cases} Ref_U = M_U cos(\omega t + \varphi_U) + M_{oU} \\ Ref_D = M_D cos(\omega t + \varphi_D) - M_{oD} \end{cases} \tag{5.4}$$

where M_x, φ_x and M_{ox} represent the amplitude, phase and offset of reference $x(= UorD)$. The offset M_{ox} is mainly a constant added for shifting Ref_U up and/or Ref_D down to avoid them crossing each other, which as earlier mentioned, is not permitted for the nine-switch converter. Also noting that the instantaneous currents through $SA1$ and $SA3$ are represented by $\pm(i_U + i_D)$, their values will be smaller if i_U and i_D are of opposite polarities, or have a phase displacement φ close to 180^o. That means an ac source connected to one terminal and an ac load connected to the other terminal from the same phase-leg like in an on-line UPS [13, 111]. Expressions for i_U and i_D can hence be expressed as:

$$\begin{cases} i_U = I_U cos(\omega t + \varphi) \\ i_D = -I_D cos(\omega t) \end{cases} \tag{5.5}$$

where I_x represents their respective amplitudes ($x = UorD$). Substituting (5.3) to (5.5) into

(5.1) and (5.2) then results in:

$$\Delta|i|_{Av} = \frac{1}{\pi}(2 - M_{oU} - M_{oD})\sqrt{I_U^2 + I_D^2 - 2I_U I_D cos\varphi} - \frac{1}{\pi}(1 - M_{oD})I_U - \frac{1}{\pi}(1 - M_{oU})I_D$$

$$\Delta i_{RMS}^2 = \frac{1}{4}(1 - M_{oU}) \times I_U^2 + \frac{1}{4}(1 - M_{oD}) \times I_D^2 - \frac{1}{2}(2 - M_{oU} - M_{oD}) \times I_U I_D cos\varphi \tag{5.6}$$

(5.7)

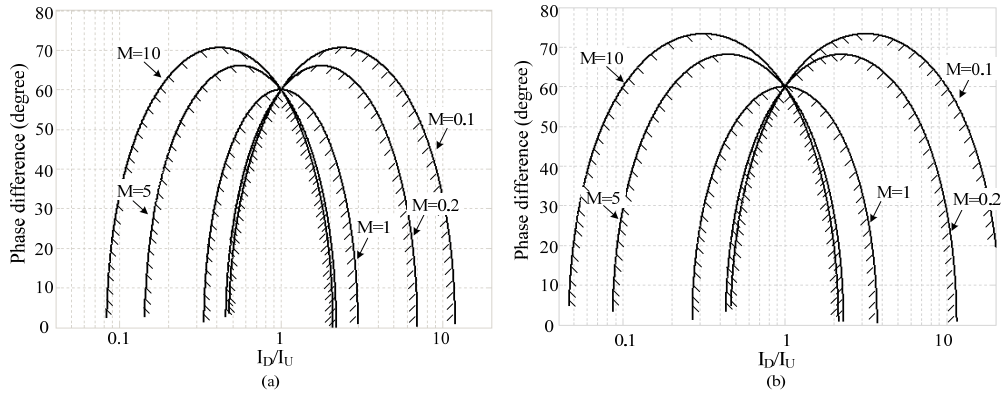


Figure 5.4: *Maximum phase displacement between upper and lower terminal currents when in ac-ac mode.* $M = \frac{1-M_{oD}}{1-M_{oU}}$*, (a)* $\Delta i_{Av} < 0$*, (b)* $\Delta i_{RMS}^2 < 0$*, and the shaded side indicating where the nine-switch converter has lower losses.*

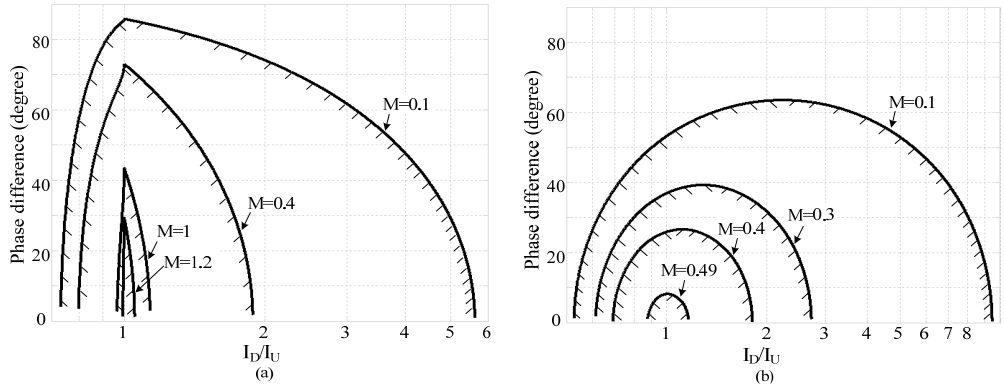


Figure 5.5: *Maximum phase between the upper terminal voltage and current when in ac-dc mode.* $M = \frac{1-M_{oD}}{1-M_{oU}}$*, (a)* $\Delta i_{Av} < 0$*, (b)* $\Delta i_{RMS}^2 < 0$*, and the shaded side indicating where the nine-switch converter has lower losses.*

To have lower conduction losses for the nine-switch converter, the earlier mentioned conditions are $\Delta|i|_{Av} < 0$ and/or $\Delta i^2_{RMS} < 0$, which when applied to (5.6) and (5.7), result in those boundary plots shown in Fig. 5.4(a) and (b) for different $\frac{I_D}{I_U}$ and $M = \frac{1-M_{oD}}{1-M_{oU}}$. The values read from these figures correspond to the maximum phase displacement φ_{max} between the two terminal currents, below which, the nine-switch converter will have lower conduction losses. The area below each boundary curve can thus be defined as the Lower Loss Area (LLA) for the nine-switch converter. In addition, it should be noted that although φ_{max} clearly changes with $\frac{I_D}{I_U}$ and M, its value remains constant at 60^o when $\frac{I_D}{I_U} = 1$.

5.2.2 AC-DC different-frequency mode

In this mode, the references used with the nine-switch converter can be expressed as:

$$\begin{cases} Ref_U = M_U cos(\omega t) + M_{oU} \\ Ref_D = -M_{oD} \end{cases} \tag{5.8}$$

where the lower reference Ref_D is a dc constant. The terminal currents of the converter can similarly be expressed as:

$$\begin{cases} i_U = I_U cos(\omega t + \varphi) \\ i_D = I_D \end{cases} \tag{5.9}$$

where the lower current again is a constant. A suitable application with such a configuration is in the case of tying multiple green power sources, e.g. PVs, fuel cells, and wind turbines, to a dc microgrid. The upper ac terminals can be tied to a wind or diesel generator, while the lower dc terminals can be tied to a combination of low-voltage fuel cells and photovoltaic sources (usually accompanied by energy storage for power smoothening purposes). The sources generate power in harmony for eventual feeding to the dc microgrid connected to the dc bus of the converter.

Substituting (5.3), (5.8) and (5.9) into (5.1) and (5.2) then results in:

$$\begin{aligned} &\Delta|i|_{Av} = \tfrac{1}{2\pi} M_U cos\varphi \left[\tfrac{I_D}{I_U} \sqrt{1 - \left(\tfrac{I_D}{I_U}\right)^2} - asin\left(\tfrac{I_D}{I_U}\right) \right] \times I_U \\ &+ \tfrac{1}{\pi}(2 - M_{oU} - M_{oD}) \left[\sqrt{1 - \left(\tfrac{I_D}{I_U}\right)^2} + \tfrac{I_D}{I_U} asin\left(\tfrac{I_D}{I_U}\right) \right] \times I_U \\ &- \tfrac{1}{\pi}(1 - M_{oD}) \times I_U - \tfrac{1}{2}(1 - M_{oU}) \times I_D, \qquad if I_D < I_U \end{aligned} \tag{5.10}$$

$$\Delta|i|_{Av} = -\frac{1}{\pi}(1 - M_{oD}) I_U + \frac{1}{2}(1 - M_{oD}) I_D - \frac{1}{4} M_U I_U cos\varphi, \quad if I_D \geq I_U \tag{5.11}$$

$$\Delta i^2_{RMS} = \frac{1}{4}(1 - M_{oD})I_U^2 + \frac{1}{2}(1 - M_{oD})I_D^2 - \frac{1}{2}M_U I_U I_D cos\varphi \tag{5.12}$$

Applying $\Delta|i|_{Av} < 0$ to (5.10) or (5.11) and $\Delta i^2_{RMS} < 0$ to (5.12) eventually leads to the boundary curves shown in Fig. 5.5(a) and (b) for different I_D/I_U and M. These curves give the maximum phase difference φ_{max} between the upper current and voltage, below which, the nine-switch converter will have lower conduction losses. Areas bounded by these curves are therefore the LLAs, whose sizes increase as M decreases. Based on the definition of $M = \frac{1-M_{oD}}{1-M_{oU}}$, it means shifting both modulating references Ref_U and Ref_D lower by decreasing M_{oU} and increasing M_{oD}, while keeping them within a carrier band with Ref_U always above Ref_D. Moreover, a maximum φ_{max} is observed to exist only when $M \leq 1.2$ if the conduction losses are related to the average switch current (Fig. 5.5(a)) and $M \leq 0.49$ if the conduction losses are related to the RMS switch current (Fig. 5.5(b)). Above those identified M values, the losses of the nine-switch converter will always be higher, and therefore not as attractive as the BTB converter even if it uses less switches.

The same analysis above can be repeated with the lower dc terminal current assumed to flow out of the converter. That means $i_D = -I_D$ in Fig. 5.1(a) and (b), whose correspondingly derived loss equations give no LLA. The losses of the nine-switch converter are therefore always higher when the lower terminal is supplying power, while the upper terminal is drawing power. The conditions of $i_D = I_D$ and $i_D = -I_D$, when considered for half a cycle each, can also be used for explaining why the nine-switch converter is not suitable for the ac-ac conversion at different frequency mode, where benefits gained during the former are lost during the latter. The ac-ac different-frequency mode is therefore not explicitly studied in this paper.

5.2.3 Comparison with other reduced switch topologies

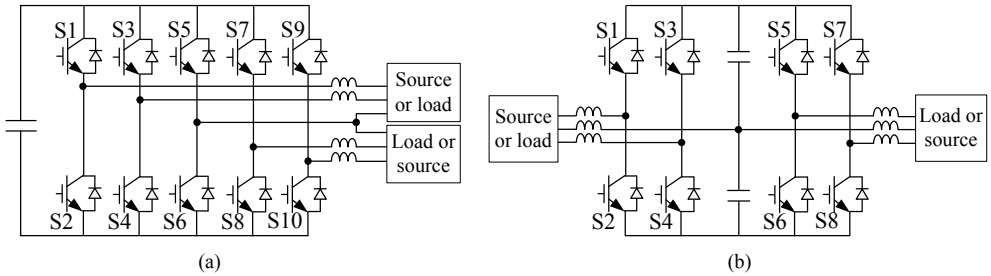


Figure 5.6: *Other reduced switch topologies. (a) a ten-switch converter (b) an eight-switch converter.*

After demonstrating the loss advantage of the nine-switch converter, when compared with

the BTB converter, it might be informative to know how the nine-switch converter is compared with other reduced switch topologies like the ten-switch converter proposed in [112], as shown in Fig. 5.6(a). The ten-switch converter is almost like the BTB converter shown in Fig. 5.1(a), but with one upper phase-leg and one lower phase-leg merged together. The merged phase-leg will hence supply one upper terminal and one lower terminal simultaneously with its switch current magnitude expressed as $|i_U + i_D|$. This is the same current that will flow through $SA1$ and $SA3$ of the nine-switch converter, whose resulting losses generated are smaller when operating within those earlier identified LLAs. The lower losses are however experienced by only two switches of the ten-switch converter, as compared to six switches of the nine-switch converter. The latter is therefore anticipated to be more efficient when operating within its LLAs.

Another topology that might be recommended for comparison is the eight-switch converter proposed in [113], as shown in Fig. 5.6(b), which when compared with the ten-switch converter, uses two split dc capacitors for replacing the shared phase-leg. The resulting eight-switch converter therefore uses the least number of switches, but experiences the highest doubled dc bus voltage, which unfortunately, cannot be reduced. Switching losses of the eight-switch converter are therefore much higher, while its conduction losses are merely shifted from the saved switches to the split dc bus capacitors. The eight-switch converter is hence not further evaluated in this paper.

5.3 Loss distribution

Section 5.2 marks out LLAs for the nine-switch converter, within which, its losses are lower than those of the BTB converter. This section continues by investigating its conduction loss distribution among switches, which should preferably not vary widely judging from the reliability prospective. Individual average and RMS switch currents of the nine-switch and BTB converters are therefore computed and compared to identify the operating regions, where the nine-switch converter will experience improved loss distribution. The expressions obtained are listed from (5.13) to (5.26), which can further be refined for ac-ac and ac-dc conversions, presented in the next two subsections.

Nine-Switch Converter

$$|i_{SA1}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left[|i_U| \times \frac{T_2}{T} + |i_U + i_D| \times \frac{T_3}{T}\right] dt \tag{5.13}$$

$$|i_{SA2}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left[|i_U| \times \frac{T_1}{T} + |i_D| \times \frac{T_2}{T}\right] dt \tag{5.14}$$

$$|i_{SA3}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left[|i_U + i_D| \times \frac{T_1}{T} + |i_D| \times \frac{T_2}{T}\right] dt \tag{5.15}$$

$$i_{SA1}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left[i_U^2 \times \frac{T_2}{T} + (i_U + i_D)^2 \times \frac{T_3}{T}\right] dt \tag{5.16}$$

$$i_{SA2}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left[i_U^2 \times \frac{T_1}{T} + i_D^2 \times \frac{T_2}{T}\right] dt \tag{5.17}$$

$$i_{SA3}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left[(i_U + i_D)^2 \times \frac{T_1}{T} + i_D^2 \times \frac{T_2}{T}\right] dt \tag{5.18}$$

Twelve-Switch Converter

$$|i_{SA1'}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left(|i_U| \times \frac{T_2 + T_3}{T}\right) dt \tag{5.19}$$

$$|i_{SA2'}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left(|i_U| \times \frac{T_1}{T}\right) dt \tag{5.20}$$

$$|i_{SA2''}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left(|i_D| \times \frac{T_3}{T}\right) dt \tag{5.21}$$

$$|i_{SA3'}|_{Av} = \frac{\omega}{2\pi}\int_0^{2T}\left(|i_D| \times \frac{T_1 + T_2}{T}\right) dt \tag{5.22}$$

$$i_{SA1'}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left(i_U^2 \times \frac{T_2 + T_3}{T}\right) dt \tag{5.23}$$

$$i_{SA2'}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left(i_U^2 \times \frac{T_1}{T}\right) dt \tag{5.24}$$

$$i_{SA2''}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left(i_D^2 \times \frac{T_3}{T}\right)dt \tag{5.25}$$

$$i_{SA3'}{}^2_{RMS} = \frac{\omega}{2\pi}\int_0^{2T}\left(i_D^2 \times \frac{T_1+T_2}{T}\right)dt \tag{5.26}$$

5.3.1 AC-AC common-frequency mode

The references and currents for this mode of operating are earlier given in (5.4) and (5.5), which when substituted with (5.3) into (5.13) to (5.26), give rise to (7.1)-(7.14) in Appendix A. Individual switch conduction losses of the nine-switch converter therefore depend on both sets of terminal parameters from the same phase-leg, while those of the twelve-switch converter depend on only one set of terminal parameters. To illustrate how they are compared, the online ac-ac nine-switch UPS mentioned in [13] is considered, whose input and output voltages, like all online UPSs, are nearly equal. Assumptions specified in (5.27) can hence be applied, which in terms of LLA (area within which the nine-switch converter will have lower losses), correspond to that with $M = 1$ in Fig. 5.4.

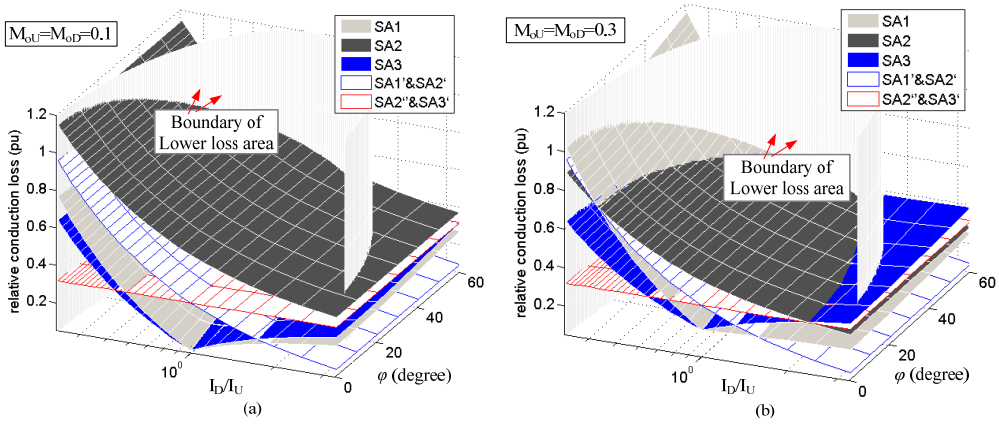


Figure 5.7: *Conduction loss distribution of the nine-switch converter when in ac-ac mode based on average switch current computation ($I_D = 1 \quad pu, M = 1$) (a) $M_{oU} = M_{oD} = 0.1$ (b) $M_{oU} = M_{oD} = 0.3$.*

$$M_U \approx M_D, \quad M_{oU} \approx M_{oD} \quad and \quad \varphi_U \approx \varphi_D \tag{5.27}$$

It should however be noted that the same LLA with unity M can be obtained with different M_{ox} (x=U,D) offset values, whose impacts on the individual switch conduction losses can be seen in Fig. 5.7 and Fig. 5.8 for the cases of $M_{oU} \approx M_{oD} = 0.1 \quad and \quad 0.3$, respectively. In

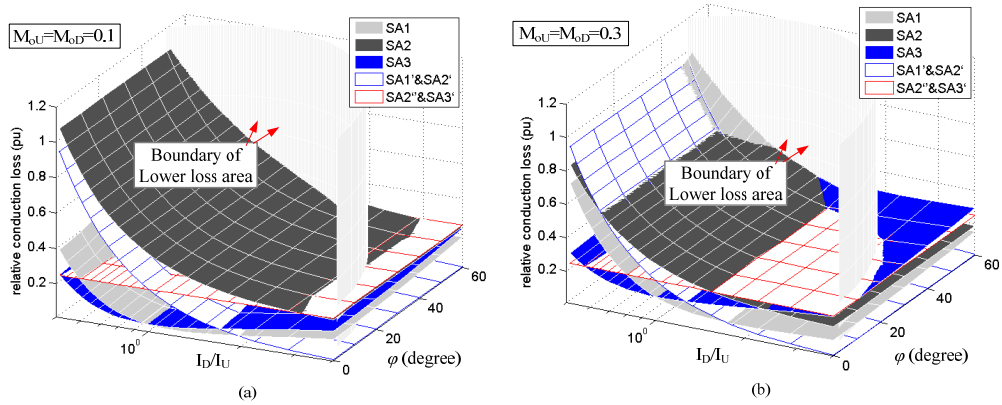


Figure 5.8: *Conduction loss distribution of the nine-switch converter when in ac-ac mode based on RMS switch current computation ($I_D = 1 \quad pu, M = 1$) (a) $M_{oU} = M_{oD} = 0.1$ (b) $M_{oU} = M_{oD} = 0.3$.*

these plots, the current ratio $\frac{I_D}{I_U}$ and ac load phase φ are varied, while arbitrarily keeping I_D fixed. The individual switch conduction losses of the twelve-switch BTB converter are also shown in Fig. 5.7 and 5.8 for comparison, but with $M_{oU} \approx M_{oD}$ set to zero since the offset is unnecessary for the BTB converter. These plots clearly reflect the same LLA with $M = 1$, but with different loss distributions among the switches of the nine-switch converter. The trends observed are a decrease in conduction losses of $SA2$ and an increase in the conduction losses of $SA1$ and $SA3$, as φ and M_{ox} increase regardless of whether the average or RMS switch currents are considered. The outcome is a better sharing of losses among the three switches per phase-leg, which thus better matches the equal loss distribution observed with the BTB converter. The conduction losses of $SA1$ and $SA3$ of the nine-switch converter are also noted to be the lowest, when $I_U = I_D$ and $\varphi = 0$, since they correspond to the largest cancellation of instantaneous switch currents through these switches. It is thus possible for the nine-switch converter to be more efficient than the BTB converter when operating in the LLA, while yet maintaining an appropriate M_{ox} for better spreading the losses among the switches in the converter.

5.3.2 AC-DC different-frequency mode

The conduction losses of the switches in this mode are evaluated by substituting (5.3), (5.8) and (5.9) into (5.13) to (5.18) for the nine-switch converter and (5.19) to (5.26) for the BTB converter. The expressions obtained are summarized as (7.3.3)-(7.26) in Appendix A. Again,

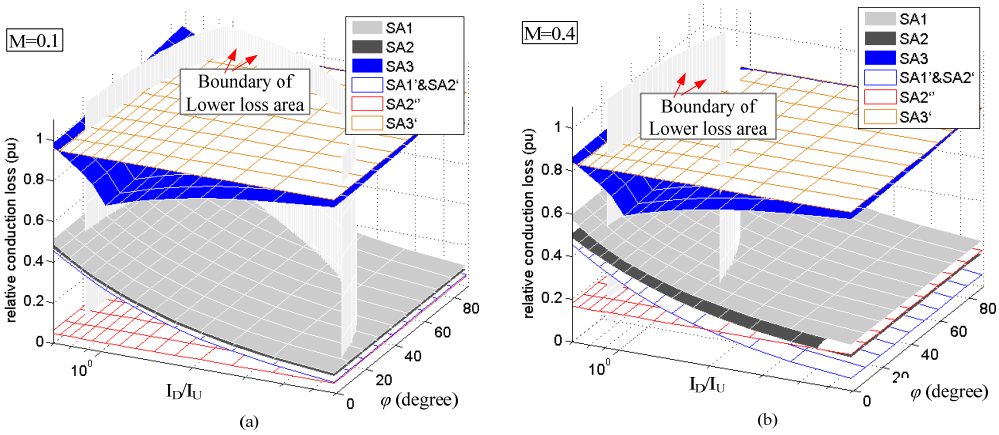


Figure 5.9: *Conduction loss distribution of the nine-switch converter when in ac-dc mode based on average switch current computation. (a) $M = 0.1$ (b) $M = 0.4$.*

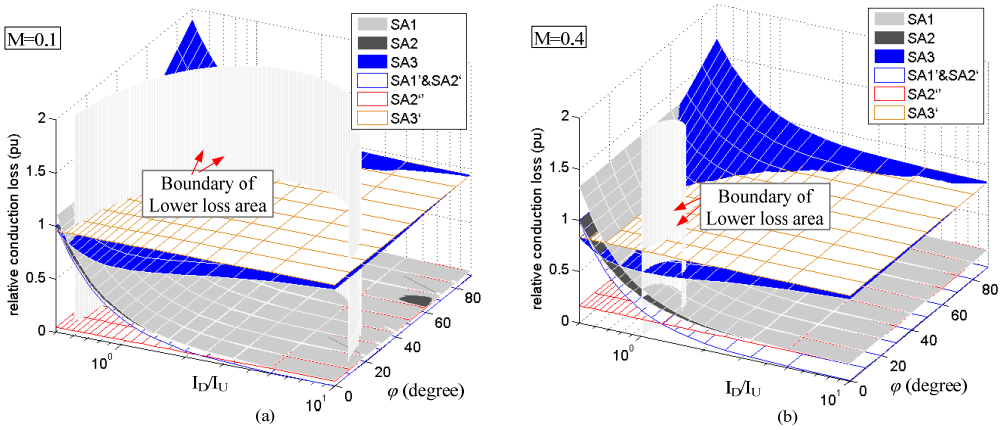


Figure 5.10: *Conduction loss distribution of the nine-switch converter when in ac-dc mode based on RMS switch current computation. (a) $M = 0.1$ (b) $M = 0.4$.*

the expressions for the nine-switch converter have both sets of terminal parameters included, while those for the BTB converter only have one set of terminal parameters included. To illustrate how they are compared, the operating criteria expected from a typical ac-dc energy conversion system are first defined [100].

Beginning with the dc terminal, its reference $Ref_D = -M_{oD}$ in (5.8) must be closer to

the negative triangular peak (in Fig. 5.2 and Fig. 5.3) for obtaining a high dc gain necessary for interfacing sources like photovoltaic and fuel cells. The offset M_{oD} must hence be large. Above Ref_D, the remaining carrier band is for Ref_U, whose maximum permitted amplitude and offset can thus be derived as (5.28), if an efficient utilization of the DC-link voltage is not to be compromised [100].

$$\begin{cases} M_{oU} = 0.5(1 - M_{oD}) \\ M_U = 1 - M_oU \end{cases} \tag{5.28}$$

Based on the definition of M, the parameters in (5.28) can also be expressed as:

$$\begin{cases} M_{oU} = \frac{M}{M+2} \\ M_oD = \frac{2-M}{M+2} \\ M_U = \frac{2}{M+2} \end{cases} \tag{5.29}$$

Substituting (5.29) into (7.3.3)-(7.26), the average and RMS loss distributions of the nine-switch and BTB converters can be plotted, as shown in Fig. 5.9 and Fig. 5.10. These plots are obtained by varying I_D, I_U and φ for two different M values ($M = 0.1$ and 0.4), and with I_D arbitrarily fixed. The respective LLAs for the two M values are also marked, within which, the nine-switch converter will have lower losses, and are hence in the preferred operating regions. Within the LLAs, $SA1$ and $SA2$ of the nine-switch converter are noted to have almost the same conduction losses, which are always lower than those of $SA3$. This is expected since $SA3$, being the inductive boosting switch, will be conducting the longest period, and hence dissipating the most power, before a high dc voltage gain can be obtained. Losses of $SA3$ can however be reduced closer to those of $SA1$ and $SA2$ by decreasing I_D, I_U and/or increasing M. They, in fact, reach a minimum when $\frac{I_D}{I_U} = 1$. Other than those, the phase angle of the ac load φ is found to have only a slight impact on the switch conduction losses, which hence renders it as not a prioritized parameter.

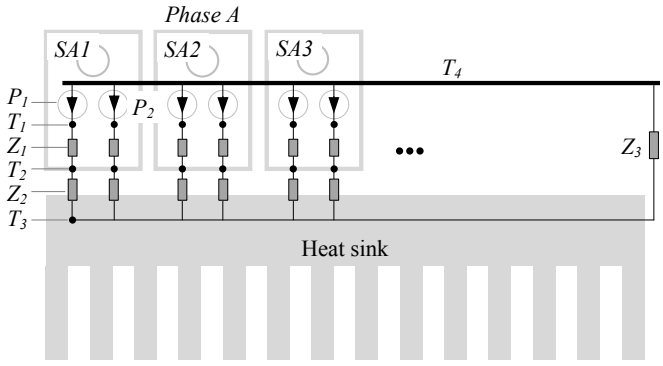
In conclusion, the observed loss distribution of the nine-switch converter within a LLA can be designed closer to that of the BTB converter, whose inductive boosting switch $SA3'$ is, in fact, generating more conduction losses than $SA3$ of the nine-switch converter. Conduction losses of $SA2''$ and $SA3'$ of the BTB converter are however dependent only on M, while those of $SA1'$ and $SA2'$ are dependent only on $\frac{I_D}{I_U}$. Their thermal management may therefore be simpler because of their respective dependencies on only single parameters.

5.4 Simulation results

The electric-thermal model [80,114] as shown in Fig. 5.11 for one phase of the nine-switch converter is simulated with PLECS for computing the power losses and temperatures at hotspots

Table 5.1: *SPECIFICATIONS OF NINE-SWITCH ONLINE-UPS (SIMULATION).*

Parameters	Values
Nominal Power	$1.5kVA$
DC-link	300 V
Upper Modulation Ratio M_U	0.8
Lower Modulation Ratio M_D	0.8 (resistive load)
Offset $M_{oU} = M_{oD}$	$0.05, 0.1, 0.15$
Upper phase angle	0
Lower phase angle	$0, 20^o, 30^o, 50^o$
Switching Frequency	$9kHz$
Power Switches	$IXGH30N120B3D1$



Note:
T1: junction temperature
T2: case temperature
T3: heatsink temperature
T4: ambient temperature
Z1: thermal impedance from junction to case
Z2: thermal impedance from case to heatsink
Z3: thermal impedance from heatsink to ambient
P1: power loss of the IGBT
P2: power loss of the Diode

Figure 5.11: *Electric-thermal model of one phase of nine-switch converter.*

using thermal impedances read from the technical literature for the IXGH30N120B3D1 power device [115, 116] and heatsink [117]. For the simulations, the ambient temperature is set at 40^oC, from which the eventual loss and temperature distributions of an online ac-ac nine-switch converter are computed based on those operating parameters listed in Table 5.1. Results ob-

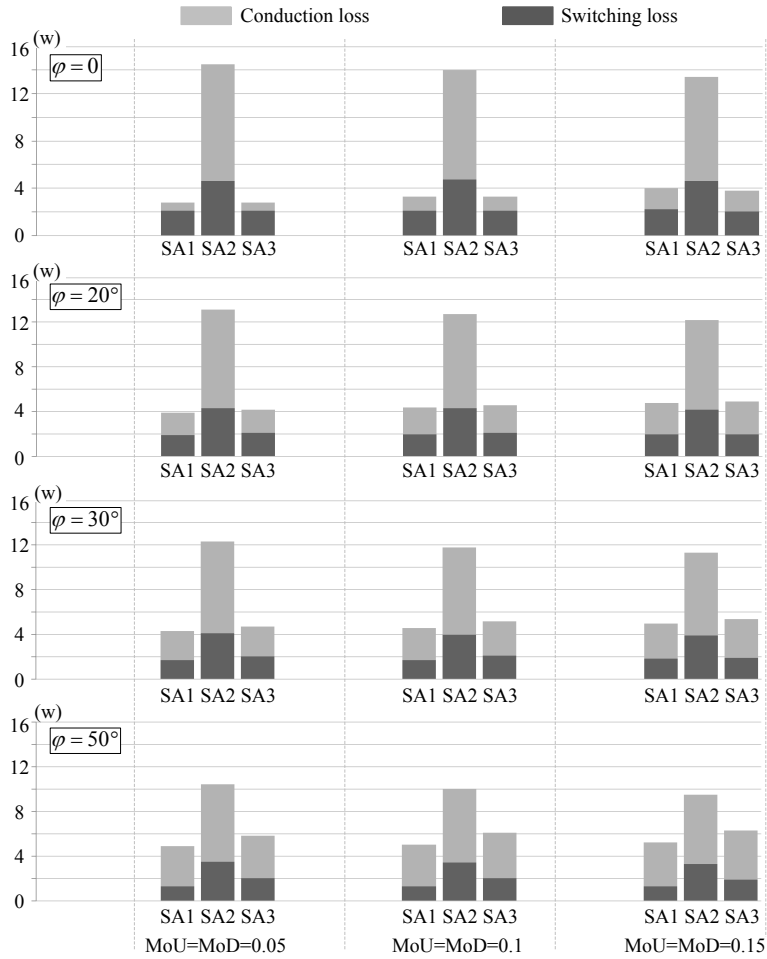


Figure 5.12: *Simulated loss distribution of nine-switch converter when operated as online ac-ac UPS.*

tained are shown in Fig. 5.12 and Fig. 5.13, which when compared with Fig. 5.7, are found to match the theoretical analysis well. To be more specific, the conduction losses, the mean temperature and temperature fluctuation of the middle SA2 are noted to fall, while those of the upper $SA1$ and lower $SA3$ are found to rise, when phase φ and M are increasing. The latter can be raised by increasing $M_{oU} \approx M_{oD}$, but not excessively if the DC-link utilization is not to be compromised. The thermal distribution of the nine-switch converter can therefore

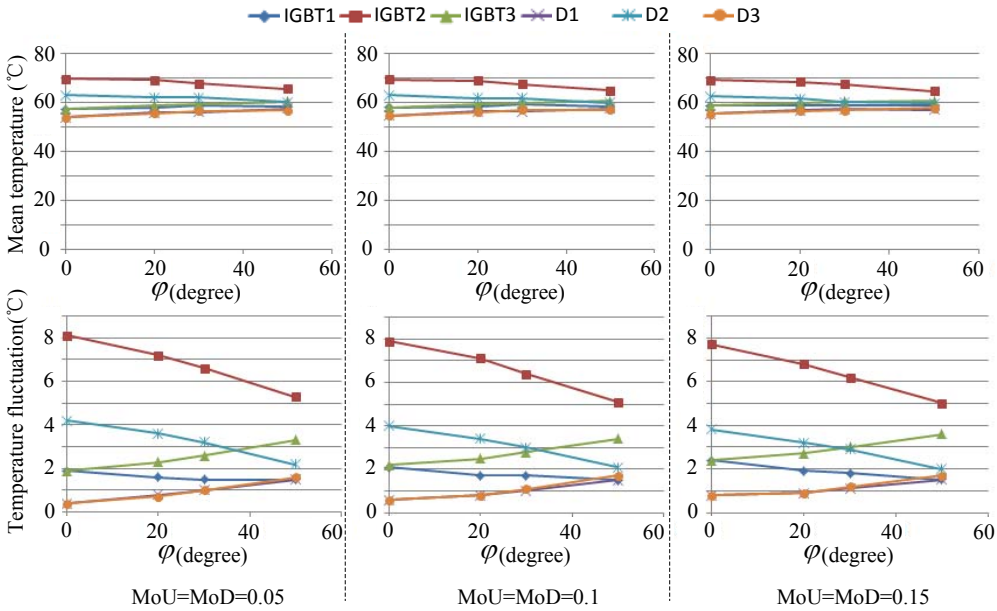


Figure 5.13: *Simulated thermal performance of nine-switch converter when operated as online ac-ac UPS.*

be improved if the scope of application is selected appropriately.

5.5 Experimental results

A nine-switch and a BTB converter have been built for verifying the theoretical analysis presented above. Illustrations of both converters are shown in Fig. 5.14, where it has been indicated that the same common dc bus snubber capacitors have been used for both converters. Besides those high frequency dc capacitors, no other snubbers have been added to the converters. The parameters chosen for the converters are listed in Table 5.2, whose values are extracted from LLAs identified from Fig. 5.4 and Fig. 5.5. These values, upon enforced, result in lower total power losses for the nine-switch converter. With these setups, the terminal voltages and currents of the nine-switch converter in its ac-ac and ac-dc modes are measured and shown in Fig. 5.15. Similar waveforms are also measured with the BTB converter, which because of their closeness, are not explicitly shown. Instead, the switch currents of the nine-switch converter are shown in Fig. 5.16, which are clearly combinations of both upper and lower terminal currents.

Table 5.2: *SPECIFICATIONS OF NINE-SWITCH SYSTEMS (EXPERIMENT).*

Parameters	**Values**	
	ac-ac mode	**ac-dc mode**
Nominal Power	$1.5kW$	
DC-link	$300V$	$300V$ Source
Upper Terminal Current I_U	$9A$ source	$-4A$ Load (resistive)
Lower Terminal Current I_D	$-9A$ Load (resistive)	$-4A$ Load (resistive)
Upper Modulation Ratio M_U	0.8	0.8
Lower Modulation Ratio M_D	0.8	0
Offset M_{oU}	0.15	0.15
Offset M_{oD}	0.15	0.85
M	1	0.18
Switching Frequency	$9kHz$	
Power Switches	IXGH30N120B3D1	

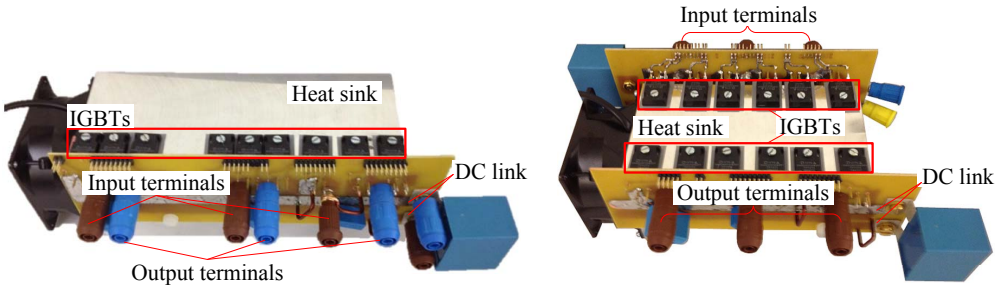


Figure 5.14: *Prototypes of (a) nine-switch and (b) BTB converters.*

Zoomed-in views of the switch currents measured with the nine-switch and BTB converters are also shown in Fig. 5.17 for illustrating a phenomenon associated with the ac-dc mode only. To be more specific, Fig. 5.17(a) shows instantaneous switch current $(i_U + i_D)$ through $SA3$ of the nine-switch converter being larger than i_D flowing through $SA3'$ of the BTB converter when in the ac-dc mode and driven by the same modulation pulses. This larger current of $SA3$ flows only for a short T_1 duration.

since Ref_U is near its positive peak. On the other hand, Fig. 5.17(b) shows $|i_U + i_D| < |i_D|$ for a longer T_1 duration when Ref_U is near its negative peak. The net effect is an average reduction of current through SA3, even though its instantaneous value has been increased and

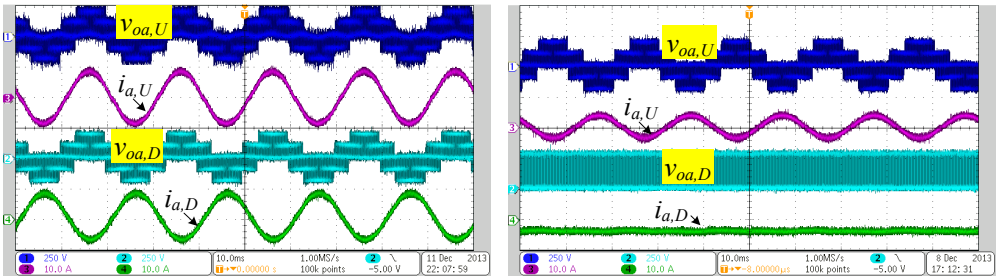


Figure 5.15: *Terminal voltages and currents of nine-switch converter when in (a) ac-ac and (b) ac-dc modes. ($v_{oa,U}$, $v_{oa,D}$: 250 V/div, $i_{a,U}$, $i_{a,D}$: 10 A/div, Timebase: 10 ms)*

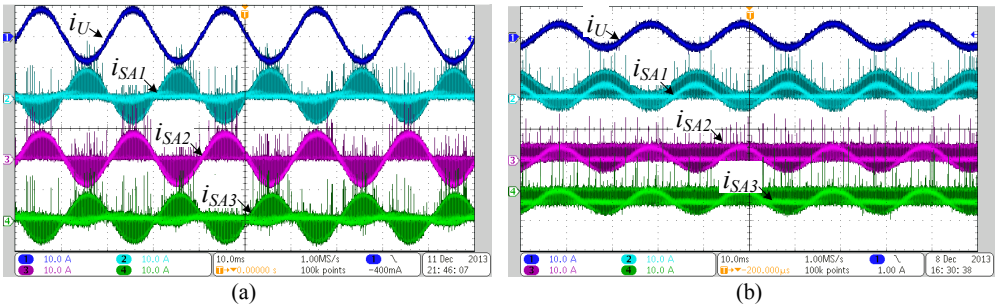


Figure 5.16: *Upper terminal current and individual switch currents of nine-switch converter when in (a) ac-ac and (b) ac-dc modes. (i_U, i_{SA1}, i_{SA2}, i_{SA3}: 10 A/div, Timebase: 10 ms)*

decreased by the same amount (but over different T_1 durations). This net reduction of current is however not experienced by $SA1$ of the nine-switch converter, because of the invariable T_3 interval fixed by Ref_D. It is also different from the ac-ac common-frequency mode, where the instantaneous switch currents through $SA1$ and $SA3$ are always either increased or decreased, but not a combination of both.

The collected switch voltage and current readings are eventually used for calculating the power losses of the nine-switch and BTB converters. The results obtained are plotted in Fig. 5.18, which as anticipated, demonstrate a significant reduction of conduction losses for the nine-switch converter. In its ac-ac mode, this reduction comes equally from the upper and lower switches of the converter, which changes to the lower switch only when in its ac-dc mode. Instead of reduction, the conduction losses of the upper switch increase slightly when in the

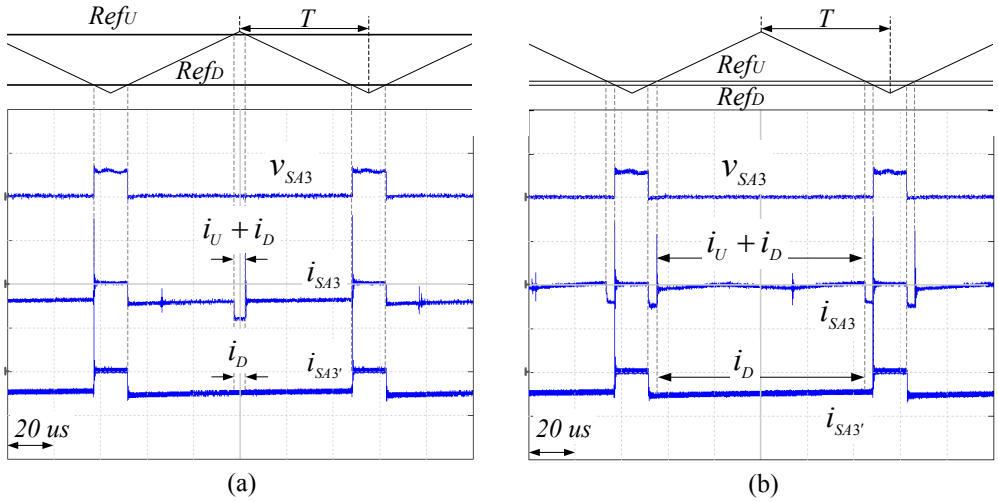


Figure 5.17: *Currents through $SA3$ of nine-switch converter and $SA3'$ of BTB converter during (a) positive and (b) negative half-cycles of Ref_U.*

ac-dc mode. Despite that, the total losses of the nine-switch converter are still reduced by 28% when in its ac-ac mode and 13% when in its ac-dc mode, as compared to the BTB converter. Thermal screenshots showing individual switch temperatures of the nine-switch converter are also shown in Fig. 5.19, which instead of the inaccessible junction temperatures, represent case temperatures of the individual devices. These temperature variations are again found to match well with the simulated and experimental bar-charts shown in Fig. 5.12 and Fig. 5.18, where the most heated switches are identified as $SA2$ when operating in the ac-ac mode, and $SA2$ and $SA3$ when operating in the ac-dc mode.

5.6 Summary

This chapter benchmarks the conduction losses of the nine-switch converter, which despite facing switching constraints, can have lower losses than BTB. Lower loss areas of the converter are mathematically adressed and plotted for both ac-ac and ac-dc modes, proving in particular that the nine-switch converter can be promisingly used as an online ac-ac UPS and an ac-dc hybrid energy conversion system. Loss distributions among devices for these applications can promptly be adjusted by changing modulation offsets and phases of the sources or loads, which within the LLAs, are found to be close to those of the BTB converter. As a consequence, the nine-switch converter can be a competitive reduced-switch alternative for applications, which

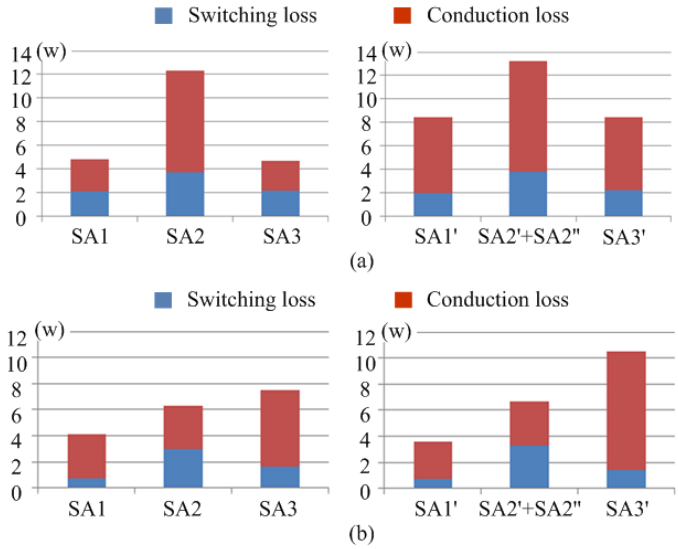


Figure 5.18: *Measured losses of nine-switch and BTB converters when in (a) ac-ac and (b) ac-dc modes. (nine-switch converter: $SA1$, $SA2$, $SA3$, twelve-switch converter: $SA1'$, $SA2'$, $SA2''$, $SA3'$)*

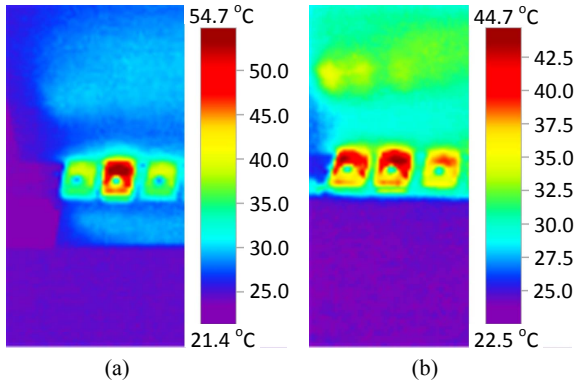


Figure 5.19: *Thermal images of nine-switch converter when in (a) ac-ac and (b) ac-dc modes (from left to right: $SA3$, $SA2$, $SA1$).*

operate within the LLAs identified and also tested in this chapter.

6 Rotating speed controller design for improved loading of three-phase BTB wind power converters

Wind power converters have variable loading due to the nature of the wind speed, and it will then induce temperature swings in wind power converters. In order to relieve the harmful temperature swings, several approaches have been proposed in literatures, in terms of using energy storage systems, heating the converter in light load by reative power and so on. Another possibility is to relieve the loading fluctuations by regulating the inertia energy stored in the rotor, which is relatively cost-effective. The inertia energy is regulated indirectly by controlling the rotating speed of the rotor, thus a rotating speed controller design method is proposed in this chapter, from improving the loading of the wind power converter point of view.

6.1 System modelling

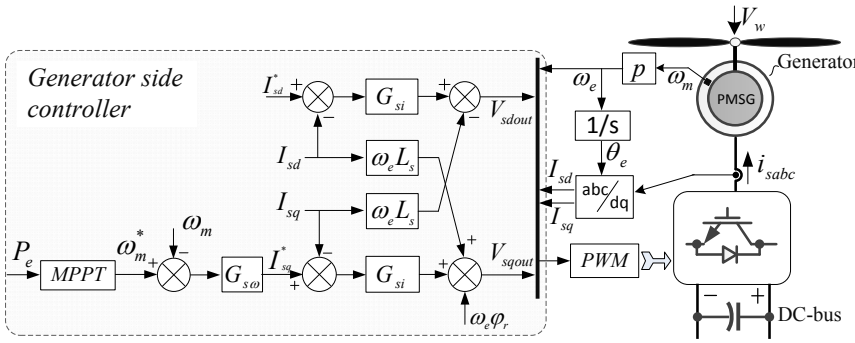


Figure 6.1: *A PMSG based direct-drive wind power generator and its drive drain.*

The overall system is modelled first, in terms of wind turbine model and generator model, as shown in Fig. 6.1. The generator side converter model is usually equivalent to a delay. The delay time is only 0.75 of the switching period [109], which is much shorter than the time constants of the wind turbine model and generator model, and thus it can be ignored. The grid side converter is not considered since the grid side converter is just tracking the power of the generator side converter. It should be noted that all the parameter values are listed in the Table given in 7.1.

6.1.1 Wind turbine model

The wind power absorbed by the turbine can be expressed as,

$$P_W = C_p \frac{\rho A}{2} V_W^3 \tag{6.1}$$

where ρ denotes the air density, $A = \pi R^2$ is the turbine swept area, R is the radius of the blade, V_W indicates the wind speed, C_p is the power coefficient of the blades, which is defined as,

$$\begin{cases} C_p(\lambda, \beta) = c_1(c_2/\lambda_i - c_3\beta - c_4)e^{-c_5/\lambda_i} + c_6\lambda \\ \frac{1}{\lambda_i} = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1} \\ \lambda = \frac{\omega_m R}{V_W} \end{cases} \tag{6.2}$$

where λ is the tip speed ratio, and β is the pitch angle, $c_1 \sim c_6$ are the coefficients, and ω_m is the rotating speed. The maximum power coefficient $C_{p,opt}$ is 0.48, which can be obtained when the optimal tip speed ratio $\lambda_{opt} = 8.1$ and zero pitch angle $\beta = 0$ are achieved. The wind power P_W can also be expressed as,

$$P_W = T_m \omega_m \tag{6.3}$$

where T_m is the aerodynamic torque on the turbine and it can be expressed as the following by substituting (6.1) into (6.3),

$$T_m = C_p \frac{\rho A V_W^3}{2\omega_m} \tag{6.4}$$

Equation (6.4) is actually the aerodynamic model of the wind turbine, which can be used to obtain the aerodynamic torque based on the wind speed, the rotating speed and the characteristics of the wind turbine.

6.1.2 Generator model

For the PMSG based wind power generator, the electrical, torque and mechanical equations are expressed in the following. In the rotating frame (dq), the q-axis is aligned with the rotor flux.

$$v_{sd} = R_s I_{sd} + L_s \frac{dI_{sd}}{dt} - \omega_e L_s I_{sq} \tag{6.5}$$

$$v_{sq} = R_s I_{sq} + L_s \frac{dI_{sq}}{dt} + \omega_e L_s I_{sd} + \omega_e \varphi_r \tag{6.6}$$

$$T_e = -\frac{3p}{2} \varphi_r I_{sq} \tag{6.7}$$

$$J \frac{d\omega_m}{dt} = T_m - T_e \tag{6.8}$$

where v_{sd} and v_{sq} are the stator voltages, i_{sd} and i_{sq} are the stator currents in the dq-frame, L_s and R_s are the stator inductance and resistance, respectively, φ_r is the rotor flux, T_e is the electromagnetic torque, p is the machine pole pairs, $\omega_e = p\omega_m$ is the electrical rotating speed, and J is the rotor inertia including the turbine and the generator. The friction is not the dominant factor and it is ignored here. The generator side controller is a conventional dq-frame control, and the compensation terms are based on the generator model, as seen in Fig. 6.1. The outer and inner loop are the rotating speed control and stator current control, respectively. The reference of the d-axis is zero in order to avoid affecting the magnetic field.

6.2 Design of the rotating speed controller

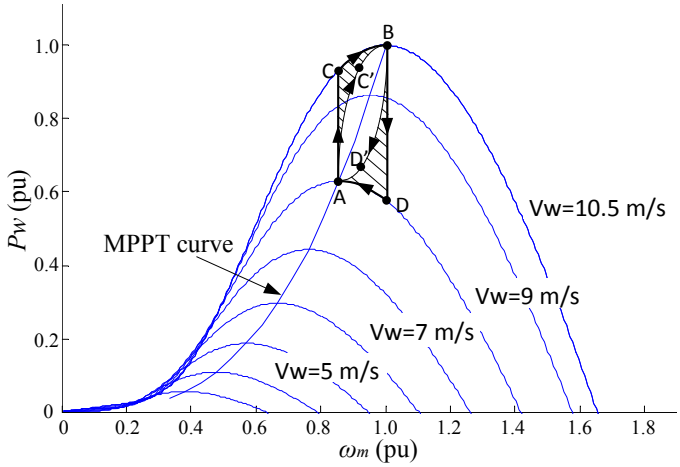


Figure 6.2: *The behaviour of the wind turbine in a wind speed step.*

As known, the kinetic energy E_m stored in the rotor can be expressed as,

$$E_m = \frac{1}{2} J \omega_m^2 \tag{6.9}$$

and the charging/discharging power of the turbine can be obtained as the following,

$$P_m = \frac{dE_m}{dt} = \frac{d}{dt}\left(\frac{1}{2} J \omega_m^2\right) = J \omega_m \frac{d\omega_m}{dt} \tag{6.10}$$

As seen in (6.10), the charging/discharging power of the turbine does not only relate to the rotating speed ω_m but also to the speed change rate $d\omega_m/dt$. Thus, $d\omega_m/dt$ can be regulated for the power levelling according to the basic relationship between the wind power P_W, the charging/discharging power of the turbine P_m and the electrical power delivered by the drive train P_e, as given in the following,

$$P_e = P_W - P_m \tag{6.11}$$

which is also indicated in Fig. 6.2. In steady state, the wind turbine operates on the MPPT curve to maximize the power generation. Assuming there is a wind speed step between 9 m/s and 10.5 m/s, the wind power P_W obtained by the turbine will follow the curve $\boldsymbol{ACB}$ in wind speed increasing and $\boldsymbol{BDA}$ in wind speed decreasing. The power changes fast and even an overshoot happens in step-down of the wind speed, which is not desired to happen in the electrical power P_e. In order to obtain a smoother electrical power, for example following the curves $\boldsymbol{AC'B}$ and $\boldsymbol{BD'A}$, the charging/discharging power P_m of the turbine is needed to compensate the difference indicated by the shadow. The P_m is indirectly regulated by the rotating speed controller, which therefore is designed in the following way.

The transfer function from the wind speed to the electrical power is first built for the design. Since the relationship between the wind speed and the electrical power is non-linear in the whole wind speed range, the small perturbation linearization is relatively more appropriate for the transfer function. The corresponding dimensionless transfer functions have been partially derived in [99] and they are expressed as the following,

$$G_{P/V}(s) = \frac{\Delta \tilde{P}_e(s)}{\Delta \tilde{V}_W(s)} = \frac{(3 - \lambda_0 C'_{p0}/C_{p0})(\omega_{m0}/P_{W0})slope}{\tau_0 s - \lambda_0 C'_{p0}/C_{p0} + (\omega_{m0}/P_{W0})slope} \tag{6.12}$$

$$G_{\omega/V}(s) = \frac{\Delta \tilde{\omega}_m(s)}{\Delta \tilde{V}_W(s)} = \frac{(3 - \lambda_0 C'_{p0}/C_{p0})}{\tau_0 s - \lambda_0 C'_{p0}/C_{p0} + (\omega_{m0}/P_{W0})slope} \tag{6.13}$$

where $\Delta \tilde{P}_e = \Delta P_e/P_{e0}$, $\Delta \tilde{V}_W = \Delta V_W/V_{W0}$, $\Delta \tilde{\omega}_m = \Delta \omega_m/\omega_{m0}$, $\lambda_0 = \omega_{m0} R/V_{W0}$, $C_{p0} =$

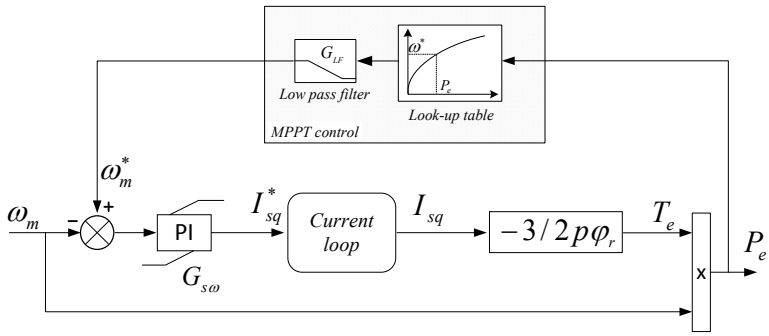


Figure 6.3: *The relationship between the rotating speed and electrical power with MPPT control.*

$C_p(\lambda_0)$, $C'_{p0} = dC_p(\lambda)/d\lambda|_{\lambda_0}$, $\tau_0 = J\omega_{m0}^2/P_{W0}$, X_0 ($X = P_e$, V_W, $\omega_m \cdots$) indicate the static values of the parameters and the power *slope* is defined as,

$$slope = \frac{\partial P_e}{\partial \omega_m} \tag{6.14}$$

According to the generator side controller (see Fig. 6.1), the torque equation (6.7) and the static equation $P_e = T_e\omega_m$, the relationship between ω_m and P_e can be indicated as shown in Fig. 6.3, where ω_m^* is the reference of the rotating speed and the low pass filter G_{LF} in the MPPT control is expressed as,

$$G_{LF} = \frac{1}{sT_{mppt} + 1} \tag{6.15}$$

According to Fig. 6.3, it is obtained as,

$$P_{e0} + \Delta P_e = (T_{e0} + \Delta T_e)(\omega_{m0} + \Delta\omega_m) \tag{6.16}$$

Removing the static and the second-order smaller terms, following can be obtained,

$$\Delta P_e = T_{e0}\Delta\omega_m + \Delta T_e\omega_{m0} \tag{6.17}$$

where ΔT_e can be obtained according to Fig. 6.3,

$$\Delta T_e = (\Delta\omega_m - \Delta\omega_m^*)G_{s\omega}\frac{3}{2}p\varphi_r \tag{6.18}$$

According to (6.1) and (6.2), the MPPT control can be expressed as,

$$\omega_m^* = \frac{\lambda_{opt}}{R}\left(\frac{2P_e}{\rho A C_{p,opt}}\right)^{1/3} G_{LF} \tag{6.19}$$

Then it can be derived,

$$\Delta\omega_m^* = \frac{\partial\omega_m^*}{\partial P_e}\Delta P_e = \frac{\lambda_{opt}}{3R} G_{LF}\left(\frac{2}{\rho A C_{p,opt}}\right)^{1/3} P_{e0}^{-2/3}\Delta P_e \tag{6.20}$$

Substituting the static expression of (6.19) into (6.20), following can be obtained,

$$\Delta\omega_m^* = \frac{\omega_{m0}}{3P_{e0}} G_{LF}\Delta P_e \tag{6.21}$$

Substituting (6.18) and (6.21) into (6.17), following is obtained,

$$slope = \frac{\Delta P_e}{\Delta\omega_m} = \frac{T_{e0} + \frac{3}{2}p\varphi_r\omega_{m0}G_{s\omega}}{1 + \frac{3}{2}p\varphi_r\omega_{m0}G_{s\omega}\cdot\frac{\omega_{m0}}{3P_{e0}}G_{LF}} \tag{6.22}$$

The rotating speed controller is a typical Proportional+Integral (PI) controller, which can be expressed as,

$$G_{s\omega} = K_{p\omega} + \frac{K_{i\omega}}{s} \tag{6.23}$$

Substituting (6.1), (6.22) and (6.23) into (6.12), and considering that $C'_{p0} = 0$ when C_{p0} achieves its maximum value, it is gained that,

$$G_{P/V}(s) = \frac{\frac{3}{J}(k_2\omega_{m0}+k_1K_{p\omega})s+\frac{3k_1K_{i\omega}}{J}}{s^2+\left(\frac{k_1}{3k_2\omega_{m0}}\frac{sK_{p\omega}+K_{i\omega}}{sT_{mppt}+1}+\frac{k_2\omega_{m0}}{J}+\frac{k_1K_{p\omega}}{J}\right)s+\frac{k_1K_{i\omega}}{J}} \tag{6.24}$$

where $k_1 = \frac{3}{2}p\varphi_r$, $k_2 = \frac{\rho A C_{p,opt}R^3}{2\lambda_{opt}^3}$. As seen of the dimensionless transfer function from wind speed to electrical power is actually a third-order and it can be simplified to a second-order, if following condition can be achieved,

$$K_{p\omega} = T_{mppt} * K_{i\omega} \tag{6.25}$$

Thus, (24) can be simplified to,

$$G_{P/V}(s) = \frac{\frac{3}{J}(k_2\omega_{m0} + k_1K_{i\omega}T_{mppt})s + \frac{3k_1K_{i\omega}}{J}}{s^2 + \left(\frac{k_1K_{i\omega}}{3k_2\omega_{m0}} + \frac{k_2\omega_{m0}}{J} + \frac{k_1K_{i\omega}T_{mppt}}{J}\right)s + \frac{k_1K_{i\omega}}{J}} \tag{6.26}$$

The transfer function becomes a second-order model with a lead compensation and it can also be expressed as,

$$G_{P/V}(s) = K_1 \frac{s + \omega_{f1}}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{6.27}$$

where K_1, ω_{f1}, ξ and ω_0 can be calculated as,

$$\begin{cases} K_1 = \frac{3}{J}(k_2\omega_{m0} + k_1 K_{i\omega} T_{mppt}) \\ \omega_{f1} = \frac{k_1 K_{i\omega}}{k_2\omega_{m0} + k_1 K_{i\omega} T_{mppt}} \\ \omega_0 = \sqrt{k_1 K_{i\omega}/J} \\ \zeta = \frac{\frac{k_1 K_{i\omega}}{3k_2\omega_{m0}} + \frac{k_2\omega_{m0}}{J} + \frac{k_1 K_{i\omega} T_{mppt}}{J}}{2\sqrt{k_1 K_{i\omega}/J}} \end{cases} \tag{6.28}$$

Another two important indicators are the mechanical stress and the variation of the rotating speed, which can be analyzed by $G_{T/V}(s)$ and $G_{\omega/V}(s)$, respectively. Substituting (6.1), (6.22), (6.23) and (6.25) into (6.13), and considering that $C'_{p0} = 0$ when C_{p0} achieves its maximum value, it is obtained that,

$$G_{\omega/V}(s) = \frac{\frac{3k_2\omega_{m0}}{J} s + \frac{k_1 K_{i\omega}}{J}}{s^2 + \left(\frac{k_1 K_{i\omega}}{3k_2\omega_{m0}} + \frac{k_2\omega_{m0}}{J} + \frac{k_1 K_{i\omega} T_{mppt}}{J}\right) s + \frac{k_1 K_{i\omega}}{J}} \tag{6.29}$$

which can also be shortened to,

$$G_{\omega/V}(s) = K_2 \frac{s + \omega_{f2}}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{6.30}$$

where K_2 and ω_{f2} are,

$$\begin{cases} K_2 = \frac{3k_2\omega_{m0}}{J} \\ \omega_{f2} = \frac{k_1 K_{i\omega}}{3k_2\omega_{m0}} \end{cases} \tag{6.31}$$

The dimensionless transfer function from the wind speed to the electromagnetic torque is defined as,

$$G_{T/V}(s) = \frac{\Delta\tilde{T}_e(s)}{\Delta\tilde{V}_W(s)} = \frac{\Delta T_e}{\Delta V_W} \cdot \frac{V_{W0}}{T_{e0}} \tag{6.32}$$

Substituting (6.17) into (6.32), it can be obtained that,

$$G_{T/V}(s) = \frac{\Delta P_e - T_{e0}\Delta\omega_m}{\omega_{m0} T_{e0}} \cdot \frac{V_{W0}}{\Delta V_W} = \frac{\Delta\tilde{P}_e(s)}{\Delta\tilde{V}_W(s)} - \frac{\Delta\tilde{\omega}_m(s)}{\Delta\tilde{V}_W(s)} \tag{6.33}$$

Substituting (6.26) and (6.29) into (6.33), it is acquired,

$$G_{T/V}(s) = \frac{\frac{3k_1K_{i\omega}T_{mppt}}{J}s + \frac{2k_1K_{i\omega}}{J}}{s^2 + \left(\frac{k_1K_{i\omega}}{3k_2\omega_{m0}} + \frac{k_2\omega_{m0}}{J} + \frac{k_1K_{i\omega}T_{mppt}}{J}\right)s + \frac{k_1K_{i\omega}}{J}} \tag{6.34}$$

Similarly, $G_{T/V}(s)$ can be expressed as,

$$G_{T/V}(s) = K_3\frac{s+\omega_{f3}}{s^2+2\zeta\omega_0 s+\omega_0^2} \tag{6.35}$$

where K_3 and ω_{f3} can be calculated as,

$$\begin{cases} K_3 = \frac{3k_1K_{i\omega}T_{mppt}}{J} \\ \omega_{f3} = \frac{2}{3T_{mppt}} \end{cases} \tag{6.36}$$

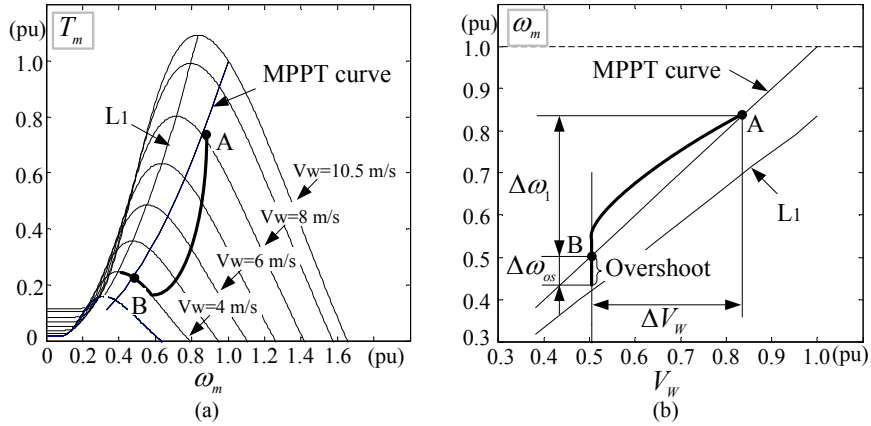


Figure 6.4: *Illustration for the stable region of the wind turbine (a) mechanical torque T_m vs. rotating speed ω_m (b) rotating speed ω_m vs. wind speed V_W.*

According to (6.27), (6.30) and (6.35), $G_{P/V}(s)$, $G_{T/V}(s)$ and $G_{\omega/V}(s)$ have the same characteristic equation, which means the same bandwidth and damping. However, the lead compensation links involved in the transfer functions are different and thereby they will lead to different frequency characteristics. In order to make the electrical power smoother, the bandwidth of $G_{P/V}(s)$ should be reduced as much as possible, where the precondition is that the wind turbine should always be kept at a stable region. Fig. 6.4(a) shows the mechanical torque as a function of the rotating speed. The curve L_1 is composed of the maximum torque

points at each wind speed. The right side of L_1 is called the stable region, because $\frac{dT_m}{d\omega_m} < 0$ so the motion of the wind turbine will be damped (see Eqn. (6.8)). The left side of L_1 is called the unstable region, since $\frac{dT_m}{d\omega_m} > 0$ so the motion of the wind turbine will be enhanced (see Eqn. (6.8)). If the wind turbine is in the unstable region and $\frac{d\omega_m}{dt} > 0$, the wind turbine will speed up and get to the stable region. But if $\frac{d\omega_m}{dt} < 0$ when the wind turbine is in the unstable region, the wind turbine will speed down until it stops, which is not expected unless it is below the cut-in wind speed. With the MPPT control, the static operation points of the wind turbine are all in the stable region. However, if the rotating speed has an overshoot as a response to the decrease of the wind speed, the wind turbine has the possibility to get to the unstable region with $\frac{d\omega_m}{dt} < 0$. As shown in Fig. 6.4(a), with a wind speed reduction ΔV_W, the wind turbine will go from A to B. The motion of the rotating speed is composed of $\Delta\omega_1$ and $\Delta\omega_{os}$, as illustrated in Fig. 6.4(b). The overshoot $\Delta\omega_{os}$ can be positive, but it should be lower than the gap between the MPPT curve and L_1 in order to avoid the undesired stop of the wind turbine. According to (6.13) and Fig. 6.4(b), following can be obtained,

$$|G_{\omega/V}(j\omega)| = \frac{\Delta\omega/\omega_{m0}}{\Delta V_W/V_{W0}} = \frac{(\Delta\omega_1 + \Delta\omega_{os})/\omega_{m0}}{\Delta V_W/V_{W0}} \tag{6.37}$$

Since $\Delta\omega_{os} \ll \Delta\omega_1$ is valid in the case of a large wind speed reduction happens, the constraint for the stability of the wind turbine therefore can be obtained as, (in steady state of MPPT, the ratio between the wind speed and the rotating speed is fixed)

$$Max(|G_{\omega/V}(j\omega)|_{\omega=0\to\infty}) \leq \frac{\Delta\omega_1/\omega_{m0}}{\Delta V_W/V_{W0}} = 1 \tag{6.38}$$

According to (6.29), it is easy to obtain $|G_{\omega/V}(j\omega)|_{\omega=0} = 1$. Therefore, it can be concluded from (6.38) that no resonances are acceptable in $|G_{\omega/V}(j\omega)|$ for the stability of the wind turbine. Meanwhile, the resonance of $G_{P/V}(j\omega)$ and $G_{T/V}(j\omega)$ can also be studied by their maximum magnitudes, which are defined as,

$$M_P = \frac{Max(\left|G_{P/V}(j\omega)\right|_{\omega=0\to\infty})}{\left|G_{P/V}(j\omega)\right|_{\omega=0}} \tag{6.39}$$

$$M_\omega = \frac{Max(\left|G_{\omega/V}(j\omega)\right|_{\omega=0\to\infty})}{\left|G_{\omega/V}(j\omega)\right|_{\omega=0}} \tag{6.40}$$

$$M_T = \frac{Max(\left|G_{T/V}(j\omega)\right|_{\omega=0\to\infty})}{\left|G_{T/V}(j\omega)\right|_{\omega=0}} \tag{6.41}$$

where M_P, M_ω and M_T are relative magnitudes. Then the constraint for the stability of the wind turbine can be expressed as,

$$M_\omega \leq 1 \tag{6.42}$$

Substituting (6.27), (6.30) and (6.35), M_P, M_ω and M_T can be calculated as,

$$M_P = Max\left(\frac{\sqrt{\omega^2+\omega_{f1}^2}}{\sqrt{(\omega_0^2-\omega^2)^2+4\zeta^2\omega_0^2\omega^2}}\right)_{\omega=0\to\infty}\cdot\frac{\omega_0^2}{\omega_{f1}} \tag{6.43}$$

$$M_\omega = Max\left(\frac{\sqrt{\omega^2+\omega_{f2}^2}}{\sqrt{(\omega_0^2-\omega^2)^2+4\zeta^2\omega_0^2\omega^2}}\right)_{\omega=0\to\infty}\cdot\frac{\omega_0^2}{\omega_{f2}} \tag{6.44}$$

$$M_T = Max\left(\frac{\sqrt{\omega^2+\omega_{f3}^2}}{\sqrt{(\omega_0^2-\omega^2)^2+4\zeta^2\omega_0^2\omega^2}}\right)_{\omega=0\to\infty}\cdot\frac{\omega_0^2}{\omega_{f3}} \tag{6.45}$$

The maximum magnitudes as a function of $K_{i\omega}$ are illustrated in Fig. 6.5. When $K_{i\omega}$ is reduced, the bandwidth decreases, while the maximum magnitudes of $G_{P/V}(j\omega)$, $G_{T/V}(j\omega)$ and $G_{\omega/V}(j\omega)$ have different behaviours. Basically, those of $G_{P/V}(j\omega)$ and $G_{\omega/V}(j\omega)$ will increase, and that of $G_{T/V}(j\omega)$ will decrease. Therefore, it is concluded that, as smoother electrical power is desired, the narrower bandwidth is required but at the same time more significant rotating speed variation will be introduced. Further, the electromagnetic torque or mechanical stress may not be increased or significantly increased with the optimal design, as seen in Fig. 6.5. Based on Fig. 6.5, three designs are made for comparison, in terms of under-design, optimal design and over-design, which are listed in Table 6.1. The coeffients $K_{i\omega}$ can be directly read from Fig. 6.5, and the coeffients $K_{p\omega}$ can be calculated according to (6.25).

Table 6.1: *A Set of Designs for the Rotating Speed Controller.*

	over-design	optimal design	under-design
$K_{p\omega}$	1150	5500	17500
$K_{i\omega}$	230	1100	3500

In the optimal design, the minimum bandwidth is obtained and the constraint (Eqn. (6.42)) is still fulfilled. The plots in Fig. 6.5 are therefore divided into two parts by the optimal design, where the left and right sides are unstable and stable regions, respectively. Moreover, in the optimal design the resonance exists in $G_{T/V}(j\omega)$, but the amplitude is only 1.02 pu. The

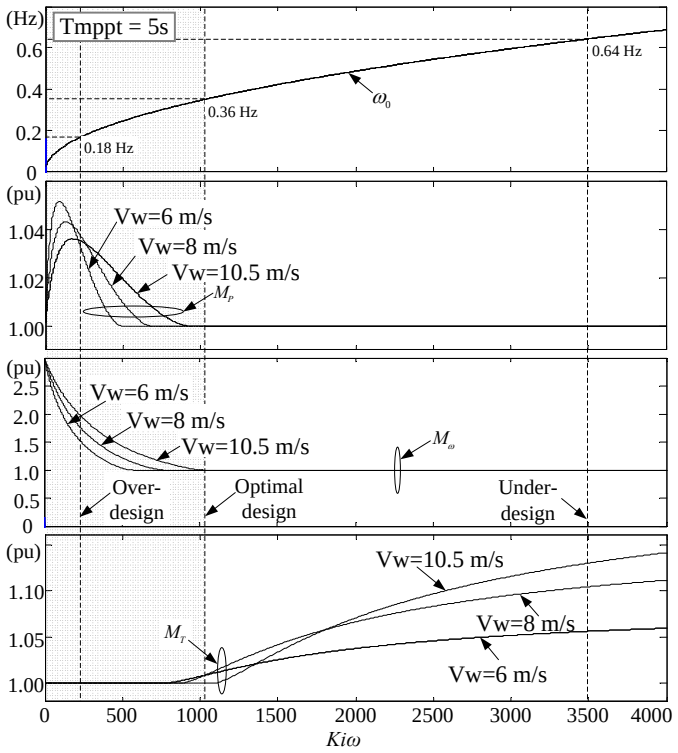


Figure 6.5: *The cut-off frequency and maximum magnitude of the transfer functions vs.* K_{iw}.

corresponding frequency characteristics are then analysed by ***Bode Plots***, as shown in Fig. 6.6. In under-design and optimal design, there is no resonance in $G_{\omega/V}(s)$, but the bandwidth of $G_{P/V}(s)$ in the under-design is higher than optimal design. In the over-design, the bandwidth of $G_{P/V}(s)$ is narrower than optimal design, but the resonance of $G_{\omega/V}(s)$ is however large. Moreover, in the under-design a small resonance of $G_{T/V}(s)$ is observed. All of these match Fig. 6.5 very well. The sensitivity of the transfer functions with wind speeds is also studied, as indicated in Fig. 6.7. As seen, the wind speed has a relatively more significant impact on $G_{\omega/V}(s)$, but it is still very small. Thus, the dimensionless transfer functions have good insistence in the whole operational region. The proposed design list of the rotating speed controller is further indicated in Table 6.2.

It should be noted that the power fluctuations of the wind turbine mostly occur when the wind speed varies below the nominal wind speed, where both the current and the power are

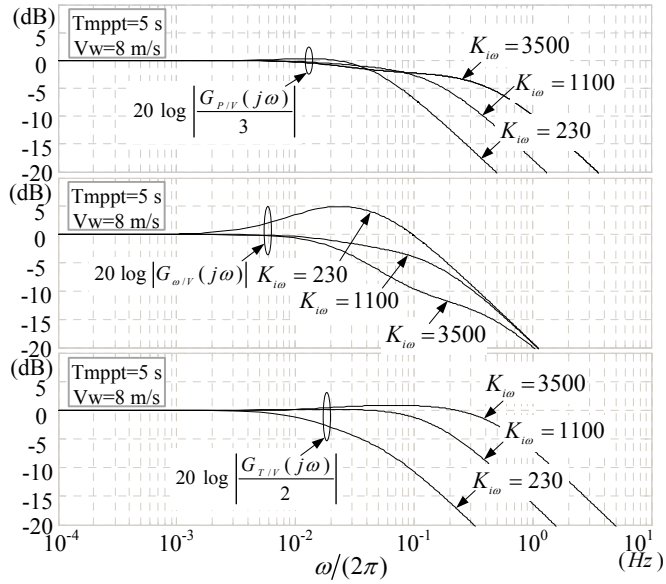


Figure 6.6: *Impact of $K_{i\omega}$ on magnitude of $G_{P/V}(s)$ in (6.27), $G_{T/V}(s)$ in (6.35) and $G_{\omega/V}(s)$ in (6.30).*

below their nominal values. When the wind speed is beyond the nominal value, the pitch control will be triggered to maintain a constant nominal power, and in this case the current of the wind power converter is limited to its nominal value. Therefore, with the proposed optimal design, the current will not go beyond the power converter rating.

6.3 Impact of the other parameters on power levelling

In order to get a better understanding of using the inertia energy for power levelling, the impact of the other parameters are also studied. From a control point of view, the time constant of the MPPT control T_{mppt}, which is the longest one in the control system, could be one of the critical parameters. Another important parameter is the rotor inertia J since it dominates the capacity of the inertia energy. A case study is done, where T_{mppt} or J have different values for each case. The optimal design is obtained for each case following the method proposed above. The ***Bode Plots*** of the transfer functions with the optimal design are then used to analyze the impact of T_{mppt} and J.

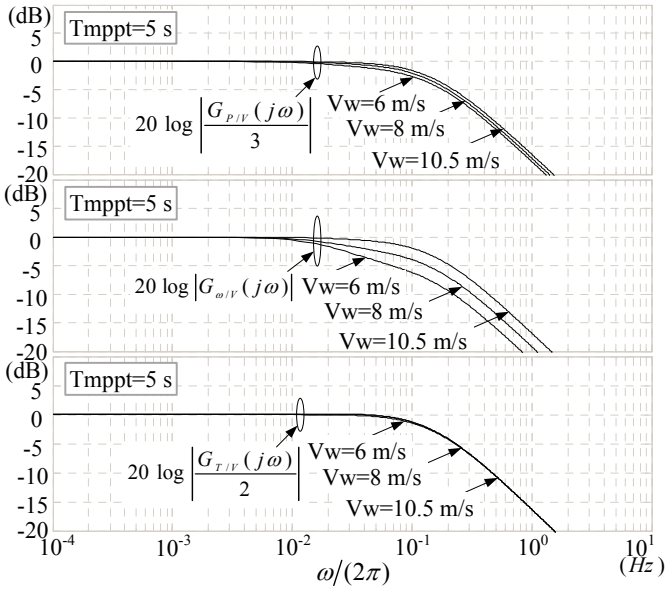


Figure 6.7: *Impact of V_W on magnitude of $G_{P/V}(s)$, $G_{T/V}(s)$ and $G_{\omega/V}(s)$.*

Table 6.2: *The design list of the rotating speed controller.*

Step 1	The dimensionless transfer functions $G_{P/V}(s)$, $G_{\omega/V}(s)$ and $G_{T/V}(s)$ are derived (see (6.26), (6.29) and (6.34)).
Step 2	Assuming $K_{p\omega} = T_{mppt} * K_{i\omega}$, the transfer functions $G_{P/V}(s)$, $G_{\omega/V}(s)$ and $G_{T/V}(s)$ becomes second-order, whose bandwidths are all proportional to $K_{i\omega}$.
Step 3	The stability condition is derived as the following $Max\|G_{\omega/V}(j\omega)\| \leq \|G_{\omega/V}(j\omega)\|_{\omega=0}$ by which the minimum value of $K_{i\omega}$ is obtained. Afterwards, $K_{p\omega}$ is calculated as $K_{p\omega} = T_{mppt} * K_{i\omega}$.
Step 4	The response of the wind power to the wind speed variation is then checked at various wind speeds in the frequency domain. Moreover, the response of the torque to the wind speed variation can also be evaluated by using $G_{T/V}(s)$.

6.3.1 Impact of the time constant T_{mppt}

The time constant T_{mppt} is set to be 5 s, 1 s and 0.1 s, respectively. The corresponding ***Bode Plots*** of the transfer functions with the optimal design are shown in Fig. 6.8. When

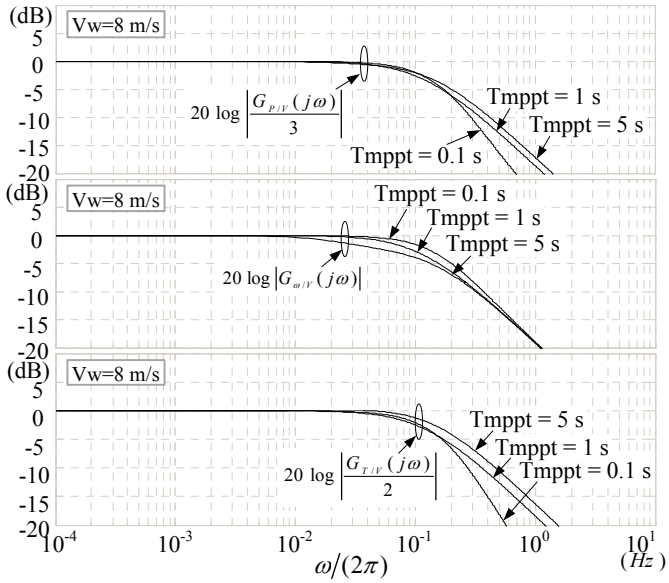


Figure 6.8: *Impact of time constant T_{mppt} on magnitude of $G_{P/V}(s)$, $G_{T/V}(s)$ and $G_{\omega/V}(s)$.*

T_{mppt} is reduced, the bandwidth of $G_{P/V}(s)$, $G_{T/V}(s)$ and $G_{\omega/V(s)}$ will decrease. However, the reduction of T_{mppt} from 5 s to 0.1 s only influences the performance of power levelling slightly. Therefore, T_{mppt} is not a critical parameter from power levelling point of view.

6.3.2 Impact of the inertia moment J

The moment of inertia J is set to be 2 pu, 1 pu and 0.5 pu, respectively, where the value of 1 pu can be found in Appendix A. The corresponding ***Bode Plots*** of the transfer functions with the optimal design are shown in Fig. 6.9. When J is doubled, the bandwidth of $G_{P/V}(s)$, $G_{T/V}(s)$ and $G_{\omega/V(s)}$ will be half of the previous value. As a consequence, the moment of inertia J is very important for the power levelling and larger inertia can lead to a smoother power, also as expected.

6.4 Simulation results

A wind power system model is built in Simulink/PLECS, where the modelling in Section 6.1 and the parameters in Appendix A are used. As seen in Fig. 6.10 and Fig. 6.11, simulation

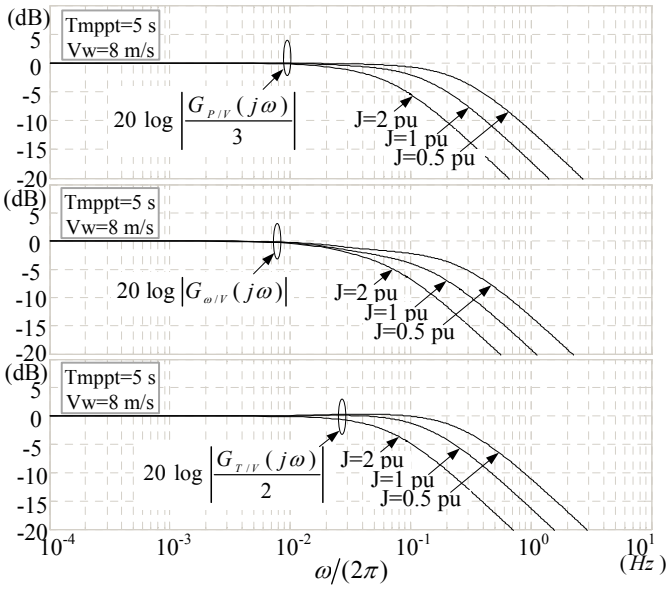


Figure 6.9: *Impact of inertia J on magnitude of $G_{P/V}(s)$, $G_{T/V}(s)$ and $G_{\omega/V}(s)$.*

of the wind turbine is first done with 5 s and 40 s wind turbulences, respectively, to verify the frequency characteristics of the proposed method. With the 5 s (0.2 Hz) wind turbulence, the over-design shows the best performance for power levelling as well as for the torque levelling, where the optimal design is followed. But with the 40 s (0.025 Hz) wind turbulence, the wind turbine with over-design approaches the unstable region gradually until it stops. This is because at 0.2 Hz the amplitude of $G_{\omega/V(s)}$ is below 1 pu, so the stability condition (6.42) is fulfilled, while at 0.025 Hz it is around 2 pu, which is beyond the constraint for stability and makes the system unstable (see Fig. 6.6).

A roughness class 4 wind profile [110] is then employed to study the behaviour of the wind turbine, as shown in Fig. 6.12. The optimal design leads to a smoother power and torque than the under-design, and its rotating speed has a more significant variation. The power coefficient C_P is also influenced by the various designs, where the under-design has the highest C_P and the optimal design just follows it. Nevertheless, C_P is above 0.95 pu with the optimal design. The over-design again has the smoothest power and torque, despite, the lowest C_P and stability issue of over-design make it unacceptable.

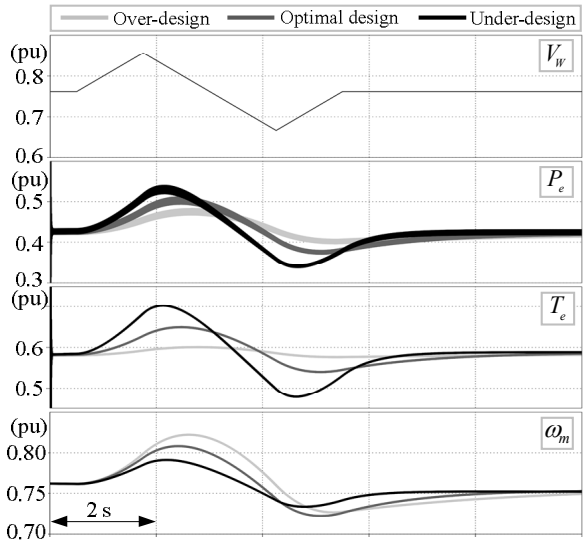


Figure 6.10: *Behaviour of the wind turbine with various design in a 5 s wind turbulence.*

6.5 Summary

The transfer functions from the wind speed to electrical power, electromagnetic torque and rotating speed are built, based on which the rotating speed controller is designed for power levelling in the frequency domain. Moreover, the impact of other parameters on the power levelling, including the time constants of MPPT and the rotor inertia, are also studied. With the proposed optimal design, the power is smoothened significantly as well as the torque, and the performance of MPPT is only weakened slightly. On the other hand, the rotating speed varies more intensely, but the wind turbine is still in the stable region since the constraint of rotating speed for stability is followed. It is also found that the rotor inertia instead of the time constant of MPPT is a critical parameter for the power levelling.

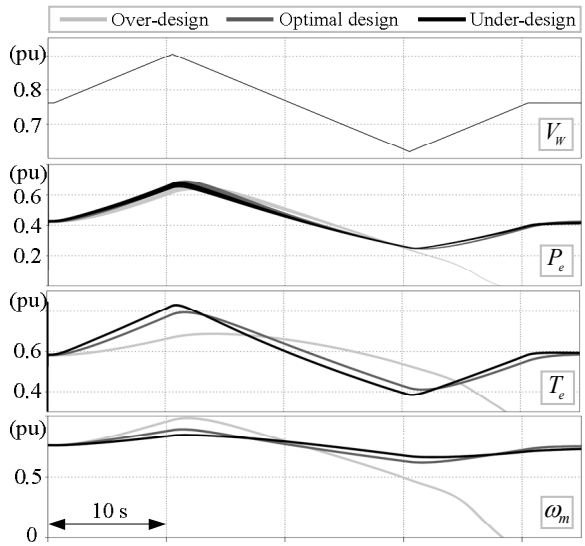


Figure 6.11: *Behaviour of the wind turbine with various design in a 40 s wind turbulence.*

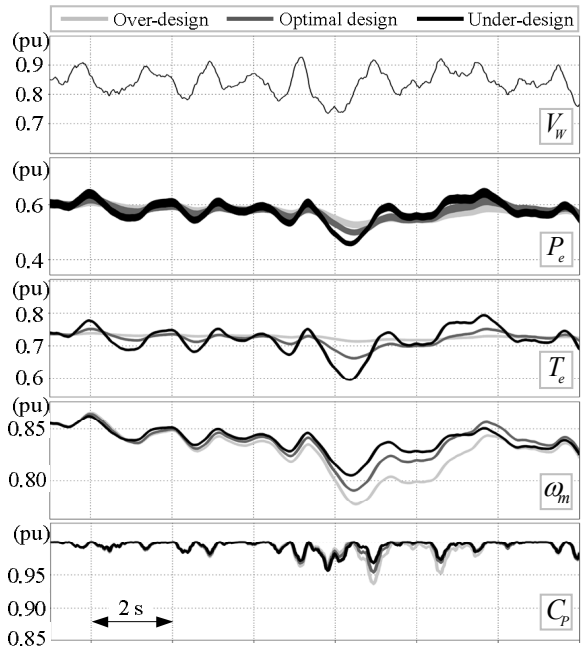


Figure 6.12: *Behaviour of the wind turbine with various design in a roughness class 4 wind profile.*

Part IV

Summary

7 Conclusions and future work

According to the obtained results presented in the previous chapters, this chapter first concludes the work and contributions of the thesis, before several research perspectives are proposed for future investigation.

7.1 Conclusions

In the thesis, several advanced design methods have been proposed for robust single- and three-phase ac-dc-ac converters. These methods include using advanced control strategies, auxiliary circuits, and application criteria, as mentioned in the introduction. The details are given as follows,

7.1.1 Advanced control strategies for robust design

With the proposed new modulation methods in Chapter 2 and Chapter 3, the single-phase B6 and H6 converter, even with less switches than two full-bridges connected back-to-back, can achieve good performance in applications like online UPS, power conditioners, and active power decoupling, where the input and ouput have the same frequency. By applying the proposed modulation schemes, both the input and ouput can realize a unity modulation index as long as the phase displacement is smaller than 60^o. Besides, the current ripple can be reduced and the loss distribution can be improved.

The inertia energy stored in the rotor can be used for power leveling if the new rotating

speed controller design method proposed in Chapter 6 is followed. At the same time, the torque is also smoothed significantly, and the performance of MPPT is only weakened slightly. On the other hand, the rotating speed varies more intensely, but the wind turbine is still in the stable region since the constraint of rotating speed for stability is followed. It is also found that the rotor inertia instead of the time constant of MPPT is a critical parameter for the power levelling.

7.1.2 Auxiliary circuits for robust design

The dc-link electrolytic capacitors in single-phase systems can be replaced by film capacitors together with power devices. The approach is named as active power decoupling. Among the various active power decoupling methods, the boost-type auxiliary circuit using dc film capacitors could be the most optimal solution for achieving high power density and high efficiency in kW-scale converters, when considering the specifications of the power devices and commercially available film capacitors, as concluded in Chapter 4. Moreover, the dc offset of the decoupling capacitor voltage can be adaptively controlled to further reduce the loss in light load condition. By theoretical analysis and experimental verification, it is concluded that with the optimized dc decoupling, a $56.7cm^3$ film capacitor is enough for compensating power oscillation in a 2 kW single-phase converter. The ac decoupling method is also optimized in Chapter 4, but the size of the decoupling capacitor is about two times larger than dc decoupling and the overall efficiency of the circuit is significantly lower than dc decoupling.

7.1.3 Application criteria for robust design

The nine-switch converter, despite facing switching constraints, can have lower losses than its BTB precedence, when used as an online ac-ac UPS and an ac-dc hybrid energy conversion system, as concluded in Chapter 5. Loss distributions among devices for these applications can promptly be adjusted by changing modulation offsets and phases of the sources or loads, which within the lower loss areas, are found to be close to those of the BTB converter. As a consequence, the nine-switch converter can be a competitive reduced-switch alternative for applications, when operating within the LLAs identified and tested in Chapter 5.

7.2 Main contributions from the author's point of view

According to the conclusions drawn, contributions of the thesis can be spelled as follows:

7.2.1 Modulation schemes for single-phase B6 and H6 converters with improved performance

New modulation schemes are proposed in Chapter 2 and Chapter 3 for single-phase B6 and H6 converters, respectively. The schemes are carrier-based and hence easy to be impelmented, which if applied, can help the converters to maximize their dc-link voltage utilization. Besides, the ac side current ripple can be reduced and the uneven loss distribution can be improved by the corresponding modulation schemes.

7.2.2 Optimized active power decoupling approach for kW-scale single-phase converters to achieve high power density and efficiency

Power decoupling methods are investigated in Chapter 4 to find the best solution in terms of high power density and efficiency in kW-scale single-phase dc-ac or ac-dc converters. The control method of the auxiliary circuit is improved to enhance its efficiency at light load. With the benckmark active power decoupling approach, the volume and power losses of the auxiliary circuit are minimized.

7.2.3 Application criteria of nine-switch converters for improved performance in terms of losses and temperature

Application criteria are found for the nine-switch converters discussed in Chapter 5, which if followed, can make the converter have lower loss than the three-phase BTB converter. Besides, loss distribution among devices for these applications can promptly be adjusted by changing modulation offsets and phases of the sources or loads. All of these make the nine-switch converter a competitive reduced-switch alternative for several specific applications.

7.2.4 Rotating speed controller design for power levelling of wind power converters

A design approach for rotating speed controller in the frequency domain is proposed for power levelling of the wind power converters in Chapter 6. The approach is easy to understand and implement, and the power filtering effect (power levelling) is very clear. Moreover, with the proposed approach, the torque becomes more stable, the MPPT performance is only slightly weaken, and the rotating speed varies more significantly but still in the stable region.

7.3 Proposals for future research topics

7.3.1 Performance investigation under fault conditions

In this thesis, performances of the converters are studied under normal conditions. The converters may perform differently under fault conditions, e.g. balance or unbalance grid voltage sag and short- or open-circuit fault of the power devices, where different approaches may be required for performance improvement. It is therefore an interesting scope for future research.

7.3.2 Performance improvement in different frequency mode

In single-phase converters, only the common frequency mode is studied in this thesis, because the single-phase B6 and H6 converter are both more promising in this mode. However, the different frequency mode is also a critical requirement in applications like motor drives. Robust circuit topologies for different freqency mode and their corresponding control approaches are therefore possible scope for future research.

7.3.3 Advanced design methods for the power filters

This thesis has studied the performance of only the power switches and dc-link. In practice, power filters can also play an important role affecting the overall performance of the power converter. Due to the fast development of power semiconductor, challenges hindering further improvement of performance of the power converter, e.g. higher power density and higher efficiency, are gradually moved from the active devices to passive components including the power filters. Therefore, filter design can also be included for future investigation.

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Appendix A

Table 7.1: *Parameters of the Wind Power System.*

Parameter	Symbol	Value
Nominal power	$\boldsymbol{P_n}$	3 MW
Nominal wind speed	$\boldsymbol{V_{Wn}}$	10.5 m/s
Nominal rotating speed	$\boldsymbol{\omega_{mn}}$	15.3 rpm
Nominal torque	$\boldsymbol{T_{mn}}$	1.86 $MN \cdot m$
Inertia of moment	$\boldsymbol{J}$	3.81 $Mkg \cdot m^2$
Radius of the blade	$\boldsymbol{R}$	53 m
Coefficients	$\boldsymbol{c_1 \sim c_6}$	0.5176, 116, 0.4 5 ,21, 0.0068
Air density	$\boldsymbol{\rho}$	1.225 kg/m^3
Flux induced by magnet	$\boldsymbol{\varphi}$	2.5 Wb
Inductance of the stator	$\boldsymbol{L_s}$	0.835 mH
Resistance of the stator	$\boldsymbol{R_s}$	6 $m\Omega$
Number of pole pairs	$\boldsymbol{p}$	120
Time constant of MPPT	$\boldsymbol{T_{mppt}}$	5 s
Current controller	$\boldsymbol{G_{si}}$	$0.9 + \frac{809}{s}$

Loss distribution of nine-switch converters and twelve-switch back-to-back converters

a. AC-AC Common Frequency Mode

Nine-Switch Converter

$$|i_{SA1}|_{Av} = \frac{1}{\pi}(M_{oU} + M_{oD}) \times I_U + \frac{1}{\pi}(1 - M_{oD})\sqrt{I_U^2 + I_D^2 - 2I_U I_D cos\varphi} \tag{7.1}$$

$$|i_{SA2}|_{Av} = \frac{1}{\pi}(1 - M_{oU}) \times I_U + \frac{1}{\pi}(1 - M_{oD}) \times I_D \tag{7.2}$$

$$|i_{SA3}|_{Av} = \frac{1}{\pi}(M_{oU} + M_{oD}) \times I_D + \frac{1}{\pi}(1 - M_{oU})\sqrt{I_U^2 + I_D^2 - 2I_U I_D cos\varphi} \tag{7.3}$$

$$i_{SA1}{}^2_{RMS} = \frac{1}{4}(1 + M_{oU})I_U^2 + \frac{1}{4}(1 - M_{oD})I_D^2 - \frac{1}{2}(1 - M_{oD})I_U I_D cos\varphi \tag{7.4}$$

$$i_{SA2}{}^2_{RMS} = \frac{1}{4}(1 - M_{oU})I_U^2 + \frac{1}{4}(1 - M_{oD})I_D^2 \tag{7.5}$$

$$i_{SA3}{}^2_{RMS} = \frac{1}{4}(1 + M_{oD})I_D^2 + \frac{1}{4}(1 - M_{oU})I_U^2 - \frac{1}{2}(1 - M_{oU})I_U I_D cos\varphi \tag{7.6}$$

Twelve-Switch Converter

$$|i'_{SA1}|_{Av} = \frac{1}{\pi}(1 + M_{oU}) \times I_U \tag{7.7}$$

$$|i'_{SA2}|_{Av} = \frac{1}{\pi}(1 - M_{oU}) \times I_U \tag{7.8}$$

$$|i''_{SA2}|_{Av} = \frac{1}{\pi}(1 - M_{oD}) \times I_D \tag{7.9}$$

$$|i'_{SA3}|_{Av} = \frac{1}{\pi}(1 + M_{oD}) \times I_D \tag{7.10}$$

$$i'_{SA1}{}^2_{RMS} = \frac{1}{4}(1 + M_{oU}) \times I_U^2 \tag{7.11}$$

$$i'_{SA2}{}^2_{RMS} = \frac{1}{4}(1 - M_{oU}) \times I_U^2 \tag{7.12}$$

$$i''_{SA2}{}^2_{RMS} = \frac{1}{4}(1 - M_{oD}) \times I_D^2 \tag{7.13}$$

$$i'_{SA3}{}^2_{RMS} = \frac{1}{4}(1 + M_{oD}) \times I_D^2 \tag{7.14}$$

b. AC-DC Different Frequency Mode

Nine-Switch Converter

$$|i_{SA1}|_{Av} = \begin{cases} \frac{1}{\pi}(M_{oU} + M_{oD}) \times I_U + \frac{1}{\pi}(1 - M_{oD})[\sqrt{1 - (\frac{I_D}{I_U})^2} + \frac{I_D}{I_U} asin(\frac{I_D}{I_U})] \times I_U, & if I_D < I_U \\ \frac{1}{\pi}(M_{oU} + M_{oD}) \times I_U + \frac{1}{2}(1 - M_{oD}) \times I_D, & if I_D \geq I_U \end{cases}$$

$$|i_{SA2}|_{Av} = \frac{1}{\pi}(1 - M_{oU}) \times I_U + \frac{1}{\pi}(1 - M_{oD}) \times I_D \tag{7.15}$$

$$|i_{SA3}|_{Av} = \begin{cases} \frac{1}{\pi}(1-M_{oU})[\sqrt{1-(\frac{I_D}{I_U})^2}+\frac{I_D}{I_U}asin(\frac{I_D}{I_U})]\times I_U \\ +\frac{1}{2\pi}M_U cos\varphi[\frac{I_D}{I_U}\sqrt{1-(\frac{I_D}{I_U})^2}-asin(\frac{I_D}{I_U})]\times I_U \\ +\frac{1}{2}(M_{oU}+M_{oD})\times I_D, \qquad if I_D < I_U \\ -\frac{1}{4}M_U cos\varphi \times I_U + \frac{1}{2}(1+M_{oD})\times I_D, \quad if I_D \geq I_U \end{cases}$$

$$i_{SA1}{}^2_{RMS} = \frac{1}{4}(1+M_{oU})I_U^2 + \frac{1}{2}(1-M_{oD})I_D^2 \tag{7.16}$$

$$i_{SA2}{}^2_{RMS} = \frac{1}{4}(1-M_{oU})I_U^2 + \frac{1}{2}(1-M_{oD})I_D^2 \tag{7.17}$$

$$i_{SA3}{}^2_{RMS} = \frac{1}{4}(1-M_{oU})I_U^2 + \frac{1}{2}(1+M_{oD})I_D^2 - \frac{1}{2}M_U cos\varphi I_U I_D \tag{7.18}$$

Twelve-Switch Converter

$$|i'_{SA1}|_{Av} = \frac{1}{\pi}(1+M_{oU})\times I_U \tag{7.19}$$

$$|i'_{SA2}|_{Av} = \frac{1}{\pi}(1-M_{oU})\times I_U \tag{7.20}$$

$$|i''_{SA2}|_{Av} = \frac{1}{2}(1-M_{oD})\times I_D \tag{7.21}$$

$$|i'_{SA3}|_{Av} = \frac{1}{2}(1+M_{oD})\times I_D \tag{7.22}$$

$$i'_{SA1}{}^2_{RMS} = \frac{1}{4}(1+M_{oU})\times I_U^2 \tag{7.23}$$

$$i'_{SA2}{}^2_{RMS} = \frac{1}{4}(1-M_{oU})\times I_U^2 \tag{7.24}$$

$$i''_{SA2}{}^2_{RMS} = \frac{1}{2}(1-M_{oD})\times I_D^2 \tag{7.25}$$

$$i'_{SA3}{}^2_{RMS} = \frac{1}{2}(1+M_{oD})\times I_D^2 \tag{7.26}$$

Publication I

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Publication IV

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Publication V

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Publication VI

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