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Abstract- **A new state observer-based current balancing method for Modular Multilevel Converters with Interleaved half-bridge Sub-Modules (ISM-MMC) is presented in this paper. The developed observer allows estimating currents through interleaved half-bridge legs in each submodule of ISM-MMC basing only on arm current and submodule's capacitor voltage measurements. Then, the interleaved current balancing control uses the estimated currents to reduce the interleaved currents imbalance caused by upstream control actions. This technique minimizes the number of required current sensors in ISM-MMC, thereby reducing the converter's cost, weight, and volume. Capabilities of the proposed sensorless interleaved currents balancing control has been tested against standard parameter tolerances of the composing passive elements. In addition to that, a novel capacitor voltage balancing strategy for MMCs is developed. The new algorithm contains main advantages of the classical sorting-based capacitor voltage balancing methods while provides an opportunity to decouple two balancing tasks of ISM-MMC, namely capacitor voltage and interleaved legs current balancing. The feasibility of the proposed methods is verified by extensive simulation and experimental tests on a laboratory prototype by the corresponding system response under the output characteristics variation and interleaved current control perturbation.**

Index Terms—**modular multilevel converter, interleaved converters, interleaved half-bridge submodule, sensorless current balancing, current sharing, capacitor voltage balancing**

I. INTRODUCTION

Demand for efficient high-power conversion systems has recently increased in industrial applications at all voltage levels. The common objectives in converter design are larger power capacity, higher power density and better power quality. In this sense, modular multilevel converters (MMCs) have already taken over the market in high- and ultra-high voltage applications [1], [2]. Recently, they have been also expanded on medium- and low-voltage applications [3]–[5]. The scalable structure of MMCs allows meeting the imposed voltage requirements by stacking the so-called submodules (SMs) in a series. SMs are normally composed by half-bridge or full-bridge configuration, while other structures are also possible [4], [6]. An increase in current capacity

can be attained in several ways, for instance, by parallel connection of power units at submodule level, arm and phase leg paralleling or even synchronized operation of several converters, as it is already reported in [7]. Another solution to achieve a higher current capacity in MMCs has been proposed in [8]. The new MMC architecture is based on interleaved half-bridge submodules, and as the name suggests, it employs the interleaving effect of the parallel-connected half-bridges. In such an arrangement, the Modular Multilevel Converters with Interleaved half-bridge Sub-Modules (ISM-MMC) demonstrates equal or superior performance (current rating scalability ease, enhanced quality of generated ac voltage waveforms, efficiency, etc.) than classical MMCs, considering identical power ratings and power switch count [9]. Due to its advantages, ISM-MMC is especially attractive in high-power, low/medium-voltage applications where classical MMC structures have limited usage due to its only one degree of freedom, namely voltage scalability. The single-phase structure of ISM-MMC is depicted in Fig. 1. The ISM-MMC resembles a double-star MMC topology without standalone arm inductors. In this case, the arm inductors are distributed among N converters' SMs. The submodule itself consists of K parallel half-bridge legs connected to a capacitor on the dc side. The midpoint of each leg is linked with an individual inductor. The other side of the inductors is joined together, creating a positive terminal of the SM.

Under ideal conditions, the current is shared equally among the half-bridges in each SM. However, the interleaving modulation scheme applied to the SM implies that the commutation between parallel legs happens in a time shifted manner. In addition to that, circuit nonlinearities (differences among equivalent branch
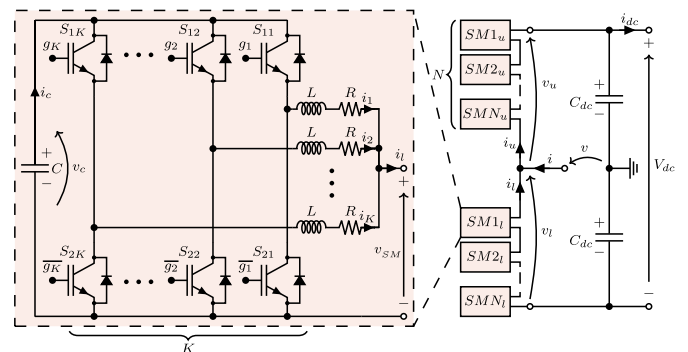

Fig. 1. Circuit diagram of a single-phase ISM-MMC.

resistances), unequal dead-times, upstream control actions and many other factors may lead to the instantaneous current imbalance of the fundamental components between the interleaved legs [8], [9]. A uniform distribution of the total arms current among the parallel legs has to be ensured to avoid excessive converter losses, thermal stress and saturation of the inductors while ensuring optimal capacity utilization of the SM half-bridges. Most of the conventional ways to solve this problem are based on sensing each interleaved current to provide the current information for the dedicated active control loop. This approach is well established for dc/dc [10], [11] and some ac/dc converters [12]. A similar method can be implemented in an ISM-MMC. However, an obvious drawback of these current balancing techniques is a large number of current sensors that is almost proportional to the number of interleaved units. To compact the converter and reduce its cost and complexity, several current estimation techniques have been developed for interleaved dc/dc converters, based on parasitic resistance estimation [13], small-signal duty cycle perturbation [14], self-tunable digital filter [15], temperature equalization [16] and many other. Even though some of the aforementioned methods allow compensate mismatch in circuitry parameters, however, they mostly suit well for dc/dc converters with slow variance of the average current and with relatively small number of parallel units. Complexity of the estimator grows significantly with an increase of the number of parallel units, thus, these schemes are not flexible in scaling. Similarly, several works have been dedicated to estimation algorithms to solve another common balancing problem for MMC structures, namely currentless sorting-based capacitor voltage balancing. For instance, authors in [17] proposed a current sensorless capacitor voltage balancing method based on a state observer. The observer provides estimates of arm currents that are typically used in most capacitor voltage balancing algorithms. Nevertheless, this topic falls out of the scope of current article.

Since ISM-MMC has been just recently introduced, very few works are dedicated to this topology. This basis from one side adds novelty to the ISM-MMC topics, from the other suggests that a single article is not capable to cover all concerns of the new topology. In fact, [9] is the only comprehensive work that includes a complete mathematical model, describes operational principle, provides control layout design, demonstrates comparative analysis among similar MMC based arrangements and calculates efficiency of the compared converters. Nevertheless, this work does not provide a solution for interleaved currents balancing problem. Thus, to the best of the authors' knowledge, no publications have been focused on the aforementioned issue in ISM-MMCs. Furthermore, no estimator based interleaved current balancing strategies have been presented in literature either. The main contribution of the current work concerns an implementation of the sensorless interleaved current balancing control loop for ISM-MMC and an analysis of its dynamic behavior under various system perturbations. In this context, the term "sensorless" means that there are no interleaved currents measurements needed. The proposed method is capable with a good accuracy to allocate interleaved HB-leg currents around their average value, while purely relaying on their estimation. In addition to that, a new capacitor voltage balancing strategy has been introduced to make possible the operation of the proposed interleaved currents balancing technique. It has been also demonstrated that even though the circuital parameter variation affects performance of the

implemented observer, the new current balancing method can still compensate for the current imbalance, which originates from the actions of the upstream capacitor voltage balancing strategy. Capabilities of the newly introduced observer and the implemented interleaved current control loop has been thoroughly investigated via numerous numerical simulations and experimental tests. It should be pointed out though that in order to avoid repetition of the material presented in [8], [9] and to short the discussion, making it more emphasized on the studied subject, the current article skips detailed introduction of the ISM-MMC topology, referring to available publications. Furthermore, being focused solely on the interleaved currents balancing problem in ISM-MMCs, this article does not concern other challenges (e.g., interleaved inductor design, etc.) associated with ISM-MMC.

The paper is structured as follows. Section II introduces the current equalization problem in ISM-MMCs, providing essential control diagrams. The novel capacitor voltage balancing control for MMC structures is discussed in Section III. The required mathematical background of the proposed state observer is explained in Section IV. In this section, observability and stability of the implemented state estimator is discussed in great detail. The sensorless current balancing technique is discussed in Section V. Sections VI and VII verify the usefulness of the proposed current sharing technique by presenting simulation and experimental results. In addition to that, some considerations about the observer's sensitivity concerning parameter variation, are highlighted there as well. Section VIII summarizes and concludes the paper.

II. CURRENT BALANCING PROBLEM IN ISM-MMCs

It is worth to notice in Fig. 1 that the average model of the ISM-MMC does not change with respect to a classical MMC structure based on a half-bridge submodule. Therefore, strictly speaking, the typical outer and inner control loops of the classical MMC are also applicable in the ISM-MMC. Many publications have been dedicated to various control methods for the conventional MMC topology and reported very clearly, for example, in [18], [19]. In addition to that, [9] gives a comprehensive description of the ISM-MMC control structure that has been used eventually in current work. Therefore, the present paper presents only parts of the control layout that are involved in the discussion, while the other treated as well-known and thus depicted as a "black" box.

The block diagram of the implemented control loops with reference to the single-phase ISM-MMC (cf. Fig. 1) and its operation in rectification mode, is illustrated in Fig. 2.

Outputs of the classical MMC control scheme, which are two voltage references of upper and lower arm voltages, enter modulation block (marked in red dashed line, cf. Fig. 2). This block represents a hybrid carrier-based pulse-width modulation
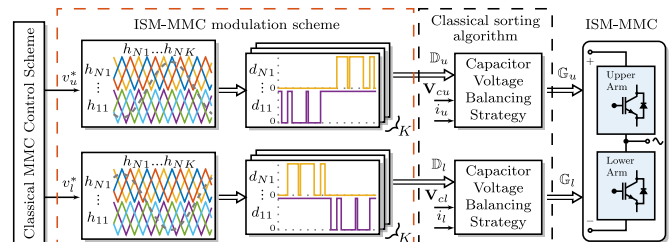

Fig. 2. Block diagram of the ISM-MMC control employing classical capacitor voltage balancing technique [9].

(PWM) method, designed specifically for ISM-MMCs [8]. It is formed of a level-shifted PWM (LS-PWM) for generating voltage levels given by series-connected SMs whether a phase-shifted PWM (PS-PWM) scheme handles interleaving of parallel HB-legs within each SM. Thus, there are KN carriers in total. Having as an input of the modulation block the upper arm voltage reference, it produces a 2D set ($\mathbb{D}_u$) of logical PWM signals ($d_{11},\dots d_{NK}$). Similarly, the lower arm PWM set $\mathbb{D}_l$ is generated. Later, these two sets are applied to the classical sorting-based capacitor voltage balancing strategy. In the classical balancing method, associated with carrier-based PWM, the capacitor voltages (vectors $\mathbf{V}_{cu}$, $\mathbf{V}_{cl}$) within one arm are sorted either in ascending or descending order in accordance with the direction of the arm current. Then, the input gate signals are rearranged in agreement with the sorted capacitor voltages and the direction of the arm current. It is important to notice that this algorithm operates directly on the generated set of PWM signals (2D arrays $\mathbb{D}_u$, $\mathbb{D}_l$). The output of this block is a set of logical gate signals (2D arrays $\mathbb{G}_u$, $\mathbb{G}_l$) that drive switches. Since regulation of capacitor voltages in this control arrangement is the independent and ultimate step of the ISM-MMC control, it is not hard to show that this regulator will try to balance capacitor voltages disregarding the proper share of the interleaved currents within each submodule. Therefore, any control method designed to balance the interleaved currents and applied upstream of the capacitor voltages balancing block (e.g., acting on arm voltage references) will fail. In addition, the small internal resistance of the individual interleaved inductors, having standard tolerances, may result in huge current imbalances among the interleaved legs. This fact becomes even more evident when the values of those internal resistances are comparable with, for instance, the equivalent on-state resistance of the power switches. Thus, a closed-loop control strategy that balances interleaved currents is essential for ISM-MMC. It is worth noticing that the regulation of interleaved currents features faster dynamics with respect to capacitor voltage balancing. So, the interleaved currents control must be the ultimate step of the ISM-MMC control. Moreover, as will be explained in the following section, this paper proposes an interleaved legs current balancing regulator that acts individually on modulating references of each SM. Therefore, a new capacitor voltage balancing function that operates directly on reference signals is proposed as well.

III. NOVEL CAPACITOR VOLTAGE BALANCING STRATEGY

This section explains a few modifications of the conventional MMC closed-loop method that must be implemented to successfully balance both capacitor voltages in series connected SMs and interleaved currents in each SM. The principal block scheme of the modified control part is illustrated in Fig. 3. It consists of the classical MMC control part that generates voltage references for upper (v_u*) and lower (v_l*) converters' arms; a novel capacitor voltage balancing strategy, which directly operates with the arm voltage references, producing K copies of the individual SM voltage references (e.g., v_{u11}*... v_{uN1}*); an original sensorless interleaved legs current balancing method that eventually followed by the hybrid ISM-MMC modulation scheme [8], [9]. The new blocks are clearly discussed in this and the following sections.

As suggested in [20] with reference to a classical MMC, arm voltage synthesis can be decoupled from the selection of which SM
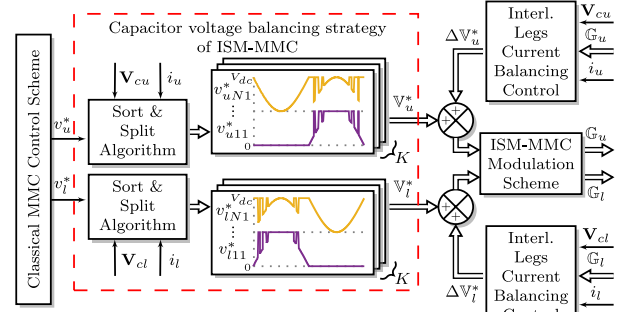

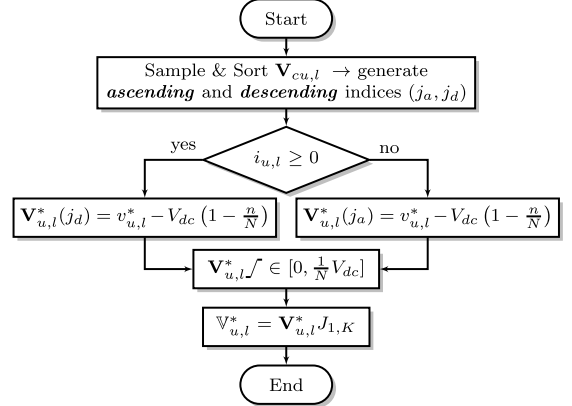Fig. 3. Block diagram of the modified ISM-MMC control method.

Fig. 4. Flowchart of the proposed Sort & Split algorithm.

must commutate at each instant. Based on this idea, several "sorting & select" algorithms have been proposed in the literature (e.g., [21]) to maintain capacitor voltage ripple within a specific limit. As pointed out in the previous section, the average model of ISM-MMC is identical to the one of classical MMC with half-bridge SMs. Therefore, strictly speaking, all invented sorting functions for the classical MMC are equally applicable in the case of ISM-MMC. The new "sort & split" algorithm permits to employ the paradigm of the well-established sorting functions while operating with reference voltages rather than with firing pulses. The flowchart depicted in Fig. 4 explains the logic behind the introduced algorithm. It starts by sampling and sorting capacitor voltages with a constant updating frequency (f_{sort}), eventually generating lists of indices (j_a, j_d) with sampled capacitor voltages in ascending and descending order. By considering the sign of the corresponding arm current that demonstrates whether the capacitor is charging or discharging, the reference voltage of each SM is synthesized. A rule to form SM reference voltage is the same for both paths, and it is based on a general idea of adding/removing extra levels following the reference arm voltage. The difference is in selecting a SM that must be inserted or bypassed (where n is the ordinal number of a SM and N is the total number of SM per arm). This selection is based on the previously generated lists of indices. During a sorting period, SM reference voltages are organized in descending order if arm current is positive; otherwise, in ascending order. At this stage, vectors of SM reference voltages ($\mathbf{V}^*_{u,l}$) for the upper and lower arms are formed. A saturation block is required to split arm voltage reference between the SMs properly. A possible shape of the generated SM voltage references can be seen in Fig. 3. It is clear that the waveform of reference SM voltages is highly dependent on updating frequency f_{sort}. The next block creates K copies of the reference vectors, composing 2D sets ($\mathbb{V}^*_{u,l}$) of SM

reference voltages for the upper and lower arms, respectively. This mathematical operation is required for subsequent adjustments of the reference voltages individually for each interleaved leg within a SM. It can be easily demonstrated that the new sorting function produces an identical switching pattern in comparison with the analogous sorting algorithm for the classical MMC. In fact, the proposed technique can be used for the classical MMC as well by setting K equal to 1.

The next block in Fig. 3 to be explained is interleaved legs current balancing control. However, this block is estimator based, therefore, an estimator design must be presented prior.

IV. DESIGN OF THE STATE OBSERVER

As depicted in Fig. 1, a single-phase ISM-MMC consists of two arms; each one of them comprises a series connection of submodules. The submodules are formed using multiple half-bridge converters (units) connected in parallel to a common dc capacitor (C). Inductors (L) are used to connect each half-bridge converter to a common point, which forms a positive terminal of the submodule. Resistances (R) placed in series with inductors represent equivalent series resistances of each branch. For the following analysis, parameters (R, L, C) in the N submodules and in the K units are assumed to be identical among themselves, unless otherwise stated. The second terminal of the submodule constitutes the negative dc rail.

With respect to Fig. 1, the voltage of a generic n-th submodule can be written as

$$v_{SM} = \frac{1}{K}\left[\mathfrak{z}v_c - L\sum_{k=1}^{K}\frac{di_k}{dt} - R\sum_{k=1}^{K} i_k \right], \quad (1)$$

where i_k, v_c, v_{sm} and $\mathfrak{z}$ are the current flowing in the k-th interleaved unit, submodule's capacitor voltage, submodule voltage and number of active half-bridge legs, respectively. In other words, $\mathfrak{z}$ correspond to the summation of the switching functions g_k (binary values) of all the K legs

$$\mathfrak{z} = \sum_{k=1}^{K} g_k. \quad (2)$$

By applying the second Kirchhoff's law for a generic half-bridge unit within the SM, the derivative of the current, flowing through the branch, can be found by

$$\frac{di_k}{dt} = \frac{1}{L}\left[v_c g_k - Ri_k - v_{SM} \right]. \quad (3)$$

Current passing through the SM's capacitor (i_c) at any instant can be determined either from the capacitor equation or as an active legs' current summation:

$$i_c = -C\frac{dv_c}{dt} = \sum_{k=1}^{K} (i_k\, g_k). \quad (4)$$

Therefore, from (4) one can obtain the time derivative of the capacitor voltage as

$$\frac{dv_c}{dt} = -\frac{1}{C}\sum_{k=1}^{K} (i_k\, g_k) = -\frac{i_c}{C}. \quad (5)$$

Summing up each single current derivative in (3) evaluated for all active HB-legs (only the ones having $g_k = 1$) capacitor current time derivative can be written as:

$$\frac{di_c}{dt} = \frac{\mathfrak{z}}{L}\left[v_c - \frac{R}{\mathfrak{z}}i_c - v_{SM} \right] = \frac{1}{L'}[v_c - R'i_c - v_{SM}], \quad (6)$$

where R' and L' accordingly represent SM's equivalent resistance and inductance with respect to a number of active HB-legs. In other words, capacitor current can be referred to an equivalent branch current that accounts for all interleaved currents in $\mathfrak{z}$ active HB-legs. Equations (5) and (6) form the basic set of equations that describe state variables (v_c and i_c) of an equivalent SM.

A. Observability Verification

A system is said to be observable if the entire system's behavior can be estimated from the system's outputs, which are generally sensed. It can be noted from (5) that the capacitor voltage, by means of the capacitor current, contains information about all interleaved currents that flow in the submodule. Therefore, by selecting capacitor voltage as an output of the system, the observability of the newly proposed state estimator can be verified based on any arbitrarily selected number of half-bridge units. Equations (5) and (6) can be transformed into the state-space representation:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx \end{cases}, \quad (7)$$

where state, input and output vectors can be defined as $x = [v_c, i_c]^T$, $u = v_{SM}$ and $y = v_c$, respectively. Matrices A, B and C denote state, input, and output matrices, respectively. Replacing (5) and (6) inside (7), the state-space form can be rewritten as

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} v_c \\ i_c \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{C} \\ \dfrac{\mathfrak{z}}{L} & -\dfrac{R}{L} \end{bmatrix}\begin{bmatrix} v_c \\ i_c \end{bmatrix} - \dfrac{\mathfrak{z}}{L}\begin{bmatrix} 0 \\ 1 \end{bmatrix}v_{SM} \\ v_c = \begin{bmatrix} 1 & 0 \end{bmatrix}\begin{bmatrix} v_c \\ i_c \end{bmatrix} \end{cases}. \quad (8)$$

The observability matrix O, in the form

$$O = \begin{bmatrix} C \\ CA \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & -\dfrac{1}{C} \end{bmatrix}, \quad (9)$$

has always full rank regardless the time varying nature of $\mathfrak{z}$. Therefore, as foreseeable, it is always possible observe states v_c and i_c, having sensed the capacitor voltage only.

Carriers phase shift, associated with interleaved modulation scheme, has a crucial role in interleaved currents estimation since it opens a possibility, within each switching period T_{sw}, to formulate multiple values of capacitor current ($i_{c,k}$) derived from corresponding sets of HB-leg currents i_k bearing in mind HB-leg's active states (i.e., $g_k = 1$). If K capacitor currents related to a set of independent K-tuple gate signals g_k can be identified, the set of K HB-leg currents i_k can be reconstructed every switching period from the sole knowledge of the capacitor voltage v_c. The latter statement can be formalized by stacking K times (4) in the form

$$\begin{bmatrix} i_{c,1} \\ i_{c,2} \\ \vdots \\ i_{c,K} \end{bmatrix} = [G]\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_K \end{bmatrix} = \begin{bmatrix} g_{1,1} & g_{2,1} & \cdots & g_{K,1} \\ g_{1,2} & g_{2,2} & \cdots & g_{K,2} \\ \vdots & \vdots & \ddots & \vdots \\ g_{1,K} & g_{2,K} & \cdots & g_{K,K} \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_K \end{bmatrix}, \quad (10)$$

where each row represents a different capacitor current composition, depending on the binary states of high switch in each HB-leg.

If the duty cycle δ given by the modulating signal stays below $1/K$, it is always possible to rewrite G as the identity matrix. On the other hand, if the duty cycle δ attain values above $(K-1)/K$, the
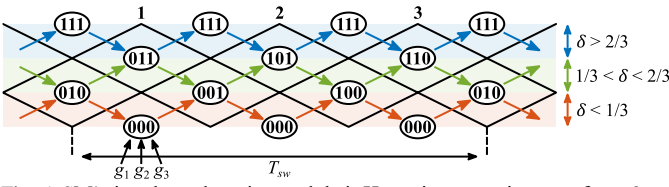
Fig. 5. SM's interleaved carriers and their Hamming space in case of $K = 3$.

matrix G converts into a matrix of ones with the main diagonal made of zeros. For all the remaining values of duty cycle δ, the Hamming space of gate signals K-tuple is characterized by non-repetitive configurations, which sequentially permutate with unity Hamming distance. Therefore, it is always possible to find K set of independent K-tuple gate signals g_k. In other words, regardless of the number of interleaved half-bridges, at least one invertible matrix G can be identified every switching period. Hence, being (10) solvable, the observability of each interleaved current can always be guaranteed.

These considerations are intuitively depicted in Fig. 5 for a submodule having three half-bridges ($K = 3$).

It clearly stands out that a SM is observable only in the occurrence of switching actions. Interleaved currents in bypassed or fully inserted submodules with all the gate signals of upper switches in HB-legs either equal to 0 or 1 are not observable (at least within a generic switching period).

B. Observer

The state observer model of a physical LTI system can be represented by

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + Bu + L(y - \hat{y}) \\ \hat{y} = C\hat{x} \end{cases}, \tag{11}$$

where $\hat{x}$ and $\hat{y}$ are estimates of the corresponding plant's state and output. Matrix L comprises observer gains.

By substituting (5) and (6) into (11) and denoting variables of matrix $L = [l_v, l_i]$, the following equations can be derived

$$\begin{cases} \dfrac{d\hat{v}_c}{dt} = -\dfrac{\hat{i}_c}{C} + l_v(v_c - \hat{v}_c) \\ \dfrac{d\hat{i}_c}{dt} = \dfrac{\mathfrak{z}}{L}\left[v_c - \dfrac{R}{\mathfrak{z}}\hat{i}_c - v_{SM}\right] + l_i(v_c - \hat{v}_c) \end{cases}, \tag{12}$$

being $\hat{v}_c$ and $\hat{i}_c$ estimates of capacitor voltage and current, respectively. By analyzing (13), one may notice that the knowledge of submodule voltage is required to derive the state of the capacitor current. Although this voltage can be measured directly, such an approach requires to double number of voltage sensors in ISM-MMC in comparison with classical MMCs, which is not an optimal solution from many perspectives (cost, volume, etc.), including a concern about sufficient bandwidth of the voltage sensors. Thus, the voltage can be derived indirectly from (1), bearing in mind that the sum of interleaved currents inside an SM is actually the arm current

$$i_{u,l} = \sum_{k=1}^{K} i_k \tag{14}$$

resulting in the following expression of SM voltage

$$\hat{v}_{SM} = \frac{1}{K}\left[\mathfrak{z}v_c - L\frac{di_{u,l}}{dt} - Ri_{u,l}\right] \tag{15}$$

Estimate sign ("hat") is added to submodule voltage in (15) to point out that it is indirectly obtained based on sensed capacitor voltage and arm current. It should be noted that the arm current

sensors are required in addition to typical capacitor voltage measurements. Nevertheless, the arm currents are commonly measured in MMC structures (depending on the control design). It also must be highlighted that the considered in (15) equivalent circuit parameters (R/K, L/K) are rated values and likely to be different in a real system. However, the voltage drops accounted by the parameters in (15) have significantly lower magnitude with respect to the capacitor voltage ($v_{c,n}$). In addition, variation of real circuitry parameters is generally limited by manufacturing tolerances, which are in the range of few tens of percent. Therefore, the reconstructed SM voltage has quite a good accuracy with respect to the actual value, and it can be treated as an independent variable in (13).

Having the estimates of capacitor current in each SM's switching configuration, the HB-leg currents can be derived by

$$\begin{bmatrix} \hat{i}_1 \\ \hat{i}_2 \\ \vdots \\ \hat{i}_K \end{bmatrix} = [G]^{-1}\begin{bmatrix} \hat{i}_{c,1} \\ \hat{i}_{c,2} \\ \vdots \\ \hat{i}_{c,K} \end{bmatrix}. \tag{16}$$

C. Stability of the Observer

Considering definition of the estimated model (capacitor voltage and current) given by (12), (13) and subtracting it from the plant's model formulated by (5) and (6), the observation error dynamics has the following form:

$$\begin{cases} \dfrac{d\tilde{v}_c}{dt} = -\dfrac{\tilde{i}_c}{C} - l_v\tilde{v}_c \tag{17} \\ \dfrac{d\tilde{i}_c}{dt} = -\dfrac{R}{L}\tilde{i}_c - l_i\tilde{v}_c \tag{18} \end{cases},$$

where $\tilde{v}_c = v_c - \hat{v}_c$ and $\tilde{i}_c = i_c - \hat{i}_c$ are observation errors of capacitor voltage and current, respectively.

The stability of the designed observer (i.e., the trajectories of estimates do not diverge from their corresponding real values) can be formulated by exhibiting a Lyapunov function that corresponds to the energy in the increment with respect to an arbitrary, nominal state trajectory. For the observer, the energy in the increment takes the form [22]:

$$W_e = \frac{1}{2}C\tilde{v}_c^2 + \frac{L}{2\mathfrak{z}}\tilde{i}_c^2, \tag{19}$$

which is clearly positive definite function. Its derivative is

$$\dot{W}_e = C\tilde{v}_c\dot{\tilde{v}}_c + \frac{L}{\mathfrak{z}}\tilde{i}_c\dot{\tilde{i}}_c. \tag{20}$$

By substituting (17) and (18) into (20) yields

$$\dot{W}_e = -l_vC\tilde{v}_c^2 - \frac{R}{\mathfrak{z}}\tilde{i}_c^2 - (1 + l_i\frac{L}{\mathfrak{z}})\tilde{v}_c\tilde{i}_c, \tag{21}$$

where circuital parameters (R, L, C), number of active half-bridge legs $\mathfrak{z}$ and observer gains (l_v, l_i) are strictly positive real numbers. In (21), the first two terms are negative definite, while the last term bounded and can be either positive or negative. Therefore, selecting relatively large l_v and reasonable l_i can ensure $\dot{W}_e < 0$, which will force the observation error converge to zero.

V. CURRENT BALANCING METHOD

This section explains an algorithm of sensorless current balancing method in ISM-MMCs (cf. Fig. 3) that is based on the estimator designed in previous section. Fig. 6 depicts a block diagram of the proposed current balancing scheme. There are few steps to obtain estimated values of interleaved currents that are
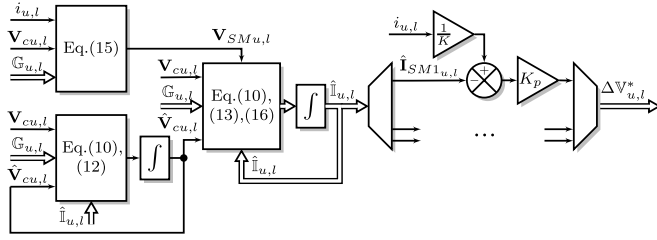
Fig. 6. Block diagram of the proposed state observer-based interleaved legs current balancing control.

typically used in the feedback loop of the proportional controller. The very first step is to compute submodule voltage (cf. Equation (15)) based on measured values of arm current, capacitor voltages and known set of firing signals. At the same time, an estimate of each capacitor voltage must be obtained based on (10) and (12). Eventually, both those quantities enter the interleaved current prediction block formed by (10), (13) and (16). Later all individual current derivatives are integrated to obtain estimated interleaved currents for each SM. Then, individually computed current errors are followed by a proportional controller (K_p) that generates portions of reference voltages. These voltage fractions are eventually added to the individual SM voltage references that have been formed by the introduced Sort & Split algorithm (cf. Section III). All in all, each interleaved leg is independently controlled, providing a high dynamic response to any rapid disturbance in the controlled system. It is evident that the sum of current errors (difference between real interleaved current and its balanced average value) within a SM is equal to zero. Thus, the sum of additive voltage portions ($\Delta \mathbb{V}_{u,l}^*$) generated by the control loop in Fig. 6 within one SM is also zero. As a result, the average value of SM voltage remains unchanged due to the operation of the proposed control.

The implemented interleaved legs current balancing control has the objective to balance fundamental components of the interleaved currents within a single SM, naturally unbalanced due to upstream control actions. Hence, it is an individual, SM-level control method. With the rise of the number of SM, the computation burden on a controller will increase proportionally. Therefore, an efficient hardware realization of the control constitutes an optimization problem. This discussion falls outside the scope of this paper. Given that the observer part (cf. Equations (12), (13) and (15)) has only a few derivatives and integrals to compute, as well as the switching frequency of individual semiconductors in ISM-MMCs usually tend to be up to a few kHz; hence the controller has sufficient time to compute and update the estimates in one PWM cycle. In this context, most of the entry-level microcontrollers will satisfy the computation requirement of the proposed current balancing method.

VI. NUMERICAL SIMULATIONS

This section presents some simulation results that aim to validate the performance of the implemented capacitor voltage balancing method, state observer and the interleaved legs current sensorless balancing method. It must be stressed here, though, that the primary objective of latter two control loops is to balance individual interleaved currents in each HB-leg around their average value given the current imbalance due to actions of capacitor voltage balancing. So, the main focus here is whether the built interleaved current regulator can balance the currents or not,

TABLE I
MAIN PARAMETERS OF THE SIMULATION MODEL

Description	Labels	Parameters
number of SMs per arm	N	2
number of interleaved HB legs in each SM	K	3
individual interleaved leg equivalent parameters	R, L	234.7 mΩ, 2.5 mH
capacitance in each SM	C, ESR	6.4 mF, 0.2 mΩ
rated ac power and line-to-neutral voltage (rms)	P_{ac}, V	60 kW, 353.6 V
power factor	-	0.985
fundamental frequency	f	50 Hz
rated dc-link voltage	V_{dc}	1000 V
carrier frequency	f_{cr}	1 kHz
sorting frequency	f_{sort}	333 Hz
sampling time	T_s	2 µs
observer current and voltage gains	l_i, l_v	10 H^{-1}, 20000 s^{-1}

while whether the new capacitor voltage balancing fulfils its main purpose. To validate this matter, the simulation model involves a simple single-phase ISM-MMC structure with two SMs per arm ($N = 2$) and three interleaved HB-legs within each SM ($K = 3$) (cf., Fig. 1). Here submodules are labeled as SM1…SM4, starting from the top submodule. The converter works as an inverter supplying power from dc to ac side connected to a constant, passive load. The converter is regulated with output current open-loop control by setting desired reference phase voltage manually with limit of 353.6 V (rms) in linear modulation range. The internal control loops, namely circulating current control and capacitor voltage balancing, are always activated to keep the operation of ISM-MMC stable and balanced. Two ideal voltage sources are placed instead of dc-link split capacitors (C_{dc}) to eliminate related dc voltage imbalances in single-phase structure. The key parameters of the implemented simulation model are given in Table I, and they correspond to a single-phase version (60 kW) of the three-phase ISM-MMC (180 kW) design example introduced in [9] for a high-power electrical vehicle dc charger. Here the selected switching frequency of individual semiconductors is a design choice, which mainly subjected by the grid side requirements to limit harmonic pollution. Furthermore, the total equivalent switching frequency of the ISM-MMC converter can be adjusted by varying either number of SMs/interleaved legs inside of SMs or both, limiting the switching frequency of individual components [9].

The first simulation test was designed to demonstrate performance of the proposed state observer-based interleaved legs current balancing control under ideal working conditions, namely when the system R, L, C parameters are well known and equal among themselves. In this test the rated parameters of the corresponding components (cf. Table I) were set as simulation initialization values in circuitry components and in the estimator settings. Fig. 7 depicts simulated interleaved currents, their comparison against the corresponding estimated values and distribution of observation errors when interleaved current control in the entire ISM-MMC is enabled (zones with white background) or disabled (gray zone). It is interesting to note that when the implemented state observer-based interleaved current balancing method is active, the fundamental components of currents within a SM are perfectly balanced. Once it is deactivated, these currents start getting instantly imbalanced. The reason is that the capacitor voltage balancing control forces switches commutate to satisfy its objective, balance capacitor voltages around their mean. The equivalent resistance of individual HB-legs acts as a damping factor limiting this unbalance. The lower the value of the equivalent resistance, the greater the current imbalance. Nevertheless, as it is visible from Fig. 7b-Fig. 7g, the estimated interleaved currents nicely repeat the
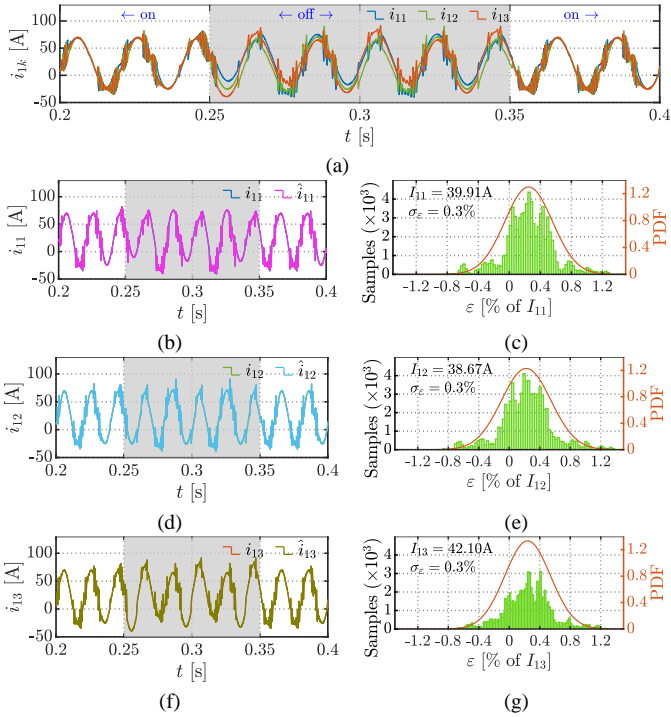
Fig. 7. Simulated interleaved currents in SM1 (a), timeseries of simulated and observed interleaved currents (b,d,f) with corresponding distribution of observation error (c,e,g) under **equal** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.
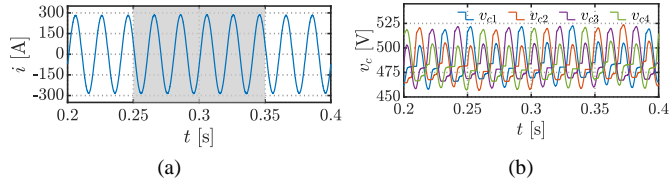

Fig. 8. Timeseries of simulated converter's ac phase current (a) and capacitor voltages (b) under **equal** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.
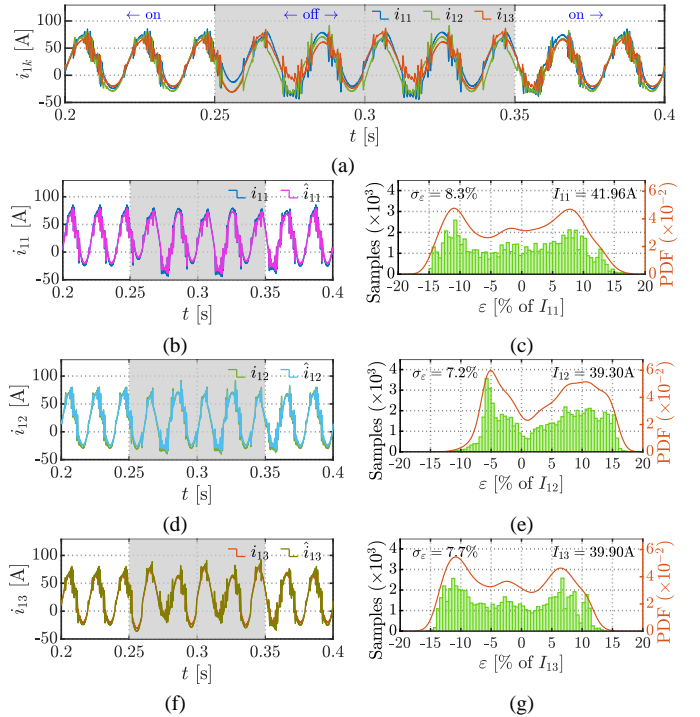

Fig. 9. Simulated interleaved currents in SM1 (a), timeseries of simulated and observed interleaved currents (b,d,f) with corresponding distribution of observation error (c,e,g) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.
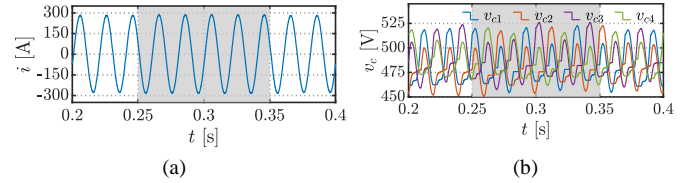

Fig. 10. Timeseries of simulated converter's ac phase current (a) and capacitor voltages (b) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.

simulated counterparts with minimal observation error staying within ±1.2% of each individual current rms value. Here it also must be pointed out that the performance of the estimator does not depend on whether the currents are equally shared or not (cf. Fig. 7b,d,f, "on" and "off" zones). The absolute error value is calculated at each sample within a given time range, subtracting simulated from estimated values. The error normalization is done with individual current rms since these currents are composed of dc, fundamental and high (switching) frequency components. Probability density functions (PDF) are calculated by using either "normal" or "kernel" distributions.

To verify that the current balancing can be implemented in a real system, where all internal components are subjected to manufacturing tolerances, the next numerical test is done with unequal circuitry parameters within each SM. In this test unequal circuitry parameters were set only as simulation initialization parameters, while the estimator is still supplied with rated parameters of the corresponding components (cf. Table I) since their true value are not known in real systems. The following simulation test shows similar zones (cf. Fig. 7) with active and inactive interleaved currents balancing loops. However, this time the R, L, C parameters of each SM in ISM-MMC have randomly distributed values. The parameter tolerances are limited by 30% of

their nominal values (cf. Table I). Accounting for these tolerances in the simulation is made by generating random numbers with a Gaussian distribution and confidence interval of ±4σ. For example, individual HB-leg equivalent resistances in SM1 (upper arm) are [229.3, 252.7, 228.5] mΩ, inductances [2.3, 2.4, 2.8] mH and capacitance of the SM's capacitor is 6 mF, while the estimator settings are correspond the values listed in Table I. It can be noted from Fig. 9a that due to these unequal parameters within a SM, the simulated interleaved currents cannot be perfectly aligned as it was in the case of Fig. 7a, even with activated interleaved current control. However, those currents are stabilized around their average value, demonstrating balanced, sinusoid-like waveforms. Again, once the control is disabled, the currents got imbalanced, however, with a larger magnitude due to the parameter's inequality. This time the estimation error is almost uniformly distributed in ±15% of each individual current rms. Nevertheless, state observer performs quite well, following the real, simulated currents in interleaved legs.

Simulation results depicted in Fig. 8 and Fig. 10 demonstrate a good correspondence to the theory. Specifically, one can notice that the reasonable interleaved current imbalance within a SM (cf. Fig. 7a and Fig. 9a) does not affect the output characteristics of ISM-MMC (ac phase currents have purely sinusoid-like shape)
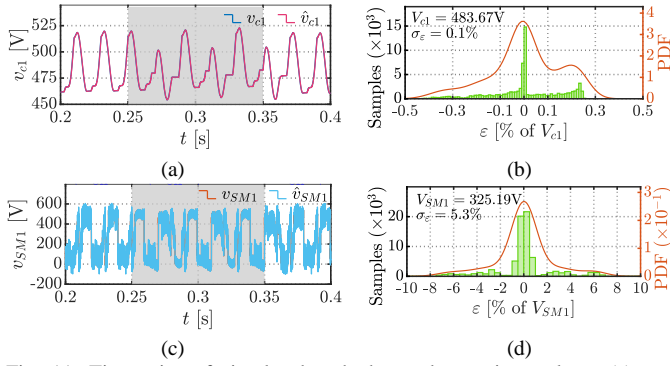
Fig. 11. Timeseries of simulated and observed capacitor voltage (a) and submodule voltage (c) of SM1 with corresponding distribution of observation error (b) and (d) under **random** R, L, C parameters and timeslots of enabled/disabled interleaved current balancing control.

and balancing of the SMs' capacitor voltages. In fact, the aforementioned characteristics in ISM-MMC have independent control loops and can be treated as decoupled tasks. Small magnitude mismatch of capacitor voltages, noticeable in Fig. 10b (compare Fig. 8b and Fig. 10b) proves that the preset capacitances in simulation initialization parameters have unequal values. Nevertheless, this parameters mismatch does not affect performance neither the proposed capacitor voltage balancing method (cf. Section III) nor the observer-based interleaved currents balancing control (cf. Sections IV, V).

To demonstrate estimation performance in terms of capacitor and submodule voltage, which are variables of the observer law, Fig. 11 depicts time-series with simulated and observed capacitor and submodule voltage of SM1 with corresponding observation errors. The absolute values of these errors were normalized with the corresponding rms value of the voltage, similar to interleaved currents. The observation error for capacitor voltages is close to 0, showing that inequality of the parameters does not play a relevant role here. In the case of capacitor voltage estimation, this happens mainly because capacitor voltage is an output of the observer and it is a sensed value; hence, the observer can track this voltage precisely. Unlike the capacitor voltage, the submodule voltage is estimated based on arm current and simulated capacitor voltage, and it depends on the equivalent circuit of an SM (cf. Equation (15)). Despite that, as explained in Section IV, the voltage drops on the R, L elements of the circuit are small compared to SM capacitor voltage. Hence relatively small mismatch in the parameters does not produce a vast estimation error.

Overall, the implemented state observer-based interleaved legs current balancing control is able quite well to reach its objective, namely balancing the individual interleaved currents around their average even in the case with unequal circuit parameters. In this context, the current regulator compensates the current imbalance due to upstream control (the main contribution comes from the capacitor voltage balancing algorithm). Hence, there is always a current error present between individual interleaved leg current and the legs common average value even in the case with equal circuitry parameters. This error provokes the controller to generate a proportional voltage increment that adds to the HB-leg's average voltage. This action repeats until the estimated current does not reach the target. The current imbalance given by characteristic inequality of the composing elements (typically small due to the proper design of the converter) cannot be eliminated since the designed observer operates with rated values rather than real

system parameters. An additional estimation loop can be implemented to assess the actual parameters of the SM circuit. However, this subject falls out of the scope of this paper.

VII. EXPERIMENTAL TESTS

The experimental tests were carried out to demonstrate dynamic and steady-state behavior of ISM-MMC, operating with newly proposed state observer-based interleaved legs current balancing control. The tests were executed on a laboratory prototype, the view of which is depicted in Fig. 12a with its circuital diagram in Fig. 12b. The laboratory ISM-MMC has a single-phase structure with two SMs per arm ($N = 2$) and three HB-legs per SM ($K = 3$). Each SM is entirely built by a three-leg converter with attached to it dc-link capacitor (C). Ac terminals of the three-leg converter are coupled with iron-core inductors (L). The second ports of these inductors are joined together, forming a positive terminal of an SM. The negative port is attached to the negative rail of the SM converter. The ISM-MMC operates as a rectifier, supplying power to an electronic load (i_{dc}). The ISM-MMC on its ac side is connected to a grid emulator that adjusts ac voltage to the required level and provides galvanic isolation from the grid. A controller for rapid prototyping RT Box 1 (Plexim) governs the power stage of the laboratory prototype. Measured currents and voltages enter the controller either as analog (marked in red, Fig. 12b) or as digital (marked in blue, Fig. 12b) input signals. In addition to the depicted in Fig. 12b analog measurements, the interleaved currents from SM2 (i_{21}, i_{22}, i_{23}) and SM3 (i_{31}, i_{32}, i_{33}) were sampled via RT
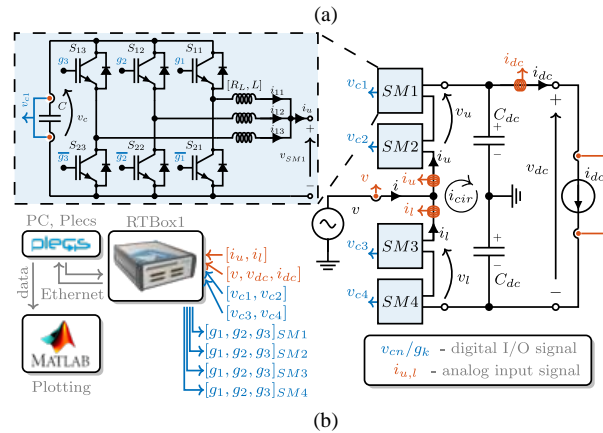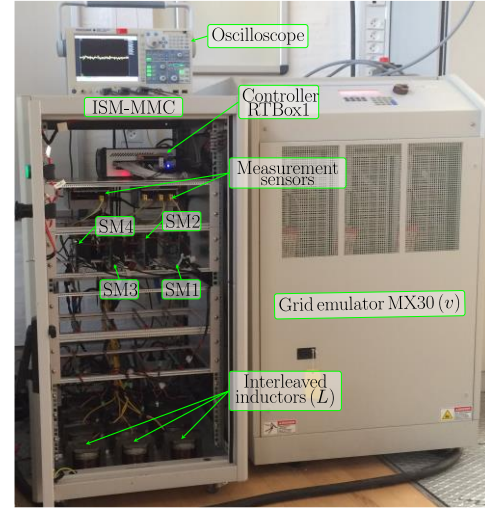

(a)

(b)

Fig. 12. View of the test setup (a) and its circuit diagram (b).

TABLE II
MAIN PARAMETERS OF THE LABORATORY TEST SYSTEM

Description	Labels	Parameters
number of SMs per arm	N	2
number of interleaved HB legs in each SM	K	3
individual interleaved leg inductor parameters	R_L, L	244 mΩ, 12.6 mH
capacitance in each SM	C	3.54 mF
dc-link split capacitance (2x)	C_{dc}	5.2 mF
rated line-to-neutral voltage (rms)	V	50 V
power factor	-	1
fundamental frequency	f	50 Hz
rated dc power and dc-link voltage	P_{dc}, V_{dc}	600 W, 200 V
carrier frequency	f_{cr}	2 kHz
sorting frequency	f_{sort}	400 Hz
observer current and voltage gains	l_i, l_v	10 H^{-1}, 20000 s^{-1}

Box 1 (are not depicted in Fig. 12b) for comparison with estimated values that are used in the new control strategy. The digital outputs of RT Box 1 provide drive circuits of power switches with PWM signals. Optical fibers are used to isolate both digital I/O of the controller from the power stage. Analog ports have galvanic isolation as well. Here again switching frequency was selected slightly elevated to reduce ripple in interleaved currents, make the current balancing more evident. RT Box 1 has a high-speed Ethernet connection with PC for real-time targeting via the PLECS (Plexim) model and data acquisition. The maximum sampling period of the controller is set to 20 μs. The stored data points later have been plotted via Matlab (MathWorks). Table II provides a summary of the main parameters of the laboratory setup.

The dc current step from 0 to 3 A has been introduced to the test ISM-MMC to demonstrate the dynamic performance of the implemented observer and associated with that interleaved current regulator. Based on the state observer, the discussed interleaved current balancing loops were always active during the conducted experiment. Fig. 13 and Fig. 14 depict the main input, output and internal characteristics of ISM-MMC, namely supplied ac power (active and reactive), ac phase current, dc-bus voltage, capacitor voltages, arm currents and individual currents of SM2 (cf. Fig. 12). It should be stressed here that the quantities presented by Fig. 13 and Fig. 14 are directly measured or derived by employing common calculus rules (Kirchhoff's current law, power calculation, etc.). It is well visible from these pictures that all quantities are well balanced and reach their steady-state value after some transient time that finishes around 2.5 s of the plot scale. The key point here to be checked is the distribution of interleaved currents within the SM (cf. Fig. 14a). In fact, they are nicely balanced, having a minor mismatch at the sinusoid peaks, provoked by circuital parameter inequality. However, as will be demonstrated shortly, the rms values of these currents are pretty close.

To visualize the dynamic behavior of the implemented state observer, measured interleaved currents from Fig. 14a are plotted versus their estimates (cf. Fig. 15a,c,e). The corresponding error distributions over the steady-state range (from 2.5 s to 4.5 s of the plot scale in Fig. 14a) are depicted in Fig. 15b,d,f. The normalization of the errors is done based on measured rms values of the corresponding interleaved currents (left-upper corner of the plots). It is noticeable from both time-series and error distribution plots that the estimates of all three interleaved currents fit quite well to the real waveforms with absolute error in the range ±20% of the measured currents rms, which is very close to the error range from performed simulations with random circuital parameters (cf. Fig. 9c,e,g). It is also visible that the errors fit quite well to Gaussian distribution. Nevertheless, even though the estimated
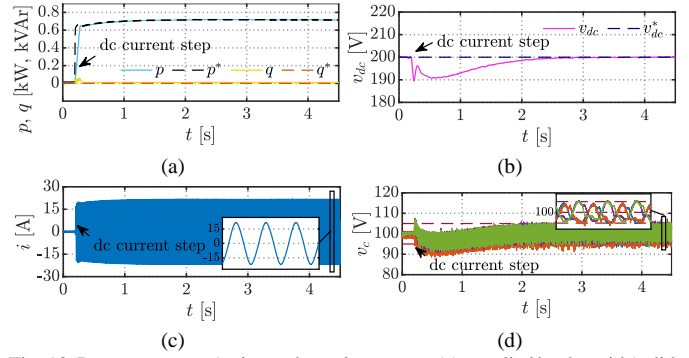

Fig. 13. Dc current step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines); dc-link voltage (b) – measured value (solid trace) and its reference (dashed trace); ac phase current (c); measured capacitor voltages (d) from each submodule of ISM-MMC (solid traces) along with its ±5% tolerance band and mean value (dashed lines).
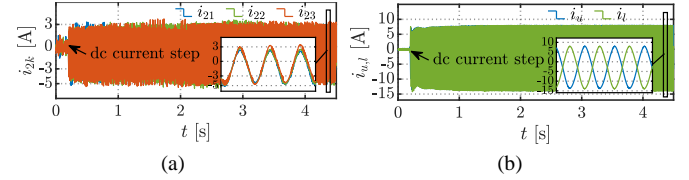

Fig. 14. Dc current step. Measured currents through interleaved legs of the submodule SM2 (a) and arm currents of ISM-MMC (b).
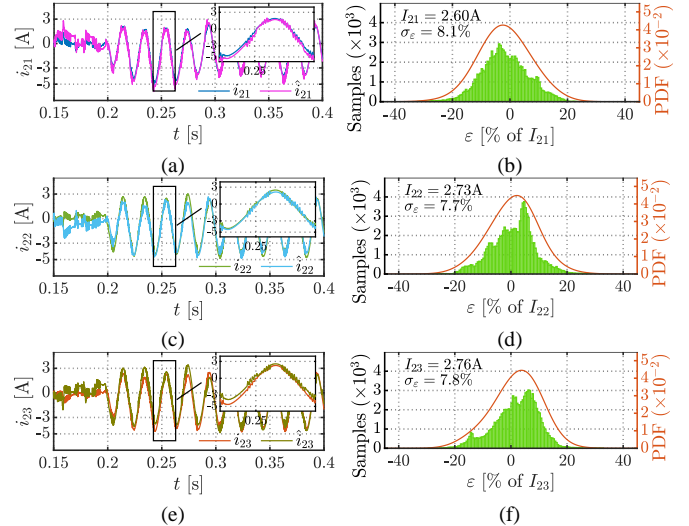

Fig. 15. Dc current step. Measured and estimated currents through interleaved legs of the submodule SM2 (a,c,e) with corresponding distribution of observation error (b,d,f).
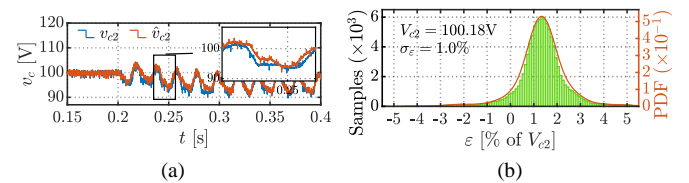

Fig. 16. Dc current step. Measured and estimated capacitor voltage of submodule SM2 (a) with corresponding distribution of observation error (b).

currents cannot repeat their measured counterpart, the fact that the interleaved currents are decently balanced in Fig. 14a proves the feasibility of the proposed state observer-based interleaved current regulator.

In addition to the current estimate, it is also essential to depict a similar comparison in the case of capacitor voltages (cf. Fig. 16) since the observer is built based on capacitor

voltage error. This fact is particularly evident when the ac phase current is zero (open-circuit case). At this operating point, the variation of capacitor voltage is minimal and interleaved currents almost purely consist of high (switching) frequency components. In such conditions, precisely estimating interleaved currents is very difficult.

Overall, the dynamic and steady-state behavior of the newly proposed sensorless interleaved currents balancing strategy is stable and predictable.

VIII. Conclusion

A current sharing problem in interleaved SMs of ISM-MMC originated from the upstream control actions is solved in this paper with new current sensorless method, by introducing a new state observer-based feedback control that operates individually with each SM. Such individual regulation ensures high dynamic response and control flexibility. Furthermore, a modified capacitor voltage balancing strategy has been proposed in this paper. The new method allows decoupling two balancing tasks in ISM-MMC converters, namely capacitor voltage and interleaved currents balancing, and it can be equally applied in classical MMC structures. The main benefit of the introduced capacitor balancing method is the possibility to directly operate with voltage references rather than with firing pulses, which provides greater flexibility in terms of control tasks arrangement.

Observers typically add complexity to the control system and demand high computational resources, especially in the highly modular structure of ISM-MMC. However, the implemented state observer employs only a few mathematical operations and can fit an entry-level controller. In addition to that, it requires only a few measured quantities, namely capacitor voltages and arm currents that are typically sensed in classical MMC structures for operation of internal control loops. Therefore, the proposed sensorless interleaved current balancing method does not need excessive and costly current measurements of each interleaved current. It can adequately share the arm current among interleaved legs of a SM, compensating the primary cause of the high current imbalance, namely actions of capacitor voltage balancing technique. Both numerical simulations and experimental tests verified the steady-state and dynamic performance of the introduced current balancing method. It has been shown thought that the implemented observer does not provide correct current estimations when the circuit parameters vary from their observer preset values. However, in a good converter design, the variance of the element parameters is limited; hence the observer-related estimation error is also limited. In this case, the potential current imbalance due to parameter variance can be effectively bounded. On the other hand, additional observer loops can be implemented trying to estimate the true value of the circuital parameters.

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