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Analysis, Modelling, and Simulation of Droop Control with Virtual Impedance Loop Applied to Parallel UPS Systems

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***Abstract*—This paper explores a control strategy for parallel uninterruptible power systems (UPS). The control technique used in that work was based on the droop control method. This method is usually applied to achieve good active and reactive power sharing when communication between the inverters is difficult due to its physical location. This paper has considered that the UPS systems there were no comunication between their controls. A detailed mathematical model about the explored system is shown in that work and simulation results are presented in order to prove the theory presented.**

***Index Terms*—Uninterruptible power systems, droop control method, nonlinear loads.**

I. Introduction

Nowadays Uninterruptible Power Supplies (UPS) with parallel configuration are becoming increasingly common in the market [1]. This occurs in both high power UPS as well as in low-power systems. In paralleling operation, two or more UPSs are electrically connected to form a unified system with one output, which is not always necessarily installed in the same room or floor. In some cases is interesting to place the UPS next to the higher load to reduce costs, improve the power quality and reliability. Due to the higher distances involved in the interconnections in each UPS module is interesting to implement the parallel operation without control communication.

Droop Control, despite its capability of load sharing between UPSs without control communication, presents a major drawback that must be overcomed, that is its compromise between proper power sharing accuracy and good amplitude and frequency output voltage regulation [2]. Among the techniques to solve this problem many authors utilize an additional control loop designated as Virtual Impedance Loop. This works deals with the inherent problems of the Droop Control. Beyond the addition of another control loop, it will be used a different PID controller, which provides a faster and more reliable transient response, in comparison to the conventional controller.

The UPS output impedance, also called *Thévenin Impedance*, added to that represented by the cables results in the connection impedance between modules. The Thévenin impedance is a function of the output filter, considering its inductor, capacitor and their equivalent resistances, and of the output voltage regulator's parameters.

It will be shown that this output impedance, composed with the proposed controller, possesses highly resistive characteristics, due to the influence of the inductor equivalent series resistance. Therefore, with the objective of imposing the wanted line characteristics some authors adopt a bulky inductor externally to the inverter [3]-[7]. Another way to achieve this is to add a so-called *virtual impedance*, which will in computational load to the system, but will be a cheaper and lighter solution.

The simple insertion of an inductive behaviour will directly affect the output reactance value, hence increasing the THD of the system when supplying nonlinear loads [8]. To solve such problem, an instantaneous droop is inserted in the virtual impedance, letting the system present a more resistive behavior at higher frequencies.

II. Multiloop Control Analysis

In this Section will be presented the modeling of the control system used by inverters. The whole system contains three nested loops: the output voltage regulation loop, the virtual impedance loop and the droop control loop. A simplified block diagram of what is written is drawn in Fig. 1.

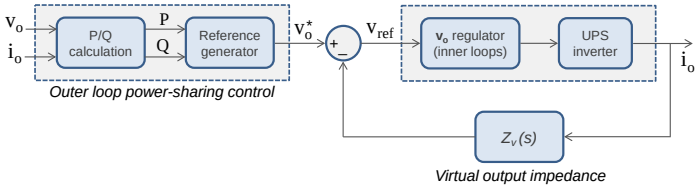


Fig. 1. Block diagram of the complete multiloop control scheme.

A. Voltage Regulation Loop

Instead of using a classical PID controller, the regulation is realized via a modified PID. The utility of this more complex controller is to provide a better and more reliable transient response to the system, in comparison to the classical one.

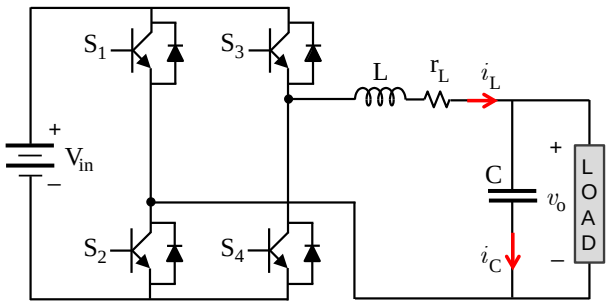


Fig. 2. Schematic diagram of the power inverter.

Figure 2 shows the power stage of a UPS inverter. From this it is possible to obtain the large-signal equations of corresponding to the inverter as following:

$$L\frac{di_L}{dt} = k \cdot V_{in} - v_o - r_L \cdot i_L \tag{1}$$

$$C\frac{dv_o}{dt} = i_c = i_L - i_o \tag{2}$$

where k varies according to the type of modulation used, for three-level, $k = \{-1, 0, 1\}$; for two-level, $k = \{-1, 1\}$.

Averaging both equations, we obtain

$$\begin{aligned} L \cdot C\frac{d^2\langle v_o\rangle}{dt} + r_L \cdot C\frac{\langle v_o\rangle}{dt} \quad + \\ + \langle v_o\rangle + L\frac{d\langle i_o\rangle}{dt} + r_L\langle i_o\rangle \quad = \quad \langle k \cdot V_{in}\rangle \end{aligned} \tag{3}$$

The controller presented in [9], showed in Fig. 3, gives the relation between the error $(v_{ref} - v_o)$ and the modulation signal

$$\begin{aligned} \langle k \cdot V_{in}\rangle \quad &= \quad v_{ref} + k_p(v_ref - \langle v_o\rangle) + \\ &+ \quad k_i \int (v_{ref} - \langle v_o\rangle) + k_d\frac{d}{dt}(v_{ref} - \langle v_o\rangle) \end{aligned} \tag{4}$$

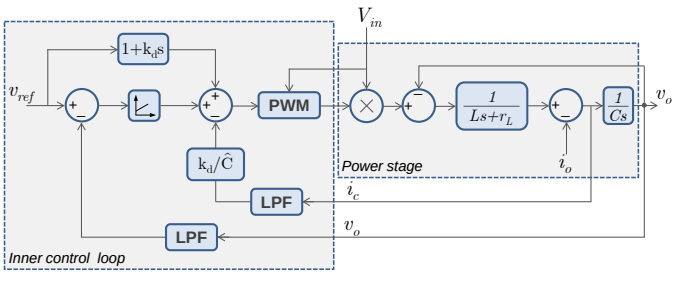


Fig. 3. Block diagram of the modified PID controller.

By using (3) and (4), we can obtain the closed-loop output voltage dynamic behavior, given by (5)

$$\begin{aligned} v_o = &\frac{k_d \cdot s^2 + (1 + k_p) \cdot s + k_i}{L \cdot C \cdot s^3 + (r_L \cdot C + k_d)s^2 + (1 + k_p)s + k_i} v_{ref} \\ &- \frac{L \cdot s^2 + r_L \cdot s}{L \cdot C \cdot s^3 + (r_L \cdot C + k_d)s^2 + (1 + k_p)s + k_i} i_o \end{aligned} \tag{5}$$

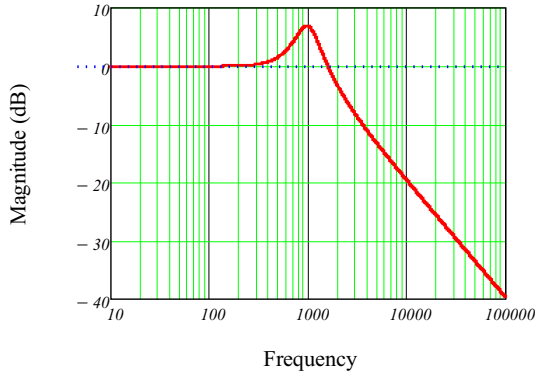
which can be expressed as a Thévenin circuit as follows:

$$v_o = G(s) \cdot v_{ref} - Z_o(s) \cdot i_o \tag{6}$$

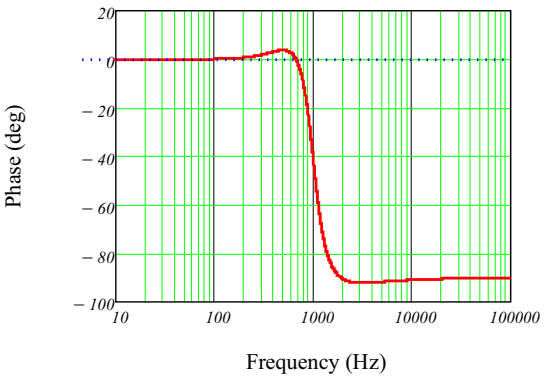
being $G(s)$ the tracking and $Z_o(s)$ the output impedance.

The Bode diagrams for $G(s)$ and $Z_o(s)$ are shown in Fig. 4(a) and 4(b).

The controller and power circuit parameters used were: $L = 1\ mH$, $C = 20\ \mu F$, $r_L = 200\ m\Omega$, $k_p = 0.04$, $k_i = 0.01$ and $k_d = 1.3 \cdot 10^{-5}$.



(a)

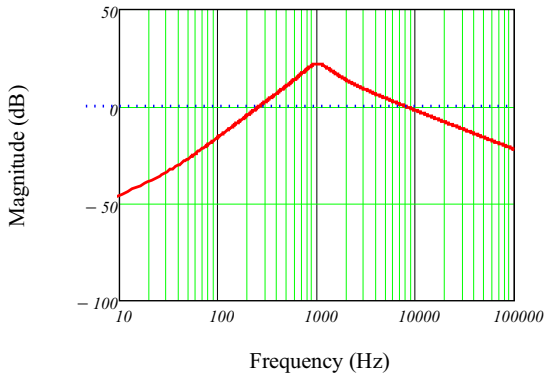


(b)

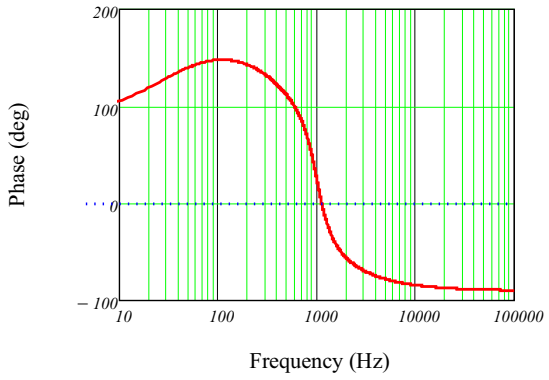
Fig. 4. $G(s)$ bode diagram: (a) Magnitude and (b) phase.

B. Virtual Impedance Loop

As the Bode diagram for $Z_o(s)$ demonstrates, the inductive behavior extends to frequencies higher than that of steady-state operation $(\approx 60Hz)$ and that jeopardizes a proper load sharing for nonlinear loads. To overcome that, an alteration was proposed for the output impedance. Instead of simply

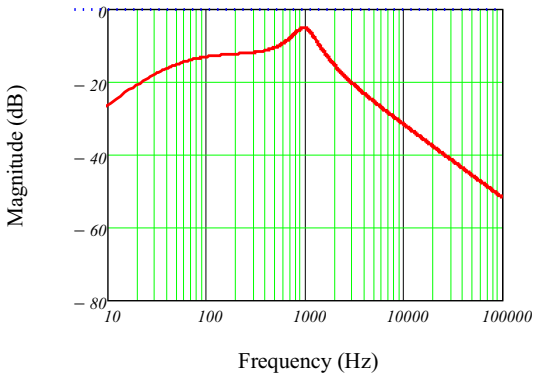


(a)

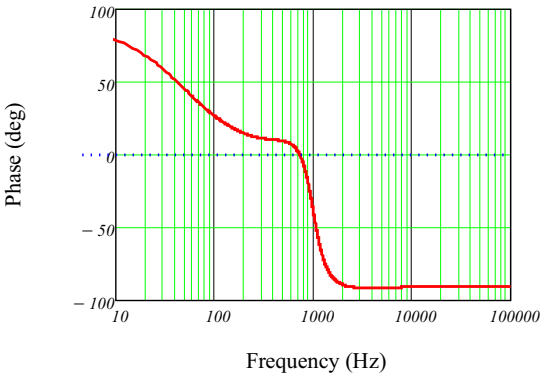


(b)

Fig. 5. $Z_o(s)$ bode diagram: (a) Magnitude and (b) phase.



(a)



(b)

Fig. 6. $Z_o(s)$ bode diagram: (a) Magnitude and (b) phase.

inserting a virtual inductor, the reference will be droop with the addition of a high-pass filter, as follows:

$$v_{ref} = v_o^* - L_v \frac{\omega_p \cdot s}{s + \omega_p} i_o \tag{7}$$

being L_v the virtual inductance value.

By using (6) and (7), we can get the closed loop output impedance.

$$Z_o(s) = \frac{A \cdot s^3 + B \cdot s^2 + C \cdot s}{D \cdot s^4 + E \cdot s^3 + F \cdot s^2 + G \cdot s + H} \tag{8}$$

Where

$$\begin{aligned} A &= \omega_p L_v k_d \\ B &= L + \omega_p L_v (1 + k_p) \\ C &= \omega_p L_v k_i + r_L \\ D &= LC \\ E &= r_L C + k_d + \omega_p LC \\ F &= 1 + k_p + \omega_p (r_L C + k_d) \\ G &= k_i + \omega_p (1 + k_p) \\ H &= \omega_p k_i \end{aligned} \tag{9}$$

The Bode plot corresponding to this new transfer function is depicted in Fig. 6.

It can be seen that a resistive is induced for higher harmonic frequencies ($100\ Hz < f < 1000\ Hz$), the high-pass filter has the following parameters: $L_v = 800 \cdot 10^{-6}\ [H]$ and $\omega_p = 2 \cdot \pi \cdot 50 = 314.159\ [rad/s]$

C. Droop Control Loop

The droop control originally is based on the power flow relations between voltage sources connected to a common bus. If the line connecting both is mainly inductive, then active and reactive power are described as:

$$P = \frac{EV}{X} \sin \phi \tag{10}$$

$$Q = \frac{EV \cos \phi - V^2}{X} \tag{11}$$

where E is the voltage source amplitude, V the bus voltage, X the line reactance, P and Q active and reactive powers, respectively.

The classical droop states that since P is mostly dependent of the power angle ϕ, and Q of the amplitude E, they can be controlled in a closed-loop fashion by the following droop controllers:

$$\omega = \omega^* - mP \tag{12}$$

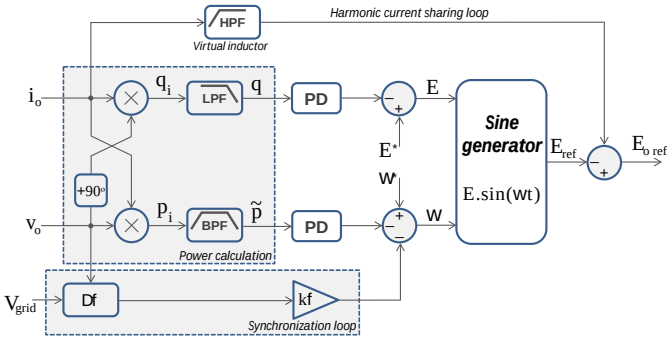


Fig. 7. Block diagram of the droop control loop.

$$E = E^* - nQ \tag{13}$$

being m and n the droop coefficients.

The manner the droop control is realized in this Section is shown the block diagram of Fig. 7. The active and reactive power are calculated measuring the output voltage and current. A delay of a quarter of the frequency applied to either current or voltage allows de separation of both powers. As it can be seen, the droop relation are not any more just an adjust with the proportional term applied to the average power.

The proposed adaptations to make the droop have a faster transient response is described in the equations below, were the classical droop suffers some alterations.

$$\omega = \omega^* - m\tilde{P} - m_d\frac{d\tilde{P}}{dt} \tag{14}$$

$$E = E^* - nQ - n_d\frac{dQ}{dt} \tag{15}$$

where:

$$\tilde{P} = \frac{\tau^{-1}s}{(s+\tau^{-1})(s+\omega_c)}P \tag{16}$$

The derivative terms are included to achieve faster transient response.

III. Droop Control: Small-Signal Analysis

In order to evaluate stability and transient response of the method above described, a small-signal analysis becomes necessary [5]. Taking equations (10) and (11) perturbing them around a steady-state operating point, and adding the averaging filters.

By defining $\lambda(\Phi)$ as

$$\lambda(\Phi) = \sin\Phi\cdot\hat{e} + E\cdot\cos\Phi\cdot\hat{\phi} \tag{17}$$

We can rewrite

$$\hat{\tilde{p}} = \frac{\tau^{-1}\cdot s}{(s+\tau^{-1})(s+\omega_c)}\cdot\frac{V}{X}\cdot\lambda(\Phi) \tag{18}$$

$$\hat{q} = \frac{\omega_c}{s+\omega_c}\cdot\frac{V}{X}\cdot\lambda(\Phi) \tag{19}$$

From the droop equation developed in (14) and (15) phase and voltage dynamics are described as:

$$\hat{\phi} = -\left(\frac{m_p}{s}+m_d\right)\cdot\hat{\tilde{p}} \tag{20}$$

$$\hat{e} = -\left(n_p + n_d\cdot s\right)\cdot\hat{q} \tag{21}$$

By inserting (18) and (19) in to (20) and (21), results:

$$\hat{\phi} = -\left(\frac{m_p}{s}+m_d\right)\cdot\frac{\tau^{-1}\cdot s}{(s+\tau^{-1})(s+\omega_c)}\cdot\frac{V}{X}\cdot\lambda(\Phi) \tag{22}$$

$$\hat{e} = -\left(n_p + n_d\cdot s\right)\cdot\frac{\omega_c}{s+\omega_c}\cdot\frac{V}{X}\cdot\lambda(\Phi) \tag{23}$$

By solving these two equations for one of the variables $\hat{\phi}$ or $\hat{e}$, the characteristic equation of the system can be obtained, thus making it possible to analyze the transient response of the closed-loop system, as well as its stability.

IV. Simulation Results

Simulations were developed in the software PSCAD/EMTC in order to validate the presented theory. It contains two $1kW$ Full-Bridge inverters with two-level modulation operating at a $20kHz$ switching frequency and an output voltage of $220V$ rms. The results are presented for a $1kW$ load and for a $1kVA$ nonlinear load. Since for this moment the variables of most interest are the currents of each inverter and the circulating current between them. To provide a more realistic simulation results, impedances were inserted in the connecting the load to each inverters, one of value $Z_{L1} = 0.434 + j\cdot 4.8\cdot 10^{-3}\Omega$, corresponding to a length of $30m$ and the other of $Z_{L2} = 0.29 + j\cdot 3.2\cdot 10^{-3}\Omega$, with $20m$ length.

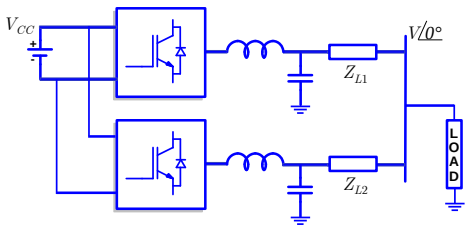


Fig. 8. Simulated system.

1) Linear Load: Steady State Analysis: To analyze the current sharing, Figure 9 shows the behavior of each of the interest waveforms: current from inverter #1 (red), inverter #2 (blue), load current (black) and circulating current (green).

Figure 10 shows the steady-state behavior of the output voltage of inverter #1 and Fig. 11 shows the voltage difference between both inverters.

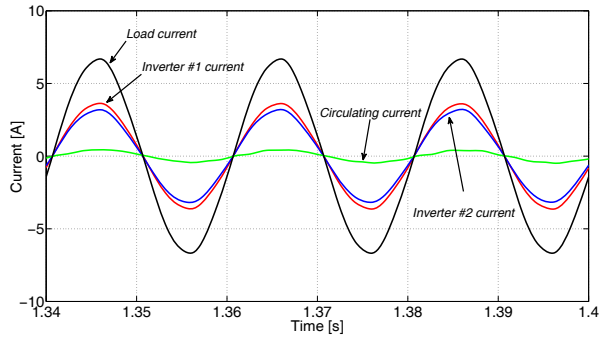


Fig. 9. Details for inverter #1 and #2 output currents, circulating current ($i_c = i_1 - i_2$) and load current.

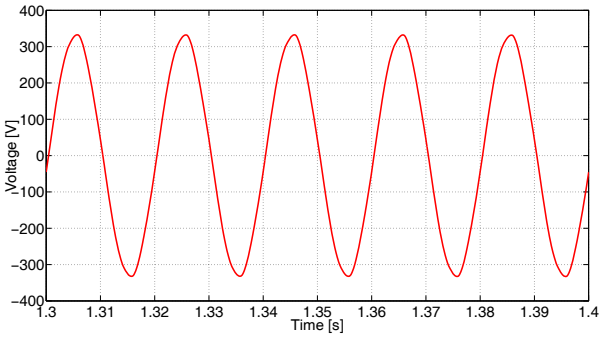


Fig. 10. Linear Load: Inverter #1 output voltage.

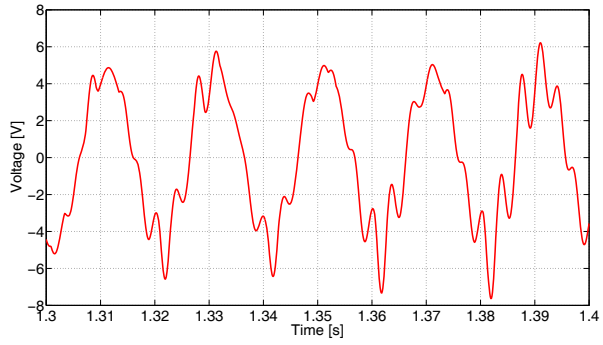


Fig. 11. Linear Load: Difference between the output voltages of the inverters #1 and #2.

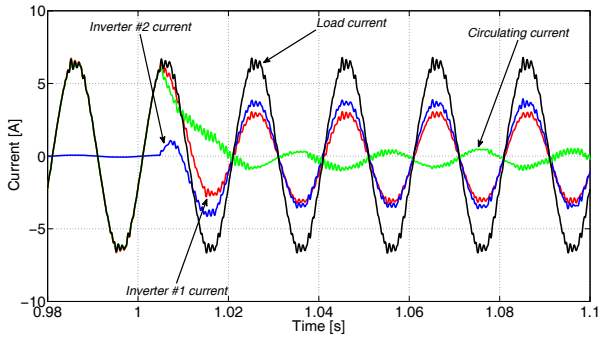


Fig. 12. Load Step Change: Details for inverter #1 and #2 output currents, circulating current and load current.

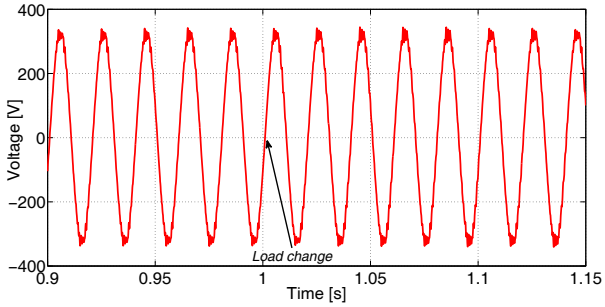


Fig. 13. Load Step: Inverter #1 output voltage.

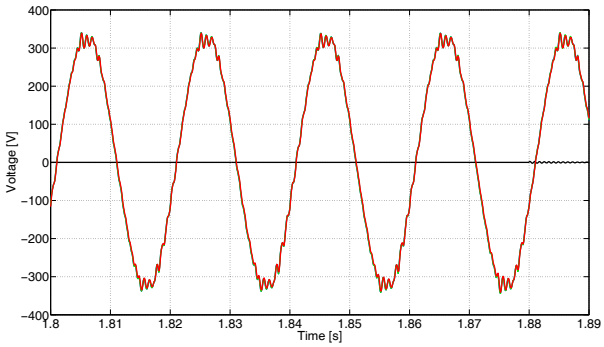


Fig. 14. Output voltages of the inverters placed at the same distance to the load.

2) Linear Load Transient Analysis: The load is now being supplied only by inverter #1 and, at $t = 1\,s$ inverter #2 is connected to the bus in order to coordinate the transient behavior of the system. Fig. 12 shows the transient response after the connection of inverter #2, the circulating current and inverter #1 current are behind the load voltage.

Figure 13 shows that, even for load changes the two inverters both present the same voltage waveforms.

3) Linear Load Inverters at the same distance to the load: This section shows results in the particular case that the two presented inverters present the same distance to the load ($30m$).

Even though the voltages and currents form each inverter are represented by different colours in the simulation results, those can not be seen, since they are superposed. The lines drawn in black in Fig. 14 and Fig. 15 are the voltage and current difference, respectively, which are zero.

4) Nonlinear Load: The next results were realized with a load $1000\ VA$ load, which consisted of a diode-bridge, a bulky capacitor of $1.15\ mF$, in parallel with a resistance of $108.75\ \Omega$ according to the IEC 62040-3 standard. In Fig. 16 and Fig. 17, inverter #2 are connected to the load at the same time $t = 1\ s$, so both steady-state and transient can be seen in each frame.

For a nonlinear load the output voltage, shown in Fig. 17, did not present a perfect sinusoidal behavior, which is explained because of the lack of a optimized design for such a kind of load. Naturally this unwanted waveform is something

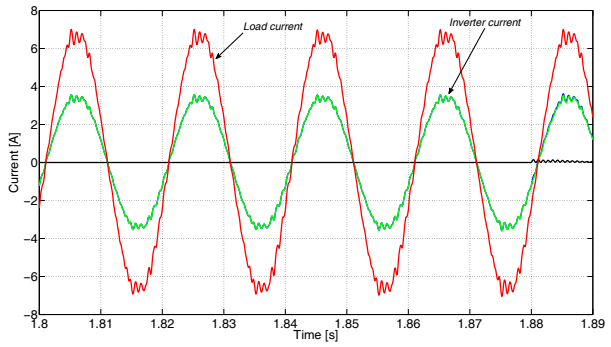


Fig. 15. Output currents of the inverters (green) placed at the same distance to the load. Load current in red.

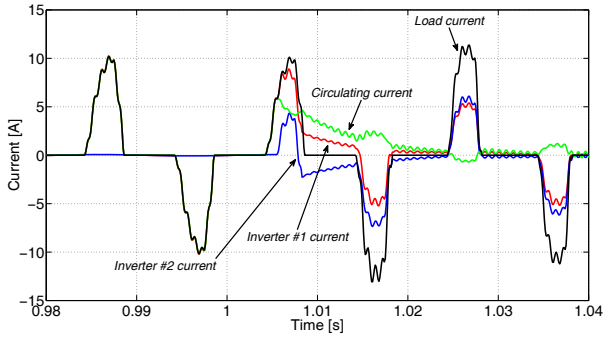


Fig. 16. Nonlinear load: Details for inverter #1 and #2 output currents, circulating current and load current.

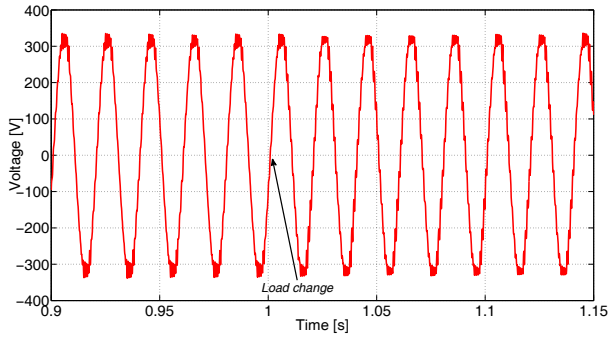


Fig. 17. Nonlinear Load: Inverter #1 output voltage.

that can be fixed further.

5) Nonlinear Load - Inverters placed at the same distance to the load: Figures 18 and 19 show the voltage and current behaviors for the UPS systems feeding nonlinear load when the inverters are at the same distance to the load.

V. Conclusion

As demonstrated, the presented control technique may be applied successfully for parallel operation of voltage source inverters. Even possessing a complicated set of control loops, the sharing accuracy and transient response showed to be valid, the proposed model will allow further improvement in the design of the control loops.

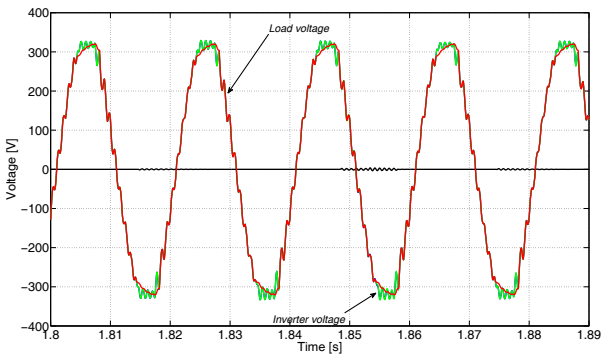


Fig. 18. Output voltages of the inverters (green) placed at the same distance to the load. Load voltage in red.

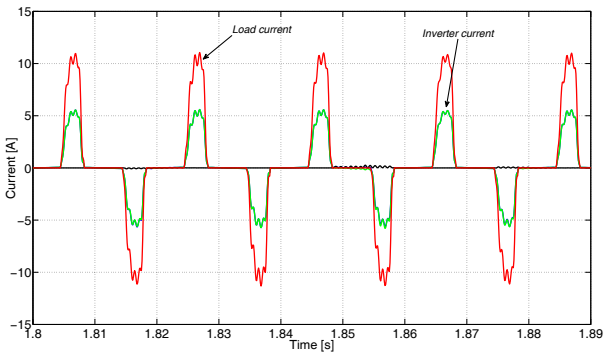


Fig. 19. Output currents of the inverters (green) placed at the same distance to the load. Load current in red.

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