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Reliability-Cost Models for the Power Switching Devices of Wind Power Converters

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***Abstract*- In order to satisfy the growing reliability requirements for the wind power converters with more cost-effective solution, the target of this paper is to establish a new reliability-cost model which can connect the relationship between reliability performances and corresponding semiconductor cost for power switching devices. First the conduction loss, switching loss as well as thermal impedance models of power switching devices (IGBT module) are related to the semiconductor chip number information respectively. Afterwards simplified analytical solutions, which can directly extract the junction temperature mean value T_m and fluctuation amplitude ΔT_j of power devices, are presented. With the proposed reliability-cost model, it is possible to enable future reliability-oriented design of the power switching devices for wind power converters, and also an evaluation benchmark for different wind power converter configurations is opened.**

I. INTRODUCTION

The wind energy production integrated into the power grid is booming up all over the world. Meanwhile, also the power capacity of a single wind turbine is increasing continuously to reduce the price pr. produced kWh. Due to much more significant impacts to the power grid than ever before, the wind power generation system is required to be more reliable and meanwhile cost-effective. According to the field feedbacks from the operating wind turbines in the past few decades [1], the electrical parts (or the power electronics converters) of wind turbines tend to be easier to fail, as a result, the reliability evaluation and improvements for the power switching devices, which are the key components of the electrical part of the wind turbines, should be specially focused.

In a traditional wind power converter design process, the power switching device ratings are normally decided based on the potential current/voltage stresses, and some rating margins may be reserved to ensure certain reliability requirements. However, it is found that the loading distribution of power devices may be quite unequal under various converter topologies as well as operation conditions [2]-[5]. With this traditional "rating-oriented" design process, it may easily lead to capacity waste of some less loaded devices. Therefore, more advanced models for wind power converter design are needed in order to satisfy the growing reliability requirements together with the most cost-effective solutions.

If the relationship between the reliability and corresponding cost of power semiconductor for a wind power converter is related, as indicated in the curve of Fig. 1, the "just-right" device cost/ratings can be determined according to the specific reliability requirements by the mission profile. With this reliability-cost model and the "reliability-oriented" design process, it is possible to enable more accurate and cost-effective design for the wind power converter achieving the target reliability requirements.

With the reliability-cost performances profiles, it is also possible to unify and compare different converter solutions in a more sensible way, as demonstrated in Fig. 2. (i.e. converter solutions with different topologies, voltage ratings, switching frequencies, etc. for a given mission profile). Therefore, a new reliability-cost evaluation benchmark for wind power

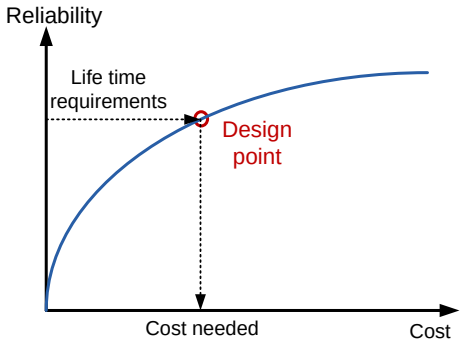


Fig. 1. Reliability-Cost profile of a converter.

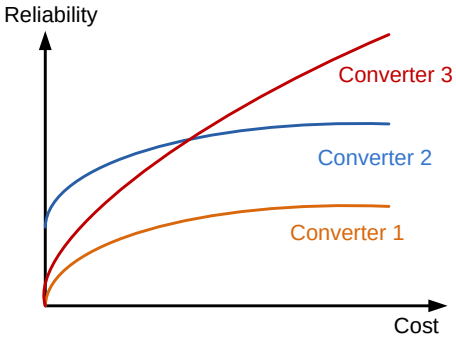


Fig. 2. Reliability-Cost profile comparison of different converter solutions.

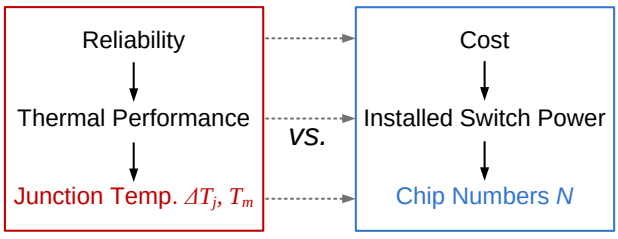


Fig. 3. Quantification of reliability and cost performances.

converters can be established and help to guide the selection of various converter solutions.

As a result, this paper will focus on the development of such models which can relate the reliability and cost of power switching devices for wind power converters, it is different from the system level reliability-cost analysis in [6]. In order to easier quantify the reliability and cost performances, as shown in Fig. 3, the reliability is represented by the power device junction temperature mean value T_m and fluctuation ΔT_j according to the manufacturer's life time models for power semiconductors [7]-[11]. The cost is represented by the used chip or cell numbers N in IGBT/ Diode modules according to the dominant packaging structure by IGBT manufacturers [12], [13]. Consequently, the relationship between the reliability and cost of converters is transferred to the relationship between junction temperature and chip numbers of power switching devices.

According to the widely used loss and thermal models for power switching devices in [8], [14]-[16] the junction temperature is generated by applying the losses to the thermal impedance. Therefore, the key method to relate the junction temperature and chip numbers of power devices is to include the chip number information into the loss model as well as the thermal impedance model respectively.

II. Loss Model with Chip Number Information

In most of the cases a series of IGBT modules at certain voltage rating is composed of different amount of IGBT and diode dies/chips/cells, which are paralleled together in order to achieve various current ratings. The datasheets of the IGBT modules as well as the used chips are available e.g. on the website of semiconductor manufacturers [17], from which the 4.5 kV series IGBT modules which consist of different numbers of IGBT chips (4.5 kV/55 A) and freewheeling diode chips (4.5kV/110A) are chosen as an example in this paper [15]. The current ratings of these series IGBT modules range from 150 A to 1200 A. A grid-side 10 MW three-level Neutral-Point-Clamped (3L-NPC) wind power converter is chosen and designed as a case study in this paper, as shown in Fig. 4, the detailed converter parameters are shown in Table I [2]-[4].

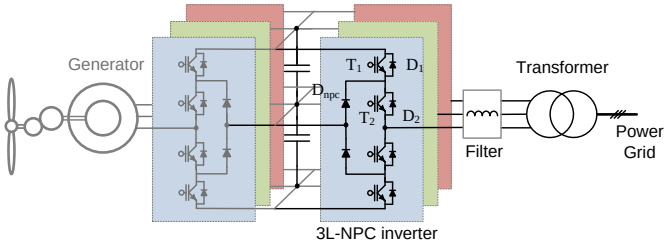


Fig. 4. Three-level neutral point clamped converter used in a wind turbine.

Table I. Parameters of a 10 MW 3L-NPC wind power converter shown in Fig. 10.

Rated output active power P_o	10 *MW*
DC bus voltage V_{dc}	5.6 *kV DC*
*Rated primary side voltage V_p	3.3 *kV rms*
Rated line-to-line grid voltage V_g	20 *kV rms*
Rated phase current I_{phase}	1750 *A rms*
Carrier frequency f_c	800 *Hz*
Filter inductance L_f	1.13 *mH* (0.2 *p.u.*)

* Line-to-line voltage in the primary windings of transformer.

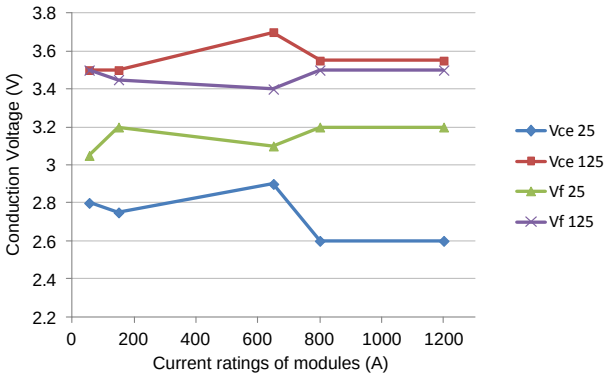


Fig. 5. Rated conduction voltage for a series of 4.5 kV IGBT modules of a manufacturer.

Table II. Calculated chips numbers for different current ratings IGBT modules (4.5 kV series).

Module ratings (A)	150	650	800	1200
IGBT chip numbers	3	11	15	22
Diode chip numbers	1	6	7	11

A. *Chip number extraction from IGBT modules.*

Unlike the switching behavior, the conduction voltage of both IGBT and diode is a relative "clean" characteristic which only depends on the junction temperature at the suggested gate drive voltage, while the switching characteristic depends not only on the junction temperature, but also on drive resistance, commutated voltage, *di/dt*, line inductance, etc [12]. Normally, the used chip numbers of an IGBT module is not provided by the manufacturer in the datasheet, however it is possible to calculate the chip numbers *N* according to the module's conduction voltage at a certain load current I_{load}.

If the load current is equally distributed in each IGBT/diode chip, the total conduction voltage with *N* paralleled chips at the load current of I_{load} should be equal to the conduction voltage of a single IGBT/Diode chip at the load current of I_{load}/N, this relationship can be written as:

$$v_{ce/N}(I_{load}) = v_{ce/1}(\frac{I_{load}}{N}) \quad (1)$$

where the $v_{ce/N}$ is the conduction voltage of *N* parallel IGBT chips and $v_{ce/1}$ is the conduction voltage of a single IGBT chip, which can be written as:

$$v_{ce/1}(\frac{i_{load}(t)}{N}) = V_{ce0/1} + r_{ce/1} \cdot (\frac{i_{load}(t)}{N})^{A_{ce/1}} \quad (2)$$

The $V_{ce0/1}$, $r_{ce/1}$ and $A_{ce/1}$ are the fitting parameters of V_{ce}-I_c relationship curve for a single IGBT chip [13], which can be found in the datasheets of manufacturer.

Put (2) into (1) the chip numbers inside an IGBT module can be calculated as:

$$N = I_{load} / \left(\frac{v_{ce/N}(I_{load}) - V_{ce0/1}}{r_{ce/1}} \right)^{1/A_{ce/1}} \quad (3)$$

Fig. 5 shows the rated conduction voltage for 4.5 kV series IGBT modules at various current ratings, where the conduction voltage of both IGBT v_{ce} and freewheeling diode v_f at junction temperature of 25 and 125 ℃ are indicated respectively. When using this information to equation (3), the used chip numbers of these modules can be calculated, and the results are indicated in Table II.

B. Conduction loss model with chip number information.

With the chip numbers in Table I, it is possible to acquire the conduction voltage characteristic for a single chip inside the IGBT modules with different current ratings. Fig. 6 and Fig. 7 show the conduction voltage-load current of a single IGBT and freewheeling diode chip in different rating modules listed in Table I. It can be seen that the conduction voltage characteristic of a single IGBT or Diode chip inside different current rating modules are quite consistent with each other.

Therefore, the instantaneous conduction loss of N chips paralleled IGBT module $P_{cond/N}$ can simply be expressed as the sum of conduction loss for each single chip $P_{cond/1}$:

$$\begin{aligned} P_{cond/N}(N,t) &= N \cdot P_{cond/1}(N,t) \\ &= N \cdot \left[v_{ce/1}\left(\frac{i_{load}(t)}{N}\right) \cdot \frac{i_{load}(t)}{N} \cdot d(t) \right] \\ &= v_{ce/1}\left(\frac{i_{load}(t)}{N}\right) \cdot i_{load}(t) \cdot d(t) \end{aligned} \quad (4)$$

Where $i_{load}(t)$ is the load current, $d(t)$ is the duty ratio of the IGBT module.

The average mean conduction loss of N chips paralleled in an IGBT Module $P_{CONDavg/N}$ can be expressed as:

$$P_{CONDavg/N}(N) = f_o \int_0^{1/f_o} P_{cond/N}(N,t)\, dt \quad (5)$$

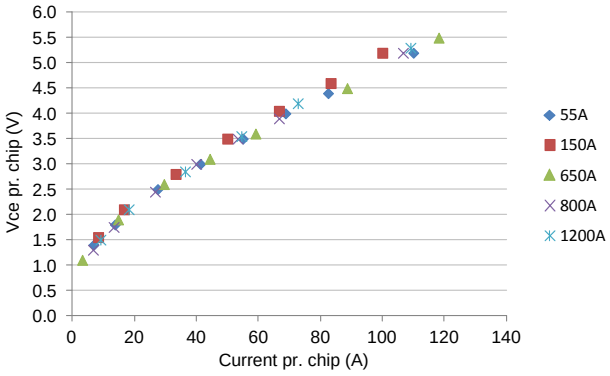


Fig. 6. Conduction voltage V_{ce} vs. load current I_c for a single IGBT chip in different modules (125℃)

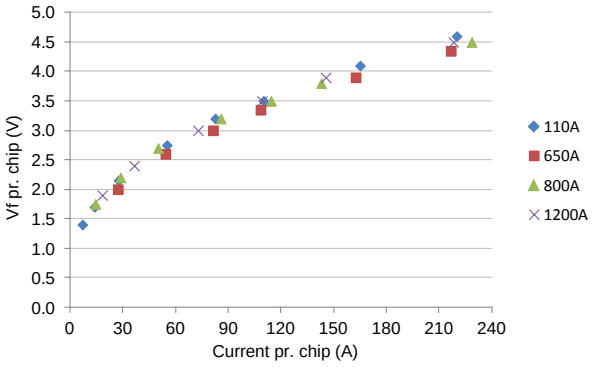
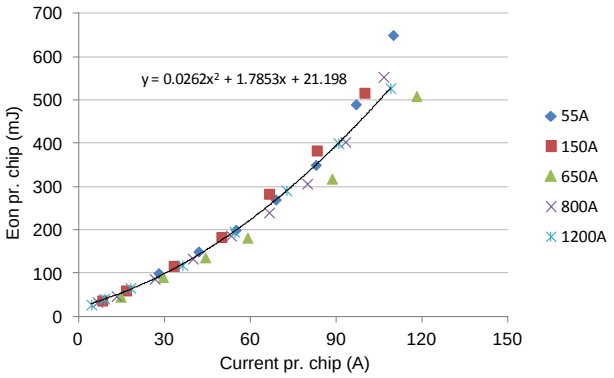
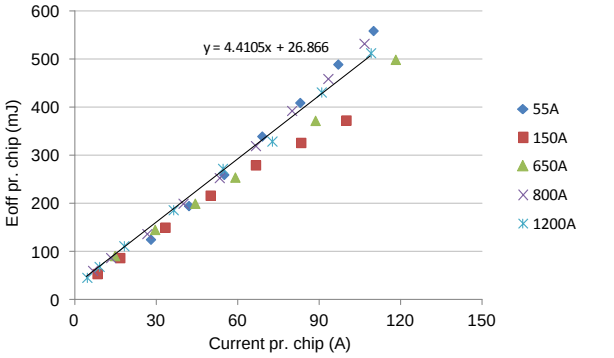


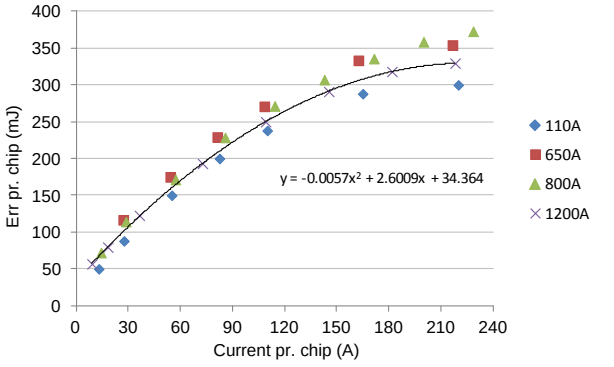
Fig. 7. Conduction voltage V_F vs. load current I_F for a single freewheeling diode chip in different modules (125℃)



(a) E_{on} vs. I_c pr. chip (125℃)

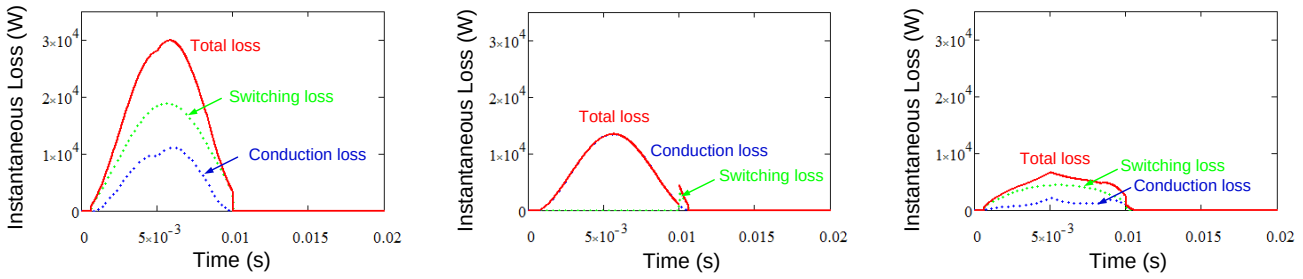


(b) E_{off} vs. I_c pr. chip (125℃)



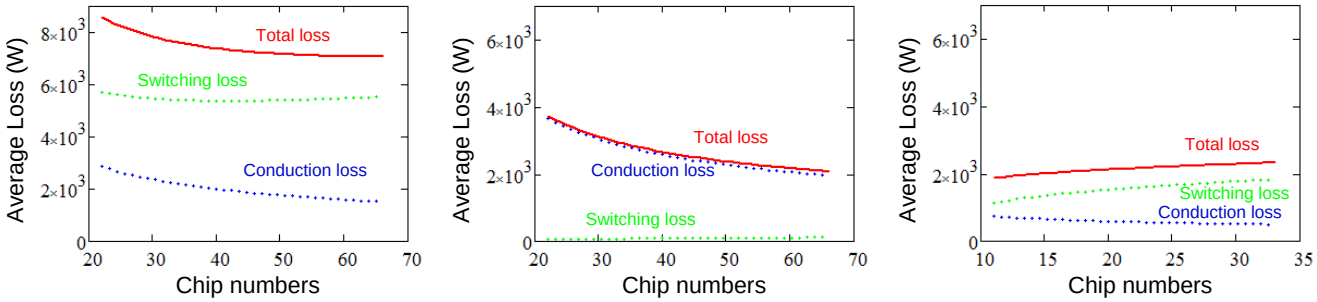
(c) Err vs. Ic pr. chip (125℃)

Fig. 8. Switching loss pr. chip vs. load current I_c for different current rating IGBT modules (4.5 kV series).



(a) T1 (b) T2 (c) Dnpc

Fig. 9. Instantaneous loss of switching devices for three-level Neutral Point Clamped grid inverter (normal operation, N=22, f_s=800 Hz. PF=1, P_o=10 MW, red line total loss, blue line conduction loss, green line switching loss).



(a) T1 (b) T2 (c) Dnpc

Fig. 10. Average loss vs. chip numbers of switching device for three-level Neutral Point Clamped grid inverter (normal operation, f_s=800 Hz. PF=1, P_o=10 MW, red line total loss, blue line conduction loss, green line switching loss).

C. *Switching loss model with chip number information.*

As mentioned before, the switching loss characteristic of power devices depends on many factors, such as the drive resistance, *di/dt*, line inductance, etc. These factors are sensitive to the operating conditions and can be easily deviated when different numbers of chips are packaged. Therefore it is inaccurate to calculate the switching loss of N chips paralleled IGBT module by simply summing up the switching loss of each single chip.

The solution is to investigate the switching loss characteristic pr. chip inside various current rating IGBT modules, and then an average Loss-Current curve is chosen to be summed up to get the total switching loss of N paralleled chips. With the information of chip numbers in Table I, the switching loss characteristic pr. chip inside various current rating modules are plotted in Fig. 8. It can be seen that the switching loss characteristic pr. chip of different rating modules slightly deviates from each other. An average curve is chosen and fitted with two order functions as indicated in Fig. 8.

With the fitting function for the average switching loss characteristic pr. chip, the instantaneous switching loss of N chips paralleled IGBT module can be calculated as:

$$P_{sw/N}(N,t) = N \cdot P_{sw/avg1}(N,t)$$
$$= N \cdot \left[S_{1/avg1} \cdot \left(\frac{|i_{load}(t)|}{N}\right)^2 + S_{2/avg1} \cdot \frac{|i_{load}(t)|}{N} + S_{3/avg1} \right] \quad (6)$$

Where $S_{1/avg1}$, $S_{2/avg1}$, $S_{3/avg1}$ are the fitting parameters for average switching loss characteristic pr. chip, as indicated in Fig. 8. The average mean switching loss of N chips paralleled IGBT module $P_{SWavg/N}$ with chip number information can be calculated as:

$$P_{SWavg/N}(N) = f_o \int_0^{1/f_o} P_{sw/N}(N,t)\, dt \quad (7)$$

D. *Loss calculation results.*

The instantaneous loss of the most stressed switching devices for the 3L-NPC grid side inverter under rated condition are shown in Fig. 9, where the chip number N is 22 and switching frequency is 800 Hz. The average losses of the most stressed switching devices with relation to the chip numbers are shown in Fig. 10.

III. THERMAL IMPEDANCE MODEL WITH CHIP NUMBER INFORMATION

According to the datasheets of IGBT modules, the thermal impedance is modeled as three layers Foster RC network inside the modules (from junction to case $Z_{thJ\text{-}C}$), and a thermal resistance outside the modules (from case to heat sink $R_{thC\text{-}H}$), as indicated in Fig. 11. The thermal impedance model with chip number information can be acquired by fitting function of the thermal parameters provided by datasheets of various current rating of IGBT modules.

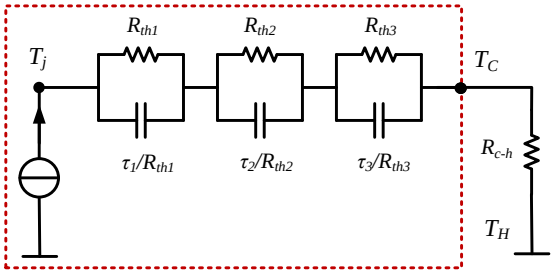
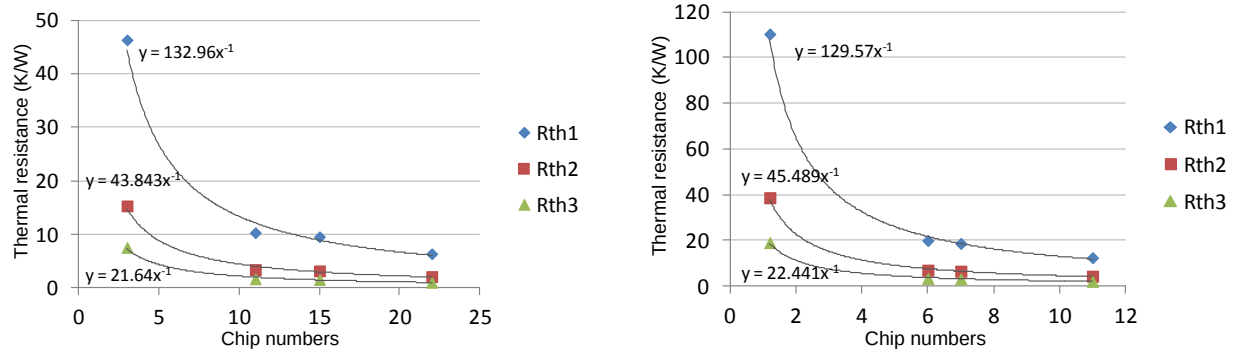


Fig. 11. Thermal impedance model for ABB 4.5 kV series IGBT modules, different chip numbers have different parameters in R_{th} and τ.

The thermal resistances R_{th1}, R_{th2}, R_{th3} in Fig. 11 of various rating IGBT modules with relation to the calculated chip numbers can be plotted in Fig. 12 [17], where the fitting function is also indicated. It can be seen that the thermal resistances R_{th1}-R_{th3} of both IGBT and diode inside the IGBT modules are inverse proportional to the chip number N, which is consistent with the thermal resistance physical model [16]:

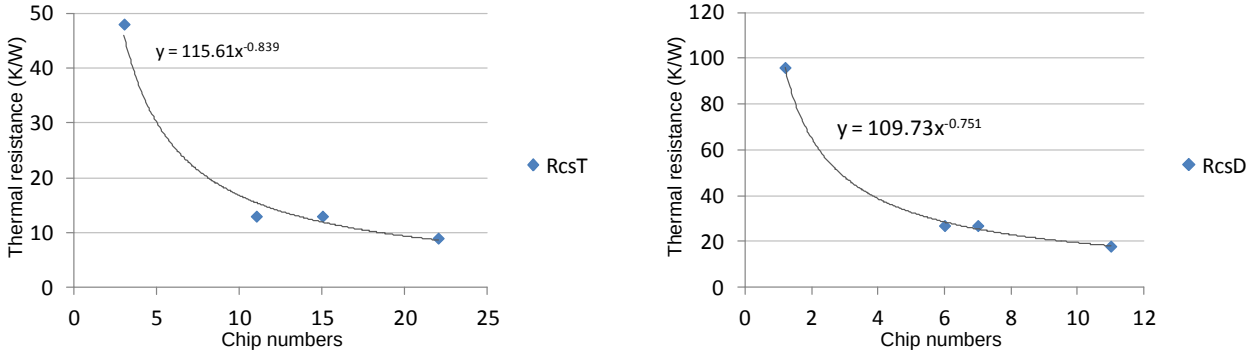
$$R_{th}(N) = \frac{d}{\lambda \cdot A \cdot N} = M_{Rth} \cdot N^{-1} \tag{8}$$

Where N is the number of chips, A is the physical area pr. chip, d is the thickness of material, λ is the thermal conductivity constant (W/m*K), M_{rth} is a fitting parameter.



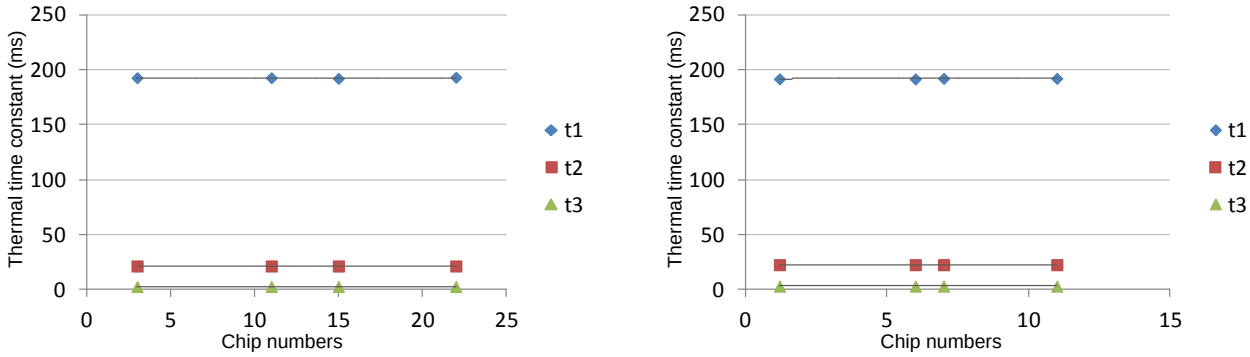
(a) IGBT (b) Diode

Fig. 12. $R_{thJ\text{-}C}$ inside the modules (Junction to Case) vs. Numbers of chips.



(a) IGBT (b) Diode

Fig. 13. $R_{thC\text{-}H}$ outside the modules (Case to Heat sink) vs. Numbers of chips.



(a) IGBT (b) Diode

Fig. 14. Time constants t_1-t_3 in Fig. 11 (Junction to Case) vs. Numbers of chips (t_x=R_{thx}*C_{thx}).

In respect to the thermal resistance from case to heat sink $R_{thC\text{-}H}$ (outside the module), it is more related to the base plate size of module case as well as packaging technology, therefore $R_{thC\text{-}H}$ is no longer inverse proportional to the chip numbers N, as plotted and fitted in Fig. 13.

The time constant of the thermal impedance in Fig. 11 (τ_1-τ_3) with relation to the chip numbers of IGBT modules are plotted in Fig. 14. It can be seen that the time constants of the thermal impedance inside the IGBT modules are kept constant with different chip numbers, this characteristic is consistent with the time constant physical model, which is represented as [16]:

$$\tau = R_{th} \cdot C_{th} = \frac{c \cdot \rho}{\lambda} \cdot d^2 \tag{9}$$

Where the thermal capacitance C_{th} can be represented as:

$$C_{th}(N) = c \cdot \rho \cdot A \cdot d \cdot N \tag{10}$$

The c is the factor proportional to heat in (Ws/g*K), ρ is the density of materials (g/cm^3). In the time constant function (9) it can be seen that there is no item for the chip numbers N, that means the time constant of thermal impedance is only related to the thickness of the chips, which should not be deviated in various current ratings IGBT modules.

In a summary the thermal impedance model with the chip number information for both IGBT and diode of IGBT modules can be written as:

$$Z_{th}(N,t) = N^{-1} \cdot \sum_{x=1}^{3} M_{Rthx} \cdot (1 - e^{-t/\tau_x}) \tag{11}$$

IV. Analytical Solution of Junction Temperature with Chip Number Information

With the instantaneous loss model (4), (6) and thermal impedance model (11) (in which the chip number information is both included), it is possible to calculate the instantaneous junction temperature of switching devices by convoluting the loss and thermal impedance models as:

$$T_j(N,t) = T_c + \int_0^t \left[\frac{d}{dz} P_{loss/N}(N,z) \right] \cdot Z_{th}(N, t-z) dz \tag{12}$$

However, this calculation is complicated and time consuming. Actually only the temperature average mean value T_m and fluctuation amplitude ΔT_j are related to the life time of power devices by most of the reliability models for power semiconductors [7]-[11]. As a result, simplified junction temperature solutions, which can directly extract the information of T_m and ΔT_j have to be developed, and it is done in this paper.

A. Simplified solution for T_m

According to [16], the steady state junction temperature mean value T_m is only related to the total thermal resistance as well as the average loss dissipation in the power devices. The T_m can be written as follows, where the chip number information is included:

$$T_m(N) = T_{ref} + P_{avg/N}(N) \cdot \left(\sum_{x=1}^{3} R_{thx} + R_{thC-H} \right) \tag{13}$$

The calculated mean junction temperature T_m with relation to the chip numbers N is shown in Fig. 15, in which each switching device in a switching arm of 10 MW 3L-NPC wind power inverter are indicated as an example.

B. Simplified solution for ΔT_j

According to the instantaneous power loss dissipation, as shown in Fig. 8, the time domain of losses in the most stressed devices are more or less sinusoidal distributed within a half fundamental cycle. On this case it is not easy to acquire the fluctuation amplitude of junction temperature ΔT_j, because the exact time when the junction temperature achieves its maximum/minimum value is hard to be derived by (12).

One possible simplification is to use square wave loss pulses which share the same loss-time area as the original sinusoidal loss distribution within a half fundamental cycle. In this case the loss is more constant and the time when the junction temperature achieves its maximum value can be determined.

In Fig. 16 three kind of loss pulses (one step, two steps and three steps) which share the same loss-time area as the original sinusoidal-like losses are generated and applied to the same thermal impedance of IGBT module, the corresponding junction temperatures are also indicated. It can be seen that the two steps loss pulses can achieve an acceptable consistency of junction temperature fluctuation with the original loss distribution.

The more detailed two steps loss pulses and its resulting junction temperature are indicated in Fig. 17. It is relative easy to calculate the temperature fluctuation amplitude ΔT_j with the information of loss pulse amplitude and step time. The approximate function is shown as follows [18]:

$$\begin{aligned} \Delta T_j &= P_{avg} \cdot Z_{th}(t_2) + (3P_{avg} - P_{avg}) \cdot Z_{th}(t_2 - t_1) \\ &= P_{avg} \cdot Z_{th}\left(\frac{3}{8 f_o}\right) + 2P_{avg} \cdot Z_{th}\left(\frac{1}{4 f_o}\right) \end{aligned} \tag{14}$$

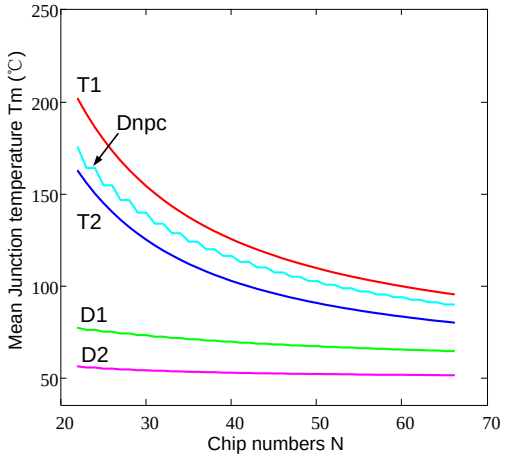


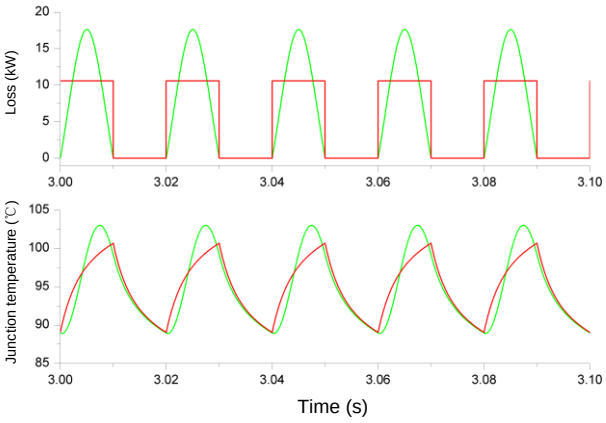
Fig. 15. Mean junction temperature T_m of each power device in 3L-NPC grid inverter vs. chip numbers. (Normal operation, P_o=10 MW, f_s=800 Hz, V_{ll}= 3.3 kVrms).

The calculated junction temperature fluctuation ΔT_j with relation to the chip numbers N is shown in Fig. 18, in which each switching device in a switching arm of 10 MW 3L-NPC inverter are indicated.

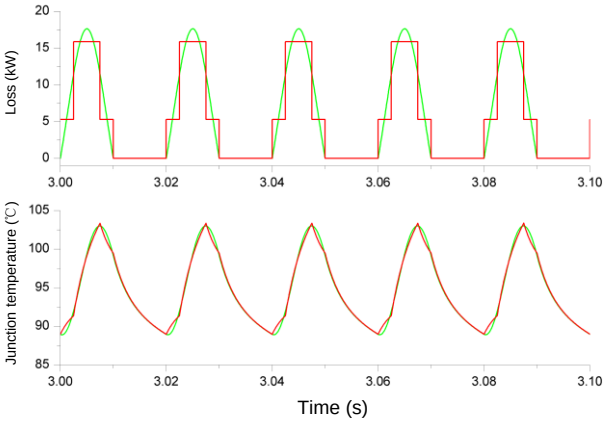
C. *Temperature-cost profile of 3L-NPC inverter*

With the relationship between junction temperature and corresponding chip numbers for each of the power switching devices in Fig. 15 and Fig. 18, the same junction temperature (maximum or fluctuation) for each of the switching device can be set by adjusting the chip numbers respectively. The characteristics of the junction temperature for all of the switching devices with relation to the needed total chip numbers for one phase of the given 10 MW three-level Neutral Point Clamped wind power inverter can be plotted in Fig. 19.

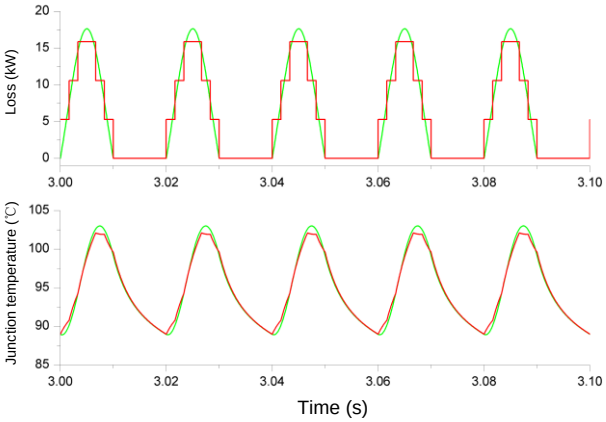
It can be seen that Fig. 19 is a unique performance profile of a given converter solution (topology, voltage rating, etc), therefore it is possible to unify and compare different converter solutions with this profile in a more sensible way. Because the junction temperature is close related to the lifetime of power switching devices according to [7], and the chip numbers will decide the current rating and packaging of IGBT modules, the connection between reliability and cost of the power devices for a certain converter solution is thereby established.



(a) One step loss pulses approximation.



(a) Two step loss pulses approximation.



(a) Three step loss pulses approximation.

Fig. 16. Loss pulses approximation to get analytical solution of junction temperature. (green: original loss and corresponding junction temperature, red: Approximate loss pulses and corresponding junction temperature)

V. CONCLUSIONS

The relationship between the reliability and cost of converters is quantified by the junction temperature and chip

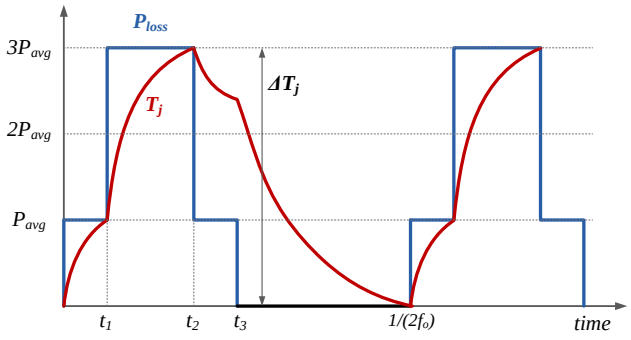


Fig. 17. The calculation of junction temperature fluctuation by 2 step loss pulses. (t1= 1/(8 f_o), t2=3/(8 f_o), t3=1/(2 f_o), f_o is the fundamental frequency)

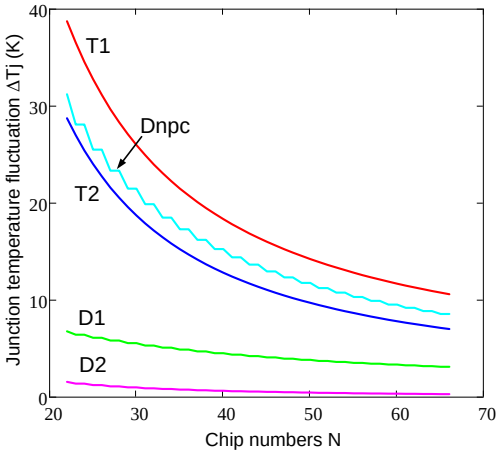
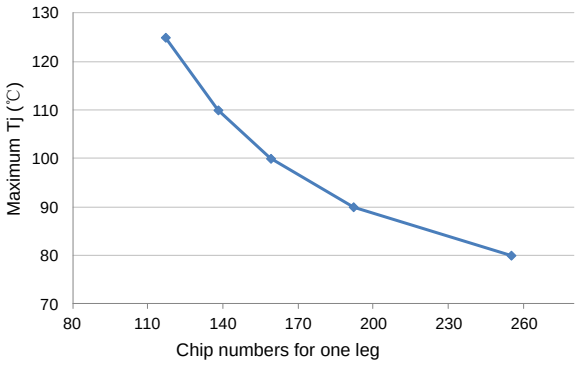


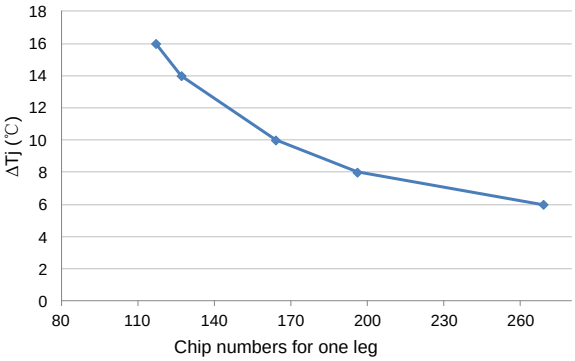
Fig. 18. Junction temperature fluctuation ΔT_j of each power device in 3L-NPC grid inverter vs. Chip numbers. (Normal operation, P_o=10 MW, f_s=800 Hz, V_{ll}= 3.3 kVrms).

numbers of power switching devices respectively in this paper. It is proved that the conduction loss, switching loss and thermal impedance models of power switching devices (IGBT module) can be included with chip number information. A simplified analytical solution which directly extracts the junction temperature mean value T_m and fluctuation ΔT_j is proposed. The proposed reliability-cost model is demonstrated on a 10 MW 3L-NPC wind power inverter as case study.

With the developed reliability-cost profile for the given converter solution, it is possible to enable more accurate and cost-effective design for wind power converter achieving the target reliability performance. And it is also possible to unify and compare different converter solutions in a more sensible way.



(a) Maximum junction temperature



(b) Fluctuation of junction temperature

Fig. 19. Junction temperature vs. chip numbers for one leg of 3L-NPC grid side converters. (All of the devices are set to have the same junction temperature by adjusting the chip numbers respectively, P_o=10 MW, f_s=800 Hz, V_{ll}= 3.3 kVrms).

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