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dq-Frame Cascaded Delayed Signal Cancellation Based PLL: Analysis, Design, and Comparison With Moving Average Filter Based PLL

Saeed Golestan, *Member, IEEE*, Malek Ramezani, *Member, IEEE*, Josep M. Guerrero, *Senior Member, IEEE*, and Mohammad Monfared *Member, IEEE*

***Abstract*—To improve the performance of phase-locked loops (PLLs) under adverse grid conditions incorporating different filtering techniques into their structures have been proposed in literature. These filtering techniques can be broadly classified into in-loop and pre-loop filtering techniques depending on their position in the PLL structure. Inspired from the concept of delayed signal cancellation (DSC), the idea of cascaded DSC (CDSC) has recently been introduced as an effective solution to improve the performance of the PLL under adverse grid conditions. However, the focus has been on the application of CDSC operator as the pre-filtering stage of PLL, and little work has been conducted on its application as the in-loop filtering stage of PLL. This paper provides a detailed analysis and design of *dq*CDSC-PLL (PLL with in-loop *dq*-frame CDSC operator). The study is started with an overview of this PLL. A systematic design method to fine tune its control parameters is then proposed. The performance of the *dq*CDSC-PLL under different grid scenarios is then evaluated in details. It is then shown that how using the proportional-integral derivative controller as the loop filter can improve the response time of *dq*CDSC-PLL. A detailed comparison between the *dq*CDSC-PLL and moving average filter (MAF) based PLL (MAF-PLL) is then carried out. Through a detailed mathematical analysis, it is also shown that these PLLs are equivalent under certain conditions. The suggested guidelines in this paper make designing the *dq*CDSC-PLL a simple and straightforward procedure. Besides, the analyses performed in this paper provide a useful insight for designers about the advantages/disadvantages of *dq*CDSC-PLL for their specific applications.**

***Index Terms*—Delayed signal cancellation (DSC), phase-locked loop (PLL), synchronization.**

I. Introduction

The three-phase synchronous reference frame phase-locked loop (SRF-PLL) is probably the most widely used synchronization technique within the areas power electronics and power systems [1]. In this PLL, the three-phase voltages are transformed to the synchronous (*dq*) reference frame by applying the Clarke and, subsequently, the Park transformations. The *dq*-frame angular position is controlled using a feedback loop which forces v_q (or v_d) to zero in steady-state. A proportional-integral (PI) controller is typically used as the loop filter (LF) in the SRF-PLL.

The SRF-PLL can achieve an accurate estimation of grid voltage phase/frequency when the grid voltage is clean and balanced; however, its performance tends to worsen under unbalanced and distorted grid conditions. To improve the performance of the SRF-PLL under adverse grid conditions, different approaches have been proposed in literature. These approaches are mainly based on adding a filtering stage either within the phase control loop of the PLL (called the in-loop filtering techniques) or before the input of the PLL (called the pre-filtering techniques).

The pre-filtering techniques are typically employed when, in addition to the grid voltage phase and frequency, the accurate extraction of the fundamental (or even harmonic) sequence components are also required by the PLL. These filtering techniques extract the gird fundamental frequency positive sequence (FFPS) component and feed it to the SRF-PLL to estimate the grid fundamental phase and frequency. The estimated phase/frequency is then fed back to make them frequency adaptive[1]. In [3], using the dual second order generalized integrator (DSOGI) is suggested as the SRF-PLL's pre-filtering stage. This method works based on the instantaneous symmetrical components (ISC) method in the stationary ($\alpha\beta$) reference frame. The extended version of this filter is suggested in [4]. Using the complex coefficient filters (CCFs) as the PLL's pre-filtering stage can be found in [5], [6]. The interesting feature of CCFs is that they can make distinction between the positive and negative sequences for the same frequency [7]. In [8], using the space-vector discrete Fourier transform (SVFT) as the pre-filtering stage is suggested. The low computational burden (if it is implemented in recursive form) and the effectiveness are the notable features of this filtering technique. In [2], a simple yet effective pre-filtering technique is suggested. This method uses a synchronous reference frame (SRF) structure rotating synchronously with the grid fundamental frequency and two moving average filters (MAFs) to extract the FFPS component for the SRF-PLL.

The in-loop filtering techniques are often preferred when the extraction of the grid fundamental sequence components are not required by the PLL. In [9]-[14], incorporating one or more

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[1]Sometimes, a secondary phase/frequency estimation algorithm is used to make the pre-filtering stage frequency adaptive (for example see [2]). The main reason behind this is to achieve a faster transient response.

notch filters (NFs) into the PLL control loop is suggested. The NF is a band-rejection filter that significantly attenuates the signals within a narrow band of frequencies and passes all other frequency components with negligible attenuation. This feature makes the NFs very interesting for selective cancellation of the desired harmonic components in the PLL control loop. In [15]-[20], using the MAF in the PLL control loop is suggested. The MAF is a linear phase filter that can act as ideal low pass filter (LPF) is certain conditions holds. In [21], using the repetitive regulators in the PLL control loop is suggested. The numerical and experimental results in [21] show that the repetitive regulator can be effective in rejection of disturbance components in the PLL control loop. To provide a fast dynamic response and, at the same time, to achieve a high disturbance rejection capability, incorporating one or more lead compensators in the PLL control loop is suggested in [22]. The suggested lead compensators are second order and have pairs of purely imaginary poles and zeros. So, they provide the selective cancellation like NFs without lagging the loop below -180° (stability limit). Thus, the PLL can achieve a high bandwidth (a fast dynamic response) without jeopardizing the stability and the filtering capability.

Inspired from the concept of delayed signal cancellation (DSC) [23]-[29], the idea of cascaded DSC (CDSC) has recently been introduced as an effective solution to improve the performance of the PLL under adverse grid conditions [30]-[33]. However, the focus has been on application of CDSC operators as the pre-filtering stage of the PLL, and little work has been conducted on its application as the in-loop filtering stage of the PLL. To be more specific 1) no systematic design approach to fine tune the control parameters of the SRF-PLL with in-loop CDSC (hereafter called *dq*CDSC-PLL) has been reported yet; 2) no detailed analysis to evaluate the performance of the *dq*CDSC-PLL under different grid scenarios has been performed yet.

This paper provides a detailed analysis and design of the *dq*CDSC-PLL. The main contributions of this paper can be summarized as follows:

- A systematic design approach to fine tune the control parameters of the *dq*CDSC-PLL is presented. A PI-type LF in the PLL is considered. The suggested design approach has a general theme, so it can be applied to different versions of the *dq*CDSC-PLL.
- To gain insight into the advantages and disadvantages of different versions of *dq*CDSC-PLL, their performance under different grid disturbances are evaluated in details.
- A simple approach to improve the dynamic response of *dq*CDSC-PLL is presented and evaluated.
- To further highlight the advantages and disadvantages of the *dq*CDSC-PLL, a detailed comparison between this PLL and MAF-PLL (SRF-PLL with in-loop MAF) is carried out. It is also shown that these two PLLs are mathematically equivalent under certain conditions.

II. Overview

In the *dq*-frame, the half-wave symmetry of harmonic components makes it possible to eliminate them by summing with their delayed versions. Obviously this process does not change the dc component in the *dq*-frame, i.e., the original FFPS component. This method is known as the *dq*-frame DSC (*dq*DSC) [30], [31].

Application of the *dq*DSC operator to an arbitrary *dq*-frame voltage signal $v(t)$ is defined as

$$\bar{v}\left(t\right)=\frac{1}{2}\left[v\left(t\right)+v\left(t-T/n\right)\right] \tag{1}$$

where $\bar{v}(t)$ is the output signal of *dq*DSC operator, T is the grid voltage fundamental period, and n is referred to as the delay factor. From (1), the transfer function of the *dq*DSC operator can be obtained as

$$dq\mathrm{DSC}_n(s)=\frac{\bar{v}\left(s\right)}{v\left(s\right)}=\frac{1}{2}\left(1+e^{-\frac{T}{n}s}\right). \tag{2}$$

By substituting $s=j\omega$ into (2), and performing some simple mathematical manipulations, the magnitude and phase expressions of the *dq*DSC operator can be obtained as

$$dq\mathrm{DSC}_n(j\omega)=\left|\cos\left(\frac{\omega T}{2n}\right)\right|\angle-\left(\frac{\omega T}{2n}\right). \tag{3}$$

Using (3), it can be shown that the *dq*DSC operator provides unity gain at zero frequency, and zero gain at frequencies $f=\frac{n}{T}\left(2k\pm\frac{1}{2}\right)$ in hertz, where $k=0,\pm1,\pm2,\pm3,\ldots$. It means that the *dq*DSC operator passes the dc component and blocks some specific harmonic components depending on the value of the delay factor n. For example, selecting $n=4$ enables the *dq*DSC operator to block all harmonics of order $h=\pm2,\pm6,\pm10,\pm14,\ldots$ in *dq*-frame. Notice that $|dq\mathrm{DSC}_n(j\omega)|\leq1$, so the other harmonic components (i.e., those harmonic components that are not blocked) are attenuated or, at most, left unchanged.

Most often a single *dq*DSC operator is not good enough to eliminate/attenuate all harmonic components of concern. So, depending on the grid harmonic type and application in hand, cascading several *dq*DSC operators with specific delay factors is often required [30], [31]. Equation (4) describes the *dq*CDSC operator in s-domain where m is the number of cascaded *dq*DSC operators.

$$\begin{aligned}\mathrm{CDSC}_{n_1,n_2,\cdots,n_m}(s)=&\,dq\mathrm{DSC}_{n_1}(s)\times dq\mathrm{DSC}_{n_2}(s)\\&\times\cdots\times dq\mathrm{DSC}_{n_m}(s).\end{aligned} \tag{4}$$

Fig. 1 illustrates the time domain implementation of $dq\mathrm{CDSC}_{n_1,n_2,\ldots,n_m}$ operator. Notice that to realize the *dq*CDSC operator with digital signal processor (DSP) in practice, the T/n_i $(i=1,2,\ldots,m)$ signal delays in cascaded units should be implemented by buffering $N_i=(T/n_i)/T_s$ samples in DSP memories, where T_s is the sampling time.

Incorporating the *dq*CDSC operator into the PLL control loop has been proposed in some recent literature [30]-[31]. However, no systematic design approach to fine tune its control parameters and no detailed analysis to evaluate its advantages/disadvantages under different grid scenarios has been presented yet. Fig. 2 shows the basic scheme of the *dq*CDSC-PLL in which the LF(s) is the LF transfer function, $\hat{\omega}$ and $\hat{\theta}_1^+$ are the estimated frequency and phase of the grid FFPS component, respectively, and ω_{ff} is the nominal value

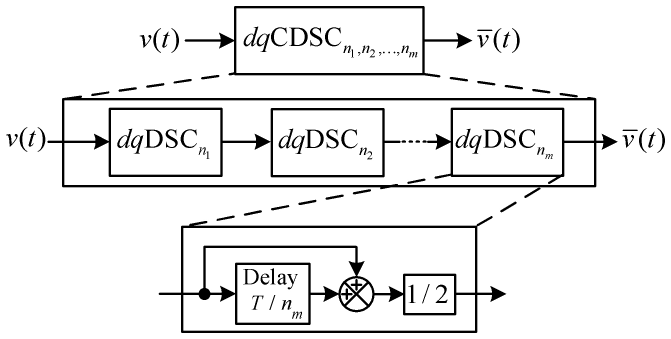

Fig. 1. Block diagram description of *dq*CDSC operator.

of grid frequency.

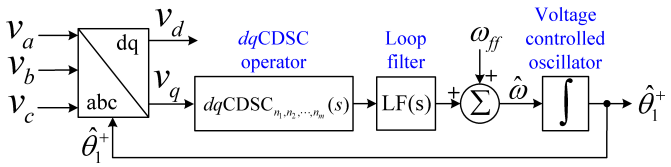

Fig. 2. Block diagram description of the *dq*CDSC-PLL.

III. Control Design Guidelines

In this section, a systematic approach to design the control parameters of the *dq*CDSC-PLL is presented. The suggested design approach is based on the small-signal model of this PLL which is shown in Fig. 3. In this model, $D(s)$ is the Laplace transform of the disturbance input to the model, and V_1^+ is the amplitude of FFPS component of the grid voltage. Notice that this model is the same as that of the conventional SRF-PLL [1], however the transfer function of *dq*CDSC operator is also included in the loop. A PI-type LF is considered in the *dq*CDSC-PLL.

An issue that may need to be discussed here is the dependence of the PLL dynamics on the amplitude of FFPS component. As it can be observed in Fig. 3, the amplitude of the FFPS component appears as gain in the forward path of the PLL small-signal model. It implies any variation in the amplitude of the FFPS component affect the PLL stability and dynamic response [34]. This problem can be simply avoided by incorporating an amplitude normalization unit into the PLL structure. This unit can be simply realized by adding another *dq*CDSC operator in the *d*-axis to obtain an estimation of the FFPS component amplitude, and dividing the LF input signal by this estimated amplitude.

A. *dq*CDSC Operator Design

The first step of design procedure is to select the number of cascaded *dq*DSC operators and their delay factors in the *dq*CDSC operator. This selection depends on whether the grid harmonic pattern is known or unknown. If the grid harmonic pattern is unknown, then it should be assumed that all sequence components of all orders are available in the grid voltage. In such a case, the $dq\text{CDSC}_{2,4,8,16,32}$ operator is a good choice [30]. On the other hand, if the grid harmonic pattern

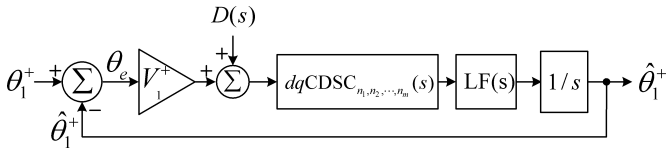

Fig. 3. Small-signal model of the *dq*CDSC-PLL.

is known, then the *dq*CDSC operator should be designed such that all anticipated harmonic components are rejected and, at the same time, the *dq*CDSC total delay time (i.e., $T/n_1+T/n_2+\cdots+T/n_m$) is as small as possible (it will be shown later that with increasing the total-time delay introduced by the *dq*CDSC operator in the control loop, the PLL bandwidth should be reduced to ensure its stability). Based on this design criteria, the proper *dq*CDSC operator for different grid scenarios can be obtained as summarized in Table I. Notice that in all scenarios the presence of fundamental frequency negative sequence component in the grid voltage (which may occur due to asymmetrical grid faults) is also considered. It is also worth noticing that when the grid harmonic pattern is unknown, or when the grid is distorted in an asymmetrical manner[2], a same *dq*CDSC operator, i.e., $dq\text{CDSC}_{2,4,8,16,32}$ operator, should be used.

The last column in table I shows the name assigned to the different versions of *dq*CDSC-PLL. Notice that the PLL that is called the *dq*CDSC-PLL1 in this Table uses an single *dq*DSC operator in its control loop, so it is actually a *dq*DSC-PLL (not *dq*CDSC-PLL). However, for the sake of consistency, we call it *dq*CDSC-PLL1.

B. Approximating the Dynamics of *dq*CDSC Operator

Incorporating the *dq*CDSC operator into the PLL control loop significantly complicates the tuning procedure. So, approximating its dynamic with a simple transfer function can be very helpful in tuning procedure. In this section, the dynamics of *dq*CDSC operator are approximated with a simple first-order transfer function. As it will be shown later, this approximation barely affects the *dq*CDSC-PLL dynamic behavior, but significantly simplifies the analysis and tuning procedure.

Let us start with the simplest case, i.e., a single *dq*DSC operator. Approximating the delay term in (2) by the first-order padé approximation , i.e., $e^{-(T/n)s} \approx \frac{1-\left(\frac{T}{2n}\right)s}{1+\left(\frac{T}{2n}\right)s}$, yields the first-order approximation of the $dq\text{DSC}_n$ transfer function (2) as

$$dq\text{DSC}_n(s) \approx \frac{1}{\left(\frac{T}{2n}\right)s+1}. \tag{5}$$

This approximation can be simply extended to the $dq\text{CDSC}$ operator. First, let us assume the $dq\text{CDSC}$ operator is consisted of two $dq\text{DSC}$ operators with delay factors n_1 and n_2. In such a case, according to (2) and (4), its transfer function

[2]When the grid is distorted in an asymmetrical manners, all harmonic components of all sequences may exist in the grid voltage [30].

TABLE I
DIFFERENT SCENARIOS FOR THE GRID HARMONIC PATTERN AND THE PROPER *dq*CDSC OPERATOR FOR THESE SCENARIOS.

Grid harmonic pattern		Proper *dq*CDSC	PLL name
Known	not distorted	$dq\mathrm{DSC}_4$	*dq*CDSC-PLL1
	non-triplen odd harmonics of order -5,$+7$,-11,$+13$,-17,$+19$	$dq\mathrm{CDSC}_{4,24}$	*dq*CDSC-PLL2
	symmetrical	$dq\mathrm{CDSC}_{4,6,24}$	*dq*CDSC-PLL3
	odd harmonic components	$dq\mathrm{CDSC}_{4,8,16,32}$	*dq*CDSC-PLL4
	asymmetrical	$dq\mathrm{CDSC}_{2,4,8,16,32}$	*dq*CDSC-PLL5
Unknown	———		

can be expressed as

$$dq\mathrm{CDSC}_{n_1,n_2}(s) = \underbrace{\frac{1}{2}\left(1+e^{-(T/n_1)s}\right)}_{dq\mathrm{DSC}_{n_1}(s)} \times \underbrace{\frac{1}{2}\left(1+e^{-(T/n_2)s}\right)}_{dq\mathrm{DSC}_{n_2}(s)}. \tag{6}$$

Using (5), (6) can be approximated by

$$\begin{aligned} dq\mathrm{CDSC}_{n_1,n_2}(s) &\approx \frac{1}{\left(\frac{T}{2n_1}\right)s+1} \times \frac{1}{\left(\frac{T}{2n_2}\right)s+1} \\ &= \frac{1}{\underline{\frac{T^2}{4n_1n_2}s^2} + \left(\frac{T}{2n_1}+\frac{T}{2n_2}\right)s+1}. \end{aligned} \tag{7}$$

At low frequency range, which is the frequency range of concern, the underlined term in (7) is negligible. As a consequence, (7) can be further simplified as

$$dq\mathrm{CDSC}_{n_1,n_2}(s) \approx \frac{1}{\frac{T}{2}\left(1/n_1+1/n_2\right)s+1}. \tag{8}$$

Following a similar procedure, it can be shown that the transfer function of the dqCDSC operator can be approximated in general form as

$$\begin{aligned} &dq\mathrm{CDSC}_{n_1,n_2,\ldots,n_m}(s) \\ &\quad\approx \frac{1}{\underbrace{\frac{T}{2}\left(1/n_1+1/n_2+\ldots+1/n_m\right)}_{T_d}s+1}. \end{aligned} \tag{9}$$

Table II summarizes the approximate transfer functions for different *dq*CDSC operators.

To evaluate the accuracy of this approximation, Fig. 4 provides a Bode plot comparison between the transfer function of the $dq\mathrm{DSC}_{2,4,8,16,32}$ operator and its approximate transfer function. As expected, the approximate transfer function is accurate enough in predicting the behavior of the *dq*CDSC operator.

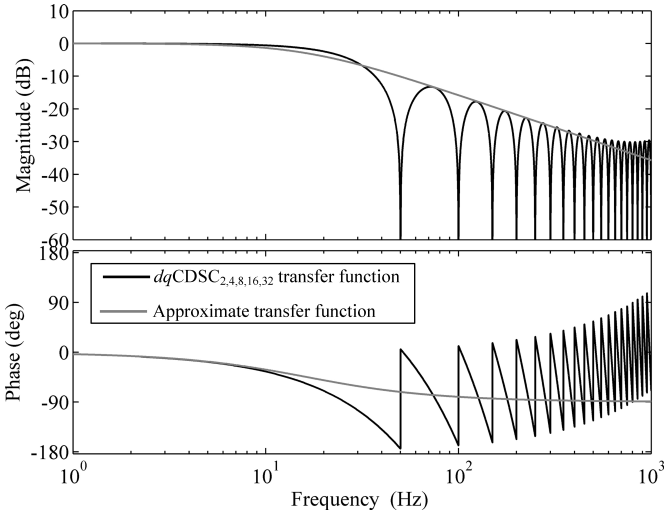

Fig. 4. Bode plots of the $dq\mathrm{CDSC}_{2,4,8,16,32}$ transfer function (black line) and its first order approximation (gray line).

C. LF Parameters Design

In this section, a systematic approach to design the LF parameters of the *dq*CDSC-PLL is presented. As mentioned before, the LF is a PI controller, i.e., $LF(s) = k_p + k_i/s$, where k_p and k_i are the proportional and integral gains, respectively. The suggested design approach is based on the symmetrical optimum (SO) method which is a standard design procedure in various applications [35]-[36].

From Fig. 3, the open-loop transfer function of *dq*CDSC-PLL can be obtained in general form as

$$G_{ol}(s) = \left.\frac{\hat{\theta}_1^+}{\theta_e}\right|_{D(s)=0} = V_1^+ dq\mathrm{CDSC}_{n_1,n_2,\ldots,n_m}(s)\mathrm{LF}(s)\frac{1}{s}. \tag{10}$$

By substituting $\mathrm{LF}(s) = k_p + k_i/s$ into (10), and replacing the transfer function of *dq*CDSC operator with its first-order approximation, we can obtain

$$G_{ol}^{\mathrm{PI}}(s) \approx V_1^+ \frac{1}{T_d s+1}\frac{k_p s+k_i}{s}\frac{1}{s} = V_1^+ \frac{\frac{1}{T_d}\left(k_p s+k_i\right)}{s^2\left(s+\frac{1}{T_d}\right)} \tag{11}$$

where the superscript PI denotes that the PLL uses the PI-type LF. The open-loop transfer function (11) can be rewritten of the form

$$G_{ol}^{\mathrm{PI}}(s) \approx \frac{V_1^+ k_p \omega_p \left(s+\omega_z\right)}{s^2\left(s+\omega_p\right)} \tag{12}$$

where $\omega_p = 1/T_d$ and $\omega_z = k_i/k_p$.

The SO method is a standard design method for the systems having an open-loop transfer function of the form (12). According to this method, the maximum phase margin (PM) is achieved if the crossover frequency ω_c is at the geometric mean of the corner frequencies of ω_p and ω_z, i.e.,

TABLE II
APPROXIMATE TRANSFER FUNCTION FOR DIFFERENT *dq*CDSC OPERATORS.

*dq*CDSC operator	$dq\mathrm{DSC}_4$	$dq\mathrm{CDSC}_{4,24}$	$dq\mathrm{CDSC}_{4,6,24}$	$dq\mathrm{CDSC}_{4,8,16,32}$	$dq\mathrm{CDSC}_{2,4,8,16,32}$
Approximate transfer function	$\frac{1}{(T/8)s+1}$	$\frac{1}{(7T/48)s+1}$	$\frac{1}{(11T/48)s+1}$	$\frac{1}{(15T/64)s+1}$	$\frac{1}{(31T/64)s+1}$

$\omega_c = \sqrt{\omega_p \omega_z}$. According to this, it is easy to obtain

$$\left.\begin{array}{ll} \left|G_{ol}^{\mathrm{PI}}(s)\right|_{s=j\omega_c} = 1 \Rightarrow \frac{V_1^+ k_p \omega_p \sqrt{\omega_c^2+\omega_z^2}}{\omega_c^2 \sqrt{\omega_c^2+\omega_p^2}} = 1 \\ \mathrm{SO\,method} \quad \Rightarrow \quad \omega_c = \sqrt{\omega_p \omega_z} \end{array}\right\} \Rightarrow k_p = \frac{\omega_c}{V_1^+} \tag{13}$$

Let us define $\omega_p = b^2 \omega_z$, where b is a positive design constant, then according to the equation $\omega_c = \sqrt{\omega_z \omega_p}$ we can obtain

$$\begin{array}{l} \omega_p = b\omega_c \\ \omega_z = \omega_c / b. \end{array} \tag{14}$$

Using (13) and (14), and remembering that $\omega_p = 1/T_d$, the proportional and integral gains k_p and k_i can be expressed as

$$\begin{array}{l} k_p = \omega_c / V_1^+ = \omega_p / \left(bV_1^+\right) = 1/\left(T_d b V_1^+\right) \\ k_i = \omega_z k_p = \omega_p^2 / \left(b^3 V_1^+\right) = 1/\left(T_d^2 b^3 V_1^+\right). \end{array} \tag{15}$$

So, k_p and k_i can be simply determined by selecting a proper value for the design constant b. Remember that the value of T_d is determined according to the selected *dq*CDSC operator (see (9) and Table II).

To determine a proper value for b, its effect on the dynamic response and stability of the PLL should be examined. First, its effect on the dynamic performance of the PLL is analyzed. From Fig. 3 and the open-loop transfer function (12), the phase-error transfer function of the PLL can be obtained as

$$\begin{aligned} G_e(s) = \left.\frac{\theta_e}{\theta_1^+}\right|_{D(s)=0} &= \frac{1}{1+G_{ol}^{\mathrm{PI}}(s)} \\ &\approx \frac{s^2\left(s+\omega_p\right)}{s^2\left(s+\omega_p\right)+V_1^+ k_p \omega_p \left(s+\omega_z\right)}. \end{aligned} \tag{16}$$

Substituting (13) and (14) into (16) and performing some simple mathematical manipulations yields

$$G_e(s) \approx \frac{s^2\left(s+b\omega_c\right)}{\left(s+\omega_c\right)\left(s^2+\left(b-1\right)\omega_c s+\omega_c^2\right)} \tag{17}$$

By defining $b = 2\zeta + 1$, (17) can be rewritten as

$$G_e(s) \approx \frac{s^2\left(s+\left(2\zeta+1\right)\omega_c\right)}{\left(s+\omega_c\right)\left(s^2+2\zeta\omega_c s+\omega_c^2\right)} \tag{18}$$

As shown, the design constant b determines the damping of the system. So, it can be selected according to required damping for the PLL. Most literature recommend $\zeta = 1/\sqrt{2}$ for best damping. This selection yields $b = \sqrt{2}+1$.

An important issue that should be analyzed here is the PLL stability margin. From open-loop transfer function (12), the PM of PLL can be expressed as

$$\mathrm{PM} \approx \tan^{-1}\left(\omega_c/\omega_z\right) - \tan^{-1}\left(\omega_c/\omega_p\right). \tag{19}$$

Notice that (19) approximates the PM of *dq*CDSC-PLL, because it is obtained using the approximate open-loop transfer function (12) . Substituting (14) into (19) and performing some mathematical manipulations, yields

$$\mathrm{PM} \approx \tan^{-1}\left(\frac{b^2-1}{2b}\right). \tag{20}$$

As shown, the PM only depends on the value of b. This result was expected as the PM is related to the damping of the system. Substituting the selected value for b (i.e., $b = \sqrt{2}+1$) into (20) yields $\mathrm{PM} \approx 45^\circ$ which ensures the PLL stability.

TABLE III
CONTROL PARAMETERS OF DIFFERENT VERSIONS OF *dq*CDSC-PLL.

	T_d (see Table II)	$k_p = 1/\left(T_d b V_1^+\right)$	$k_i = 1/\left(T_d^2 b^3 V_1^+\right)$
*dq*CDSC-PLL1	$T/8$	165.68	11370.85
*dq*CDSC-PLL2	$7T/48$	142.02	8354.09
*dq*CDSC-PLL3	$11T/48$	90.37	3383.06
*dq*CDSC-PLL4	$15T/64$	88.36	3234.37
*dq*CDSC-PLL5	$31T/64$	42.76	757.27

Table III summarizes the designed values for the control parameters of *dq*CDSC-PLL under different grid scenarios ($V_1^+ = 1$ pu and $b = \sqrt{2}+1$ are considered in calculation of the parameters). Notice that k_p and therefore the crossover frequency (according to (13), the crossover frequency ω_c is equal to k_p for $V_1^+ = 1$) decreases with increasing the total time delay (as shown in (9), T_d is equal to half the total time delay of *dq*CDSC operator) in the *dq*CDSC-PLL control loop. This result was expected as, according to (15), k_p is inversely proportional to T_d. Therefore, we expect the fastest and slowest transient response for the *dq*CDSC-PLL1 and *dq*CDSC-PLL5, respectively.

D. Accuracy Assessment of Suggested Design Method

The suggested design approach in previous section was based on the approximate open-loop and phase-error transfer functions of the *dq*CDSC-PLL, which are obtained by approximating the dynamics of the *dq*CDSC operator in the PLL small-signal model with a simple first-order LPF. The aim of this section is to evaluate the accuracy of this approximation.

Fig. 5 shows the *exact* open-loop Bode plots of different versions of *dq*CDSC-PLL using the designed control parameters (see Table III). It can be observed the PM of all PLLs is very close to what was predicted by the approximate open-loop transfer function, i.e., $\mathrm{PM} = 45^\circ$. It can also be observed that the crossover frequency corresponds to the peak of phase plot (maximum PM) for all PLLs. This result was also predicted by the approximate open-loop transfer function.

According to the approximate phase-error transfer function (18), the phase-error response of the *dq*CDSC-PLL when the grid voltage undergoes a phase-angle jump $\Delta\phi$ and a frequency-step change $\Delta\omega$ can be approximated by (21) and

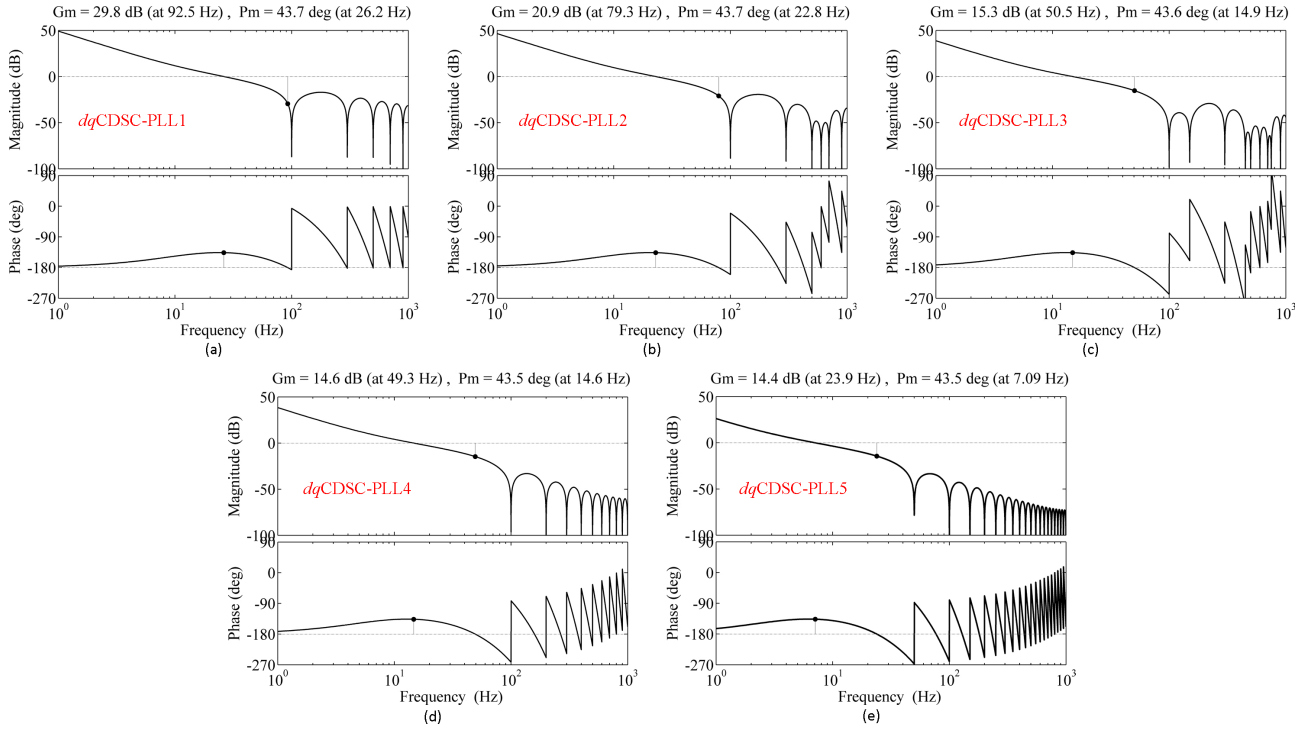

Fig. 5. The open loop Bode plots of (a) *dq*CDSC-PLL1, (b) *dq*CDSC-PLL2, (c) *dq*CDSC-PLL3, (d) *dq*CDSC-PLL4, and (e) *dq*CDSC-PLL5 using the designed control parameters (see Table III).

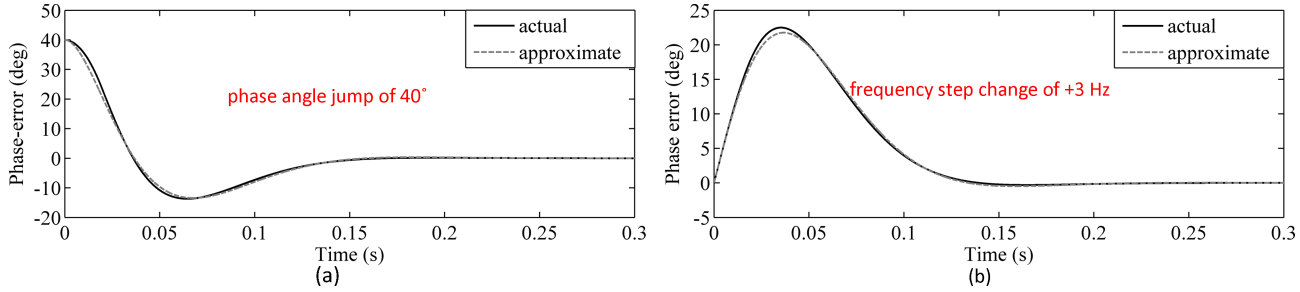

Fig. 6. Approximate phase-error (dashed lines) and actual phase-error (solid lines) responses of the *dq*CDSC-PLL5 under (a) a phase-angle jump of $+40^\circ$ and (b) a frequency step change $+3$ Hz.

(22), respectively.

$$\theta_e^{\Delta\phi}(t) \approx \frac{\Delta\phi}{\zeta-1}\left[\zeta e^{-\omega_c t} - e^{-\zeta\omega_c t}\cos\left(\omega_c t\sqrt{1-\zeta^2}\right)\right] \tag{21}$$

$$\theta_e^{\Delta\omega}(t) \approx \frac{\Delta\omega}{(1-\zeta)\omega_c}\left[\zeta e^{-\omega_c t} - e^{-\zeta\omega_c t}\left\{\zeta\cos\left(\omega_c t\sqrt{1-\zeta^2}\right) - \sqrt{1-\zeta^2}\sin\left(\omega_c t\sqrt{1-\zeta^2}\right)\right\}\right]. \tag{22}$$

Fig. 6 (a) and (b) compares the approximate phase-error and actual phase-error responses of the *dq*CDSC-PLL5 under a phase-angle jump of $+40^\circ$ and frequency step change $+3$ Hz, respectively. The approximate plots are obtained using (21) and (22), and the actual plots are obtained by simulating the actual *dq*CDSC-PLL5. It can be observed that the approximate results can accurately predict the *dq*CDSC-PLL5 behavior. Similar results can be obtained for other versions of *dq*CDSC-PLL.

According to what was shown in this section, it can be concluded that the approximation made during the design procedure and, therefore, the obtained approximate transfer functions are very accurate in prediction of the *dq*CDSC-PLL behavior.

IV. Numerical Results

The aim of this section is to evaluate the performance of the *dq*CDSC-PLL under different grid scenarios. To achieve this goal, all *dq*CDSC-PLLs are numerically simulated in Matlab/Simulink environment. Throughout the simulation studies, the sampling frequency is fixed to 14.4 kHz, and the nominal angular frequency is set to $2\pi 50$ rad/s. The other control parameters can be found in Table III.

A. Phase Angle Jump

Fig. 7 shows the numerical results when the grid voltage undergoes a phase angle jump of $+40^\circ$. It can be observed

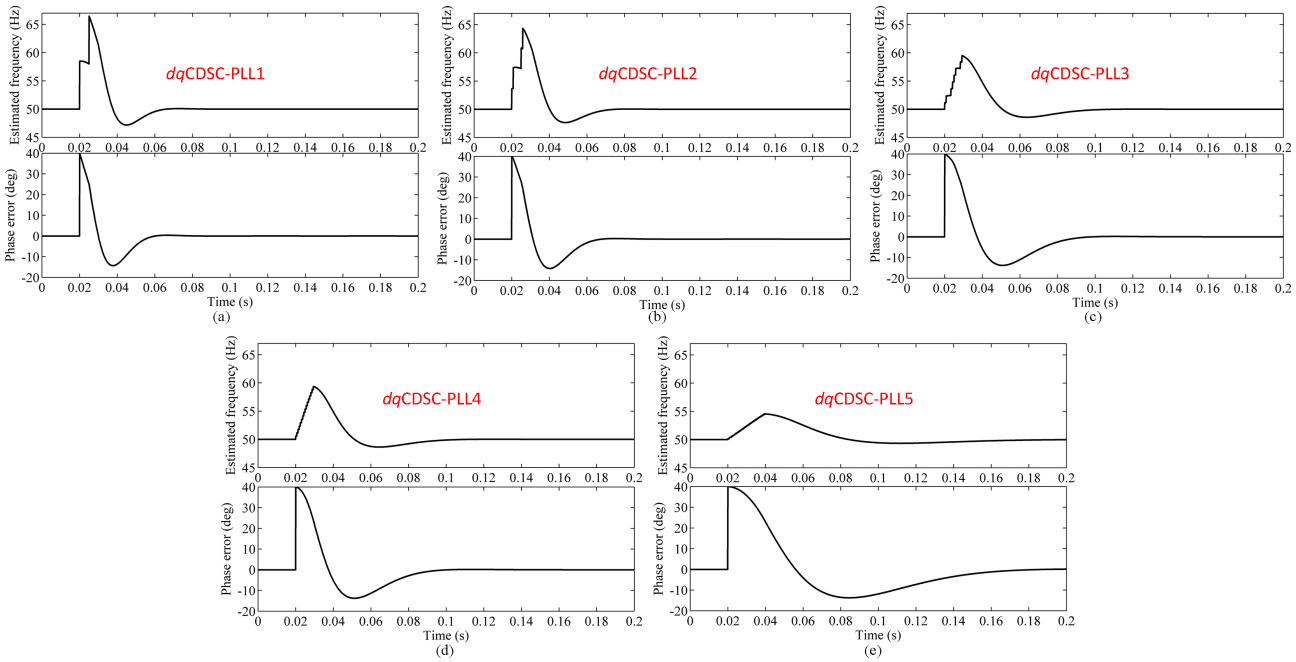

Fig. 7. Numerical results for (a) *dq*CDSC-PLL1, (b) *dq*CDSC-PLL2, (c) *dq*CDSC-PLL3, (d) *dq*CDSC-PLL4, and (e) *dq*CDSC-PLL5 when the grid voltage undergoes a phase angle jump of $+40°$.

TABLE IV
SUMMARY OF RESULTS.

	*dq*CDSC-PLL1	*dq*CDSC-PLL2	*dq*CDSC-PLL3	*dq*CDSC-PLL4	*dq*CDSC-PLL5
Phase-angle jump of $40°$					
2% settling time	36.6 ms (1.83 cycles)	43.2 ms (2.16 cycles)	68.8 ms (3.44 cycles)	70.5 ms (3.52 cycles)	146.2 ms (7.31 cycles)
Phase overshoot	14.37° (35.9%)	14.16° (35.4%)	13.83° (34.57%)	13.83° (34.57%)	13.72° (34.3%)
Peak frequency error	16.47 Hz	14.35 Hz	9.5 Hz	9.49 Hz	4.55 Hz
Frequency step change of $+3$ **Hz**					
2% settling time	36.3 ms (1.81 cycles)	42.7 ms (2.13 cycles)	68.1 ms (3.4 cycles)	69.6 ms (3.48 cycles)	144.2 ms (7.21 cycles)
Frequency overshoot	1.09 Hz (36.3%)	1.08 Hz (36%)	1.05 Hz (35%)	1.05 Hz (35%)	1.05 Hz (35%)
Peak phase error	5.77°	6.74°	10.59°	10.85°	22.52°
Unbalanced voltage sag					
Peak-to-peak phase error (freq.=49 Hz)	0.2°	0.16°	0.05°	0.07°	0.03°
Peak-to-peak phase error (freq.=47 Hz)	0.62°	0.51°	0.18°	0.22°	0.1°
Distorted grid condition					
Peak-to-peak phase error (freq.=49 Hz)	——	0.05°	0.03°	0.01°	0°
Peak-to-peak phase error (freq.=47 Hz)	——	0.15°	0.09°	0.03°	0.01°

that the *dq*CDSC-PLL1 and *dq*CDSC-PLL2 have a relatively fast transient response; the 2% settling time, i.e., the time after witch the phase error reaches and remains within $0.02 \times 40° = 0.8°$ neighborhood of zero, is around 2 cycles of the fundamental frequency for these PLLs. The *dq*CDSC-PLL5, however, has a slow transient response; the 2% settling time is around 7 cycles for this PLL. The *dq*CDSC-PLL3 and *dq*CDSC-PLL4 have a moderate transient response; the 2% settling time is around 3.5 cycles for these PLLs. An important issue that may need to be discussed here is the transient behavior of the estimated frequency when the phase-jump happens. From Fig. 7, it can be observed that the *dq*CDSC-PLL1 and *dq*CDSC-PLL5 experience the largest and smallest transient in the estimated frequency, respectively. The reason is that the *dq*CDSC-PLL1 and *dq*CDSC-PLL5 have the highest and lowest control bandwidth, respectively. Notice that increasing the PLL bandwidth increases the coupling between phase and frequency variables and, therefore, results in large transients in the estimated frequency during the phase angle jumps [37]. See Table IV for details.

B. Frequency Step Change

Fig. 8 shows the numerical results when the grid voltage undergoes a frequency step change of $+3$ Hz. From the settling-time point of view, similar results as previous test can be observed. The 2% settling time, i.e., the time after which the estimated frequency reaches and remains within 0.02×3 Hz$= 0.06$ Hz of its final value, is around 2 cycles of fundamental frequency for *dq*CDSC-PLL1 and *dq*CDSC-PLL2, around 3.5 cycles for *dq*CDSC-PLL3 and *dq*CDSC-PLL4, and around 7 cycles for the *dq*CDSC-PLL5. See Table IV for details.

C. Unbalanced Voltage Sag

In this test, the steady-state performances of PLLs under an unbalanced voltage sag ($V_{1,a}^{+} = 0.4$ pu, $V_{1,b}^{+} = 1$ pu,

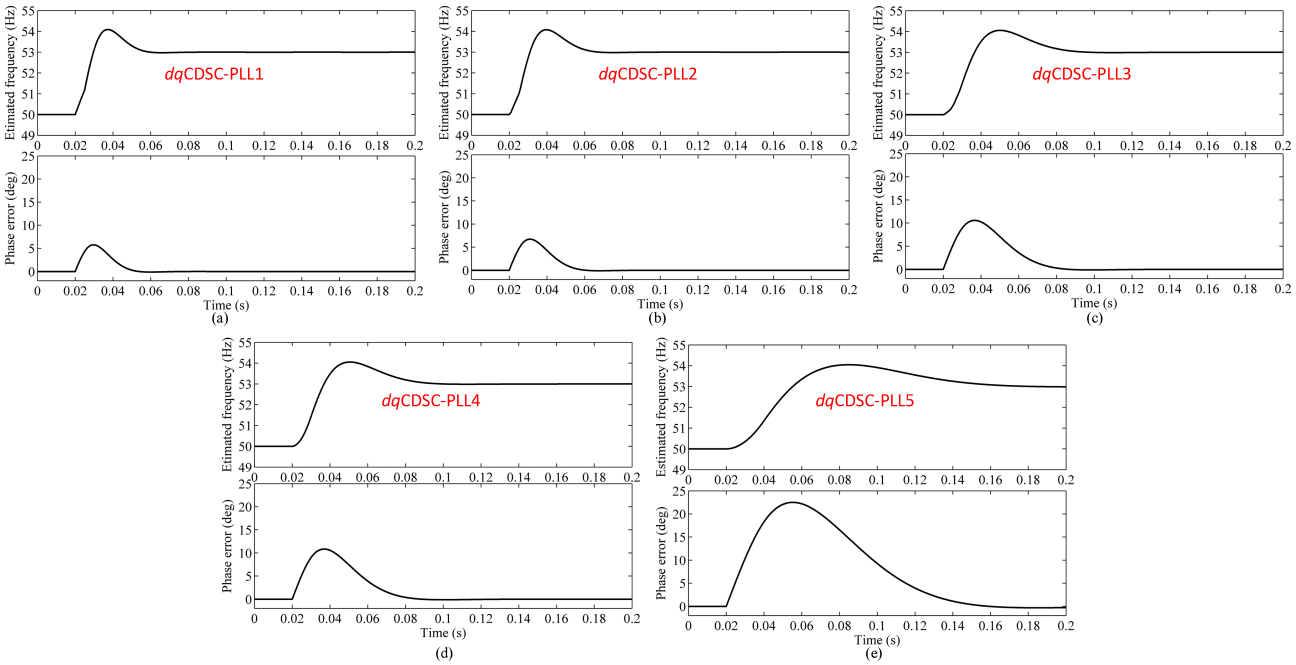

Fig. 8. Numerical results for (a) *dq*CDSC-PLL1, (b) *dq*CDSC-PLL2, (c) *dq*CDSC-PLL3, (d) *dq*CDSC-PLL4, and (e) *dq*CDSC-PLL5 when the grid voltage undergoes a frequency step change of $+3$ Hz.

and $V_{1,c}^{+} = 1$ pu) are evaluated. Since we already know that the PLLs under study have high filtering capabilities under nominal frequency condition (see open-loop Bode plots shown in Fig. 5), off-nominal frequency condition is considered in this test. Notice that according to the European standard EN-50160 [38], the grid frequency should be within the range of 50 Hz $-6\%/+4\%$ (i.e., $47-52$ Hz). So, 47 Hz can be considered as the worst case scenario for the grid frequency.

Fig. 9 shows the obtained results. It can be observed that all PLLs, particularly the *dq*CDSC-PLL5, show a good detection accuracy when the grid frequency is close to its nominal value. However, their performances, particularly the performance of *dq*CDSC-PLL1 and *dq*CDSC-PLL2, tend to worsen with increasing the deviation of grid frequency from its nominal value. See Table IV for details.

D. Distorted Grid Condition

In this test, the performances of PLLs are evaluated when the grid voltage is distorted with harmonics. The numerical results for *dq*CDSC-PLL1 are not presented as it has been designed for unbalanced but not distorted grid conditions (see Table I). The parameters of distorted input voltage are summarized in Table V. Notice that the considered values for the amplitude of harmonic components are the maximum allowed values according to IEC standards (see Table I in [39]). For the same reason mentioned in previous test, off-nominal grid frequency condition is considered in this test.

The obtained results are shown in Fig. 10. It can be observed that the detection accuracy of all PLLs, particularly *dq*CDSC-PLL4 and *dq*CDSC-PLL5, is good for most applications. See Table IV for details.

TABLE V
PARAMETERS OF DISTORTED INPUT VOLTAGE

Voltage component	**Amplitude** (p.u.)
Fundamental positive sequence	1
5^{th} harmonic negative sequence	0.06
7^{th} harmonic positive sequence	0.05
11^{th} harmonic negative sequence	0.035
13^{th} harmonic positive sequence	0.03

E. Summary and Recommendations

- The *dq*CDSC-PLL1 and *dq*CDSC-PLL2 have a rather fast transient response, however they suffer from a weak performance under unbalanced grid conditions when the grid frequency deviation from its nominal value is high. So, we recommend to make the *dq*DSC/*dq*CDSC operators in these PLLs frequency adaptive particularly when high variations in grid frequency is expected. It is worth mentioning that realizing a frequency-adaptive *dq*CDSC operator can be achieved in different ways such as 1) adaptive adjustment of the number of samples per delay times in the *dq*CDSC operator, using the linear interpolation method [28]-[31], using a variable sampling frequency [18], [19]. The last method is not very popular since a variable sampling frequency may not be always allowed or possible.
- the *dq*CDSC-PLL3, the *dq*CDSC-PLL4, and, particularly, the *dq*CDSC-PLL5 have a good performance under unbalanced and distorted grid conditions, but they suffer from a rather slow transient response. So, frequency adaptability of *dq*CDSC operators in these PLLs are not required. To overcome the problem of slow transient response, a solution is presented in the next section.

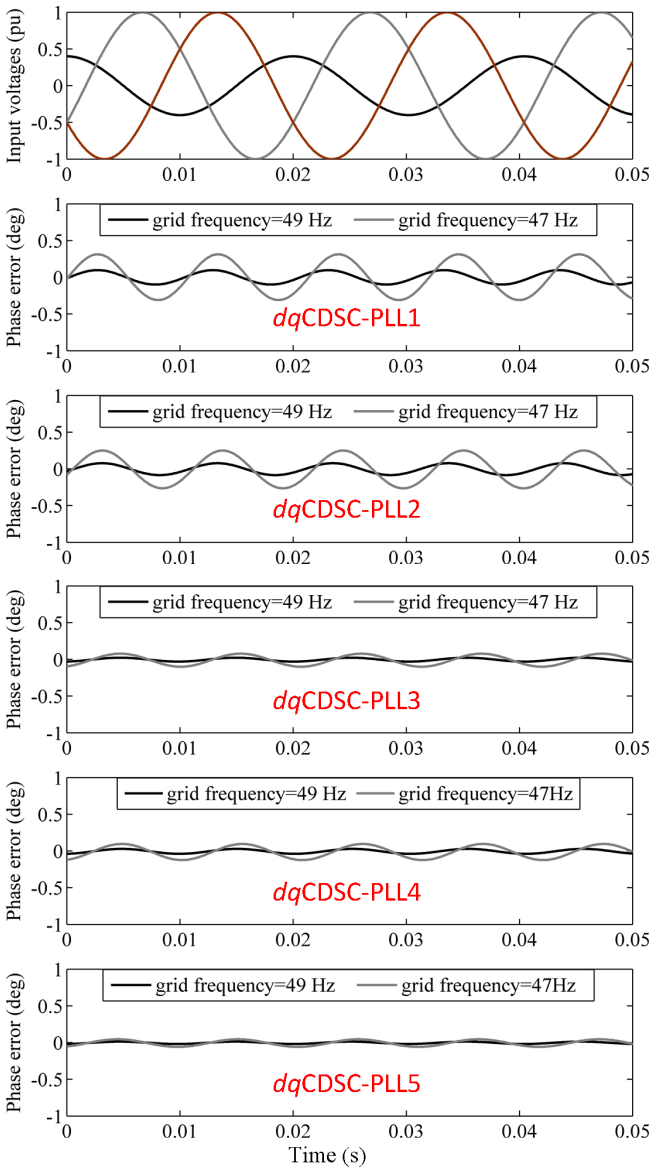

Fig. 9. Numerical results under an unbalanced voltage sag and during off-nominal grid frequency conditions.

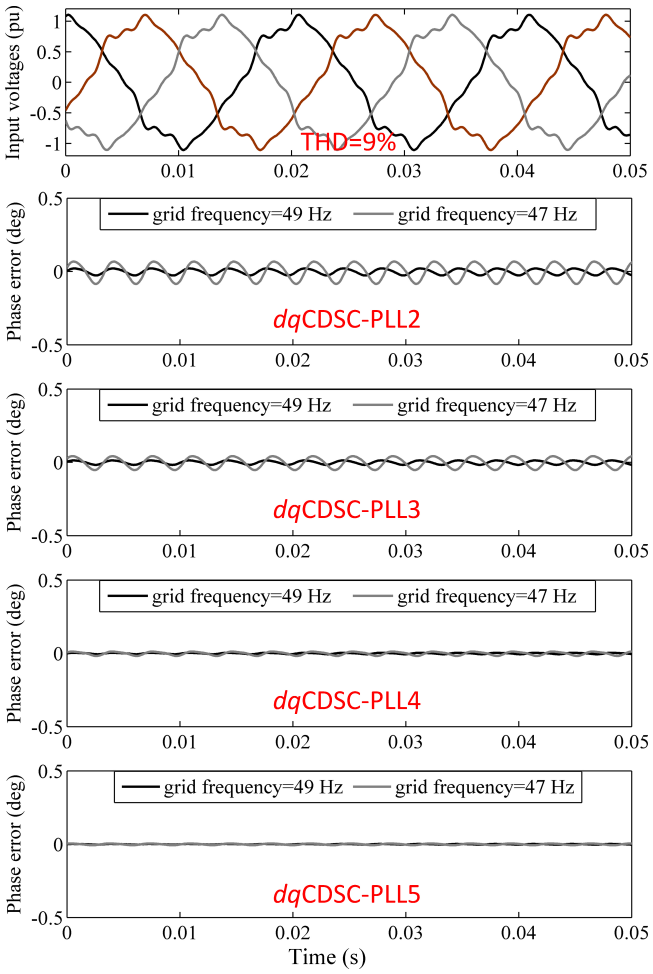

Fig. 10. Numerical results under harmonically distorted and off-nominal frequency conditions.

V. Improvement of Response Time

This section deals with improving the response time of *dq*CDSC-PLL3, *dq*CDSC-PLL4, and the *dq*CDSC-PLL5. Notice that the response times of *dq*CDSC-PLL1 and *dq*CDSC-PLL2 are fast enough for most applications, so further improvement may not be required.

A. Proposed Approach

It was shown before that with increasing the total-time delay introduced by the *dq*CDSC operator in the control loop, the *dq*CDSC-PLL bandwidth should be reduced to ensure its stability. So, the PLL bandwidth (response time) can be increased (reduced) by compensating the delay introduced by the *dq*CDSC operator. To this end, we recommend to use a proportional-integral-derivative (PID) controller as the LF. Compared to the PI controller, the PID controller has an additional zero which enables the designer to further compensate the phase-delay in the control-loop.

The transfer function of the PID controller is considered of the form

$$\mathrm{PID}(s) = k_p \left(\frac{1+\tau_i s}{\tau_i s}\right)\left(\frac{1+\tau_d s}{1+\beta\tau_d s}\right) \tag{23}$$

where k_p is the proportional gain, and τ_i and τ_d are the integral and derivative time constants, respectively. Notice that the derivative action of the PID controller is filtered by a high frequency pole, i.e., $s = -1/(\beta\tau_d)$. For this reason, β ($\beta < 1$) is typically referred to as the derivative filter factor. The value of 0.1 is a typical choice for this factor.

B. Design Guidelines

As shown in (10), and repeated here for convenience, the open-loop transfer function of the *dq*CDSC-PLL is in general form as

$$G_{ol}(s) = \left.\frac{\hat{\theta}_1^+}{\theta_e}\right|_{D(s)=0} = V_1^+ dq\mathrm{CDSC}_{n_1,n_2,\ldots,n_m}(s)\mathrm{LF}(s)\frac{1}{s}. \tag{24}$$

By substituting $\mathrm{LF}(s) = \mathrm{PID}(s)$ into (24), and replacing the transfer function of *dq*CDSC operator with its first-order

approximation, we can obtain

$$G_{ol}^{\mathrm{PID}}(s) \approx V_1^+ \left(\frac{1}{T_d s+1}\right) k_p \left(\frac{1+\tau_i s}{\tau_i s}\right) \left(\frac{1+\tau_d s}{1+\beta\tau_d s}\right) \frac{1}{s} \tag{25}$$

where the superscript PID denotes that the PLL uses the PID-type LF.

From (25) it can be observed that the phase delay introduced by the *dq*CDSC operator can be compensated by selecting the derivative time constant τ_d equal to T_d. With this selection, and neglecting the derivative filter (which is a high frequency pole), (25) can be approximated by

$$G_{ol}^{\mathrm{PID}}(s) \approx V_1^+ k_p \left(\frac{1+\tau_i s}{\tau_i s^2}\right). \tag{26}$$

Using (26), the closed loop transfer function can be obtained as

$$G_{cl}^{\mathrm{PID}}(s) = \frac{G_{ol}^{\mathrm{PID}}(s)}{1+G_{ol}^{\mathrm{PID}}(s)} \approx \frac{V_1^+ k_p s + V_1^+ k_p/\tau_i}{s^2 + \underbrace{V_1^+ k_p}_{2\xi\omega_n} s + \underbrace{V_1^+ k_p/\tau_i}_{\omega_n^2}} \tag{27}$$

which is a standard second order transfer function, but with a zero. According to (27), the control parameters k_p and τ_i can be determined by selecting proper values for the damping factor ζ and natural frequency ω_n. In most literature $\zeta = 1/\sqrt{2}$ is recommended to achieve the best damping, while selection of ω_n depends on the required control bandwidth. Here the shortest possible response time (the widest possible bandwidth) is needed, so ω_n should be chosen as high as possible. The question that arises immediately is: how we should determine the upper limit for ω_n? The answer is: using the minimum required stability margin. In order to better visualize this fact, Fig. 11 shows the PM variations of the *dq*CDSC-PLL3, and *dq*CDSC-PLL4, and *dq*CDSC-PLL5 as a function of ω_n. The exact (no approximate) open-loop transfer functions of these PLLs are used to obtain these plots. As expected, for all PLLs the PM decreases as ω_n increases. So, the required stability margin limits the natural frequency ω_n.

Most often, a PM within the range of $30^\circ - 60^\circ$ is good enough to ensure the system stability. In this paper, a PM in the middle of this range, i.e., $\mathrm{PM} = 45^\circ$, is selected which corresponds to selecting $\omega_n = 2\pi 22.85$ rad/s, $\omega_n = 2\pi 21.92$ rad/s, and $\omega_n = 2\pi 10.5$ rad/s for the *dq*CDSC-PLL3 and *dq*CDSC-PLL4, and *dq*CDSC-PLL5, respectively.

The suggested design procedure can be summarized as follow

1) Select the derivative time constant τ_d equal to T_d.
2) Select $\beta = 0.1$.
3) Define $k_p = 2\zeta\omega_n/V_1^+$, and $\tau_i = 2\zeta/\omega_n$.
4) Select $\zeta = 1/\sqrt{2}$.
5) Select ω_n as high as possible without jeopardizing the PLL stability margin.
6) Calculate k_p and τ_i from definitions of step 3.

According to this design procedure, the control parameters of these PLLs can be calculated as summarized in Table VI.

Fig. 12 shows the open-loop Bode plots of the *dq*CDSC-PLL3, *dq*CDSC-PLL4, and *dq*CDSC-PLL5 when using the PID-type LF. By comparing these Bode plots with those shown in Fig. 5(c), (d), and (e), it can be observed that the PID-type LF makes it possible to achieve a higher bandwidth and therefore a faster transient response than that achievable using the PI-type LF without jeopardizing the PLL stability.

TABLE VI
DESIGNED VALUES FOR THE PLLS CONTROL PARAMETERS WHEN USING THE PID-TYPE LF.

	$k_p = 2\zeta\omega_n/V_1^+$	$\tau_i = 2\zeta/\omega_n$	$\tau_d = T_d$
*dq*CDSC-PLL3	203.04	0.00985	0.00458
*dq*CDSC-PLL4	194.77	0.01027	0.00469
*dq*CDSC-PLL5	93.3	0.02144	0.00969

C. Numerical Results

The effectiveness of the PID-type LF in improvement of the response time of the *dq*CDSC-PLL3, *dq*CDSC-PLL4, and *dq*CDSC-PLL5 is evaluated in this section. Similar to previous numerical study, the nominal grid frequency is set to 50 Hz, and the sampling frequency is fixed to 14.4 kHz.

Fig. 13 shows the numerical results when the grid frequency undergoes a frequency step change of +3 Hz. Table VII summarizes the obtained results. It can be observed that the PID-type LF reduces the settling times of all PLLs to almost half of those obtained using the PI-type LF (compare the results of table VII with those of table IV for frequency-step change test). So, effectiveness of PID-type LF in improvement of PLL response time is confirmed.

Unfortunately, the response time improvement brought by the PID-type LF is at the cost of degrading the filtering capability of the *dq*CDSC-PLL when the grid frequency deviation from its nominal value is high. To illustrate this fact, Fig. 14 shows the performance of PLLs under harmonically distorted grid conditions (see Table V for the parameters of distorted input voltage). The detailed results are summarized in Table VII.

According to these results, we recommend to use the PID-type LF in the *dq*CDSC-PLL3, *dq*CDSC-PLL4, and *dq*CDSC-PLL5 only when small variations in grid frequency is expected. For the case high variations in the grid frequency is expected, using the PID-type LF in these PLLs makes it necessary for them to have frequency-adaptive *dq*CDSC operators, which increases their complexity and computational burden due to the high number of *dq*DSCs they have in their *dq*CDSC operators.

VI. COMPARISON WITH MAF-PLL

To highlight the advantages/disadvantages of the *dq*CDSC-PLL, a detailed comparison between this PLL and MAF-PLL (SRF-PLL with in-loop MAF) is carried out in this section. First, a brief overview of MAF and MAF-PLL is presented.

A. Overview

MAF, also known as the rectangular window filter (RWF), can be described in s-domain as

$$\mathrm{MAF}(s) = \frac{1-e^{-T_w s}}{T_w s} \tag{28}$$

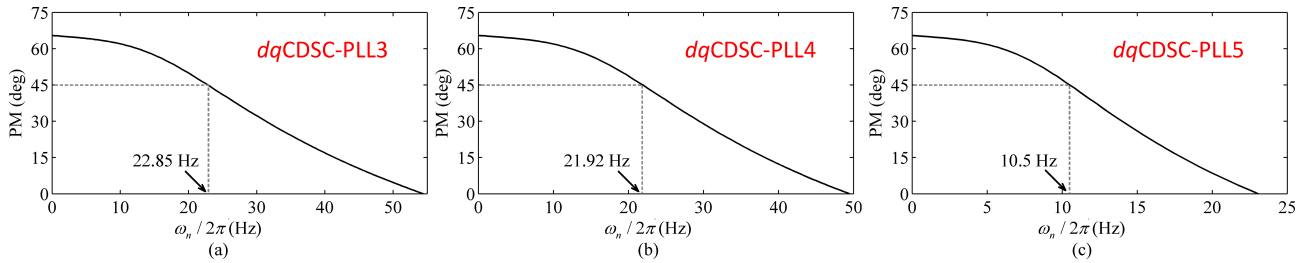

Fig. 11. PM variations of (a) *dq*CDSC-PLL3, and (b) *dq*CDSC-PLL4, and (c) *dq*CDSC-PLL5 as a function of ω_n.

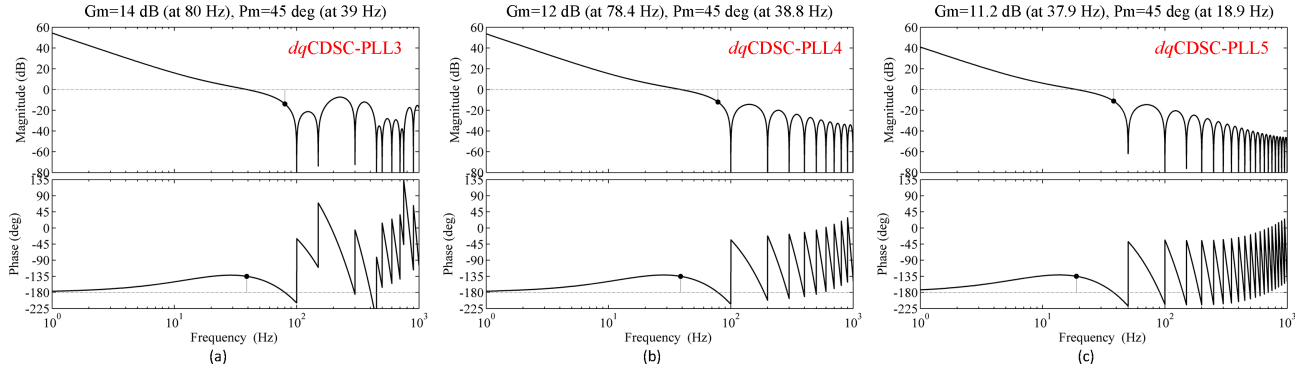

Fig. 12. Open loop Bode plots of (a) *dq*CDSC-PLL3, (b) *dq*CDSC-PLL4, and (c) *dq*CDSC-PLL5 when using the PID-type LF (see Table VI for parameters).

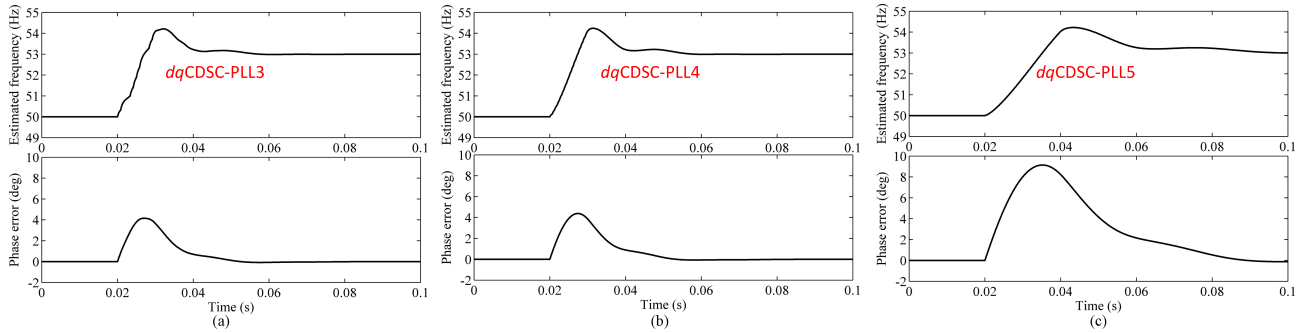

Fig. 13. Numerical results for (a) *dq*CDSC-PLL3, (b) *dq*CDSC-PLL4, and (c) *dq*CDSC-PLL5 when the grid voltage undergoes a frequency step change of $+3$ Hz. All PLLs use PID-type LF.

TABLE VII
SUMMARY OF RESULTS FOR *dq*CDSC-PLL3, *dq*CDSC-PLL4, AND *dq*CDSC-PLL5 WHEN USING PID-TYPE LF.

	*dq*CDSC-PLL3	*dq*CDSC-PLL4	*dq*CDSC-PLL5
Frequency step change of $+3$ Hz			
2% settling time	34.2 ms (1.71 cycles)	34.6 ms (1.73 cycles)	71.3 ms (3.56 cycles)
Frequency overshoot	1.21 Hz (40.33%)	1.22 Hz (40.67%)	1.21 Hz (40.33%)
Peak phase error	4.16°	4.37°	9.12°
Distorted grid condition			
Peak-to-peak phase error (freq.=49 Hz)	0.48°	0.17°	0.1°
Peak-to-peak phase error (freq.=47 Hz)	1.58°	0.5°	0.23°

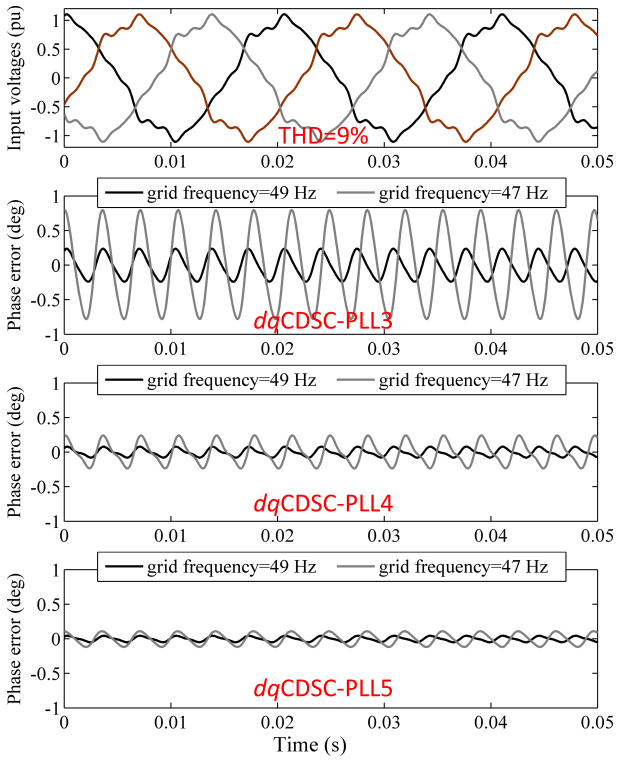

Fig. 14. Numerical results for *dq*CDSC-PLL3, *dq*CDSC-PLL4, and *dq*CDSC-PLL5 under harmonically distorted grid condition. All PLLs use PID-type LF.

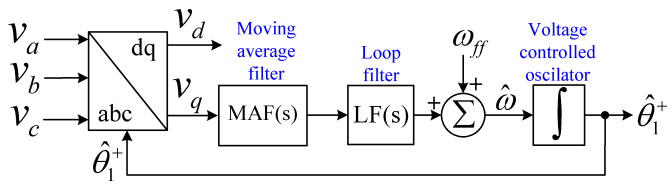

Fig. 15. Block diagram description of the MAF-PLL.

where T_w is the window length of MAF.

By substituting $s = j\omega$ into (28), and performing some simple mathematical manipulations, the magnitude and phase expressions of the MAF can be obtained as

$$\mathrm{MAF}(j\omega) = \left|\frac{\sin(\omega T_w/2)}{\omega T_w/2}\right| \angle -\omega T_w/2. \tag{29}$$

From (29), it can be noticed that the MAF provides unity gain at zero frequency and zero gain at frequencies $f = k/T_w$ ($k = \pm1, \pm2, \pm3, ...$) in hertz. It means that the MAF passes the dc component and completely blocks the frequency components of integer multiples of $1/T_w$ in hertz. Two different values for the MAF's window length are typically suggested: $T_w = T$ and $T_w = T/2$. The former blocks all harmonic components, and the latter blocks only even order harmonic components.

Incorporating the MAF into the PLL control-loop has been recommended in many literature [15]-[20]. The block diagram description of the MAF-PLL is shown in Fig. 15. Notice that the MAF-PLL is exactly the same as the *dq*CDSC-PLL (see Fig. 2), but the *dq*CDSC operator is replaced with MAF. It is shown in next section that the MAF-PLL and *dq*CDSC-PLL are equivalent under certain conditions.

B. Equivalence of dqCSDC-PLL and MAF-PLL

From trigonometric identities, we know that

$$\begin{aligned}
&\sin(X) = 2\sin(X/2)\cos(X/2)\\
&\sin(X/2) = 2\sin(X/4)\cos(X/4)\\
&\vdots\\
&\sin(X/2^{m-1}) = 2\sin(X/2^m)\cos(X/2^m)
\end{aligned} \tag{30}$$

where X is an arbitrary signal, and m is a positive integer. Using (30), $\sin(X)$ can be expressed as

$$\begin{aligned}
\sin(X) &= 2^m \sin(X/2^m)\left[\cos(X/2)\cos(X/4)\ldots\cos(X/2^m)\right]\\
&= \underline{2^m \sin(X/2^m)} \prod_{i=1}^{m} \cos(X/2^i).
\end{aligned} \tag{31}$$

As m tends to infinity, the underlined term in (31) tends to X. According to this, (31) can be rewritten as

$$\frac{\sin(X)}{X} = \prod_{i=1}^{\infty} \cos(X/2^i) \tag{32}$$

and therefore

$$\left|\frac{\sin(X)}{X}\right| = \prod_{i=1}^{\infty} \left|\cos(X/2^i)\right|. \tag{33}$$

Using (33), and considering that the arbitrary signal X can be expressed as a geometric progression with a factor of $1/2$, i.e.,

$$\underbrace{X/2 + X/4 + X/8 + \ldots}_{\sum_{i=1}^{\infty} X/2^i} = \frac{X/2}{1-1/2} = X \tag{34}$$

we can obtain

$$\left|\frac{\sin(X)}{X}\right| \angle -X = \prod_{i=1}^{\infty} \left\{\left|\cos\left(X/2^i\right)\right| \angle -\left(X/2^i\right)\right\}. \tag{35}$$

Substituting $X = \omega T_w/2$ into (35), yields

$$\begin{aligned}
&\overbrace{\left|\frac{\sin(\omega T_w/2)}{\omega T_w/2}\right| \angle -(\omega T_w/2)}^{\mathrm{MAF}(j\omega)}\\
&\quad = \prod_{i=1}^{\infty} \left\{\left|\cos\left(\omega T_w/2^{i+1}\right)\right| \angle -\left(\omega T_w/2^{i+1}\right)\right\}.
\end{aligned} \tag{36}$$

Notice that the left hand side of (36) is the same as (29).

As mentioned before, there are two typical choices for MAF window length: 1) $T_w = T$, and 2) $T_w = T/2$. These two cases are examined in the following.

By substituting $T_w = T$ into (36), and considering the magnitude and phase expressions of *dq*DSC operator in (3), we can obtain

$$\mathrm{MAF}(j\omega)|_{Tw=T} = \prod_{i=1}^{\infty} dq\mathrm{DSC}_{2^i}(j\omega) \tag{37}$$

or equivalently

$$\mathrm{MAF}(s)|_{Tw=T} = dq\mathrm{CDSC}_{2,4,8,16,32,\cdots}(s) \tag{38}$$

which means the MAF with window length of $T_w = T$ is mathematically equivalent with $dq\mathrm{CDSC}_{2,4,8,16,32,\ldots}$ operator.

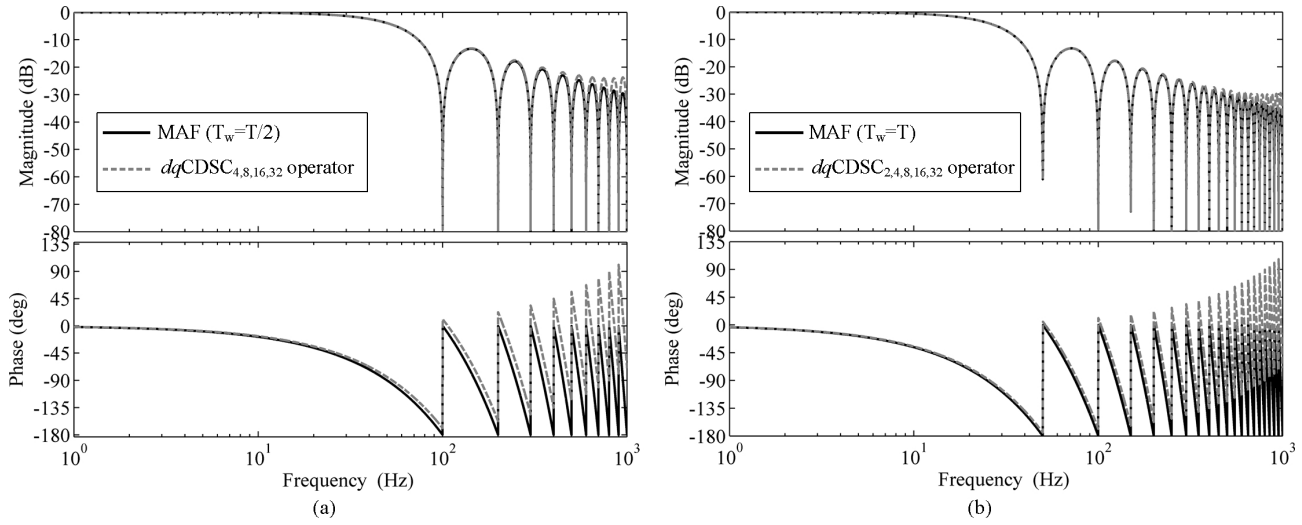

Fig. 16. Bode plots of (a) MAF ($T_w = T/2$) and $dq\mathrm{CDSC}_{4,8,16,32}$ operator, and (b) MAF ($T_w = T$) and $dq\mathrm{CDSC}_{2,4,8,16,32}$ operator.

Following a similar manner it can be shown that the MAF with window length of $T_w = T/2$ is mathematically equivalent with $dq\mathrm{CDSC}_{4,8,16,32,\cdots}$ operator. In order to illustrate this fact, Fig. 16(a) compares the Bode plots of MAF ($T_w = T/2$) and $dq\mathrm{CDSC}_{4,8,16,32}$, and Fig. 16(b) compares the Bode plots of MAF ($T_w = T$) and $dq\mathrm{CDSC}_{2,4,8,16,32}$ operator. As expected, they have a close frequency response.

According to above analysis, it can be concluded that the *dq*CDSC-PLL4 (which uses the $dq\mathrm{CDSC}_{4,8,16,32}$ operator) is practically equivalent to MAF-PLL($T_w = T/2$), and the *dq*CDSC-PLL5 (which uses the $dq\mathrm{CDSC}_{2,4,8,16,32}$ operator) is practically equivalent to MAF-PLL($T_w = T$).

C. Numerical Results and Comparison

In previous section, the equivalence of *dq*CDSC-PLL4 and MAF-PLL($T_w = T/2$), and equivalence of *dq*CDSC-PLL5 and MAF-PLL($T_w = T$) was shown through a mathematical analysis. To verify this finding, some numerical results are presented in this section. In all PLLs, the PI controller is considered as the LF. The PI controller's gains for *dq*CDSC-PLL4 and *dq*CDSC-PLL5 can be found in Table III. The PI controller's gains for MAF-PLL($T_w = T/2$) and MAF-PLL($T_w = T$) are the same as those for *dq*CDSC-PLL4 and *dq*CDSC-PLL5, respectively.

Fig. 17 shows the numerical results when the grid voltage undergoes a phase-angle jump of $40°$. As expected, the *dq*CDSC-PLL4 and MAF-PLL($T_w = T/2$), as well as the *dq*CDSC-PLL5 and MAF-PLL($T_w = T$) show well-matched results. Similar well-matched results can be obtained under distorted and unbalanced grid conditions, however these results are not shown here for the sake of brevity.

It is worth mentioning that from the computational effort point of view there is also no appreciable difference between the *dq*CDSC-PLL4 and MAF-PLL ($T_w = T/2$) and between the *dq*CDSC-PLL5 and MAF-PLL ($T_w = T$).

D. Discussion

To highlight the advantages/disadvantages of the *dq*CDSC-PLL compared to the MAF-PLL, some issues are discussed in this section.

As mentioned before, to realize the *dq*CDSC with DSP in practice, the T/n_i ($i = 1, 2, \cdots, m$) signal delays in cascaded units are realized by buffering $N_i = (T/n_i)/T_s$ samples in DSP memories. In practice, it is almost impossible to make every N_i ($i = 1, 2, \cdots, m$) in cascaded *dq*DSC operators an integer as the DSP sampling frequency is determined by factors other than the *dq*CDSC-PLL operator. For example, if the *dq*CDSC-PLL operator is a part of the control of a grid-connected voltage source converter (VSC), factors such as the pulse width modulation (PWM) scheme, switching losses, etc. determines the sampling frequency [28]. In such a case, every non-integer N_i should be rounded to the nearest integer which results in discretization error. Another approach is to use the linear interpolation method, reducing the discretization error at the cost of increased computational effort [28], [29].

Contrary to the *dq*CDSC operator, realization of MAF does not require multiple time delays with different lengths (there is only one time delay with length of T_w). So, it is more likely to achieve an ideal discretization in implementation of MAF with a given sampling frequency. It is the main advantage of MAF over *dq*CDSC operator and therefore the MAF-PLL over the *dq*CDSC-PLL.

The *dq*CDSC operator (*dq*CDSC-PLL) offers much higher design flexibility than the MAF (MAF-PLL). The reason is that in designing the MAF there is only one degree of freedom (i.e., the MAF window length), while in designing the *dq*CDSC operator there are multiple degrees of freedom (i.e., number of cascaded *dq*DSC operators and their delay factors). Thanks to this flexibility, the designer can avoid unnecessary computational effort and achieve the shortest possible response time in some grid scenarios, particularly when selective cancellation of some specific disturbance components in the PLL control loop is required. It is the main advantage of *dq*CDSC operator over the MAF and therefore the *dq*CDSC-PLL over the MAF-

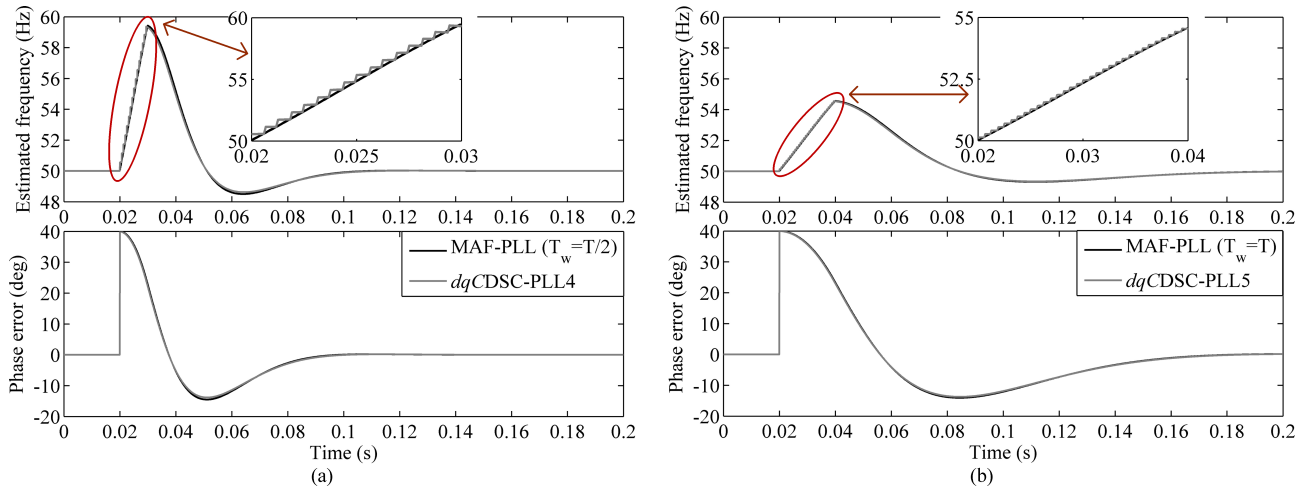

Fig. 17. Numerical results for (a) *dq*CDSC-PLL4 and MAF-PLL($T_w = T/2$), and (b) *dq*CDSC-PLL5 and MAF-PLL($T_w = T$) when the grid voltage undergoes a phase angle jump of $+40°$.

PLL.

VII. Conclusion

In this paper, a systematic approach to fine tune the control parameters of *dq*CDSC-PLL (when PI-type LF is used in the PLL) is proposed. This approach, which is based on approximating the dynamics of *dq*CDSC operator with a firdt-order LPF and using the SO method, has a general theme so it can be applied to different versions of the *dq*CDSC-PLL. Then, through extensive numerical results, the performance of different versions of *dq*CDSC-PLL under different grid scenarios are examined. These results provide a helpful insight for designer about the advantages/disadvantages of different versions of *dq*CDSC-PLL for their specific application.

To further improve the response time of some versions of *dq*CDSC-PLL, using the PID controller (instead of the PI controller) as the LF is suggested. A systematic approach to design the control parameters is then proposed. Through Bode plots and numerical results, it is shown that the PID-type LF enables the *dq*CDSC-PLL to obtain a higher bandwidth (and therefore a faster transient response) than that achievable using the PI-type LF. However, this improvement is at the cost of degrading the filtering capability of *dq*CDSC-PLL when large variations in grid frequency happen. So, we recommend to use the PID-type LF only when small variations in grid frequency expected.

To further highlight the advantages/disavantages of *dq*CDSC-PLL, a detailed comparison between this PLL and MAF-PLL is carried out. It is shown that the *dq*CDSC-PLL offers a higher design flexibility than the MAF-PLL, however it may suffer from discretization error (due to non-ideal sampling frequency) in some practical cases. Through a detailed mathematical analysis it is also shown that the *dq*CDSC-PLL and MAF-PLL are equivalent under certain grid conditions. This finding is also confirmed through some numerical results.

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