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Wu, Rui; Iannuzzo, Francesco; Wang, Huai; Blaabjerg, Frede

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An Icepak-PSpice Co-Simulation Method to Study the Impact of Bond Wires Fatigue on the Current and Temperature Distribution of IGBT Modules under Short-Circuit

Rui Wu, *Student Member, IEEE*, Francesco Iannuzzo, *Senior Member, IEEE*, Huai Wang, *Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

Centre of Reliable Power Electronics (CORPE), Department of Energy Technology
Aalborg University, Pontoppidanstraede 101, 9220
Aalborg, Denmark
rwu@et.aau.dk, fia@et.aau.dk, hwa@et.aau.dk, fbl@et.aau.dk.

Abstract— Bond wires fatigue is one of the dominant failure mechanisms of IGBT modules. Prior-art research mainly focuses on its impact on the end-of-life failure, while its effect on the short-circuit capability of IGBT modules is still an open issue. This paper proposes a new electro-thermal simulation approach enabling analyze the impact of the bond wires fatigue on the current and temperature distribution on IGBT chip surface under short-circuit. It is based on an Icepak-PSpice co-simulation by taking the advantage of both a finite element thermal model and an advanced PSpice-based multi-cell IGBT model. A study case on a 1700 V/1000 A IGBT module demonstrates the effectiveness of the proposed simulation method.

I. INTRODUCTION

In modern power electronics systems, there are increasing demands to improve whole system endurance and safety level while reducing manufacturing and maintenance costs caused by degradations [1], especially the ones where maintenance costs are very high or the applications are critical, e.g. in MW-level wind turbine systems [2]. According to questionnaires for manufacturers, semiconductor devices are considered as the most critical and fragile component in industrial power electronic systems [3]-[4]. Based on another survey, semiconductor failure and soldering joint failure in power devices take up 34% of power electronic system failures [5]. Because Insulated Gate Bipolar Transistors (IGBTs) are one of the most critical components as well as the most widely used power devices in industrial power electronic systems in the range above 1 kV and 1 kW [5], the reliability of IGBTs has drawn more and more attention.

Power module is the most used packaging for IGBTs in modern medium and high power applications. In multichip IGBT modules there are typically up to 800 wedged bond

wires, and half of them are bonded onto the active area, which means they are exposed to almost the full temperature swing introduced by both the silicon (Si) chip power dissipation and wire's ohmic self-heating. Therefore, bond wires fatigue, including lift-off and heel cracking, is a common failure mechanism for IGBT modules [6], [10]-[13]. Besides, bond wires fatigue could occurs together with reconstruction of chip surface aluminium (Al) metallization, which in turn unavoidably degrades the IGBT performance, for instance altering current and temperature distributions [7]. These degradations can lead to emitter resistance variation and further hot spots during operation. Based on this analysis, the chip emitter resistance network can be used to model the electrical degradation, which contains bond wire resistance and emitter metallization resistance.

Accurate prediction of the impact of bond wires fatigue on current and temperature distributions within the entire IGBT chip under both normal operation and short-circuit, is critical to avoid potential failures and design robust and reliable power electronic systems. Some experimental measurements, like high speed infrared thermography, can provide spatial temperature distributions, but they demand special and expensive equipment and hardly help to characterize the current distributions through the chip [8]. On the other hand, simulation tools, especially multi-disciplinary design platforms, provide good possibilities to predict such phenomena with detailed electrical and thermal simulations [9].

As clearly mentioned in the previous literatures [10]-[13], bond wires fatigue can lead to IGBT electrical and thermal behaviour degradations. However, all these work have not studied the consequent IGBT performance degradation, for instance current or temperature imbalanced distribution after bond wires fatigue. An electro-thermal

model is proposed to study IGBT top-metal ageing effects under short-circuit in [14], by which the current distribution can be achieved but not detailed temperature map because of using lumped thermal impedance network. In order to study the ageing effects caused by bond wires fatigue, a co-simulation with both physical-based electrical and thermal models is needed.

So far, most electro-thermal co-simulations are aimed at integrated circuit simulations and optimizations, which are hard to extend to power semiconductor study because advanced electrical models are absent [15], [16]. Some researchers attempted to extend widely-used electrical simulation tools for power semiconductors (e.g. Spice, Saber) to electro-thermal simulations by introducing lumped thermal impedance. However, this method cannot provide accurate temperature distribution and hot spots caused by fatigue and degradation in power semiconductors, because the intrinsic nodes of such tools are limited to few thousands [17]-[19]. Similarly, a compact electrical model can be integrated with a distributed 3D mathematical description of thermal phenomena [20], [21], which can reduce the computing time but also the accuracy. Another method is connecting Finite Element Method (FEM) thermal simulation e.g. Icepak [22] to circuit-level simulator Simplorer [23] in ANSYS. Icepak can generate thermal impedance network for Simplorer, but this process is unidirectional and lack of interaction between two simulators. What is more, a lot of information is unavoidably omitted by this intrinsically-single-cell approximation method, e.g. junction temperature distribution and hot spots dynamics in the semiconductor chips, which strongly limit the prediction of imbalances among the cells of the real device especially under abnormal conditions (e.g. short-circuit, overload).

This paper proposes a novel perspective for electro-thermal co-simulation, which connects a physics-based, device-level, distributed electrical simulation tool with a thermal FEM simulation, to obtain high accuracy on both the electrical side and the thermal side. It can also gain another advantage - independent time steps can be adopted for the electrical and thermal parts, thus gaining improved calculation efficiency. A physics-based IGBT model in PSpice is adopted, since it has shown accurate results, high modularity and fast simulating speed, which is suitable to simulate normal as well as abnormal conditions [24]. In order to model the bond wires fatigue and Al layer reconstruction, an emitter resistance network is introduced to the electrical model.

This paper is organized as follows: Section II describes the detailed procedures of the approach, including model preparation and supervision scripts. Section III applies the proposed method to study the bond wires fatigue influences on current and temperature distribution of IGBT power modules. Firstly, the detailed information of the commercial 1700 V/1000 A IGBT module is given. Secondly, the corresponding lumped charge IGBT model is built and calibrated in PSpice. Thirdly, the detailed thermal model

with accurate material parameters is constructed in Icepak. Then the proposed co-simulation approach is applied for a critical 10 μ s short-circuit at 1 kV for a new IGBT module. Simulation results are shown in section IV. The obtained current and temperature distributions demonstrate the efficiency and effectiveness of the method. Furthermore, electro-thermal co-simulation in the case of bond wires fatigue is implemented under the same short-circuit condition, which evidences the new approach's capabilities. Section V gives concluding remarks and recommendations for further ageing effects simulations in future.

II. PRINCIPLES OF ELECTRO-THERMAL ICEPAK-PSPIICE CO-SIMULATION

The proposed electro-thermal co-simulation method includes three major parts: IGBT electrical model in PSpice, IGBT thermal analysis model in the FEM software ANSYS/Icepak, and a supervising MATLAB script. Based on the PSpice electrical simulation, a map of current and power loss map inside the chip is obtained and sent to the ANSYS thermal simulation, and then ANSYS/Icepak thermal simulation feeds back the temperature map to the PSpice electrical simulation, so finally the chip temperature map can be achieved. The co-simulation process is shown in Fig. 1, of which the details will be illustrated as follows.

A. Circuit file Preparation

Before the co-simulation, the user defines the desired simulation profile. Sample simulation profiles are: normal operation, overload and short-circuit. Then, the IGBT model is automatically generated as a PSpice circuit containing an arbitrary number of IGBT cells with an emitter resistance network, as shown in Fig. 2.

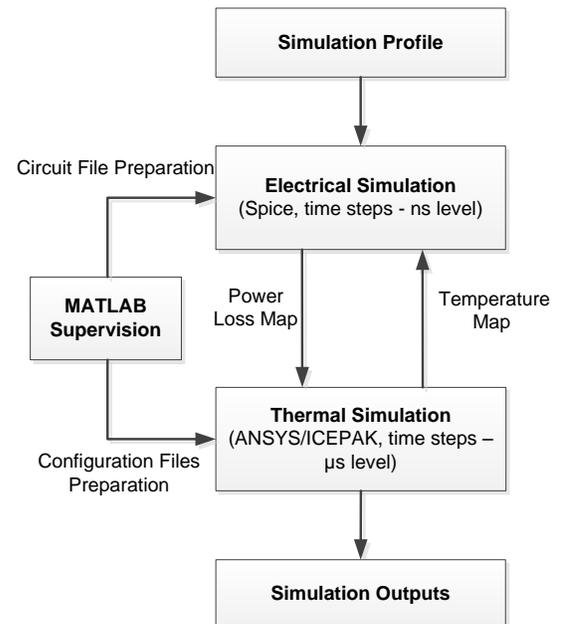


Fig. 1. Structure of the proposed electrical-thermal co-simulation.

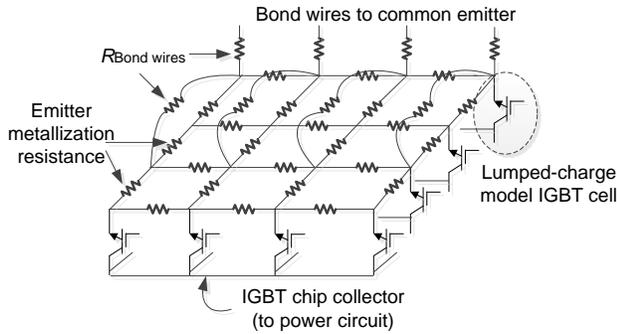


Fig. 2. IGBT chip electrical model with emitter resistance network.

The emitter resistance network represents the bond wire and the Al metallization layer resistance. It is used to reflect the electrical degradation as well as predict the consequent thermal effects.

Each IGBT cell model is scaled with a physics-based lumped charge IGBT model, which demonstrated an improved accuracy and comparable simulation speed for high voltage IGBTs than widely used classical PSpice model [24]. A few parameters are required to identify the model, which can be obtained from the datasheets and manufacturers: chip area, stray resistance, stray inductance, and gate capacitances.

With all the aforementioned information defined, a PSpice circuit file is generated by the MATLAB supervision script before the co-simulation starts.

B. Icepak Model Preparation

A detailed Icepak geometry model is necessary for thermal simulation. The schematic cross-section structure and materials of typical IGBT power module are shown in Fig. 3. From top to bottom, typical IGBT module contains: Al layer, Si chip, solder for chip, Direct Copper Bonded (DCB) layers, solder for baseplate and Copper (Cu) baseplate. Both the geometry and material properties should be precisely described in Icepak.

All geometry and material information are defined in the Icepak “model” file. It also includes the power loss information before simulation, which will be updated by the PSpice electrical simulation during co-simulation processes.

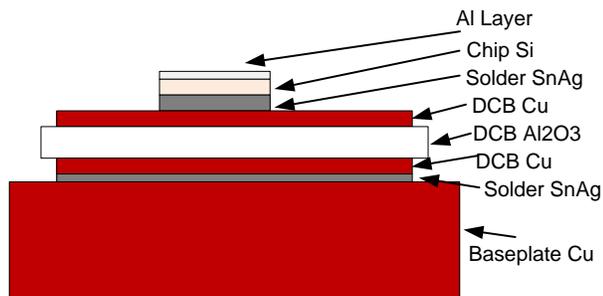


Fig. 3. Schematic cross-section of the multilayers in a typical IGBT power module.

All thermal simulation setting information is included in the Icepak “problem” file. It defines thermal simulation step and ending time. The monitoring points are set for each IGBT cell, which can record the temperature information after each thermal simulating step. The temperature map will be fed back later to the next electrical simulation in PSpice. The locations of these points are also included in the “problem” file.

After the “model” and “problem” files have been defined by MATLAB supervision script, the co-simulation is started.

C. MATLAB Script

A MATLAB script is implemented to prepare configuration files in the preparation state and then coordinate information sharing at each thermal simulation step for the above two packages. Operations are divided as preparation state and simulation state.

At the preparation state, the MATLAB script automatically divides the device under simulation (i.e. the IGBT) into a specific number of virtual cells, which should be rectangle-shaped. Each cell includes one power source and one temperature monitoring point, which are placed in the IGBT body. One PSpice sub-circuit is automatically generated for each cell starting from a circuit template file, that includes the parameter identified for the considered device, and all of them are connected in parallel. The user should also define external PSpice circuit profile as normal operation, overload or short-circuit.

At the simulation state, the power loss of each cell is calculated by the PSpice circuit with time resolution of nanoseconds for a given constant temperature map. The PSpice simulation lasts a thermal time step (typically in the range of microseconds) and it is stopped. At this point, dissipated power losses are given to the thermal simulation – the corresponding files in Icepak are updated accordingly, and the thermal simulation in Icepak is then done. Afterwards, the temperature data are transferred back to the PSpice model and so forth.

III. CO-SIMULATION FOR BOND WIRES FATIGUE OF A COMMERCIAL IGBT MODULE

In order to illustrate the proposed PSpice-Icepak co-simulation method, a case study of a 1700 V/1000 A commercial IGBT module is given in this section. First, the IGBT module information is introduced. Then, the co-simulation configuration is explained in details, including: simulation profile definition, electrical model and thermal model configurations, as well as MATLAB supervision configuration.

A. Information about the Studied IGBT Module.

The main specifications of the IGBT module are shown in Table I. It worth noting that rated short-circuit current is 4 kA. The chips are soldered on a standard DCB layer, which is further soldered to a Cu baseplate, and the cross section is the same as the structure shown in Fig. 3. The high current rating is achieved by six identical sections connected in

TABLE I MAIN SPECIFICATIONS OF THE IGBT MODULE UNDER SIMULATIONS.

Characteristic	Value
Collector-emitter voltage V_{CES}	1700 V
Continuous DC collector current I_{Cnom}	1000 A
Rated short-circuit current I_{SC}	4000 A
Gate-emitter maximum voltage V_{GES}	+/- 20V
Internal gate resistance	4 Ω
Number of parallel sections	6

parallel inside the module. An open power module with an internal structure is shown in Fig. 4.

Each section includes two IGBT chips and two freewheeling diode chips, which are configured as a half-bridge. Ten Al bond wires connect each IGBT chip emitter and the freewheeling diode chip anode. A detailed picture of one section is shown in Fig. 5.

B. Co-simulation Configuration for the IGBT Module.

In order to study the bond wires fatigue effects on abnormal conditions, one section of the power module is selected for electro-thermal simulation (as shown in Fig. 5). The details of the co-simulation configuration are illustrated as follows.

1) Simulation Profile Definition.

As is well known, the most critical abnormal working condition for IGBTs is short-circuit, where both high voltage and high current are applied to the device at the same time.



Fig. 4. Geometry of the 1.7 kV/1 kA IGBT power module with six sections in parallel.

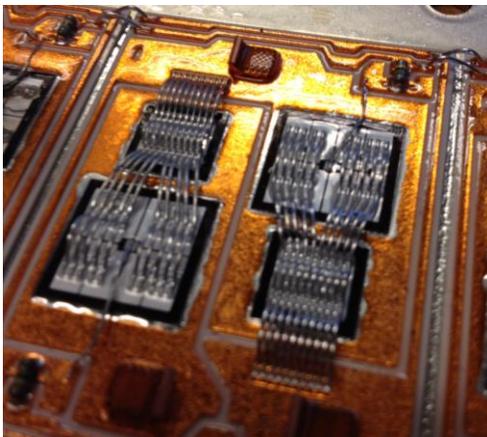


Fig. 5. One section of the studied IGBT power module.

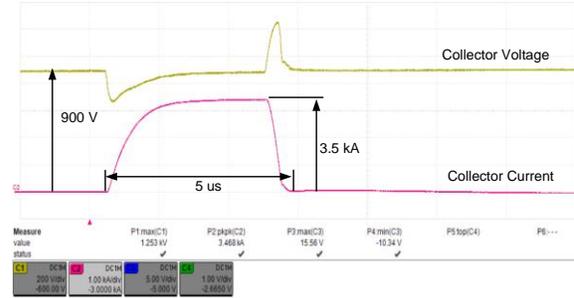


Fig. 6. Experimental collector voltage and current waveforms during a 900 V short-circuit (200 V/div; 1 kA/div) for the IGBT module at room temperature 25 $^{\circ}$ C.

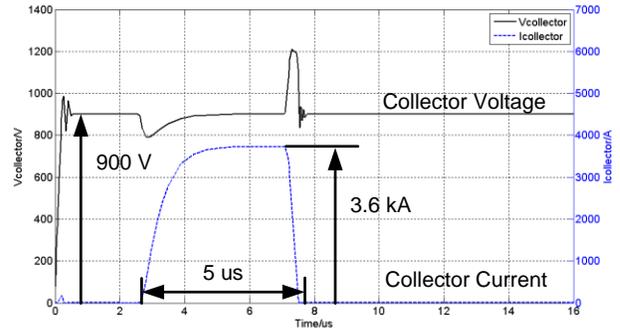


Fig. 7. Short-circuit simulation waveforms of studied IGBT module lumped charge model in PSpice (short-circuit current 3.6 kA at 900 V, room temperature at 25 $^{\circ}$ C).

Therefore, a standard 10 μ s short-circuit duration is chosen in the case study, with a thermal simulation step of 1 μ s. It is worth to note that the diodes do not operate in this case study.

2) Electrical Model Configuration.

In the electrical model, the studied IGBT chip is divided into 4 by 4 cells. According to the information from manufacturer, the IGBT module's stray inductance is 10 nH, its gate capacitance is 81 nF, while the IGBT chip is 12.6 mm by 12.6 mm square size. Based on the datasheet information, corresponding IGBT lumped charge model can be obtained according to the method in [24].

In order to calibrate the model, a comparison between simulation and experiments has been executed. A 5 μ s short-circuit test at 900 V for the studied power module has been performed in the laboratory at room temperature (25 $^{\circ}$ C). The short-circuit current finally reaches 3.5 kA. Experimental collector voltage/current waveforms are shown in Fig. 6. Due to the test circuit stray inductance, it is observed the collector voltage undershoot and overshoot at the starting and end of the short-circuit operation, respectively.

A short-circuit simulation under the same conditions is performed in PSpice with the built IGBT lumped charge model at room temperature. Short-circuit current also reaches 3.5 kA at 900 V, and the collector voltage/ current waveforms are shown in Fig. 7. The results prove that the

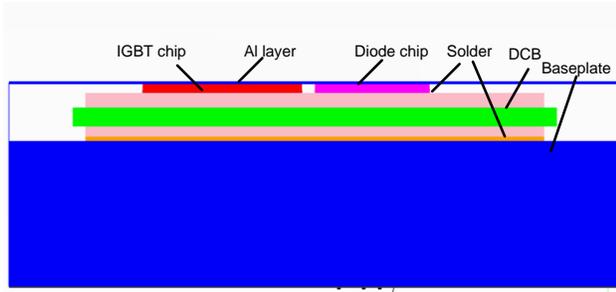


Fig. 8. Details of the IGBT module cross section on the vertical plane.

lumped charge model is sufficiently accurate for the short-circuit study.

3) Thermal Model Configuration.

Based on the information provided by the IGBT manufacturer, one IGBT section model is constructed in Icepak for thermal simulation.

The geometry in Icepak is the same as shown in Fig. 5. The cross section of the Icepak model is shown in Fig. 8. It contains Al top layer, IGBT trench gate layer, IGBT body layer, solder, DCB and baseplate. Power source is located in the IGBT body layer. 543,000 nodes are defined in Icepak model.

TABLE II IGBT MODULE MATERIAL THERMAL PROPERTIES AT 25 °C [25].

Material	Al	Si	Solder	Cu
Thermal Conductivity (W/m-K)	237	148	57	401
Heat Capacity (J/Kg-K)	897	705	220	385

TABLE III MATERIALS THERMAL PROPERTIES AT DIFFERENT TEMPERATURE [25].

Temperature		25 °C	75 °C	125 °C	225 °C	325 °C
Si	Thermal Conductivity (W/m-K)	148	119	98.9	76.2	61.9
	Heat Capacity (J/Kg-K)	705	757.7	788.3	830.7	859.9
Al	Thermal Conductivity (W/m-K)	237	240	240	236	231
	Heat Capacity (J/Kg-K)	897	930.6	955.5	994.8	1034
Cu	Thermal Conductivity (W/m-K)	401	396	393	386	379
	Heat Capacity (J/Kg-K)	385	392.6	398.6	407.7	416.7

The thermal conductivity and heat capacity information of the materials used in the simulations at 25 °C are listed in Table II.

However, the thermal parameters are also strongly dependent on temperature, as reported in Table III for thermal conductivity and specific heat of the materials (Si, Al, Cu) [25], [26]. Based on this, it is clear that the power module thermal behavior depends directly on the local temperature [27]. This point is very critical for overload and short-circuits analysis, where the chip temperature rises dramatically, even if for limited time duration (in the range of several milliseconds). Therefore, this nonlinear temperature behavior has also been included in the used Icepak model to improve the simulation accuracy.

4) MATLAB Supervision Configuration.

All the above electrical/ thermal settings are configured in MATLAB script. Besides, the bond wires fatigue information can also be defined: weak cells with higher emitter resistance caused by bond wires lift-off, healing crack or Al layer destruction. The weak cells location and resistance variation can be defined in MATLAB during the preparation state.

IV. CO-SIMULATION RESULTS

A. Short-circuit Simulation in Non-degraded Conditions

1) General Settings.

At first, the short-circuit simulation is implemented for a new IGBT module, with no bond wires degradation for the module. The total simulation duration is 18 μ s, with 18 thermal steps (1 μ s each). The short-circuit happens at 1 kV voltage. The short-circuit operation lasts 10 μ s, from 3 μ s until 13 μ s.

For the electrical simulation, the calibrated IGBT lumped charge model is used, and the chip has been divided into 4 by

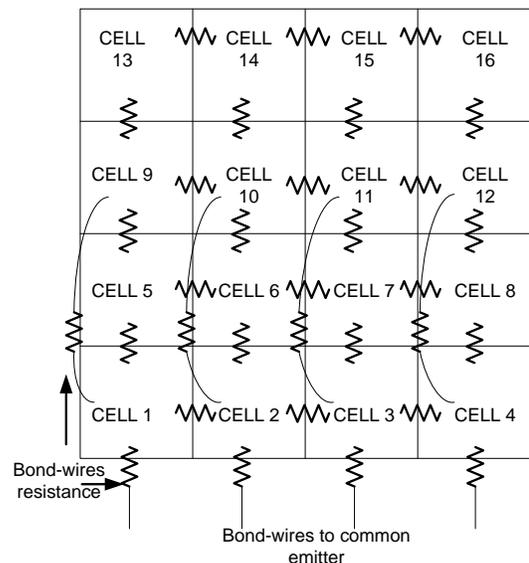


Fig. 9. IGBT cells and emitter resistance network definition for the simulation.

4 cells. Cells and emitter resistance network definition is as shown in Fig. 9. External emitter is directly connected to cell 1-4 by bond wires. Cells 9-12 are contacted to cells 1-4 by bond wires, and then to external emitter. The other cells are connected by Al layer network on the chip top.

The Icepak model in section III is used for thermal analysis. It is worth noting that the parameters in Table II and Table III are described in the model, which is essential for temperature analysis under short-circuit simulation due to aforementioned reason.

2) Electrical Simulation Results.

When short-circuit happens during IGBT turn-on (at 3

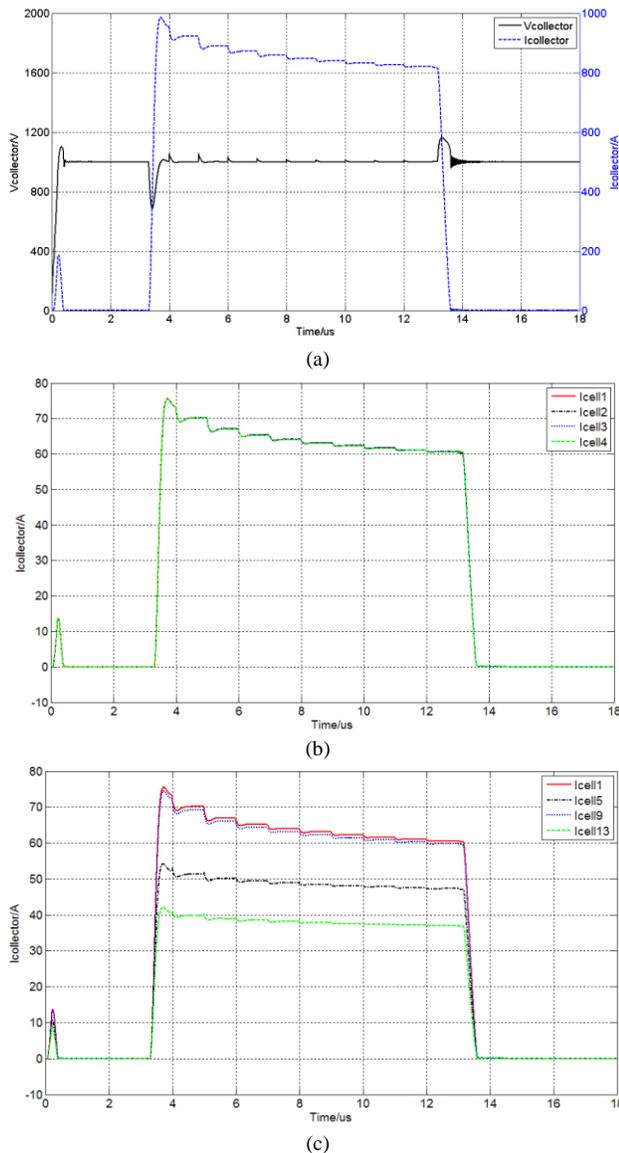


Fig. 10. PSpice simulation results of the new module: (a) Short-circuit current/voltage waveforms of the whole IGBT chip; (b) current distribution among cells close to external emitter (cell 1, cell 2, cell 3, and cell 4 in Fig.9); (c) current distribution among cell 1, cell 5, cell 9, and cell 13 in Fig.9.

μs), collector current I_c rises rapidly until reaching the saturated value of 900 A. The PSpice simulation results are plotted in Fig. 10 (a).

According to the semiconductor physics, IGBT short-circuit current decreases with the junction temperature rising [6]. This phenomenon is also evidenced in the simulation, as shown in Fig. 10 (a). Because the IGBT cells temperature is updated every thermal step – 1 μs, the short-circuit current also decreases by 1 μs step. As introduced in Section II, part B, the thermal step duration can be modified in the MATLAB script according to requirements.

The current distribution among cells can be also observed through the co-simulations.

In Fig. 9, it is clearly shown that cells 1-4 are connected directly to external emitter by the bond wires. The current distribution among these cells is plotted in Fig. 10 (b), which is uniform.

It can be found the IGBT chip bond wires configuration in the geometry figure in Fig. 5 and the corresponding setting in Fig. 9: cell 1 is connected to the external emitter by bond wire, cell 9 is connected to cell 1 by bond wire, and there is no direct emitter bond wires for cell 5 and cell 13 (they are connected through Al metallization). Therefore, it can be expected that cell 1 has best emitter contact, followed by cell 9, cell 5, while cell 13 has worst emitter contact.

It is demonstrated by the current distribution among cell 1, cell 5, cell 9 and cell 13 in Fig. 10 (c). The currents through cell 1 and cell 9 are higher than the currents through cell 5 and cell 13, and cell 13 has lowest current.

3) Thermal Simulation Results.

Four chip temperature maps obtained during short-circuit

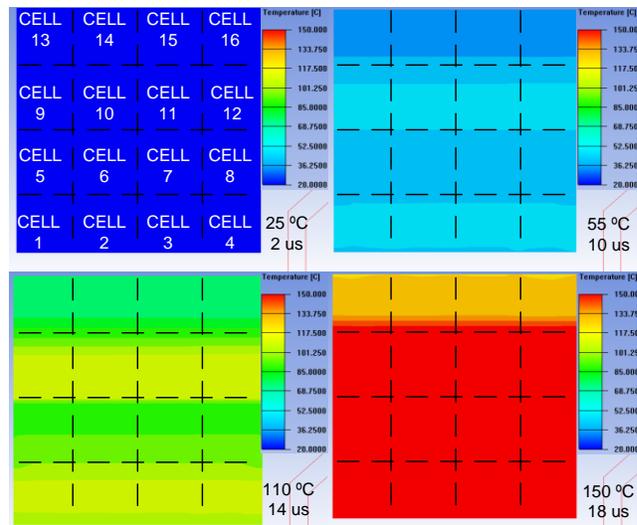


Fig. 11. New IGBT module chip temperature map in Icepak during short-circuit at 2/10/14/18 μs (times and highest temperature at bottom right of each image) (Temperature color bar – max 150 °C, min 20 °C).

are reported in Fig. 11. They are before short-circuit (at 2 μ s), during short-circuit (at 10 μ s), after short-circuit (at 14 μ s and 18 μ s) respectively.

In the case of non-degraded conditions, temperature rises almost uniformly on the whole chip, but still some differences can be observed. This is because of the not perfectly equal current distribution among cell, as clearly shown in Fig. 10 (c).

Before short-circuit, the chip is at room temperature (25 $^{\circ}$ C) (as shown in the first picture at 2 μ s). During short-circuit (at 10 μ s): cells under bond wires (cells 1-4 and cells 9-12) are about 5 $^{\circ}$ C hotter than other ones because of the imbalanced current. After the turn-off of short-circuit, the temperature keeps rising due to the heat flow from the Si layer. IGBT chip's temperature rises as high as 150 $^{\circ}$ C at 18 μ s due to the high energy shock in these conditions.

B. Short-circuit Simulation of One Bond Wires Fatigue.

1) General Settings.

In the presence of bond wires fatigue, the degraded emitter bond wire has poorer contact and higher resistance than the other bond wires. In the case study, emitter resistance network is set as follows: the lower-left corner cell (cell 1 in Fig. 9) has tens of k Ω -level emitter bond-wire contact resistance, which represents bond wire lift-off, while

normal bond wire contact resistance is at m Ω level.

To compare the results with new module, all the other settings in PSpice and Icepak are kept the same as the simulation in section IV, part A.

2) Electrical Simulation Results.

When short-circuit happens during IGBT turn-on (at 3 μ s), collector current I_c rises rapidly until reaching saturated value.

Due to the lifted bond wire on the top of cell 1, the current distribution among cells is redistributed, of which the cell 1 has lower current stress compared to that in the new module. As shown in Fig. 12 (a), the cell 1 has almost zero current flow due to the lifted bond wire. Meanwhile cells 2-4 with perfect wire connections carry 70 A at the short-circuit beginning.

At the same time, cell 5, cell 9 and cell 13 have lower current flow, which is plotted in Fig. 12 (b). This is because these cells can only be connected to external emitter through Al metallization.

3) Thermal Simulation Results.

During short-circuit, the unequal temperature map is effectively predicted in thermal simulation, as shown in Fig. 13. Same as in Fig. 11, four chip temperature maps during short-circuit are reported in Fig. 13. They are before short-circuit (at 2 μ s), during short-circuit (at 10 μ s), after short-circuit (at 14 μ s and 18 μ s) respectively.

Starting from room temperature (25 $^{\circ}$ C) (the first picture at 2 μ s), chip surface temperature becomes unequal during short-circuit. Cell 1 under the lifted-off bond wire, is much cooler than the other cells. Cells under non-degraded bond wires (cells 2-4 and cells 10-12) show higher temperature

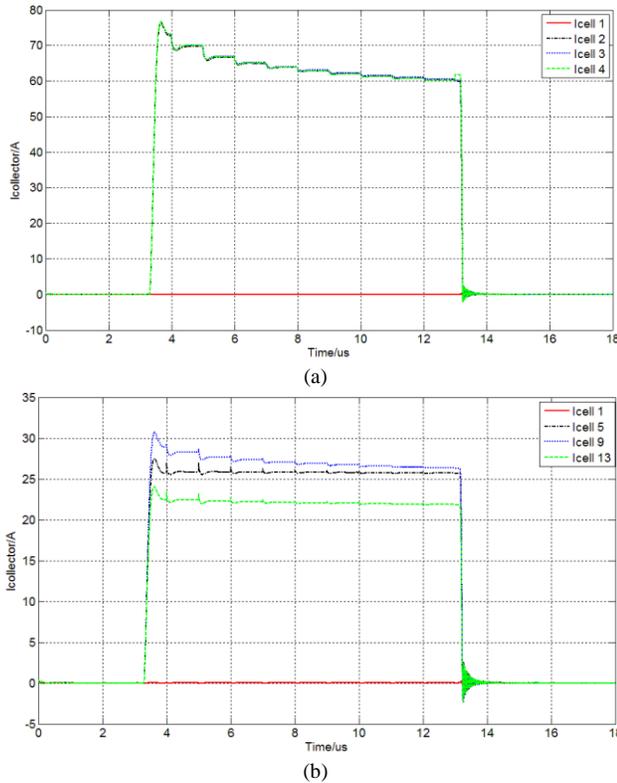


Fig. 12. PSpice simulation results in case of one bond wire lifted off: (a) current distribution among cells close to external emitter (cell 1, cell 2, cell 3, and cell 4 in Fig.9); (c) current distribution among cell 1, cell 5, cell 9, and cell 13 in Fig.9.

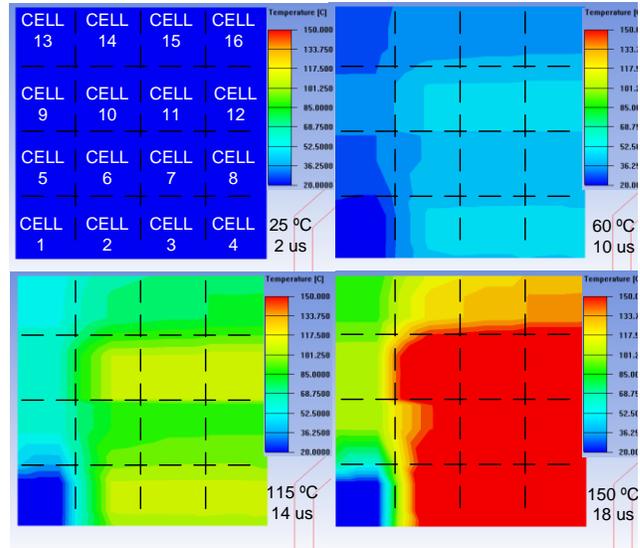


Fig. 13. IGBT chip temperature map in case of one bond wire lifted off in Icepak during short-circuit at 2/10/14/18 μ s (times and peak temperature at bottom right of each image) (Temperature color bar – max 150 $^{\circ}$ C, min 20 $^{\circ}$ C).

than other ones, especially compared with the degraded ones. Comparing with results of the new module in Fig. 11, temperature of non-degraded bond wires is more than 5 °C higher in Fig. 13. It is worth to note that this evidenced phenomenon can accelerate the degradation of the remaining bond wires.

V. CONCLUSION

A new electro-thermal co-simulation approach involving PSpice and ANSYS/Icepak has been presented, which exhibits capability of predicting current and temperature distribution inside the chip of power IGBT modules. Through a case study of a 1700 V/1000 A commercial IGBT module, the approach successfully predicts imbalanced current as well as temperature distribution due to bond wires fatigue under short-circuit situation. The proposed method enables to predict the effects of bond wire fatigue under severe conditions which are not straightforward to be experimentally studied. Further aging effects like solder delamination and/or metal degradation can be also studied in the future with the proposed approach.

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