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An Efficient Implementation of Generalized Delayed Signal Cancellation PLL

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***Abstract*—The phase, frequency, and amplitude of the fundamental-frequency positive-sequence component of the grid voltage are crucial information in control of most grid-connected power electronic based equipment. Often, a standard phase-locked loop (PLL) with a prefiltering stage is employed for the extraction of them. Inspired by the concept of delayed signal cancellation (DSC), the generalized DSC (GDSC) operator has recently been introduced as an interesting option for the PLL prefiltering stage. In its typical structure, the GDSC operator extracts the grid fundamental component and feeds it to a conventional synchronous reference frame PLL (SRF-PLL). The frequency estimated by the SRF-PLL is then fed back to the GDSC operator to make it frequency adaptive. This structure, however, suffers from two main drawbacks: 1) the system is highly nonlinear and, therefore, it is very difficult to ensure its stability under all circumstances; 2) adapting the GDSC to grid frequency variations increases the implementation complexity and computational effort, particularly when the interpolation techniques are used for this purpose. To avoid these problems while maintaining high accuracy in the extraction of grid voltage quantities, an efficient and low-cost implementation of the GDSC-PLL is suggested in this paper. The proposed structure, which is called the enhanced GDSC-PLL (EGDSC-PLL), uses a non-adaptive GDSC operator as its prefiltering stage, and compensates the phase-shift and amplitude scaling caused by this operator by using two units, called the phase-error compensator and amplitude-error compensator. The effectiveness of the EGDSC-PLL is confirmed through simulation and experimental results.**

***Index Terms*—Delayed signal cancelation (DSC), phase-locked loop (PLL), synchronization.**

I. Introduction

The phase, frequency, and amplitude of the fundamental-frequency positive-sequence (FFPS) component of the grid voltage are crucial information in control of grid-connected power electronic based equipment such as uninterruptible power supplies [1], distributed generation systems [2], flexible AC transmission systems [3], and high voltage direct current systems [4], [5] . To extract this information, different methods have been proposed in the literature. Phase locked-loop (PLL) based algorithms are probably the most popular and widely used techniques owing to their robust performance and effectiveness.

A PLL is a closed-loop feedback control system which synchronizes its output in frequency and phase with its input [6]. The phase detector, the loop filter, and the voltage controlled oscillator are common parts of almost all PLLs [6]. A major challenge associated with PLLs is how to achieve a high disturbance rejection capability without degrading the dynamic performance [7]. Different researchers have proposed different strategies to deal with this challenge. These methods can be classified into two major categories, namely in-loop and pre-loop methods.

The in-loop approaches can be considered as any modification in the PLL control loop to improve its dynamic response/filtering capability tradeoff. Some examples of such techniques are: 1) using adaptive notch filters [8] or adaptive lead compensators [9] for selective cancellation of harmonic components in the PLL control loop; 2) dynamically adjusting the gain of the frequency estimation loop to improve the PLL dynamic performance during startups and phase angle jumps [10]; and 3) using moving average filters (MAFs) or repetitive regulators for elimination of all (or at least most) low-order harmonics in the PLL control loop [11]-[18].

The pre-loop methods, on the other hand, can be typically understood as a filtering stage which is used before the input of the PLL and is responsible for extracting the FFPS component and eliminating (or at least attenuating) some (or most) of the grid voltage harmonics. The complex coefficient filters [19], [20], the space vector Fourier transform [21], and the dual second-order generalized integrators [22] are the well-known pre-loop filtering methods.

Inspired by the concept of delayed signal cancellation (DSC) [23]-[26], the generalized DSC (GDSC) operator has recently been introduced as an effective solution to improve the performance of the PLL under adverse grid conditions [27]-[29]. Typically, the GDSC operator is employed as the PLL prefiltering stage and is responsible for extracting the grid voltage FFPS component. The PLL receives this component as its input and extracts its phase, frequency, and amplitude. The frequency estimated by the PLL is then fed back to the GDSC operator to make it frequency adaptive. The main drawback of this structure is that it is highly nonlinear, so it is very difficult to ensure the stability of the whole system under all circumstances [30]. Moreover, adapting the GDSC operator to the grid frequency variations increases the implementation complexity and computational burden, particularly when the

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interpolation techniques are used for this purpose.

To avoid the aforementioned problems, an efficient and low-cost implementation of the GDSC based PLL is suggested in the paper. The proposed PLL structure employs a non-adaptive GDSC operator as its prefiltering stage, and uses two units, called the phase-error compensator (PEC) and amplitude-error compensator (AEC), to correct the phase-shift and amplitude scaling caused by this operator in the presence of frequency drifts. Designing the PEC and AEC is based on the idea of post-processing proposed in [31]. The small-signal model of the proposed PLL structure is also derived, which simplifies the tuning procedure and stability analysis. The effectiveness of the suggested PLL structure, which is called the enhanced GDSC-PLL (EGDSC-PLL), is confirmed through simulation and experimental results.

II. Overview of DSC-PLL and GDSC-PLL

A. DSC-PLL

Application of the DSC operator for extraction of the FFPS component in the stationary ($\alpha\beta$) reference frame can be expressed as [23], [24]

$$\vec{v}^{+}_{\alpha\beta,1}(t) = \frac{1}{2}\left[\vec{v}_{\alpha\beta}(t) + e^{\frac{j2\pi}{n}}\vec{v}_{\alpha\beta}(t-T/n)\right] \tag{1}$$

where $\vec{v}_{\alpha\beta}(t) = v_\alpha(t) + jv_\beta(t)$ is the grid voltage vector in the $\alpha\beta$ frame, $\vec{v}^{+}_{\alpha\beta,1}(t) = v^{+}_{\alpha,1}(t) + jv^{+}_{\beta,1}(t)$ is the extracted FFPS voltage vector, T is the nominal value of the grid voltage fundamental period, and n is the delay factor. Taking the Laplace transform of both sides of (1) yields

$$\vec{v}^{+}_{\alpha\beta,1}(s) = \underbrace{\frac{1}{2}\left[1 + e^{\frac{j2\pi}{n}}e^{-\frac{T}{n}s}\right]}_{\mathrm{DSC}_n(s)}\vec{v}_{\alpha\beta}(s) \tag{2}$$

where $\mathrm{DSC}_n(s)$ is the transfer function of the $\alpha\beta$-frame DSC operator.

Substituting $s = j\omega$ into the transfer function of the DSC operator yields

$$\mathrm{DSC}_n(j\omega) = \left|\cos\left(\frac{\omega T}{2n} - \frac{\pi}{n}\right)\right| \angle - \left(\frac{\omega T}{2n} - \frac{\pi}{n}\right). \tag{3}$$

Fig. 1 illustrates the frequency response of (3) for $n = 4$, which is the recommended choice for blocking the fundamental-frequency negative-sequence (FFNS) component of the grid voltage [23]. As shown, the DSC_4 operator provides unity gain with zero phase at the fundamental frequency of positive sequence and zero gain at the fundamental frequency of negative sequence. This means that the DSC_4 operator passes the FFPS component and blocks the FFNS component. It can also be observed that the DSC_4 operator blocks all harmonics of order $h = 4k-1$ ($k = \pm1, \pm2, \pm3, \ldots$), but leaves all harmonics of order $h = 4k+1$ ($k = \pm1, \pm2, \pm3, \ldots$) unchanged. The 11th harmonic of negative sequence and 13th harmonic of positive sequence are among the most important harmonic components that the DSC_4 operator cannot block.

Fig. 2 shows the block diagram description of the DSC-PLL, which consists of a conventional synchronous reference frame

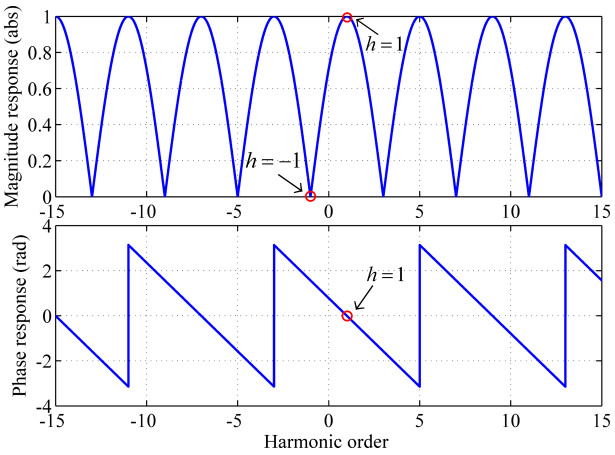

Fig. 1. Frequency response of the DSC_4 operator. h denotes the harmonic order.

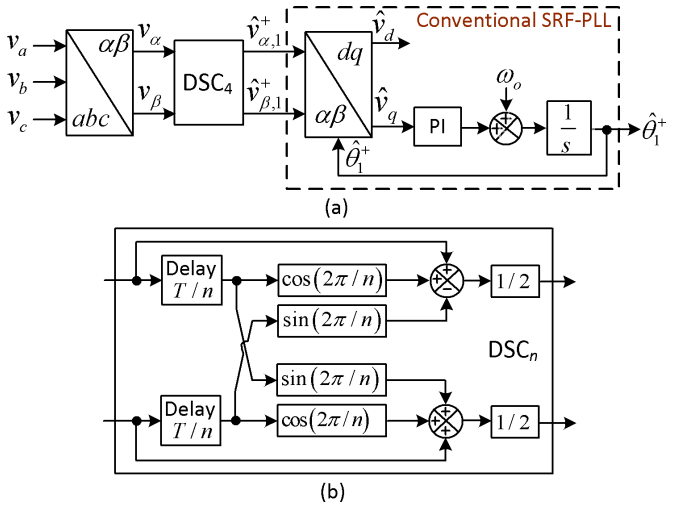

Fig. 2. (a) Block diagram description of the DSC-PLL. (b) Time domain implementation of the DSC_n operator.

PLL (SRF-PLL) and DSC_4 operator [25], [26]. The DSC_4 operator is responsible for extracting the FFPS voltage vector, and the SRF-PLL is responsible for extracting the phase, frequency, and amplitude of this voltage vector. The DSC-PLL can provide an accurate estimation of the grid fundamental phase, frequency, and amplitude under unbalanced and/or low-distorted grid conditions; however, it fails to do so under highly distorted grid conditions, particularly when, in addition to the odd-order harmonic components, there are even-order harmonic components and dc offset in the grid voltage. To overcome this drawback, the idea of GDSC and GDSC-PLL has recently been proposed [27]-[29].

B. GDSC-PLL

The idea behind the GDSC operator is quite simple: several DSC operators (with proper delay factors) are cascaded with the DSC_4 operator to block those harmonics that it cannot. The question that may arise here is: how many DSCs are needed for this purpose? The answer to this question depends on the anticipated harmonic pattern for the grid voltage. For

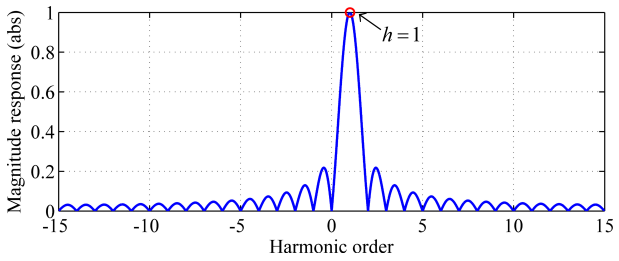

Fig. 3. Magnitude response of the $\mathrm{GDSC}_{2,4,8,16,32}$ operator.

example, if only odd-order harmonic components are expected in the grid voltage, then cascading three DSC operators with delay factors $n = 8, 16, 32$ with the DSC_4 operator is good enough to block them. However, the grid harmonic pattern is often unknown. Therefore, it should be assumed that all harmonic components of all sequences are present in the grid voltage. In this case, cascading four DSC operators with delay factors $n = 2, 8, 16, 32$ with the DSC_4 operator is often recommended [27]-[29]. Equation (4) describes the s-domain transfer function of the resultant GDSC operator in this condition, and Fig. 3 shows its magnitude frequency response.

$$\mathrm{GDSC}_{2,4,8,16,32}(s) = \prod_{n=2,4,8,16,32} \mathrm{DSC}_n(s). \tag{4}$$

Fig 4(a) shows the GDSC-PLL proposed in [28], which consists of three distinct parts: 1) the $\mathrm{GDSC}_{2,4,8,16,32}$ operator, which extracts the FFPS voltage vector; 2) the SRF-PLL, which extracts the phase, frequency, and amplitude of the FFPS voltage vector; and 3) a frequency-feedback loop (FFL), which feeds back the estimated frequency to the $\mathrm{GDSC}_{2,4,8,16,32}$ operator to make it frequency adaptive. The main drawbacks of this structure are the following: 1) the FFL makes the system highly nonlinear, so it is very difficult to ensure the system stability under all circumstances [30]; 2) adaptation of GDSC operator to the grid frequency variations increases the required computational effort, particularly when the interpolation techniques are used for this purpose.

Fig 4(b) shows the GDSC-PLL proposed in [27]. To avoid the aforementioned stability problem, this structure uses two $\mathrm{GDSC}_{2,4,8,16,32}$ operators and two SRF-PLLs: one set provides an estimation of the grid frequency for the other set. However, it clearly demands more digital resources.

III. Proposed Structure

Fig. 5 shows the schematic diagram of the proposed EGDSC-PLL. As shown, to avoid the implementation complexity, the high computational burden and the nonlinearity caused by adaptive GDSC operator, a non-adaptive GDSC operator is considered as the PLL prefiltering stage. This non-adaptive operator accurately extracts the FFPS component when the grid frequency is at its nominal value. However, it fails to do so in the presence of frequency drifts: the extracted FFPS component undergoes a phase shift and amplitude scaling under off-nominal grid frequencies. To correct these

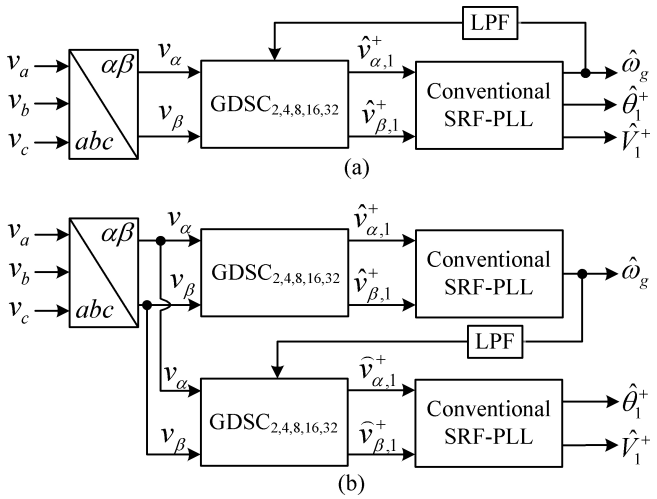

Fig. 4. Different structures of GDSC-PLL. (a) Structure proposed in [28]. (b) Structure proposed in [27].

errors, two units, called the PEC and AEC, are designed and incorporated into the SRF-PLL structure.

A. Phase and Amplitude Error Compensation

Substituting $s = j\omega_g$ into (4), where ω_g is the grid fundamental frequency, gives the phase and magnitude of the GDSC operator at the fundamental frequency as

$$\angle\mathrm{GDSC}_{2,4,8,16,32}(j\omega_g) = -\sum_{n=2,4,8,16,32}\left(\frac{\omega_g T}{2n} - \frac{\pi}{n}\right) \tag{5}$$

$$|\mathrm{GDSC}_{2,4,8,16,32}(j\omega_g)| = \prod_{n=2,4,8,16,32}\left|\cos\left(\frac{\omega_g T}{2n} - \frac{\pi}{n}\right)\right|. \tag{6}$$

Defining $\omega_g = \omega_o + \Delta\omega_g$, where $\omega_o = 2\pi/T$ is the nominal value of grid frequency and $\Delta\omega_g$ denotes the deviation of grid frequency from its nominal value, and substituting it into (5) and (6) yields

$$\begin{aligned}\angle\mathrm{GDSC}_{2,4,8,16,32}(j\omega_g) &= -\sum_{n=2,4,8,16,32}\left(\frac{\Delta\omega_g T}{2n}\right) \\ &= -\underbrace{\frac{T}{2}\left[\sum_{n=2,4,8,16,32}\frac{1}{n}\right]}_{k_\phi}\Delta\omega_g \end{aligned} \tag{7}$$

$$\begin{aligned}|\mathrm{GDSC}_{2,4,8,16,32}(j\omega_g)| &= \prod_{n=2,4,8,16,32}\cos\left(\frac{\Delta\omega_g T}{2n}\right) \\ &\approx \prod_{n=2,4,8,16,32}\left[1-\left(\frac{\Delta\omega_g T}{2n}\right)^2/2\right] \\ &\approx 1 - \underbrace{\frac{T^2}{8}\left(\sum_{n=2,4,8,16,32}\frac{1}{n^2}\right)}_{k_v}(\Delta\omega_g)^2. \end{aligned} \tag{8}$$

Notice that in the derivation of (7) no approximation is made; however, in the derivation of (8), it is assumed that the argument of the cosine term, which depends on the grid frequency,

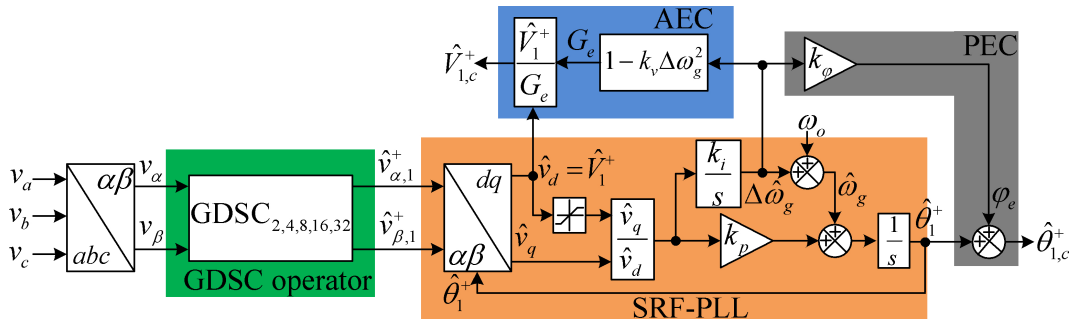

Fig. 5. Block diagram description of the EGDSC-PLL.

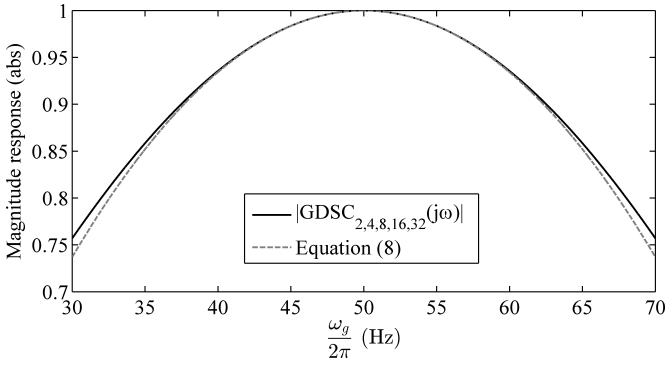

Fig. 6. Accuracy assessment of (8) in the prediction of the magnitude frequency response of the $\mathrm{GDSC}_{2,4,8,16,32}$ operator around the nominal frequency.

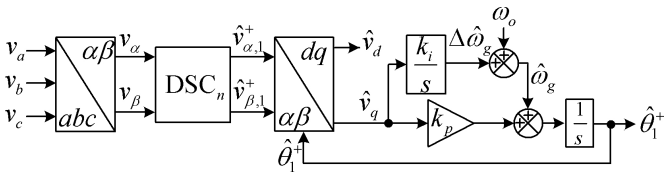

Fig. 7. Schematic diagram of the DSC-PLL.

is much lower than the unity. Therefore, the accuracy of (8) should be evaluated.

Fig. 6 compares the magnitude frequency response of the $\mathrm{GDSC}_{2,4,8,16,32}$ operator with that predicted by (8). It can be observed that (8) is quite accurate within the range of 50 ± 10 Hz, which is much wider than the allowable range of variations of grid frequency [35].

Equations (7) and (8) show that a phase shift of $-k_\varphi \Delta\omega_g$ and amplitude scaling of about $1-k_v(\Delta\omega_g)^2$ in the extraction of the FFPS component by the PLL prefiltering stage happens. Considering that k_φ and k_v are constant gains that can be simply calculated from (7) and (8), respectively, and that the output signal of the integrator of the proportional-integral (PI) controller provides an estimation of $\Delta\omega_g$, these errors can be simply compensated as shown in Fig. 5.

B. Small-Signal Modeling

The small-signal modeling of the EGDSC-PLL is rather complicated. To simplify this task, the small-signal model of a simple DSC-PLL is first derived. This model is then extended to the proposed PLL structure. Fig. 7 shows the schematic diagram of the DSC-PLL, where DSC_n, as mentioned before, denotes a $\alpha\beta$-frame DSC operator with delay factor n. Equation (2) expresses the transfer function of this operator.

Fig. 8 shows the alternative mathematically equivalent representation of the DSC-PLL, in which the $\alpha\beta$-frame DSC operator is replaced by its dq-frame equivalent, i.e., the $dq\mathrm{DSC}_n$ operator, in a generic synchronous reference frame rotating at the nominal angular frequency. The transfer function of the $dq\mathrm{DSC}_n$ operator, as shown in (9), can be simply obtained by replacing s by $s + j\omega_o$ in the transfer function of the DSC_n operator, because transferring from the stationary to the synchronous reference frame is mathematically equivalent to a frequency shift equal to the rotating speed of the synchronous reference frame [32].

$$dq\mathrm{DSC}_n(s) = \mathrm{DSC}_n(s + j\omega_o) = 0.5\left(1 + e^{-\frac{T}{n}s}\right). \quad (9)$$

For the sake of simplicity in the modelling procedure, let the three-phase voltage in the DSC-PLL input be balanced and without harmonic distortion, i.e.,

$$\begin{aligned} v_a(t) &= V_1^+ \cos\left(\theta_1^+\right) \\ v_b(t) &= V_1^+ \cos\left(\theta_1^+ - 2\pi/3\right) \\ v_c(t) &= V_1^+ \cos\left(\theta_1^+ + 2\pi/3\right) \end{aligned} \quad (10)$$

where V_1^+ and $\theta_1^+ = \int \omega_g dt$ are the amplitude and phase angle of the FFPS component of the grid voltage, respectively. Applying the Clarke's transformation and subsequently the Park's transformation to the three-phase voltages (10) gives the input signals of the $dq\mathrm{DSC}_n$ operator, i.e., v_d and v_q, as

$$\begin{aligned} v_d(t) &= V_1^+ \cos\left(\Delta\theta_1^+\right) \\ v_q(t) &= V_1^+ \sin\left(\Delta\theta_1^+\right) \end{aligned} \quad (11)$$

where $\Delta\theta_1^+ = \theta_1^+ - \theta_o = \int (\omega_g - \omega_o)\, dt = \int \Delta\omega_g dt$.

Using (11) and (9) and assuming that $\Delta\omega_g$ is a constant, the output signals of the $dq\mathrm{DSC}_n$ operator, i.e., $\bar{v}_d$ and $\bar{v}_q$, can be obtained as

$$\begin{aligned} \bar{v}_d(t) &= 0.5V_1^+ \cos\left(\Delta\theta_1^+\right) + 0.5V_1^+ \cos\left(\Delta\theta_1^+ - \tfrac{\Delta\omega_g T}{n}\right) \\ \bar{v}_q(t) &= 0.5V_1^+ \sin\left(\Delta\theta_1^+\right) + 0.5V_1^+ \sin\left(\Delta\theta_1^+ - \tfrac{\Delta\omega_g T}{n}\right). \end{aligned} \quad (12)$$

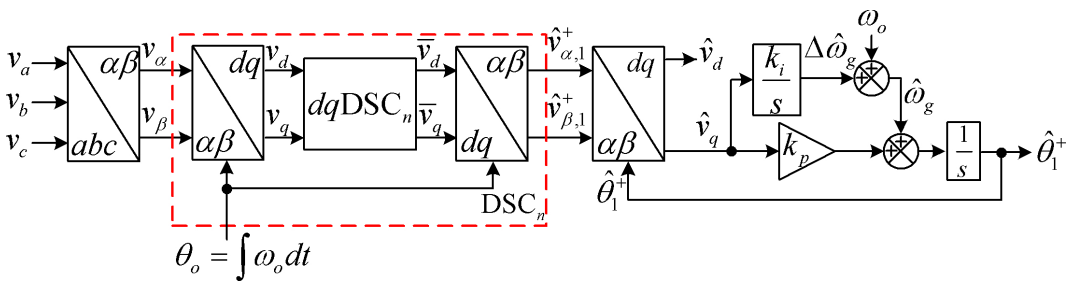

Fig. 8. Alternative mathematically equivalent representation of the DSC-PLL.

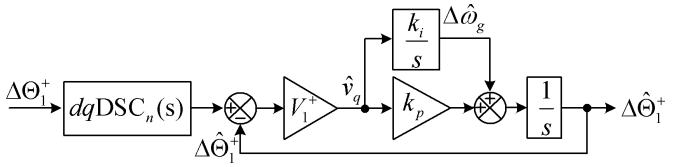

Fig. 9. Small-signal model of the DSC-PLL.

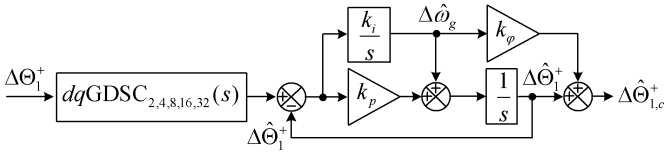

Fig. 10. Small-signal model of the EGDSC-PLL.

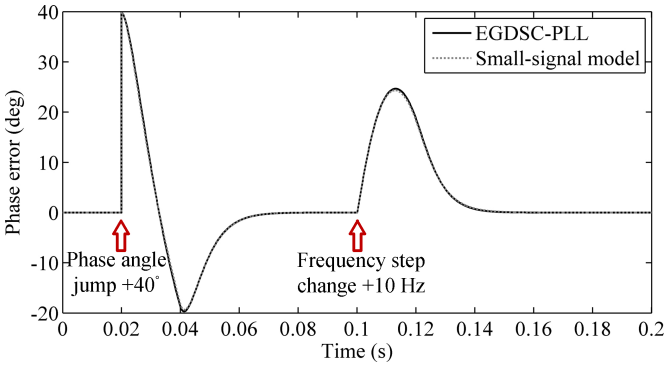

Fig. 11. Accuracy assessment of the EGDSC-PLL small-signal model. Control parameters: $k_p = 440$, $k_i = 48361$ and $k_\varphi = 9.6875e-3$.

Applying the inverse Park's transformation with a rotating angle θ_o to (12) and then the Park's transformation with a rotating angle $\hat{\theta}^+_1$ to the result gives the PI controller input signal, i.e., $\hat{v}_q$, as

$$\hat{v}_q(t) = 0.5V^+_1 \sin\left(\Delta\theta^+_1 - \Delta\hat{\theta}^+_1\right) + 0.5V^+_1 \sin\left(\Delta\theta^+_1 - \frac{\Delta\omega_g T}{n} - \Delta\hat{\theta}^+_1\right) \quad (13)$$

where $\Delta\hat{\theta}^+_1 = \hat{\theta}^+_1 - \theta_o$.

By replacing the sine functions by their arguments, (13) can be approximated by

$$\begin{aligned}\hat{v}_q(t) &= 0.5V^+_1\left(\Delta\theta^+_1 - \Delta\hat{\theta}^+_1\right) \\ &\quad +0.5V^+_1\left(\Delta\theta^+_1 - \frac{\Delta\omega_g T}{n} - \Delta\hat{\theta}^+_1\right) \\ &= V^+_1\left[0.5\left(\Delta\theta^+_1 + \Delta\theta^+_1 - \frac{\Delta\omega_g T}{n}\right) - \Delta\hat{\theta}^+_1\right]. \quad (14)\end{aligned}$$

Taking the Laplace transform of (14) gives

$$\hat{v}_q(s) = V^+_1\left[\underbrace{0.5\left(1 + e^{-\frac{T}{n}s}\right)}_{dq\text{DSC}_n(s)}\Delta\Theta^+_1 - \Delta\hat{\Theta}^+_1\right] \quad (15)$$

where $\Delta\Theta^+_1$ and $\Delta\hat{\Theta}^+_1$ denote the Laplace transform of $\Delta\theta^+_1$ and $\Delta\hat{\theta}^+_1$, respectively. Using (15), the DSC-PLL small-signal model can be obtained as shown in Fig. 9.

The small-signal model of the proposed EGDSC-PLL can now be derived by applying the following changes to the model shown in Fig. 9.

1) The voltage amplitude V^+_1, which appears as a gain in the forward path of the DSC-PLL model, should be removed. The reason is that the proposed PLL uses an amplitude normalization mechanism before the PI controller.
2) The transfer function of the $dq\text{DSC}_n$ operator in the DSC-PLL model should be replaced by

$$\begin{aligned}dq\text{GDSC}_{2,4,8,16,32}(s) &= \prod_{n=2,4,8,16,32} dq\text{DSC}_n(s) \\ &= \prod_{n=2,4,8,16,32} \frac{1}{2}\left(1 + e^{-\frac{T}{n}s}\right) \quad (16)\end{aligned}$$

which is the transfer function of the dq-frame equivalent of the $\text{GDSC}_{2,4,8,16,32}$ operator.
3) The PI controller integrator output, i.e., $\Delta\hat{\omega}_g$, should be multiplied by k_φ and added to the small-signal model output in order to model the dynamics of the PEC.

Fig. 10 shows the small-signal model of the proposed PLL, and Fig. 11 evaluates the accuracy of this model. As it can be observed, the derived small-signal model is very accurate and perfectly predicts the dynamic behavior of the EGDSC-PLL.

C. Stability Analysis and Parameter Design Guidelines

The derived small-signal model can be very helpful for stability analysis and for selecting the control parameters of the

TABLE I
CONTROL PARAMETERS OF THE EGDSC-PLL.

Parameter	Value
Proportional gain, $k_p = 2\zeta\omega_n$	440
Integral gain, $k_i = \omega_n^2$	48361
PEC gain, $k_\varphi = 31T/64$	$9.6875e-3$
AEC gain, $k_v = 341T^2/8192$	$1.665e-5$

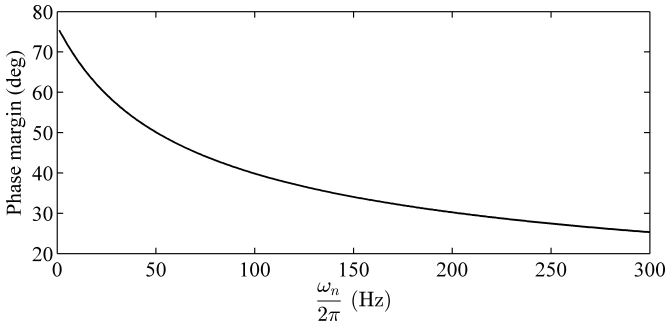

Fig. 12. PM of the EGDSC-PLL as a function of ω_n.

SRF-PLL. Using this model, the closed-loop transfer function of the PLL can be obtained as

$$G_{cl}(s) = \frac{\Delta\hat{\Theta}_{1,c}^{+}}{\Delta\Theta_{1}^{+}} = dq\mathrm{GDSC}_{2,4,8,16,32}(s)\frac{(k_p + k_i k_\varphi)\, s + k_i}{s^2 + k_p s + k_i} \quad (17)$$

which shows that the proposed PLL is stable for $k_p > 0$ and $k_i > 0$.

Defining $k_p = 2\zeta\omega_n$ and $k_i = \omega_n^2$, where ζ is the damping factor and ω_n is the natural frequency, k_p and k_i can be determined by selecting appropriate values for ζ and ω_n. As recommended in [33], $\zeta = 1$ is chosen for the damping factor. On the other hand, the natural frequency ω_n should be tuned depending on the required stability margin, filtering capability and transient response. Fig. 12 shows the variation of phase margin (PM) of the EGDSC-PLL as a function of ω_n. It can be observed that increasing ω_n, which corresponds to raising the speed of response and reducing the filtering capability of the PLL, decreases the PM. Here, $\omega_n = 2\pi 35$ rad/s, which corresponds to $\mathrm{PM} \approx 55^\circ$, is adopted for the natural frequency of the EGDSC-PLL. This value ensures a fast dynamic response and good filtering capability for the PLL. Table I summarizes the selected values of the control parameters.

It should be mentioned that the gain margin (GM) of proposed PLL, which is -5.75 dB, is negative. Notice that a negative GM does not necessarily mean instability. It just means that the PLL may become unstable if the loop gain reduces too much [36]. Fortunately, the amplitude normalization mechanism included into the EGDSC-PLL structure prevents such condition and ensures its stability.

TABLE II
PARAMETERS OF DISTORTED INPUT VOLTAGE

Voltage component	**Amplitude** (p.u.)
Fundamental positive-sequence	1
Fundamental negative-sequence	0.1
5^{th} harmonic negative-sequence	0.1
7^{th} harmonic positive-sequence	0.1
11^{th} harmonic negative-sequence	0.05
13^{th} harmonic positive-sequence	0.05

IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the effectiveness of EGDSC-PLL is evaluated through simulation and experimental results. Simulations are carried out in Matlab/Simulink environment and experimental results are obtained using a dSPACE MABXII DS1401 platform. Throughout the simulation and experimental studies, $f_s = 8$ kHz (f_s is the sampling frequency) and $\omega_o = 2\pi 50$ rad/s are considered.

A. Symmetrical Voltage Sag with Frequency Step Change

Fig. 13 shows the simulation and experimental results for the EGDSC-PLL under a symmetrical voltage sag of $+0.5$ p.u. and a frequency step change of $+3$ Hz. It can be observed that the EGDSC-PLL provides a zero steady-state phase error and an accurate estimation of the grid voltage amplitude in the presence of frequency drifts. The PLL settling time in the estimation of amplitude and frequency are about one and two cycles of fundamental frequency, respectively. For those situations where a faster dynamic response is needed, the $\mathrm{GDSC}_{4,8,16,32}$ operator can be used instead of the $\mathrm{GDSC}_{2,4,8,16,32}$. Notice that this solution can be employed only when the dc offset and even-order harmonic components in the PLL input voltage are negligible.

B. Distorted and Unbalanced Grid Condition

In this test, the steady-state performance of EGDSC-PLL under distorted and unbalanced grid condition is evaluated. The harmonic components of the test voltage, which are summarized in Table II, are almost twice of the maximum allowed values according to the IEC standards [37]. This test is performed under off-nominal frequencies ($\omega_g = 2\pi 49$ and $\omega_g = 2\pi 47$ rad/s). The obtained results are shown in Fig. 14. As it can be observed, the PLL phase and amplitude errors are limited to 0.5° and 0.01 pu, respectively, which confirm the high filtering capability of the EGDSC-PLL.

C. Asymmetrical Voltage Sag

This section evaluates the EGDSC-PLL performance under different levels of voltage sag at phase *A* of the grid voltage. During this test, the amplitudes of phase *B* and *C* are fixed at 1 pu. This test, similar to the previous one, is carried out under off-nominal grid frequencies. The obtained results are shown in Fig. 15. As it can be observed, the performance of

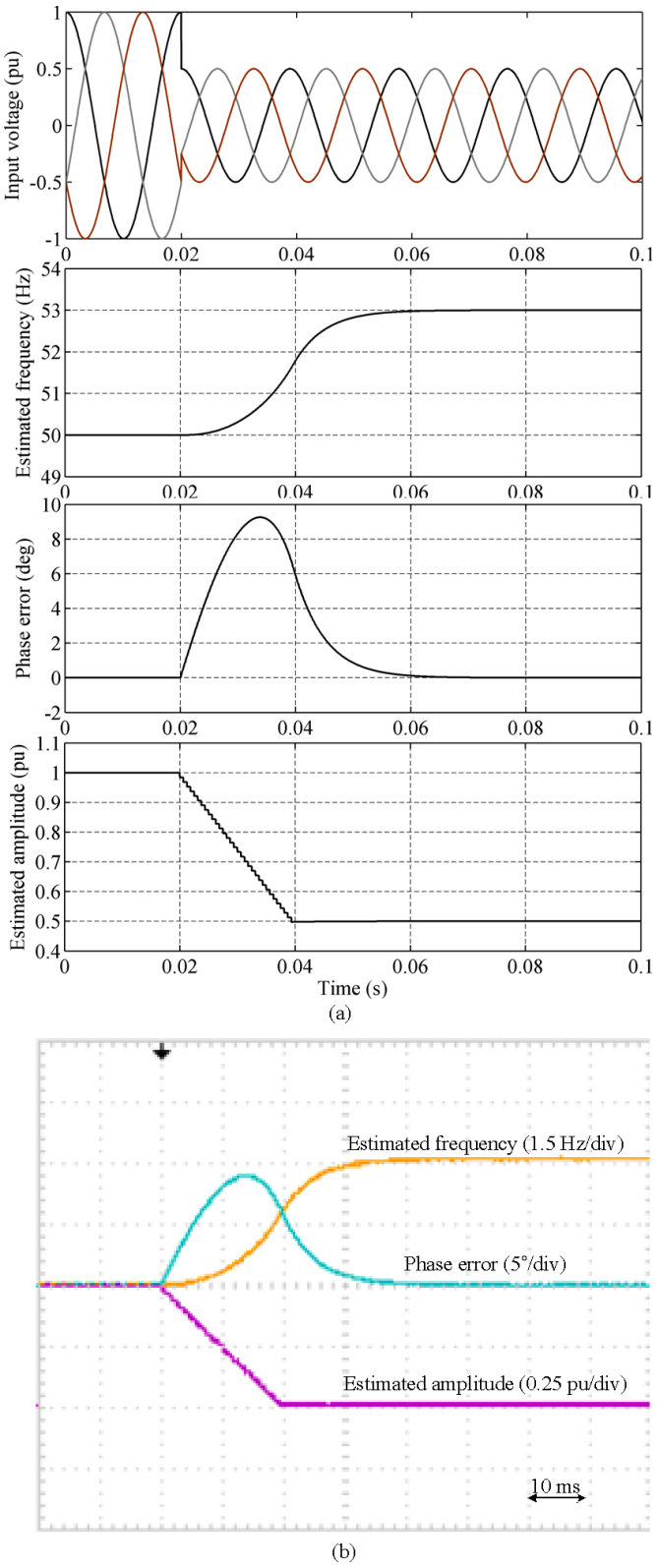

Fig. 13. (a) Simulation and (b) experimental results for the EGDSC-PLL when the grid voltage undergoes a symmetrical voltage sag of 0.5 p.u. with a frequency step change of $+3$ Hz.

the proposed PLL is quite good when the grid frequency is close to its nominal value. It, however, tends to worsen in the presence of large frequency drifts. To improve the performance

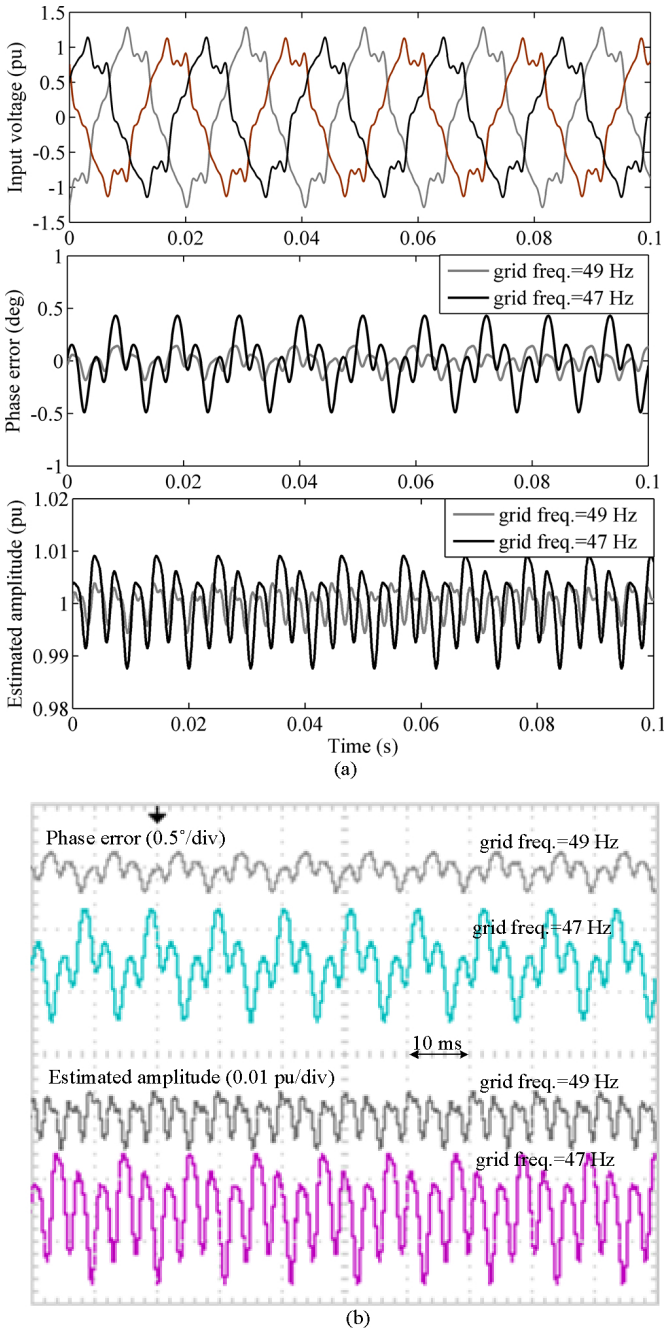

Fig. 14. (a) Steady-state simulation and (b) experimental results under distorted and unbalanced grid conditions.

of the proposed PLL in such scenarios, an extra DSC_4 operator can be included in the $\mathrm{GDSC}_{2,4,8,16,32}$ operator.

V. Comparison with Conventional GDSC-PLLs

The GDSC-PLLs proposed in [27] and [28], which use frequency adaptive GDSC operator in their structure, can provide a performance as good as that of the developed EGDSC-PLL; however, their implementations require a higher computational effort, particularly when the interpolation techniques are used for adapting them to the grid frequency variations. To support this claim, Table III summarizes the key elements of the

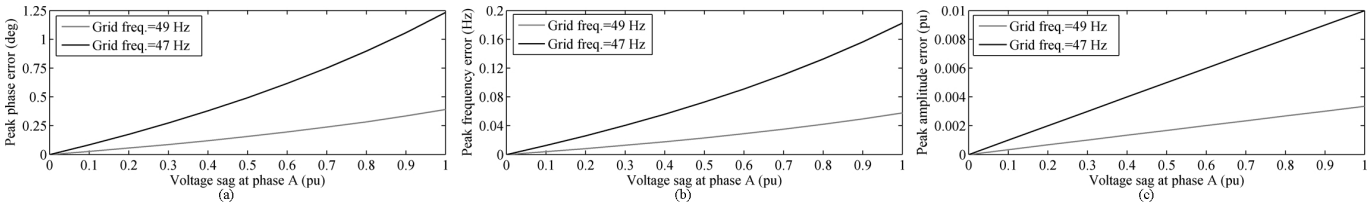

Fig. 15. Magnitude of double frequency oscillatory error in (a) the estimated phase, (b) the estimated frequency, and (c) the estimated amplitude under single-phase voltage sags.

TABLE III
KEY ELEMENTS OF THE SUGGESTED GDSC-PLL STRUCTURE AND THOSE PROPOSED IN [27] AND [28].

	EGDSC-PLL	**GDSC-PLL proposed in [28]**	**GDSC-PLL proposed in [27]**
Required number of SRF-PLLs	one	one	two
Required number of GDSC operators	one	one	two
Type of GDSC operators	non-adaptive	adaptive	first GDSC operator is non-adaptive and the second one is adaptive

TABLE IV
NUMBER OF OPERATIONS REQUIRED FOR DIGITAL IMPLEMENTATION OF ADAPTIVE AND NON-ADAPTIVE $\mathrm{GDSC}_{2,4,8,16,32}$ OPERATOR. **M**=MULTIPLICATION, **A**=ADDITION, AND **T**=TRIGONOMETRIC FUNCTION CALCULATION.

	M	**A**	**T**
Adaptive $\mathrm{GDSC}_{2,4,8,16,32}$ with linear interpolation*	70	30	20
Non-adaptive $\mathrm{GDSC}_{2,4,8,16,32}$	12	16	0

* The mathematical operations required for updating arguments of trigonometric functions and frequency dependent gains has been neglected.

suggested PLL structure and those proposed in [27] and [28], and Table IV compares the mathematical operations required for the implementation of the non-adaptive GDSC operator with those of the adaptive GDSC with linear interpolation. Based on these results, it is immediate to conclude that the EGDSC-PLL and the structure proposed in [27] demand the lowest and highest computational efforts, respectively.

VI. SUMMARY AND CONCLUSION

In this paper, an efficient and low-cost implementation of GDSC-PLL was proposed. The suggested PLL structure is based on employing a non-adaptive GDSC operator as the SRF-PLL prefiltering stage and two compensators, called the PEC and AEC, to correct the phase shift and amplitude scaling caused by the non-adaptive GDSC operator under off-nominal grid frequencies.

It was shown that the PEC and AEC can be simply implemented using very few mathematical operations. In the PEC design no assumption about the value of the grid frequency has been made. Therefore, the PEC can effectively compensate the phase shift caused by the non-adaptive GDSC operator regardless of the value of grid frequency. The design of the AEC, however, was made under the assumption that the grid frequency varies within a specific range. Therefore, the AEC cannot effectively correct the amplitude scaling caused by the non-adaptive GDSC operator for any value of grid frequency; however, as it was shown, it works well in the range of 50 ± 10 Hz, which is wider than the allowable range of grid frequency variations defined in international standards.

The small-signal model of the proposed PLL was also presented. It was demonstrated that this model is very accurate and can be very helpful in the selection of the control parameters. The closed-loop transfer function, which was obtained using this model, also proved that the proposed PLL is stable for positive values of the control parameters.

Finally, the effectiveness of the suggested PLL structure was evaluated through simulation and experimental results. It was verified that the PEC and AEC can effectively compensate the phase shift and amplitude scaling caused by the PLL prefiltering stage, i.e., the non-adaptive GDSC operator. It was also shown that the proposed PLL provides a fast transient response and a good disturbance rejection capability. Through a comparison between the proposed PLL structure and the conventional GDSC-PLLs, it was also highlighted that the former requires a much lower computational effort in digital implementation.

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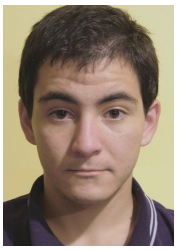

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