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Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs

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***Abstract*—This paper addresses the influences of device and circuit mismatches on paralleling the Silicon Carbide (SiC) MOSFETs. Comprehensive theoretical analysis and experimental validation from paralleled discrete devices to paralleled dies in multichip power modules are first presented. Then, the influence of circuit mismatch on paralleling SiC MOSFETs is investigated and experimentally evaluated for the first time. It is found that the mismatch of the switching loop stray inductance can also lead to on-state current unbalance with inductive output current, in addition to the on-state resistance of the device. It further reveals that circuit mismatches and a current coupling among the paralleled dies exist in a SiC MOSFET multichip power module, which is critical for the transient current distribution in the power module. Thus, a power module layout with an auxiliary source connection is developed to reduce such a coupling effect. Lastly, simulations and experimental tests are carried out to validate the analysis and effectiveness of the developed layout.**

***Index Terms*—DBC layout, parallel connection, power module, SiC MOSFET, WBG devices**

I. Introduction

SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have been undergoing a rapid development in recent years, thanks to its high breakdown voltage, fast switching speed, and good thermal conductivity [1]-[6]. Compared with Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs), SiC MOSFETs have no tail current due to their unipolar structure and thus allowing reduced switching losses and higher switching frequency [5], [7]-[10]. However, the lower current rating of SiC MOSFETs often requires paralleled connection of discrete SiC MOSFETs [11]-[13] or using multichip power module [14]-[22].

For the paralleled operation of power semiconductor devices, current unbalance has always been an important concern, which may cause unequal conduction loss and switching loss [23], [24]. Moreover, besides the steady-state current unbalance, the unequal transient current distribution can further result in higher current overshoot in the device, which may be out of the Safety Operation Area (SOA). Consequently, the current capability of the multichip module tends to be derated [25].

There are generally two main causes of current unbalance in paralleled power semiconductor devices, which are the device mismatch and the asymmetrical circuit layout, i.e. the circuit mismatch. Among the device parameters of MOSFETs, the on-state resistance (R_{on}) and the gate threshold voltage (V_{th}) have more obvious effect on the current sharing performance in parallel connection. The different R_{on} leads to unequal steady-state current, while the different V_{th} results in unbalanced transient current [26]. Asymmetrical circuit layout will result in unequal parasitic inductances, which are mainly switching loop stray inductance (L_d) and common source stay inductance (L_s).

To address the current unbalance, a number of research works are reported on paralleling SiC MOSFETs [11]-[13], [27], [28]. However, only the current unbalance caused by the device mismatch of discrete devices is discussed. The influence of the asymmetrical circuit layout is often overlooked, even though the effects of the circuit parasitic parameters on a single device have been well documented [29], [30]. In [12], a current balancing method based on active gate driver is developed for paralleling discrete devices. This scheme requires accurate current information, which is possible for the pulse currents, but it is challenging for the continuous current due to the limits of bandwidth, galvanic isolation, and physical size of current sensors. Furthermore, in a SiC MOSFET multichip module, it is also important to characterize the effect of circuit layout mismatch on the current distribution among the dies. The switching characteristic and thermal performance of SiC MOSFET modules have been discussed in [17], [20]-[22]. However, the current distribution among the paralleled dies has not been studied yet.

This paper, therefore, presents a systematic analysis of the influences of device and circuit mismatches on paralleling SiC MOSFETs. First, the main sources of device mismatches are discussed, with particular attentions to the material property and fabrication process of SiC MOSFETs. Influences of device mismatches are experimentally investigated regarding the device parameter R_{on} and V_{th}. Then, the mathematic analysis and experimental tests on the effects of asymmetrical circuit design with paralleled discrete devices are carried out. It is shown that the mismatch of the switching loop stray inductance may also lead to on-state current unbalance, besides the difference of R_{on}. This is followed by a detailed analysis of the current distribution in a full SiC MOSFET multichip power module. The circuit mismatch of the Directed Bonded Circuit (DBC) layout and a current coupling effect among the paralleled dies are both found for the first time, which are shown to have a significant influence on the transient current distribution among the dies based on the theoretical analysis. A DBC layout with auxiliary source connection is then developed to mitigate such a current coupling effect, and is validated through simulations and experimental results.

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II. Device Mismatch

A. Device Mismatch Description

Define Among the device parameters of SiC MOSFETs, the on-state resistance and the threshold voltage are two most critical parameters that affect the current sharing performance in parallel connection. R_{on} determines the on-state current distribution among the devices, whereas V_{th} influences the sharing of transient current.

Fig. 1 shows a cross-section schematic of a unit cell for the planar SiC MOSFET [31], which is similar to that of Si MOSFET [32]. Compared to Si MOSFETs, SiC MOSFETs have a lower drift region resistance (R_D), but a higher channel resistance (R_{CH}), due to its lower carrier mobility [31] and a higher level of the channel defect density, which also contributes to the overall on-resistance. At the low Gate-Source voltages (V_{GS}<13V), R_{CH} dominates the total R_{on}, which has a negative temperature coefficient. Hence, it is always recommended to turn on SiC MOSFETs with V_{GS} higher than 18V [31], [33]. Otherwise, paralleling SiC MOSFETs does not have a self-balancing capability and there is a risk of thermal run away.

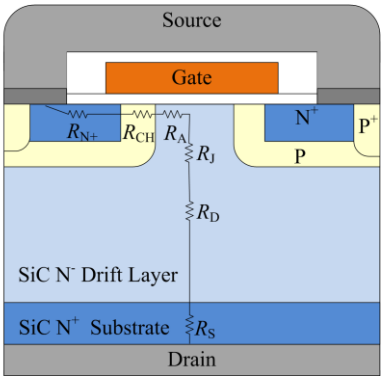
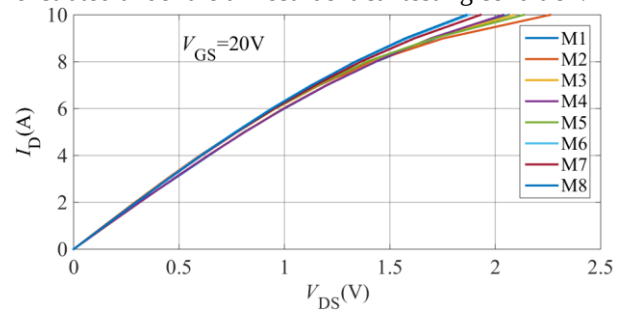


Fig. 1. A cross-section schematic of unit cell for the planar SiC MOSFET.

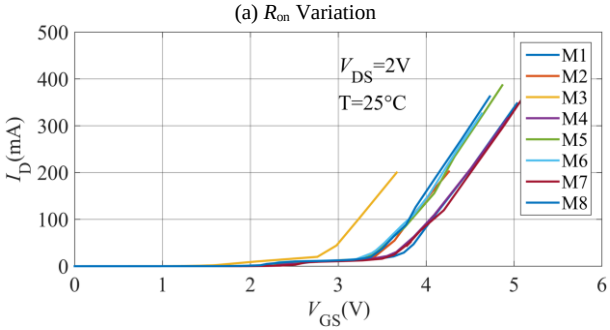
From semiconductor physics, it is known that the threshold voltage V_{th} of the MOS structure is affected by non-idealities, which can lead to shifts in the threshold voltage during long term of cycling. Such non-idealities can be oxide trap states that contain fixed charges or interface states, which are imperfections at the atomic level at the boundary between the oxide and the SiC [34]. Moreover, the material processes of SiC are not as mature as Si, the manufacturing process and the interface quality remains a material issue [35], [36], although this is being addressed by improving material processing, like nitridation of the gate oxide [37]-[40]. As a consequence, slight synthesis variations in the processing may lead to process related variations in the interface and oxide quality, with a variation in threshold voltage as a result[40]. Therefore, SiC MOSFETs are more likely to operate with V_{th} mismatch, especially after long term of cycling.

B. Device Parameters Test and Hardware Setup

To demonstrate the effect of device mismatch, 8 SiC MOSFETs (C2M0160120D) from Cree are tested in the lab. They are denoted as M_1-M_8. R_{on} and V_{th} variations of these devices are plotted in Fig. 2. The procedure of measuring R_{on} variation is summarized as the following. First, the gate source voltage is kept constant at 20V. The drain and the source terminals are connected to a power supply, which operates in the current source mode and is adjusted from 0 to 10A. The MOSFETs are mounted on a heatsink with fan cooling. Then, the drain source voltage (V_{DS}) is measured after V_{DS} becomes stable. Even though there is self-heating effect during the testing procedure, the R_{on} variation of the MOSFETs can still be demonstrated under the almost identical testing condition.

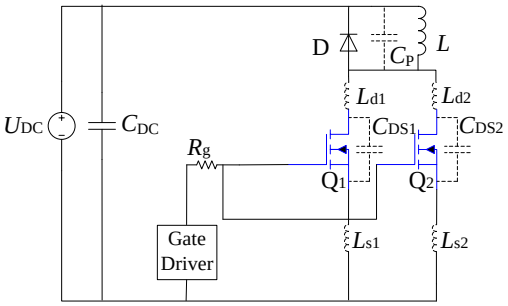


(a) R_{on} Variation

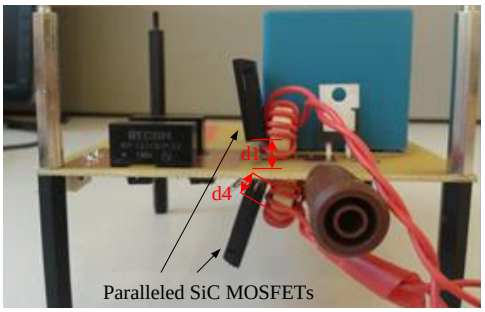


(b) V_{th} Variation

Fig. 2. MOSFETs parameters variation



(a) Double Pulse Test Circuit



(b) Hardware prototype

Fig. 3. Double pulse test circuit and hardware prototype

The current sharing of paralleling SiC MOSFETs is evaluated with a double pulse test circuit, as shown in Fig. 3(a). The hardware implementation is shown in Fig. 3(b). In the simulation and experimental study in this paper, the gate source voltage bias is 25V and -5V unless otherwise specified. Since the device mismatch is of the main concern in this test, two SiC MOSFETs are paralleled in a flipped way, as shown in Fig.3(b),

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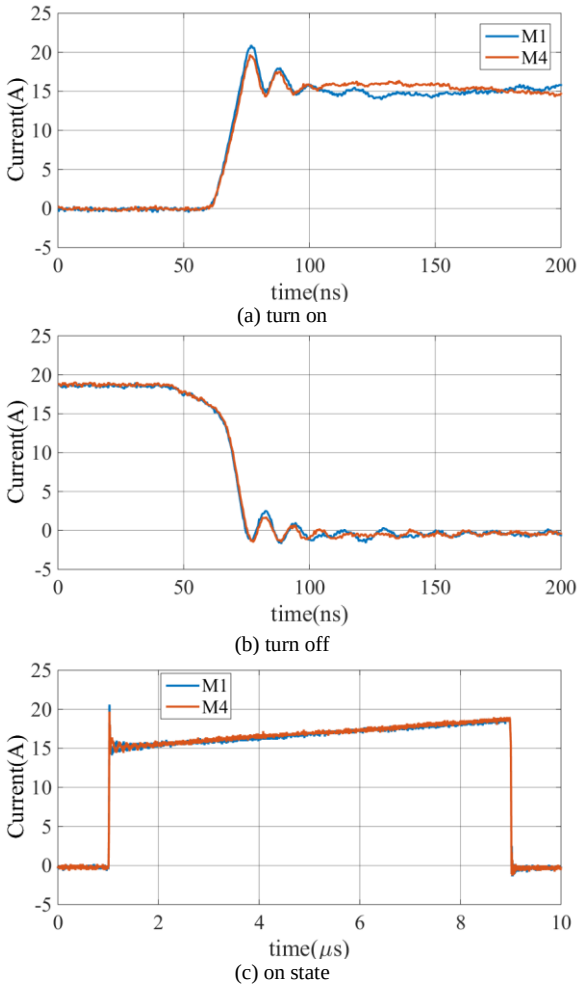
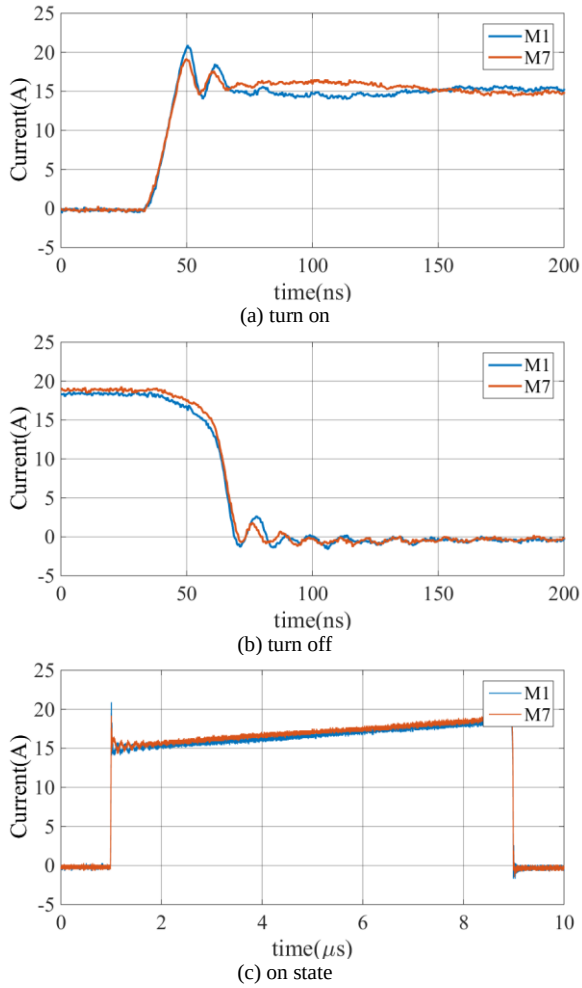


(a) turn on
(b) turn off
(c) on state

Fig. 4. Current sharing performance of M_1 and M_4 with little mismatch



(a) turn on
(b) turn off
(c) on state

Fig. 5. Current sharing performance of M_1 and M_7 with R_{on} mismatch

in order to reduce the influence of circuit mismatch. The MOSFET drain current is measured with a two stage current measurement method, which includes a 10 turns current transformer at the first stage and a Pearson Current Monitor 2877 in the second stage [41].

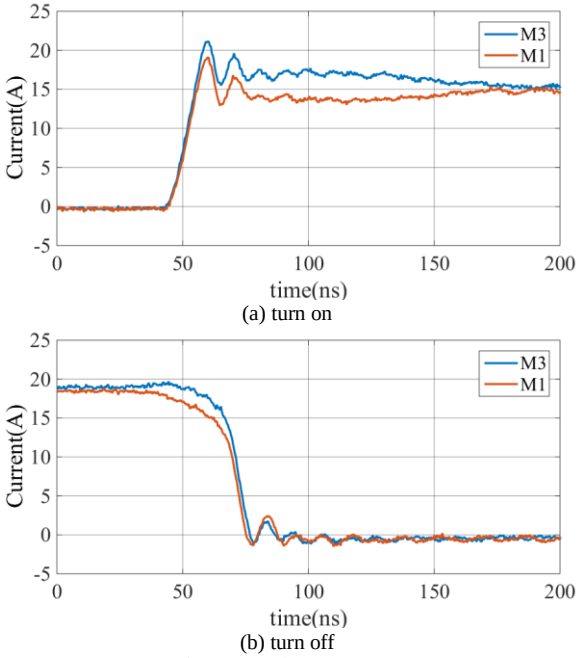
C. *Influences of On-Resistance Mismatch*

SiC MOSFETs M_1 and M_7 are used for the study of R_{on} mismatch influence, as they have nearly same V_{th} but different R_{on}, M_1 has a higher R_{on} than M_7. As shown in Fig. 5(a), during turn-on transient, M_1 and M_7 have identical current. After the turn-on, M_1 has lower current than M_7. M_1 has lower on-state current because of its higher R_{on}, as shown in Fig. 5(c). It is confirmed that the R_{on} mismatch has an impact on on-state current sharing performance but little influence on transient current sharing.

D. *Influences of Threshold Voltage Mismatch*

M_1 and M_3 are selected for the study of V_{th} mismatch influence, as they have nearly identical R_{on} but different V_{th}, M_1 has a higher V_{th} than M_3. The switching transient current sharing with the mismatched V_{th} is given in Fig. 6.

M_3 turns on faster yet turns off slower than M_1. During turn-on, v_{GS} first reach V_{th} of M_3, and then M_3 starts to turn-on and i_{D3} starts rising. When v_{GS} continue increasing and reaches V_{th} of M_1, M_1 turns on and i_{D1} starts rising. However, during turn-off, the process is slightly different. The minimum gate



(a) turn on
(b) turn off

Fig. 6. Current sharing performance of M1 and M3 with V_{th} mismatch

source voltage maintaining the specific drain current is defined as V_p. If the reduced v_{GS} is still larger than V_p, the drain current will not fall and the channel resistance of the SiC MOSFET will increases. Only if v_{GS} keeps decreasing to be lower than V_p, the

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SiC MOSFET will start to work in the saturation region, and the drain current will be determined by v_{GS}. v_{GS} first decreases to the point V_{P1}, at which M_1 cannot sustain its drain current. i_{D1} starts to decrease. v_{GS} continues falling to the point V_{P3}, at which M_3 can no longer sustain i_{D3}, and then i_{D3} starts decreasing. Since the drain current i_D is determined by v_{GS} in the saturation region, as (1).

$$i_D = g_{fs}(v_{GS} - V_{th}) \tag{1}$$

$V_{th1}>V_{th3}$, trans-conductance of these two SiC MOSFET $g_{fs1}=g_{fs3}$ and on-state current $i_{D1}=i_{D3}$ before turning off, $V_{P1}>V_{P3}$. As i_{D1} first decreases but the load inductor current i_L keeps unchanged and the diode is not conducted, M_3 needs to handle more current. Therefore, during turn-off, i_{D3} first increases small amplitude before it starts decreasing, as shown in Fig. 6(b).

III. Circuit Mismatch

A. Circuit Mismatch Description

The difference in switching loop stray inductance (L_d) and common source stray inductance (L_s) are the main causes of current unbalance due to circuit mismatch, as shown in Fig. 3(a). L_{d1} and L_{d2} represent switching loop stray inductance. L_{s1} and L_{s2} are the common source stray inductances. C_P is the total capacitance of the diode junction capacitor and the parasitic paralleled capacitor of load inductor. C_{DS1} and C_{DS2} are junction capacitance of Q_1 and Q_2. The switching loop stray inductance includes the equivalent-series-inductor (ESL) of the dc-link capacitors, the stray inductance of the power connection, including PCB trace and partial inductance from the package of power devices. The common source stray inductance is mainly from the package of SiC MOSFETs and PCB trace which is both in the gate-source loop and drain-source loop. The mismatch of L_d and L_s can easily be increased in the case of paralleling more than two SiC MOSFETs, where an ideally symmetric layout is difficult to achieve, especially when a large heat sink is needed.

In the study of circuit mismatch influence, M_1 and M_4 are selected as they have little device parameter mismatch. The L_s mismatch is realized by different effective source pin length, as shown in Fig.3 (b). d_1 and d_4 are the effective source pin length for M_1 and M_4. L_d mismatch is by inserting different small air core inductors in the drain connection.

B. Influences of Common Source Stray Inductance Mismatch

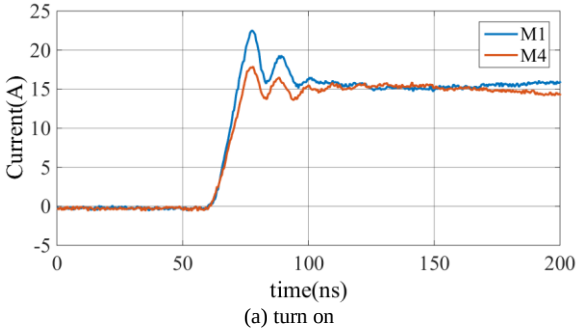
L_s influences the switching characteristics by its negative feedback effect on v_{GS}, which can be explained with (2)-(3) during saturation region in transient switching time. In this condition, SiC MOSFET source current i_s is considered identical with drain i_D, because gate source current is much smaller than the i_D.

$$v_{GS} = V_{driver} - i_G R_G - L_s \frac{di_s}{dt} \tag{2}$$

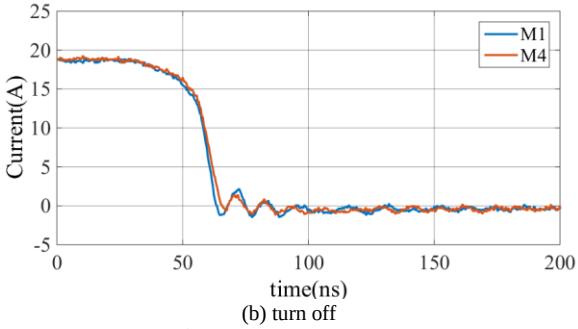
$$i_{D1} - i_{D2} = g_{fs}(L_{s2} - L_{s1}) \frac{di_L}{2dt} \tag{3}$$

According to (2) and (3), during turn-on transient, SiC MOSFET with larger L_s turns on slower and takes less current compared to the one with smaller L_s. During turn-off transient, the SiC MOSFET with larger L_s turns off slower but has more current.

Fig. 7 and Fig. 8 show the L_s mismatch influence on the current sharing performance of paralleled SiC MOSFETs. The L_s mismatch is adjusted by changing the effective source pin lengths, which are specified as d_1 and d_4 in Fig.2 (b). d_1 and d_4 are the source pin length connected to the power loop, i.e. the distance from the PCB trace to the end of the source pin, which can be readily adjusted by lifting the MOSFET up and down with different distances. With L_s mismatch increased, the current unbalance during switching transient also increases. For the SiC MOSFET with larger L_s, both the processes of turn-on and turn-off become slower. The current overshoot of the SiC MOSFET with smaller L_s increases with the increase of L_s mismatch. The current unbalance leads to uneven turn-on and turn-off losses during switching transient.

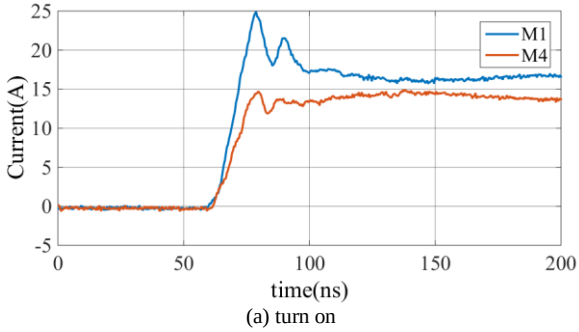


(a) turn on

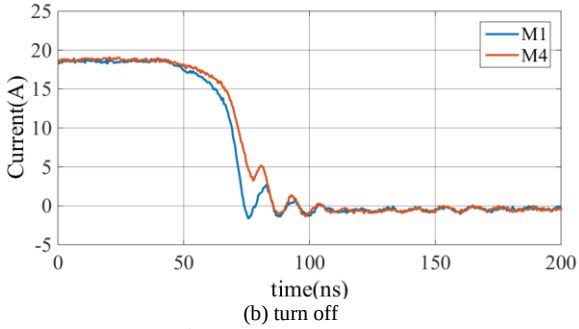


(b) turn off

Fig. 7. Current sharing performance with d1=6mm and d4=10mm



(a) turn on



(b) turn off

Fig. 8. Current sharing performance with d1=6mm and d4=16mm

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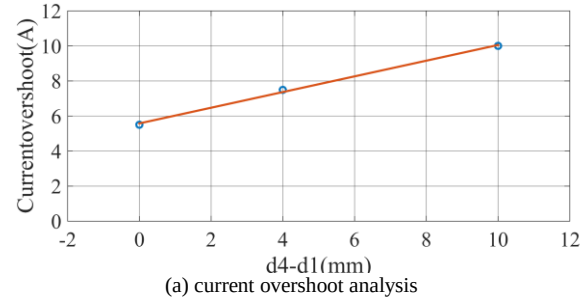
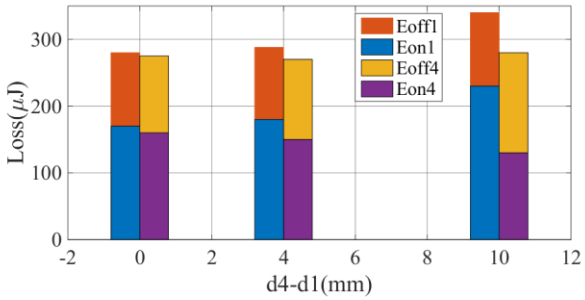
The current overshoot and switching loss analysis are shown in Fig. 9 for different values of (d_4-d_1). E_{on} and E_{off} are SiC MOSFET turn-on loss and turn-off losses. It can be seen from Fig. 9(a) that the current overshoot of the SiC MOSFET increases with the increase of L_s mismatch. On the other hand, L_s mismatch has little effect on the on-state current sharing performance since it affects the current sharing performance through v_{GS}.



(a) current overshoot analysis



(b) switching losses analysis

Fig. 9. Current overshoot analysis and switching losses analysis with Ls mismatch

C. Influences of Switching Loop Stray Inductance Mismatch

The capacitor C_P shown in Fig.3 (a) could lead to a current overshoot during turn-on transient. L_d and C_P form a resonant circuit and causes oscillations in a short period after turn-on. The oscillation frequency could be determined as (4). For the oscillation, R_{on} of SiC MOSFET in series with the equivalent series resistance (ESR) of the dc-link capacitors (R_C) acts as the damping resistor and the damping factor ξ is given by (5).

$$f = \frac{1}{2\pi\sqrt{L_d C_P}} \tag{4}$$

$$\xi = \frac{(R_{on} + R_C)}{2}\sqrt{\frac{C_P}{L_d}} \tag{5}$$

$$f = \frac{1}{2\pi\sqrt{L_d C_{DS}}} \tag{6}$$

$$\xi = \frac{(R_d + R_C)}{2}\sqrt{\frac{C_P}{L_d}} \tag{7}$$

During turn-off, there is a current charging the drain-source capacitor (C_{DS}) of SiC MOSFET. In a short period after turn-off, L_d and C_{DS} form a resonant circuit and the oscillation frequency could be determined as (6). Damping resistor for this oscillation is ESR of DC capacitors and the ESR of diode (R_d). Damping factor ξ is as (7).

With the above analysis, L_d has an influence on the current in a short period after turn-on and turn-off. SiC MOSFET with larger L_d has smaller oscillation frequency and smaller damping factor after turn-on and turn-off. As a result, the SiC MOSFET with larger L_d has a larger current overshoot and the current oscillation amplitude after turn-off is also larger.

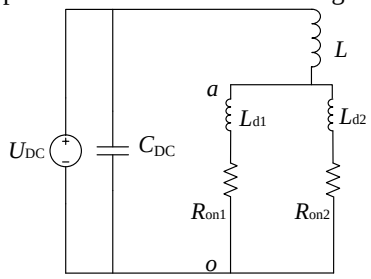


Fig. 10. On-State equivalent circuit of paralleling two SiC MOSFETs

Besides L_d mismatch influences on the transient period current sharing performance, mismatch of L_d also has an impact on the on-state current distribution. During on-state, there are cases that the SiC MOSFETs see an inductive load current and i_D has a changing slope. During on-state period, the equivalent power circuit is shown as Fig. 10. The drain current can be described with (8). In condition of R_{on1}=R_{on2} and di_{D1}/dt=di_{D2}/dt (determined by load), the current difference of i_{D1} and i_{D2} can be determined as (9), which means different L_d lead to different on-state current. Larger L_d results smaller on-state current.

$$\begin{cases} i_{D1} + i_{D2} = i_L \\ L\dfrac{\mathrm{d}i_L}{\mathrm{d}t} + u_{ao} = U_{DC} \\ L_1\dfrac{\mathrm{d}i_{D1}}{\mathrm{d}t} + R_{on1}i_{D1} = L_2\dfrac{\mathrm{d}i_{D2}}{\mathrm{d}t} + R_{on2}i_{D2} \end{cases} \tag{8}$$

$$i_{D1} - i_{D2} \approx \frac{L_{d2} - L_{d1}}{2R_{on}}\frac{U_{DC}}{L} \tag{9}$$

The experiment of L_d mismatch influence is realized by inserting a small inductors in the drain of SiC MOSFET M_1. The experiment results are shown in Fig. 11 and Fig. 12. With the increase of L_d, the current oscillation frequency decreases but the oscillation amplitude increases. With the increases of L_d mismatch, on-state current unbalance increases.

Besides the influence on current, L_d has a large impact on the drain source voltage (V_{DS}) during switching transient. The effect of L_d on a single MOSFET V_{DS} has been analyzed in [29], [30]. The conclusion is with the larger L_d, V_{DS} has larger voltage dip during turn-on and higher voltage overshoot during turn-off, which results a smaller turn-on loss but larger turn-off loss. For the paralleled connection, the experiment results of V_{DS1} and V_{DS4} are given in Fig. 13 and Fig. 14. V_{DS} overshoot and switching losses analysis with L_d mismatch are summarized as Fig. 15.

IV. Current Distribution in SiC MOSFET Multichip Power Modules

A. DBC Layout Mismatch in Multichip Power Modules

To describe the influence of the DBC layout mismatch on the current distribution among the paralleled dies, a SiC MOSFETs multichip power module is considered. Fig. 16 shows the half-bridge SiC power module, which is consisted with 8 SiC MOSFETs dies and 4 of them are in parallel. This power module is made by Danfoss and dedicated for testing the DBC for high current modules.

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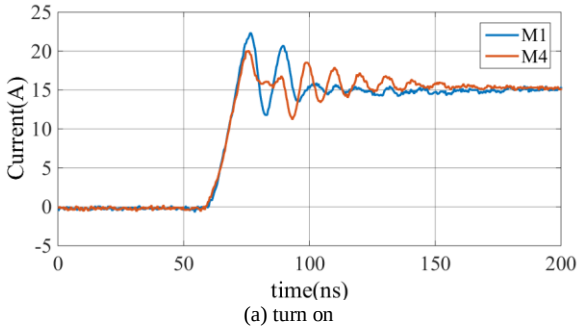
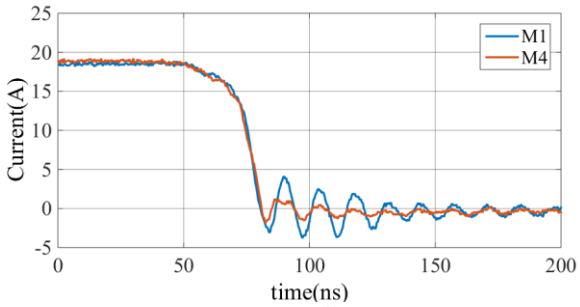
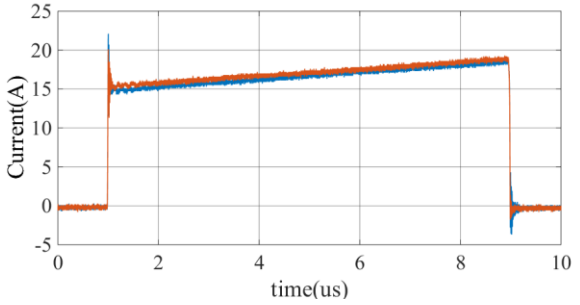


(a) turn on

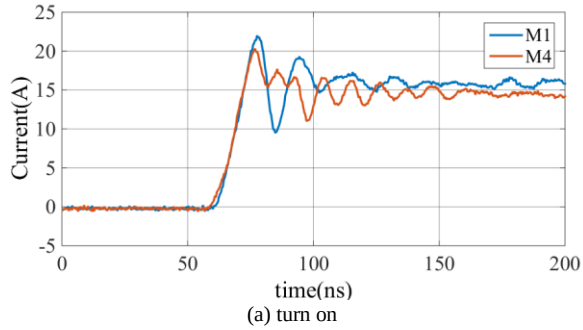


(b) turn off

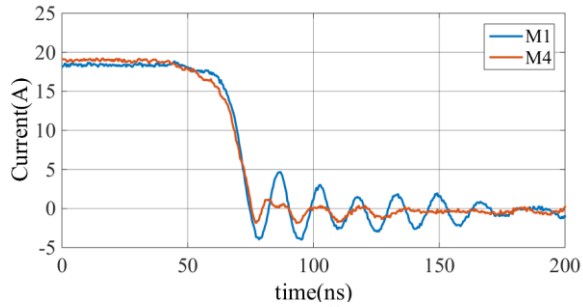


(c) on state

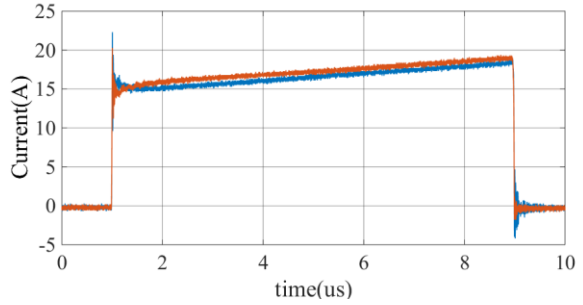
Fig. 11. Current sharing performance with L_{d1}-L_{d4}=66nH



(a) turn on

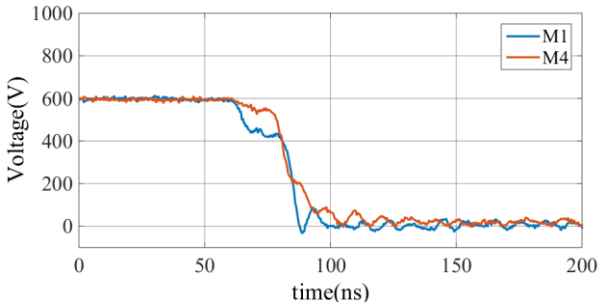


(b) turn off

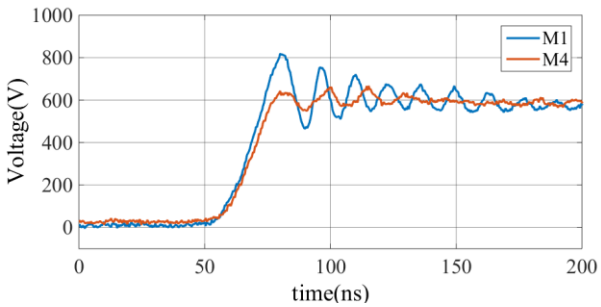


(c) On-state

Fig. 12. Current sharing performance with L_{d1}-L_{d4}=140nH

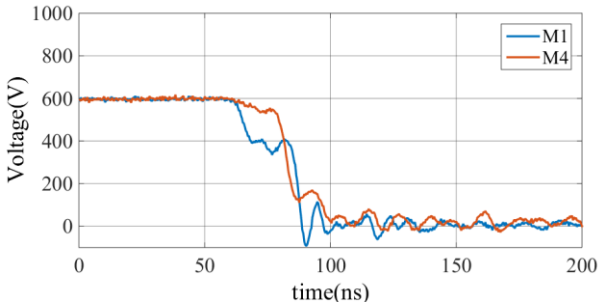


(a) turn on

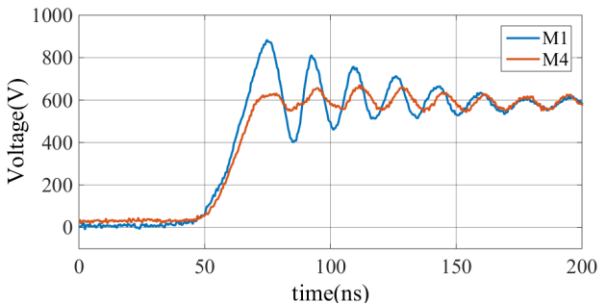


(b) turn off

Fig. 13. Drain-Source voltage of M1 and M4 with L_{d1}-L_{d4}=66nH



(a) turn on



(b) turn off

Fig. 14. Drain-Source voltage of M1 and M4 with L_{d1}-L_{d4}=140nH

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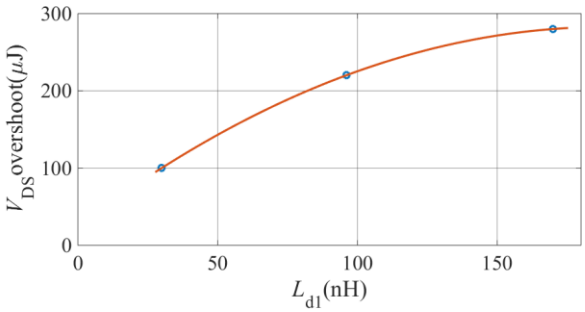
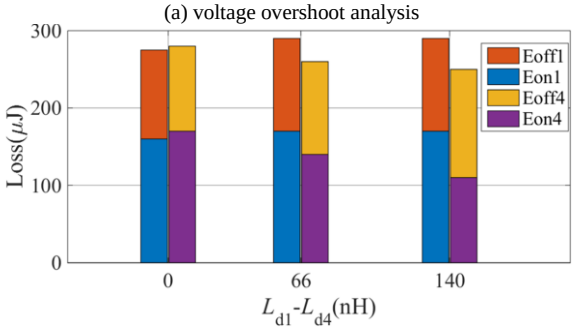


(a) voltage overshoot analysis



(b) switching losses analysis

Fig. 15 Drain-source voltage overshoot analysis and switching losses analysis

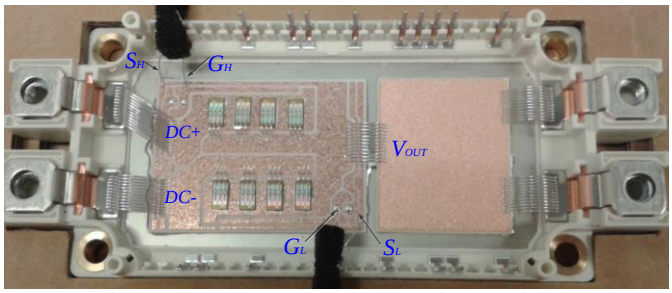


Fig. 16. Half-bridge SiC MOSFET power module from Danfoss

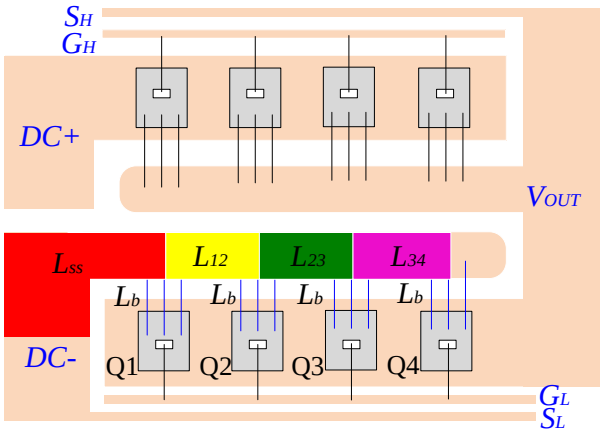
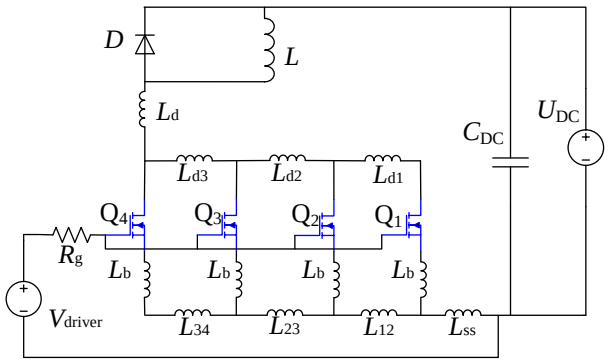


Fig. 17. The layout of SiC MOSFET half bridge power module

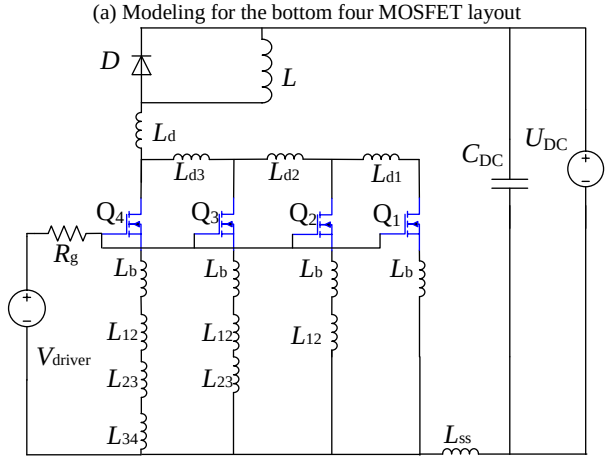
Fig. 17shows the layout of the power module with the stray inductance indicated in different colors. The layout of this power module is designed to minimize mismatch of L_d for the paralleled four SiC MOSFETs dies, Q_1, Q_2, Q_3 and Q_4. However, the common source stray inductance L_s of each die is significantly different from each other. In Fig. 17, L_b is the stray inductance of the source connection bond-wire (blue) for each die. L_{ss} is the stray inductance of the DBC trace (red) from Q_1 to DC negative. L_{12}, L_{23} and L_{34} are the stray inductance of the DBC trace between Q_1 and Q_2 (yellow), Q_2 and Q_3 (green), Q_3 and Q_4 (purple), respectively. According to Fig. 17, the common source stray inductance (L_{s1}, L_{s2}, L_{s3} and L_{s4}) for each SiC MOSFET die can be determined as (10). It is clear that all the four paralleled SiC MOSFET dies have different common source stray inductances.

$$\begin{cases} L_{s1} = L_{ss} + L_b \\ L_{s2} = L_{ss} + L_{12} + L_b \\ L_{s3} = L_{ss} + L_{12} + L_{23} + L_b \\ L_{s4} = L_{ss} + L_{12} + L_{23} + L_{34} + L_b \end{cases} \tag{10}$$

B. Influences of DBC Layout Mismatch and Current Coupling Effect



(a) Modeling for the bottom four MOSFET layout



(b) Artificial DBC layout modeling without current coupling effect

Fig. 18. DBC layout modeling

Besides the mismatch of the common source stray inductance, the paralleled SiC MOSFET dies has current coupling effect between each other, which means the gate source voltage of one SiC MOSFET is affected by the slope of the source current of other three SiC MOSFETs.

$$\begin{bmatrix} i_{D1} \\ i_{D2} \\ i_{D3} \\ i_{D4} \end{bmatrix} = g_{fs} \begin{bmatrix} V_{driver} - i_G R_G - V_{th} - \Delta V_{LS1} \\ V_{driver} - i_G R_G - V_{th} - \Delta V_{LS2} \\ V_{driver} - i_G R_G - V_{th} - \Delta V_{LS3} \\ V_{driver} - i_G R_G - V_{th} - \Delta V_{LS4} \end{bmatrix} \tag{11}$$

The modeling of the power module layout is shown in Fig. 18(a). To describe the current coupling effect, the modeling of an artificial layout is made as shown in Fig. 18(b), which has identical L_s mismatch with Fig. 18(a) but no current coupling effect. For both two modeling, in saturation region during

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transient time, the current can be determined as (11). ΔV_{LS1}, ΔV_{LS2}, ΔV_{LS3} and ΔV_{LS4} are the voltage drop of the common source stray inductance L_{s1}, L_{s2}, L_{s3} and L_{s4}.

For the modeling in Fig. 18(a), ΔV_{LS1}, ΔV_{LS2}, ΔV_{LS3} and ΔV_{LS4} are determined as (12) and the current unbalances between the paralleled dies are as (13). On the other hand, for the modeling of Fig. 18(b) without the current coupling effect, ΔV_{LS1}, ΔV_{LS2}, ΔV_{LS3} and ΔV_{LS4} are determined as (14) and the current unbalances among the paralleled dies are as (15).

In (13) and (15), in high current multichip modules, the current differences slope, e.g. $d(i_{D1}- i_{D2})/dt$, $d(i_{D2}-i_{D3})/dt$, and $d(i_{D3}-i_{D4})/dt$, are much smaller than the sum of drain currents slope, e.g. $d(i_{D2}+i_{D3}+i_{D4})/dt$, $d(i_{D3}+i_{D4})/dt$, and di_{D4}/dt.

Consequently, the bond-wire inductance L_b effect in (13) and (15) could be ignored for the current unbalance analysis. During turn-on transient, the MOSFET drain currents increases. According to (13) and (15), for both these two modeling, the MOSFETs drain currents should follow $i_{D1}> i_{D2}> i_{D3}> i_{D4}$. During turn-off transient, the MOSFET current decreases. The MOSFETs drain current should follow $i_{D1}< i_{D2}< i_{D3}< i_{D4}$. Therefore, in both cases, there are current unbalances during transient switching period. However, compared to that of (15), it is obvious that with the current coupling effect, the current unbalance is larger in (13).

To validate the analysis, simulations of different models in Fig. 18(a) and Fig. 18(b) are made with LTspice. The simulation results can be compared in Fig. 19. With the current coupling effect, the drain current has a larger current overshoot and the current unbalance is also larger. It is clear that the coupling effect worsens the current sharing performance.

$$\begin{bmatrix} \Delta V_{LS1} \\ \Delta V_{LS2} \\ \Delta V_{LS3} \\ \Delta V_{LS4} \end{bmatrix} = \begin{bmatrix} L_b + L_{ss} & L_{ss} & L_{ss} & L_{ss} \\ L_{ss} & L_b + L_{ss} + L_{12} & L_{ss} + L_{12} & L_{ss} + L_{12} \\ L_{ss} & L_{ss} + L_{12} & L_b + L_{ss} + L_{12} + L_{23} & L_{ss} + L_{12} + L_{23} \\ L_{ss} & L_{ss} + L_{12} & L_{ss} + L_{12} + L_{23} & L_b + L_{ss} + L_{12} + L_{23} + L_{34} \end{bmatrix} \begin{bmatrix} i_{D1} \\ i_{D2} \\ i_{D3} \\ i_{D4} \end{bmatrix} \tag{12}$$

$$\begin{cases} i_{D1} - i_{D2} = g_{fs}\left[L_b \dfrac{d(i_{D2} - i_{D1})}{dt} + L_{12} \dfrac{d(i_{D2} + i_{D3} + i_{D4})}{dt} \right] \\ i_{D2} - i_{D3} = g_{fs}\left[L_b \dfrac{d(i_{D3} - i_{D2})}{dt} + L_{23} \dfrac{d(i_{D3} + i_{D4})}{dt} \right] \\ i_{D3} - i_{D4} = g_{fs}\left[L_b \dfrac{d(i_{D4} - i_{D3})}{dt} + L_{34} \dfrac{di_{D4}}{dt} \right] \\ i_{D1} - i_{D4} = g_{fs}\left[L_b \dfrac{d(i_{D4} - i_{D1})}{dt} + L_{12} \dfrac{d(i_{D2} + i_{D3} + i_{D4})}{dt} + L_{23} \dfrac{d(i_{D3} + i_{D4})}{dt} + L_{34} \dfrac{di_{D4}}{dt} \right] \end{cases} \tag{13}$$

$$\begin{bmatrix} \Delta V_{LS1} \\ \Delta V_{LS2} \\ \Delta V_{LS3} \\ \Delta V_{LS4} \end{bmatrix} = \begin{bmatrix} L_b + L_{ss} & L_{ss} & L_{ss} & L_{ss} \\ L_{ss} & L_b + L_{ss} + L_{12} & L_{ss} & L_{ss} \\ L_{ss} & L_{ss} & L_b + L_{ss} + L_{12} + L_{23} & L_{ss} \\ L_{ss} & L_{ss} & L_{ss} & L_b + L_{ss} + L_{12} + L_{23} + L_{34} \end{bmatrix} \begin{bmatrix} i_{D1} \\ i_{D2} \\ i_{D3} \\ i_{D4} \end{bmatrix} \tag{14}$$

$$\begin{cases} i_{D1} - i_{D2} = g_{fs}(\Delta V_{LS2} - \Delta V_{LS1}) = g_{fs}\left[L_b \dfrac{d(i_{D2} - i_{D1})}{dt} + L_{12} \dfrac{di_{D2}}{dt} \right] \\ i_{D2} - i_{D3} = g_{fs}(\Delta V_{LS3} - \Delta V_{LS2}) = g_{fs}\left[L_b \dfrac{d(i_{D3} - i_{D2})}{dt} + L_{23} \dfrac{di_{D3}}{dt} \right] \\ i_{D3} - i_{D4} = g_{fs}(\Delta V_{LS4} - \Delta V_{LS3}) = g_{fs}\left[L_b \dfrac{d(i_{D4} - i_{D3})}{dt} + L_{34} \dfrac{di_{D4}}{dt} \right] \\ i_{D1} - i_{D4} = g_{fs}(\Delta V_{LS4} - \Delta V_{LS1}) = g_{fs}\left[L_b \dfrac{d(i_{D4} - i_{D1})}{dt} + (L_{12} + L_{23} + L_{34}) \dfrac{di_{D4}}{dt} \right] \end{cases} \tag{15}$$

$$i_{D1} - i_{D2} = g_{fs}\left[(L_b + L_{12}) \frac{di_{D2}}{dt} - L_b \frac{di_{D1}}{dt} \right] \tag{16}$$

$$i_{D1} - i_{D2} = g_{fs} \frac{2L_{b1} + L_{s12}}{2L_b + L_{12} + 2L_{b1} + L_{s12}} \left[(L_b + L_{12}) \frac{di_{D2}}{dt} - L_b \frac{di_{D1}}{dt} \right] \tag{17}$$

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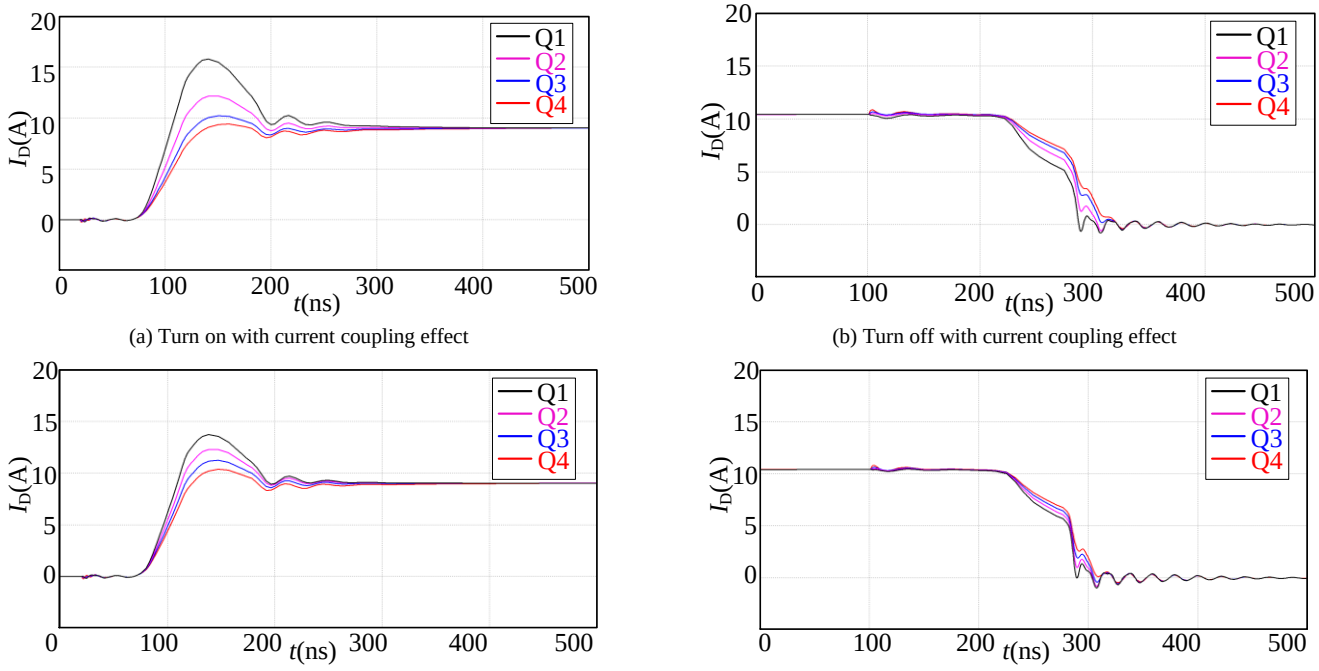


(a) Turn on with current coupling effect

(b) Turn off with current coupling effect

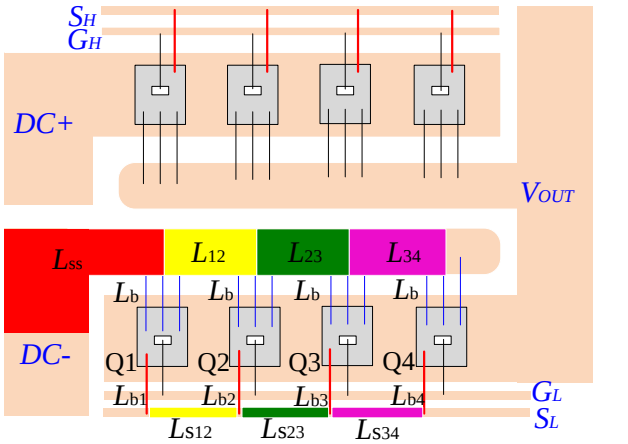
(c) Turn on without current coupling effect

(d) Turn off without current coupling effect

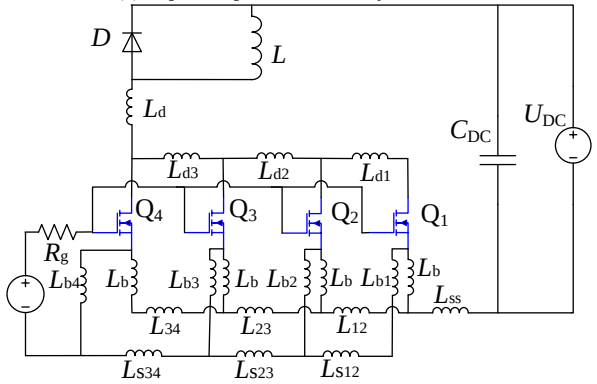
Fig. 19. LTspice simulation results comparison with and without current coupling effect

C. *Improved Layout of SiC MOSFET Power Module*

The difference of modeling in Fig.18 (a) and Fig. 18(b) is the current coupling effect among the paralleled dies. However, a layout corresponding to the model of Fig. 18(b) does not exist in the real power modules.



(a) Improved power module layout

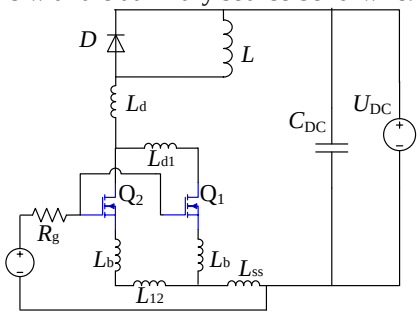


(b) Modeling of improved power module layout

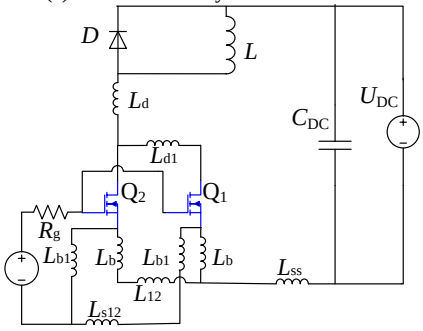
Fig. 20. Improved power module layout and modeling

To reduce the current coupling effect and mitigate the transient current unbalance in the SiC MOSFET power module, a slight modification is introduced based on this layout. An auxiliary source bond-wire for the gate driver source path is added. The new layout is shown in Fig. 20(a). The modeling of the new layout is shown as Fig. 20(b).

To analyze the modeling in Fig. 20(b) and the current distribution with the auxiliary source bond-wire, it is reasonable to simplify the model to paralleling two SiC MOSFETs, as shown in Fig. 21. Fig. 21(a) shows the modeling of paralleling two SiC MOSFETs without the auxiliary source bond-wire. Fig. 21(b) shows the modeling of paralleling two SiC MOSFETs with the auxiliary source bond-wire.



(a) Without auxiliary source connection



(b) With auxiliary source connection

Fig. 21. Modeling of paralleling two SiC MOSFETs

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The current unbalance of the paralleled SiC MOSFETs in Fig 21(a) and Fig. 21 (b) can be described as (16) and (17). With (16) and (17), it is clear that the current unbalance of the paralleled two SiC MOSFETs with the auxiliary source is reduced by a factor of $(2L_{b1}+L_{s12})/(2L_{b1}+L_{s12}+2L_b+L_{12})$. In the case of paralleling more than 2 SiC MOSFETs, the current unbalance can be mitigated even more because the current coupling effect increases with the number of paralleled dies.

The LTspice simulation results of the modeling in Fig. 18(a) are shown in Fig. 22. The simulation results of modeling in Fig. 20(b) with the auxiliary source bond-wire are shown in Fig. 23 and Fig. 24. Compared Fig. 22 and Fig. 23, with the auxiliary source bond-wire, the four paralleled MOSFETs turn on and turn off faster. Meanwhile, the drain current unbalance of the four paralleled MOSFETs is also reduced. To make the comparison fairly, the gate resistance of the simulation of Fig. 24 is increased to make the current rising time (t_r) similarly with that in Fig. 22. In this case, during turn-on, the drain current unbalance of Q_1 and Q_4 is reduced from 7A to 3.5A. The current overshoot of Q_1 is reduced from almost 100% to less than 50%.During turn-off, the current delay among the paralleled dies are reduced.

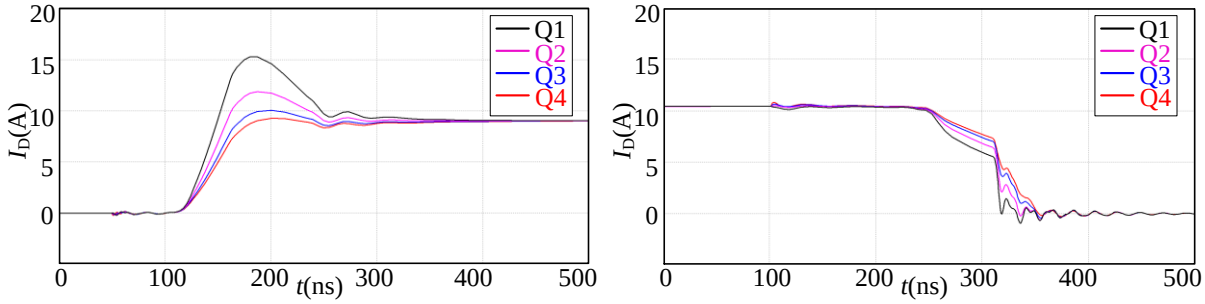


Fig. 22. Current sharing performance without the auxiliary source connection (R_g=10Ω, tr=60ns)

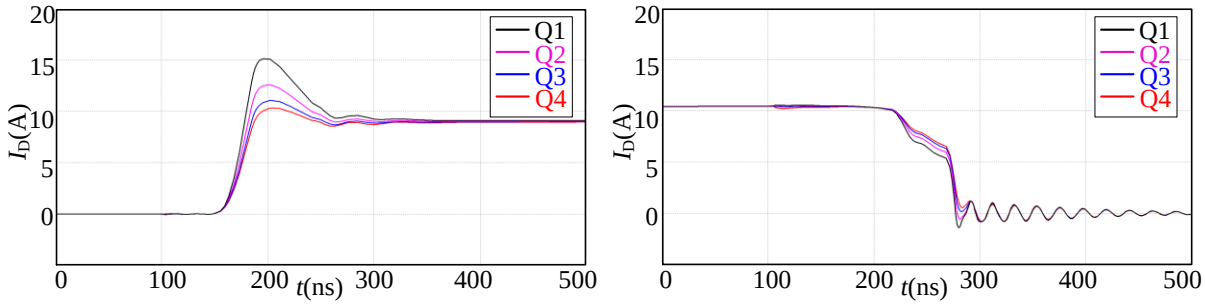


Fig. 23. Current sharing performance with the auxiliary source connection (R_g=10Ω, tr=30ns)

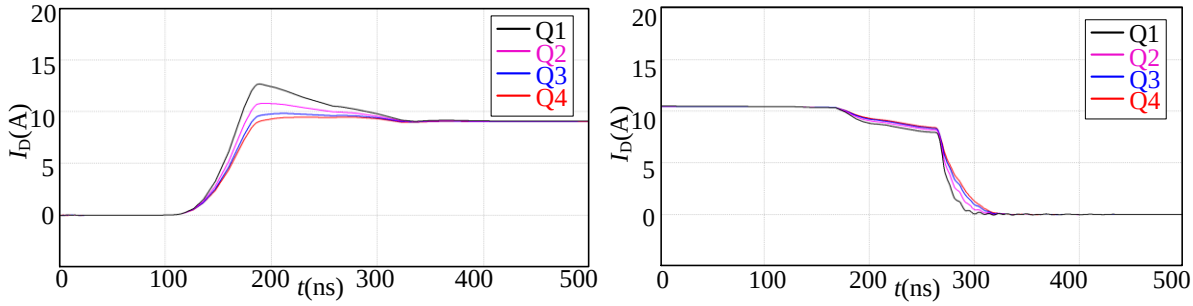
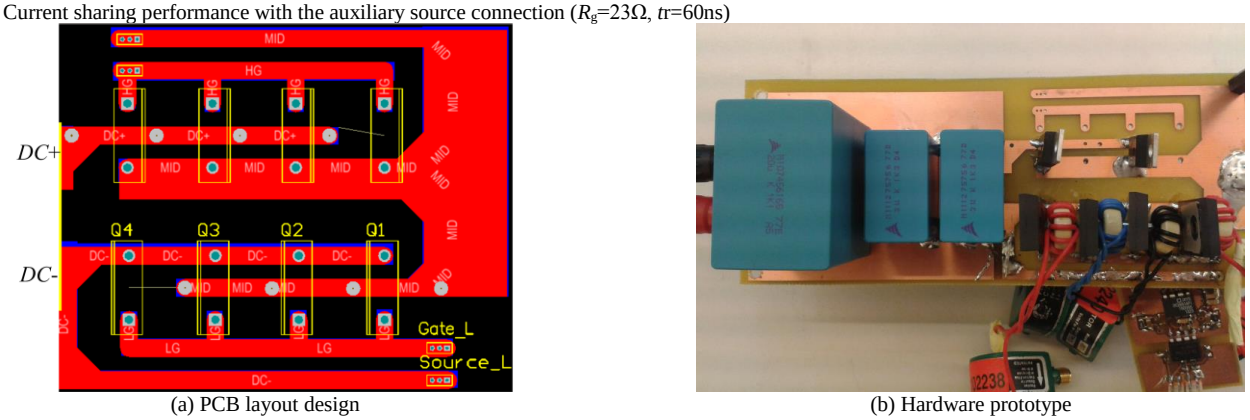


Fig. 24. Current sharing performance with the auxiliary source connection (R_g=23Ω, tr=60ns)



(a) PCB layout design

(b) Hardware prototype

Fig. 25. PCB layout and double pulst test PCB circuit

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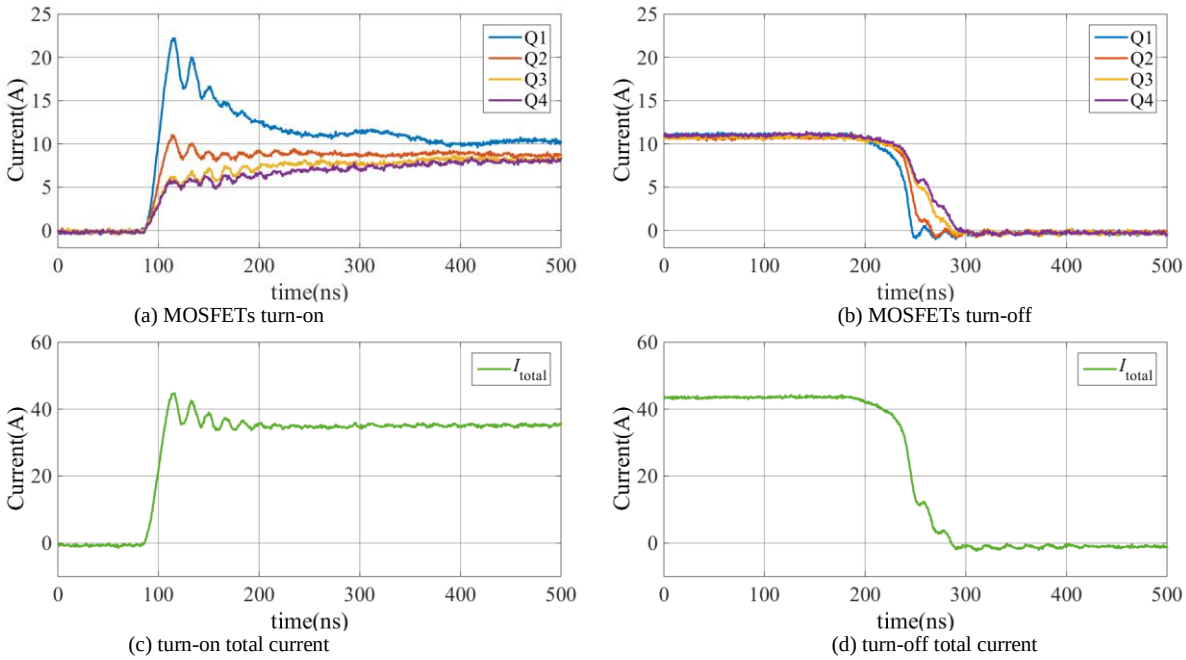
D. *Experimental Study*

The current measurement of dies in the power module is difficult. To experimentally evaluate the current sharing performance in the power module, a PCB circuit with similar layout of the power module is designed as Fig. 25 (a). The hardware setup is shown in Fig. 25 (b).

Fig. 26 shows the experimental results corresponding to the layout of Fig. 18(a), which is without the auxiliary source bond-wire. The largest current unbalance between paralleled SiC MOSFETs is more than 15A while the on state current is only around 10A. Q_1 turns on and turns off fastest and takes highest current during turn-on. The current overshoot of Q_1 is larger than 200%, even though the total turn-on current has only around 30% overshoot, which means Q_1 may be working out of SOA although the total module current is operating within SOA of the power module. This phenomenon may easily lead to device failure.

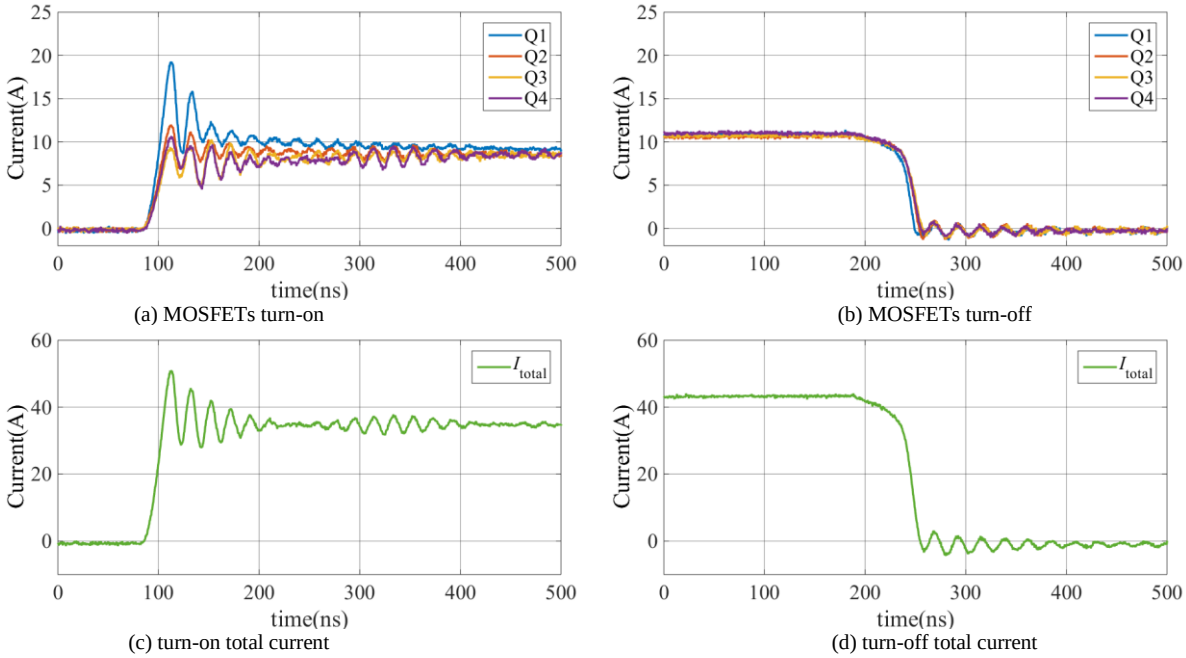
Fig. 27 shows the experimental results corresponding to the layout of Fig. 20(b), which is with the auxiliary source connection. Compared with the experiment results in Fig. 26, the 4 paralleled SiC MOSFETs have a better current sharing performance. The largest drain current overshoot is reduced from 22A to 18A. The current turn-on and turn-off delay between each SiC MOSFET is much smaller, which could mitigate the switching losses unbalance. Moreover, the total current of these 4 SiC MOSFETs turn on and turn off faster.



(a) MOSFETs turn-on (b) MOSFETs turn-off

(c) turn-on total current (d) turn-off total current

Fig. 26. PCB circuit experiment results without the auxiliary source connection



(a) MOSFETs turn-on (b) MOSFETs turn-off

(c) turn-on total current (d) turn-off total current

Fig. 27. PCB circuit experiment results with the auxiliary source connection

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Compared with Fig. 26, the total current even has a higher overshoot and more oscillations during turn-on period. That is because the 4 paralleled SiC MOSFETs has smaller common source inductance, which makes these SiC MOSFETs switch faster. It indicates that a "good" total current performance of the power module cannot prove that the paralleled dies also operate with a "good" current. The paralleled dies in the multichip power module may work in the border or out of the SOA of the SiC MOSFET dies, which affects the reliability of the power module.

With the auxiliary source connection, the current sharing performance is improved. However, the auxiliary source connection is not as good as Kelvin-source connection [42]. In case of 4 SiC MOSFETs are paralleled, Kelvin-source connections for all the paralleled dies could not be achieved. The auxiliary source connection can also take part of the drain current which cannot be avoided in parallel connection. It requires that the auxiliary source bond-wires should be capable of handling power current.

V. Conclusion

This paper presents a systematic analysis on the influences of device and circuit mismatches on paralleling SiC MOSFETs. From the experimental study on the effects of device mismatch and asymmetrical circuit design of paralleled discrete devices, it is shown that the mismatch of the switching loop stray inductance may also lead to on-state current unbalance, besides the different on-state resistance of devices. The mismatch of common source stray inductance causes transient current unbalance. Moreover, from the detailed analysis of the current distribution in a full SiC MOSFET multichip power module, the mismatch of common source stray inductance in the DBC layout is investigated. Furthermore, there is a current coupling effect among the paralleled dies, which is found to have a significant influence on the transient current distribution among the dies. Then, a current coupling mitigation method is developed by introducing an auxiliary source connection bond-wire. Simulation and experimental results validate the analysis and the effectiveness of the developed power module layout.

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