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A Flexible Five-level Cascaded H-bridge Inverter for Photovoltaic Grid-connected Systems

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***Abstract*— With the rapid penetration of photovoltaic (PV) grid-connected system in industrial and commercial application, it is critical to improve the efficiency and enhance the utilization of PV power generation system. This paper proposes a flexible five-level topology based on cascaded multi-level inverter for PV grid-connected system. By adding a bidirectional switch to conventional multi-level inverter, the proposed topology transforms operating mode between two-level H-bridge inverter (HBI) and cascaded multilevel inverter (CMI) according to the variation of DC link voltage. When output voltages of PV arrays are lower, the proposed inverter works in CMI mode to widen the generation range. When output voltages of PV panels are higher, inverter works in HBI mode to increase the efficiency. Hence the system incorporate the low losses feature of HBI and low grid-connected current THD advantages of CMI. This way, a wide range output voltage operation with high efficiency can be achieved without extra DC-DC converter. Experimental results of the proposed five-level CMI are presented to validate the feasibility of the proposed topology.**

***Index Terms*— Multi-level grid-connected inverter, photovoltaic generation, efficiency**

I. INTRODUCTION

Nowadays, fossil fuels such as coal, oil and gas are still supplying most energy for worldwide industry and economy; however they are also considered to be one major reason to cause the environmental pollutions and greenhouse effect [1]. Each country has paid great attention to the environmental issues arising from the fossil energy and economic development, and has made protecting the environment an important aspect of the development plans. Hence, the renewable energy sources such as wind turbines and photovoltaic (PV) systems are certainly going to gain more visibility and value in future smart grid [2],[3].

On the other hand, Solar-electric-energy demand has grown exponentially over the past decades, which is mainly due to the decreasing costs and prices. Nevertheless, the cost of per watt is still relatively higher than other renewable energy sources, current research on PV mainly focus on [3]: 1) increasing efficiency of solar cells; 2) manufacturing-technology improvements; and 3) power electronic conversion efficiency.

Power electronic conversion is a key component to improve the total efficiency and generation range of PV grid connected system [4],[5]. In the existing research work, a wide diversity of PV system structures is introduced based on various kinds of grid-connected inverter topologies. Conventionally, a classification of PV topologies is divided into two major categories: PV inverters with dc/dc converter and PV inverters without dc/dc converter [6],[7]. Another possible classification of PV inverter topologies can be based on the number of cascade power processing stages: single stage and two-stage system [8],[9].

In single-stage grid-connected system, buck-type inverters are usually used to connect PV to the grid, implying that DC voltage should be greater than the amplitude of AC voltage, which cause smaller input voltage and limit the PV generation range [10]. In a two-stage system [11], DC/DC converter is commonly added to the system and control the DC link voltage according to maximum-power-point-tracking (MPPT) control, and the dedicated DC/DC converter can boost the input voltage range. Another option is to use multi-level inverter, in [12] cascade multilevel inverters are taken into consideration to be applied in PV system and a multiple of photovoltaic modules can operate equivalently in series, hence increasing the DC voltage and the system operating range, multi-level topologies also presents the advantage of low grid current THD. However, the inverter loss increases due to the larger number of additional devices and complex structure.

All the PV system aforementioned are based on conventional power electronics topologies, the topology remains unchanged regardless of DC voltage input, while the output voltage of PV arrays varies in a wide range due to its characters and weather circumstance along the day. Therefore, this may result in low utilization, losses and efficiency reduction.

This paper proposes a new single phase inverter topology for PV grid connected system, which can adapt to variable DC input voltage in order to enhance system efficiency and widen the generation range. The proposed inverter operates as a cascaded multi-level inverter (CMI)

to enhance the generation range when DC voltage is lower, and work as a two-level H-bridge inverter (HBI) when DC voltage is higher. In this way, the proposed inverter integrate the advantages of both CMI and HBI to widen operation range in low DC voltage zone and reduce losses in high DC voltage zone. The rest of paper is organized as follows. Section II introduces the structure, graph analysis and the SPWM schemes of proposed flexible cascaded multilevel topology; section III shows the losses analysis of proposed inverter under different modes; finally the experimental results of Section IV validate the feasibility of proposed topology.

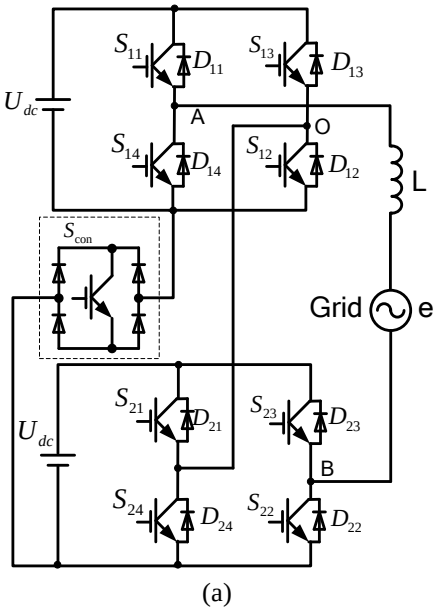
II. Proposed Five-level Cascaded H-bridge Inverter

A. Structure description of proposed inverter

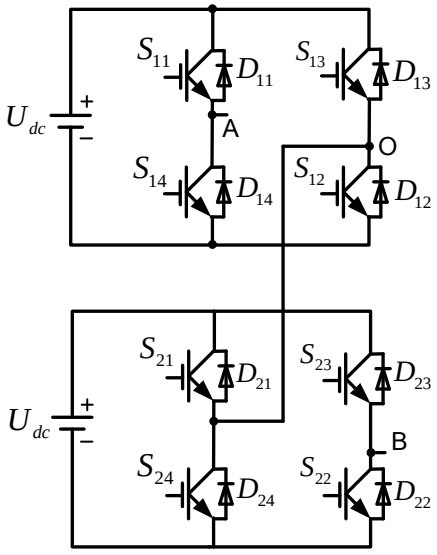
In order to realize a wide generation range with high efficiency, the flexible cascaded multilevel inverter topology is proposed, shown in Fig. 1(a). It consists of two H-bridge inverter connected between their negative terminals through a bidirectional static switch S_{con}, and the middle point of one of their legs (O) and the middle point of the other legs (A and B) is connected to the grid through a inductor filter. The topology operation is presented as follows:

(i) When S_{con} is off, the inverter is a conventional cascaded five-level inverter, as is shown in fig. 1(b);

(ii) When S_{con} is on, the negative terminals are connected, and S_{12}, S_{24} are off and S_{13}, S_{21} are on, the positive terminals are connected, the inverter switch to HBI mode, as is shown in Fig. 1(c). Then the two DC sources will work in parallel to share the power supply for grid. It is required that the output characteristics of two DC sources should be the same.



(a)



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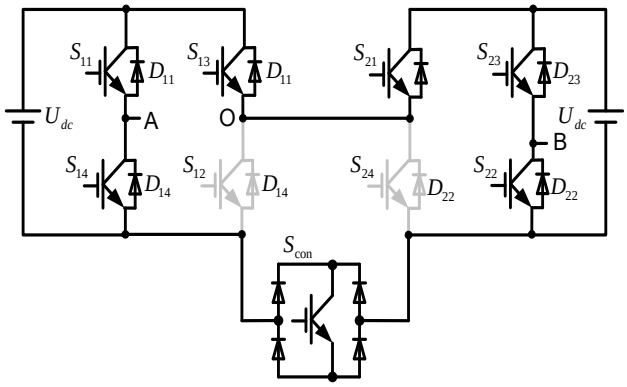


(c)

Fig.1. Schematic diagram of proposed on-line topology-variable inverter. (a) proposed inverter, (b) CMI mode, (c) HBI mode

B. Graph analysis

Based on the graph theory, the cascaded multilevel inverter topology can be modeled as a directed graph composed of nodes and edges, as is show in Fig 2, Node 1 and 3 respectively represent positive terminals of two DC power supplies, while nodes 2 and 4, represent associated negative terminals. Node 6 is the connection point of two H-bridges in cascaded inverter, nodes 5 and 7 are the points connected to the output filter and grid when the inverter is grid-connected.

Based on the simplified graph Fig. 5, the connectivity matrix of CMGI C_1 is obtained:

$$C_1 = \begin{vmatrix} 1 & 0 & 0 & 0 & S_{11} & S_{13} & 0 \\ 0 & 1 & 0 & 0 & S_{14} & S_{12} & 0 \\ 0 & 0 & 1 & 0 & 0 & S_{21} & S_{23} \\ 0 & 0 & 0 & 1 & 0 & S_{24} & S_{22} \\ S_{11} & S_{14} & 0 & 0 & 1 & 0 & 0 \\ S_{13} & S_{12} & S_{21} & S_{24} & 0 & 1 & 0 \\ 0 & 0 & S_{23} & S_{22} & 0 & 0 & 1 \end{vmatrix} \quad (1)$$

The paths connecting node 1 and node 3 (positive terminal of DC link) can be expressed by a cofactor:

$$\Delta_{13}=\begin{vmatrix} 0 & 1 & 0 & S_{14} & S_{12} & 0 \\ 0 & 0 & 0 & 0 & S_{21} & S_{23} \\ 0 & 0 & 1 & 0 & S_{24} & S_{22} \\ S_{11} & S_{14} & 0 & 1 & 0 & 0 \\ S_{13} & S_{12} & S_{24} & 0 & 1 & 0 \\ 0 & 0 & S_{22} & 0 & 0 & 1 \end{vmatrix} \tag{2}$$

Then values cofactor, and ignore the squared term, the switching function can be obtained:

$$\begin{aligned} F_{13} &= S_{13}\cdot S_{21}+S_{13}\cdot S_{24}\cdot S_{22}\cdot S_{23}+S_{11}\cdot S_{14}\cdot S_{12}\cdot S_{21} \\ &\quad +S_{11}\cdot S_{14}\cdot S_{12}\cdot S_{24}\cdot S_{22}\cdot S_{23} \end{aligned} \tag{3}$$

F_{13} expresses all the paths connecting node 1 and node 3, and considering the IGBTs in the same arm cannot be on simultaneously, so the path connecting the positive of two bridges is only the route of $S_{13}\cdot S_{21}$

Accordingly, The paths connecting node 2 and node 4 (negative terminal of DC link) can be expressed by cofactor:

$$\Delta_{24}=\begin{vmatrix} 1 & 0 & 0 & S_{11} & S_{13} & 0 \\ 0 & 0 & 1 & 0 & S_{21} & S_{23} \\ 0 & 0 & 0 & 0 & S_{24} & S_{22} \\ S_{11} & S_{14} & 0 & 1 & 0 & 0 \\ S_{13} & S_{12} & S_{21} & 0 & 1 & 0 \\ 0 & 0 & S_{23} & 0 & 0 & 1 \end{vmatrix} \tag{4}$$

Accordingly ignoring the squared term the switching function F_{24} is calculated:

$$\begin{aligned} F_{24} &= S_{12}\cdot S_{24}+S_{12}\cdot S_{21}\cdot S_{23}\cdot S_{22}+S_{14}\cdot S_{11}\cdot S_{13}\cdot S_{24} \\ &\quad +S_{14}\cdot S_{11}\cdot S_{13}\cdot S_{21}\cdot S_{23}\cdot S_{22} \end{aligned} \tag{5}$$

F_{24} expresses all the paths connecting node 2 and node 4, and considering the IGBTs in the same arm cannot be on simultaneously, so the path connecting the negative of two bridges is only the route of $S_{12}\cdot S_{24}$.

From the analysis above, in order to achieve the parallel operation of the two DC sources only by the internal paths of cascaded inverter, the $S_{13}-S_{21}$ and $S_{12}-S_{24}$ should be on at the same time. However, the IGBT S_{13},S_{12} and S_{21},S_{24} are in the same arm and cannot be on simultaneously. So the parallel connection of inverters cannot be achieved only using internal paths.

Therefore, a bidirectional switch is added to the circuit to provide a path to connect the negative terminals of two DC source and ensure the power bidirectional flow, meanwhile connect the positive terminals through the internal path $S_{13}-S_{21}$. Thereby, the parallel operation of inverters and topology switching could be implemented.

C. SPWM scheme for proposed inverter

The cascaded 3-level inverter can be controlled in the unipolar carrier-shifting SPWM, where a sine reference is compared with 4 triangle carriers which are 90 degrees out of phase with each other. On the other hand, the 2-level inverter can be controlled in the unipolar SPWM, in which a sine reference is compared with 2 triangle carriers which are 180 degrees out of phase with each other.

Actually, two carriers of the SPWM schemes for 3-level and 2-level inverter are totally the same if the carrier frequency is same. So a Carrier-Shifting Carrier-Multiplexing SPWM (CSCMSPWM) for the flexible multilevel inverter is proposed, as is shown in Fig 4: The dead time should be set between two complementary switches, and hence when system operates in 3-level mode, the bidirectional switch is off. A sine reference U_r is compared with 4 carriers $Tri1$, $Tri2$, $Tri3$, $Tri4$, the comparison signals of U_r and $Tri1$ are the control signals of S_{11}, and its logic inversion signal is as the control signal of S_{14}, the comparison signals of U_r and $Tri2$ are the control signals of S_{12}, and its logic inversion signal are the control signal of S_{13}, the comparison signals of U_r and $Tri3$ are as control signals of S_{21}, and its logic inversion signal is as the control signal of S_{24}, the comparison signals of U_r and $Tri4$ are control signals of S_{22}, and its logic inversion signals are the control signal of S_{23}.

When the system operation mode switches to 2-level mode, the bidirectional switch is on. And two carriers $Tri3$, $Tri4$ are cut down, and keep the IGBT S_{13}, S_{21} on, and S_{12}, S_{24} off. The comparison signals of U_r and $Tri1$ are as control signals of S_{11}, and its logic inversion signal is as the control signal of S_{14}, the comparison signals of U_r and $Tri2$ are as control signals of S_{22}, and its logic inversion signal is as the control signal of S_{23}. In CSCMSPWM, the output frequency reaches 4 times carrier frequency in 3-level mode, and 2 times carrier frequency in 2-level mode.

III. LOSSES ANALYSIS

Based on the modulation scheme shown in Fig. 2, the features of two operation modes are compared by analyzing losses and grid current THD. The inverter losses mainly include conduction losses, switching losses, diodes turn-off losses [13]. The power switch device losses are analyzed, for one power switching device IGBT, its conduction losses are :

$$p_{scon}\approx\left[V_{ceo}+R_{ons}i\right]i \tag{6}$$

Where V_{ceo} and R_{ons} are collector-emitter saturation voltage and conduction resistor respectively, i is the instantaneous grid current value.

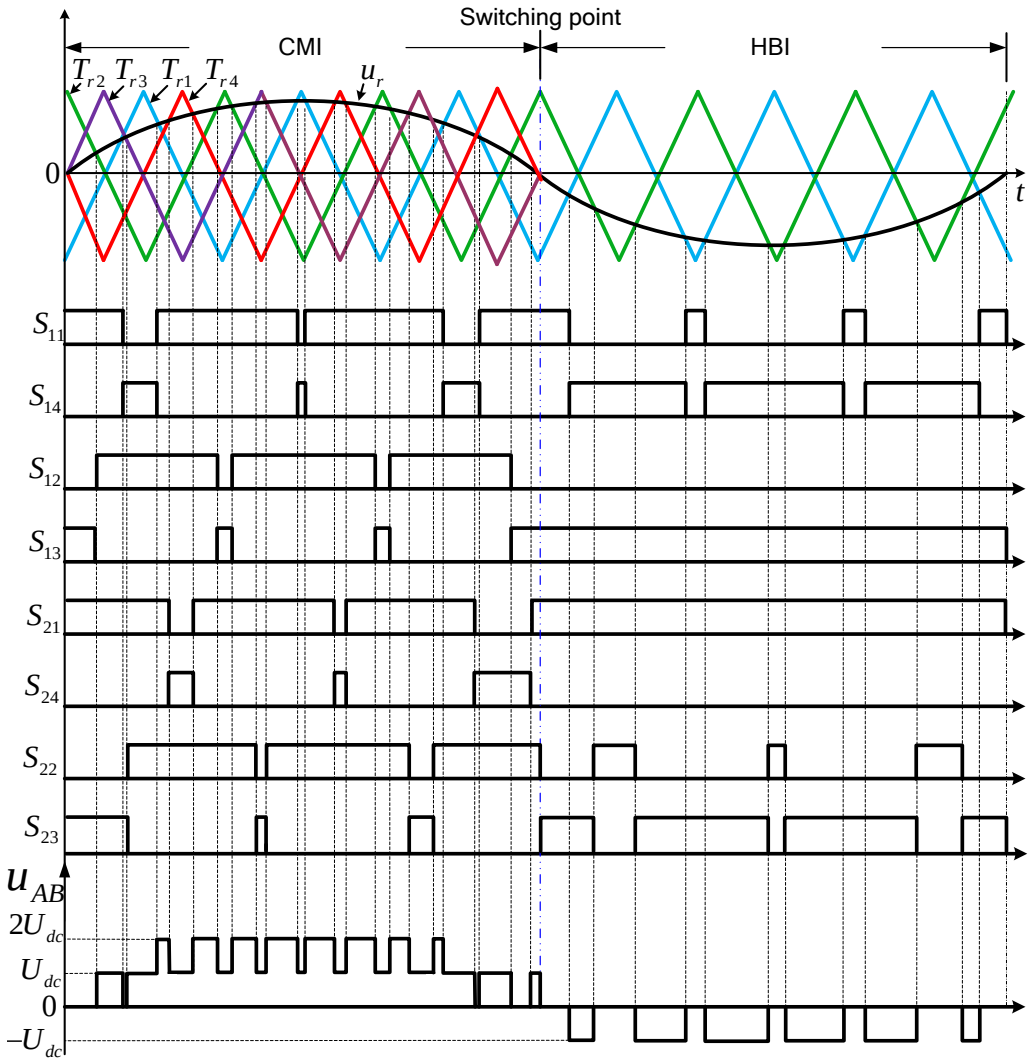


Fig.2 SPWM scheme for proposed inverter

The diodes conduction power losses of can be expressed as:

$$p_{dcon} \approx [V_{do} + R_{ond} i] i \tag{7}$$

Where V_{do} and R_{ond} are diode conduction saturation voltage and conduction resistor respectively.

The total switching losses of Power switching devices and diodes in a switching cycle $T_s = 1/f_s$ can be expressed as follows:

$$P_{sw} = f_s (E_{on1} + E_{off1} + E_{offD1}) \frac{i}{I_{co}} \frac{U_{dc}}{U_{ceo}} \tag{8}$$

Where E_{on1}, E_{off1} and E_{offD1} are IGBT turn-on energy, IGBT turn-off energy and diode turn-off energy respectively. U_{ceo} is the DC bus voltage .

Fig.2 shows, in a carrier cycle for the CMI mode that, the output voltage presents four levels, while for HBI mode, the output voltage only two levels, each level change corresponds to a switched-off power device, a diode in conduction state, a power device in on-state and a diode in off-state. Further the number of on-state power device in one carrier cycle of CMI and HBI mode are shown in Table I. Note that, in HBI mode the current through the two IGBT and diodes is half than that in CMI mode.

From Table I, in CMI mode the average total losses of power devices in one carrier cycle can be obtained as following:

$$P_{cas} = 2P_{scon} D(\omega t) + 2P_{scon} + 2P_{dcon} [1 - D(\omega t)] + 4P_{sw} \tag{9}$$

In HBI mode, average total losses in one carrier cycle yields to:

$$P_{Hb} = P_{scon} D(\omega t) + 2P_{scon} + 2P_{dcon} + P_{dcon} [1 - D(\omega t)] + 2P_{sw} \tag{10}$$

From the equation (9) and (10), the difference of conduction losses between CMI and HBI is small, while the switching losses in CMI is double in HBI mode, hence the total power device losses in CMI mode is higher than HBI mode. The curves of the total losses corresponding to various DC output voltages of the PV array are drawn based on the former theoretical analysis

results and shown in Fig. 3, and the devices parameter is based on the datasheet of FF600R1KL4C from Infineon Technologies Co. Ltd..

TABLEI The number of on-state power device in one carrier cycle of CMI and HBI mode

Topology mode	DC source output power		Fly-back		Switching times
	IGBT	diode	IGBT	diode	
CMI mode	4	0	2	2	4
HBI mode	3	3	2	2	2

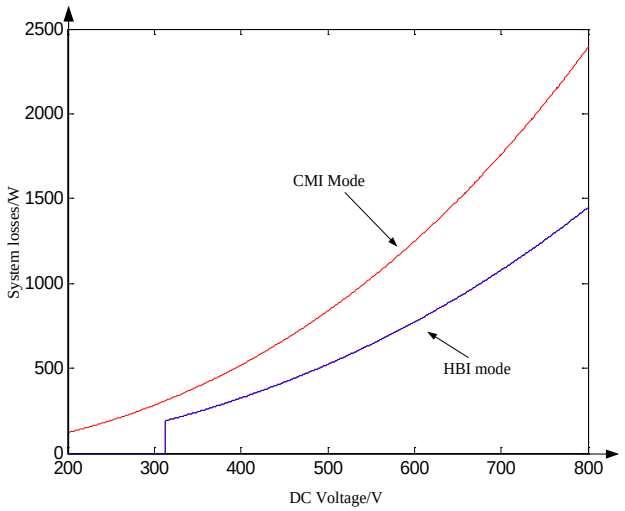


Fig.3 system power devices losses in CMI and HBI mode

IV. EXPERIMENTAL RESULTS

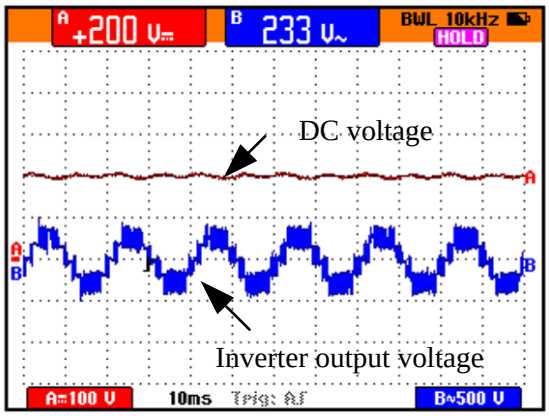
The experimental setup for the flexible multi-level grid-connected inverter was built based on a DSPTMS28335 and FPGA EP1C6T144I7 Platform. The inverter is connected to the grid through a inductor filter. The PR current controller and Phase PLL Loop (PLL) are implemented for grid synchronization in DSP, and PWM scheme and mode switching control are implemented in FPGA. The relative parameters are presented in Table II.

TABLE II. Parameters of experimental prototype

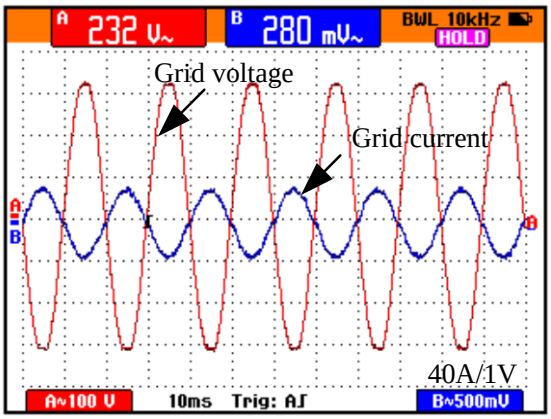
Parameter	Value	Parameter	Value
U_{dc}	200-450V	I_m	24-56A
E_m	311V	f_c	5kHz
ω	50Hz	L	1.5mH

A. CMI mode test

First the low DC voltage condition is tested when the input voltage is 200V, HBI mode cannot operate at this voltage level. The system works in CMI mode and the cascaded output voltage meet the grid connected requirement, as is shown in Fig. 4(a), and the waveforms of grid current and grid voltage are presented in fig. 4(b), where a sinusoidal output grid current can be observed.



(a)

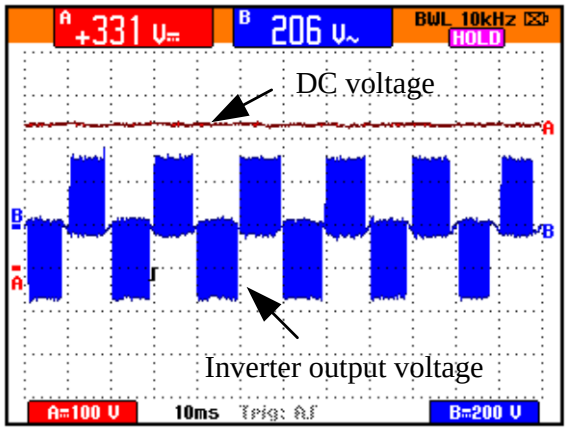


(b)

Fig.4 the experimental results in CMI mode (a) DC voltage and inverter output voltage (b) grid voltage and current

B. HBI mode test

In this section, high DC voltage condition is tested when the input voltage is 331V, system works in HBI mode to reduce the losses and the output voltage can meet the grid connected requirement, as is shown in Fig. 5(a), a sinusoidal output grid current out of phase with grid voltage can also be observed in fig. 5(b),



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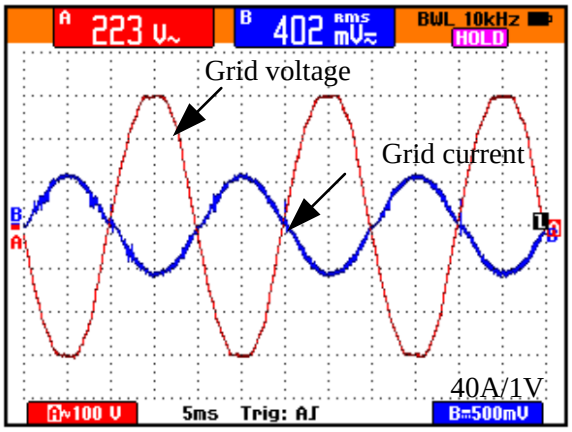
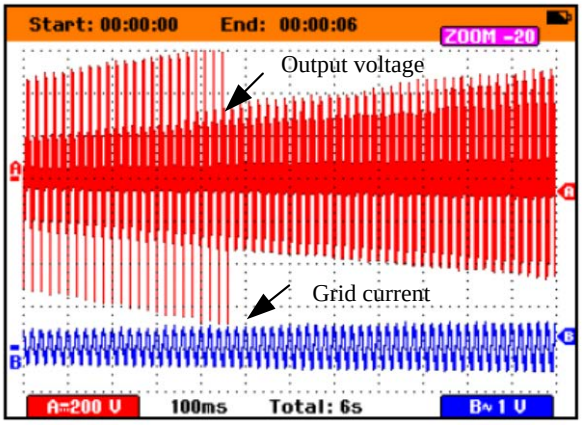


(b)

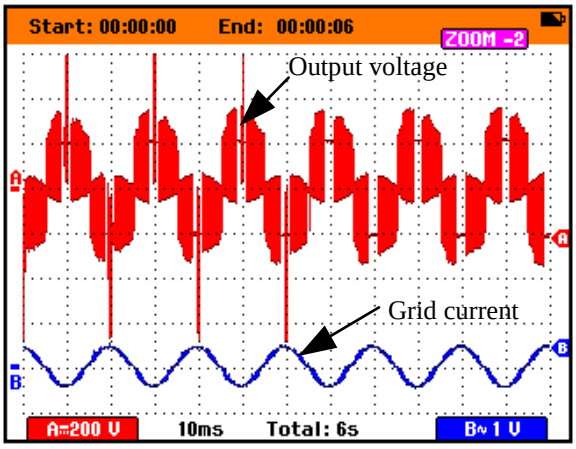
Fig.5 the experimental results in CMI mode (a) DC voltage and inverter output voltage (b) grid voltage and current

C. Mode switching test

In this section, DC voltage changes from 200V to 450V, and around 380V, the inverter transform from CMI mode to HBI mode. The output voltage of inverter, DC voltage and system efficiency is presented in Fig. 6. It can be observed that when the inverter changes from CMI to HBI mode, the system can still operate stably and the system efficiency obtain an obvious boost.



(a)



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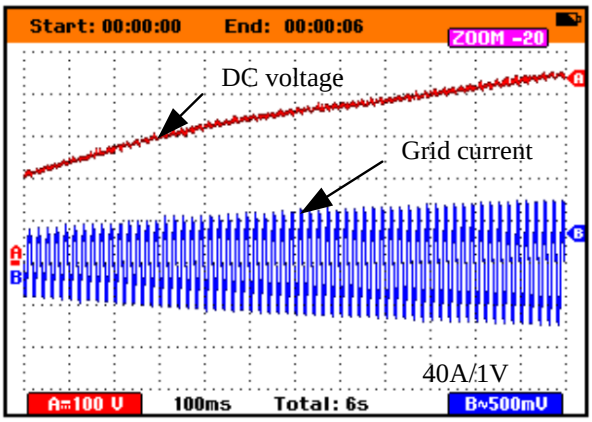
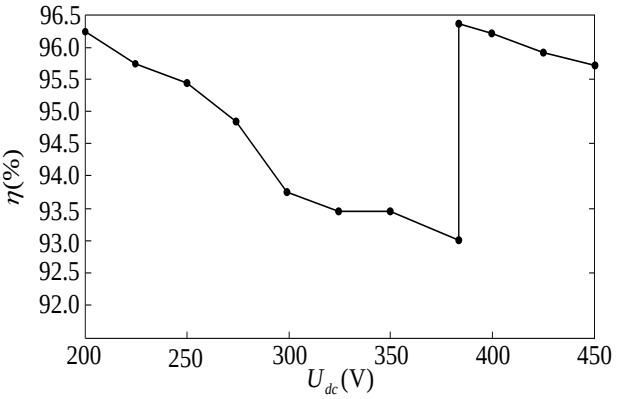


(c)



(d)

Fig.7 Experiment waveforms of operation modes switching (a) output voltage and grid current (b) zoomed-in output voltage and grid current (c) DC voltage and grid current (d) inverter efficiency

V. Conclusion

In order to achieve a wide generation range and efficiency improvement of PV grid connected system, this paper proposed a flexible cascaded multilevel inverter which can transform its operation modes between CMI and HBI according to the wide DC voltage varying of PV arrays. The corresponding experimental results validate the feasibility of proposed topology. In future work, current THD and more intelligent mode switching control will be studied.

ACKNOWLEDGEMENT

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