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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2015.2462082

Publication date:
2016

Document Version
Early version, also known as pre-print

Link to publication from Aalborg University

Citation for published version (APA):
Golestan, S., Guerrero, J. M., Vidal, A., Yepes, A. G., Doval-Gandoy, J., & Freijedo Fernandez, F. D. (2016). Small-Signal Modeling, Stability Analysis and Design Optimization of Single-Phase Delay-Based PLLs. *I E E E Transactions on Power Electronics*, *31*(5), 3517-3527. https://doi.org/10.1109/TPEL.2015.2462082

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Small-Signal Modeling, Stability Analysis and Design Optimization of Single-Phase Delay-Based PLLs

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***Abstract*—Generally speaking, designing single-phase phase-locked loops (PLLs) is more complicated than three-phase ones, as their implementation often involves the generation of a fictitious orthogonal signal for the frame transformation. In recent years, many approaches to generate the orthogonal signal have been proposed, the simplest perhaps being the transfer delay based method. In the transfer delay based PLL (TD-PLL), the orthogonal signal is generated by delaying the original single-phase signal by $T/4$ (one-quarter of a period). The phase shift caused by the transfer delay block, however, will not be exactly 90° under off-nominal grid frequencies, which results in errors in the estimated quantities by the TD-PLL. To alleviate this issue, an improved version of TD-PLL, called the non-frequency dependent TD-PLL (NTD-PLL), has recently been proposed. The NTD-PLL uses another $T/4$ delay unit in its feedback path to make the PLL immune to grid frequency variations. To the best of the authors' knowledge, the accurate small-signal modeling of the TD-PLL and NTD-PLL has not yet been carried out, and no detailed analysis of their performance has been presented. The main aim of this paper is to address these issues and explore new methods to enhance their performance. The stability analysis, control design guidelines and performance comparison with the state-of-the-art PLLs are presented as well.**

***Index Terms*—Orthogonal signal generator, phase-locked loop (PLL), synchronization.**

I. Introduction

A phase-locked loop (PLL) is a negative-feedback system that tries to generate a sinusoidal signal with the same phase and frequency as its input signal [1]. PLLs are now widely used for synchronization and control purposes in the areas of electrical machines, power distribution systems and power electronics thanks to the great advantages that they offer, such as their ease of digital implementation, effectiveness and robustness [2]-[4]. The phase detector (PD), the loop filter and the voltage controlled oscillator are three basic parts of almost all PLLs [1].

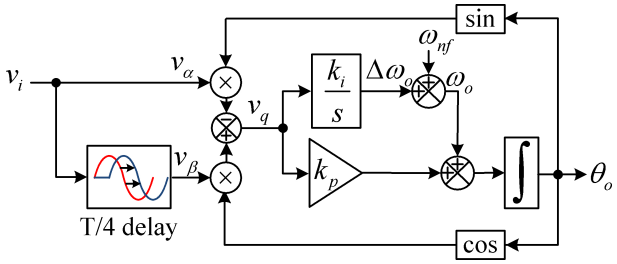

Fig. 1. Schematic of the TD-PLL.

In recent years, many single-phase PLLs have been designed by different researchers. The main difference among these PLLs typically lies in the implementation of their PDs. A mixer, also called the product type PD, is probably the simplest option [1]. This PD generates the phase error information by multiplying the PLL input signal by the PLL output. This multiplication, nevertheless, causes a double frequency component at the mixer output, which results in double frequency ripples on the quantities estimated by the PLL [5]. To deal with this problem of product type PDs, including double frequency decoupling networks into the PLL structure is suggested in [6]-[8].

The orthogonal signal generation (OSG) based PDs are presumably the most popular PDs in single-phase PLLs. The main difference among these PDs typically lies in the technique they use to create the orthogonal signal. The transfer delay [9], [10], all-pass filter [11], Hilbert transform [12], Kalman filter [13], second order generalized integrator [14], [15] and inverse Park technique [5], [15] are the most common methods to create the orthogonal signal.

Using the transfer delay is probably the simplest method to generate the orthogonal signal. Fig. 1 shows the schematic diagram of the single-phase transfer delay based PLL (TD-PLL). As illustrated in this figure, the orthogonal signal is generated by delaying the original single-phase signal by $T/4$, where T is the grid fundamental period. This approach, however, suffers from high sensitivity to the grid frequency variations, because the phase shift caused by the transfer delay will not be exactly 90° in the presence of frequency drifts. To deal with this problem, the frequency estimated by the PLL can be fed

This work was supported in part by the Research Programme on Microgrids, Department of Energy Technology, Aalborg university, in part by the Spanish Ministry of Science and Innovation, and in part by the European Commission, European Regional Development Fund (ERDF) under Project DPI2012-31283.

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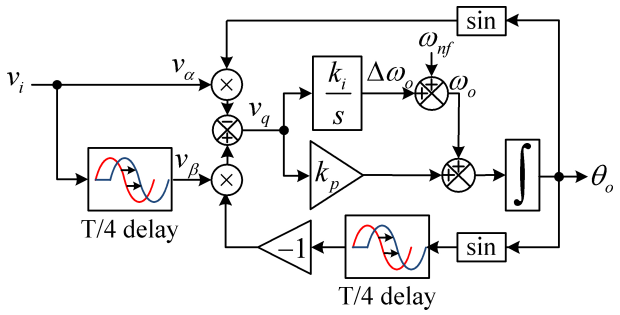

Fig. 2. Block diagram of the NTD-PLL.

back to the delay block to make it frequency adaptive. This frequency feedback loop, nevertheless, makes the PLL highly nonlinear. In this condition, it is rather difficult to analyse the PLL and ensure its stability under all circumstances [16]. Recently, another approach has been proposed in [17] and [18] to tackle this problem. In this method, as shown in Fig. 2, the TD-PLL uses another delay block in the feedback loop to generate $\cos(\theta_o)$ from $\sin(\theta_o)$, where θ_o is the phase estimated by the PLL. This PLL structure is called the non-frequency dependent TD-PLL (NTD-PLL).

In this paper, for the first time, the accurate small-signal modeling of the TD-PLL and NTD-PLL is presented. A detailed analysis of the performance of these PLLs is then carried out and some approaches to enhance their performance are presented. The stability analysis, control design guidelines, and performance comparison with the state-of-the-art PLLs are other contributions of this paper.

II. TD-PLL

A. Small-Signal Modeling

For the sake of simplicity in the modeling procedure, let the TD-PLL input voltage, v_i, be clean and undistorted as

$$v_i(t) = v_\alpha(t) = V_i \cos(\theta_i) \tag{1}$$

where V_i is the input voltage amplitude and

$$\theta_i = \int \omega_i dt = \omega_{nf} t + \underbrace{\int \Delta\omega_i dt}_{\Delta\theta_i} \tag{2}$$

is the grid voltage phase, while $\omega_i = \omega_{nf} + \Delta\omega_i$, $\omega_{nf} = 2\pi/T$ and $\Delta\omega_i$ denote the grid frequency, the nominal value of grid frequency and the deviation of grid frequency from its nominal value, respectively. Assuming a constant value for the grid frequency, the β-axis voltage (i.e., the delay block output signal) can be expressed as

$$\begin{aligned} v_\beta(t) &= v_i\left(t - \frac{T}{4}\right) = V_i \cos\left(\theta_i - \frac{\omega_i T}{4}\right) \\ &= V_i \cos\left(\theta_i - \frac{\pi}{2} - \frac{\Delta\omega_i T}{4}\right) \\ &= V_i \sin\left(\theta_i - \frac{\Delta\omega_i T}{4}\right). \end{aligned} \tag{3}$$

Using Fig. 1, (1) and (3), the proportional-integral (PI) controller input signal, v_q, can be obtained as

$$\begin{aligned} v_q(t) &= -v_\alpha(t)\sin(\theta_o) + v_\beta(t)\cos(\theta_o) \\ &= \frac{V_i}{2}\sin(\theta_i - \theta_o) + \frac{V_i}{2}\sin\left(\theta_i - \frac{\Delta\omega_i T}{4} - \theta_o\right) \\ &\quad - V_i \underbrace{\left[\frac{1}{2}\sin(\theta_i + \theta_o) - \frac{1}{2}\sin\left(\theta_i - \frac{\Delta\omega_i T}{4} + \theta_o\right)\right]}_{D_2(t)} \end{aligned} \tag{4}$$

where $\theta_o = \omega_{nf} t + \Delta\theta_o$, as mentioned before, is the phase estimated by the PLL and $D_2(t)$ denotes a double frequency term. Notice that $D_2(t)$ is equal to zero when the grid frequency is at its nominal value, i.e., when $\Delta\omega_i = 0$.

Under a quasi-locked state, (4) can be approximated by

$$\begin{aligned} v_q(t) &\approx \frac{V_i}{2}(\theta_i - \theta_o) + \frac{V_i}{2}\left(\theta_i - \frac{\Delta\omega_i T}{4} - \theta_o\right) - V_i D_2(t) \\ &= \frac{V_i}{2}(\Delta\theta_i - \Delta\theta_o) + \frac{V_i}{2}\left(\Delta\theta_i - \frac{\Delta\omega_i T}{4} - \Delta\theta_o\right) \\ &\quad - V_i D_2(t). \end{aligned} \tag{5}$$

Taking the Laplace transform from both sides of (5) gives

$$v_q(s) \approx V_i\left[\left(\frac{1 + e^{-sT/4}}{2}\right)\Delta\Theta_i - \Delta\Theta_o - D_2(s)\right] \tag{6}$$

where $\Delta\Theta_i$ and $\Delta\Theta_o$ denote the Laplace transform of $\Delta\theta_i$ and $\Delta\theta_o$, respectively.

Using (6) and Fig. 1, the small-signal model of the TD-PLL can be obtained as shown in Fig. 3. As it can be seen, the dynamics of the delay based OSG in the TD-PLL is modeled by what is known as the *dq*-frame delayed signal cancellation (*dq*DSC) operator [19]-[21]. This operator is a finite impulse response (FIR) filter that is defined in general form as

$$dq\mathrm{DSC}_n(s) = \frac{1 + e^{-\frac{T}{n}s}}{2} \tag{7}$$

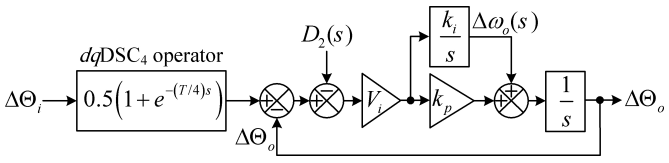

Fig. 3. Small-signal model of the TD-PLL.

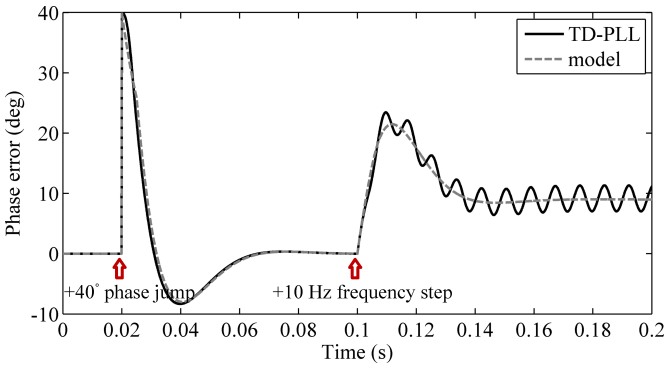

Fig. 4. Accuracy assessment of the TD-PLL small-signal model.

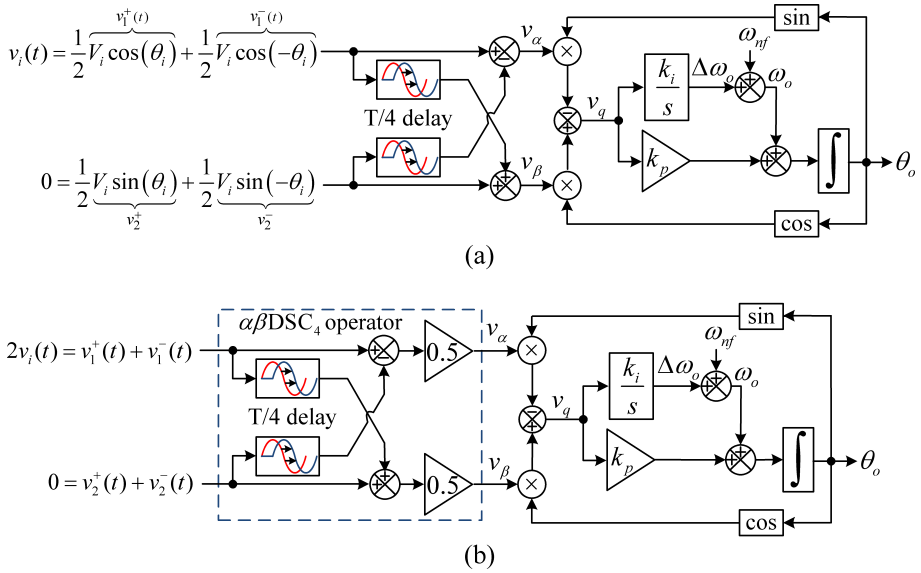

Fig. 5. Alternative mathematically equivalent representations of the TD-PLL.

where n is the operator delay factor.

To evaluate the model accuracy, any arbitrary values can be assigned to the proportional and integral gains k_p and k_i. Here, $k_p = 180$ and $k_i = 2500$ are selected. For the sake of simplicity, the double frequency disturbance input to the model is neglected. A phase-angle jump of $+40°$ and subsequently an exaggeratedly large frequency jump ($+10$ Hz) are programmed for the model accuracy assessment, whose results are shown in Fig. 4. It can be observed that the derived model accurately predicts the TD-PLL behavior.

The major drawbacks of the TD-PLL, i.e., its non-zero average phase error and its double frequency oscillatory error in the presence of frequency drifts, are also evident from Fig. 4. To remove these errors, as mentioned before, the frequency estimated by the TD-PLL can be fed back to the delay block to make it frequency adaptive. Such frequency feedback loop, however, makes the TD-PLL highly nonlinear. In this condition, it is rather difficult to evaluate and ensure the TD-PLL stability under all circumstances. Achieving a zero phase-error for the TD-PLL without using a frequency-feedback loop is discussed in the next sections.

B. Performance Enhancement Under Frequency-Varying Conditions

Let the single-phase input signal of the TD-PLL be as expressed in (1). Considering that a single-phase system is an unbalanced two-phase system, alternative mathematically equivalent representations of the TD-PLL can be obtained as shown in Fig. 5, in which v_1^+ and v_2^+ denote the positive-sequence components of the unbalanced two-phase system and v_1^- and v_2^- indicate its negative-sequence components. The system inside the dashed box is a well-known FIR filter called the $\alpha\beta$-frame DSC ($\alpha\beta$DSC) operator [22]. The s-domain transfer function of this operator in general form is as follows:

$$\alpha\beta\mathrm{DSC}_n(s) = \frac{1 + e^{\frac{j2\pi}{n}} e^{-\frac{T}{n}s}}{2} \tag{8}$$

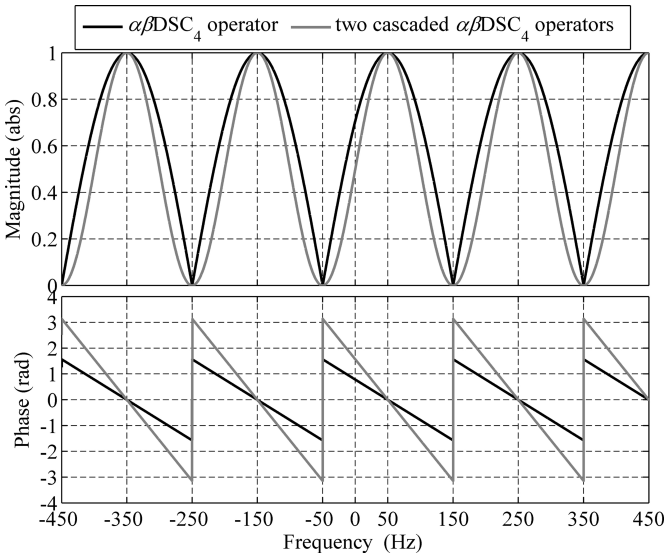

Fig. 6. Frequency response of the $\alpha\beta\mathrm{DSC}_4$ operator (dark line) and two cascaded $\alpha\beta\mathrm{DSC}_4$ operators (gray line).

where n, as defined before, is the delay factor. In our case, the delay factor n is equal to 4.

The dark line in Fig. 6 shows the frequency response of the $\alpha\beta\mathrm{DSC}_4$ operator. It can be observed that the $\alpha\beta\mathrm{DSC}_4$ operator has unity gain and zero phase shift at $+50$ Hz, and zero gain at -50 Hz. This means that the $\alpha\beta\mathrm{DSC}_4$ operator [the dashed box in Fig. 5(b)] passes the fundamental-frequency positive-sequence (FFPS) component and blocks the fundamental-frequency negative-sequence (FFNS) one when the grid frequency is at its nominal value, i.e., 50 Hz. In the presence of frequency drifts, nevertheless, this operator is unable to completely block the FFNS component. It also causes a phase shift in the FFPS component. That is the reason why the TD-PLL suffers from a double frequency oscillatory error and a non-zero average phase error under off-nominal

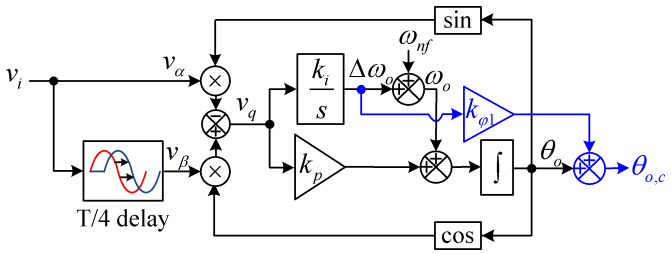

Fig. 7. TD-PLL with phase error compensator.

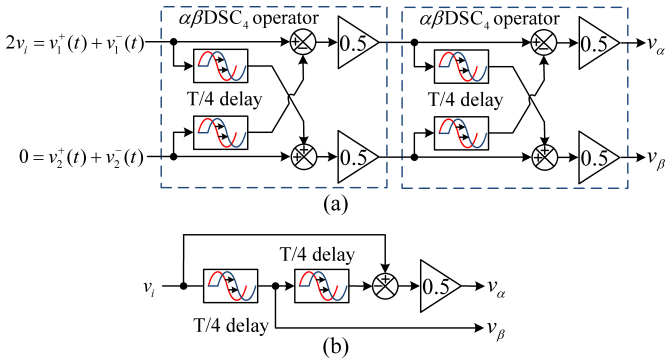

Fig. 8. (a) Two cascaded $\alpha\beta\text{DSC}_4$ operators and (b) its mathematically equivalent structure.

grid frequencies.

Using (8), the phase shift caused by the $\alpha\beta\text{DSC}_4$ operator at the fundamental frequency of positive sequence can be calculated as

$$\angle\alpha\beta\text{DSC}_4(j\omega_i) = -\left(\frac{\omega_i T}{8} - \frac{\pi}{4}\right). \tag{9}$$

Substituting $\omega_i = \omega_{nf} + \Delta\omega_i$ into (9) and performing some mathematical manipulations yields

$$\angle\alpha\beta\text{DSC}_4(j\omega_i) = -\underbrace{\left(\frac{T}{8}\right)}_{k_{\varphi 1}}\Delta\omega_i. \tag{10}$$

As (10) shows, the phase shift caused by the $\alpha\beta\text{DSC}_4$ operator depends on $\Delta\omega_i$. Therefore, correcting this phase shift requires an estimation of $\Delta\omega_i$. Fortunately, the integral action of the PI controller provides an estimation of $\Delta\omega_i$. Therefore, the TD-PLL non-zero average phase error can be easily corrected by multiplying the PI controller integral output (i.e., $\Delta\omega_o$) by $k_{\varphi 1} = T/8$ and adding the result to the TD-PLL output, as shown in Fig. 7. It should be mentioned here that correcting the phase shift caused by the PLL prefiltering stage at the PLL output has been first proposed in [23].

Adding this compensator, as it will be confirmed numerically later, enables the TD-PLL to achieve a zero average phase error in the presence of frequency drifts. However, it has no effect on its double frequency oscillatory error. This error, as mentioned before, is due to imperfect cancellation of the FFNS component by the $\alpha\beta\text{DSC}_4$ operator under off-nominal grid frequencies. An easy yet effective approach to deal with this problem is the repeated passes of the signal through the identical filter [24] as shown in Fig. 8(a), which

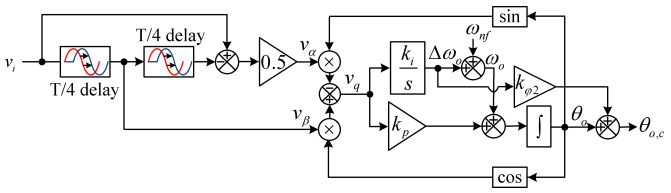

Fig. 9. TD-PLL with two-stage $\alpha\beta\text{DSC}_4$ operator and phase-error compensator.

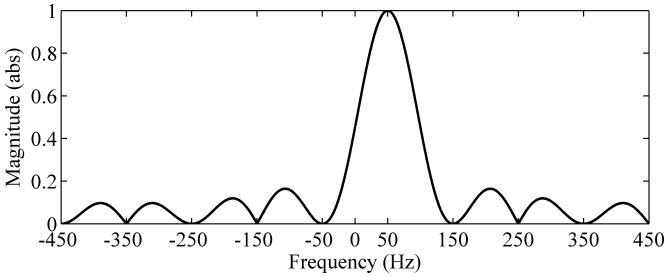

Fig. 10. Resultant magnitude frequency response of cascading $\alpha\beta\text{DSC}_8$ and $\alpha\beta\text{DSC}_{16}$ operators with two $\alpha\beta\text{DSC}_4$ operators.

is mathematically equivalent to the structure depicted in Fig. 8(b). The effectiveness of this approach can be better visualized by obtaining the frequency response of two cascaded $\alpha\beta\text{DSC}_4$ operators, which is shown by a gray line in Fig. 6. As it can be observed, two cascaded $\alpha\beta\text{DSC}_4$ operators provide a wider notch around -50 Hz compared to the single $\alpha\beta\text{DSC}_4$ operator and, therefore, can more effectively reject the FFNS component in the presence of frequency drifts.

The phase error caused by the cascaded $\alpha\beta\text{DSC}_4$ operators under off-nominal frequencies can be compensated for in the same manner as shown in Fig. 7; however, it should be noticed that the phase error compensator gain in this case is twice that of the previous case, i.e., $k_{\varphi_2} = 2k_{\varphi 1} = T/4$. Fig. 9 shows the schematic of TD-PLL with two-stage $\alpha\beta\text{DSC}_4$ operator and phase-error compensator.

It should be mentioned that a similar structure to the one in Fig. 9, but without the phase error compensator can be found in [25]. Such structure, consequently, is not able to track the grid phase-angle in the presence of frequency drifts and, therefore, it can only be used in applications where the grid frequency is fixed at (or very close to) its nominal value.

C. Performance Enhancement Under Harmonically-Distorted Condition

As shown in Fig. 6, the two cascaded $\alpha\beta\text{DSC}_4$ operators block the odd harmonics of order $h = 4k - 1$ ($k = \pm 1, \pm 2, \pm 3, \ldots$) and slightly attenuate the even harmonics, but leave other odd harmonics unchanged. This means that they have a limited harmonic filtering capability. Therefore, additional $\alpha\beta\text{DSC}$ operators with appropriate delay factors should be cascaded with them to improve their filtering capability. Selecting these additional operators should be made based on the grid harmonic pattern and application in hand. In this paper, the presence of even harmonics is neglected. In such scenario, cascading $\alpha\beta\text{DSC}_8$ and $\alpha\beta\text{DSC}_{16}$ operators with two $\alpha\beta\text{DSC}_4$ operators, which results in the magnitude

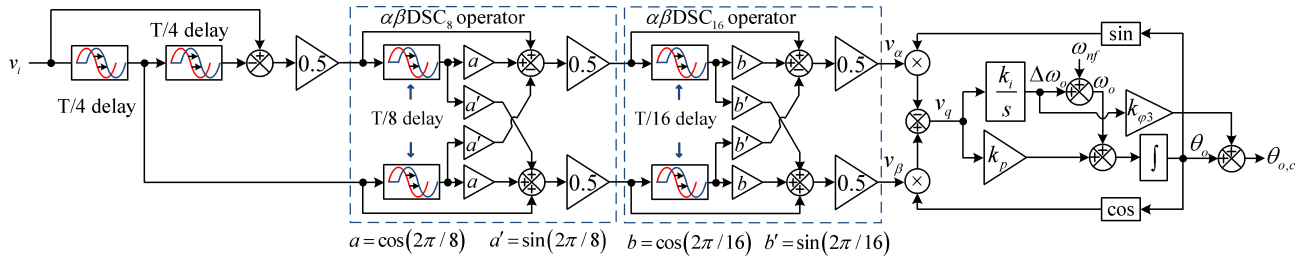

Fig. 11. ETD-PLL.

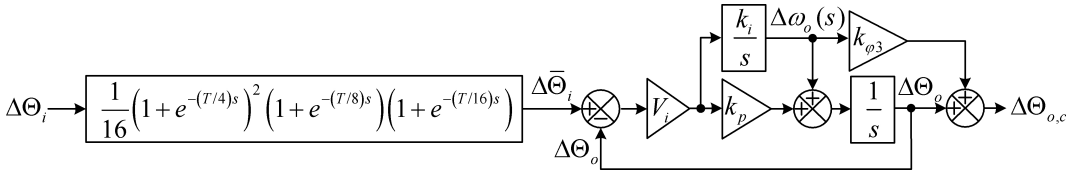

Fig. 12. Small-signal model of the ETD-PLL.

frequency response shown in Fig. 10, is good enough. For those applications where the even harmonics are not negligible, using $\alpha\beta\mathrm{DSC}_2$ operator may also be required. More detailed information about selecting $\alpha\beta\mathrm{DSC}$ operators for different grid scenarios can be found in [19], [20].

Including these additional operators into the TD-PLL results in the structure illustrated in Fig. 11. For the sake of brevity, this structure is called the enhanced TD-PLL (ETD-PLL). The phase error compensator gain in the ETD-PLL, as calculated in (11), is $k_{\varphi 3} = \frac{11T}{32}$:

$$\angle\left\{[\alpha\beta\mathrm{DSC}_4(j\omega_i)]^2\alpha\beta\mathrm{DSC}_8(j\omega_i)\ \ \alpha\beta\mathrm{DSC}_{16}(j\omega_i)\right\} = -\underbrace{\frac{11T}{32}}_{k_{\varphi 3}}\Delta\omega_i. \quad (11)$$

D. Stability Analysis and Parameter Design Guidelines

Fig. 12 shows the ETD-PLL small-signal model, which can be obtained by following the same procedure used for deriving the TD-PLL model. The presence of double frequency disturbance input to the model is neglected as the two-stage $\alpha\beta\mathrm{DSC}_4$ operator effectively suppresses it.

Using Fig. 12, the ETD-PLL open-loop[1] and closed-loop transfer functions can be obtained as

$$G_{ol}(s) = \frac{\Delta\Theta_{o,c}}{\Delta\bar{\Theta}_i - \Delta\Theta_{o,c}} = \frac{V_i\left[(k_p + k_i k_{\varphi 3})\,s + k_i\right]}{s\left(s - V_i k_i k_{\varphi 3}\right)} \quad (12)$$

$$G_{cl}(s) = \frac{\Delta\Theta_{o,c}}{\Delta\Theta_i} = \frac{1}{16}\left(1+e^{-(T/4)s}\right)^2\left(1+e^{-(T/8)s}\right)\left(1+e^{-(T/16)s}\right)\frac{V_i\left[(k_p + k_i k_{\varphi 3})\,s + k_i\right]}{s^2 + V_i k_p s + V_i k_i}. \quad (13)$$

As (12) shows, the ETD-PLL has an unstable open-loop pole, which is created by the phase error compensator. This unstable pole makes the gain margin (GM) negative (in dB) and adversely affects the phase margin (PM). Having a negative GM, however, does not mean that the ETD-PLL is unstable. Indeed, as the characteristic polynomial of (13) shows, the ETD-PLL is stable for positive values of k_p and k_i. The characteristic polynomial also indicates that the grid voltage amplitude variations affect the ETD-PLL dynamics. To avoid this, signals v_α and v_β can be divided by an estimation of V_i, which can be calculated as $\hat{V}_i = \sqrt{v_\alpha^2 + v_\beta^2}$.

The proportional and integral gains k_p and k_i can be determined by defining $k_p = 2\zeta\omega_n$ and $k_i = \omega_n^2$, where ζ is the damping factor and ω_n is the natural frequency, and selecting appropriate values for ζ and ω_n. Recommended values for the damping factor are $\zeta = 0.707$ and $\zeta = 1$ [26]. The latter is a more suitable choice for the ETD-PLL. The reason is that a higher value for ζ compensates more effectively the negative effects of the phase-error compensator. Selecting the natural frequency ω_n, on the other hand, involves a trade-off between the speed of response and the stability: Increasing ω_n raises the PLL bandwidth and, therefore, makes its dynamic response fast, but degrades its stability margin as shown in Fig. 13. Here, $\omega_n = 2\pi 35$ rad/s is selected, which corresponds to a PM around $60°$, a GM about -7 dB, and a 2% settling time equal to around two cycles of the nominal frequency in response to phase-angle jumps and frequency steps. The selected values for ζ and ω_n result in $k_p = 440$ and $k_i = 48361$.

III. NTD-PLL

A. Small-Signal Modeling of NTD-PLL

The small-signal model of the NTD-PLL is derived under the same assumptions as those described in Section II-A.

Using Fig. 2, (1) and (3), the input signal of the NTD-PLL

[1]To derive the open-loop transfer function, the small-signal model should be rearranged to its classic feedback form.

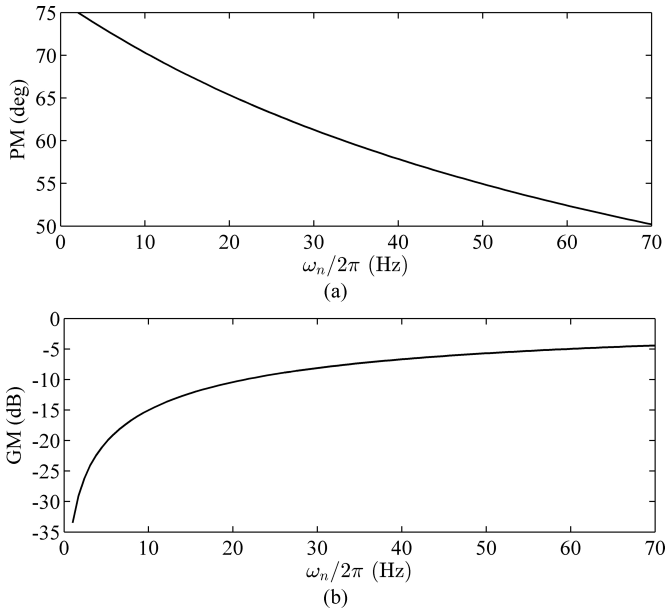

Fig. 13. (a) PM and (b) GM of the ETD-PLL as a function of ω_n.

PI controller can be obtained as

$$\begin{aligned} v_q(t) &= -v_\alpha(t)\sin(\theta_o) - v_\beta(t)\sin\left(\theta_o - \frac{\omega_o T}{4}\right) \\ &= \frac{V_i}{2}\sin(\theta_i - \theta_o) + \frac{V_i}{2}\sin\left(\left(\theta_i - \frac{\omega_i T}{4}\right) - \left(\theta_o - \frac{\omega_o T}{4}\right)\right) \\ &\quad - \frac{V_i}{2}\underbrace{\sin(\theta_i + \theta_o)}_{D_2'(t)} - \frac{V_i}{2}\underbrace{\sin\left(\theta_i - \frac{\omega_i T}{4} + \theta_o - \frac{\omega_o T}{4}\right)}_{D_2'(t-T/4)} \end{aligned} \quad (14)$$

where $D_2'(t)$ denotes a double frequency term.

Under a quasi-locked state, (14) can be approximated by

$$\begin{aligned} v_q(t) &\approx \frac{V_i}{2}\left[(\theta_i - \theta_o) + \left(\theta_i - \frac{\omega_i T}{4}\right)\right. \\ &\quad \left. - \left(\theta_o - \frac{\omega_o T}{4}\right) - D_2'(t) - D_2'(t - T/4)\right] \\ &= \frac{V_i}{2}\left[(\Delta\theta_i - \Delta\theta_o) + \left(\Delta\theta_i - \frac{\Delta\omega_i T}{4}\right)\right. \\ &\quad \left. - \left(\Delta\theta_o - \frac{\Delta\omega_o T}{4}\right) - D_2'(t) - D_2'(t - T/4)\right]. \end{aligned} \quad (15)$$

Taking the Laplace Transform from (15) yields

$$v_q(s) \approx V_i \frac{1 + e^{-sT/4}}{2}\left[\Delta\Theta_i - \Delta\Theta_o - D_2'(s)\right]. \quad (16)$$

Using (16) and Fig. 2, the small-signal model of the NTD-PLL can be obtained as shown in Fig. 14.

Fig. 15 checks out the small-signal model accuracy in the prediction of the NTD-PLL dynamic behavior. As shown, the model is very accurate.

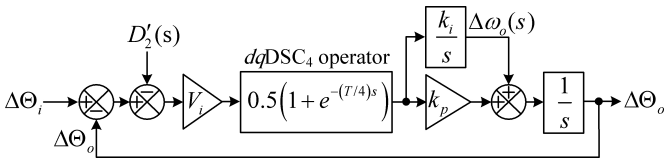

Fig. 14. Small-signal model of the NTD-PLL.

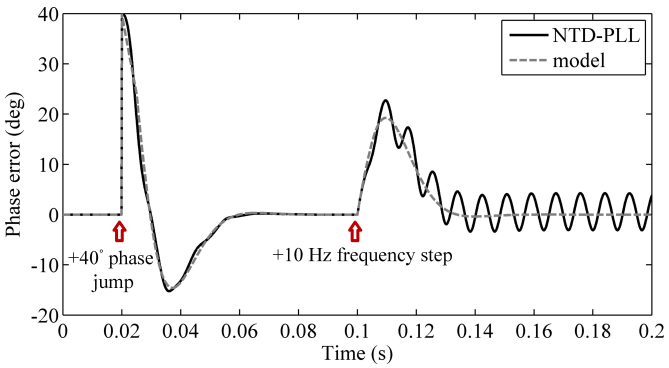

Fig. 15. Accuracy assessment of the NTD-PLL small-signal model.

B. Stability Analysis and Parameter Design Guidelines

Using the NTD-PLL small-signal model, the open-loop transfer function can be obtained as

$$G_{ol}(s) = \left.\frac{\Delta\Theta_o}{\Delta\Theta_i - \Delta\Theta_o}\right|_{D_2'(s)=0} = V_i \frac{1 + e^{-(T/4)s}}{2}\frac{k_p s + k_i}{s^2}. \quad (17)$$

The delay term in the open-loop transfer function (17) complicates the stability analysis and the parameter tuning procedure. For this purpose, the delay term in (17) is replaced by its first-order Padé approximation, i.e., $e^{-(T/4)s} \approx \frac{1-(T/8)s}{1+(T/8)s}$, which results in

$$G_{ol}(s) \approx V_i \frac{1}{\underbrace{(T/8)}_{T_d}s + 1}\frac{k_p s + k_i}{s^2}. \quad (18)$$

Using the symmetrical optimum method [6], the integral and proportional gains k_i and k_p can be selected as

$$\begin{aligned} k_i &= 1/\left(V_i g^3 T_d^2\right) \\ k_p &= 1/\left(V_i g T_d\right) \end{aligned} \quad (19)$$

where g is a design constant which determines the PM of the PLL as $\mathrm{PM} = \tan^{-1}\left(\frac{g^2-1}{2g}\right)$.

The recommended range of PM for stability of control systems is $30^\circ \le \mathrm{PM} \le 60^\circ$. It is shown in [6] that $\mathrm{PM} = 45^\circ$ is the optimum choice, as this value minimizes the 2% settling time in response to phase-angle jumps. Therefore, $\mathrm{PM} = 45^\circ$ is selected, which corresponds to $g = 1 + \sqrt{2}$.

Once the design constant g is selected, k_p and k_i can be calculated from (19) as $k_i = 11371$ and $k_p = 166$. Fig. 16 shows the open-loop Bode plot of the NTD-PLL using the selected values of k_p and k_i. It can be seen that the PM of PLL is very close to the intended value, i.e., 45°, which confirms the accuracy of the suggested design procedure.

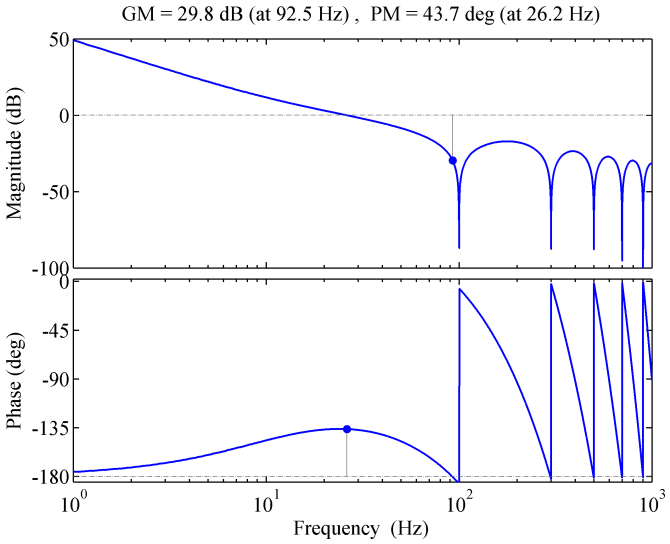

Fig. 16. Open-loop Bode plot of NTD-PLL.

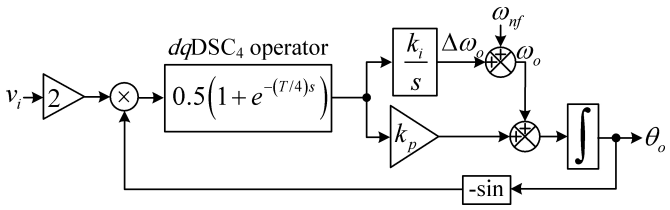

Fig. 17. pPLL with in-loop $dq\mathrm{DSC}_4$ operator.

C. A More Straightforward Implementation of NTD-PLL

The small-signal model of the NTD-PLL (Fig. 14) seems to be the same as the small-signal model of a power-based PLL (pPLL)[2] with an in-loop $dq\mathrm{DSC}_4$ operator. Fig. 17 shows the schematic of this pPLL. Therefore, it is reasonable to say that the NTD-PLL and the pPLL with in-loop $dq\mathrm{DSC}_4$ operator (briefly called the $dq\mathrm{DSC}_4$-pPLL) are mathematically equivalent. To support this fact, a performance comparison between the NTD-PLL and the $dq\mathrm{DSC}_4$-pPLL under the same condition as in Fig. 15 is carried out. Fig. 18 shows the obtained results. It can be observed that the NTD-PLL and the $dq\mathrm{DSC}_4$-pPLL have identical responses, which proves their equivalence. This equivalence implies that it is more straightforward and even computationally beneficial to use the $dq\mathrm{DSC}_4$-pPLL structure when the implementation of the NTD-PLL is intended.

D. Performance Enhancement Under Frequency Varying and Harmonically Distorted Conditions

As Fig. 18 shows, the NTD-PLL and, therefore, its mathematically equivalent structure, i.e., the $dq\mathrm{DSC}_4$-pPLL, achieve a zero average phase error in the presence of a frequency drift, but they suffer from a double frequency oscillatory error in this condition. This problem, as recommended in [10], can be alleviated by including an additional $dq\mathrm{DSC}_4$ operator into the $dq\mathrm{DSC}_4$-pPLL control loop. The harmonic

[2]The pPLL is a standard single-phase PLL [5], [6], [15].

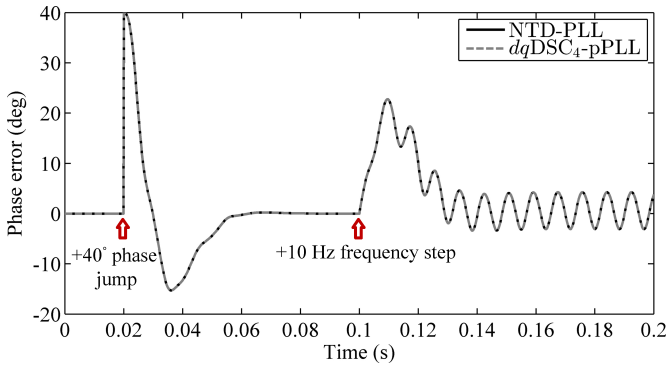

Fig. 18. A performance comparison between the NTD-PLL and the $dq\mathrm{DSC}_4$-pPLL.

filtering capability of this PLL is also rather low, and it can be improved by incorporating a $dq\mathrm{DSC}_8$ operator and a $dq\mathrm{DSC}_{16}$ operator into its control loop. Using these additional operators, however, causes a considerable phase delay in the PLL control loop, which significantly slows down its dynamic response. Therefore, this approach is only useful for specific applications where a slow and damped dynamic response for the PLL is needed. An example of such applications is described in [27]. Considering the limited application of such PLLs, this issue will not be further discussed here.

IV. Simulation and Experimental Results

In this section, the dynamic behavior and filtering capability of the ETD-PLL (Fig. 11) and NTD-PLL (Fig. 2) is evaluated through simulation and experimental results. Simulations are carried out in Matlab/Simulink environment and experimental results are obtained using a dSPACE MABXII DS1401 platform. Throughout the simulation and experimental studies, the sampling frequency and nominal grid frequency are considered to be 8 kHz and 50 Hz, respectively.

Fig. 19 shows the simulation and experimental results for the ETD-PLL and NTD-PLL in response to a $+40°$ phase-angle jump. It can be observed that both PLLs have comparable dynamic behaviors. The 2% settling time for both PLLs is around two cycles of the nominal frequency.

Fig. 20 illsutrates the ETD-PLL and NTD-PLL performance when the grid voltage frequency undergoes a step change of -3 Hz. Contrary to the NTD-PLL, which suffers from double frequency oscillatory errors, the ETD-PLL provides an accurate estimation of phase and frequency in this condition. To have a better view, Fig. 21 illustrates the magnitude of double frequency oscillatory errors in the phase and frequency estimated by the ETD-PLL and NTD-PLL as a function of the grid frequency. According to the EN50160 standard [28], the grid frequency variations are considered to be in the range of 47 to 52 Hz. These results highlight the high ability of ETD-PLL to reject double frequency errors in the presence of large frequency drifts. They also show that the NTD-PLL may not be a suitable choice for applications where the grid frequency deviation from its nominal value is high.

Fig. 22 evaluates the harmonic filtering capability of the ETD-PLL and NTD-PLL in the presence of 4% third har-

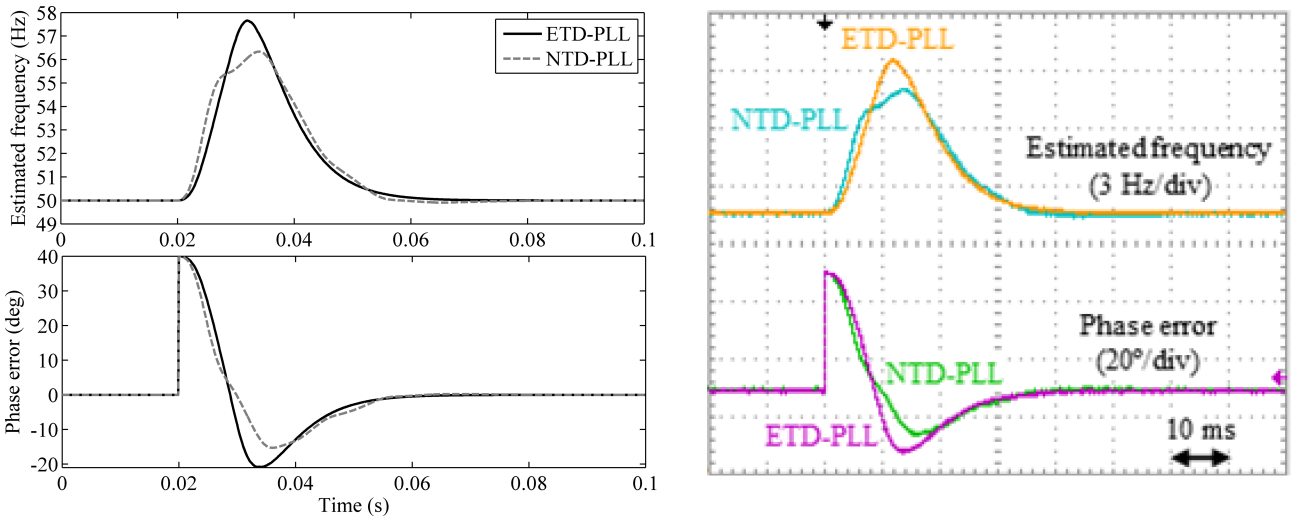

Fig. 19. Simulation and experimental results for the ETD-PLL and NTD-PLL in response to a $+40°$ phase-angle jump.

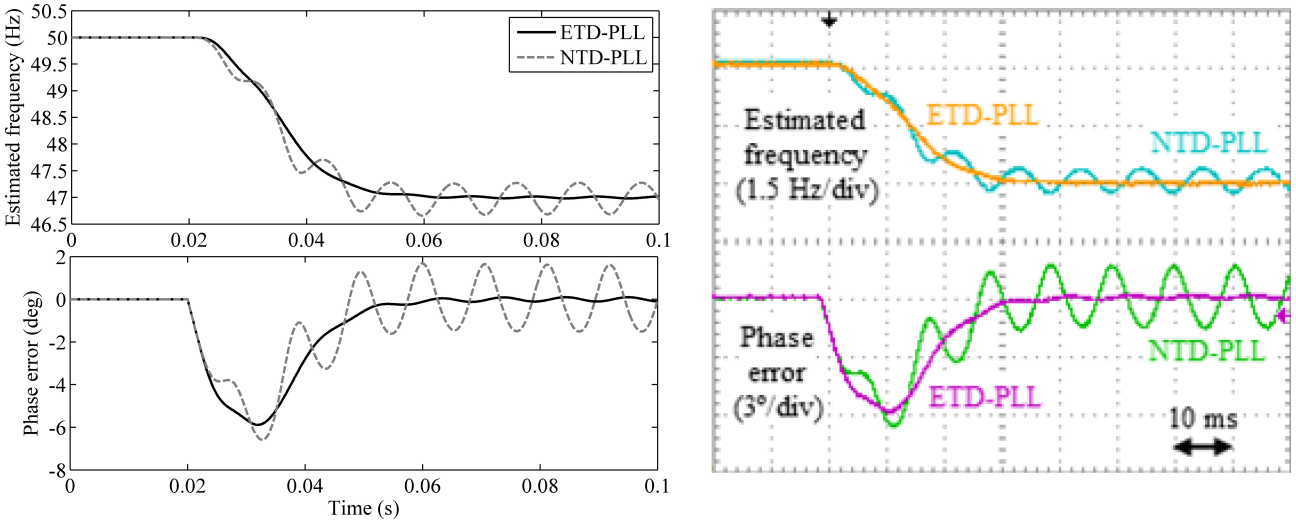

Fig. 20. Simulation and experimental results for the ETD-PLL and NTD-PLL in response to a -3 Hz frequency step change.

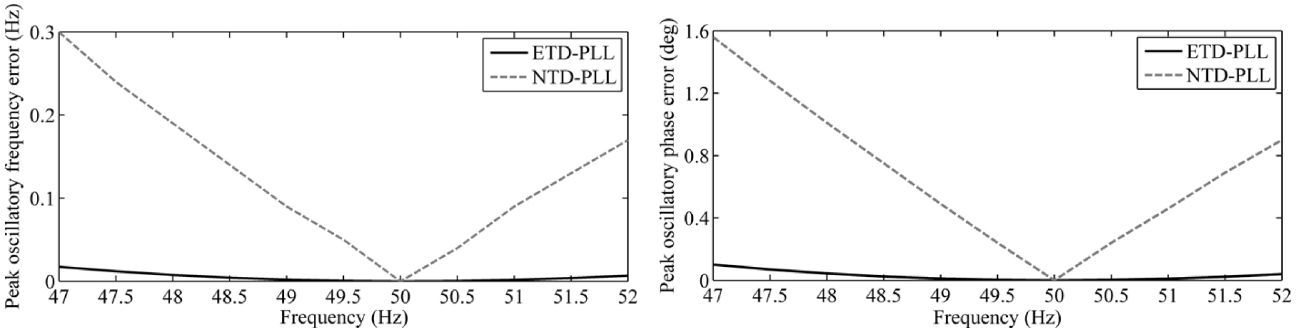

Fig. 21. Magnitude of double frequency oscillatory errors in the estimated frequency and phase of the ETD-PLL and NTD-PLL in the frequency range defined by the standard EN50160.

monic component, 5% fifth harmonic component, 4% seventh harmonic component, 1% ninth harmonic component and 3% eleventh harmonic component in the grid voltage. The total harmonic distortion of the grid voltage is 8.18 %. As shown, the filtering capability of the ETD-PLL is quite good even in the presence of large frequency drifts. The filtering capability of the NTD-PLL, however, is acceptable only when the grid frequency is at (or very close to) its nominal value.

To highlight the advantages and disadvantages of the ETD-PLL and NTD-PLL, two advanced single-phase PLLs, i.e., the

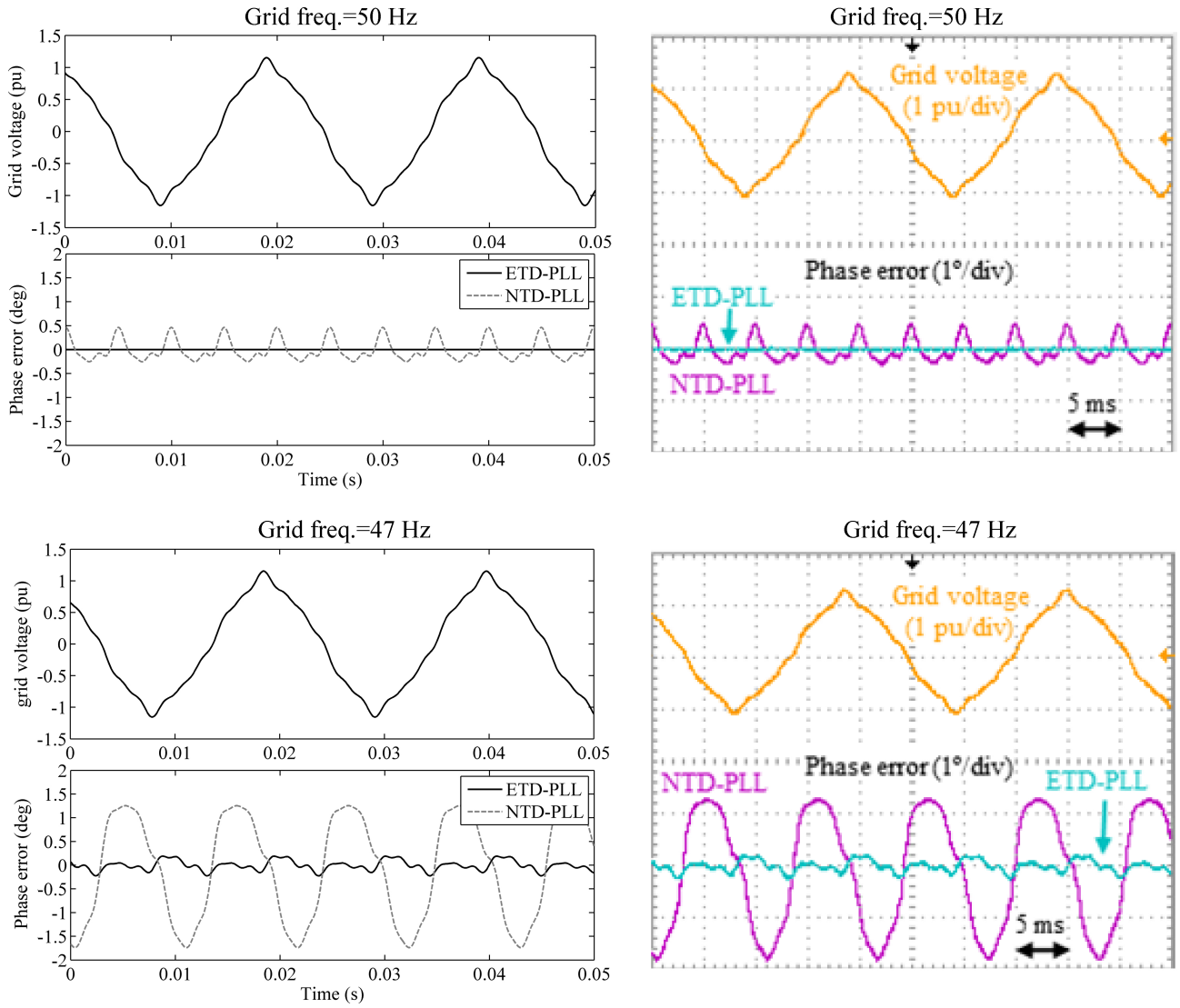

Fig. 22. Simulation and experimental results under harmonically distorted grid conditions.

second-order generalized integrator based PLL (SOGI-PLL) [14] and pPLL with in-loop moving average filter (briefly called the MAF-pPLL) [29], are also evaluated under the same tests as the ones in Figs. 19, 20 and 22 and their results are compared with those of the ETD-PLL and NTD-PLL. The control parameters of the SOGI-PLL and MAF-pPLL are designed using the symmetrical optimum method, as described in [15] and [29], respectively. Table I summarizes the obtained results, in which the best performance is highlighted in bold font.

V. Summary and Conclusion

For the first time, the accurate small-signal model of the TD-PLL was derived in this paper. It was shown that the dynamics of the transfer delay unit, contrary to what was believed, is not negligible. Indeed, its dynamics appear as a set-point filter in the TD-PLL small-signal model. Regardless of the importance of such model in the analysis and design of the TD-PLL, it may stimulate new ideas in the modeling of other single-phase OSG based PLLs, because neglecting the dynamics of OSG unit during the modeling of these PLLs is a common practice.

It was then shown that the drawbacks of the standard TD-PLL, i.e., its poor harmonic filtering capability and its phase offset and oscillatory errors in the presence of frequency drifts, can be overcome by adding additional delay based filtering stages and a phase error compensator into its structure. These modifications only require $10\ \times/\div$, $10\ +/-$ and storing $\frac{5T}{8T_s}$ samples (100 samples, for a sampling frequency 8 kHz) in the DSP memory, which means they demand a very low computational effort.

The NTD-PLL small-signal modeling was then presented, which indicated that the NTD-PLL is mathematically equivalent to a pPLL with in-loop $dq\mathrm{DSC}_4$ operator ($dq\mathrm{DSC}_4$-pPLL). Considering this equivalence and more straightforward implementation of the $dq\mathrm{DSC}_4$-pPLL, it is recommended in this paper to use the $dq\mathrm{DSC}_4$-pPLL when the implementation of the NTD-PLL is intended. A systematic method based on the symmetrical optimum method to fine-tune the NTD-PLL control parameters was also proposed.

TABLE I
PERFORMANCE COMPARISON

	ETD-PLL	NTD-PLL	SOGI-PLL	MAF-pPLL
$+40°$ phase-angle jump				
2% settling time	37.1 ms (1.85 cycles)	**35.6 ms (1.78 cycles)**	48.7 ms (2.43 cycles)	75.9 ms (3.8 cycles)
Phase overshoot	20.8° (52%)	15.28° (38.2%)	**12.28° (30.7%)**	13.43° (33.6%)
Peak frequency deviation	7.66 Hz	6.34 Hz	6.03 Hz	**3.22 Hz**
-3 Hz frequency step change				
2% settling time	**36.4 ms (1.82 cycles)**	—	37.6 ms (1.88 cycles)	96.4 ms (4.82 cycles)
Peak phase deviation	**5.88°**	6.58°	6.34°	11.64°
Peak oscillatory frequency error	0.017 Hz	0.3 Hz	**0 Hz**	0.049 Hz
Peak oscillatory phase error	0.1°	1.56°	**0°**	0.51°
Harmonically distorted grid condition				
Peak-to-peak phase error (freq.=50 Hz)	**0°**	0.72°	0.51°	**0°**
Peak-to-peak phase error (freq.=47 Hz)	**0.41°**	3°	0.54°	1°
Phase margin (PM)	**59.5°**	43.7°	44.7°	43.6°
Gain margin (GM)	−7.32 dB	29.8 dB	**Inf.**	14.1 dB

The paper finally evaluated the performance of the ETD-PLL and NTD-PLL through simulation and experimental results and compared their performance with the state-of-the-art single-phase PLLs. It was shown that the ETD-PLL has a fast dynamic response (a settling time of less than two cycles of the nominal frequency) and a good harmonic filtering capability. These features along with its ease of implementation make the ETD-PLL a suitable choice for the synchronization of single-phase grid-connected equipment. The NTD-PLL, like the ETD-PLL, has a fast dynamic response, but it suffers from a limited harmonic filtering capability and considerable double frequency oscillatory error in the presence of frequency drifts. Therefore, it can be a suitable choice only for applications where the grid frequency is at or very close to its nominal value.

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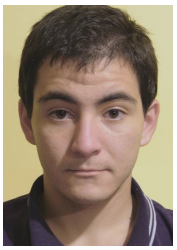

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