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On-state voltage drop based power limit detection of IGBT inverters

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Keywords

<<Power density>>, <<power converter>>, <<junction temperature>>, <<IGBT>>, <<gate drivers>>, << online monitoring >>, << power limit detection >>.

Abstract

Power density is a key performance factor in order to reduce the cost and size of a power converter. Because of the unknown junction temperature, today's design margins are relatively high to ensure safe and a reliable operation. In this paper, the on-state voltage drop is measured online for all insulated gate bipolar transistors (IGBTs) in the inverter, using advanced gate driver. The die temperature is estimated and monitored on each device during power converter operation. Based on the monitored temperature in real time, the maximum power capability is detected. The output power is increased until a safe operating temperature of power modules. This enable a power density is increased by 11.16 $kW/litre$ to 19.13 $kW/litre$ in a low voltage power stack which is typically used in wind power converters. Experiment results are shown for safe operation of converter at around 1.2 MW, which is built in a standard size for the 600 - 700 kW. Furthermore, the 1700 V, 1000 A power module is replaced with a 1400 A module to increase the load current.

Introduction

The improvement in efficiency, power density, reliability, and cost of power converters is a continuous research effort in academia and industry. The power converter design must take into account all performance factors, because the efficiency, power density and reliability are always very well-linked. Cost is a design limitation, where the tendency is always to increase the rated power for the same price or decrease the price for the same rated power. Cost is in line with the power density, and usually works against the efficiency and reliability [1]. Depending on the application requirements, some factor may have higher priority than the others.

Advancement in reliability of power devices with their packaging can allow the increase of power density, making it possible to cycle the devices at higher junction temperature variation. In the best case scenario, the reliability will allow the operation of power devices up to their maximum junction temperature [2].

The accurate detection or estimation of the junction temperature is required to detect the power limit. In a converter prototype, it is impossible to directly measure the temperature while the converter is operating. Therefore, the only way is to estimate as accurately as possible [3]. Several static and dynamic

characteristics of semiconductor devices are proposed to estimate the junction temperature, but still there are many constraints to apply them in a field condition. Recently proposed methods are inclined to be applicable in real operation.

State of the art junction temperature estimation methods are based on datasheet or measured energy loss data. However, in most cases the thermal model is not accurate enough to estimate the actual temperature of the power devices, instead it gives a rough indication on the efficiency and operating temperature. Moreover, with the ageing of the power electronic devices, the electrical and thermal characteristics are changing [4], [5]. Because of thermo-mechanical induced stress in interconnection and bondings, the on-state voltage is increased gradually with the number of loading cycles [6]. The progressive degradation in interconnection is occurred throughout the life where the device remains functional until a catastrophic failure is occurred [7].

The power output of a converter shall be increased upto useable power, which typically used to generate power with a reasonable size of cooling. Generally, derating technique is used in components to ensure the components operating within a safe limit. Furthermore, the proper derating improves reliability as well as elongates device functional life. In high power converters, temperature as a key stressor can be used to derate or uprate based on operating status of a converter. An accurate measurement technique of stress parameters play vital role in order to make smart decision on derating/uprating of a converter. Applying this to a full power converter requires a comprehensive monitoring of all critical parameters including voltages, currents, temperatures, and other environmental stress factors.

This paper introduces a test setup for characterizing the conversion power limits of IGBT inverters. An estimation method based on measurement of on-state voltage while the converter is operating was used. The test reveals that with regard to power density, a LV power stack can almost double its operating power in the same construction. This paper does not include a long term reliability aspects in operating at design margin, which is under investigation and presents later.

Derating/Uprating in a Converter Operation

Smart de-rating is used to continue converter operation in harsh conditions without sacrificing lifetime to improve reliability. Fig. 1 shows the response from current/power de-rating control to a deteriorating cooling system performance for increasing cooling temperature [8]. The output power is smoothly reduced for the rise in cooling temperature. In active components inside a power module, the temperature is generated by electrical load, cooling and thermal resistance between the components and the cooling. In order to enhance reliability, the temperature in such components should be under the rated value. Based on this temperature, the power can be uprated/derated for a safe operation. Standard thermal and electrical design guidelines are available depending upon the critical or normal reliability application. However, other factors such as cost, volume, component selection, passive components, and the application are affected the operating parameters. Manufacturer provides derating guide lines for each devices based on the sensitivity of the application [9].

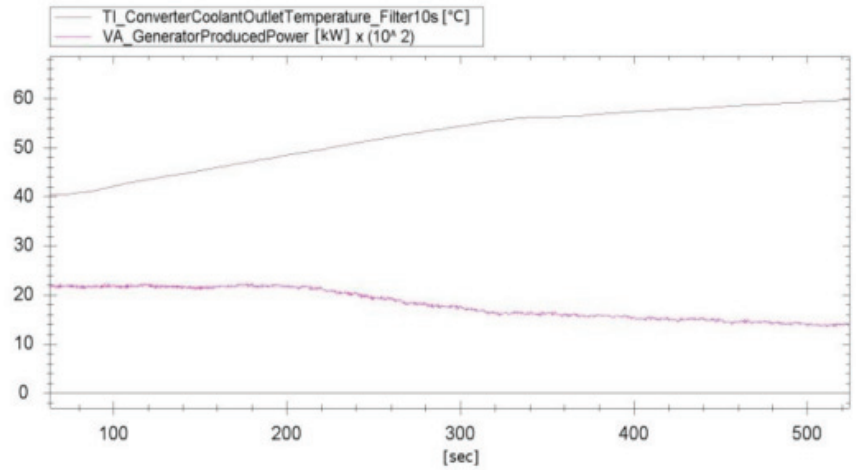


Figure 1: Converter power de-rating control response to an increasing coolant temperature, from [8].

Temperature and a Power Limit Detection

Temperature is one of a key parameter considered in design of power converters. Generally, manufacturer provides maximum operating virtual junction temperature for semiconductor devices. State of the art power modules used in wind power applications are safe to operate until 150°C. This however, doesn't represent for any specific components inside a multi-chip power module. The stress in a IGBT or a corresponding free-wheeling diode may change based on an operating load point or an application. An optimum thermal design is a daunting task to operate the device within a safe limit as well as to maintain a maximum power capability of a converter. Hence monitoring of operating temperature is the paramount importance to ensure a good thermal design as well as to operate a power converter safe and reliable.

Junction temperature simply can not be determined by a power dissipation or a power density in power modules. The temperature distribution is significantly affected by other parameters such as interconnections, device layers, thermal interface etc. in both temporal and spatial. Because of a spatial distribution and power module packaging constraints, a direct measurement of temperature is not practical [10]. Hence, several methods are proposed using dynamic and static characteristics of power modules [11]. However, until today, few methods are discussing to make them applicable directly into a converter operation without any modification in a converter structure and control [12], [3]. This paper presented

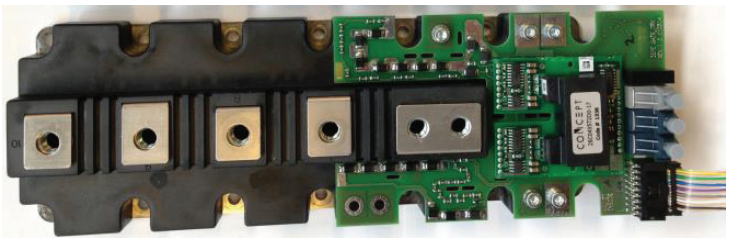


Figure 2: Gate drive with on-state voltage measurement feedback.

$V_{ce,on}$-load current method [3]. For this purpose a high accuracy on-state voltage measurement method is used [13]. Fig. 2 shows a commercial prototype of a gate driver featured with on-state voltage measurement feedback.

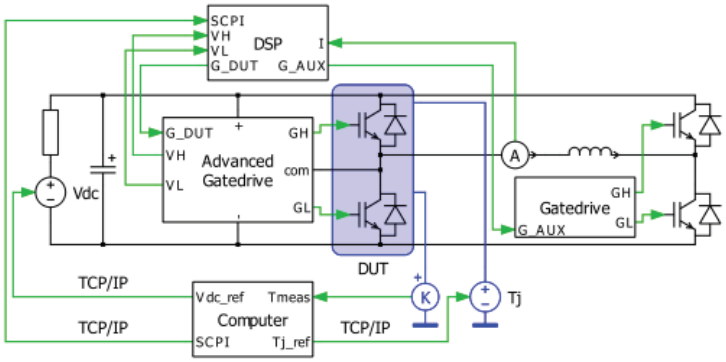


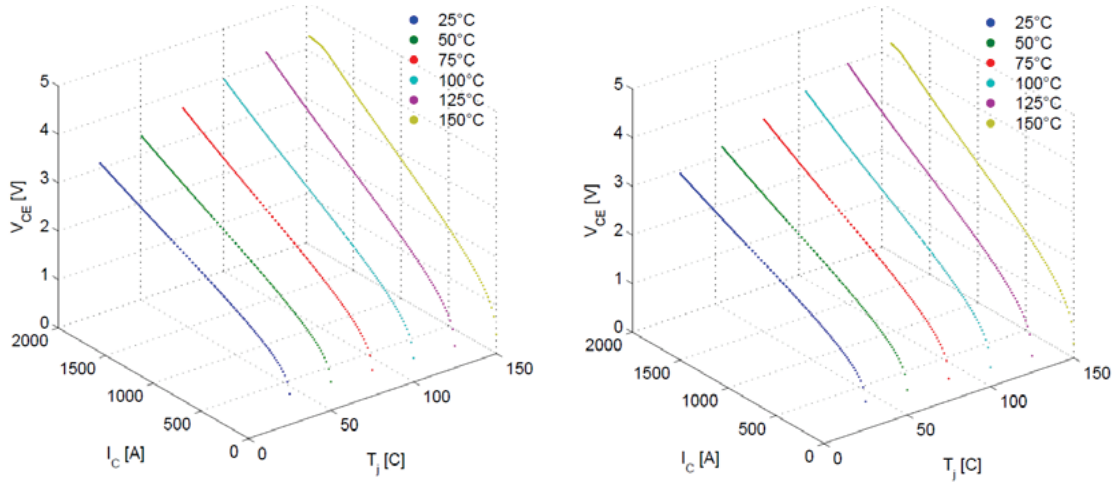
Figure 3: IGBT-gate drive calibration test setup.

Fig. 3 demonstrates schematic of gate drive calibration test setup in order to detect a die temperature in power modules. The method requires a two major steps; first a calibration of $V_{ce,on}$ - T obtain temperature dependency at different current levels. Second, an accurate measurement of $V_{ce,on}$ while in loading.

A 1700 V and 1400 A half bridge power module Infineon FF1400R17IP4 is used, where six half bridge sections are used to share a total load current.

Calibration

A temperature calibration setup was built to characterize the on-state voltage of all power devices in a power module. The schematic block is shown in Fig 3. The device under test (DUT) is the power module from one phase of the inverter, mounted on a temperature controlled heating plate. A gate driver was designed and built as such that the on-state voltage measurement circuitry introduced in [13] is integrated, and measurements are sent using fiber optics to a digital signal processor (DSP). The on-state voltage measurement resolution is 0.61 mV and the precision around ± 3 mV. An inductor and an auxiliary



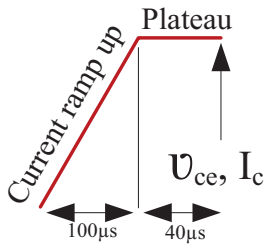
(a) IV characteritics for high side IGBT.

(b) IV characteristics for LS IGBT.

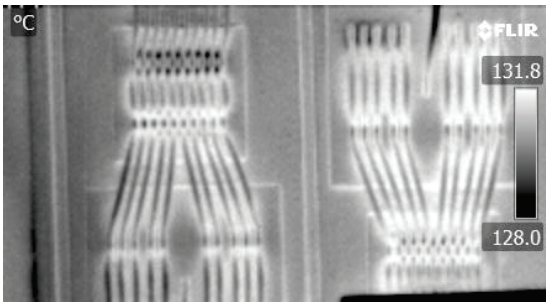
Figure 4: Calibration data for one phase power module (a) high side IGBT and (b) low side IGBT.

converter legs are used to force a desired current through all the devices of the DUT module. The current is measured with a LEM IT 1000-S/SP1 Ultrasab current sensor. The calibration is conducted in 10 A and 25 $^{\circ}C$ temperature steps for the on-state gate-emitter voltage of 15 V. The characteristics for high side and low side as transistors are shown in Fig 4. Based on the measured calibration data, polynomial curve fitting was done for all the transistors.

The calibration is conducted in a very short period of time in less than 140 μs in order to limit the die temperature rise. The die temperature is monitored using IR - thermography in an open module in a converter operation. Also a transient thermal characterization is investigated as a function of conduction time at different temperatures and also seen that the rise in the die temperature is less than 0.5$^{\circ}C$until 200 μs [14].



(a) A calibrated current profile.



(b) A thermal image at 125$^{\circ}C$.

Figure 5: A calibrating current and thermal image during $V_{ce,on}$ - T calibration in a 1700 V and 1000 A power module.

Temperature Estimation

Temperature estimation method includes an accurate measurement of on-state voltage drop in a converter operation. A first calibration is conducted at initial phase with a very good accuracy. Based on the $\upsilon_{ce,on}$ at the actual current for 20$^{\circ}C$ and 150$^{\circ}C$, a polynomial fitting is used to obtain the voltage profile for corresponding load current. During converter operation, an actual measurement is compared with calibrated data and a linear interpolation is used at each current level. The temperature dependency factors for different load currents are unique. The linear interpolation is used to detect die temperature from calibration and measurement data is given Eq. 1.

$$T_{j,estim} = 25 + \left(\frac{V_{ce,meas} - V_{CE,25}}{V_{ce,150} - V_{CE,25}}.125\right) \tag{1}$$

A correction parameter $\Delta\upsilon_{err}$ is necessary to obtain a temperature close to a die temperature. This parameter compensates the on-state voltage drop from homogeneous temperature profile during calibration to non-homogeneous profile in operation [15]. The parameter shall be obtained at each temperature using temperature gradients from chip to cooling and using temperature coefficient of internal resistance obtained from a Shockley with a resistor model as explained in [15]. Because of lateral temperature profile, the voltage drop in series interconnects is deviated than in the calibration process.

$$T_{j,estim} = 25 + (\frac{V_{ce,meas} - V_{CE,25,new}}{V_{ce,150} - V_{CE,25,new}}.125 + \Delta\upsilon_{err}) \tag{2}$$

Without the correction parameter, the Eq. 1 underestimates the temperature, hence measurement shown in this paper are lower than the actual temperature. Furthermore, in a long operation a re-calibration of DUT is required to compensate the rise in $V_{CE,25,new}$ due to electro-mechanical induced ageing in interconnects. The $V_{ce,meas}$ is increasing for above cross-over current because of positive temperature coefficient (PTC) behaviour. Hence, recalibrating transistor after certain number of cycles and using newer $V_{CE,25,new}$ as shown in Eq. (2) cancels the rise in voltage from ageing in interconnects such as bond wire, chip metallization and *cu* terminals.

The temperature estimation based on $\upsilon_{ce,on}$ gives close to the average in space of die temperature [14]. There are six sections in parallel operating at the same time. One IGBT die has 12 heavy *Al* wires sharing the total current. Because of wire length and bonding positions, the current distribution between the wires are uneven. Hence, the temperature distribution from center to edge also uneven. To illustrate more, Fig. 6 shows the maximum, minimum and average temporal distribution in a single cycle for a $1000\,A$ module in a converter operation.

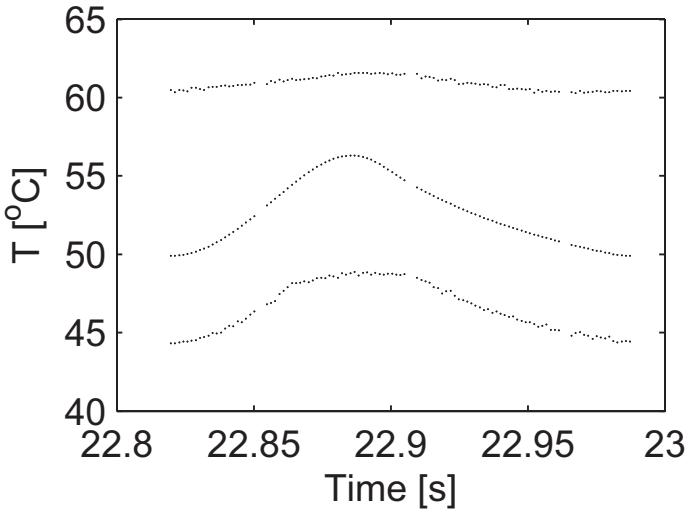


Figure 6: Tempertaure in a single cycle at $900A_{peak}$.

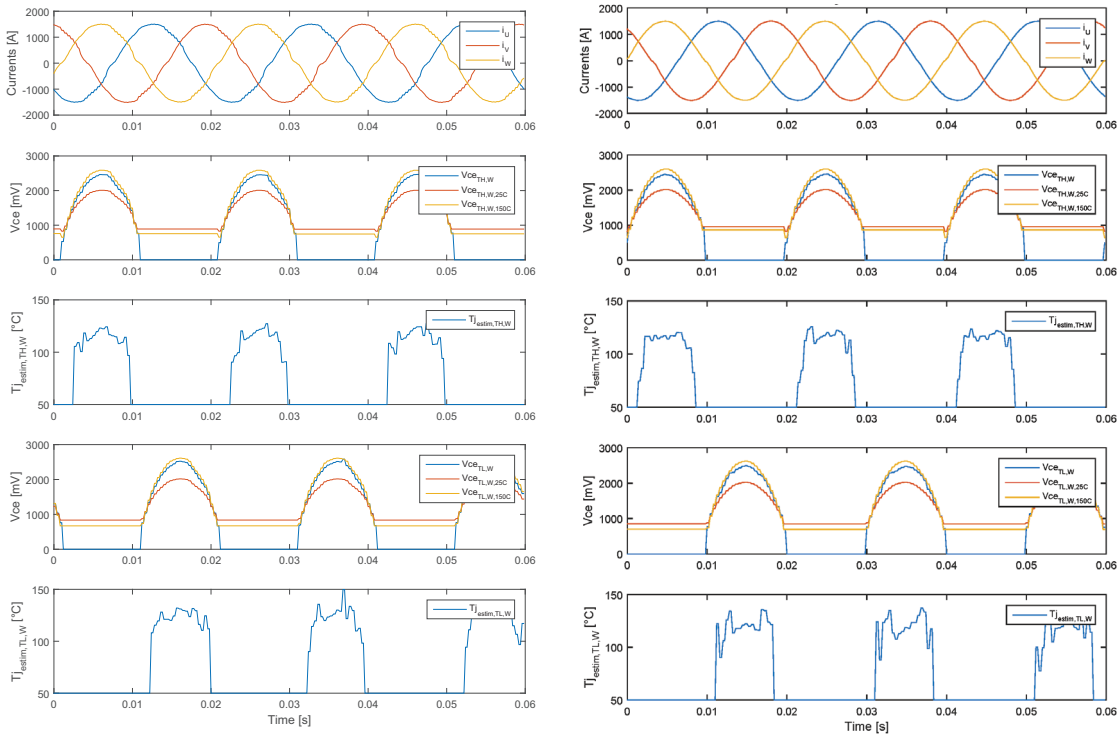
The converter is operated at nominal power rating of the semiconductor devices. The test conditions are tabulated in Table I. The actual current, $\upsilon_{ce,on}$ measurement, and estimated temperature using Eq. 1 are

Table I: Test parameters

Symbol	Meaning	Magnitude
V_{DC}	DC link voltage	$1070\,V$
$V_{AC,RMS}$	AC voltage	$650\,V$
i_L	Load current	$1080\,A$ at PF=1
i_L	Load current	$1060\,A$ at PF=0.8 inductive
$T_{cooling,outlet}$	Cooling temperature	$65°C$
Q_{liquid}	Liquid flow	$45\,l/min$

demonstrated in Fig. 7 for unity and 0.8 inductive power factor. In the first subplot load currents are shown for phase *u*, *v* and *w*. Similarly, in the second subplot $\upsilon_{ce,on}$ and calibrated voltage at $25°C$ and $150°C$ are shown for high side IGBT. In the third subplot Fig. 7, the junction temperature estimation

is shown for the high side IGBT of the phase W. Similar to the high side, the measurement data for the low side of the phase W is shown in subplot 4 and 5. Similar data was measured on the other two phases where data are not shown. It can be seen that the temperature estimation is somewhat noisy, because of junction capacitance and settling time required by the on-state voltage measurement circuit. It is however noticed that if the noise is filtered out, the junction temperature are still way below the maximum operating temperature of 150°C.



(a) PF=1.

(b) PF=0.8 inductive.

Figure 7: Junction temperature estimation.

Experimental Test Setup

The converter is operated in an inverting mode, modulating the output voltage using space vector pulse width modulation (PWM). To be able to detect the inverter power limit, a test setup for power circulation is needed. Fig. 8 shows the simplified schematic of a power circulation circuit that can be realized. One converter will produce a pulse width modulation (PWM) voltage while the other converter will be used to control the current in the inductor, for example using a proportional integral controller.

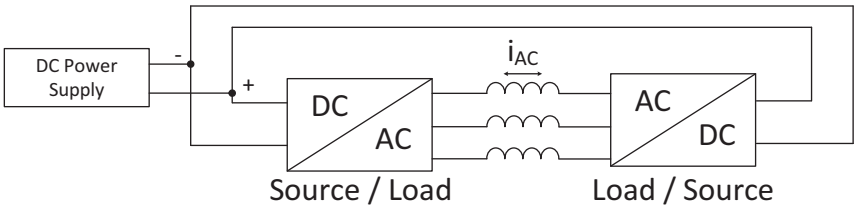


Figure 8: Test setup schematic for power circulation.

A power supply is required to supply the power losses in the circuit, and used to adjust the level of the DC link voltage for testing. Parameters that can be adjusted by control are: AC frequency, AC voltage, AC current, and power factor. Therefore, such a system is advantageous when the converter must be tested at different frequency operation resulting in testing of either a grid side converter or a generator

side converter from a full scale or doubly fed induction generator based wind turbine. Adjusting the current and power factor references the test can emulate the operation in any of the four quadrants.

To avoid unwanted harmonic currents, dead-time compensation is necessary to be done for both converters. Moreover, to enhance the current control bandwidth it is necessary to feed-forward the voltage reference from the converter that controls the voltage to the current controlled converter in a similar way like a grid converter uses grid voltage feed-forward. That can easily be implemented if a single control platform is used to control both converters, like in this case.

Depending on the sign of of the current, it can be said that one converter acts as source and the other as load.

Fig. 9 shows the simplified electric schematic and the power converters used in the setup. For practical reasons, due to the limited power capability in the available hardware, two power converters in parallel are used to control the current flow in the inverter under test. The inductor used is a three-phase nine windings, which provides both differential and common mode inductance to aid the paralleling the two control converters.

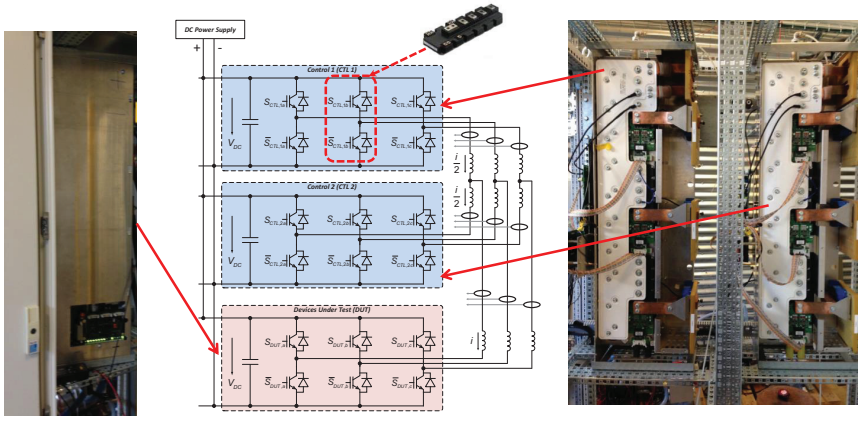
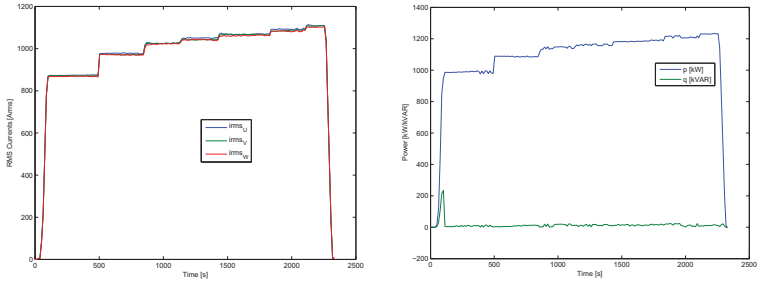


Figure 9: A converter test setup.

All power converters are liquid cooled, using two independent cooling systems. One system for the two control stacks that maintains the outlet temperature at 10 $^{\circ}C$ above the ambient temperature, and another one that controls the outlet temperature of the inverter under test.

Results

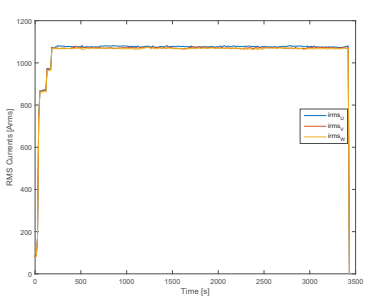
The power limit is detected based on the operating die temperature level as shown in Fig. 7. The peak temperature is detected and increased the power level. Fig. 10 demonstrates an example of power limit detection and increased of power level. Fig. 10a shows RMS load current and Fig. 10b shows corresponding active and reactive power at power factor 1.



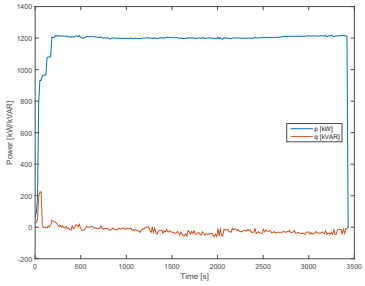
(a) RMS current. (b) Detection of power limit.

Figure 10: Detection and increasing power limit of a power converter.

After reaching close to limit of safe operating point, the converter is operated at full power level as demonstrated in Fig. 11. Fig. 11a shows load current in RMS at maximum power limit and Fig. 11b



(a) RMS current at maximum limit.

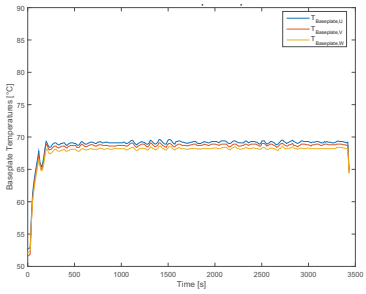


(b) Active and reacive power at maximum limit.

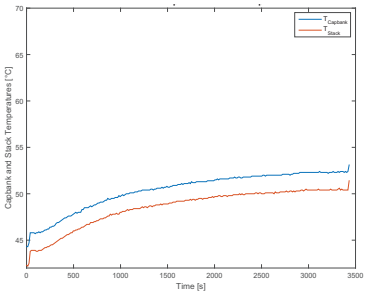
Figure 11: Opeartion at maximum limit of power converter.

shows corresponding active and reactive power at power factor 1.

It is equally important to maintain power stack ambient temperature with in a safe limit to not add additional stress on passive components, control interface and other parts of a converter. Fig. 12a shows baseplate temperature at high power level. Similarly, Fig. 12b shows the rise in power stack temperature upon increasing the power level at maximum limit.



(a) Basepale temperature.



(b) Power stack temperature.

Figure 12: Baseplate and power stack ambient temeprature to ensure safe operation at maximum power limit.

Discussion

The maximum operating temperature limit of a power module determines the maximum power capability of a power converter. However, there are constraints to reduce the size as well as maintain an optimum performance of the converter. Online die temperature detection adds a great advantage to increase the operating power limit of a power module. Initially, as displayed in Fig. 7 the monitoring of die temperature is displayed in an inverter operation. Together with the die temperature, cooling temperature, stack ambient temperature, and electrical parameters are monitored continuously. Based on the peak temperature, the output circulating current is increased as shown in Fig. 10a. At designed power, the operating temperature is observed at less than $130°C$. The output current is increased step by step and monitored the rise in die temperature. The power module is designed to be functional until maximum operating temperature upto $150°C$. Hence the power output is increased until the die temperature reaches under $150°C$. The converter designed to operate at 600 kW - 700 kW is operated safely at close to 1.2 MW under a safe die temperature limit. Initially, the converter is designed with 1000 A power module, which is also replaced with 1400 A power module to increase the load current. The increment in power dissipation and power density also raises a stack and an ambient temperature around capacitor bank, which is closely monitored continuously. Using this method a low voltage power stack power density is increased from 11.16 $kW/litre$ to 19.13 $kW/litre$. A comprehensive test with monitoring of all stress parameters are required further. Similarly, a long term reliability test is under investigation.

Conclusions

A power converter with on-state voltage measurement of power devices was designed and tested. The feedback from the advanced gate provides a closer to reality method to estimate the temperature based on the temperature sensitivity of the on-state voltage drop on the IGBTs. A calibration method was used to measure the devices characteristics at different temperatures. Monitoring the estimated junction temperature, it was shown that the converter can safely operate at around 1.2MW, built in a standard size for 600 - 700 kW converters. Furthermore, a long term reliability test is under investigation to increase the viability of the proposed method.

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