FEM Thermal Modeling and Improvement for High Power IGBT Modules Used in Wind Turbine Systems

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FEM Thermal Modeling and Improvement for High Power IGBT Modules Used in Wind Turbine Systems

Amir Sajjad Bahman *, Ke Ma *, and Frede Blaabjerg *

Abstract – Thermal management of high power IGBT (Insulated Gate Bipolar Transistor) modules is crucial to ensure the reliable operation of power electronic systems especially in wind power applications. The important stage in thermal management of power modules is temperature estimation inside the IGBT modules. Generally, thermal information on datasheet is used to estimate transistor and diode chip temperatures, but this information is based on average and rough temperature measurements. In addition this information does not consider thermal coupling impact between the chips and the impact of different cooling conditions on thermal behavior of power module. In this paper, a detailed 3D thermal network of high power module is presented based on FEM (Finite Element Method) simulation. The thermal coupling impact between chips will be studied and the transient thermal impedances will be examined under different cooling conditions. Finally, the extracted thermal network will be validated with a circuit simulator for a fast temperature estimation with a given loss profile.

Keywords: Finite element method, High power modules, transient thermal impedance, and thermal coupling

1. Introduction

Nowadays, power electronic devices like high power IGBT modules have found wide applications in many industries, such as renewable energy systems, traction and high power motor drives [1], [2]. With the increase of power densities and integration of power electronic systems, like in wind energy systems, manufacturers demand IGBT modules which can withstand high currents and adverse power/thermal cycling, which e.g. occur frequently in wind turbines. Applying high current power modules leads to a larger amount of power dissipation, which generates a significant amount of heat inside the power module. Since the reliability of power modules has a direct relationship to the thermal behavior of the semiconductor devices, larger power/thermal cycling may have negative impact on reliability problems and may also cause wear out failures like solder cracking and bond-wire lift-off [3]-[5]. In addition, it has been proven that the thermal behavior of power modules has direct influence on the reliability of power electronic converters [6], [7]. Therefore, the accuracy of the methods that are applied to capture the temperatures inside module or estimate the temperatures is an important step to improve the reliability of converter design.

Today, there are many methods to determine the junction temperature based on experimental measurements and temperature calculations using datasheet information provided by manufacturers [8]-[14]. Experimental setups can give accurate temperatures by using thermal infrared cameras or using voltage/current sensors or thermocouples, but in many cases they are costly and modification of the device. Other methods are based on the thermal estimation with the information by manufacturers in datasheets. This information gives only an average temperature of the IGBT module and does not provide any information regarding different layers and accurate temperatures distribution in different locations of the chips. Besides, the thermal coupling impact between IGBT and diode chips as well as different environmental conditions are not considered in the thermal curves from the datasheet.

This paper focuses on the identification of transient thermal impedances of high power IGBT modules by means of FEM analysis. The structure of the IGBT module is explained and simulated with a FEM tool. Thermal couplings between IGBT and diode chips are studied with different chip locations and distances between the chips. Also thermal impedance curves are extracted in different cooling conditions. Based on the discussions, a 3D thermal impedance network is presented, which is a simplified model to substitute the FEM simulation for long term loss profiles.

2. Modeling of High Power IGBT module in FEM

In this section the high power IGBT module which is going to be studied is modeled using a commercial FEM software, ANSYS Icepak, for thermal study in both

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transient and steady state modes. The target IGBT module consists of 6 half-bridge converters connected in parallel and placed on 6 separated DCBs (Direct Copper Bonded). All DCBs are placed on a common copper baseplate. The baseplate is placed on a cooling system which is defined as a wall with thermal boundary condition. The schematic of the IGBT module is given in Fig. 1.

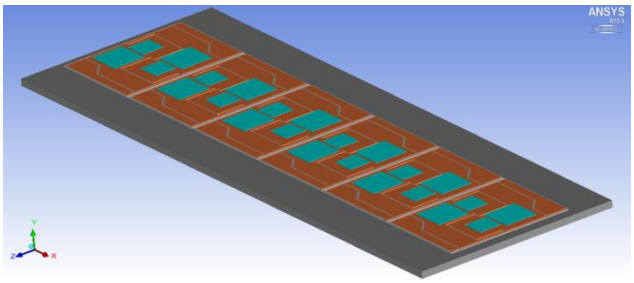


Fig. 1. Graphical view of high power IGBT module developed in ANSYS Icepak.

The geometries and materials of thermal properties have been provided by IGBT module manufacturer. For better studying of thermal behavior of IGBT module, thermal conductivities of different materials are set to be temperature dependent. The main reason is that the materials used in IGBT module, especially copper and silicon, behave differently at various temperatures, so using a constant thermal conductivity for the materials lead to wrong temperature estimation at higher power levels. Since this paper is focused on thermal behaviors from junction to case, the bond-wires are ignored for simplification. The vertical cross-section of the IGBT module is shown in Fig. 2 with materials indicated at different layers. As discussed in the introduction, most of the wear-out failures inside the module occur on bond-wire interconnections to chips and soldering layers. Hence, the critical points to be studied in this paper are defined in the junction layer and two soldering layers underneath the silicon chips and DCBs.

The target IGBT module is loaded with a three-phase DC-AC voltage source converter which is shown in Fig. 3. The converter specifications are presented in Table I.

The converter is modeled in a circuit simulator to

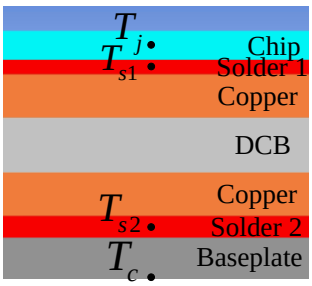


Fig. 2. Cross-section layers of IGBT module.

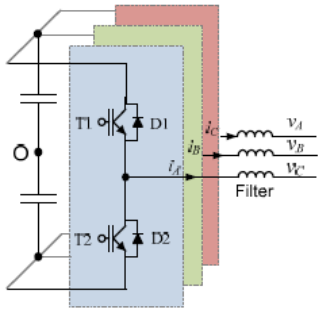


Fig. 3. Two-level voltage source DC-AC converter.

Table 1. Parameters of the power converter shown in Fig. 3.

Rated output active power P_o	250 kW
Output power factor PF	1.0
DC bus voltage V_{dc}	1050 VDC
*Rated primary side voltage V_p	690 V rms
Rated load current I_{load}	209 A rms
Fundamental frequency f_o	50 Hz
Switching frequency f_c	2 kHz
Filter inductance L_f	1.2 mH (0.2 p.u.)
IGBT module DP1000B1700TU103717	1700V/1000A

calculate the power losses, since the input data for the FEM simulation are average power losses for IGBT and diode chips. The loss profile used to inject to chips are given in Fig. 4.

To calculate more accurate temperatures, a multi-level meshing process is executed in FEM analysis, which means for the mentioned critical layers (junction and solder layers), higher level of meshing is executed rather than other layers like DCB or baseplate. The power losses are considered as one of the boundary conditions in the FEM analysis; the other boundary condition is the baseplate interface layer to the heatsink system. In this paper two conditions of constant temperatures (i.e. hot plate in this case) and constant heat transfer coefficient (i.e. fluid cooling system in this case) are taken into consideration.

As an example Fig. 5 shows the temperature profile on IGBT module with the loss profile given in Fig. 4 and when

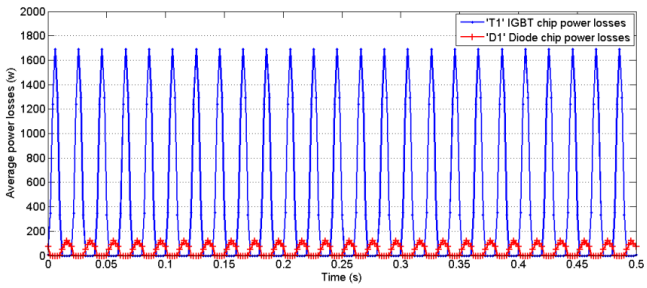


Fig. 4. Average power losses in the IGBT module calculated by PLECS

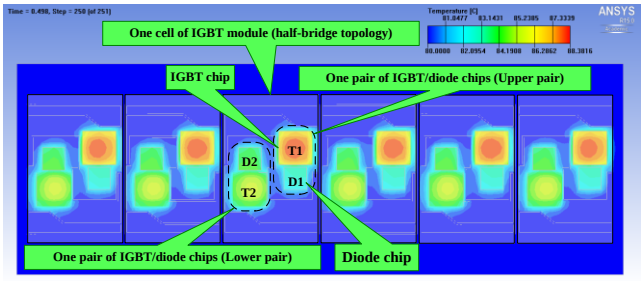


Fig. 5. Temperature distribution in 6 cell IGBT module in a real operating condition.

the upper IGBT chips are conducting (like T1). The power losses are injected in the volume of chips uniformly. For the thermal boundary condition, fixed temperature at 80° C is set underneath the baseplate. Since the baseplate has a large surface to spread the heat propagated from chips and also copper has a large thermal conductivity, it can be seen that the baseplate shows a homogenous and fixed temperature like the hot plate temperature.

3. Thermal coupling effects between chips

As it is observed in Fig. 5, the temperatures of IGBT/diode chips are not symmetrical distributed over the surfaces of the chips and they are oriented to their individual IGBT/diode pairs. This behavior is called thermal coupling between chips. It is observed that each section of half-bridges is placed on the baseplate as the least thermal coupling occurs between adjacent sections. Besides, the thermal coupling between two pairs of IGBT/diode chips on each sections are negligible comparing to thermal coupling between IGBT and diode chips in an individual pair. For example the thermal coupling between T2/D2 and T1/D1 pairs can be ignored compared to the thermal coupling between T1 and D1. In order to study the thermal distribution in the chips, nine equally distanced measurement points are considered on the surface of each IGBT and diode chip. These points are shown in Fig. 6.

The loss profile given in Fig. 4 is injected equally to the

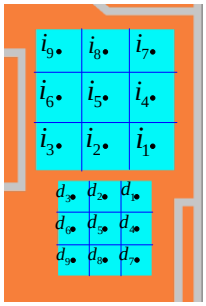
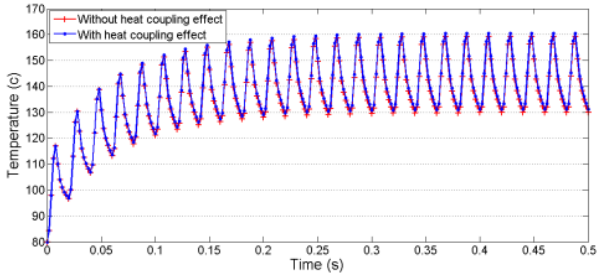
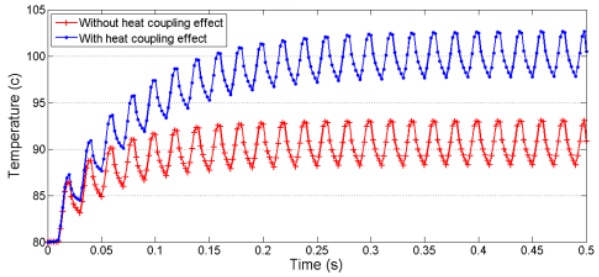


Fig. 6. Temperature monitoring points on IGBT and diode chips



(a) i_2



(d) d_2

Fig. 7. Transient temperatures with and without thermal coupling effects for the i2 and d2 measurement points (Fig. 6) with power losses given in Fig. 4.

IGBT/diode pairs. The temperature responses for two states, when only IGBT or diode is conducting and when both IGBT and diode are conducting are shown in Fig. 7. The results show that with lower power losses of diode chip compared to IGBT chip, the thermal coupling from diode to the IGBT chip is ignorable.

4. Thermal Impedance under Different Loss and Cooling Conditions

There are some other important external factors which influence the thermal behavior of the high power IGBT modules such as loading conditions, ambient temperature, cooling system, etc. In this paper two factors of loading and cooling conditions are going to be studied. The parameter which represents thermal characteristics of the IGBT module is the thermal impedance, $Z_{th}(t)$, which is defined as (1).

$$Z_{th}(t) = \frac{\Delta T(t)}{P} \quad (1)$$

where $\Delta T(t)$ is the temperature rise to a predefined reference point and P is the power losses. The IGBT module chips are fed with different power loss levels of 50W, 450W and 1000W. The power loss is injected uniformly to the volume of IGBT chip and the temperature is measured in the middle of IGBT chip and underneath the baseplate, as junction temperature and case temperature respectively. So applying eq. (1) gives the junction to case thermal impedance. The calculated thermal impedances are shown in Fig. 8. The thermal impedance curves show the

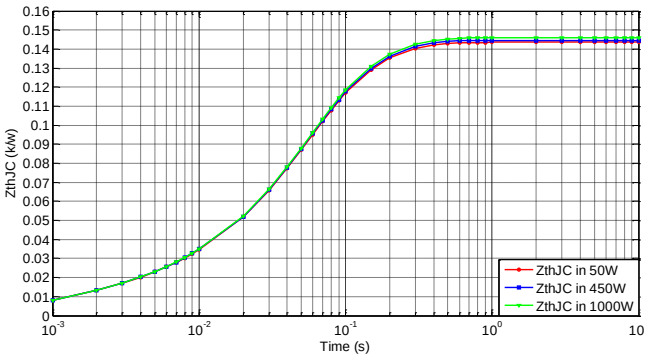


Fig. 8. Thermal impedance curves for different IGBT loss levels.

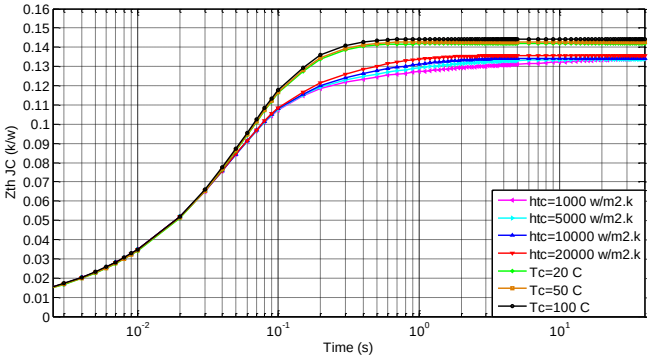


Fig. 9. Thermal impedance curves for different cooling conditions.

same values for the transient time. The differences can be seen in the steady-state condition with 3% difference between the lowest thermal impedance and the highest one. The reason originates from the dependency of materials thermal conductivity to temperature variation, especially in higher loading levels.

On the other hand, the IGBT module is placed on different cooling conditions including fixed hot plate or different water cooling systems. To model the hot plate, constant temperatures of 20°C, 50°C and 100°C are assumed underneath the baseplate. In addition to model the water cooling system, different thermal boundary conditions are considered as a wall underneath the baseplate. For each boundary condition the HTC (Heat Transfer Coefficient) of related cooling condition is defined. HTC is used in thermodynamics to represent the amount of heat which is transferred between a solid volume and fluid [15]. Using equivalent HTC instead of real water cooling system will simplify the model and reduce the simulation time. The FEM simulation results are shown in Fig. 9. It is observed that with higher HTC, the thermal impedance from junction to case decreases, especially in the transient time. The reason is that higher HTC gives smaller heat spreading over the baseplate surface that leads to a higher temperature on the case and higher thermal impedance from junction to case. Similarly, lower HTC gives larger heat spreading over the baseplate surface, which leads to higher temperature on the case and larger thermal impedance from junction to case. In addition, keeping the temperature at the backside of the baseplate at a constant value means an infinitely high HTC. This again results in a very low heat spreading and higher thermal impedance from junction to case.

5. Simplified 3D Thermal Impedance RC lump Network

5.1 Model Extraction from FEM analysis

In this section, a three dimensional thermal impedance network is presented based on FEM thermal model. This model can be used in circuit simulators like PLECS [16] or PSpice [17] for a fast simulation of the thermal behavior especially with long-term loss profiles. As it was described in the previous sections, the critical points inside the high power IGBT module are where failures occur in junction and soldering layers. According to this, a detailed thermal impedance network can be extracted from nine temperature measurement points as shown in Fig. 6 and in junction, cheap soldering, DCB soldering and case layers of IGBT module. This network is shown in Fig. 10. In this figure, *j* stands for junction layer, *s1* stands for chip solder layer and *s2* stands for DCB (or baseplate) solder layer. $Z_{th(a-b)}^{im}$ and $Z_{th(a-b)}^{dm}$ are thermal impedances of point *m* between lay er *a* and layer *b* for IGBT chip and diode chip resp ectively. $Z_{th(a-b)}^{(dm-coupl)}$ means coupling thermal impedanc e of point *m* between layer *a* and layer *b* for diode chip. As it was shown in section 2, the coupling effect from diode to IGBT is negligible with the loss profile given in Fig. 4 and therefore not shown in the network.

To extract the thermal impedance between each two layers, a step power loss is injected to IGBT/diode chips and the temperature is measured on two target points. Applying (1), the thermal impedance curve can be calculated. The thermal impedance network model, which is used in this paper, is a Foster model and it is shown in Fig. 11. The thermal impedance curves are mathematically curve-fitted to derive the Foster model as given in (2). It must be mentioned that (2) is shown for 4 layers of RC pairs and it can be reduced down till 1 layer for simplification.

$$Z_{th}(t) = R_1.\left(1 - e^{-\left(t/R_1.C_1\right)}\right) + R_2.\left(1 - e^{-\left(t/R_2.C_2\right)}\right) + R_3.\left(1 - e^{-\left(t/R_3.C_3\right)}\right) + R_4.\left(1 - e^{-\left(t/R_4.C_4\right)}\right) \quad (2)$$

in (2), R_i values stand for thermal resistances and C_i st ands for thermal capacitance in each layer.

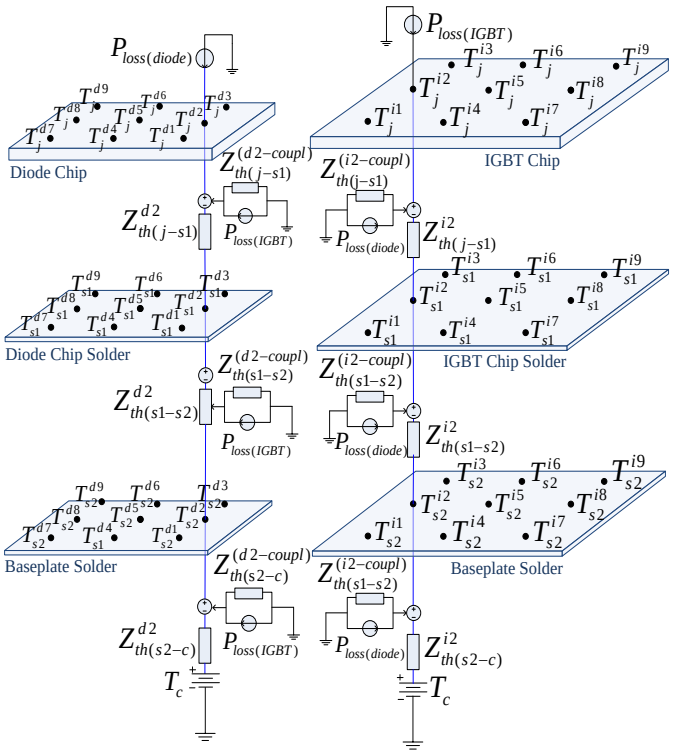


Fig. 10. 3D thermal impedance network for a pair of IGBT/diode chips (Thermal network is shown for i_2 and d_2; all the other measurement points share the same thermal network configuration).

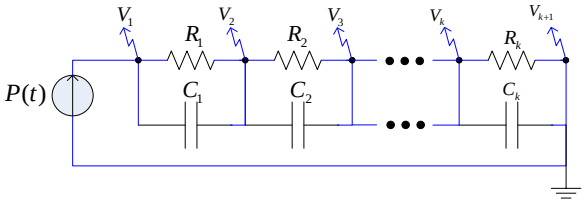
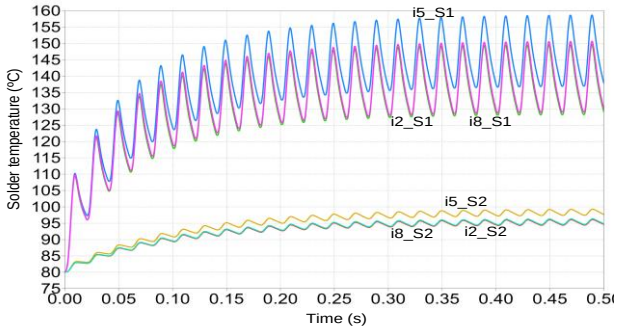


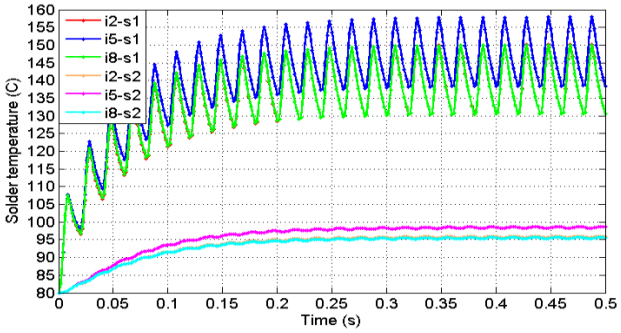
Fig. 11. Foster network of the power devices in the power module

5.2 Thermal network model verification

In this section the presented thermal network is verified with both FEM analysis using ANSYS Icepak and circuit simulator using PLECS blockset in SIMULINK. The loss profile given in Fig. 4 is injected into the IGBT and diode chips and temperatures are measured in the chip soldering and DCB soldering layers for three measurement points of i2, i5 and i8 (as previously described in Fig. 6). The results are shown in Fig. 12.a and Fig. 12.b. Two simulations are well tracking each other with maximum error for i2-s2 with 1.3 % error and minimum error for i8-s1 with 0.4% error. The simulation time needed for PLECS is 15 seconds and it can be run with a Intel i7 3740QM, RAM 8GB system and the simulation time needed for ANSYS Icepak is 12 minutes with an Intel E5-2650, RAM 32GB system. This shows about 80 times faster simulation time. To ensure that the thermal model is valid for other power loss profiles, another loss profile is given in Fig. 13, as an example. The temperatures of solder layers for i2, i5 and i8 are shown in Fig.14.a and Fig.14.b. For this loss profile, the maximum temperature estimation error is about 1.5% that is still acceptable. For better clarification of thermal impedance extraction method, a block diagram is shown in Fig. 15 describing the whole process.



(a) Presented thermal model simulated by PLECS



(b) FEM results simulated by ANSYS Icepak

Fig. 12. IGBT chip solder temperatures on monitoring points i_2, i_5 and i_8 with power losses given in Fig. 4.

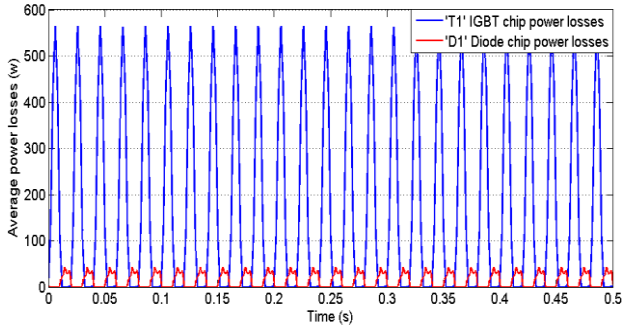
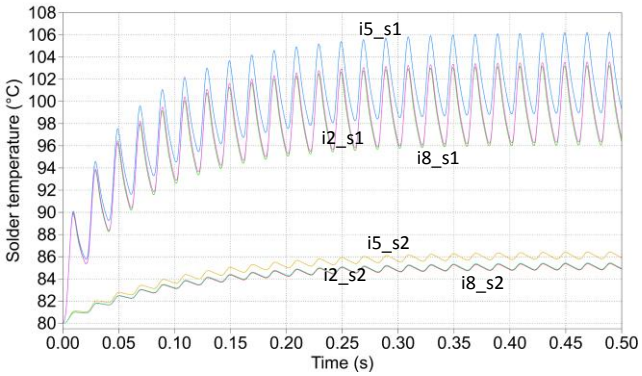
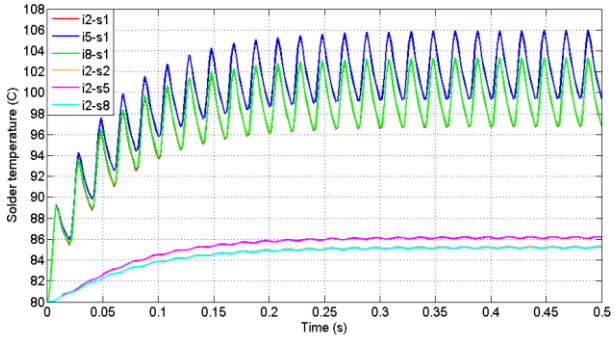


Fig. 13. Average power losses in the IGBT module



(a) Presented thermal model simulated by PLECS



(b) FEM results simulated by ANSYS Icepak

Fig. 14. IGBT chip solder temperatures on monitoring points i_2, i_5 and i_8 with power losses given in Fig. 13.

6. Conclusion

In this paper the thermal behavior of high power IGBT modules, which are used in wind power applications have been studied by means of FEM analysis. The thermal coupling effect between IGBT and diode chips has been studied for different locations on the chips. It was shown that the thermal coupling can be negligible for low power loss values to simplify the thermal model. In addition, the impact of different cooling systems on thermal impedance has been investigated. It was proved that with larger heat transfer coefficient of cooling system, the thermal impedance from junction to case is reduced. Finally based on FEM analysis a 3D thermal impedance network has been derived which can be used in circuit simulators for a fast and easy implementation for long-term dynamic loss profiles. This thermal network can help the converter designers with a fast life-time estimation of device in real operating conditions.

Acknowledgements

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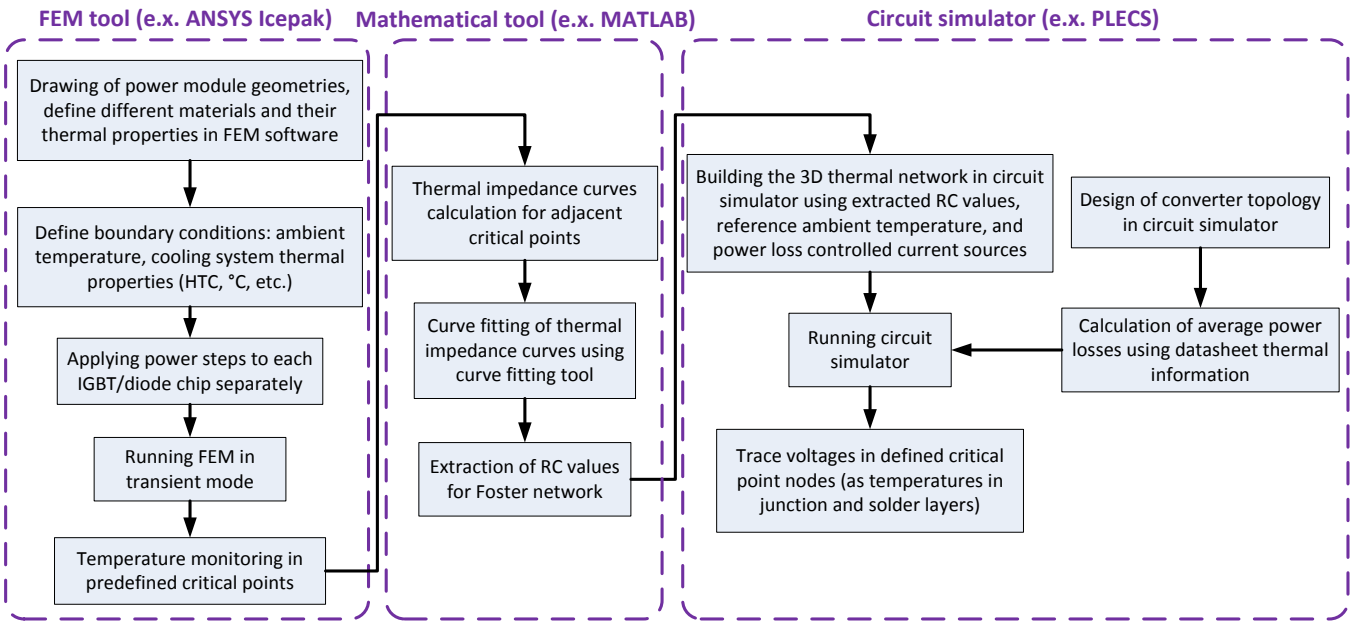

Fig. 15. Block diagram of thermal impedance network extraction process

physical model for lifetime estimation of power modules," in Proc. IPEC'10, pp. 2106-2114, 2010.
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