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Discrete-Time Domain Modelling of Voltage Source Inverters in Standalone Applications: Enhancement of Regulators Performance by Means of Smith Predictor

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***Abstract*— The decoupling of the capacitor voltage and inductor current has been shown to improve significantly the dynamic performance of voltage source inverters in standalone applications. However, the computation and PWM delays still limit the achievable bandwidth. In this paper a discrete-time domain modelling of the LC plant with consideration of delay and sample-and-hold effects on the state feedback cross-coupling decoupling is derived. From this plant formulation, current controllers with wide bandwidth and good relative stability properties are developed. Two controllers based on lead compensation and Smith predictor design, respectively, are obtained. Subsequently, the voltage regulator is also designed for a wide bandwidth, which permits the inclusion of resonant filters for the steady-state mitigation of odd harmonics at nonlinear unbalance load terminals. Discrete-time domain implementation issues of an anti-wind up scheme are discussed as well, highlighting the limitations of some discretization methods. Extensive experimental results, including a short-circuit test, verify the theoretical analysis.**

***Index Terms*— Current control, voltage control, power quality**

I. Introduction

THE design of voltage and current regulators for Voltage Source Inverters (VSIs) intended for standalone applications, i.e. islanded microgrids or Uninterruptible Power Supply (UPS) systems, should aim to achieve good performance during steady-state and transient conditions. This means the system should be operated with wide stability margins. The poor dynamics of these regulators are responsible for degraded performance of the overall control system. Thus effective control design and implementation of the regulators is mandatory. In this context, four general requirements are usually imposed on any current or voltage regulator [1]: i) to achieve zero steady-state error; ii) to accurately track the commanded reference and reject any disturbance; iii) to widen the closed-loop control bandwidth as much as possible to achieve fast transient response; iv) to reduce the total harmonic distortion by compensating for low order harmonics. Mandatory requirements specifically for AC power supply/UPS systems are fault and peak current protection [2].

A possible design of voltage or current regulators is based on Proportional Resonant (PR) controllers in the αβ stationary reference frame. This structure is equivalent to two Proportional Integral (PI) controllers, one for the positive and the other for the negative sequence in the synchronous reference frame [3]. Independently of the PR controller structure, the effect of delays and voltage coupling in standalone applications should be carefully considered in the design stage. In particular, as proved in a recent publication [4], the coupling between the capacitor voltage and inductor current in VSIs with LC output filter, which is usually the case in UPS systems [5], degrades the dynamics of the inner regulators.

A possible approach for analysis is based on s-domain models, which are useful as they improve the general perception of the dynamic behavior of pulse-width modulators [6]. Subsequently, the design of the regulators in the s-domain is followed by their discretization. However, the mapping from the s-domain to the z-domain can introduce some discrepancy, depending on the discretization method used [5], [7]. On the other hand, the direct design of digital compensators in the discrete-time domain provides more accuracy, being able to capture the sampling effects. In fact, the transformation of the system in the discrete-time domain

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by means of z-transform or discrete-time modelling in state-space form allows the sample-and-hold effect and time lag to be treated accurately [8]-[11], without the need of using the approximated rational transfer functions of the delay [12]. Moreover, the methodology presented in [13] allows the Cross-Coupled State Equations of a system with coupled variables and multiple feedback paths to be derived, following a discretization approach. This is the approach to be used in order to correctly represent the coupling between the controlled states. In general, other advantages can be identified for direct design in the z-domain: i) design for direct discrete-time pole-placement [14], [15]; ii) improved dynamic performance and robustness of the regulators [16], especially if the ratio of the sampling frequency to the fundamental frequency is low [14] or the current regulator is tuned for a very wide bandwidth [17]. Accordingly, z-domain modelling is considered convenient for an accurate design.

Usually, when voltage decoupling is performed, the influence of compensating for computation and PWM delays on the state feedback decoupling path is not taken into account. In fact, in previous works, the decoupling of the controlled states does not take into account the effect of computation and PWM delays when performed. Specifically, state feedback decoupling has often been used for decoupling the cross-coupling caused by the implementation of current controllers in the synchronous reference frame [1], for decoupling the back-emf effect in dc [18] and ac drives [19] (resulting in a current control strategy independent of the speed), and for decoupling current and voltage states in dc-dc converters [20] and UPS systems [4], [21]. Nevertheless, in these applications the decoupling is analyzed in the continuous time domain. Because the delays introduced by the discrete-time modelling are not present, the resulting model used to design and analyze the inner current loop is simply the model of an RL load. This is equivalent to considering the decoupling as ideal. Nevertheless, system delays significantly degrade the performance of state feedback decoupling. As proved in [4], the state feedback decoupling action can be improved by leading the capacitor voltage on the state feedback decoupling path. Moreover, the possibility to widen the current loop bandwidth either by means of a lead compensator on the forward path or a Smith Predictor structure has not previously been investigated, and is the main original proposal of this work. To the best knowledge of the authors, no deep analyses in the discrete-time domain have been previously provided for these kinds of techniques. As will be shown in the paper, both structures allow good dynamics properties to be achieved as the controller bandwidth is widened. However, the way these techniques aim at compensating for system delays is different. Specifically, the lead compensator adds an additional degree of freedom to the system in order to directly locate the poles of the closed-loop controller transfer function. On the other hand, the Smith predictor structure permits the design of the controller based on the un-delayed model of the physical plant by building a parallel model which cancels the system delay. As the current regulator dynamics are enhanced, the voltage loop dynamics are widened as well. In this paper it is shown how an accurate modelling of the delay effects in decoupling leads to a better control design and dynamics assessment.

A model in the discrete-time domain which takes into account the coupling of the capacitor voltage with the inductor current, even if voltage decoupling is performed, is derived analytically. This model is shown to better represent the physical system being addressed. It is important to note that even without the one sample delay introduced by computation, the sample-and-hold effect is still present and limits the achievable bandwidth, thus reducing the benefits introduced by the decoupling. The effect of widening the inner current loop bandwidth by means of two techniques based on a lead compensator structure and Smith Predictor is proposed. Finally, the results obtained for the current loop analysis are applied to design the voltage loop, based on the Nyquist criterion. A straightforward mathematical formulation to select the fundamental integral gain of the resonator by moving the zeros of the controller to the real axis is used for practical design.

This work is organized as follows. In Section III the model in the discrete-time domain which takes into account the coupling of the controlled states is derived. The devised model is compared to the simplified formulation based on an RL load and the main differences are discussed. In Section IV the inner loop current control with state feedback voltage decoupling is analyzed. Two techniques aimed to widen the bandwidth of the current regulator, based on a lead compensator structure and Smith Predictor, are proposed and compared. Subsequently, in Section V, a PR voltage controller design is proposed based on the design of the current regulator with wide bandwidth. Detailed design and tuning is provided according to the Nyquist criterion. Moreover, discretization issues of an anti-wind up scheme for the voltage regulator are analyzed. In Section VI the theoretical solution is supported by experimental results, verifying their compliance with the IEC 62040 normative for UPS systems.

II. System Description

In standalone applications, the VSI is implemented with an LC filter at its output. In general, it operates in voltage control mode with the capacitor voltage and inductor currents being the controlled states. Fig. 1 shows the block diagram representation including a three-phase power converter with its inner loops. The inner current loop has to track the commands provided by the outer voltage loop and to ensure disturbance rejection within its bandwidth [17], [22].

The simplified block diagram representation of the closed-loop system is shown in Fig. 2, where $\boldsymbol{V}^*_{C\alpha\beta} = V^*_{C\alpha} + jV^*_{C\beta}$ and $\boldsymbol{I}^*_{L\alpha\beta} = I^*_{L\alpha} + jI^*_{L\beta}$ are the voltage and current reference vectors and $\boldsymbol{I}_{o\alpha\beta} = I_{o\alpha} + jI_{o\beta}$ is the output current vector, which acts as a disturbance to the system. $G_i(z)$ and $G_v(z)$ represent the current and voltage regulators transfer functions (TF) in the discrete-time domain. There is one sample computational delay associated to the implemented regular sampled symmetrical PWM strategy, i.e. the time required to

compute the duty-cycle control signal [9], [23]. $G_{dec}(z)$ is the TF related to the decoupling of the cross-coupling controlled states. The capacitor $C_f = 3C$ is the equivalent capacitance of a Y connection configuration.

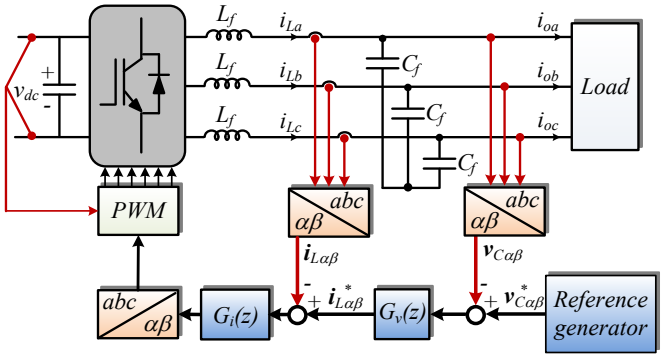


Fig. 1. Block diagram of a three phase VSI with voltage and current loops.

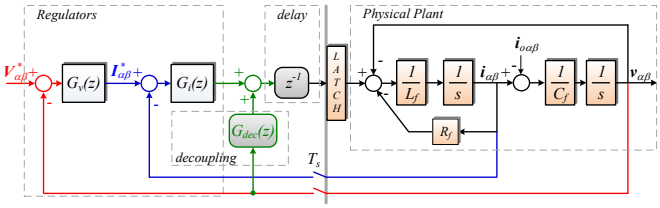


Fig. 2. Simplified block diagram of the closed-loop system.

III. Discrete-Time Domain Plant Modelling

As voltage decoupling is performed, higher damping is achieved with less overshoot for a given bandwidth [4]. If it was possible to exactly decouple (cancel) the capacitor coupling, the system would become not dependent on the load impedance and the physical plant could be represented by an RL load. In this case, the modelling in the discrete-time domain is based on the Z-transform of the part of the plant related to the inductor current $G_p(s)$ along with the sample-and-hold effect [10], leading to

$$G_p(z) = \frac{\boldsymbol{I}_{L\alpha\beta}}{\boldsymbol{V}_{i\alpha\beta}} = \boldsymbol{Z}\{\boldsymbol{L}\{Latch\}G_p(z)\} = \\ = (1-z^{-1})\boldsymbol{Z}\left\{\frac{G_p(s)}{s}\right\} = \frac{1}{R_f}\frac{(1-e^{-T_s/\tau_p})z^{-1}}{1-e^{-T_s/\tau_p}z^{-1}}. \quad (1)$$

Where $\boldsymbol{I}_{L\alpha\beta}(z)$ and $\boldsymbol{V}_{i\alpha\beta}(z)$ are the inductor current and input voltage in the z-domain, respectively; $\tau_p = L_f/R_f$ is the plant time-constant. However, the coupling effect introduced by the second-order LC filter cannot be neglected, because of computation and PWM delays which are not fully compensated for on the state feedback decoupling path. Even without the one sample delay introduced by computation, the latch interface is still present, not allowing the complete decoupling of the controlled states. The effect of capacitor voltage in the dynamics should be considered in the design stage [24]. For this reason, a model which reflects this effect has been developed. The general methodology, here reported, is similarly applied in [13].

Step 1: Model and derive the Ordinary Differential Equations (ODEs) of the system;

Step 2: Form the Laplace transform of the ODEs including the effects of initial conditions;

Step 3: Form a step input for the latched manipulated input;

Step 4: Find the continuous time step response solution;

Step 5: Find the response at the next sampling instant;

Step 6: Generalize the solution for arbitrary sampling instants (kT);

Step 7: Form eventually the correspondent transfer function in the discrete-time domain.

With reference to Fig. 3 and neglecting the disturbance $i_o(t)$, the ODEs of the system are

$$\begin{cases} \dfrac{d}{dt}v_c(t) = \dfrac{1}{C_f}i_L(t) \\ \dfrac{d}{dt}i_L(t) = \dfrac{1}{L_f}[v_i(t) - Ri_L(t) - v_c(t)]. \end{cases} \quad (2)$$

The equivalent series resistance (ESR) of the filter capacitor C_f is not considered in the model, since its effect appears far above the frequency range of concern [25], it is usually small and has little effect in dynamics. The system in (2) is transformed in the Laplace domain including the effects of initial conditions, fundamental to derive the Cross-Coupled State Equations. The sample-and-hold effect is modelled as $V_i(s) = v_i(t=0)/s$ (input modelled as steps). In particular the relationships between the states are

$$V_c(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}\Big\{v_i(t=0)\frac{1}{s} \\ + \frac{1}{\omega_n^2}[sv_c(t=0) + \dot{v}_c(t=0)] \\ + \frac{2\xi}{\omega_n}v_c(t=0)\Big\}. \quad (3)$$

$$I_L(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}\big[C_f v_i(t=0) \\ + L_f C_f s i_L(t=0) - C_f v_c(t=0)\big]. \quad (4)$$

Where

$$\omega_n^2 = \frac{1}{L_f C_f};\quad \xi = \frac{1}{2\omega_n}\frac{R_f}{L_f} = \frac{R_f}{2}\sqrt{\frac{C_f}{L_f}}. \quad (5)$$

Being ω_n the natural frequency of the plant and ξ the damping factor. Then the inverse Laplace transform is applied to (3) and (4). The continuous time step response is generalized for arbitrary sampling instants, followed by the transformations to the z-domain and αβ stationary reference frame. More details are provided in Appendix. The Cross-Coupled State Equations are thus obtained

$$\boldsymbol{V}_{c\alpha\beta}(z)\Big[1 + \frac{\omega_n}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T - \phi)z^{-1} \\ - \frac{2\xi\omega_n}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T)z^{-1}\Big] \\ = \Big[1 - \frac{\omega_n}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T + \phi)\Big]\boldsymbol{V}_{i\alpha\beta}(z)z^{-1} \\ + \frac{1}{C_f\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T)\boldsymbol{I}_{L\alpha\beta}(z)z^{-1}. \quad (6)$$

$$\frac{\boldsymbol{I}_{L\alpha\beta}(z)}{\boldsymbol{V}^{*}_{i\alpha\beta}(z)} = \frac{1}{1+\frac{\omega_n}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T-\phi)\,z^{-1}}\,C_f\frac{\omega_n^2}{\omega_d}e^{-\xi\omega_n T}sin(\omega_d T)z^{-1}. \quad (7)$$

Where

$$\omega_d = \omega_n\sqrt{1-\xi^2};\ \ \phi = tg^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right). \quad (8)$$

Moreover, $\boldsymbol{V}^{*}_{i\alpha\beta}(z) = \boldsymbol{V}_{i\alpha\beta}(z) - \boldsymbol{V}_{c\alpha\beta}(z)$ is the applied voltage to the model after the voltage capacitor coupling effect in a block diagram representation. It can be clearly seen that the model of the RL load in (7) takes into account the effect of the coupling with the output capacitor by including C_f.

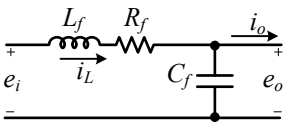


Fig. 3. Single-phase representation of an LC filter.

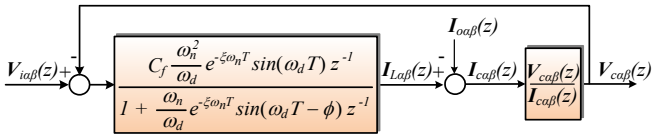


Fig. 4. Discrete time block diagram of an LC filter neglecting the disturbance $\boldsymbol{I_{o\alpha\beta}(z)}$.

Similarly, the relationship between $\boldsymbol{I}_{L\alpha\beta}(z)$ and $\boldsymbol{V}_{C\alpha\beta}(z)$, can be derived. Additional details are provided in the Appendix.

$$\frac{\boldsymbol{V}_{c\alpha\beta}(z)}{\boldsymbol{I}_{L\alpha\beta}(z)} = \frac{a_1+a_2z^{-1}}{b_1(1-z^{-1})}. \quad (9)$$

Where

$$a_1 = 1-\frac{\xi\omega_n}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T) - e^{-\xi\omega_n T}\cos(\omega_d T)$$

$$a_2 = \frac{\xi\omega_n}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T) - e^{-\xi\omega_n T}\cos(\omega_d T) + e^{-2\xi\omega_n T}$$

$$b_1 = C_f\frac{\omega_n^2}{\omega_d}e^{-\xi\omega_n T}\sin(\omega_d T)$$

The block diagram in Fig. 4 shows the complete system here derived, highlighting (7). The closed-loop frequency responses of (1) and (7) with a P controller as current regulator are shown in Fig. 5, considering voltage decoupling. The parameters used are reported in Table II and Table III. The key point is that because of the coupling with the output capacitor, which is modelled by (7), a lower gain is achieved at low frequencies. This model justifies the higher steady-state error observed in both simulation and experiments than with the continuous-time model and the discrete-time one based on (1). For this reason, the plant model in Fig. 4 should be used to design and analyze the system

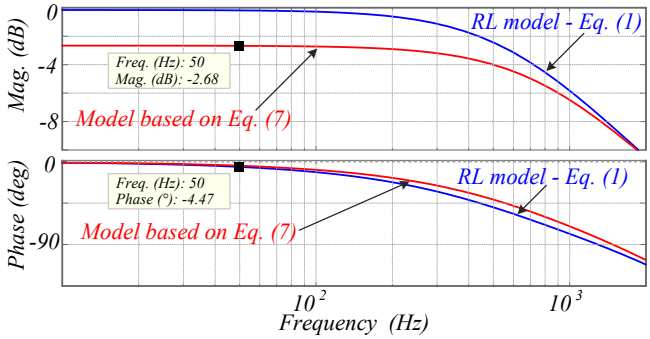


Fig. 5. Frequency response of the closed-loop system of the RL model in (1) and model based on (7), and a P controller with $\boldsymbol{k_{pI}} = \mathbf{5.54}$, neglecting the one sample delay.

A. Validation of the Plant Model by Simulation

The derived model is validated in simulation. With reference to Fig. 2, the block diagram representation of an LC filter only without the current controller is considered (see Fig. 6), using the system parameters in Table II. A discrete-time sinusoidal input voltage is provided as input to the LC filter via a latch interface. For a better understanding, the one sample delay is neglected in this test. The simulation is performed at no load. To effectively validate (7) and (9), the LC filter in Fig. 6 is modelled in two different ways:

1) by using elementary transfer functions Simulink blocks for L_f, R, the integrator terms $1/s$ and C_f. The latch interface is modelled using a Zero-Order Hold block;

2) by replacing $1/(L_f\,s + R_f)$ and the latch interface with (7). Additionally, $1/(Cs)$ is replaced by (9). This is equivalent to test the block diagram in Fig. 4.

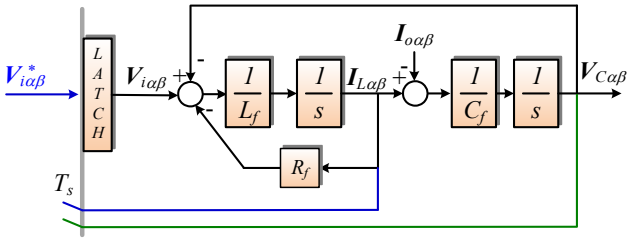


Fig. 6. Block diagram of the physical system.

The inductor current and capacitor voltage provided by the two models are compared. With reference to Fig. 7, there is a perfect match at the sampling instants between the inductor current provided by the two models. It should be noted only model 2) provides access to the inductor current as an internal state. This is a key issue for design purposes. With reference to Fig. 8, the capacitor voltage simulated using the discrete-time model (see Fig. 4) is equal (at the sampling instants) to the capacitor voltage simulated using the continuous-time model.

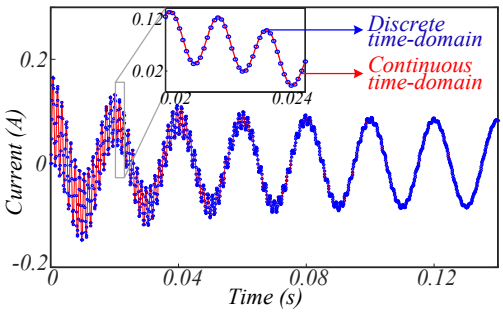


Fig. 7. Inductor current (α-axis) - Comparison of modelling: TF Simulink blocks (plant modelling in the continuous time-domain); current simulated by using the derived model (block diagram showed in Fig. 4).

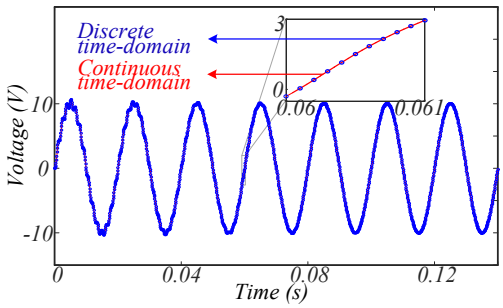


Fig. 8. Capacitor voltage (α-axis) - Comparison of modelling: TF Simulink blocks (plant modelling in the continuous time-domain); voltage simulated by using the derived model (block diagram showed in Fig. 4).

A more rigorous validation is based on applying, in open loop, the actual pulse-width modulated voltage provided by a three-phase power converter to an LC filter at no load conditions. Again, the one sample delay is not included in the analysis. In order to mitigate non-linearity effects introduced by PWM, the physical parameters in Table I are used to perform the simulation. The results are compared with those provided by the model based on (7) and (9).

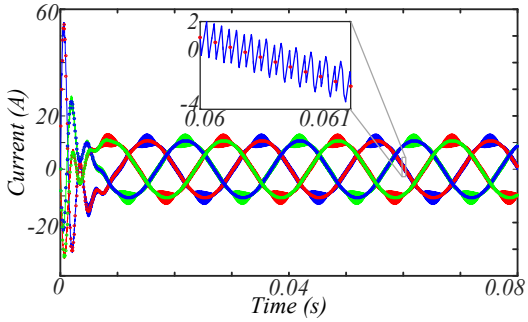


Fig. 9. Inductor current - Comparison of modelling: pulse-width modulated simulation; current simulated by using the derived model in the natural reference frame (block diagram showed in Fig. 4).

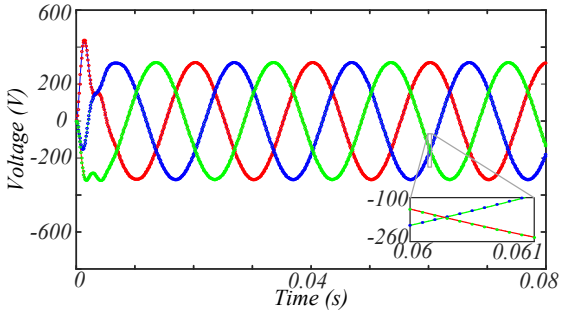


Fig. 10. Capacitor voltage - Comparison of modelling: pulse-width modulated simulation; current simulated by using the derived model in the natural reference frame (block diagram showed in Fig. 4).

With reference to Fig. 9 and Fig. 10, it can be seen the average value of the controlled states provided by the two models are equivalent. In fact, by using synchronous sampling, the average value, mainly of the inductor current, is used for control purposes. All these results demonstrate the correctness of the devised model, which can be used for design purposes.

TABLE I
SYSTEM PARAMETERS FOR SIMULATION PURPOSES

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 108\ \mu F$
Inductor ESR	$R = 10\ \Omega$

To investigate the effect of the latch interface and one sample delay on the closed-loop TF, three different models with the inner current loop only and a P controller as regulator are considered (see Fig. 11, Fig. 13 and Fig. 15). The parameters in Table II and Table III are used for analysis. As the latch interface and one sample delay are neglected [see Fig. 11(a)], the physical system as seen from the controller simplifies to an RL load [see Fig. 11(b)]. This means the state feedback decoupling path perfectly cancels out the physical coupling of the capacitor voltage. As a consequence, the reference current is properly tracked with almost zero steady-state error (see Fig. 12). On the other hand, as the latch interface is included (see Fig. 13) the steady-state error between the reference and real inductor current increases (see Fig. 14). Given the reference current at f = 50 Hz in α-axis $i_\alpha^* = 5$ A, the real inductor current is $i_\alpha = 3.68$ A. This means $i_\alpha = 0.736\ i_\alpha^*$, which corresponds to -2.68 dB, in accordance with the frequency response analysis at 50 Hz of Fig. 5. Additionally, with reference to Fig. 15, it can be seen the combined effect of the one sample delay and latch interface. An even higher steady-state error is observed (see Fig. 16), limiting the current loop control bandwidth. As Fig. 13 and Fig. 15 implement the plant modelling previously verified in Fig. 7 and Fig. 8, it can be concluded that state feedback decoupling is far from being ideal. Thus, a design procedure based on (7) and (9) provides a more accurate pole placement.

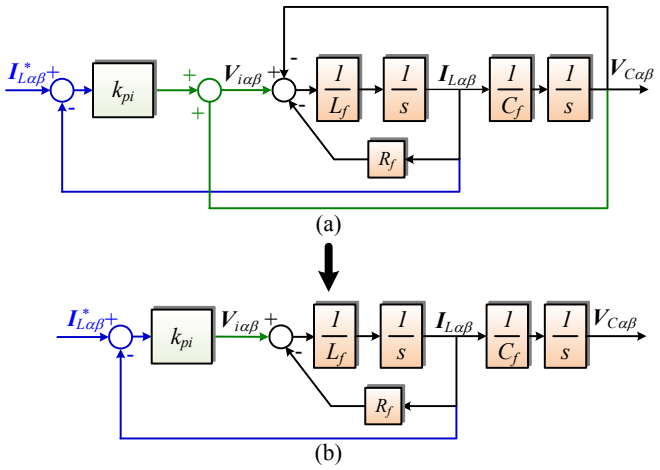


Fig. 11. Block diagram of the physical system with current loop only: (a) Plant modelling in the continuous time-domain; (b) Simplification of (a).

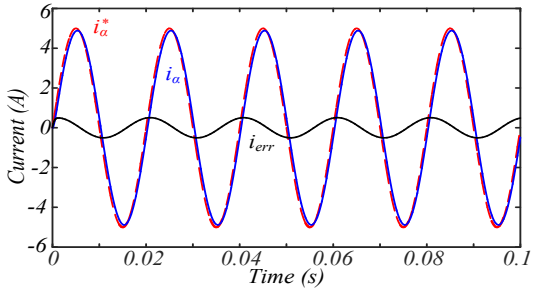


Fig. 12. Command tracking of the inductor current with $\boldsymbol{k_{pI} = 5.54}$: (a) reference, real and inductor current error of the system (α-axis) in Fig. 11.

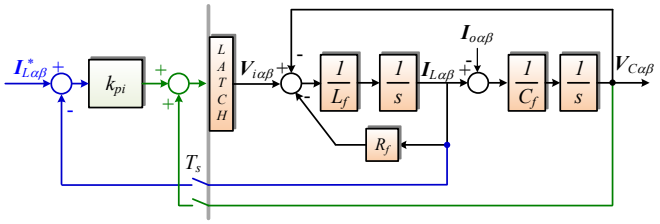


Fig. 13. Block diagram of the physical system with current loop only and latch interface.

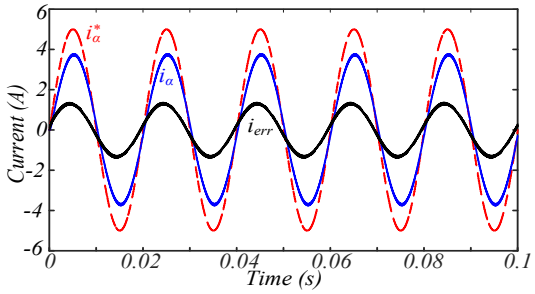


Fig. 14. Command tracking of the inductor current with $\boldsymbol{k_{pI} = 5.54}$: (a) reference, real and inductor current error of the system (α-axis) in Fig. 13.

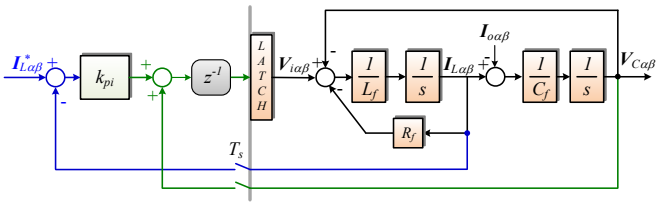


Fig. 15. Block diagram of the physical system with current loop only, latch interface and one sample delay.

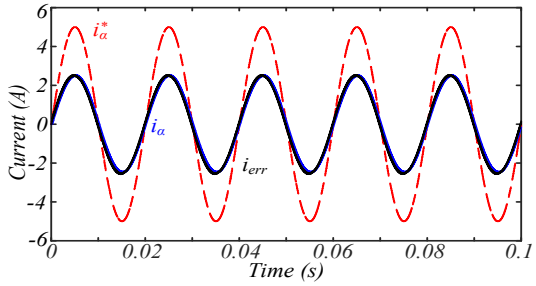


Fig. 16. Command tracking of the inductor current with $\boldsymbol{k_{pI} = 5.54}$: (a) reference, real and inductor current error of the system (α-axis) in Fig. 15.

IV. Current Regulator Design

Since voltage and current regulators are built in a cascade control configuration, serial tuning can be used for design purposes. For this reason, the loop characterized by the fastest dynamics is the first to be designed according to system requirements [26]. The proportional gain k_{pI} of the current regulator is selected to achieve the desired bandwidth (f_{bw}), which in principle has to be much wider than the outer loops [27]. The reason is to avoid interactions between the outer and the inner loops. Moreover, the closed-loop controller bandwidth is mainly limited by the computation and PWM delays [15]. This limitation is overcome by implementing techniques aimed at compensating for the system delays. In this work, it is shown that the current control bandwidth can be designed for a third of the sampling frequency with wide stability margins, either by means of a P controller + Smith predictor or a P controller along with a lead compensator structure. The physical and control parameters for the current loop used both in simulation and in laboratory tests are presented in Table II and Table III.

TABLE II
System Parameters

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 108\ \mu F$
Inductor ESR	$R = 10\ \Omega$
Linear Load	$R_l = 68\ \Omega$
Nonlinear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 155\ \Omega$ $L_{NL} = 0.084\ mH$

TABLE III
Current Regulator Parameters

Parameter	Value
Proportional gain w/o lead	$k_{pI} = 5.54$
Proportional and lead gains $@\omega_{nCL} = 4800\pi\ rad/s,\ \xi_{CL} = 0.707,\ f_{bw} = 3.1\ kHz$	$\begin{cases} k_{pI} = 11.56 \\ k_L = 0.559 \end{cases}$
Proportional gain with Smith Predictor $@f_{bw} = 3.1\ kHz$	$k_{pI} = 14.62$

A simple P controller for the inner current loop, with a decoupling TF $G_{dec}(z) = 1$ (see Fig. 2) and the discrete-time model based on (7) are considered, as shown in the block diagram of Fig. 17.

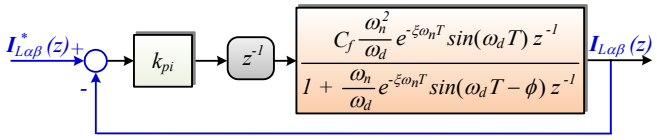


Fig. 17. Block diagram for design the inner current loop, including the lag introduced by computational delay.

The closed-loop TF of the inner current loop in Fig. 17 is

$$\frac{\boldsymbol{I}_{L\alpha\beta}(z)}{\boldsymbol{I}^*_{L\alpha\beta}(z)} = \frac{k_{pI} b}{z^2 - az + k_{pI} b}, \tag{10}$$

Where $b = C_f \frac{\omega_n^2}{\omega_d} e^{-\xi\omega_n T} sin(\omega_d T); a = -\frac{\omega_n}{\omega_d} e^{-\xi\omega_n T} sin(w_d T - \phi)$. For the system parameters in Table II, the root locus is shown in Fig. 18. It can be stated that, because of the delay, there is a limitation in the gain to achieve system dynamics with enough damping. There are two poles and just one variable (k_{pI}) which can change their locations. It is clear that it is not possible to place the roots at any desired location. The designed gain to achieve a damping of $\xi = 0.707$ is $k_{pI} = 5.54$, as presented in Table III.

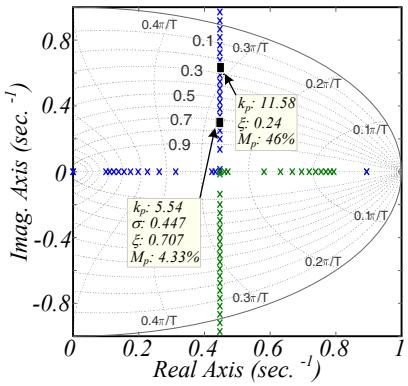


Fig. 18. Root locus of open loop TF in Fig. 17 including the lag introduced by PWM update.

To widen the system bandwidth and still achieve a reasonable damped closed-loop response, it is possible to design a lead compensator as shown in Fig. 19, also referred to as 'Delay prediction and Feedback' [15].

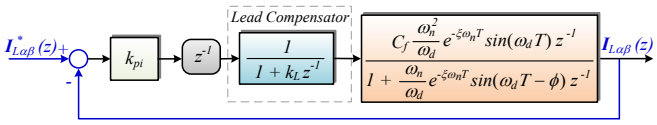


Fig. 19. Block diagram for design the inner current loop, including the lag introduced by computational delay, and the model of the lead compensator.

The closed-loop TF becomes

$$\frac{\boldsymbol{I}_{L\alpha\beta}(z)}{\boldsymbol{I}^*_{L\alpha\beta}(z)} = \frac{k_{pI} b}{(z + k_L)(z - a) + k_{pI} b}, \tag{11}$$

where k_L is the lead compensator gain. The poles of this TF must satisfy the relationship

$$z^2 - (p_1 + p_2)z + p_1 p_2 = z^2 + (k_L - a)z - k_L a + k_{pI} b, \tag{12}$$

where p_1, p_2 are the desired pole locations, defined as

$$p_{1,2} = e^{-\xi\omega_{nCL}T_s}[\cos(\omega_{dCL}T_s) \pm j sin(\omega_{dCL}T_s)], \quad \omega_{dCL} = \omega_{nCL}\sqrt{1 - \xi_{CL}^2}. \tag{13}$$

Solving the system leads to

$$\begin{cases} k_L = a - (p_1 + p_2) \\ k_{pI} = (p_1 p_2 + k_L a)/b. \end{cases} \tag{14}$$

For the case $\omega_{nCL} = 2\pi 2400\, rad/s$ and $\xi_{CL} = 0.707$, the poles are located at $p_{1,2} = 0.166 \pm j0.301$ and the bandwidth of the system is $f_{bw} = 3.1\, kHz$. The controller and lead compensator gains are presented in Table III. The resulting root locus with the lead compensator is shown in Fig. 20. The poles locations are more on the left compared to the previous case in Fig. 18, which means the system is faster [13]. Therefore, the proposed technique provides a wider bandwidth for the same damping factor.

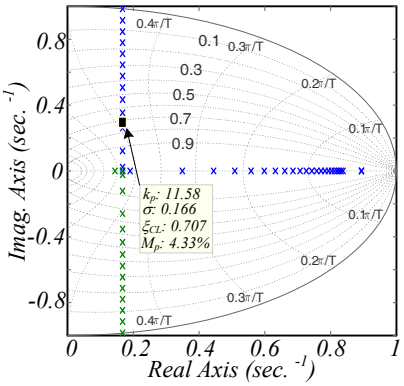


Fig. 20. Root locus of open loop TF in Fig. 19 including the lag introduced by PWM update, with the lead compensator: $k_L = 0.561$.

As shown in Fig. 21, the system with the lead compensator is much more damped around the desired bandwidth.

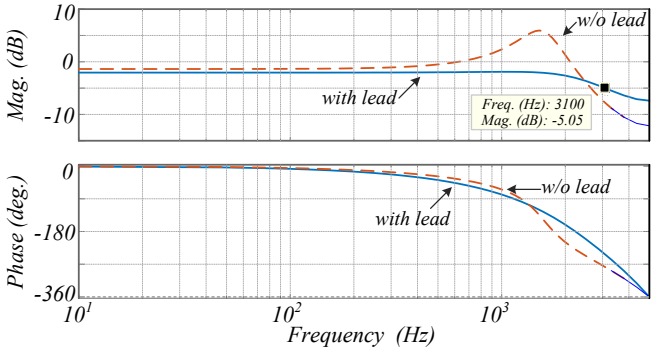


Fig. 21. Frequency response analysis with/without lead compensator, $k_L = 0.561$.

The sensitivity to changes in the plant parameters is investigated. The system is less sensitive to variations of the ESR of the inductor (see Fig. 22) than to changes in the inductance value. The eigenvalue migration as the inductance value changes is shown in Fig. 23.

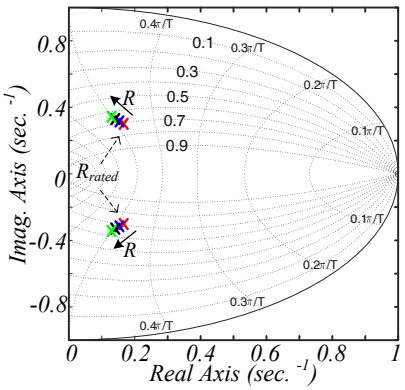


Fig. 22. Eigenvalue migration as a function of variation in $R_{rated} = 0.1\ \Omega \rightarrow R = 2\ \Omega$.

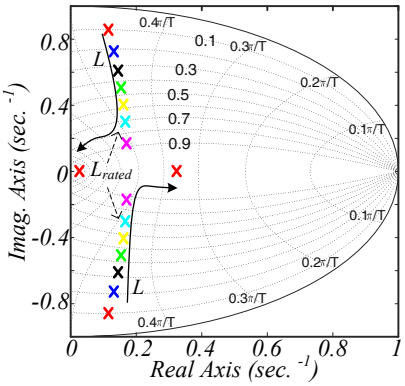


Fig. 23. Eigenvalue migration as a function of variation in $L = 0.9\ mH \rightarrow 2L_{rated} = 3.6\ mH$.

Another technique aimed at widening the bandwidth of the current regulator while still achieving good dynamic properties is based on the Smith Predictor structure [28]. The basic idea is to build a parallel model which cancels the system delay (see Fig. 24). In this way, the design of the controller can be performed using the un-delayed model of the plant. Robustness issues must be considered with this method. If there is any model error, especially in the delay itself, the Smith predictor can degrade the system performance. These aspects are verified in the experiments by changing the predicted values of the plant and computation delay.

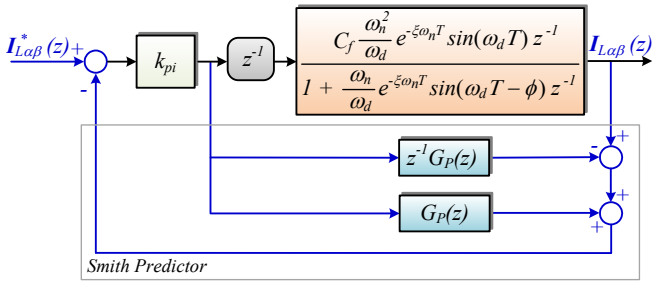


Fig. 24. Block diagram for design the inner current loop, including the lag introduced by computational delay, and the model of the Smith Predictor.

The root locus of the system is shown in Fig. 25. In detail, the closed-loop pole corresponding to $f_{bw} = 3.1\ kHz$ is highlighted and the correspondent gain is reported also in Table II. Since the un-delayed model of the plant is considered, the design is made for a first-order system.

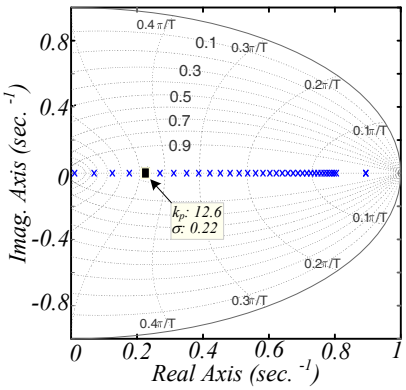


Fig. 25. Root locus of open loop TF in Fig. 24 including the lag introduced by PWM update, with the Smith Predictor.

For the same damping the system response can be made faster than the model with the lead compensator, as can be seen by the step response in Fig. 26.

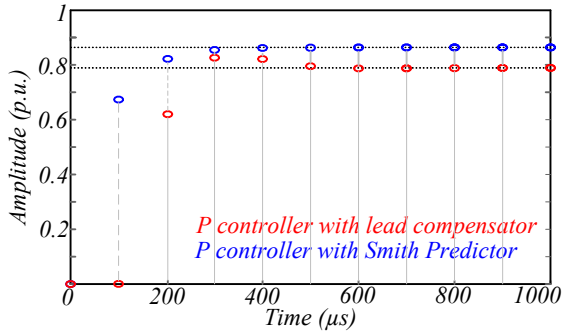


Fig. 26. Step response with the lead compensator ($k_L = 0.561$) and the Smith predictor for $f_{bw} = 3.1\ kHz$.

V. Voltage Regulator Design

The voltage regulator is based on PR controllers with a lead compensator structure. The inner current loop is based on a P controller, e.g. employed in [29], [25], along with Smith Predictor. The addition of resonant filters provides a good steady-state tracking of the fundamental component and mitigates the main harmonics associated to nonlinear loads. The gains of the system are selected to provide also a good dynamic response when the system is tested according to the requirements imposed by the normative for islanded systems. The voltage regulator TF is

$$G_v(s) = k_{pV} + \sum_{h=1,5,7} k_{iV,h} \frac{s\cos(\varphi_h) - h\omega_1 \sin(\varphi_h)}{s^2 + (h\omega_1)^2}. \quad (15)$$

The proportional gain k_{pV} determines the bandwidth of the voltage regulator. In order for the cascaded loops to be effective, the inner current loop time constant should be lower than that of the voltage loop by one fourth up to one tenth [30]. As the effects of the delays are well compensated with the proposed P + Smith predictor for the inner controller, high bandwidth with wide stability margins is achieved. This allows the selection of a low outer over inner bandwidth ratio. According to [30] the minimum ratio is chosen and thus the voltage regulator is designed for around 700 Hz of bandwidth. The phase-leading angles at each harmonic frequency are set such that the trajectories of the open loop system on the

Nyquist diagram, with the PR regulators at fundamental, 5th and 7th harmonics, guarantee a sensitivity peak $1/\eta$ lower than a threshold value [31]. In this work the threshold has been set to $\eta = 0.6$ at no-load condition. After calculating the phase-leading angles, the fundamental resonant gain $k_{iV,1}$ is selected in order to have a fast response to changes in the fundamental component. Equation (15) can be rewritten just for the resonant controller at fundamental, leading to the second-order system

$$G_v(s) = k_{pV}\frac{s^2 + \frac{k_{iV,1}}{k_{pV}}\cos(\varphi_1)s + \left[\omega_1^2 - \frac{k_{iV,1}}{k_{pV}}\omega_1\sin(\varphi_1)\right]}{s^2 + \omega_1^2}. \quad (16)$$

According to Evans root locus theory, the open loop poles move towards the open loop zeros when the loop is closed. For this reason, the pair of zeros of the PR controller in (16) is moved as furthest as possible from the right half plane. This corresponds to the critically damped solution of the numerator equation, such that the pair of zeros of $G_v(s)$ is coincident. As a consequence, $k_{iV,1}$ can be designed according to

$$k_{iV,1} \geq K\frac{2k_{pV}\zeta_{crit}\omega_1}{\cos(\varphi_1)}. \quad (17)$$

Where the lower bound of the inequality refers to $K = 1$, with the damping factor $\zeta_{crit} = 1$. For the phase-leading angle at fundamental frequency $\varphi_1 = 3.3°$, the gain is $k_{iV,1} = 126$. The upper bound is set by $k_{iV,1}$ values which do not significantly degrade the relative stability of the closed-loop system.

The harmonic resonant gains are selected to have reduced transient oscillations [32], as well as to fulfill the requirements set by the IEC 62040 standard for UPS systems (see Table IV)

TABLE IV
VOLTAGE REGULATOR CONTROL PARAMETERS

Parameter		Value	
Proportional gain		$k_{pV} = 0.2$	
Integral gains and lead angles	@50Hz	$k_{iV,1} = 126$	$\varphi_1 = 3.3°$
	@250Hz	$k_{iV,5} = 15$	$\varphi_5 = 37°$
	@350Hz	$k_{iV,7} = 15$	$\varphi_7 = 44°$

In Fig. 27 the Nyquist diagram of the system in Fig. 2 with the parameters of Table III is shown. The inverse of the sensitivity peak, i.e. η, is almost equal to 0.8 at no-load condition with all the harmonic resonators activated. It should be noted the harmonic resonators at 5th and 7th do not intersect the unit circle since the voltage loop bandwidth is set much higher than the highest harmonic order of the resonant filters.

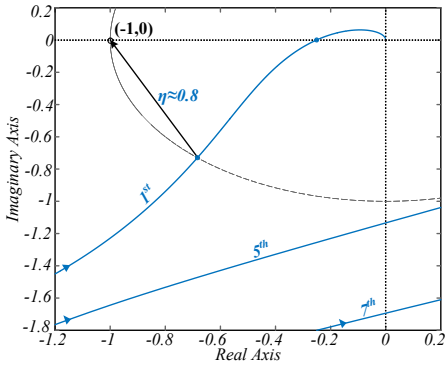


Fig. 27. Nyquist diagram of the system at no-load condition (command tracking of the reference voltage).

A. Anti-wind up scheme

A discrete anti-wind up scheme must be implemented to avoid the saturation of the integral term in the voltage regulator. No anti-wind up scheme is needed for the current loop since a P controller is used as regulator. The anti-wind up scheme, which is based on a feedback implementation of inverse dynamics [33], is shown in Fig. 28 [28].

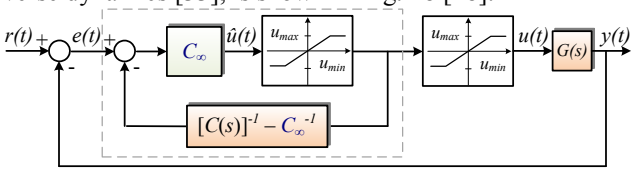


Fig. 28. Anti-wind up scheme based on a feedback implementation of inverse dynamics.

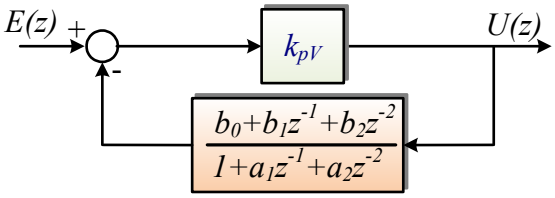


Fig. 29. Anti-wind up implementation in the discrete-time domain during normal operation.

This technique allows the states with bounded signals to be driven in any condition, i.e. also during demanding transients. This represents a major advantage compared to usual anti-wind up implementations, e.g. the frozen scheme [15].

According to [28], the controller $C(s)$ should be: i) biproper, i.e. zero relative degree between the TF numerator and denominator, and ii) minimum phase. If this is the case, the controller can be split into a direct feedthrough term (C_∞) and a strictly proper transfer function $\bar{C}(s)$

$$C(s) = C_\infty + \bar{C}(s). \quad (18)$$

For the particular case of an ideal PR controller

$$C_\infty = k_{pV}; \qquad \bar{C}(s) = k_{iV,1}\frac{s}{s^2 + \omega_o^2}. \quad (19)$$

$$C(s) = k_{pV} + k_{iV,1}\frac{s}{s^2 + \omega_o^2}. \quad (20)$$

In normal operation ($u_{min} < \hat{u}(t) < u_{max}$), the closed-loop TF (within the dotted line in Fig. 28) is equal to $C(s)$. During saturation, the input to the controller states is bounded.

As the anti-wind up scheme is implemented in the discrete-time domain, the following implementation issue, not recognizable in the s-domain, must be considered. In general,

the discrete-time implementation of the feedback path in normal operation (without the saturation block) takes the form in Fig. 29. If $b_0 \neq 0$, an algebraic loop arises, which means that this anti-wind up strategy cannot be implemented in real time. This is directly related to the discretization method used for $\bar{C}(s)$.

A possibility to avoid the algebraic loop can be to use as discretization methods Zero-Order Hold (ZOH), Forward Euler (FE) or Zero-Pole Matching (ZPM), which assure $b_0 = 0$. As an example, the TF in the feedback path in Fig. 28 takes the form in Table V for ZPM and Impulse Invariant. This latter cannot be used otherwise an algebraic loop arises, even though it is usually recommended for direct implementations [7].

TABLE V
DISCRETIZATION OF THE FEEDBACK PATH IN THE ANTI-WIND UP SCHEME OF FIG. 28

Method	Value
Impulse Invariant	$\frac{-\frac{k_{iV,1}}{k_{pV}}T_s\cos(\varphi_1)+\frac{k_{iV,1}}{k_{pV}}T_s\cos(\varphi_1-\omega_1T_s)z^{-1}}{[k_{pV}+k_{iV,1}T_s\cos(\varphi_1)]-[2k_{pV}\cos(\omega_1T_s)+k_{iV,1}T_s\cos(\varphi_1-\omega_1T_s)]z^{-1}+k_{pV}z^{-2}}$
Zero-Pole Matching	$\frac{-\frac{k_{iV,1}}{k_{pV}}K_dz^{-1}+\frac{k_{iV,1}}{k_{pV}}K_de^{\tan(\varphi_1)\omega_1T_s}z^{-2}}{k_{pV}-[2k_{pV}\cos(\omega_1T_s)-k_{iV,1}K_d]z^{-1}+[k_{pV}-k_{iV,1}K_de^{\tan(\varphi_1)\omega_1T_s}]z^{-2}}$

In case FE is used as discretization method, the performance of the voltage controller is degraded since zero steady-state error is not achieved [7]. This can be seen in Fig. 30, where the frequency response of the controller discretized with these methods is shown. The gain at the resonant frequency is no more infinite if FE is used as discretization method.

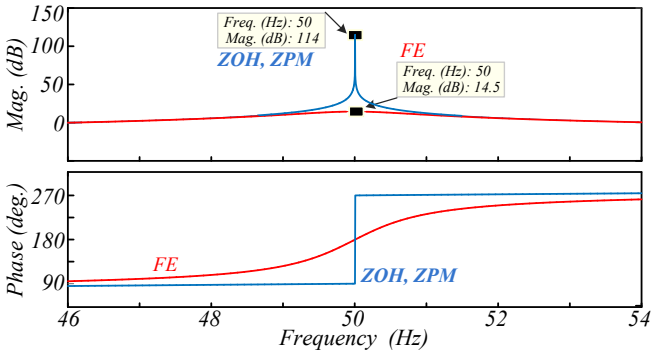


Fig. 30. Frequency response of the resonant controller using ZOH, ZPM and FE.

The resulting implementation with ZOH or ZPM avoids wind-up after saturation and algebraic loops, without losing any basic feature of the PR control during normal operation.

Moreover, in order to get an even more damped step response during transients [5], which corresponds to a lower gain at the resonant frequency, the following implementation is proposed. Firstly, the coefficients a_1 and a_2 are determined by discretization of $[C(s)^{-1} - k_p^{-1}]$, using ZOH for discretization in order to get an implementation which avoids algebraic loops. Then, the closed-loop TF of the system in Fig. 29 is derived

$$\frac{U(z)}{E(z)} = \frac{k_{pV}(1 + a_1z^{-1} + a_2z^{-2})}{1 + (a_1 + b_1k_{pV})z^{-1} + (a_2 + b_2k_{pV})z^{-2}}. \quad (21)$$

After discretization, some errors arise at the resonant frequency. For this reason, the b_1 and b_2 coefficients should be re-calculated such that the inverse dynamics implementation matches the desired resonant frequency

$$(a_1 + b_1k_{pV}) = -2\cos(\omega_1T_s)\,;\ (a_2 + b_2k_{pV}) = 1. \quad (22)$$

This implementation provides zero steady-state error and a damped response after transients.

In the next section, the robustness of the controllers designed is verified via extensive experimental results performing step responses and step load changes with resistive and nonlinear loads.

VI. EXPERIMENTAL RESULTS

The power system of Fig. 1 was tested to check the theoretical analysis presented. For this purpose, a low scale test-bed has been built using a Danfoss 2.2 kW converter, driven by a dSpace DS1006 platform. The LC filter parameters and operational information are presented in Table II. In all the tests voltage decoupling is performed as shown in Fig. 2.

In order to compare the current loop performance with/without lead compensator schemes and Smith Predictor in terms of dynamic response, a step change of the inductor current is performed. In order to achieve approximately zero steady-state error with different control structures, the reference is multiplied by a constant, which is equivalent to multiply by a gain the closed-loop TF of the inductor current. It should be noted that the dynamics of the system with the current loop only, i.e. voltage loop disabled and the current reference is generated manually, are not affected by this gain, which is also significantly lower as the bandwidth is widened. For the case with the proportional gain only (see Fig. 17), the step response is degraded as k_{pI} is increased [see Fig. 31(a) and Fig. 31(b)]. This result also shows that due to additional losses the setup has more damping than expected. In Fig. 31(b) the step response is even less damped and more oscillatory for $k_{pI} = 11.58$. It is clear that there is a limitation in the achievable bandwidth due to the system delays.

If the control structure with a lead compensator is used (see Fig. 19), the bandwidth can be widened in comparison to the case with just a P controller for the same k_{pI} value, without degrading the dynamic performance. The step response for $f_{bw} = 3.1$ kHz, to which corresponds $k_{pI} = 11.58$, is less oscillatory than the result in Fig. 31(b), as shown in Fig. 32(a). The step response is even faster if the Smith predictor, designed for the same bandwidth, is used to perform the test [see Fig. 32(b)]. The main reason is due to the fact that the Smith predictor produces a system similar to a first order one. These results are in accordance with the step responses shown in Section IV in Fig. 26.

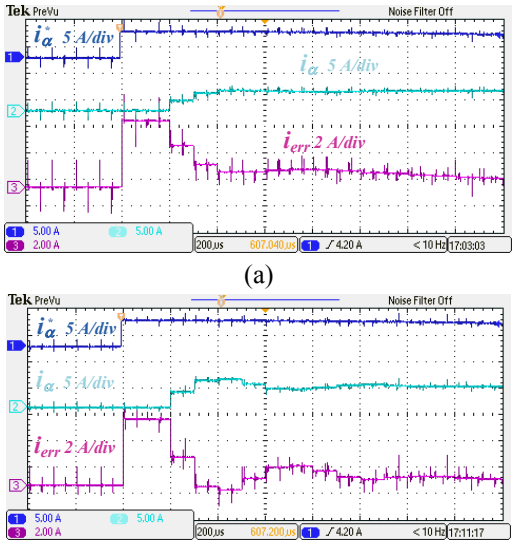


Fig. 31. Step response, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis), time scale (200 µs/div): (a) P controller, $k_{pI} = 5.54$; (b) P controller, $k_{pI} = 11.58$.

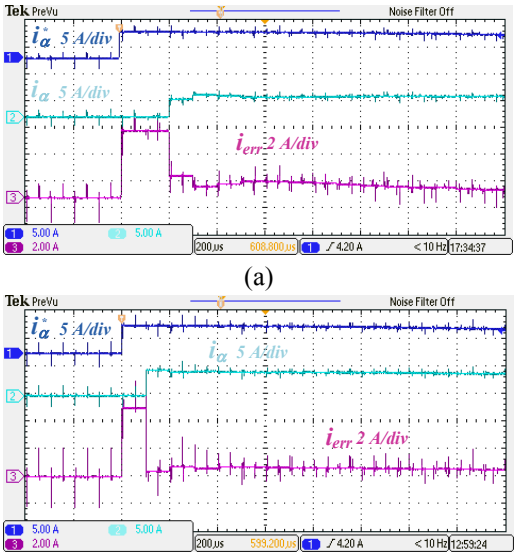


Fig. 32. Step response, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis), time scale (200 µs/div): (a) P controller + lead compensator, $k_{pI} = 11.58$, $k_L = 0.561$; (b) P controller + Smith Predictor, $k_{pI} = 12.6$.

The sensitivity to changes in the predicted parameters values is verified. For this purpose, the predicted inductor value L_{SP} is set twice than the rated value [see Fig. 33(a)]. The predicted ESR of the inductor R_{SP} is increased by ten times [see Fig. 33(b)]. The Smith Predictor is almost insensitive to changes in R_{SP}, while is more dependent on L_{SP}. Nevertheless, even with huge variations in these parameters, the step response has an acceptable behavior. The predicted computation delay T_{dSP} is changed to $0.5T_s$ and $2T_s$, as can be seen in Fig. 33(c) and Fig. 33(d). The system becomes more oscillatory during transients, in particular if T_{dSP} is higher than the real computation delay.

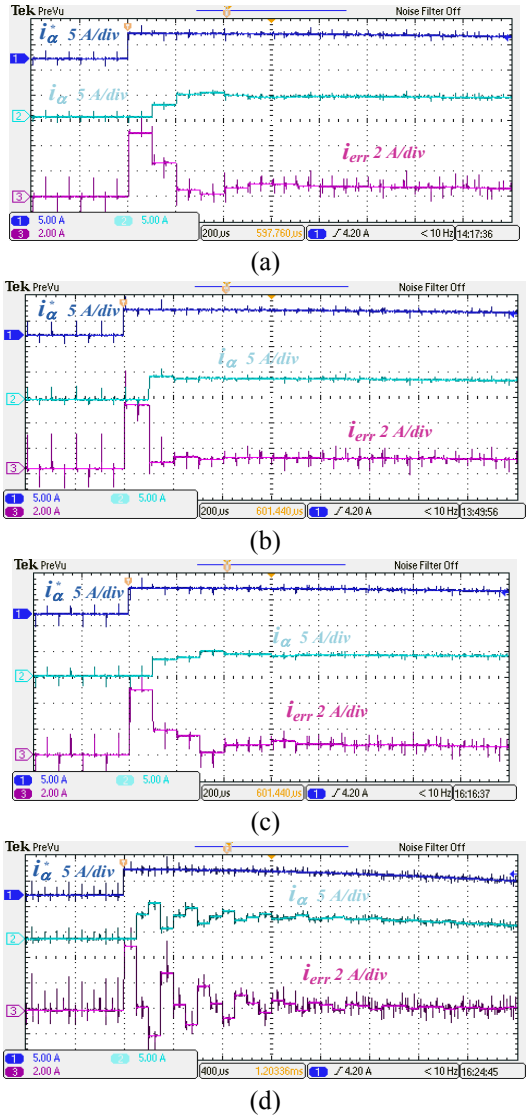


Fig. 33. Sensitivity analysis on predicted plant values for the Smith predictor - reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis), time scale (200 µs/div): (a) $L_{SP} = 1.2L_{SP,rated}$; (b) $R_{SP} = 10R_{SP,rated}$; (c) $T_{d,SP} = 0.5T_{d,SP,rated}$; (d) $T_{d,SP} = 2T_{d,SP,rated}$.

A P controller with Smith Predictor is chosen because computation and PWM delays are well-known deterministic parameters in this application and hence, it can be concluded that this current controller is feasible to be used as inner current loop. For this reason all the following results (from Fig. 34 to Fig. 38) regarding the voltage loop are obtained with voltage decoupling, P + Smith Predictor as current regulator and the anti-wind up scheme proposed in the previous section. The parameters of the system are presented in Table II. In Fig. 34(a) a 100% linear step load change is shown, using just the regulator at the fundamental frequency. The results obtained are compared to the envelope of the voltage deviation v_{dev} as reported in the IEC 62040 standard for UPS systems [see Fig. 34(b)]. It can be seen that the system reaches steady-state in less than half a cycle after the load step change. The dynamic response is within the limits imposed by the standard. Moreover, the dynamics of the inductor current in α-axis are shown in Fig. 34(c). These last data have been recorded in dSpace ControlDesk scopes and then plotted in Matlab. Since

the capacitor voltage is sinusoidal, the inductor current is slightly distorted even in case a linear load is supplied.

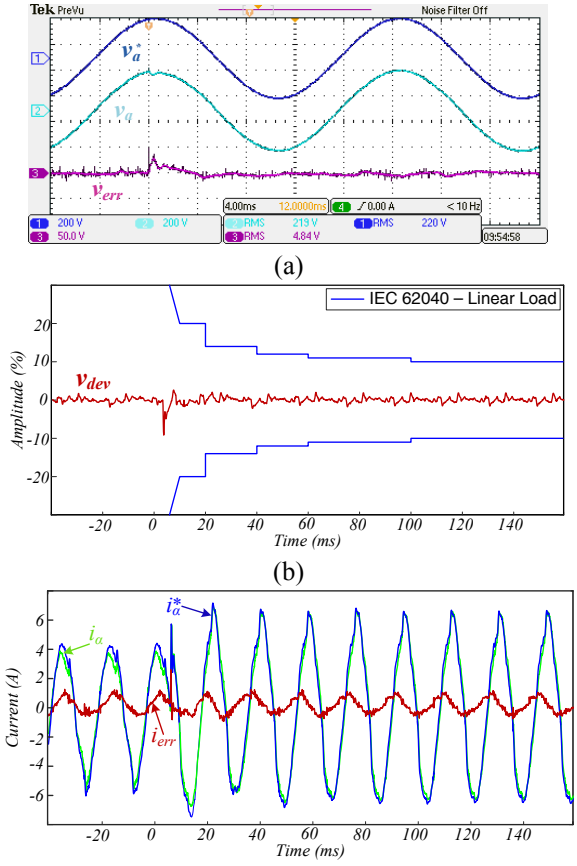
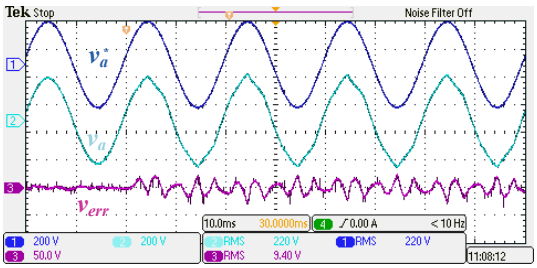


Fig. 34. Linear step load changing (0 – 100%): (a) reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (4 ms/div); (b) Dynamic characteristics according to IEC 62040 standard for linear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$); (c) reference, real and inductor current error (α-axis).

A diode bridge rectifier with an LC output filter supplying a resistive load is used as nonlinear load. Its parameters are presented in Table II. A 100% nonlinear step load change is performed with and without the harmonic compensators (HC) tuned at the 5th and 7th harmonics. The results are in accordance with the standard IEC 62040 even for linear loads, as can be seen in Fig. 35(b) and Fig. 36(b). The correspondent inductor current in α-axis for the test performed without HC is shown in Fig. 35(c). A similar trend for the inductor current is achieved with the HC activated. It is evident in Fig. 36(b) that the benefits of using the harmonic compensators are in a lower the steady-state error



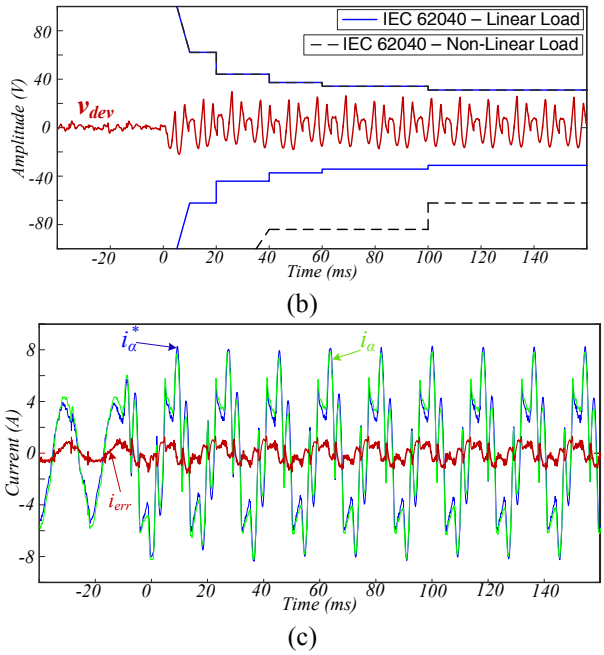


Fig. 35. Nonlinear step load changing (0 – 100%) without HC: (a) reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (10 ms/div); (b) Dynamic characteristics according to IEC 62040 standard for linear and nonlinear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$); (c) reference, real and inductor current error (α-axis).

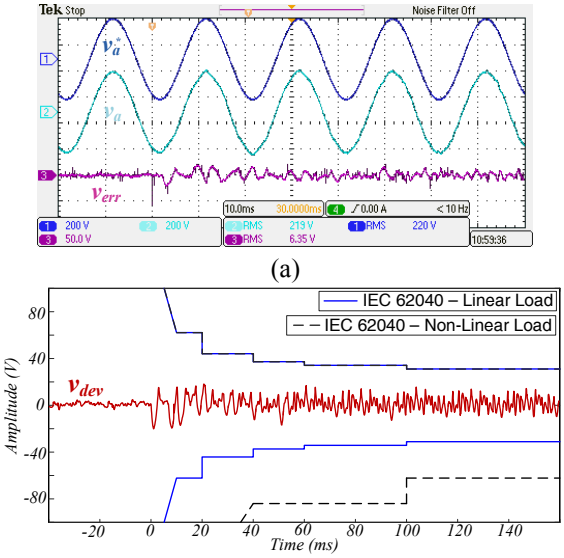
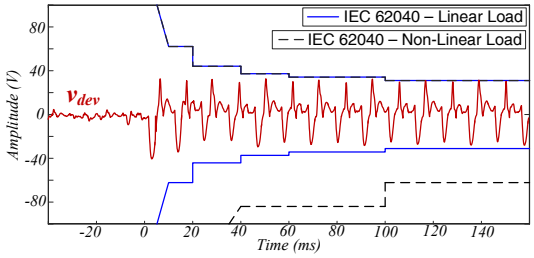


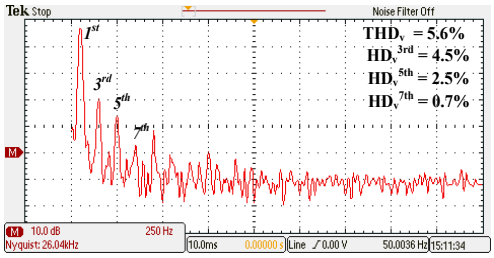
Fig. 36. Nonlinear step load changing (0 – 100%) with HC at 5th and 7th harmonics: (a) reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (10 ms/div); (b) Dynamic characteristics according to IEC 62040 standard for linear and nonlinear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$).

To verify the attenuation of triplen harmonics, a 100% nonlinear unbalance (one phase open) step load change is performed, using the harmonic compensator at the fundamental frequency only. The response is again in the boundaries imposed to linear loads [see Fig. 37(a)]. The FFT results in Fig. 37(b) show the mitigation of the 3rd harmonic component by a large extent, even with just the resonator tuned at the fundamental frequency. These results show the benefits of widening the bandwidth for the voltage loop, which can be

achieved with the design of the inner current loop based on Smith predictor.



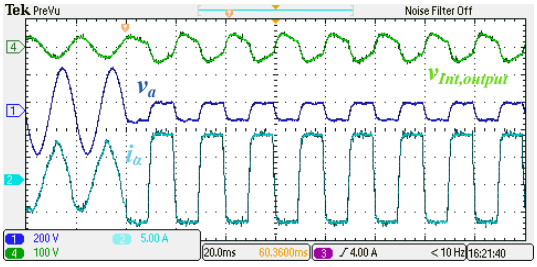
(a)



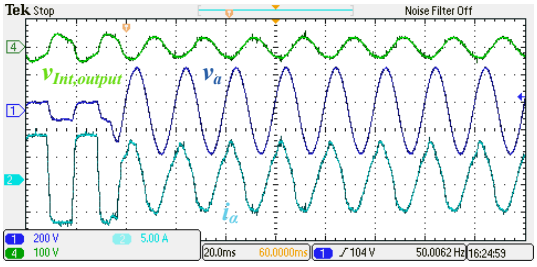
(b)

Fig. 37. Unbalance nonlinear step load changing (0 – 100%): (a) Dynamic characteristics according to IEC 62040 standard for linear and nonlinear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$) without HC; (b) FFT of the capacitor voltage.

In order to show the performance of the anti-wind up implementation, a saturated control action (current reference) along with results of a step change from rated load to overload conditions and vice versa are shown in Fig. 38(a) and Fig. 38(b). The current limiter is set to 8 A as well as the saturation blocks in the anti-wind up scheme. It can be noted the output of the integral is bounded because of the anti-wind up scheme implemented.



(a)



(b)

Fig. 38. Linear step load changing (100% - 950% and viceversa) - integral output (100 V/div), real capacitor voltage (200 V/div) and real inductor current (5 A/div) (α-axis), time scale (20 ms/div): (a) from rated load (68 Ω) to overload conditions (7.2 Ω); (b) from overload conditions (7.2 Ω) to rated load (68 Ω).

VII. Conclusions

Recent approaches in the control of power converters working in standalone applications have proved that state-feedback decoupling allows better dynamic response to be achieved. In this context, the model derived directly in the discrete-time domain permits a clear representation of the limitations in dynamics introduced by computation and PWM delays when state feedback voltage decoupling is performed. The simulation results validate the discrete-time model developed, which allows access to the internal states of the system. In order to enhance the current controller dynamics, a P controller with a lead compensator and Smith Predictor structure are implemented and compared. The implementation based on Smith Predictor has been shown to provide the fastest response to changes in the reference inductor current, allowing the current loop bandwidth to be widened while still preserving good dynamic properties. The wider inner current control bandwidth permits the bandwidth of the voltage loop to be increased. A systematic design methodology based on the Nyquist criterion allows the fundamental integral gain value to be identified by means of a straightforward mathematical relationship. As the dynamics of the voltage loop are faster, an anti-wind up scheme becomes even more important. The proposed design in the discrete-time domain of the anti-wind up scheme based on a feedback implementation of inverse dynamics avoids algebraic loops, which could arise depending on the discretization method employed.

The overall design provides good performance both in steady-state and transient conditions. More specifically, the requirements during the transient, imposed by the UPS standard IEC 62040, are verified according to the design proposed for the current and voltage regulators. Moreover, when a balanced or even unbalanced nonlinear load is supplied, the dynamic response is within the standards imposed to linear loads with just the compensator tuned at fundamental frequency.

Appendix

In this section the derivation of the first Cross-Coupled State Equation is provided, following the step-by-step methodology provided in Section II. Moreover, the derivation of the transfer function $\boldsymbol{V}_{C\alpha\beta}(z)/\boldsymbol{I}_{L\alpha\beta}(z)$ is provided.

Eq. (6) is derived as follows. Firstly, the Inverse Laplace Transform applied to (3) leads to

$$\begin{aligned} v_c(t) = &\left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t}\sin(\omega_d t + \phi)\right] v_i(t=0) \\ &+ \frac{v_c(t=0)}{\omega_n^2}\frac{-\omega_n^2}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t}\sin(\omega_d t - \phi) \\ &+ \frac{2\xi}{\omega_n} v_c(t=0)\frac{\omega_n}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t}\sin(\omega_d t) \\ &+ \frac{\dot{v}_c(t=0)}{\omega_n^2}\frac{\omega_n}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t}\sin(\omega_d t). \end{aligned} \tag{A.1}$$

Accordingly, the response in the next sample time is

$$\begin{aligned} v_c(T) = &\left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n T}\sin(\omega_d T + \phi)\right] v_i(t=0) \\ &- \frac{\omega_n}{\omega_d} e^{-\xi\omega_n t}\sin(\omega_d T - \phi) v_c(t=0) \\ &+ \frac{2\xi\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) v_c(t=0) \\ &+ \frac{1}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T)\dot{v}_c(t=0). \end{aligned} \tag{A.2}$$

The solution at a generic sample instant is

$$\begin{aligned} v_c(kT) = &\left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n T}\sin(\omega_d T + \phi)\right] v_i\big((k-1)T\big) \\ &- \frac{\omega_n}{\omega_d} e^{-\xi\omega_n t}\sin(\omega_d T - \phi) v_c\big((k-1)T\big) \\ &+ \frac{2\xi\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) v_c\big((k-1)T\big) \\ &+ \frac{1}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T)\dot{v}_c\big((k-1)T\big). \end{aligned} \tag{A.3}$$

This equation cannot be written in transfer function format due to the term $\dot{v}_c\big((k-1)T\big)$. However, being $\dot{v}_c\big((k-1)T\big) = \frac{1}{C_f} i_L\big((k-1)T\big)$, this model with cross-coupling can be written as

$$\begin{aligned} v_c(kT) = &\left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n T}\sin(\omega_d T + \phi)\right] v_i\big((k-1)T\big) \\ &- \frac{\omega_n}{\omega_d} e^{-\xi\omega_n t}\sin(\omega_d T - \phi) v_c\big((k-1)T\big) \\ &+ \frac{2\xi\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) v_c\big((k-1)T\big) \\ &+ \frac{1}{C_f\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) i_L\big((k-1)T\big). \end{aligned} \tag{A.4}$$

By substituting for the z operator in the discrete-time domain and by transforming to the αβ stationary reference frame leads to

$$\begin{aligned} \boldsymbol{V}_{c\alpha\beta}(z)&\left[1 + \frac{\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T - \phi) z^{-1} - \frac{2\xi\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) z^{-1}\right] \\ &= \left[1 - \frac{\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T + \phi)\right] \boldsymbol{V}_{i\alpha\beta}(z) z^{-1} \\ &+ \frac{1}{C_f\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T)\, \boldsymbol{I}_{L\alpha\beta}(z). \end{aligned} \tag{A.5}$$

A similar mathematical development can be performed to derive (7), starting from (4). Solving the coupling equations (6) and (7), yields to the independent TF

$$\frac{\boldsymbol{V}_{c\alpha\beta}(z)}{\boldsymbol{V}_{i\alpha\beta}(z)} = \frac{a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \tag{A.6}$$

where

$$a_1 = 1 - \frac{\xi\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) - e^{-\xi\omega_n T}\cos(\omega_d T)$$

$$a_2 = \frac{\xi\omega_n}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T) - e^{-\xi\omega_n T}\cos(\omega_d T) + e^{-2\xi\omega_n T}$$

$$b_1 = -2e^{-\xi\omega_n T}\cos(\omega_d T);\; b_2 = e^{-2\xi\omega_n T}$$

Similarly, starting from (6) we can achieve the transfer function $\boldsymbol{I}_{L\alpha\beta}(z)/\boldsymbol{V}_{i\alpha\beta}(z)$ already including the output voltage feedback, i.e. $\boldsymbol{V}_{c\alpha\beta}(z)$

$$\frac{\boldsymbol{I}_{L\alpha\beta}(z)}{\boldsymbol{V}_{i\alpha\beta}(z)} = \frac{\left[C_f \frac{\omega_n^2}{\omega_d} e^{-\xi\omega_n T}\sin(\omega_d T)\right](z^{-1} - z^{-2})}{1 - 2e^{-\xi\omega_n T}\cos(\omega_d T)\, z^{-1} + e^{-2\xi\omega_n T} z^{-2}}. \tag{A.7}$$

The derivation of (A.7) is necessary to obtain the transfer function $\boldsymbol{V}_{c\alpha\beta}(z)/\boldsymbol{I}_{L\alpha\beta}(z)$. In fact, by considering (A.6) and (A.7), the relationship between $\boldsymbol{I}_{L\alpha\beta}(z)$ and $\boldsymbol{V}_{c\alpha\beta}(z)$ can be derived as

$$\frac{\boldsymbol{V}_{c\alpha\beta}(z)}{\boldsymbol{I}_{L\alpha\beta}(z)} = \frac{\boldsymbol{V}_{c\alpha\beta}(z)}{\boldsymbol{V}_{i\alpha\beta}(z)} \cdot \frac{\boldsymbol{V}_{i\alpha\beta}(z)}{\boldsymbol{I}_{L\alpha\beta}(z)}. \tag{A.8}$$

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