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Multilevel Modular Converter for VSC-HVDC Transmission Applications: Control and Operational Aspects

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Abstract— Control methods for a new class of converter, the multilevel modular converter (MMC), recently introduced for HVDC transmission are discussed. The paper discusses converter-level controls including firing pulse generation and capacitor voltage balancing. It also covers higher level controls for incorporating the converter into a larger power network, with a weak ac receiving end. The performance behavior is studied using electromagnetic transients simulation.

Keywords— Voltage Source Convert (VSC), Multilevel Modular Converter (MMC), HVDC Transmission, Weak ac networks

I. INTRODUCTION

Voltage sourced converter (VSC) based HVDC systems exhibit many attractive features over the conventional line commutated converter (LCC) based systems in high voltage high power applications [1]. These unique features such as independent control of active and reactive power [2], operation in weak ac systems [3], black start capability [4], and multi terminal connection [5] have led to their increased adoption in modern schemes. Till recently, two-level or three-level VSC topologies were used for HVDC transmission applications, with pulse-width modulation (PWM) control to reduce the lower harmonic content. The ratings were typically limited to below 400 MW because of the higher switching losses inherent in such topologies.

Numerous multilevel topologies and modulation strategies have been introduced for machine drive applications [6]–[8]. Diode clamped multilevel converters [6] [7] synthesize a stepped ac waveform resembling a sine wave, by stacking fixed magnitude voltage steps on top of each other. This topology typically has lower losses than two level PWM converters. However, the number of levels has been limited to 3 (in HVDC applications) due to the circuit complexity. Also capacitor voltage balancing is a critical and challenging issue.

The recently initiated modular multilevel converter (MMC) is a major step forward in VSC converter technology for HVDC transmission [9]. This topology is designed to make lower switching frequency, avoid connecting the devices in series. The modular structure easily scales to higher voltage

and power levels, with the addition of more modules. A power rating of 1 GW and above now becomes possible. Although the MMC topology has been presented in earlier literature [9], [10], the discussion on control methods is sparse. This paper discusses control approaches and investigates their performance using electromagnetic transients (EMT) simulation. The paper also investigates the control and performance of a HVDC transmission scheme feeding to a weak ac system.

II. MODULAR MULTILEVEL CONVERTER TOPOLOGY

A. Circuit Structure of Modular Multilevel Converter

The basic building block of the MMC converter is the sub-module shown in Fig. 1, which consists of two IGBT switches T_1 and T_2 and a capacitor C . In normal operation, exactly one switch (T_1 or T_2) is ON at any instant, giving a sub-module output voltage of V_c or 0 (1):

$$V_{OUT}(t) = \begin{cases} V_c & T_1\text{-ON, } T_2\text{-OFF} \\ 0 & T_1\text{-OFF, } T_2\text{-ON} \end{cases} \quad (1)$$

When the sub-module voltage is V_c , it is said to be in the ‘ON’ state, and when it is zero, it is considered to be ‘OFF’.

B. Output Voltage Waveform Synthesis

The single phase block diagram of the MMC (modular multi-level converter) is shown in Fig. 2. The MMC phase includes upper and lower multi-valves, each with a number (N) of sub-modules (SM_j). The number N is chosen based on the dc voltage rating (V_d) and individual sub-module rating (V_c).

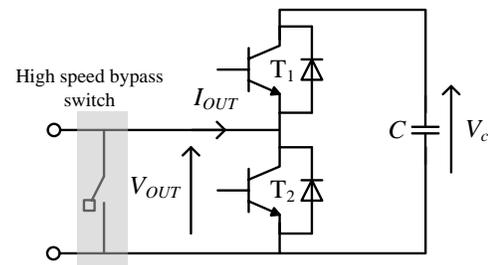


Fig. 1. Sub-module of MMC converter

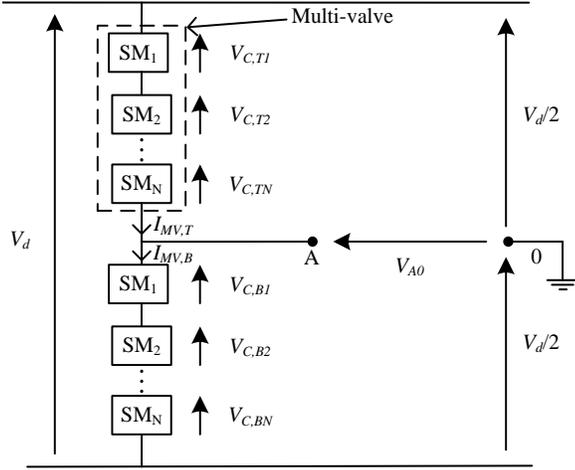


Fig. 2. Phase module of an MMC scheme for an N-level arrangement

Thus, this modular structure can be scaled for different voltage and power levels [9]. By controlling the ON/OFF state of the sub-modules, the output voltage waveform, V_{A0} , can be synthesized to track a given sinusoidal voltage reference V_{ref} as shown in Fig. 3.

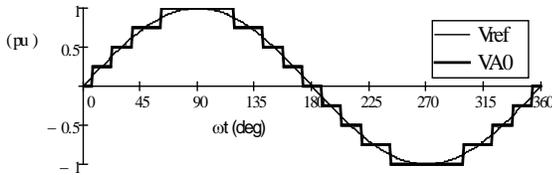


Fig. 3: Reference and output waveforms for MMC with 8 sub-modules per multi-valve

The reference V_{ref} is compared with ' N ' discrete equidistant quantization thresholds (see Fig.4, top left). The number of sub-modules N_U and N_L required to be 'ON' in the upper and lower multi-valves respectively is thus determined as:

$$\begin{aligned} N_L &= \text{round}(V_{ref} N) \\ N_U &= N - N_L \end{aligned} \quad (2)$$

Here it is assumed that V_{ref} is 1, when output voltage is at its maximum possible value of $V_d/2$. With the above waveform synthesis method at any given instant, the full dc bus voltage appears across $N_U + N_L = N$ sub-modules [9]. Hence, since all capacitor voltages are required to be the same, each must be equal to:

$$V_c = V_d / N \quad (3)$$

C. Redundant Sub-modules

Redundant sub-modules are provided in each multi-valve. If a sub-module fails during operation, it is quickly removed from the circuit by operating the high-speed bypass switch [11] shown in Fig. 1. Normal operation can continue with the remaining sub-modules in the multi-valve. The waveform synthesis algorithm discussed in the previous sub-section is informed of the failure and now only controls the remaining

sub-modules in the multi-valve. The capacitor voltages on the remaining sub-modules (and hence the step height of the waveform) is now slightly larger as the number of sub-modules available for generating the waveform is reduced.

D. Capacitor Voltage Balancing

In Fig. 1, with T_1 ON and T_2 OFF, the capacitor voltage increases or decreases depending on the direction of sub-module current I_{OUT} being positive or negative. The capacitor voltage remains unchanged with T_2 ON and T_1 OFF. Hence, during the operation, the 'OFF' sub-modules maintain constant capacitor voltages, whereas the 'ON' sub-modules experience an increase or decrease of their capacitor voltages. Hence a capacitor voltage balancing algorithm is required. Note that the output waveform synthesis algorithm merely states that N_U and N_L sub-modules are 'ON' in the upper and lower multi-valves. Assuming all sub-module capacitors to have equal voltages provides a measure of freedom in selecting the individual 'ON' state sub-modules, which are utilized in the capacitor voltage balancing algorithm described below.

The function of this capacitor balancing algorithm is to generate firing pulses for each sub-module in a multi-valve by maintaining the sub-module's capacitor voltages at a value, given by equation (3). A table is created in which the capacitors are ranked in order of increasing dc voltages. The table is consulted when the quantization algorithm demands a step change (i.e. change in N_U and N_L).

Consider the upper multi-valve which requires N_U sub-modules to be ON. If the current I_{OUT} is positive (see Fig. 1), then turning on a sub-module will result in capacitor voltage increase. In that case, the N_U sub-modules ranked lowest in voltage are turned on, so that they can be re-charged. If I_{OUT} is negative, then the highest-voltage sub-modules are turned on, so that their voltages may discharge. The same is done for the lower multi-valve.

The capacitor voltages of sub-modules can be controlled in a narrow band by applying this methodology for all three phases [10]. The overall control structure for the converter, including the waveform quantizer and the capacitor balancing controller is shown schematically in Fig. 4.

III. OPERATIONAL ASPECTS OF MMC CONVERTER

A detailed model of the single phase MMC converter was developed in the electro-magnetic transient's simulation program PSCAD/EMTDC.

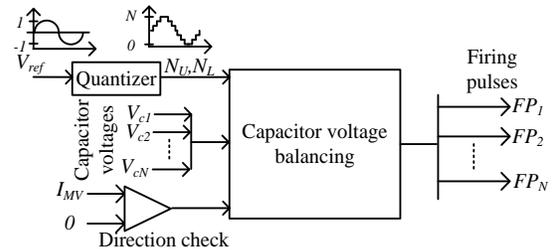


Fig. 4. Firing pulse control algorithm of MMC

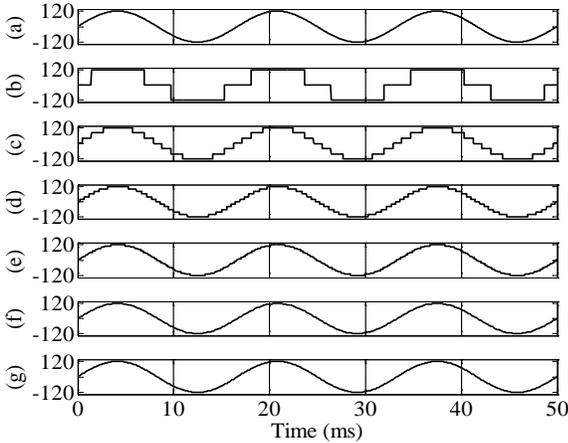


Fig. 5. a) Sinusoidal reference waveform and converter output voltage waveforms when number of sub-modules per multi-valve is; b) 2, c) 6, d) 12, e) 24, f) 48, and g) 96

A. Multi-level AC Waveform of MMC

The output voltage waveforms obtained for different number of sub-modules in a phase unit are presented in Fig. 5. In these simulations, the dc bus voltage (pole-pole) is $V_d = 240\text{kV}$.

Fig. 5(a) shows the reference sinusoidal waveform, and each subsequent graph shows the waveform attained with increasing number of sub-modules ranging from 2 to 96. The sub-module capacitance was set to a high value so that the change of capacitor voltage in a conduction interval is negligible. As the number of sub-modules is increased, the steps become smaller, and the waveform becomes closer to that of the reference sine wave.

Standard IEEE 519 recommends two indices for voltage distortion [12]. The individual harmonic distortion D_n is the magnitude of the n th harmonic as a percentage of the fundamental. The total harmonic distortion is the root mean square of all harmonics expressed as a percentage of the fundamental. A commonly used limit for these in HVDC systems is D_n less than 1% for each harmonic, and THD less than 2%, considering all harmonics up to the 50th. Fig. 6 shows the maximum D_n and THD values for an ideal MMC waveform, with the above thresholds indicated, as the number of sub-modules per multi-valve is increased. It is quite clear that with more than 22 sub-modules per multi-valve, all harmonic limits are satisfied. The MMC with this number of sub-modules can therefore be operated without any ac filters, which is a significant advantage. Actual MMC installations use a larger number of modules, because they operate at high dc voltages, and the additional modules reduce the voltage stress per module.

B. Performance of Capacitor Voltage Balancing Controller

In this section, the performance of capacitor balancing controller, as described in section II-D, is presented by disabling and enabling the control operation for different time intervals. First, the controller was disabled at 0.5 s. Capacitor voltages start to diverge from their nominal value. The

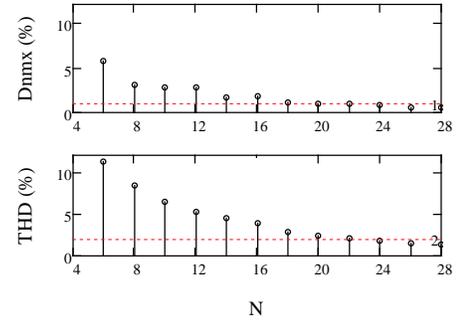


Fig. 6. Max. individual harmonic and THD variations with no. of levels

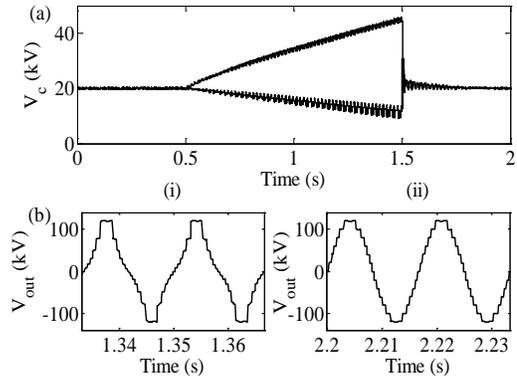


Fig. 7. a) Capacitor voltages in 2 candidate sub-modules showing effect of enabling/disabling voltage balancing control. b) MMC output voltage (i) without and (ii) with voltage balancing in operation.

capacitor voltages of two sub-modules that show the widest deviations are shown Fig. 7 (a). These deviations are caused by the different capacitor conduction (charging or discharging) intervals which depend on the sub-module's duty cycle. The sub-modules having the longest ON period either overcharge or undercharge based on the current direction.

However, when the balancing controller is re-enabled at 1.5s, the capacitor voltages were quickly restored to their nominal values. The corresponding converter output voltage waveforms around the 1.33s mark with capacitor voltage balancing disabled, and at the 2.2s mark with voltage balancing enabled are shown in Fig. 5 (b). In this simulation, there are 12 sub-modules in a multi-valve. The above results show that the voltage balancing controller is rapidly able to equalize the capacitor voltages.

C. Impact of Capacitor Size on Performance

A smaller size for the sub-module capacitance results in more dc-side ripple voltage. If the ripple is too large, it can distort the ac side voltage waveform significantly. Fig. 8 shows the variation of a typical sub-module capacitor voltage depending on the size of capacitance used. In order to per-unitize the capacitor size, it is customary to express it in the form of the total capacitor energy stored at rated dc voltage for all capacitors in the converter, to the complex power rating of the converter as shown in (4).

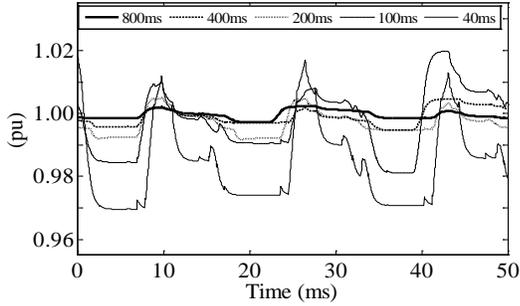


Fig. 8. Average capacitor voltage fluctuation for different capacitance values of 6-level MMC

$$C_{pu} = \frac{(0.5CV_c^2)(6N)}{\sqrt{P_c^2 + Q_c^2}} \quad (4)$$

Here C is the sub-module capacitance, V_c , its voltage, P_c and Q_c , the converter's rated real and reactive powers, and N the number of sub-modules. The number 6 in (4) arises from the fact that there are 6 multi-valves with N sub-modules per valve. With this definition, the unit of C_{pu} is the second.

The resulting ac output voltage for different sub-module capacitance values (from 8 ms to 800 ms) for a 6-level MMC is shown in Fig. 9. For a capacitance value 80 ms or larger (Fig. 9(a to e)), the waveform is essentially the same. However, capacitance values smaller than 80 ms (e.g. Fig. 9(f and g)) introduce distortion. These results show that the MMC capacitor should be larger than 80ms.

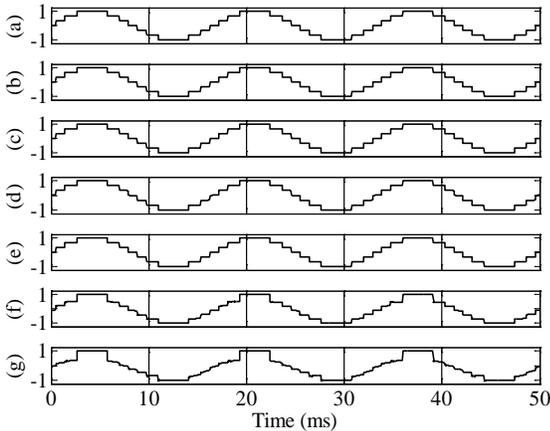


Fig. 9. Converter output voltage waveforms for different capacitance values; a) 800 ms, b) 400 ms, c) 200 ms, d) 100 ms, e) 80 ms, f) 40 ms, g) 8 ms

IV. CHALLENGES IN MODELLING MMC

In the MMC, the number of sub-modules is very large. Each of the N sub-modules of the 6 multi-valves in a three phase MMC contains 2 switch elements, giving a total of 12 N switches per converter. With 100 sub-modules, this gives 1200 switches per converter. Systems of this size pose a significant computational burden in terms of CPU time to electromagnetic

transient (EMT) programs.

To overcome this computational effort of MMC simulation in EMT simulation programs, a recently introduced model based on the Nested Fast and Simultaneous Solution [13] approach was used [14]. This method represents the converter power electronics as a time-varying Thévenin's equivalent that is able to maintain the same level of accuracy as brute-force EMT simulation, but with much reduced computation time. Unlike averaged models [15], the model used here is still able to represent individual sub-module details, and can simulate phenomena such as sub-module failure or capacitor voltage balancing.

V. SIMULATION OF A MMC BASED HVDC SYSTEM

In this section, a point to point MMC based HVDC transmission system; feeding to a weak ac network has been simulated. The dc link is connected to the two ac systems. The sending end ac system has a short circuit ratio (SCR) of 2.5, and is relatively strong. The receiving end system is weak, with an SCR of 1.0. The simulated system is schematically shown in Fig. 10. In the simulation, MMC1 acts as the rectifier and MMC2 acts as the inverter. The dc system is rated at 400MW, ± 200 kV. Each MMC has 100 sub-modules in a multi-valve; hence the sub-modules were rated at 4.0kV.

As there is a total of 2400 switches in the two converters, it is practically impossible to model the converters using the traditional approach using individual switches in EMT programs. Therefore, computationally fast model discussed in section IV, was used for modelling the system [14].

A. HVDC System Controls

The direct control strategy [16] was selected for the higher level controllers of the system. The controllers output the desired phase shift angle δ and the magnitude M of the reference signal (V_{ref}). The reference for measuring the angle δ is the ac converter bus-bar (Bus 1 for MMC1 and Bus 2 for MMC2). The angle of this bus voltage is tracked by a phase-locked loop (PLL) which provides the synchronizing reference. The details of the individual rectifier and inverter side controllers are given below.

1) Rectifier Side Controller

The MMC1, rectifier is responsible for regulating the dc side voltage and ac side Bus1 voltage as shown in Fig. 11. Proportional-integral controllers derive magnitude, M_1 , and phase, δ_1 , of the reference waveform to regulate the ac bus-bar voltage and the dc bus voltage respectively. Using these, three phase reference waveforms are generated and sent to the firing control system shown in Fig. 4. as described in section II-D.

2) Inverter Side Controller

At the inverter, a similar control strategy is used, with the difference that the magnitude, M_2 , and phase, δ_2 , of the reference waveform are the outputs of proportional-integral controllers that regulate ac bus voltage and real power respectively, as shown in Fig. 12.

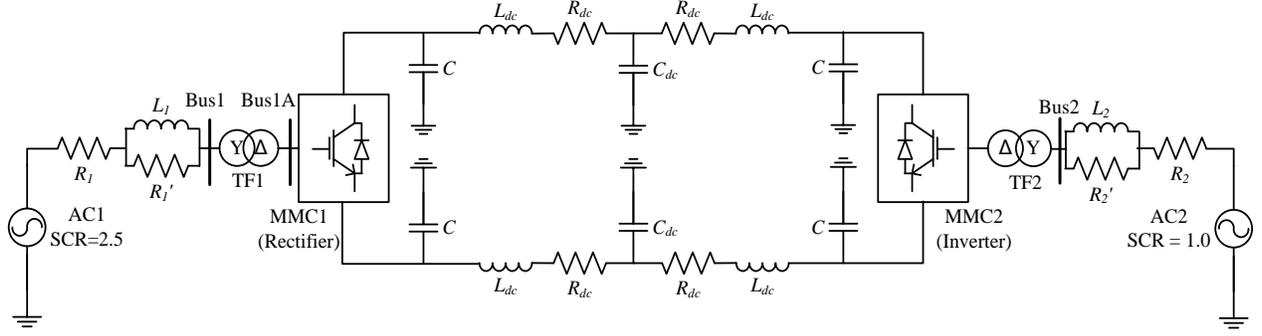


Fig. 10. MMC based HVDC system

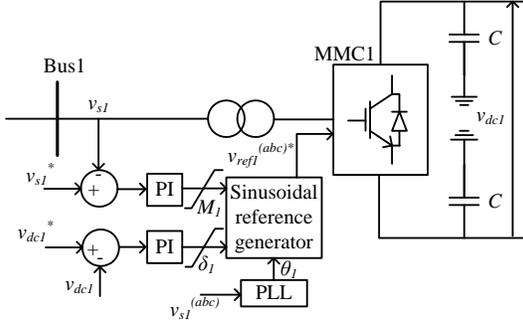


Fig. 11. Rectifier side converter controller

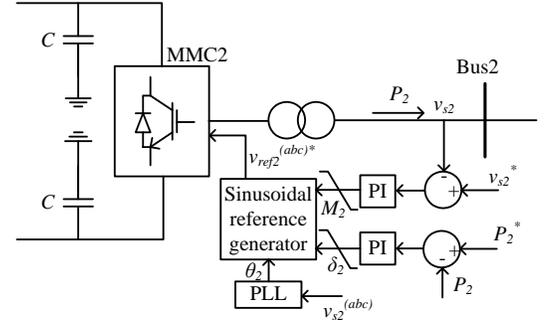


Fig. 12. Inverter side converter controller

B. Response of HVDC System to Power Order Change

Fig. 13 shows waveforms for the above HVDC transmission system where a power order change from full power (400 MW) to half power (200 MW) is applied at 0.4 s. The real and reactive power at the receiving end are shown in Fig. 13 (a), with the inverter side rms ac voltage and three phase bus voltage waveforms shown in Figs. 13 (b) and (c) respectively. From the simulation, it can be seen that when the load is reduced, the voltage is immediately controlled to the rated value of 115kV and no significant overvoltage is seen, even though the inverter side ac system is weak. The control of voltage is obtained by rapid control of the reactive power to follow the real power change, as shown in the trace of reactive power in Fig. 13 (a). The change in power to (to 90% of final setting) is seen to be achieved in approximately 60 ms in Fig. 13(a). The converter output ac voltage waveforms are shown during this transient and are indeed sinusoidal even though no ac filters are used.

VI. CONCLUSION

The multi-level modular converter is an attractive topology for HVDC operation. The paper presented the basic control approach for use of this device in HVDC transmission applications. Through calculation and EMT simulation, it was shown that the MMC can provide an essentially sinusoidal waveform that meets accepted guidelines of harmonic content, without the need for ac filters when the number of sub-modules per multi-valve exceeds 22.

A mechanism for voltage balancing is essential and one

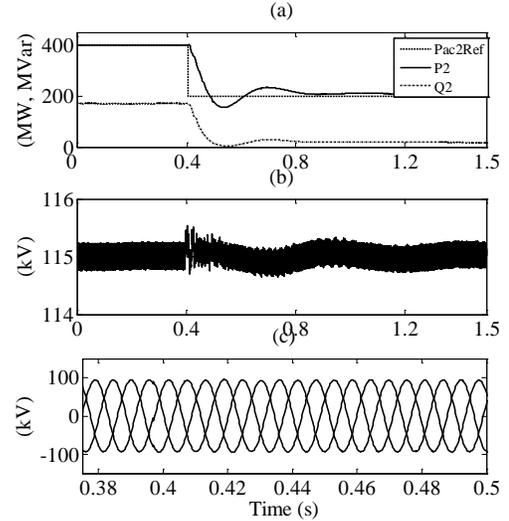


Fig. 13. Waveforms during the inclusion of a redundant sub-module; a) converter output voltage, b) output current, c) defective sub-module's capacitor voltage, and e) incoming sub-module's voltage

possible method for doing this was described and demonstrated through the use of simulation. The capacitor voltage balancing controller was rapidly able to restore balanced capacitor voltages.

The simulation model of the point to point HVDC system showed that the MMC works well in a full-scale application. It can respond rapidly to power order changes while maintaining ac and dc voltages at their desired reference values. Also, like other VSC converters, it is able to operate satisfactorily into very weak ac networks (SCRs of the order of 1.0).

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