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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2012.2183894

Publication date:
2012

Document Version
Early version, also known as pre-print

Design and Tuning of a Modified Power-Based PLL for Single-Phase Grid-Connected Power Conditioning Systems

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Abstract

One of the most important aspects for the proper operation of the single-phase grid-tied power-conditioning systems is the synchronization with the utility grid. Among various synchronization techniques, phase locked loop (PLL) based algorithms have found a lot of interest for the advantages they present. Typically, the single-phase PLLs use a sinusoidal multiplier as the phase detector (PD). These PLLs are generally referred to as the power-based PLL (pPLL). In this paper, the drawbacks associated with the pPLL technique (i.e., the sensitivity to the grid voltage variations, and the double frequency oscillations which appear in the estimated phase/frequency) are discussed in detail, and some of the previously reported solutions are examined. Then, to overcome these drawbacks, a simple and effective technique, called the double-frequency and amplitude compensation (DFAC) method is proposed. The effectiveness of the proposed method is evaluated through a detailed mathematical analysis. A systematic design method to fine-tune the PLL parameters is then suggested, which guarantees a fast transient response, a high disturbance rejection capability, and a robust performance. Finally, the simulation and experimental results are presented, which highlight the effectiveness of the proposed PLL.

Index Terms

Frequency estimation, phase estimation, phase-locked loop (PLL), power-based PLL (pPLL), synchronization, single phase grid-connected converters.

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This work was supported by the Abadan Branch-Islamic Azad University under Innovative Research Scheme.

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I. Introduction

The phase-angle and frequency of the utility grid are vital information for most single-phase grid-tied power-conditioning systems, such as active power filters (APF) [1], dynamic voltage restorers (DVR) [2]-[3], flexible AC transmission systems (FACTS) [4]-[6], uninterruptible power supplies (UPS) [7], and distributed power generation and storage systems [8].

To estimate the frequency and phase-angle of the single-phase signals various methods have been proposed in literature [4]-[25]. Among these techniques, the phase locked loop (PLL) based algorithms are the most widely accepted ones, due to their simplicity, robustness, and effectiveness [4]-[20]. Focusing on grid-connected power converter applications, a PLL is a closed loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with the grid voltage fundamental component. In spite of their differences, all PLL techniques are composed of three basic parts, namely: 1) phase detector (PD), 2) loop filter (LF), and 3) voltage-controlled oscillator (VCO), as illustrated in Fig. 1.

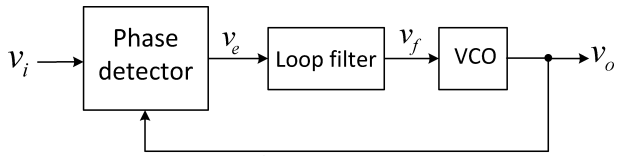


Fig. 1. Basic scheme of a single-phase PLL.

The main difference among different PLLs usually lies in how the PD block is implemented. Typically, the single-phase PLLs use a sinusoidal multiplier as the PD. These PLLs are generally referred to as the power-based PLL (pPLL). In the following section, the drawbacks associated with the pPLL technique (i.e., the sensitivity to the grid voltage variations, and the double frequency oscillations which appear in the estimated phase/frequency) are discussed in detail, and some of the previously reported solutions are examined. Then, to overcome these drawbacks, a simple and effective technique, called the double-frequency and amplitude compensation (DFAC) method is proposed. Through a detailed mathematical analysis it is shown that the proposed DFAC method successfully

compensates for the undesired double frequency oscillations, as well as the input voltage amplitude variations without decreasing the bandwidth of the PLL, which leads to a poor dynamic performance. It is worth remarking that, for three-phase PLLs, tackling the generation of the low order oscillations in the estimated phase/frequency has been well addressed [26], [27].

An accurate tuning of the PLL parameters requires considering several factors such as the stability margin, the disturbance rejection ability, and the transient response to the phase-jump and frequency variation. Some suggestions to design the PLL parameters have been presented in literature [7], [10]-[13], [28]-[29]. In this paper, a systematic design procedure to fine-tune the PLL parameters is proposed. The suggested approach guarantees a fast transient response, a high disturbance rejection capability, and a robust performance.

This paper is organized as follows. Section II provides a brief review of the pPLL topology. The main drawbacks of the pPLL, and previously reported solutions are also discussed in this section. The proposed phase detector is presented in Section III. The small-signal modeling of the proposed PLL, here, referred to as DFAC-pPLL, and the stability analysis are addressed in Section IV. The proposed systematic design method is discussed in Section V. The simulation and experimental results are presented in Section VI. Finally, Section VII concludes this paper.

II. Background

The basic scheme of the single-phase pPLL is depicted in Fig. 2 [7]. Throughout this section and the following section, for the sake of simplicity, the input voltage v_i is assumed to be a pure sine wave, i.e. $v_i = Vcos\theta$, where V and $\theta\,(=\omega t+\phi)$ are the input voltage amplitude and angle, respectively. ω_{ff} is the nominal value of the frequency ω, and ϕ is the phase-angle. The superscript "^" denotes the estimated quantities.

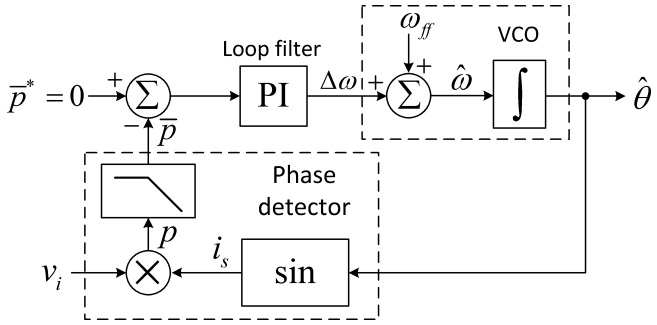


Fig. 2. Single-phase pPLL.

The pPLL, as seen, uses a sinusoidal multiplier followed by a low pass filter (LPF) for the PD. Note that the PD block tries to emulate an active power calculation unit. If the PD block output signal (i.e., $\bar{p}$) is zero, then the input voltage v_i and the fictitious current i_s will be in quadrature relative to each other [7]. In this case, the estimated value of the voltage angle $\hat{\theta}$ is equal to the real value θ.

Based on Fig. 2, the fictitious power p can be expressed as

$$p = v_i i_s = V cos\theta sin\hat{\theta}. \tag{1}$$

Applying the product-to-sum trigonometric identity, yields

$$p = \underbrace{\frac{V}{2}\sin(\hat{\theta}-\theta)}_{\text{dc term}} + \underbrace{\frac{V}{2}\sin(\hat{\theta}+\theta)}_{\text{double frequency term}}. \tag{2}$$

Supposing a small difference between θ and $\hat{\theta}$, (2) can be divided into two parts: a small dc term which has the information on the phase difference, and a high-amplitude double-frequency disturbance term which must be filtered out to keep up the phase jittering within an acceptable range [30].

To cancel out the undesired double-frequency component from the fictitious power p, one can use either a first- (or second-) order LPF with a low cut-off frequency or a high-order LPF with a higher cut-off frequency. In addition to stability problems, using a high-order LPF imposes a high computational load on the control system [31]. On the other hand, using a low-order LPF with a low cut-off frequency, significantly degrades the transient performance of the PLL. Another approach is to use a notch filter tuned at twice the input voltage fundamental frequency. Because of the grid frequency variations, the notch filter should be adaptive, which increases the system cost and complexity.

Some improvements to the pPLL have been suggested in [16]-[17]. In these techniques, referred to as orthogonal signal generation (OSG) based techniques, the fundamental component of the input voltage is shifted by 90° to generate a fictitious phase signal, thus making it possible to represent the single-phase system as a pseudo two-phase ($\alpha\beta$) system. Applying the well-known park ($\alpha\beta \longrightarrow dq$) transformation to the two phase ($\alpha\beta$) system, yields the phase error information without generating the undesired double frequency component. It should be noticed that the main difference among different OSG based techniques lies in how the fictitious orthogonal signal is generated. In spite of their differences, all OSG based techniques suffer from some common drawbacks, such as high sensitivity to the grid frequency variations, and relatively high complexity [18].

The most recent improvement to the pPLL is that proposed by Thacker et al. [12]. In their method, a unity value for the input voltage amplitude is assumed which is realized by a peak voltage detection (PVD) scheme at the input of the PLL. Under this assumption, and in phase/frequency-locked conditions (i.e., $\theta \cong \hat{\theta}$), the unwanted double frequency component is filtered out by subtracting a product term (i.e., $sin\hat{\theta}cos\hat{\theta}$) from the fictitious power p, as shown in Fig. 3. Although this PLL exhibits some improvements over the pPLL technique, it suffers from a major drawback; regardless of the cost and the complexity imposed by the PVD, the exact and fast estimation of the input voltage amplitude may not always be possible. In this case, the PLL performance is significantly degraded.

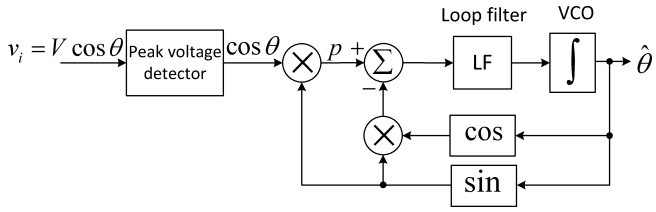


Fig. 3. Proposed PLL by Thacker et al. [12].

The dependency of the PLL stability and dynamic performance on the input voltage amplitude is other drawback of the pPLL. It is shown that the voltage amplitude V contributes as a gain in the forward path of the PLL small-signal model [32]. Thus, under the voltage sag condition, which is commonly associated with the phase-angle jump [33], [34], the PLL transient response is significantly degraded. In this situation, the PLL may also become unstable, if the phase margin is too low [35]. These drawbacks can be eliminated in part by compensating the PLL input signal with an amplitude estimation scheme, as reported in [4]- [5], [12], and [14], but at the expense of higher complexity and cost.

To filter out the undesired steady-state double-frequency oscillations without degrading the stability and the transient performance of the PLL and, at the same time, to compensate for the input voltage amplitude variations, an effective method, called the double-frequency and amplitude compensation (DFAC) method, is presented in the next section.

III. Proposed DFAC Method

Fig. 4 displays the basic scheme of the proposed phase detection unit, where v_d and v_q are obtained as expressed in (3).

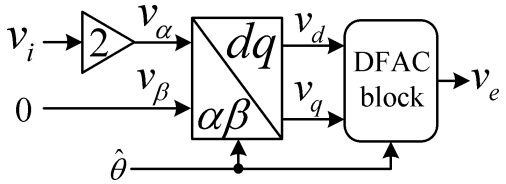


Fig. 4. Basic scheme of the proposed phase detection unit.

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} 2v_i(t) \\ 0 \end{bmatrix} \tag{3}$$

Substituting $v_i = Vcos\theta$ into (3), gives

$$v_d(t) = V\cos(\theta - \hat{\theta}) + V\cos(\theta + \hat{\theta}) \tag{4}$$

$$v_q(t) = V\sin(\theta - \hat{\theta}) - V\sin(\theta + \hat{\theta}). \tag{5}$$

Considering $\theta_e = \theta - \hat{\theta}$, and after some simple mathematical manipulations, (4) and (5) can be rewritten as

$$v_d(t) = V\cos(\theta_e) + V\cos(2\hat{\theta} + \theta_e) \tag{6}$$

$$v_q(t) = V\sin(\theta_e) - V\sin(2\hat{\theta} + \theta_e). \tag{7}$$

Expanding the second terms on the right hand side of (6) and (7), yields

$$v_d(t) = V\cos(\theta_e) + V\cos(\theta_e)\cos(2\hat{\theta}) - V\sin(\theta_e)\sin(2\hat{\theta}) \tag{8}$$

$$v_q(t) = V\sin(\theta_e) - V\sin(\theta_e)\cos(2\hat{\theta}) - V\cos(\theta_e)\sin(2\hat{\theta}). \tag{9}$$

For a small angle difference θ_e, the first terms on the right hand side of (8) and (9) (i.e., $Vcos(\theta_e)$, and $Vsin(\theta_e)$, respectively) are almost DC components. It is also clear from (8) and (9) that the amplitudes of the double-frequency components depend on these DC components. Thus, the perfect cancellation of the undesired double-frequency components can be easily achieved by injecting double-frequency signals with the same amplitude but an opposite angle into v_d and v_q, as shown in Fig. 5.

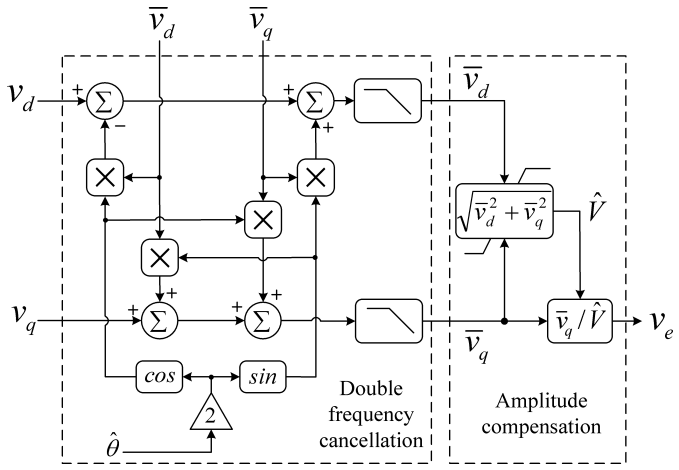


Fig. 5. Schematic diagram of the proposed DFAC method.

The proposed DFAC strategy consists of two main parts; a double frequency cancellation block, and an amplitude compensation block. The LPF block is considered as a first-order LPF as follows

$$LPF(s) = \frac{\omega_p}{s + \omega_p} \tag{10}$$

where ω_p is the cut-off frequency of the LPF.

A. Mathematical Analysis

To analyze the performance of the proposed DFAC method, the mathematical expressions for $\bar{v}_d$ and $\bar{v}_q$ are derived.

From Fig. 5, in the Laplace domain, we have

$$\bar{v}_d(s) = \frac{\omega_p}{s+\omega_p} \times \ell \left[v_d(t) - \bar{v}_d(t)\cos(2\hat{\theta}) \ + \bar{v}_q(t)\sin(2\hat{\theta}) \right] \tag{11}$$

$$\bar{v}_q(s) = \frac{\omega_p}{s+\omega_p} \times \ell \left[v_q(t) + \bar{v}_d(t)\sin(2\hat{\theta}) \ + \bar{v}_q(t)\cos(2\hat{\theta}) \right] \tag{12}$$

where, ℓ denotes the Laplace operator.

Multiplying both sides of (11) and (12) by $(s+\omega_p)$, and rearranging them, gives

$$s\bar{v}_d(s) = \omega_p \times \ell \left[v_d(t) - (\cos(2\hat{\theta}) + 1)\bar{v}_d(t) \ + \sin(2\hat{\theta})\bar{v}_q(t) \right] \tag{13}$$

$$s\bar{v}_q(s) = \omega_p \times \ell \left[v_q(t) + \sin(2\hat{\theta})\bar{v}_d(t) \ + (\cos(2\hat{\theta}) - 1)\bar{v}_q(t) \right]. \tag{14}$$

Transforming (13) and (14) into the time-domain, and rearranging the results into the matrix form, yields

$$\begin{bmatrix} \dot{\bar{v}}_d(t) \\ \dot{\bar{v}}_q(t) \end{bmatrix} = \omega_p \begin{bmatrix} -\cos(2\hat{\theta}) - 1 & \sin(2\hat{\theta}) \\ \sin(2\hat{\theta}) & \cos(2\hat{\theta}) - 1 \end{bmatrix} \begin{bmatrix} \bar{v}_d(t) \\ \bar{v}_q(t) \end{bmatrix} + \begin{bmatrix} \omega_p & 0 \\ 0 & \omega_p \end{bmatrix} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix}. \tag{15}$$

Substituting (8) and (9) into (15), and making some rearrangements, gives

$$\begin{bmatrix} \dot{\bar{v}}_d(t) \\ \dot{\bar{v}}_q(t) \end{bmatrix} = \omega_p \begin{bmatrix} -\cos(2\hat{\theta}) - 1 & \sin(2\hat{\theta}) \\ \sin(2\hat{\theta}) & \cos(2\hat{\theta}) - 1 \end{bmatrix} \left\{ \begin{bmatrix} \bar{v}_d(t) \\ \bar{v}_q(t) \end{bmatrix} - \begin{bmatrix} V\cos(\theta_e) \\ V\sin(\theta_e) \end{bmatrix} \right\}. \tag{16}$$

Based on (16), the state-space description of the DFAC block can be derived, as follows

$$\begin{cases} \dot{x}(t) = A(t)x(t) + B(t)u(t) \\ \qquad y(t) = C(t)x(t) \end{cases} \tag{17}$$

where,

$$x(t) = \begin{bmatrix} \bar{v}_d(t) \\ \bar{v}_q(t) \end{bmatrix}; \quad u(t) = \begin{bmatrix} V\cos(\theta_e) \\ V\sin(\theta_e) \end{bmatrix}$$

$$A(t) = -B(t) = \omega_p \begin{bmatrix} -\cos(2\hat{\theta}) - 1 & \sin(2\hat{\theta}) \\ \sin(2\hat{\theta}) & \cos(2\hat{\theta}) - 1 \end{bmatrix}$$

$$C(t) = I.$$

The state-space equation (17), describes a linear time-variant (LTV) system with two inputs and two outputs, which its solution takes a lot of time and space, and needs enormous patience. To simplify the solution, it is assumed that $\omega \cong \hat{\omega}$. Hereby, the angle difference θ_e becomes approximately equal to the phase difference $\phi - \hat{\phi}$. Under this condition, and considering the inputs (i.e., $V\cos(\theta_e)$, and $V\sin(\theta_e)$) as step functions, the expressions for $\bar{v}_d(t)$ and $\bar{v}_q(t)$ can be derived as

$$\bar{v}_d(t) = A_d + \{B_d\cos(\omega t)\cos(\omega_f t) + C_d\sin(\omega t)\sin(\omega_f t) + D_d\sin(\omega t)\cos(\omega_f t) + E_d\cos(\omega t)\sin(\omega_f t)\}\, e^{-\omega_p t} \quad (18)$$

$$\bar{v}_q(t) = A_q + \{B_q\cos(\omega t)\cos(\omega_f t) + C_q\sin(\omega t)\sin(\omega_f t) + D_q\sin(\omega t)\cos(\omega_f t) + E_q\cos(\omega t)\sin(\omega_f t)\}\, e^{-\omega_p t} \quad (19)$$

where,

$\omega_f = \sqrt{\omega^2 - \omega_p^2}$,

$A_d = -B_d = D_q = V\cos(\theta_e)$,

$C_d = E_q = -V\left[\omega\cos(\theta_e) + \omega_p\sin(\phi + \hat{\phi})\right]/\omega_f$,

$D_d = -A_q = B_q = -V\sin(\theta_e)$, and

$E_d = -C_q = V\left[\omega_p\cos(\phi + \hat{\phi}) + \omega\sin(\theta_e)\right]/\omega_f$.

From (18) and (19) it can be seen that, the fluctuating terms decay to zero with a time constant of $1/\ \omega_p$, and $\bar{v}_d(t)$ and $\bar{v}_q(t)$ converge to $V\cos(\theta_e)$ and $V\sin(\theta_e)$, respectively. These results are clearly illustrated in Fig. 6 for three different values of the cut-off frequency ω_p, i.e., $\omega_p = 10\,Hz$ (solid line), $\omega_p = 30\,Hz$ (dashed line), and $\omega_p = 60\,Hz$ (dotted line), and for $\phi = \hat{\phi} = \pi/6$ rad, $\omega = \hat{\omega} = 120\pi$ rad/s, and V = 100 V. As expected, using the proposed DFAC method, the perfect cancellation of the double-frequency components is achieved.

On the other hand, the negative effect of the input voltage amplitude variations on the PLL stability and transient performance is damped by calculating the input voltage amplitude, as follows, and then dividing $\bar{v}_q$ by the estimated amplitude $\hat{V}$ (see Fig. 5).

$$\hat{V} = \sqrt{\bar{v}_d^2 + \bar{v}_q^2}. \quad (20)$$

To avoid instability problems, the estimated amplitude $\hat{V}$ is limited by a saturation block. The upper and lower

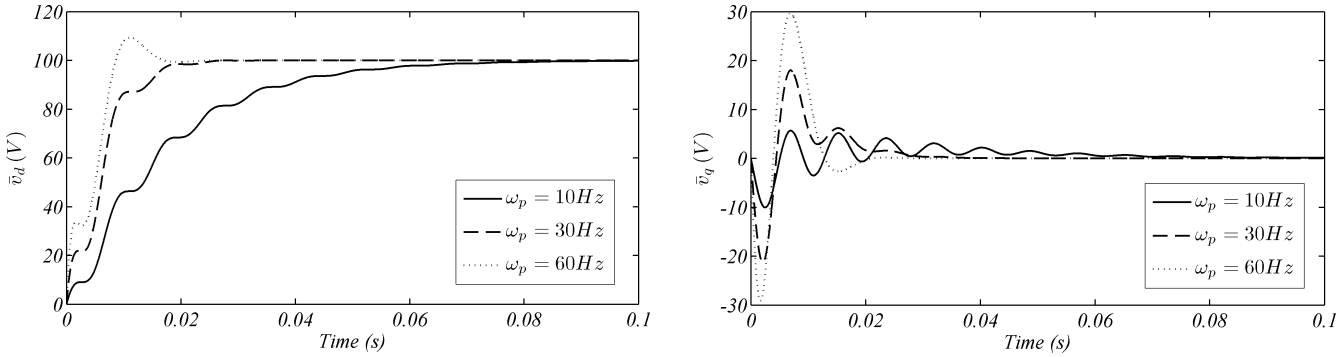


Fig. 6. $\bar{v}_d(t)$ and $\bar{v}_q(t)$ for different values of ω_p.

limits should be set according to the allowable range of the input voltage amplitude variations. In this paper, the lower and upper limits are set to 0.2 pu and 1.5 pu, respectively.

IV. Small-Signal Model and Stability Analysis

Fig. 7 illustrates the basic scheme of the proposed DFAC-pPLL. The input voltage v_i is considered to be harmonic polluted (as a result of the proliferation of nonlinear loads in power systems), and is represented by

$$v_i(t) = \underbrace{V\cos(\omega t + \phi)}_{\text{Fundamental componet}} + \underbrace{f\,(3\omega,\ 5\omega,\ 7\omega,\ ...)}_{\text{Harmonic components}}. \tag{21}$$

Applying the transformation matrix (3) to (21), gives

$$v_q(t) = V\sin(\theta - \hat{\theta}) - V\sin(\theta + \hat{\theta}) + g\,(2\omega,\ 4\omega,\ 6\omega,\ ...)\,. \tag{22}$$

Note that, the second term on the right hand side of (22), and the amplitude V are both compensated by the function of the DFAC block in the steady-state. Hence, for a small angle difference θ_e, the PD output signal, i.e. v_e, can be approximated in the Laplace domain as

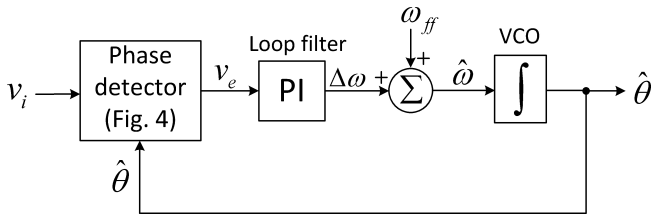


Fig. 7. Basic scheme of the proposed DFAC-pPLL.

$$v_e(s) \cong \frac{\omega_p}{s+\omega_p}\left(\theta_e(s) + D(s)\right) \tag{23}$$

where, $D(s)$ is the Laplace transform of the harmonic function $g\left(2\omega,\, 4\omega,\, 6\omega,\, ...\right)$ divided by V.

Based on the above discussion, the small-signal model of the DFAC-pPLL can be obtained, as shown in Fig. 8, where k_p and k_i are the proportional and integral gains, respectively. Note that, $D(s)$ appears as a disturbance input to the PLL small-signal model.

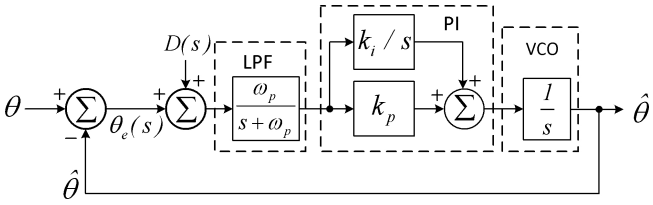


Fig. 8. Small-signal model of the DFAC-pPLL.

From Fig. 8, the closed loop transfer function of the system can be obtained as

$$\hat{\theta}(s) = G(s)\left[\theta(s) + D(s)\right] \tag{24}$$

where,

$$G(s) = \frac{k_p s + k_i}{\tau_p s^3 + s^2 + k_p s + k_i} \tag{25}$$

and $\tau_p = 1/\omega_p$.

The system stability is guaranteed, if the closed-loop poles, which are the roots of the characteristic equation (26), have negative real parts.

$$\tau_p s^3 + s^2 + k_p s + k_i = 0 \tag{26}$$

Applying the Routh-Hurwitz stability test to (26), gives the following range of parameters to keep the system stable.

$$0 < k_i < k_p \omega_p \tag{27}$$

V. Design Guidelines

The aim of this section is to design the PLL parameters (i.e., k_p, k_i, and ω_p) such that the system stability is guaranteed, and at the same time, a proper transient performance, and a high disturbance rejection capability is achieved. Some suggestions to improve the ride-through capability of the PLL is also presented in this section.

A. Stability

The main focus in this section is to establish a design criterion, based on the symmetrical optimum method [36], so that the maximum possible stability margin for the PLL is achieved.

Considering $k_i/k_p = \omega_z$, the open loop transfer function of the DFAC-pPLL can be derived as

$$G_{ol}(s) = \frac{k_p \omega_p (s + \omega_z)}{s^2 (s + \omega_p)}. \tag{28}$$

From (28), the phase margin (PM) can be obtained as

$$PM = \underbrace{\tan^{-1}(\omega_c/\omega_z)}_{\phi_z} - \underbrace{\tan^{-1}(\omega_c/\omega_p)}_{\phi_p} \tag{29}$$

where, ω_c is the crossover frequency, and is given by

$$\omega_c = k_p \frac{\cos(\phi_p)}{\sin(\phi_z)}. \tag{30}$$

Differentiating (29) with respect to the crossover frequency ω_c, i.e. $\partial(PM)/\partial(\omega_c)$, and equating the result to zero, yields

$$\omega_c = \sqrt{\omega_p \omega_z}. \tag{31}$$

Substituting (31) into (30), gives

$$\omega_c = k_p \tag{32}$$

which means that the PM is maximized when the proportional gain k_p is equal to the crossover frequency ω_c.

From (31), and assuming $\omega_p = k^2 \omega_z$, where k is a constant value, we get

$$\begin{cases} \omega_z = \omega_c/k \\ \omega_p = k\omega_c. \end{cases} \tag{33}$$

Substituting (33) into (29), PM can be rewritten as

$$PM = \tan^{-1} \frac{k^2 - 1}{2k}. \tag{34}$$

Fig. 9 displays the phase margin versus factor k. As shown, the higher the factor k is, the higher is the phase margin.

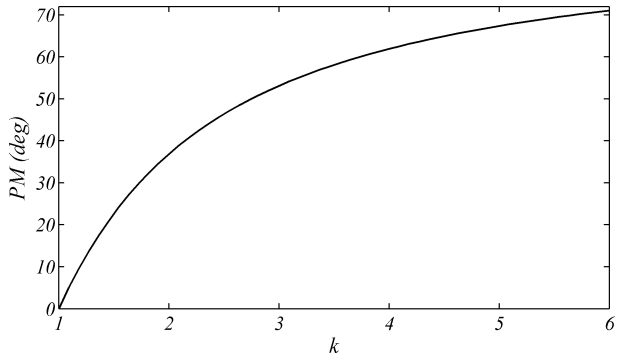


Fig. 9. Phase margin versus factor k.

Recommended value for a proper phase margin is [37]

$$30^\circ < PM < 60^\circ. \tag{35}$$

To meet this, we need

$$1.732 < k < 3.732. \tag{36}$$

B. Transient Performance

Here, we are going to optimize the PLL transient performance through minimizing its settling time for both phase and frequency jumps.

Substituting (32) and (33) into (28), the open loop transfer function G_{ol} can be rewritten as

$$G_{ol}(s) = \frac{k\omega_c^2 s + \omega_c^3}{s^2(s + k\omega_c)}. \tag{37}$$

The transfer function (37) has two poles at the origin (i.e., type-2 system). Thus, the zero steady-state error is guaranteed for both phase jump (step input) and frequency jump (ramp input) [28].

From Fig. 8, the error transfer function, i.e. $\theta_e(s)/\theta(s)$, can be derived as

$$G_e(s) = \frac{\theta_e(s)}{\theta(s)} = \frac{1}{1 + G_{ol}(s)}. \tag{38}$$

Substituting (37) into (38), yields

$$G_e(s) = \frac{s^2(s + k\omega_c)}{(s + \omega_c)(s^2 + (k-1)\omega_c s + \omega_c^2)}. \tag{39}$$

Considering $\zeta = (k-1)/2$, and $\omega_c = \omega_n$, (39) can be rewritten as

$$G_e(s) = \frac{s^2(s + (2\zeta+1)\omega_n)}{(s+\omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)}. \tag{40}$$

The inverse Laplace transform of $\theta_e(s) = G_e(s)\theta(s)$, for step and ramp inputs, yield the time-domain tracking errors for phase ($\theta_e^{\Delta\phi}(t)$) and frequency ($\theta_e^{\Delta\omega}(t)$) jumps, respectively, as given in (41) and (42).

$$\theta_e^{\Delta\phi}(t) = \begin{cases} \frac{\Delta\phi}{\zeta-1}\left[\zeta e^{-\omega_n t} - e^{-\zeta\omega_n t}\cos\left(\omega_n t\sqrt{1-\zeta^2}\right)\right] & \zeta < 1 \\ \Delta\phi\ e^{-\omega_n t}(1 + \omega_n t - \omega_n^2 t^2) & \zeta = 1 \\ \frac{\Delta\phi}{\zeta-1}\left[\zeta e^{-\omega_n t} - \frac{1}{2}e^{-(\zeta-\sqrt{\zeta^2-1})\omega_n t} - \frac{1}{2}e^{-(\zeta+\sqrt{\zeta^2-1})\omega_n t}\right] & \zeta > 1 \end{cases} \tag{41}$$

$$\theta_e^{\Delta\omega}(t) = \begin{cases} \frac{\Delta\omega}{(1-\zeta)\omega_n}\left[\zeta e^{-\omega_n t} + e^{-\zeta\omega_n t}\left\{-\zeta\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) + \sqrt{1-\zeta^2}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right\}\right] & \zeta < 1 \\ \frac{\Delta\omega}{\omega_n}e^{-\omega_n t}(\omega_n t + \omega_n^2 t^2) & \zeta = 1 \\ \frac{\Delta\omega}{(1-\zeta)\omega_n}\left[\zeta e^{-\omega_n t} - \frac{\zeta+\sqrt{\zeta^2-1}}{2}e^{-(\zeta-\sqrt{\zeta^2-1})\omega_n t} - \frac{\zeta-\sqrt{\zeta^2-1}}{2}e^{-(\zeta+\sqrt{\zeta^2-1})\omega_n t}\right] & \zeta > 1 \end{cases} \tag{42}$$

From (41) and (42), it is clear that by increasing the natural frequency ω_n, the PLL transient behavior (for both phase and frequency jumps) can be improved. Hence, ω_n should be chosen as high as possible to achieve a fast transient response. Evidently, a high value of ω_n, degrades the PLL disturbance rejection capability, thus one has to find a satisfactory trade-off.

Using Bode diagrams, it can be shown quite simply that, for a given value of ω_n, and for $1.732 < k < 3.732$ (i.e., $0.366 < \zeta < 1.366$), the damping factor ζ has relatively little effect on the disturbance rejection capability of the PLL. Hence, ω_n should be selected according to the disturbance rejection requirements of the PLL, and ζ should be chosen to meet the required transient response and the stability margin of the PLL.

Fig. 10 illustrates the DFAC-pPLL simulated settling-time (which has been normalized by a factor ω_n) versus the damping factor ζ, for both phase jump (black line) and frequency jump (gray line). As shown, for $\zeta < 1$, $\theta_e^{\Delta\phi}$ (phase-jump) and $\theta_e^{\Delta\omega}$ (frequency-jump) both have almost the same settling times. However, for $\zeta > 1$, the longer settling time can be observed for $\theta_e^{\Delta\omega}$. The minimum settling time for both $\theta_e^{\Delta\phi}$ and $\theta_e^{\Delta\omega}$ appears around $\zeta = 0.7$, as highlighted in Fig 10. Thus, $\zeta = 0.7$ is selected as the optimum value of the damping factor.

It is evident from (34) that the phase margin is only dependent on the factor k (and hence ζ). Thus, it is

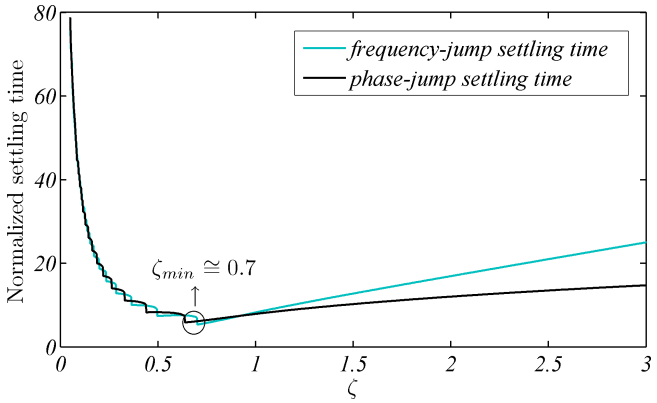


Fig. 10. Normalized settling time versus the damping factor ζ for the phase-jump (black line) and the frequency jump (gray line).

necessary to analyze the PLL stability for the selected value of the damping factor ζ. Substituting $\zeta = 0.7$ (which is corresponding to $k = 2.4$) into (34), yields

$$PM|_{k=2.4} = 44.76^{\circ} \tag{43}$$

which guarantees the PLL stability.

C. Disturbance Rejection

As mentioned earlier, the input voltage harmonics (i.e., the odd harmonics as 3^{rd}, 5^{th}, 7^{th}, etc) appear as disturbance inputs (i.e., the even harmonics as 2^{nd}, 4^{th}, 6^{th}, etc) to the PLL linearized model. Thus, it is necessary to provide a sufficient attenuation at the concerned frequencies.

From Fig. 8, the disturbance transfer function relating the estimated angle $\hat{\theta}$ to the disturbance input $D(s)$ can be derived as

$$G_D(s) = \frac{\hat{\theta}(s)}{D(s)} = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{(2\zeta + 1)\omega_n^2 s + \omega_n^3}{(s + \omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)}. \tag{44}$$

Fig. 11 illustrates the Bode plot of the transfer function (44) for three different values of the natural frequency ω_n, namely, $\omega_n = 5\,Hz$ (solid line), $\omega_n = 15\,Hz$ (dashed line), and $\omega_n = 30\,Hz$ (dotted line), and for $\zeta = 0.7$. As shown, the transfer function (44) exhibits a low-pass filtering behavior. The lower the natural frequency is, the higher is the attenuation at the disturbance frequencies, and hence, the better is the filtering property.

Providing a sufficient attenuation at twice the input voltage fundamental frequency (i.e., 2ω), guarantees the high disturbance rejection capability. Fig .12 displays the PLL attenuation at 2ω versus the natural frequency ω_n. The proper attenuation (which depends on the application where the PLL is used) is selected to be $-20dB$ in this paper,

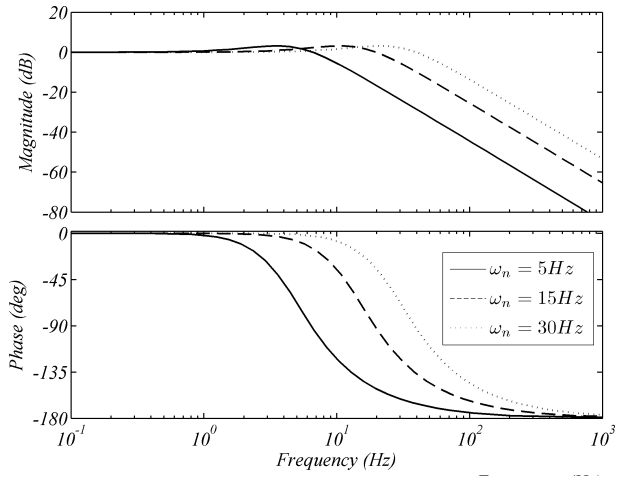


Fig. 11. Bode plot of the disturbance transfer function as a function of the natural frequency ω_n: $\omega_n = 5\,Hz$ (solid line), $\omega_n = 15\,Hz$ (dashed line), and $\omega_n = 30\,Hz$ (dotted line).

yielding the natural frequency ω_n (and hence the crossover frequency ω_c) equals to $24.71\,Hz$.

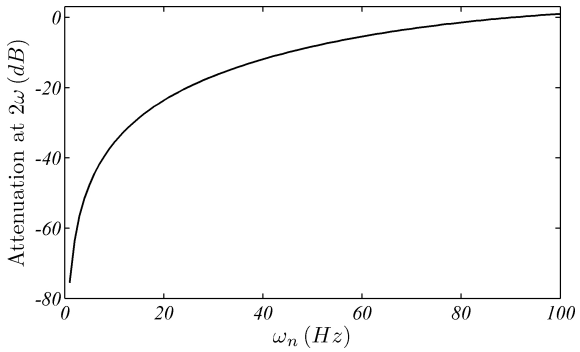


Fig. 12. Attenuation at twice the input voltage fundamental frequency versus the natural frequency ω_n.

Considering $\omega_c = 24.71\,Hz$ ($155.26\,rad/s$), and $k = 2.4$, the PLL parameters k_p, k_i, and ω_p can be obtained as

$$\begin{cases} k_p = \omega_c = 155.26 \\ k_i = \omega_c^2/k = 10044 \\ \omega_p = k\omega_c = 59.3\,Hz. \end{cases} \tag{45}$$

D. Ride Through

Another important feature of a PLL for grid-connected power conditioning systems is the ride-through capability, meaning that, the PLL has to remain synchronized with the grid voltage during the abnormal conditions such as

the severe voltage sags.

Voltage sags are the most common power quality disturbances in the utility grid [39]. They are transitory in nature, and mainly caused by switching of large loads, energizing of transformers, connection of large induction motors, and short circuit faults. When a voltage sag occurs, thanks to the action of the amplitude compensation block, a fast estimation (about one cycle of the fundamental frequency, as shown in Fig. 13) of the input voltage amplitude is achieved, making the proposed DFAC-pPLL insensitive to the grid voltage amplitude variations during the steady-state condition.

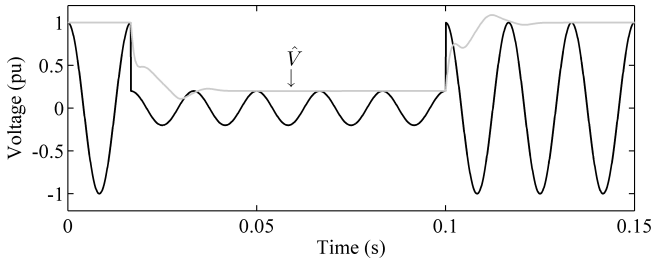


Fig. 13. Grid voltage waveform and its estimated amplitude by the DFAC-pPLL under a voltage sag of 0.8 pu.

In the case of line outages, or when the grid faults cause the input voltage amplitude reduces to almost zero, the PLL may not be able to work properly. The reason is that, even under such conditions, the loop filter tries to track the reference signal. To assure the ride-through capability, the structure shown in Fig. 14 is recommended [7], [40]. Here, the grid voltage is continuously monitored by a line quality algorithm, which can be a voltage amplitude monitoring algorithm in its simplest form. Once an unacceptable grid condition is detected, the loop filter is disconnected from the phase detector, so that the output signal of the PLL remains on its nominal condition. Obviously, the threshold values for detecting the unacceptable grid condition depend on the application where the PLL is used, and can be chosen in accordance with the standards EN 50160 [38], IEEE 1547.1-2005 [41], UL 1741 [42], and IEC 61727 [43], or the national grid codes.

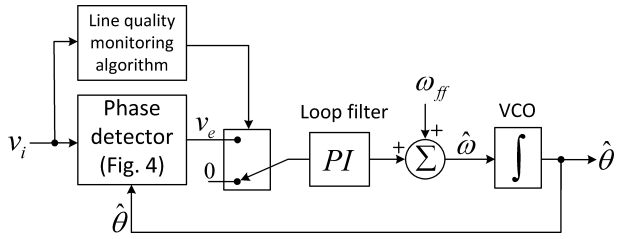


Fig. 14. Modified structure of the DFAC-pPLL to assure the ride-through capability.

VI. Performance Evaluation

In the following, the performance of the proposed DFAC-pPLL has been evaluated through extensive simulations in Matlab/Simulink environment, and experiments based on a TMS320F28335 floating-point 150-MHz digital signal controller (DSC) from Texas Instruments. The sampling frequency has been fixed to 10 kHz, and the nominal frequency has been set to 60 Hz. To generate the desired input voltage in experimental verifications, a programmable ac voltage source has been utilized.

A. Phase Jump

Figs. 15 and 16 depict the simulation and experimental results, respectively, when a phase jump of 40° occurs in the input voltage. It can be seen that the phase error decays to zero in about 40 ms (i.e. less than 2.5 cycles), and the overshoot is limited to 15°. Notice that the simulation and experimental results are in perfect agreement.

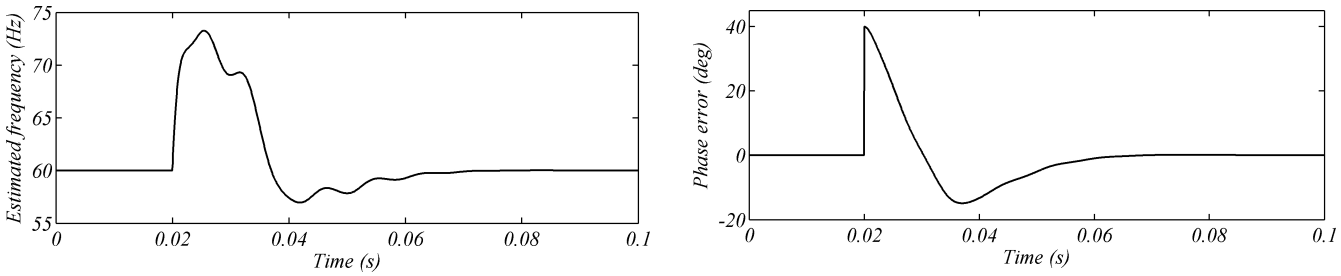


Fig. 15. Simulation results for the phase jump of 40°: a) estimated frequency, b) phase error.

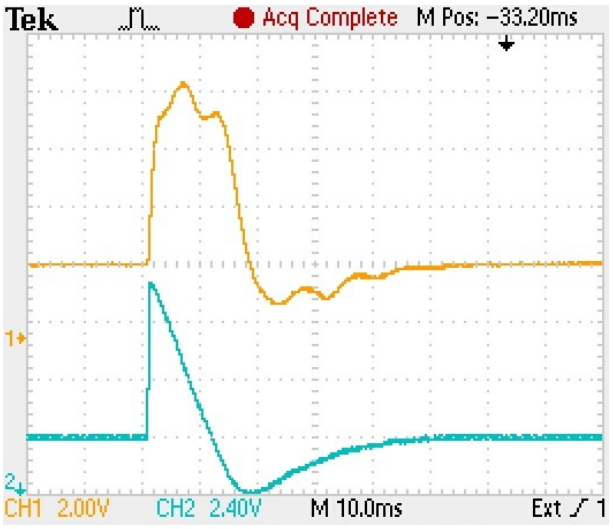


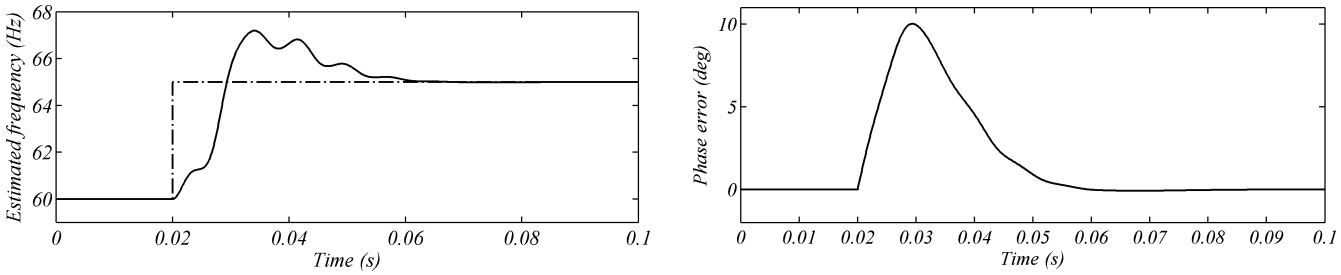
Fig. 16. Experimental results for the phase jump of 40°: Ch1) estimated frequency (4 Hz/div), Ch2) phase error (15 deg/div).

B. Frequency Jump

Figs. 17 and 18 illustrate the simulation and experimental results, respectively, when the input voltage undergoes a frequency-jump of 5 Hz. As shown, the estimated frequency is locked to the real one in about 40 ms (i.e. less than 2.5 cycles). The phase-error peak is about 10° in this condition.

C. Voltage Sag

Figs. 19 and 20 show the simulation and experimental results, respectively, when the input voltage undergoes a voltage sag of 30%. As shown, the phase-error settling time is less than one-and-a-half cycles. During the transient, the peak-to-peak value of the phase error is limited to 4°.



(a) (b)

Fig. 17. Simulation results for the frequency jump of 5 Hz: a) estimated frequency, b) phase error.

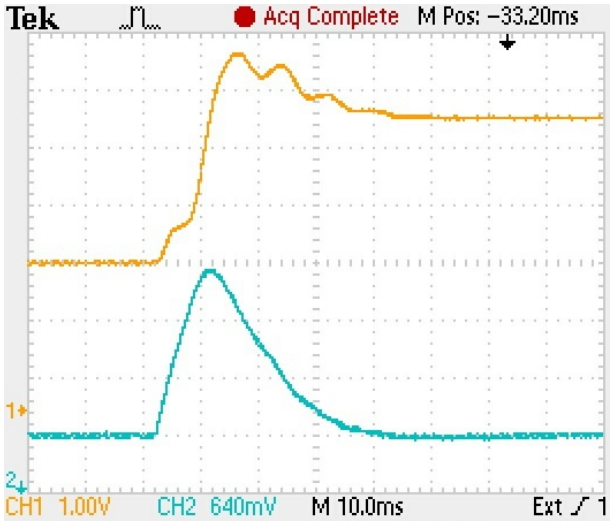
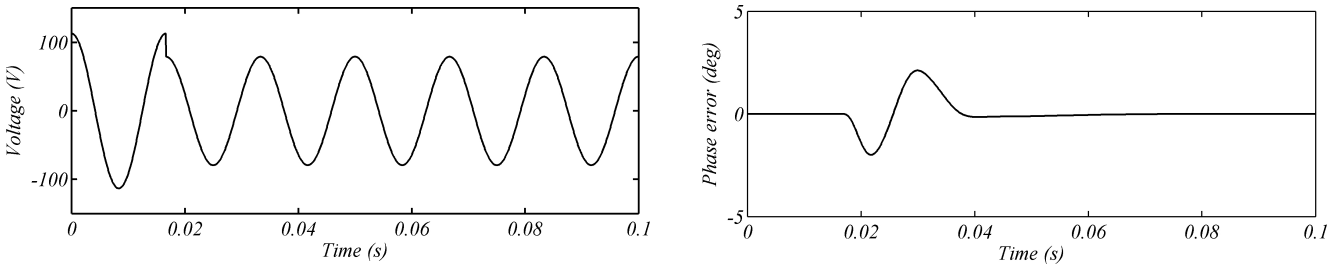


Fig. 18. Experimental results for the frequency jump of 5 Hz: Ch1) estimated frequency (2 Hz/div), Ch2) phase error (4 deg/div).



(a) (b)

Fig. 19. Simulation results for voltage sag of 30%: a) input voltage, b) phase error.

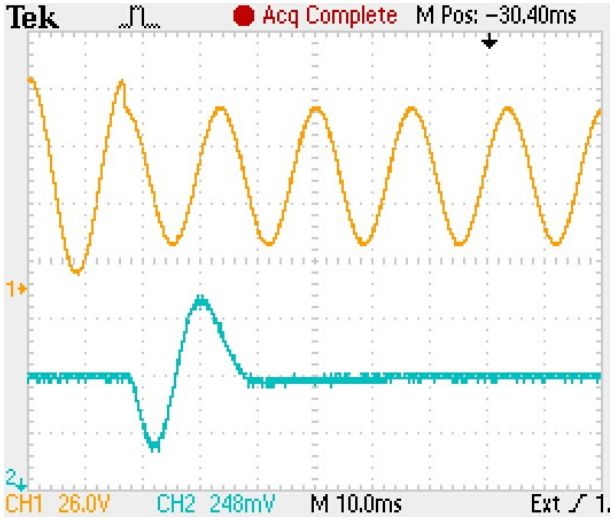


Fig. 20. Experimental results for voltage sag of 30%: Ch1) input voltage (26 V/div), Ch2) phase error (1.5 deg/div).

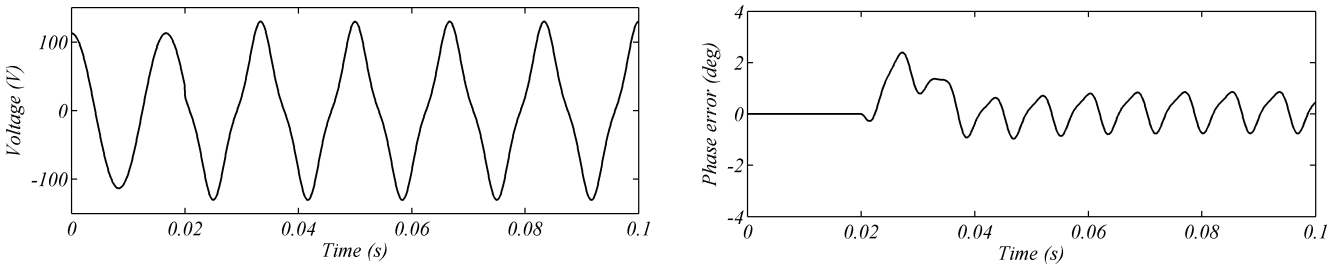
D. Harmonic Distortion

Figs. 21 and 22 illustrate the simulation and experimental results, respectively, when 15% third-harmonic component is injected into the input voltage. As shown, the harmonic distortion causes a peak-to-peak phase-error of about 1.7° in the steady-state. It is worth mentioning that, this error can be further reduced by selecting a lower crossover frequency ω_c (and hence higher attenuation at the disturbance frequencies), but at the expense of degrading the transient behavior of the PLL.

E. Noise Immunity

The degree of the noise immunity of the DFAC-pPLL is investigated in this section. For this reason, the voltage v_i is contaminated by a zero-mean white Gaussian noise of variance 0.05. Considering a unity value for the input signal amplitude, the signal-to-noise ratio (SNR) at the input terminal is [44]

$$\mathrm{SNR}_{\mathrm{in}} = 10\log(\frac{V^2}{2\sigma^2}) = 10\ dB \tag{46}$$



(a) (b)

Fig. 21. Simulation results for 15% third harmonic injection: a) input voltage, b) phase error.

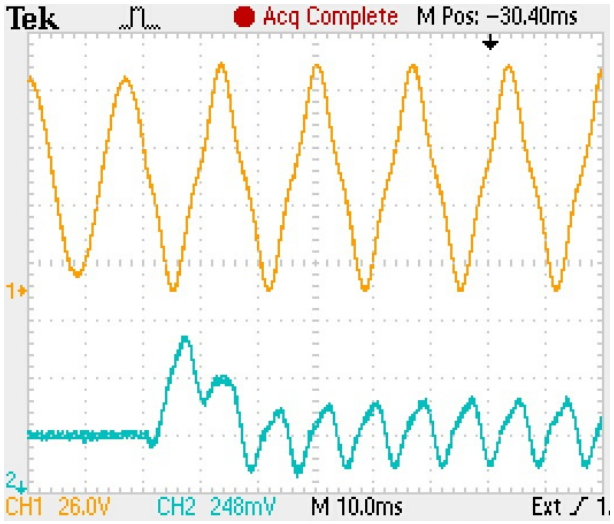
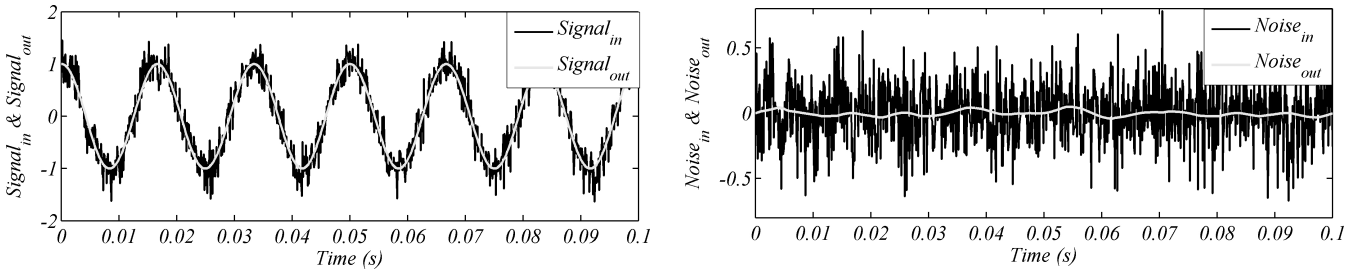


Fig. 22. Experimental results for 15% third harmonic injection: Ch1) input voltage (26 V/div), Ch2) phase error (1.5 deg/div).

where σ^2 is the noise variance.

Fig. 23(a) illustrates the noise-corrupted input signal (dark line) and output signal (light line) of the PLL. It can be seen that the proposed PLL yields high degree of noise immunity. The output noise is about one-tenth of the input noise (see Fig. 23(b)).



(a) (b)

Fig. 23. Degree of noise immunity of the proposed DFAC-pPLL: $\mathrm{SNR_{in}} = 10dB$ a) input (dark line) and output (light line) signals, b) input (dark line) and output (light line) noises.

F. Comparison

Table I provides a comparison between the results obtained from the DFAC-pPLL, and the ones obtained from pPLL, park-PLL, and Enhanced PLL (EPLL). The parameters of these three PLLs (i.e. pPLL, prak-PLL, and EPLL) are set equal to the values suggested in [7], yielding almost the same bandwidth for the EPLL (40 Hz), and the park-PLL (45 Hz) as compared to the DFAC-pPLL (42 Hz). The pPLL bandwidth is much lower (about 24 Hz), which is unavoidable, due the the high attenuation required at twice the input voltage fundamental frequency. The results shown in Table I highlight the promising performance of the proposed DFAC-pPLL.

TABLE I
COMPARISON SUMMARY.

	pPLL	**Park-PLL**	**EPLL**	**DFAC-pPLL**
$+40^\circ$ **phase-angle jump**				
Settling time	7 cycles	3 cycles	2.5 cycles	2.4 cycles
Overshoot	23°	14°	15°	15°
$+5Hz$ **frequency jump**				
Settling time	7 cycles	3 cycles	2.5 cycles	2.4 cycles
Peak phase error	30°	9°	9°	10°
Voltage sag of 30%				
Settling time	5 cycles	2 cycles	2.5 cycles	1.2 cycles
15% 3^{rd} **harmonic injection**				
Peak-to-Peak phase error	$\approx 0^\circ$	3°	5°	1.7°
Phase margin	34°	35.3°	61.3°	44.76°
Noise immunity	perfect	good	fair	good
Computational load	$2.58\,\mu s$	$3.8\,\mu s$	$3.04\,\mu s$	$3.96\,\mu s$

VII. CONCLUSION

To overcome the drawbacks associated with the pPLL, a simple and effective method, called DFAC method, was proposed in this paper. Through a detailed mathematical analysis it was shown that the suggested method successfully compensates for the undesired double frequency oscillations, as well as the input voltage amplitude variations without decreasing the bandwidth of the PLL, which leads to a poor dynamic performance. A systematic design procedure to fine-tune the PLL parameters was then proposed, which guarantees a fast transient response,

a high disturbance rejection capability, and a robust performance. To confirm the promising performance of the DFAC-pPLL, extensive simulation and experimental verifications were provided.

REFERENCES

[1] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, P. Fernandez-Comesana, C. Martinez-Penalver, "A Signal-Processing Adaptive Algorithm for Selective Current Harmonic Cancellation in Active Power Filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2829-2840, Aug. 2009.

[2] B. Bae, J. Lee, J. Jeong, and B. Han, "Line-Interactive Single-Phase Dynamic Voltage Restorer With Novel Sag Detection Algorithm," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2702-2709, Oct. 2010.

[3] C. N. m. Ho, H. S. H. Chung, and K. T. K. Au, "Design and implementation of a fast dynamic control scheme for capacitor-supported dynamic voltage restorers," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 237-251, Jan. 2008.

[4] D. Jovcic, "Phase locked loop system for FACTS," *IEEE Trans. Power Syst.*, vol. 18, no. 3, pp. 1116-1124, Aug. 2003.

[5] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, D. Pineiro, C. M. Penalver, and A. A. Nogueiras, "Real-time implementation of a SPLL for FACTS," *in 32nd Annual Conference on IEEE Industrial Electronics*, Nov. 2006, pp. 2390-2395.

[6] M. Karimi-Ghartemani, "A distortion-free phase-locked loop system for facts and power electronic controllers," *Elect. Power Syst. Res.*, vol. 77, no. 8, pp. 1095-1100, Jun. 2007.

[7] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923-2932, Aug. 2008.

[8] J. W. Choi, Y. K. Kim, H. G. Kim, "Digital PLL control for single-phase photovoltaic system," *Electric Power Applications, IEE Proceedings*, vol. 153, no. 1, pp. 40-46, Jan. 2006.

[9] G. C. Hsieh, and J. C. Hung, "Phase-locked loop techniques - a survey," *IEEE Trans. Power Electron.*, vol. 43, no. 6, pp. 609-615, Dec. 1996.

[10] S. Shinnaka, "A robust single-phase PLL system with stable and fast tracking," *IEEE Trans. Ind. Appl.*, vol. 44, no. 2, pp. 624-633, Mar./Apr. 2008.

[11] S. Shinnaka, "A novel fast-tracking D-estimation method for single-phase signals," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1081-1087, Apr. 2011.

[12] T. Thacker, D. Boroyevich, R. Burgos, and F. Wang, "Phase-Locked Loop Noise Reduction via Phase Detector Implementation for Single-Phase Systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2482-2490, Jun. 2011.

[13] Q. Zhang, X. D. Sun, Y. R. Zhong, M. Matsui, and B.-Y. Ren, "Analysis and design of a digital phase-locked loop for single-phase grid-connected power conversion systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3581-3592, Jul. 2011.

[14] M. Karimi-Ghartemani, H. Karimi, and M. R. Iravani, "A magnitude/phase-locked loop system based on estimation of frequency and inphase/quadrature-phase amplitudes," *IEEE Trans. Ind. Electron.*, vol. 51, no. 2, pp. 511-517, Apr. 2004.

[15] Y. Han, L. Xu, M. M. Khan, G. Yao, L. Zhou, and C. Chen, "A novel synchronization scheme for grid-connected converters by using adaptive linear optimal filter based PLL (ALOF-PLL)," *Simulation Modelling Practice and Theory*, vol. 17, no. 7, pp. 1299-1345, Aug. 2009.

[16] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Boaventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," *in 39th Conf. Rec. IEEE IAS Annu. Meeting*, Aug. 2004, vol. 4, pp. 2259-2263.

[17] L. N. Arruda, S. M. Silva, and B. J. C. Filho, "PLL structures for utility connected systems," *in 36th Conf. Rec. IEEE IAS Annu. Meeting*, Sep. 2001, vol. 4, pp. 2655-2660.

[18] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," *Proc. 37th IEEE PESC*, Jun. 2006, pp. 1511-1516.

[19] M. Ciobotaru, V. Agelidis, R. Teodorescu, and F. Blaabjerg, "Accurate and less-disturbing active antiislanding method based on PLL for grid-connected converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1576-1584, Jun. 2010.

[20] D. Velasco, C. Trujillo, G. Garcera, and E. Figueres, "An active anti-islanding method based on phase-PLL perturbation," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1056-1066, Apr. 2011.

[21] D. Yazdani, A. Bakhshai, G. Joos, and M. Mojiri, "A nonlinear adaptive synchronization technique for grid-connected distributed energy sources," *IEEE Trans. Power Electron.*, Jul. 2008, Vol. 23, no. 4, pp. 2181-2186.

[22] M. Mojiri, and A. Bakhshai, "An adaptive notch filter for frequency estimation of a periodic signal," *IEEE Trans. Automat. Control*, vol. 49, no. 2, pp. 314-318, Feb. 2004.

[23] M. Mojiri, and A. Bakhshai, "Estimation of n frequencies using adaptive notch filter," *IEEE Trans. Circiuts Syst. II*, vol. 54, no. 4, pp. 338-342, Apr. 2007.

[24] B. P. McGrath, D. G. Holmes, and J. J. H. Galloway, "Power converter line synchronization using a Discrete Fourier Transform (DFT) based on a variable sample rate," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 877-884, Jul. 2005.

[25] O. Vainio, S. J. Ovaska, and M. Polla, "Adaptive Filtering Using Multiplicative General Parameters for Zero-Crossing Detection," *IEEE Tran. Ind. Electron.*, vol. 50, no. 6, pp. 1340-1342, Dec. 2003.

[26] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584-592, Mar. 2007.

[27] P. Rodriguez, R. Teodorescu, I. Candela, , A. V. Timbus, , M. Liserre, and F. Blaabjerg, "New Positive-Sequence Voltage Detector for Grid Synchronization of Power Converters under Faulty Grid Conditions," *In Proceedings of the IEEE Power Electronics Special Conference (PESC'06)*, June 2006, pp. 1-7.

[28] F. M. Gardner, *Phaselock Techniques*, 3rd ed. Hoboken, NJ: Wiley, 2005.

[29] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1067-1080, April 2011.

[30] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of Phase-Locked Loops for Power Converters Under Distorted Utility Conditions," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2039-2047, Dec. 2009.

[31] C. H. Ng, K. Busawon, G. A. Putrus and L. Ran, "Fast-Individual-Harmonic-Extraction Technique," *IEE Proc.-Gener. Transm. Distrib.*, vol. 152, no. 4, pp. 556-562, Jul. 2005.

[32] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58-63, Jan./Feb. 1997.

[33] H. Awad, J. Svensson, and M. J. Bollen, "Tuning software phase-locked loop for series-connected converters," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 300-308, Jan. 2005.

[34] F. D. Freijedo, A. G. Yepes, O. Lopez, A. Vidal, and J. Doval-Gandoy, "Three-phase PLLs with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 85-97, Jan. 2011.

[35] F. D. Freijedo, "Contributions to Grid-Synchronization Techniques for Power Electronic Converter," Phd thesis, Vigo University, June 2009.

[36] S. Preitl and R.-E. Precup, "An extension of tuning relations after symmetrical optimum method for PI and PID controller," *Automatica*, vol. 35, no. 10, pp. 1731-1736, Oct. 1999.

[37] R. C. Dorf and R. H. Bishop, *Modern Control Systems*, 9th ed. Englewood Cliffs, NJ: Prentice-Hall, 2000.

[38] *Voltage characteristics of electricity supplied by public distribution systems*, European Standard EN 50160.

[39] S. Subramanian, and M. K. Mishra, "Interphase AC-AC topology for voltage sag supporter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 514-518, Feb. 2010.

[40] J. Dai, D. Xu, B. Wu, and N. R. Zargari, "Unified DC-link current control for low-voltage ride-through in current-source-converter-based wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 288-297, Jan. 2011.

[41] *IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources With Electric Power Systems*, IEEE Std. 1547.1-2005, Jul. 2005.

[42] *Inverters, Converters, and Controllers for Use in Independent Power Systems*, UL Std. 1741, Jun. 2002.

[43] *Photovoltaic (PV) Systems-Characteristics of the utility interface*, IEC 61727, Dec. 2004.

[44] M. Karimi-Ghartemani, and H. Karimi, "Processing of Symmetrical Components in Time Domain," *IEEE Trans. Power Sys.*, vol. 22, no. 2, pp. 572-579, May 2007.

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