Modulation Methods for Neutral-Point-Clamped Wind Power Converter Achieving Loss and Thermal Redistribution under Low-Voltage-Ride-Through

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***Abstract* - The three-level neutral-point-clamped (3L-NPC) converter is a promising multilevel topology in the application of mega-watts wind power generation system. However, the growing requirements by grid codes may impose high stress and even give reliability problem to this converter topology. This paper investigates the loss and thermal performances of a 10 MW 3L-NPC wind power inverter undergoing Low Voltage Ride Through (LVRT) operation. A series of new space vector modulation methods are then proposed to relocate the thermal loading among the power switching devices. It is concluded that, with the proposed modulation methods, the thermal distribution in the 3L-NPC wind power inverter undergoing LVRT becomes more equal, and the junction temperature of the most stressed devices can be also relieved. Also the control ability of DC-bus neutral point potential, which is one of the crucial considerations for the 3L-NPC converter, is even more improved by the proposed modulation methods.[1]**

I. INTRODUCTION

The European Union is committed to source 20% of its energy from renewables by 2020 [1]. As the most promising candidate, the wind energy production integrated into the power grid is booming all over the world. Meanwhile, the power capacity of a single wind turbine is increasing continuously to reduce the price pr. produced kWh, as the cutting-edge achievement, 7 MW offshore wind turbines have already been presented on the market [2]-[5]. Consequently, due to much more significant impacts to the power grid after a failure or disconnection than ever before, the wind power generation system is required to be more reliable and able to withstand grid disturbances. The Transmission System Operators (TSO) have issued stricter Low Voltage Ride Through (LVRT) grid codes [6], moreover, it is becoming a need that the wind power generation system should also provide reactive current (up to 100% rated current capacity of converter) to contribute to the grid recovery when LVRT is present [7]. A lot of work has been done related to the control of the wind power converter to satisfy the grid codes during LVRT [8], [9]. However, the loss and thermal performances under this condition, especially when using MW full-scale power converters, are important and interesting topics needed to be clarified.

It is expected that 10 MW wind turbines with PMSG and full-scale power converter will be the next long-term target to be conquered according to the technology trends [2]-[5]. In most cases, the multi-level converter topologies will be demanded to handle such a high power with medium voltage ratings [10]-[17]. As the most commercialized multilevel converter [12]-[17], three-level neutral-point-clamped (3L-NPC) topology seems to be a promising candidate for the 10 MW full-scale wind power converter [18]-[20], as shown in Fig. 1, where T_{out} is the outer switch, D_{out} is the outer freewheeling diode, T_{in} is the inner switch, D_{in} is the inner freewheeling diode, D_{npc} is the clamping diode.

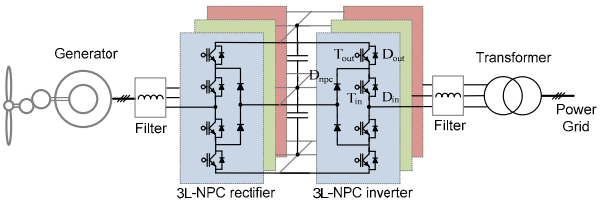

Fig. 1. Three-level neutral point clamped converter used in a wind turbine.

One drawback of 3L-NPC converter is the unequal loss distribution among the inner switches T_{in} and D_{in}, the outer switches T_{out}/D_{out} and the neutral point clamped (NPC) diodes D_{npc}, as indicated in Fig. 1. The inefficient and unequal utilization of power devices may limit the maximum achievable power, switching frequency and reliability of the whole converter system. Some works are proposed to improve this drawback with two-level modulation at lower modulation index [21], [22] or active neutral point clamped (NPC) switches [15]-[17]. But they have the disadvantages of either poorer control ability of neutral point potential or extra power switching devices. In [23] a modulation sequence is proposed to relieve the device thermal stress under LVRT, but it introduces extra switching events and the neutral point control method will compromise the thermal relieving effects. The problems of 3L-NPC converter may

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raise the uncertainty and restrict the availability of this converter topology in the application of wind turbines.

In this paper, the loss and thermal distribution among the power semiconductors of three-level neutral-point-clamped (3L-NPC) inverter are first investigated, the analysis is focusing on the application of 10 MW wind turbines which is undergoing the low voltage ride through (LVRT) condition. Afterwards a series of new space-vector-modulation sequences which aim to reduce the stress of the "hottest" power devices and more equal thermal distribution are proposed. The neutral point (NP) potential control performances for the proposed modulation methods are also evaluated.

II. Thermal Distributions of 3L-NPC Inverter under LVRT

A 10 MW medium-voltage 3L-NPC wind power inverter is basically designed for a case study. As summarized in Table I, all of the power devices have the commutated voltage of 2.8 kV in order to utilize the dominant 4.5 kV high-power semiconductors available on the market, and the rated DC bus voltage can be determined at 5.6 kV. Normal continuous Space Vector Modulation (SVM) method for 3L-NPC converter is applied and the carrier frequency is typically designed to be 800 Hz in order to get an acceptable switching loss in the power devices. The output filter inductance is designed to limit the maximum current ripple to 25% of the rated current amplitude, and the filter capacitance is not taken into account. For simplicity of analysis and keep the analysis focus on the power loss and thermal behavior of the power semiconductors, the power grid is considered as three ideal AC voltage sources, the DC bus capacitance is assumed high, and the transformers are assumed ideal.

The simulations are carried out based on PLECS Blockset in Simulink software [24], press-pack IGCT 5SHY 40L4511 from ABB (commutated voltage 2.8 kV/ maximum 3.6 kA, optimized for medium frequency switching) and freewheeling diodes 5SDF 10H4503 (2.8 kV/ maximum 4 kA, recommended by the manufacturer) are chosen as the switching devices in this case study.

Table I. Parameters of a 10 MW 3L-NPC wind power inverter for case study (rated condition).

Rated output active power P_o	10 *MW*
DC bus voltage V_{dc}	5.6 *kV DC*
*Rated primary side voltage V_p	3.3 *kV rms*
Rated line-to-line grid voltage V_g	20 *kV rms*
Rated phase current I_{phase}	1750 *A rms*
Carrier frequency f_c	800 *Hz*
Filter inductance L_f	1.13 *mH* (0.2 *p.u.*)

* Line-to-line voltage in the primary windings of transformer.

As an extreme example, the inverter is set under the LVRT condition, when the grid voltage dips to 0.05 p.u. providing 100% rated reactive current to the power grid according to [7]. Because of the action of a DC bus chopper, the DC bus voltage during LVRT is assumed to be maintained at 10% higher than the rated value. The simulation output of the 3L-NPC inverter with normal Space Vector Modulation (SVM) sequence in two fundamental cycles is shown in Fig. 2. It can be seen that the output features of the converter during LVRT are quite different from the normal operation: the zero voltage level has longer dwelling time compared to the positive and negative voltage levels because of relative lower modulation index. The phase current lags 90 degree to the grid phase voltage because the inverter achieves 100% rated reactive current injection (1.75 kA rms) into the power grid.

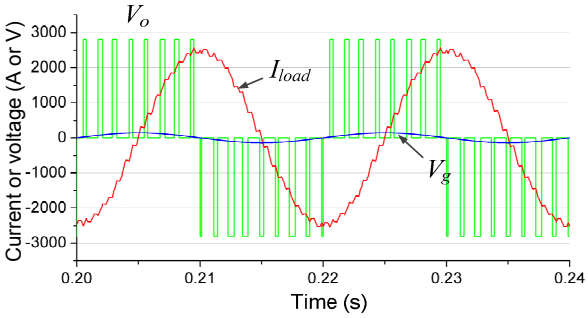


Fig. 2. Simulation outputs of 3L-NPC inverter with normal space vector modulation, (V_o-output voltage pulses, V_g-grid voltage, I_{load}-phase current. V_g=0.05 p.u., 100% rated reactive current).

When the operating condition for 3L-NPC wind power inverter is settled, the loss model can be applied based on the current and voltage information in the power devices. Afterwards the thermal model is applied to the loss dissipation, and junction temperature of each power device in 3L-NPC inverter can thereby be acquired. The loss model shares the same idea as in [24],[25], which is a commonly accepted method for the loss evaluation of power semiconductor devices. The thermal models of a single switch and clamping diode are indicated in Fig. 3 [26], [27], in which the thermal impedance from junction to case $Z_{(j\text{-}c)}$ is modeled as a four-layers Foster RC network, as shown in Fig. 4, and it has to be transferred to the equivalent Cauer network for simulation [24]. Each of the thermal parameters can be found from the manufacturer datasheets and they are summarized in Table II, where the thermal resistance R_{th} will decide the steady state level of junction temperature, and the time constant τ (decided by R_{th} and thermal capacitance C_{th}) will decide the dynamic performance of the junction temperature, their relationship is governed by [24]:

$$\tau = R_{th} \cdot C_{th} \tag{1}$$

It is noted that the Foster thermal network will be automatically transferred to the equivalent Cauer RC network in PLECS for the convenience of extending thermal impedance from case to ambient [24]. Due to the normally

large thermal capacitance, the heat sink temperature is set to be 60 ℃ and considered constant during the converter operation. However it may be changed depending on the operation site.

The steady state mean junction temperature of each power device can be calculated as follows according to [26]:

$$T_{jIGCT/Diode} = T_H + P_{IGCT/Diode} \cdot (R_{th(j-c)} + R_{th(c-h)}) \qquad (2)$$

$T_{jIGCT/Diode}$ and $P_{IGCT/Diode}$ represent the junction temperature and the total loss in a single IGCT or diode respectively, T_H is the heat sink temperature, $R_{th(j-c)}$ is the thermal resistance of IGCT or Diode from junction to case, $R_{th(c-h)}$ is the thermal resistance of IGCT or Diode from case to heat sink.

The junction temperature distribution for each power device with relation to the grid voltage is shown in Fig. 5, in which the situations that the inverter needs to provide 100% rated reactive current are indicated. It can be seen that the

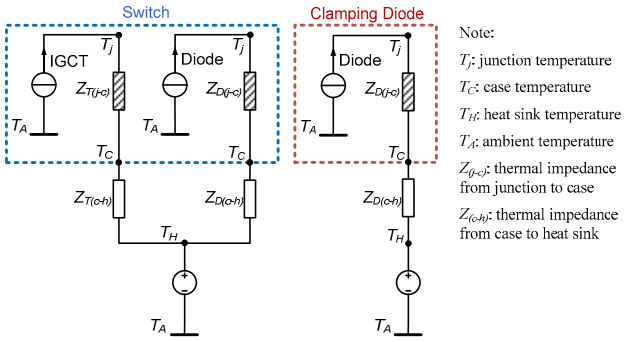


Fig. 3. Thermal models of the used power devices.

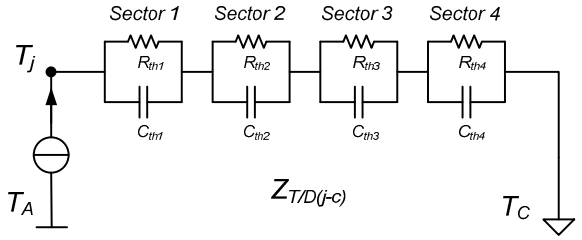


Fig. 4. Thermal model of the impedance $Z_{T(j-c)}$ or $Z_{D(j-c)}$ from junction to case in Fig. 3. (It has to be transferred to equivalent Cauer network for simulation).

Table II: Parameters of thermal impedance for IGCT/diode.

Thermal Impedance	$Z_{T/D(j-c)}$				$Z_{T/D(c-h)}$
	Sector 1	Sector 2	Sector 3	Sector 4	
R_{iIGCT} (K/kW)	5.562	1.527	0.868	0.545	3
τ_{iIGCT} (s)	0.5119	0.896	0.0091	0.0024	-
R_{iDiode} (K/kW)	7.705	2.748	1.009	0.539	3
τ_{iDiode} (s)	0.5244	0.0633	0.0065	0.0015	-

*Sector 1-4 means different layers of RC lump circuit in Fig. 4.

thermal distribution of 3L-NPC inverter under LVRT is quite unequal and inefficient: as the "hottest" power devices, the NPC diodes D_{npc} and inner switch T_{in} has 15 K to 25 K higher junction temperatures than the average level of all power devices at around 80 ℃. While the most "cold" device D_{in} is barely loaded and has up to 40 K lower junction temperature than the "hottest" device D_{npc}. The extreme unequal thermal distribution happens when the grid voltage dips close to zero. It is obvious that the thermal optimization target for 3L-NPC wind power inverter under LVRT is to reduce the junction temperature in the NPC diodes D_{npc} and

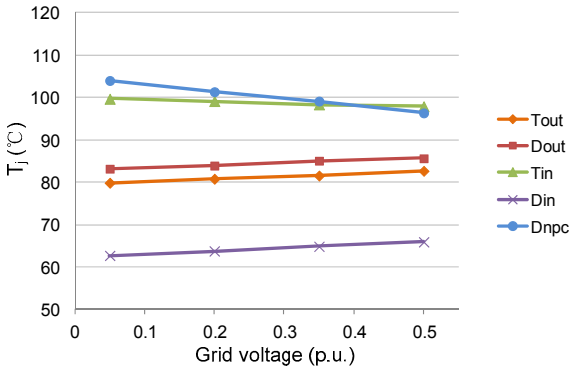
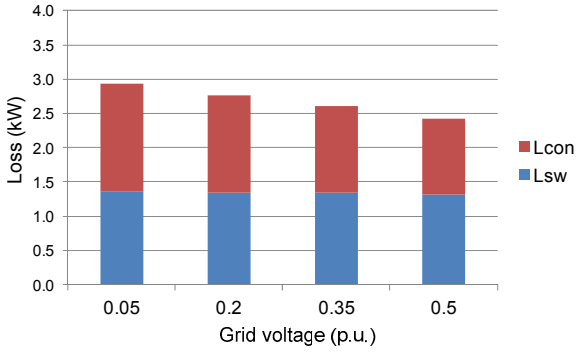
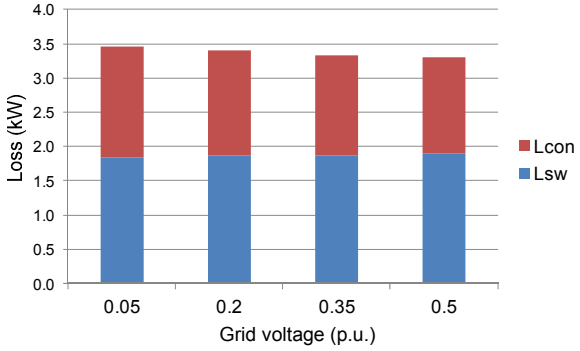


Fig. 5 Thermal distribution vs. grid voltage during Low Voltage Ride Through (100% reactive power is needed).



(a) Clamping diode Dnpc.



(b) Inner switch Tin.

Fig. 6. Loss distribution of the 3L-NPC wind power inverter under LVRT (Lcon conduction loss, Lsw switching loss).

the inner switch T_{in}, while at the same time to achieve a more equal junction temperature distribution.

The loss distribution of the clamping diode D_{npc} and inner switch T_{in} in 3L-NPC inverter when grid voltage dips to 0.05, 0.2, 0.35 and 0.5 p.u. is shown in Fig. 6 (a) and Fig. 6 (b). It can be seen that the conduction loss in the NPC diode is slightly more dominant while the switching loss in T_{in} is more dominant. Referring to the switching process of the 3L-NPC converter [21], the thermal stress in D_{npc} and T_{in} will be effectively relieved by reducing the dwelling time of zero voltage level (reduced conduction loss) and reducing the commutations involving zero voltage level (reduced switching loss).

When implementing the space vector modulation for 3L-NPC inverter, the reference vector under extreme LVRT is mainly located in the inner hexagon of space vector diagram. In this special area, there are one or two redundancies for each of the switching state. The switching state redundancy enables quite a lot of possibilities to arrange the "three-nearest" state vectors - it is possible that some of the state vectors sequence could modify the loss distribution and achieve the thermal optimization target for the 3L-NPC wind power inverter under LVRT.

III. Generation Method for Space Vector Modulation Sequences

For simplicity, the sequence generation method is demonstrated only based on sector I (0-60 degree) in the space vector diagram for 3L-NPC converter, and other sectors will share similar analysis. The detailed information of sector I is shown in Fig. 7, in which each of the state vectors group and sub-regions (A-D) are illustrated. As mentioned before, the voltage reference vector $\boldsymbol{V_{ref}}$ in this sector mainly locates in region A under extreme LVRT condition. The reference can be synthesized by the three nearest state vectors: one from the redundant short vectors group ***211/100*** (red), one from the other redundant short vectors group ***221/110*** (blue) and one from the redundant zero vectors group ***000/111/222*** (black). The numbering "2", "1", "0" of the state vectors represent that a certain phase is connected by the converter to the positive DC bus, the neutral point and the negative DC bus respectively [21], [28]-[30].

It is interesting that when using all of the state vectors including the redundant ones in region A to synthesize the reference vector $\boldsymbol{V_{ref}}$, the sequence arrangement is unique if the least switching process and symmetric pulses for each phase are realized, as shown in Fig. 8. All of the state vectors in region A are visited without unnecessary switching processes and abrupt voltage level changes: Output voltage level in each phase gradually change from negative to zero and then from zero to positive (reverse fashion is from positive to zero and then to negative). Other applicable modulation sequences can be generated by eliminating some redundant state vectors in the "complete" vector sequence.

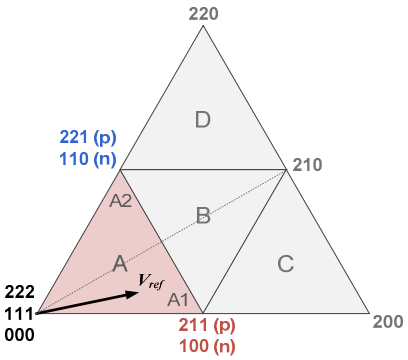


Fig. 7. Sector I of the space vector diagram for 3L-NPC converter.

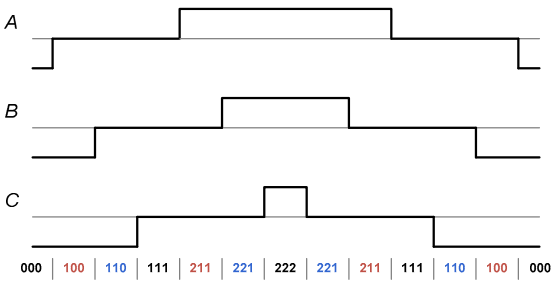
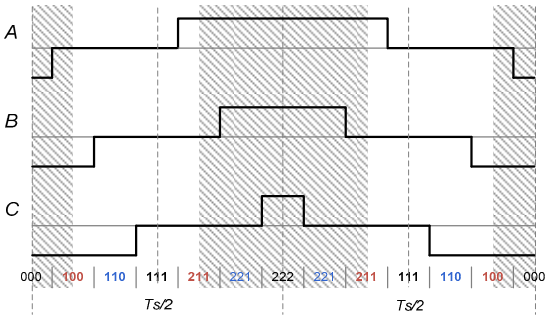
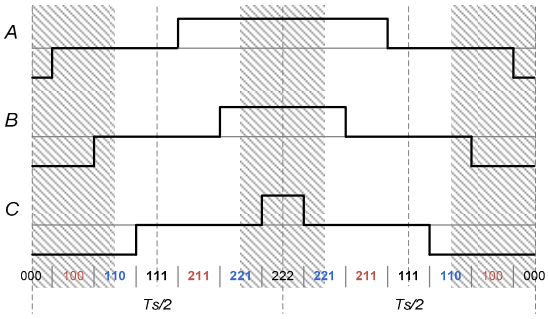


Fig. 8. The "complete" vector sequence in region A.



(a) Region A1 (0-30 degree)



(b) Region A2 (30-60 degree)

Fig. 9. Vector sequences for normal space vector modulation, (grey parts mean eliminated state vectors, region A, sector I).

However, the sequence generation method must follow two criteria:

I. At least one state vector from each of the "three nearest" redundant vectors group has to be used in order to synthesize the desired reference voltage.

II. The state vectors have to be arranged in reverse fashion over one carrier cycle in order to smoothly connect with the succeeded vector sequence without extra switching processes.

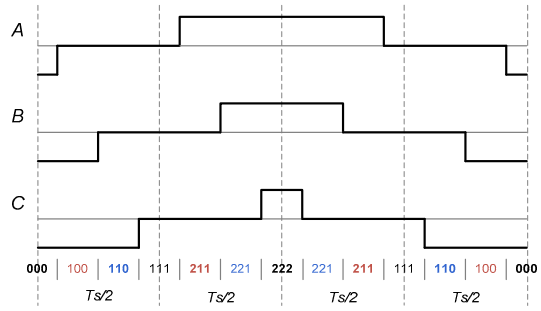
An example of this vector sequence generation method is demonstrated in Fig. 9, in which the most commonly used SVM sequence (normal) for 3L-NPC converters in the region A1 (0-30 degree) and region A2 (30-60 degree) of sector I are generated. It is noted that the grey blocks in Fig. 9 indicate the eliminated redundant state vectors, and the used state vectors are arranged within one switching cycle. It can be seen that the two sequence generation criteria are satisfied.

IV. Thermal Redistributed Modulations for 3L-NPC Inverter under LVRT

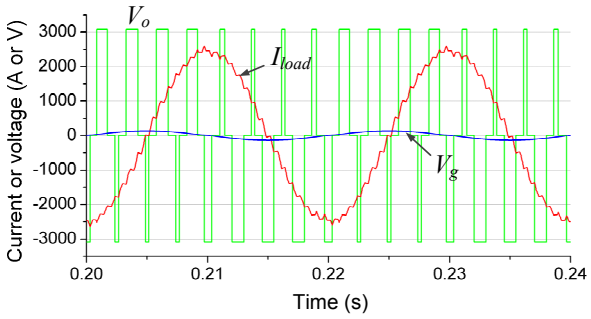
4.1 Basic principles

As mentioned before, the thermal optimized modulation target is to reduce the dwelling time of zero voltage level or decrease the commutations involving zero voltage level. Based on the proposed generation method for modulation sequence, a series special modulation sequences are of interest:

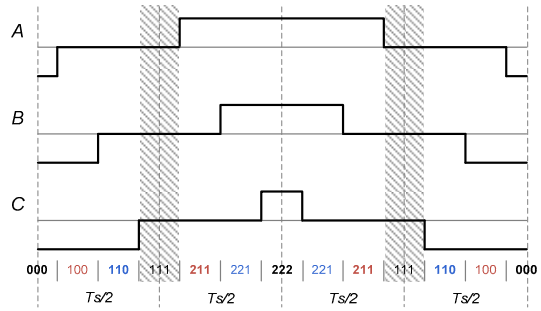
In order to reduce the output time for zero voltage level of 3L-NPC inverter during LVRT, one effective way is to reduce the activating time for the zero state vector "***111***" (because vector ***111*** outputs zero voltage level for all of the three phases). Fig. 10 (a) indicates a special modulation sequence which allocates the "complete" vectors of Fig. 8 within two switching cycles, it is called Optimized sequence



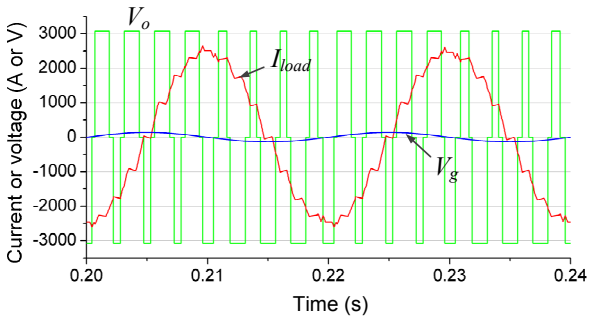
(a) O1 sequence arrangement



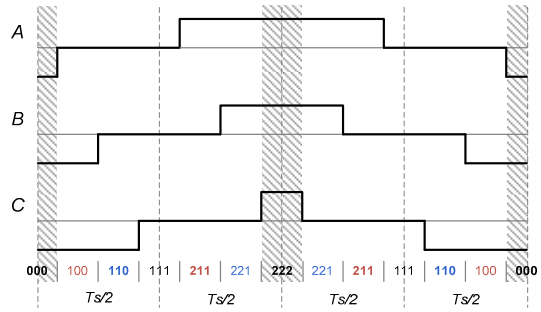
(b) Output of O1 sequence



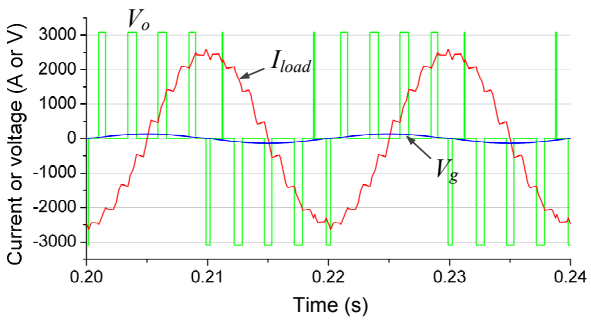
(c) O2 sequence arrangement



(d) Output of O2 sequence

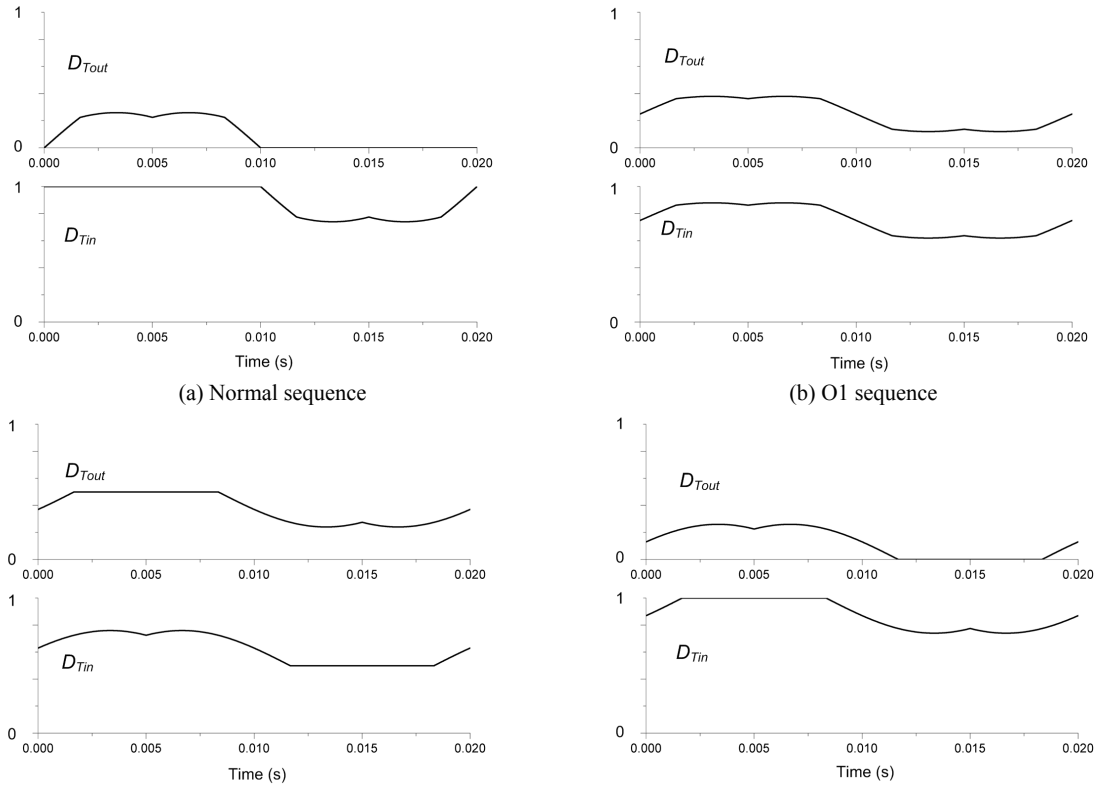


(e) O3 sequence arrangement



(f) Output of O3 sequence

Fig. 10. The loss and thermal redistributed modulation schemes. (V_o-output voltage pulses, V_g-grid voltage, I_{load}-phase current. V_g=0.05 p.u., 100% rated reactive current).



(a) Normal sequence

(b) O1 sequence

(c) O2 sequence

(d) O3 sequence

Fig. 11. SVM sequences in the form of carried-based modulation refences (duty ratio for the inner switch S1 and outer switch S2).

1 (O1) for convenience. In the normal SVM sequence shown in Fig. 9, the dwelling time for zero vector is all occupied by ***111***, while in the O1 sequence the zero vector is shared by ***000***, ***111*** and ***222***, that means the output time for ***111*** in the O1 sequence is reduced and partly replaced by the equivalent vectors ***000*** and ***222***. The output waveforms of the O1 sequence are shown in Fig 10 (b), it can be seen that the output voltage of this modulation sequence alternates between positive, zero, negative voltage levels within neighboring switching cycles, which is quite different from the traditional three-level output pattern of 3L-NPC converter as indicated in Fig. 2. But the amplitude and phase angle of the load current is kept unchanged.

Another direct and basic idea is trying to avoid using the state vector "***111***" based on the "complete" sequence, as shown in Fig. 10 (c) which is called Optimized sequence 2 (O2) for convenience. It can be seen that the sequence generation criteria are satisfied and the zero state vectors ***111*** are totally replaced by the equivalent state vectors ***000*** and ***222***. The output waveforms of the O2 sequence are shown in Fig. 10 (d), in which the widths of both positive and negative output voltage pulses are expanded compared to the O1 sequence - that means further reduced dwelling time for zero voltage level.

In order to reduce the commutations involving zero voltage level, the third modulation sequence is generated in Fig. 10 (e), which eliminates the zero state vectors ***000*** and ***222*** and is called Optimized sequence 3 (O3) for convenience. It can be seen that for O3 sequence the commutations from zero to positive voltage levels in phase C and commutations from zero to negative voltage level in phase A are avoided in sector I (0-60 degree). The decreasing commutation times will benefit the switching loss reduction in the 3L-NPC inverter during LVRT. The output waveforms of the O3 sequence are shown in Fig. 10 (f), in which there are less output voltage pulses compared to the O1 and O2 sequence - that means reduced commutation times and less switching loss in D_{npc} and T_{in}.

It is noticed that because there is redundancy for each of the state vector, all the used vectors in the proposed sequences are arranged within two switching cycles rather than one, as indicated at the bottom of Fig. 10 (a), Fig. 10 (c), Fig. 10 (e) respectively. As a result, compared to the normal sequence, the equivalent switching frequency in the proposed sequences is not further increased especially for O1 and O2.

For better understanding the proposed space vector modulation sequences in the form of carried-based modulation, they are transferred to the voltage references/duty ratio for the inner and outer switches of 3L-NPC converter, as shown by D_{Tout} and D_{Tin} in Fig. 11. It can be seen that compared to the normal sequence in Fig. 11 (a), the O1 and O2 sequence generally move the level of voltage references, introducing larger duty ratio for the outer switch and smaller duty ratio for the inner switch, - this will lead to the longer dwelling time for the positive/negative voltage

output and reduce the dwelling time of the zero voltage output. In respect to the O3 sequence, the duty ratio is very similar to the normal sequence but deviation can be found around the time for zero crossing of voltage reference - this means the dwelling time for zero voltage output is not significantly reduced. The O3 sequence is very similar to the modulation sequence proposed by [31], [32].

4.2 Neutral point potential control and Total Harmonic Distortion

In order to analyze the control ability of Neutral Point (NP) potential by the proposed modulation sequence, the neutral point current i_{NP} which is the main reason for the DC bus unbalance will be focused. The used state vectors and their corresponding i_{NP} for each of the modulation sequence are summarized in Table III. It can be seen that under the ideal condition, all of the proposed sequences will utilize the short vectors having zero accumulated i_{NP} over a switching cycle. The difference is only for the zero vectors which have no impact to the NP current. Therefore the positive and negative DC bus can naturally be balanced in the proposed three sequences without any active methods.

In case of non-ideal situations, e.g. unbalanced load, the i_{NP} will be disturbed in the 3L-NPC converter. It is well known that for the normal SVM sequence the average i_{NP} can be controlled at zero by adjusting the time proportion of redundant vectors [33]-[35]. However according to Table III, in the normal sequence only one short vector (short 1) has redundancy and the other (short 2) doesn't, therefore the NP current control ability is limited by just half control freedom, It is also proven in [33] that the NP potential control can be only effective under certain power factors and modulation indexes. As for the proposed three sequences O1, O2, O3, both of the used short vectors have redundancies, which mean full control freedom for the NP current, therefore it is possible to achieve zero i_{NP} within one switching cycle under all power factors and applicable modulation indexes. Consequently the NP potential control ability of all the proposed modulation sequences should be better than the normal SVM sequence.

Nevertheless, the proposed modulation sequences especially for O2 and O3 have no Total Harmonic Distortion (THD) improvements compared to the normal sequence. This can be also observed from the load current waveforms in Fig. 10 (d) and Fig. 10 (f), where the current distortion in the O2, O3 sequences are actually more than that in the normal sequence of Fig. 2. However it is noted that under the LVRT operation, which is an abnormal condition and normally last up to few seconds, the first control target is to make the grid converter survive when withstanding the grid voltage dips and providing large amount of reactive power support, therefore under the LVRT, THD is relatively less important performance for the wind power converter.

4.3 Loss and thermal performances

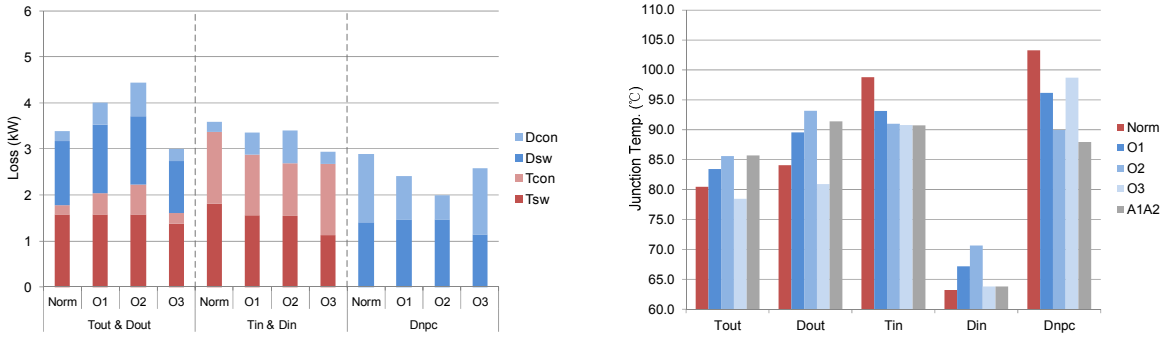
The loss distributions of the 3L-NPC wind power converter under LVRT when utilizing the normal and optimized vector sequences are compared in Fig. 12 (a), where D_{con} and T_{con} are the conduction loss in diode and IGCT respectively, D_{sw} and T_{sw} are the switching loss in diode and IGCT respectively. The comparison of steady state mean junction temperature distribution is shown in Fig. 12 (b), where the optimized sequence enabling i_{NP} balance proposed in [23] is also indicated for comparison (called

Table III. The used vectors and neutral point current in sector I-III for different sequences within one switching cycle

Sectors	Vector types	O1		O2		O3		Normal (0-30°)	
		Used vectors	i_{NP}	Used vectors	i_{NP}	Used vectors	i_{NP}	Used vectors	i_{NP}
I	Short 1	**211**	$-i_a$	**211**	$-i_a$	**211**	$-i_a$	**211**	$-i_a$
		100	i_a	**100**	i_a	**100**	i_a	**100**	i_a
	Short 2	**110**	$-i_c$	**110**	$-i_c$	**110**	$-i_c$	**110**	$-i_c$
		221	i_c	**221**	i_c	**221**	i_c		
	Zero	**000 111 222**	*0*	**000 222**	*0*	**111**	*0*	**111**	*0*
II	Short 1	**121**	$-i_b$	**121**	$-i_b$	**121**	$-i_b$	**121**	$-i_b$
		010	i_b	**010**	i_b	**010**	i_b		
	Short 2	**110**	$-i_c$	**110**	$-i_c$	**110**	$-i_c$	**110**	$-i_c$
		221	i_c	**221**	i_c	**221**	i_c	**221**	i_c
	Zero	**000 111 222**	*0*	**000 222**	*0*	**111**	*0*	**111**	*0*
III	Short 1	**121**	$-i_b$	**121**	$-i_b$	**121**	$-i_b$	**121**	$-i_b$
		010	i_b	**010**	i_b	**010**	i_b	**010**	i_b
	Short 2	**011**	$-i_a$	**011**	$-i_a$	**011**	$-i_a$	**011**	$-i_a$
		122	i_a	**122**	i_a	**122**	i_a		
	Zero	**000/111/222**	*0*	**000/222**	*0*	**111**	*0*	**111**	*0*

A1A2 for simplicity). It can be seen that, the optimized sequences O1, O2 and O3 all achieve the loss and thermal redistribution among the power devices, the stress of D_{npc} and T_{in} can be relieved under LVRT operation. The mean junction temperature reduction in the most stressed device D_{npc} and T_{in} are estimated to be up to 12 K and 8 K respectively when O2 modulation is applied. And O3 sequence shows another advantage in reducing the stress in T_{out} and D_{out} by 3 K and 5 K respectively. It is noted that the optimized sequence A1A2 in [23] has the similar thermal distribution as O2.

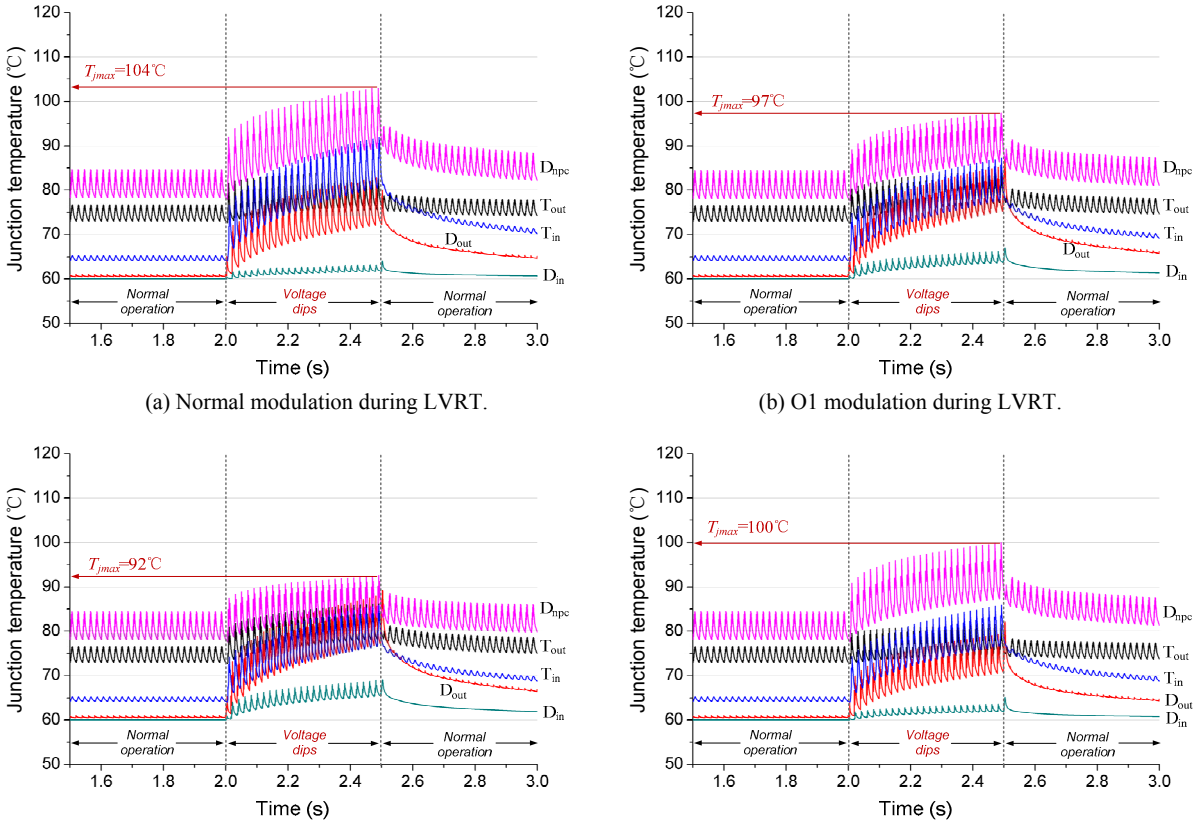
The dynamic thermal performance of 3L-NPC wind power inverter which goes from normal operation to extreme LVRT and then back to normal operation can also be simulated. The junction temperature of each power device when applying different modulation methods during LVRT is shown in Fig. 13. If the O1 and O2 modulation methods are applied, as shown in Fig. 13 (b) and Fig. 13 (c), the



(a) Loss distribution.

(b) Mean junction temperature comparison.

Fig. 12. Thermal and loss comparison for the 3L-NPC wind power inverter under LVRT for different modulation sequences, V_g=0.05 p.u., 100% reactive power.



(a) Normal modulation during LVRT.

(b) O1 modulation during LVRT.

(c) O2 modulation during LVRT.

(d) O3 modulation during LVRT.

Fig. 13. Junction temperature dynamic response with a voltage dip time of 500 ms of different modulation sequences (from normal operation with wind speed 8 m/s to 0.05 p.u. LVRT, and then back to normal operation).

Table IV: Parameters for the experimental setup of 3L-NPC converter.

DC bus voltage V_{dc}	200 V
Modulation index m	0.3
Switching frequency f_s	2 kHz
Fundamental frequency f_o	50 Hz
Load inductance L_{load}	28 mH
Load resistance R_{load}	1.2 Ω
Maximum load current i_{loadM}	3.5 A
Phase angle θ	80 °

maximum junction temperature in D_{npc} and T_{in} are both reduced compared to the normal modulation in Fig. 13 (a). While the O3 modulation sequence shows more ability to reduce the junction temperature in T_{out} and D_{out} compared to O1 and O2 modulation methods.

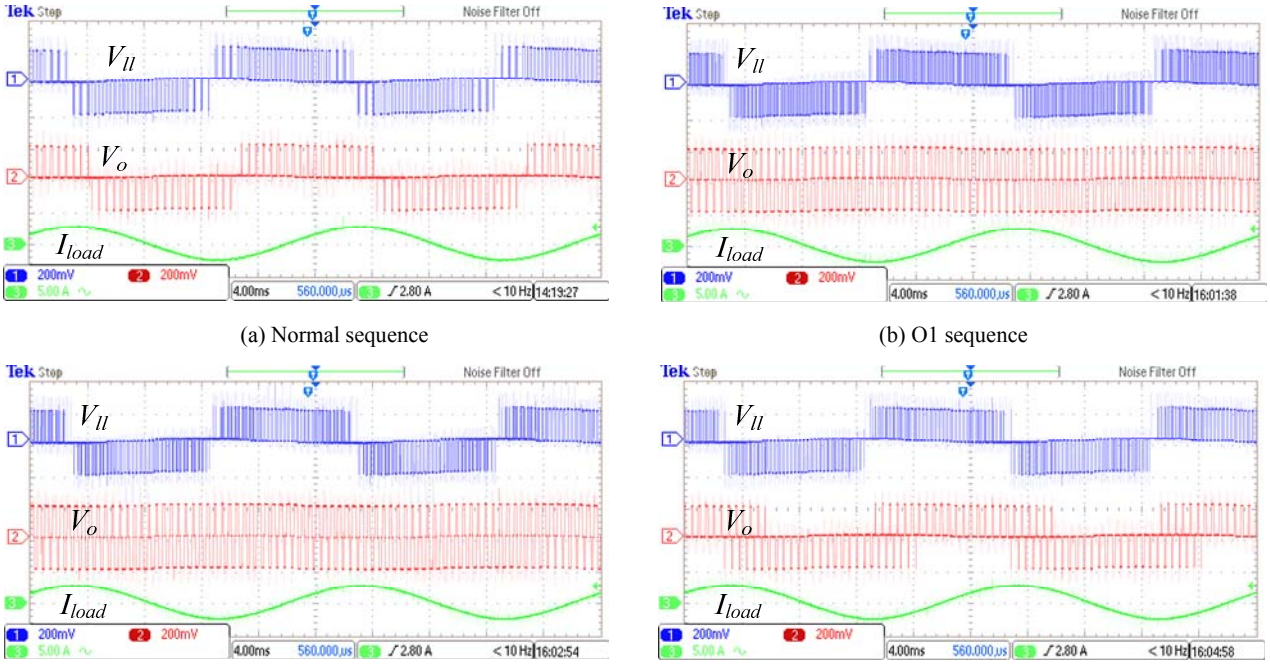
The optimal sequence in respect to the thermal redistribution under LVRT depends on many factors like the voltage/power level, switching frequency, heat sink design and the used power switching devices [36]. Generally speaking O2 sequence shows better thermal performance where the conduction loss is dominant, like the application with high power and low switching frequency. While O3 sequence may show better thermal performance if the switching loss is dominant like the application with low power and high switching frequency. However the preferred modulation sequence under LVRT should be evaluated case by case.

It is noted that, the proposed sequences are trying to move the loss from the most stressed devices to the less stressed ones. Although the total loss in the devices might not be significantly reduced, but the loss distribution is more equal, and the maximum junction temperature of the most devices can be reduced during LVRT. The more equal thermal distribution and maximum temperature limitation can be also observed from the dynamic thermal change in Fig. 13. The resulting maximum junction temperature reduction in the most stressed power devices may contribute to a life time extension of the converter according to e.g. the important Coffin-Masson life time model [37].

V. Experimental Results

The proposed modulation sequences are validated on a downscale 3L-NPC converter, whose parameters are indicated in Table IV. It can be seen that a special *RL* passive load is used to simulate the LVRT operating condition for the grid-connected converter with large amount of reactive power (θ=80º) and low modulation index (m=0.3).

Based on the setup the converter outputs with different modulation sequences are shown in Fig. 14, where the line to line voltage pulses (blue), phase voltage pulses (red), and load current (green) are indicated respectively. It can be seen that the different modulation sequences can achieve the



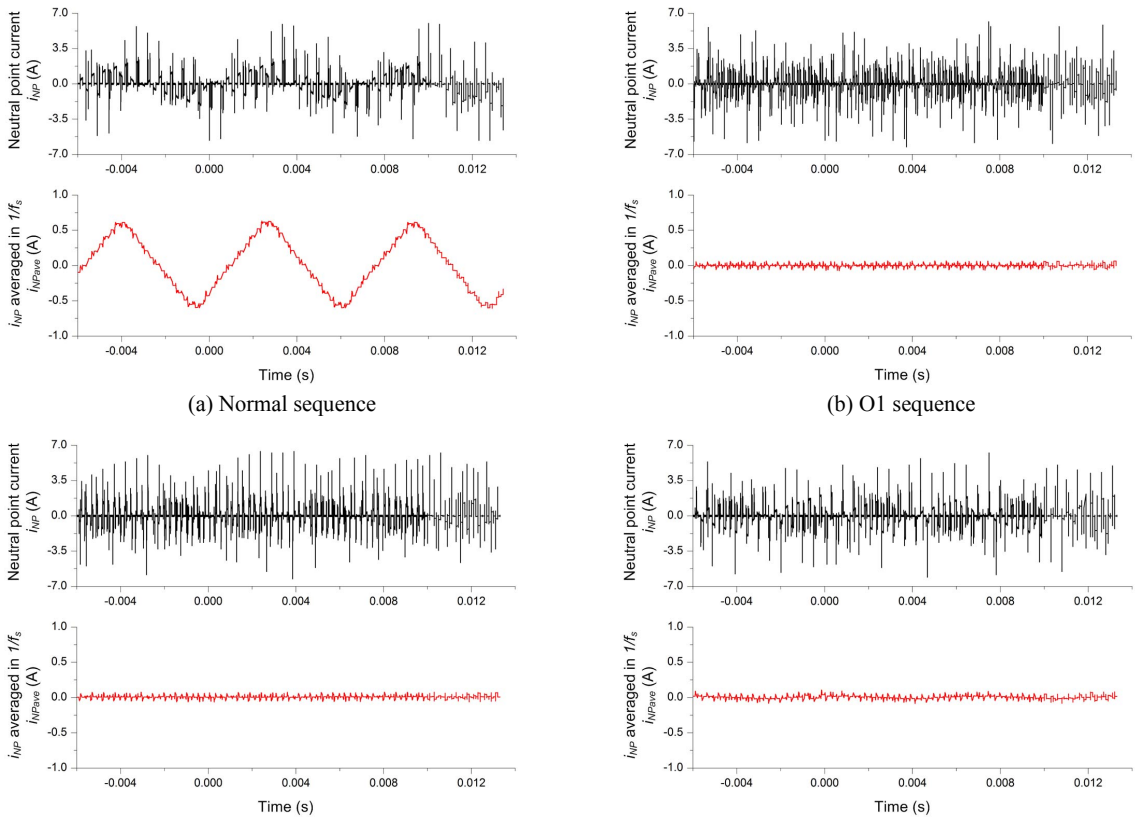
(a) Normal sequence

(b) O1 sequence

(c) O2 sequence

(d) O3 sequence

Fig. 14. Experimental outputs of different modulation sequences, V_{ll}-line to line voltage pulses (100V/div), V_o-phase voltage pulses (100V/div), I_{load}-load current (5A/div), modulation index M=0.3 p.u., phase angle θ=80º.



(a) Normal sequence

(b) O1 sequence

(c) O2 sequence

(d) O3 sequence

Fig. 15. Experimental neutral point current i_{NP} and its switching-cycle-averaged value i_{NPave} in different modulation sequences.

similar line-to-line voltage and load current, but the phase voltage are significantly different when various modulation sequences are applied, this agrees with the simulation results in Fig. 10.

Fig. 15 indicates the experimental NP current of the 3L-NPC converter when different modulation methods are applied, it is noted that the active NP current control is not active. For clarity, both the instantaneous neutral point current i_{NP} and its switching-cycle-averaged value i_{NPave} are indicated. It can be seen that the i_{NPave} in the proposed modulation sequences O1-O3 are almost eliminated, while the normal modulation sequence has acuminated-zero i_{NPavg} which oscillates at 0.2 p.u. amplitude and three times of the fundamental frequency.

VI. Conclusions

According to the investigations in this paper, the thermal optimization target for 3L-NPC wind power inverter under extreme LVRT is to reduce the junction temperature in the NPC diode and inner switch, which are the hottest power devices of the whole inverter system.

By the proposed insight generation method for modulation sequence of 3L-NPC inverter, it is possible to develop a series of different thermal optimized modulation sequences. Compared to the normal modulation, the proposed thermal redistributed modulation sequences, which all enable full neutral point potential control ability, can effectively reduce the dwelling time or commutations involving zero voltage level output, achieving more equal thermal distribution and reliving the hottest power devices under extreme LVRT operation of 3L-NPC inverter. The proposed thermal optimized modulation methods are especially feasible during the LVRT operation, where the modulation index is relative low and more redundant switching states can be utilized.

It is noted that the thermal improvements by the proposed modulation methods during LVRT depend a lot on the design of heat sink system and used power switching devices, which may change the thermal distribution and the loading level in the most stressed devices, as analyzed in [36]. Therefore, the preferred modulation sequences in respect to the thermal redistribution under LVRT need to be evaluated case by case.

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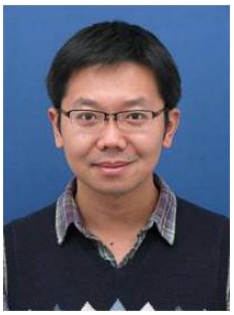

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