Open-Switch Fault Diagnosis and Fault Tolerant for Matrix Converter with Finite Control Set-Model Predictive Control

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***Abstract*—To improve the reliability of the matrix converter (MC), a fault diagnosis method to identify single open-switch fault is proposed in this paper. The introduced fault diagnosis method is based on finite control set-model predictive control (FCS-MPC), which employs a time-discrete model of the MC topology and a cost function to select the best switching state for the next sampling period. The proposed fault diagnosis method is realized by monitoring the load currents and judging the switching state to locate the faulty switch. Compared to the conventional modulation strategies such as carrier-based modulation method, indirect space vector modulation and optimum Alesina-Venturini, the FCS-MPC has known and unchanged switching state in a sampling period. It is simpler to diagnose the exact location of the open switch in MC with FCS-MPC. To achieve better quality of the output current under single open-switch fault conditions without any redundant hardware, a fault tolerant strategy based on predictive control is also studied. The fault tolerant strategy is to select the most appropriate switching state, associated with the remaining normal switches of the MC. Experiment results are presented to show the feasibility and effectiveness of the proposed fault diagnosis method and fault tolerant strategy.**

***Index Terms*—Fault diagnosis, fault tolerant, finite control set-model predictive control, matrix converter, open-switch fault.**

I. Introduction

MATRIX converter (MC) is a special power converter, which has many desirable features compared with the conventional AC/AC converter, such as bi-directional power flow and four-quadrant operation, sinusoidal input or output currents, alterable power factor, high power density and no DC-link elements [1], [2]. Thanks to these advantages, MCs have been applied in industrial fields such as military/civil aircrafts and electric vehicle applications with more electrically driven actuation systems [3], [4], which have special requirements for high-temperature operation, as well as space and weight savings. In addition, the highly reliable system operation even after some fault is also important [4]. As the reliability of power devices is very closely related to the reliability of overall power electronics systems [5], [6], there is a clear need to add fault diagnosis and fault tolerant capabilities to the MC as voltage-source inverters [6], [7]. For MC systems, great efforts have been made on topics like topologies and modulation strategies [8]-[13]. In comparison, studies on fault diagnosis and fault tolerant strategies are relatively less. Open circuit or short circuit fault of power devices are typical faults in the MC systems and can appear at any time. As a protection circuit is always installed in MC system, a fast fuse in series with each of the switches can be employed when a short circuit fault occurs, then a short circuit fault is changed into an open circuit fault.

With the aim to detect and locate open-switch fault in MC, two main solutions can be found in the literature. The first one is signal processing-based approach. In [14], a fault diagnosis method is implemented based on the discrete wavelet transform analysis of the measured output current waveform. However, the diagnosis strategy is too complex and time-consuming. The other one is the analytical model-based approach [15]. In [16]-[18], the differences between the measured and reference line-to-line voltages are used as the criterion for diagnosis. But it adds to system cost due to additional installation of voltage transducers besides the ones installed for control purposes. In [19], the faulty switch is identified with the information of the clamp current and the load current. However, an additional current sensor is needed to sample the clamp current. In [20], the faulty phase is identified by determining whether the load current is equal to zero, then the exact location of the open-switch is figured out by the second stage. In [21], the fault diagnosis method is developed for Alesina Venturini (AV). The diagnosis approach uses the information of the load currents, the angles of the input and output voltage space vectors, and the values of the duty-cycles of the switches. Although no extra hardware is needed for the fault diagnosis methods in [14], [20], [21], the detection time is too long. To reduce the detection time, a fault diagnosis method has been proposed [22], which is realized with knowledge about the switch state and the current

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sensor location. In [22], the current sensors are moved ahead of the clamp circuit connection to sample the converter currents during the zero vectors.

In recent years, the finite control set-model predictive control (FCS-MPC) has been applied for the control of power converters due to its several advantages, like fast dynamic response, easy inclusion of nonlinearities and constraints of the system, and the flexibility to include other system requirements in the controller [23]-[26]. The FCS-MPC method employs time-discrete models of the MC topology and a cost function to select the best switching state for the next sampling period. The fault diagnosis methods for conventional modulation strategies such as carrier-based modulation method [14], indirect space vector modulation [20] and optimum Alesina-Venturini [21], have been studied. But it has not been paid enough attention on the fault diagnosis for the MC with FCS-MPC. To enhance the reliability of MC with FCS-MPC, a fault diagnosis method to identify single open-switch fault is proposed in this paper.

Application of fault tolerant technique is one of major operations to increase the reliability of power electronic systems [27]. In the technical literature, two main fault tolerant solutions for the MC under open-switch fault have been studied. The first one is modifying and refactoring the MC topology by adding additional hardware to the converter [18], [19], [28], [29]. For this solution, the main drawback is that it adds to the system cost, complexity, and volume, and may not be applicable when the source/load neutral point is not accessible. The second one is modifying the modulation or control strategy with the remaining normal switches to operate the MC, without adding any extra devices. In [21], taking the faulty switch into account, the duty cycles of switching states are modified using the Alesina-Venturini method depend on the operating conditions of the converter and the time instant. In [30], the proposed fault tolerant strategies, which are based on the space vector modulation (SVM) method, replace the non-synthesizable vectors with the synthesizable ones. In [20], the fault tolerant method regards the MC as a two-stage rectifier and inverter circuit, and recomposes the control of rectifier stage to counteract the fault. The same fault tolerant method is used to counteract the double open-switch fault in [31]. Although these methods do not require any additional hardware or circuit reconfiguration, the optimal duty cycle of the switching state is not considered, which minimizes the error between the reference voltages and the actual voltages. In [32], the fault tolerant method obtains the optimize duty cycle of the switching state based on the Karush-Kuhn-Tucker (KKT) condition. However, the calculation process is too complex. In [33], the fault tolerant method based on FCS-MPC is proposed, which is easier to realize than the one in [32]. It selects the switching state which produces the minimum cost function value among the remaining eight switching states, but only the simulation result is given. In this paper, the fault tolerant strategy based on FCS-MPC is experimental verified and incorporated with the fault diagnosis method.

This paper is organized in the following manner. Section II presents the configuration and FCS-MPC strategy of MC system in normal operation. The performance in the presence of single open-switch fault is studied and a fault diagnosis method for MC with FCS-MPC is developed in section III. Section IV presents the fault tolerant strategy for MC with FCS-MPC. In section V, experiment results are presented to show the feasibility and effectiveness of the proposed methods.

II. MC System Description

A. Modeling of MC System

The matrix converter topology is illustrated in Fig. 1. It consists of nine bidirectional switches, each of which possesses the capability of bidirectional energy flow and connects a three phase voltage source to a three phase resistance-inductance load. An input filter is connected between the mains and the converter for avoiding high harmonic distortion in the source current. The clamp circuit is set to protect the MC circuit and switching devices against high voltage and current stresses. In the following, the source voltages u_{si} (i a, b, c) are assumed to be symmetrical. Thus, the variables can be represented as three-dimensional space vectors in a three-phase coordinate system. The equations describe the relationship between the load voltage u_o and the input voltage u_e, input current i_e and the load current i_o by the 3*3 switching states matrix S. S_{XY} (X {A, B, C}, Y {a, b, c}) equals to '1' when S_{XY} is turned on and equals to '0' when S_{XY} is turned off, respectively.

$$\begin{bmatrix} u_{oA} \\ u_{oB} \\ u_{oC} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} u_{ea} \\ u_{eb} \\ u_{ec} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} i_{ea} \\ i_{eb} \\ i_{ec} \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix}^T \begin{bmatrix} i_{oA} \\ i_{oB} \\ i_{oC} \end{bmatrix} \tag{2}$$

$$S = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \tag{3}$$

where u_{eY} (Y {a, b, c}) and u_{oX} (X {A, B, C}) represent the three phase input and output voltages, respectively. i_{eY} (Y {a,

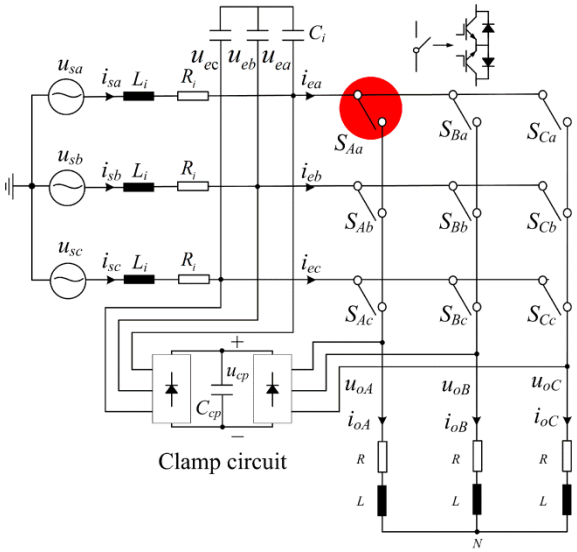


Fig. 1. Matrix converter topology.

$b, c\}$) and i_{oX} (X $\{A, B, C\}$) represent the three phase input and output currents, respectively.

Based on the restriction of the MC topology: the load cannot be connected in an open circuit and phases of the source cannot be connected in a short circuit, the switching states of each load phase must satisfy:

$$\begin{cases} S_{Aa} + S_{Ab} + S_{Ac} = 1 \\ S_{Ba} + S_{Bb} + S_{Bc} = 1 \\ S_{Ca} + S_{Cb} + S_{Cc} = 1 \end{cases} \tag{4}$$

So the MC can generate 27 valid switching states.

The model of the load is based on the resistance-inductance load as shown in Fig. 1. And the following equation describes the behavior of the load:

$$L\frac{di_o}{dt} = u_o - Ri_o \tag{5}$$

where L is the load inductance, R is the load resistance. Considering the sampling period T_s, the load current prediction can be obtained by using a forward Euler approximation as follows:

$$i_o^{k+1} = F_1 u_o^k + F_2 i_o^k \tag{6}$$

where

$$F_1 = \frac{T_s}{L} \tag{7}$$

$$F_2 = 1 - \frac{T_s R}{L} \tag{8}$$

The continuous system model of input filter in Fig. 1 can be represented by the following equations:

$$L_i\frac{di_s}{dt} = u_s - u_e - R_i i_s \tag{9}$$

$$C_i\frac{du_e}{dt} = i_s - i_e \tag{10}$$

where R_i, L_i, and C_i are the filter resistances, the mains and filter inductances, the filter capacitance, respectively. The continuous-time model can be represented by a state-space description as follows:

$$\begin{bmatrix} \frac{du_e}{dt} \\ \frac{di_s}{dt} \end{bmatrix} = A\begin{bmatrix} u_e \\ i_s \end{bmatrix} + B\begin{bmatrix} u_s \\ i_e \end{bmatrix} \tag{11}$$

where

$$A = \begin{bmatrix} 0 & 1/C_i \\ -1/L_i & -R_i/L_i \end{bmatrix} \tag{12}$$

$$B = \begin{bmatrix} 0 & -1/C_i \\ 1/L_i & 0 \end{bmatrix} \tag{13}$$

where A and B are assumed for the formula derivation simply. A discrete input filter model can be derived from (11) and the relation between the discrete-time variables can be described as:

$$\begin{bmatrix} u_e^{k+1} \\ i_s^{k+1} \end{bmatrix} = G\begin{bmatrix} u_e^k \\ i_s^k \end{bmatrix} + H\begin{bmatrix} u_s^k \\ i_e^k \end{bmatrix} \tag{14}$$

where

$$G = e^{AT_s};\ \ H = A^{-1}(G - I)B \tag{15}$$

According to this model, a prediction value of the source current and the input voltage in the next sampling instant can be obtained under each possible switching state by substituting (15) into (14), the prediction of the source current and input voltages are computed as follow:

$$i_s^{k+1} = D_1 u_s^k + D_2 u_e^k + D_3 i_s^k + D_4 i_e^k \tag{16}$$

$$u_e^{k+1} = E_1 u_s^k + E_2 u_e^k + E_3 i_s^k + E_4 i_e^k \tag{17}$$

where constants D_1, D_2, D_3, D_4, E_1, E_2, E_3, and E_4 depend on the filter parameters R_i, L_i, C_i and the sampling time T_s.

B. FCS-MPC Strategy

FCS-MPC strategy is used to make the controlled variables catch up with the corresponding references respectively at the end of the sampling period. The operation of MC is required to satisfy two limitations: i), the MC should run with unit power factor; ii), the load current i_o should accurately follow the reference value.

The first limitation is achieved by minimizing the error between the predicted values of the source current i_s and the corresponding reference . The reference value of source current can be given by:

$$i_s^* = \begin{bmatrix} I_{sm}^* \cos\phi & I_{sm}^* \cos(\phi - 2\pi/3) & I_{sm}^* \cos(\phi + 2\pi/3) \end{bmatrix}^T \tag{18}$$

where is the angle of source voltage u_s, which can be obtained through u_{sa}, u_{sb}, u_{sc}, and is the amplitude of the expected source current, which is determined by the active power flow. The input and output active power can be calculated from equations (19) to (21).

$$P_o = \tfrac{3}{2} {I_{om}^*}^2 R \tag{19}$$

$$P_{in} = \tfrac{3}{2}(U_{sm} I_{sm}^* \cos\theta - {I_{sm}^*}^2 R_i) \tag{20}$$

$$\eta = \frac{P_o}{P_{in}} \tag{21}$$

where P_o, P_{in} are the output and input active power, , U_{sm} are the amplitude of the reference load current and the source voltage u_s, respectively. is the efficiency of the converter. To achieve the unity power factor, phase difference between the source current i_s and the source voltage u_s, is considered equal to zero. Hence, the amplitude of the expected source current can be calculated as:

$$I_{sm}^* = \frac{-\eta U_{sm} \pm \sqrt{(\eta U_{sm})^2 - 4\eta R_i {I_{om}^*}^2 R}}{-2\eta R_i} \tag{22}$$

So , an important part of the cost function, can be designed by:

$$g_1 = \Delta i_{s\alpha}^2 + \Delta i_{s\beta}^2 \tag{23}$$

where and are the errors between the predictive source current and the reference source current in static two-phase coordinates, and it can be expressed as:

$$\Delta i_s = (\Delta i_{s\alpha} \quad \Delta i_{s\beta})^T = T_{abc to \alpha\beta}(i_s^P - i_s^*) \tag{24}$$

where the variable represents the prediction for the next sampling period. is the parameter matrix which transforms the static three-phase coordinates to the static two-phase coordinates, and is expressed as:

$$T_{abc to \alpha\beta} = \sqrt{\tfrac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{25}$$

The second limitation is achieved by minimizing the error

between the predicted values of the load current and the reference current . , can be designed by:

$$g_2 = \Delta i_{o\alpha}^2 + \Delta i_{o\beta}^2 \tag{26}$$

where and can be obtained according to the following equation:

$$\Delta i_o = (\Delta i_{o\alpha} \quad \Delta i_{o\beta})^T = T_{abcto\alpha\beta}(i_o^P - i_o^*) \tag{27}$$

As mentioned above, the final cost function g which includes both the objectives, is obtained by:

$$g = \lambda * g_1 + g_2 \tag{28}$$

The weighting factor λ of the cost function (28) is empirically adjusted based on [34]. First λ is set to 0, priority will be given to control the load current at the cost of the highly distorted input current. Later, the weighting factor λ is slowly increased with the purpose of obtaining unity power factor in the source current while maintaining good output performance. At each sampling time, all 27 possible switching states are used to evaluate the cost function g, the switching state N that produces the minimum value of is selected to be applied in the next sampling period according to the following equation:

$$\mathrm{g}[N] = \min\{g^{k+2}[i]\}, \quad i = 1, 2...27 \tag{29}$$

In Fig. 2, the flowchart of the FCS-MPC strategy applied on MC is described. At the k^{th} sampling period , the source voltage , the source current , the input voltages and the load current are measured and the switching states S^k in can be known easily. The input current can be computed from (2) using S^k and while the load voltages can be calculated from (1) using S^k and . Thus, , and at the $(k+1)^{\text{th}}$ sampling period can be derived from (6), (16) and (17). Considering that the change in the source voltages is small in one sampling period, will be considered equal to . In the same way, predictive values of and at the $(k+2)^{\text{th}}$ sampling period can be obtained for each valid switching state. Substituting each predictive value into , the switching state making get the minimum will be applied in the $(k+1)^{\text{th}}$ sampling period .

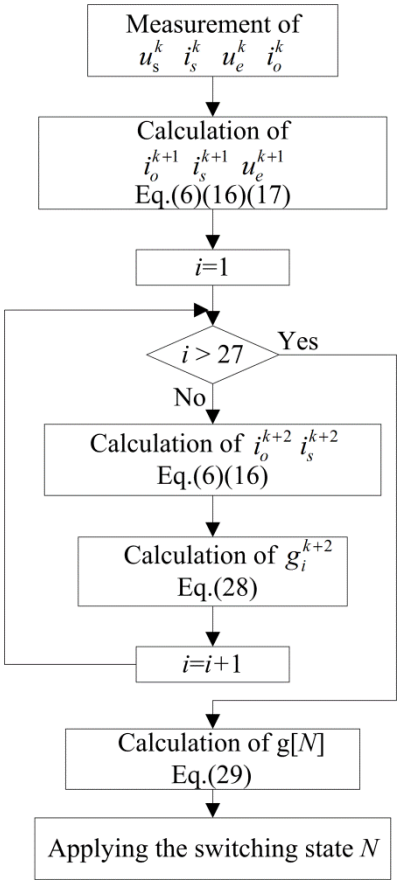


Fig. 2. The flowchart of the FCS-MPC strategy.

III. Fault Diagnosis Method

On the basis of the FCS-MPC, the effect of an open-switch fault on system performance is first discussed by way of an example scenario and then generalized. Following that, a fault diagnosis method for MC with FCS-MPC is proposed in this section.

Assume the following example conditions:

1) Sampling period is T_s.

2) The input voltage period T_{in} is subdivided and labeled with six different sectors as shown in Fig. 3. Input voltage angle is presently at sector V but is entering the range of sectors VI, I. The load phase-A reference current and the load phase-A current i_{oA} are positive.

3) At the k^{th} sampling period , the controller attempts to minimize the difference between the load current i_{oA} and its reference by setting S_{Aa} = 1. However, switch S_{Aa} is

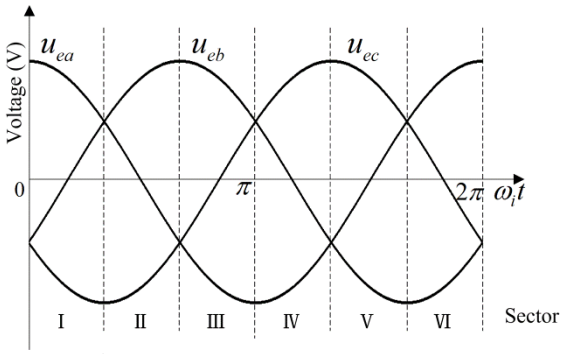
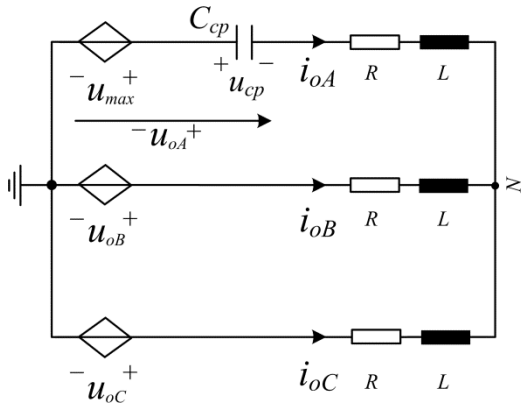
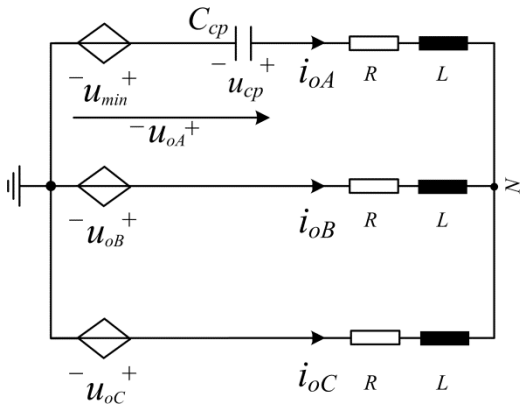


Fig. 3. The sector of the input voltage



(a)



(b)

Fig. 4. The equivalent circuit of Fig. 1 when an open-switch fault occurs in switch S_{Aa} (a) load phase-*A* current $i_{oA}>0$, (b) load phase-*A* current $i_{oA}<0$

suffering an open-switch fault.

Thus, it leads to an open circuit of phase-*A*. The load phase-*A* current i_{oA} flows through both the matrix converter and the clamp circuit. The equivalent circuit is shown in Fig. 4 (a). Then, the circuit model is achieved as follow:

$$\begin{cases} u_{oA} - Ri_{oA} - L\frac{di_{oA}}{dt} = u_N \\ u_{oB} - Ri_{oB} - L\frac{di_{oB}}{dt} = u_N \\ u_{oC} - Ri_{oC} - L\frac{di_{oC}}{dt} = u_N \\ i_{oA} + i_{oB} + i_{oC} = 0 \end{cases} \tag{30}$$

where u_N is the voltage between the load neutral point and the ground point of the power supply.

The output phase voltages are expressed as follow:

$$\begin{cases} u_{oA} = u_{\max} - u_{cp}, \quad faulty, i_{oA} > 0 \\ \begin{bmatrix} u_{oB} \\ u_{oC} \end{bmatrix} = \begin{bmatrix} S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} u_{ea} \\ u_{eb} \\ u_{ec} \end{bmatrix} \end{cases} \tag{31}$$

where U_{cp} denotes the capacitor voltage of the clamp circuit. Since the load phase-*A* current charges the capacitor of the clamp circuit, U_{cp} is larger than the maximum input line-to-line voltage. It can be achieved as:

$$\begin{cases} u_{\max} = \max(u_{ea}, u_{eb}, u_{ec}) \\ u_{\min} = \min(u_{ea}, u_{eb}, u_{ec}) \\ u_{cp} \ge u_{\max} - u_{\min} \end{cases} \tag{32}$$

Then, according to equations (30) and (31), the change rate of the load phase-*A* current i_{oA} can be obtained as:

$$\frac{di_{oA}}{dt} = \frac{2u_{\max} - 2u_{cp} - u_{oB} - u_{oC} - 3Ri_{oA}}{3L} \tag{33}$$

According to equation (32), it can be achieved as:

$$\begin{cases} u_{cp} \ge u_{\max} - u_{oB} \\ u_{cp} \ge u_{\max} - u_{oC} \end{cases} \tag{34}$$

Then, Substituting (34) into (33), it can be achieved as:

$$\frac{di_{oA}}{dt} < 0, \quad \text{when } i_{oA} > 0 \tag{35}$$

Construct an energy function v as:

$$v = \tfrac{1}{2} L i_{oA}^2 \tag{36}$$

Then, the change rate of the energy function can be obtained as:

$$\frac{dv}{dt} = L i_{oA} \frac{di_{oA}}{dt} < 0 \tag{37}$$

Thus, when the faulty switch satisfies $S_{Aa}=1$, the amplitude of load phase-*A* current decreases. Then, the error between the load current and the reference current become bigger. Since the switch S_{Aa} connects the maximum input voltage to the load phase-*A* in sectors VI and I, the predictive controller sets $S_{Aa}=1$ again. However, switch S_{Aa} is now suffering an open-switch fault. The result is that the amplitude of the load current i_{oA} decrease and the signal S_{Aa} is set as '1' for some consecutive sampling periods. If the time is long enough, the amplitude of load phase-*A* current will converge to zero.

Assume that input voltage angle is in the range of sectors III and IV, and the load phase-*A* reference current and the load phase-*A* current i_{oA} are negative. The equivalent circuit can also be achieved in Fig. 4 (b). Then, after some manipulations, the change rate of the energy function can be achieved as:

$$\frac{dv}{dt} = \frac{i_{oA}\left(2u_{\min} + 2u_{cp} - u_{oB} - u_{oC} - 3Ri_{oA}\right)}{3} < 0 \tag{38}$$

Thus, if the time is long enough, the amplitude of load phase-*A* current will converge to zero.

So the fault diagnosis logic is schematically described as follow:

If and $S_{Aa}=1$ for some consecutive sampling periods => switch S_{Aa} is faulty.

$$\begin{cases} \textit{fault in } S_{Aa}, |i_{oA}| < \varepsilon \text{ and } S_{Aa}=1 \textit{ for some consecutive sampling periods} \\ \textit{fault-free in } S_{Aa}, \textit{others} \end{cases} \tag{39}$$

where is a positive threshold which is selected to make the fault diagnosis method more robust and to minimize the possibility of the false alarms mainly caused by the noises and non-ideal characteristics of the switches.

In order to realize reliable fault detection, the method for selecting fault diagnosis time is carefully analyzed [20]. The fault condition is related to the input voltage period and the load current fundamental period, denoted as T_o, The reference load current changes sign every half of the fundamental period. The fault time duration is approximated by:

$$T_{fault} = \min\{\tfrac{T_{in}}{3}, \tfrac{T_o}{2}\} \tag{40}$$

Considering the time for the current to discharge from its initial value to zero through the clamp circuit, denoted as , the time of the consecutive zero load current can be calculated as:

$$T_{zero} = T_{fault} - T_{discharge} \tag{41}$$

To distinguish the phenomenon of load current remaining zero in the faulty condition from zero-current crossings of normal operation, the proposed method employs the time-based analysis introduced in [35]. The fault diagnosis time should satisfy the equation (42), where k_f is the sensitivity factor for the fault diagnosis, is the zero-current crossing time that the load reference current keeps less than in normal operation.

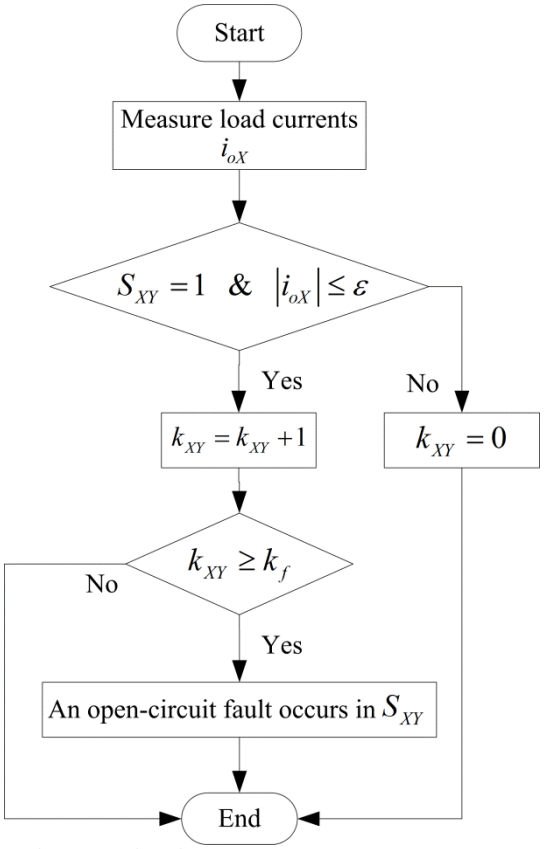


Fig. 5. The flowchart of the fault diagnosis method X {A, B, C}, Y {a, b, c}.

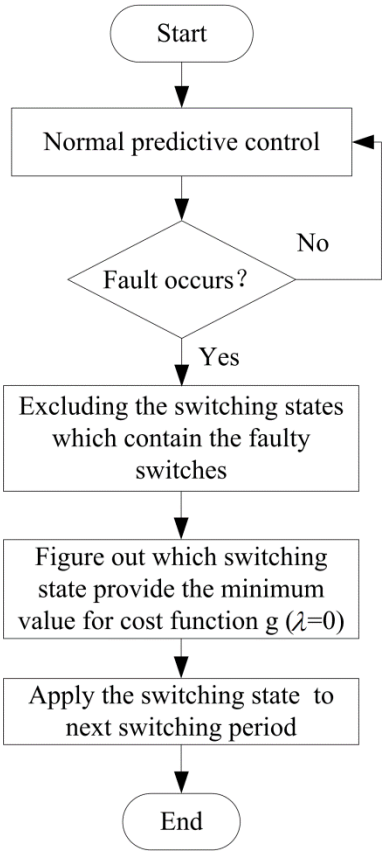


Fig. 6. The flowchart of the fault tolerant control strategy.

$$k_f T_s > T_\varepsilon \tag{42}$$

According to equation (30)-(42), the fault diagnosis time should satisfy:

$$\min\{\tfrac{T_{in}}{3}, \tfrac{T_o}{2}\} - T_{discharge} > k_f T_s > T_\varepsilon \tag{43}$$

Based on these observations, the fault diagnosis method is generalized for all switch devices in MC. The flowchart of the fault diagnosis method is shown in Fig. 5. At the beginning of the fault diagnosis method, the hall sensors measure the three-phase load current i_{oX}. k_{XY} is the number of consecutive sampling periods, which satisfy the conditions that and S_{XY} = 1. If , then the switch S_{XY} is faulty.

IV. Fault Tolerant Control Strategy

A. Fault Tolerant Control Strategy

To improve the quality of the output current at faulty operation without hardware reconfiguration and redundant devices, a fault tolerant method for MC with FCS-MPC is presented in this section. The number of possible switching states is reduced when a single open-switch fault occurs because the faulty switch is unable to be turned on. For example, if open-switch fault occurs in switch S_{Aa}, load phase-A can only be connected to input phase-b and input phase-c, as input phase-a is not accessible due to the fault in the switch S_{Aa}. The constraints of the load phase are expressed by:

$$\begin{cases} S_{Ab} + S_{Ac} = 1 \\ S_{Ba} + S_{Bb} + S_{Bc} = 1 \\ S_{Ca} + S_{Cb} + S_{Cc} = 1 \end{cases} \tag{44}$$

Then only 18 switching states are allowed.

Under the faulty condition mentioned above, maintaining the quality of load current is of the primary concern, compared with the quality of source current. Thus, the fault tolerant strategy aims to generate the optimum load currents without taking the quality of the source current into account. The flowchart of the fault tolerant control strategy is shown in Fig. 6. Among the remaining switching states, the cost function g is calculated, and the weighting factor λ is selected as zero. Then the switching state which provides the minimum value for the cost function g is selected and applied to the MC in next switching period.

B. Reliability Analysis

With the fault tolerant strategy, better quality of the output current is obtained under the faulty condition, and the reliability of the MC system can be improved as well. The Markov reliability model is used to analyze the reliability of power electronic converter [36], [37]. The MC with fault tolerant capability (FTC) can operate under normal operation and single open-switch fault. The state-transition diagram of MC with FTC is shown in Figs. 7. The nodes of the state-transition diagram represent operation states. The k^{mn} (k = 0, 1, 2, 3, 4; m = 0, 1, 2; n = 0, 1) denotes the system state with m failed bi-directional switches and n failed events that input filter,

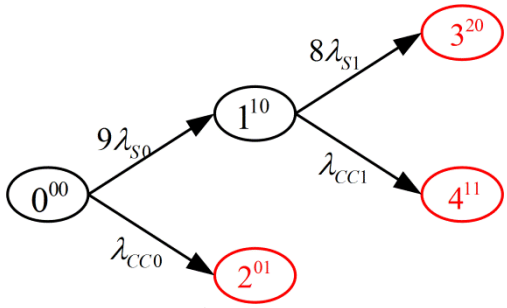


Fig. 7. State-transition diagram of MC with FTC.

Table I
RELIABILITY RESULTS OF MC

Case	*MTTF* (hours)
MC without FTC	34894
MC with FTC	49528

power connectors, controls or clamp circuit are fail. The edges stand for transitions between states triggered by components failures. λ_{Sm} is the failure rate of bi-directional switch under the condition of m failed bi-directional switches. λ_{CCm} is the total failure rate of input filter, power connectors, controls and clamp circuit under the condition of m failed bi-directional switches.

The Chapman-Kolmogorov equation is used to analyze the State-transition diagram in Fig. 7 [36], which leads to the following equations:

$$\frac{dp_0(t)}{dt} = -(9\lambda_{S0} + \lambda_{CC0})\,p_0(t) \tag{45}$$

$$\frac{dp_1(t)}{dt} = 9\lambda_{S0} * p_0(t) - (\lambda_{CC1} + 8\lambda_{S1}) * p_1(t) \tag{46}$$

where $p_k(t)$ is the probability of MC being in state k^{mn} at time t. $R(t)$ represents the probability that the MC will operate without failures over a time interval [0, t]. The MC without FTC can only operate under states 0^{00}, while the MC with FTC can operate under states 0^{00} and 1^{10}. Thus, the following equation is obtained:

$$\begin{cases} R(t) = p_0(t), \text{without } FTC \\ R(t) = p_0(t) + p_1(t), \text{with } FTC \end{cases} \tag{47}$$

MTTF is defined as the mean time to the failure of the system (complete impossibility of its operation). It can be obtained as follow:

$$MTTF = \int_0^{+\infty} R(t)\mathrm{d}t \tag{48}$$

Therefore, the system reliability function and *MTTF* of MC with FTC are as follow:

$$R(t) = e^{-(9\lambda_{S0}+\lambda_{CC0})t} + \frac{9\lambda_{S0}e^{-(8\lambda_{S1}+\lambda_{CC1})t}}{\lambda_{CC0}+9\lambda_{S0}-\lambda_{CC1}-8\lambda_{S1}}\left[1-e^{(\lambda_{CC1}+8\lambda_{S1}-\lambda_{CC0}-9\lambda_{S0})t}\right] \tag{49}$$

$$MTTF = \frac{1}{9\lambda_{S0}+\lambda_{CC0}} + \frac{9\lambda_{S0}}{(8\lambda_{S1}+\lambda_{CC1})(9\lambda_{S0}+\lambda_{CC0})} \tag{50}$$

Under the conditions of paper [4], the failure rate of bi-directional switches in MC is $1.27e^{-6}$, the failure rate of other failure events in MC is $17.16e^{-6}$. Assume that = $=1.276e^{-6}$, = $=17.16e^{-6}$ (not considering the change of failure rate after fault tolerance), the reliability results of MC with and without FTC are listed in Table I. Under the conditions of paper [4], the *MTTF* of MC with FTC can be 14634 hours longer than the MC without FTC.

V. EXPERIMENTAL RESULTS

In this section, the fault diagnosis and fault tolerant strategies are verified on a low-voltage experimental prototype as shown in Fig. 8. The corresponding component parameters are indicated in Table II. The setup is fed by 60V/50Hz (root mean square, RMS), the power source is not ideally perfect and the AC source voltage contains some undesirable fifth-order and seventh-order harmonics. Thus, the MC cannot properly operate without a small passive damping resistor R_p in parallel with L_i. The value of R_p is chosen as 9Ω. The bi-directional switches are realized by the IGBT module FF200R12KT3_E. A floating-point digital signal processor (DSP, TMS320F28335) is used to select the optimal switching state while a field programmable gate array (FPGA, EP2C8J144C8N) is used for generating an impulse to control the switches.

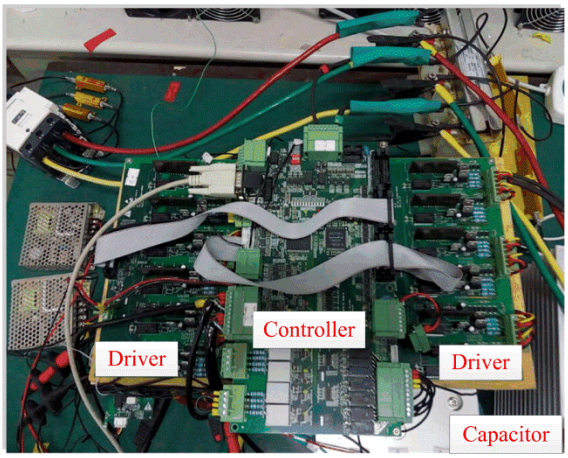


Fig. 8. Experimental setup.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

Parameters	Value
Source phase voltage (V_{RMS})	60V
Source voltage frequency(f_m)	50Hz
Sampling period (T_s)	70us
Input mains and filter inductor (L_i)	0.6mH
Input filter capacitor (C_i)	66uF
Input mains and filter resistor (R_i)	0.1Ω
Input passive damping resistor (R_p)	9Ω
Resistor of load (R)	4.4Ω
Inductor of load (L)	6mH

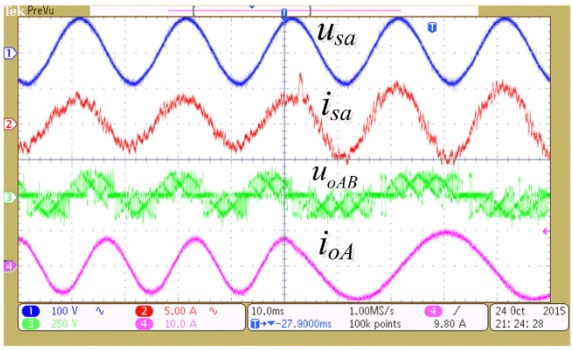
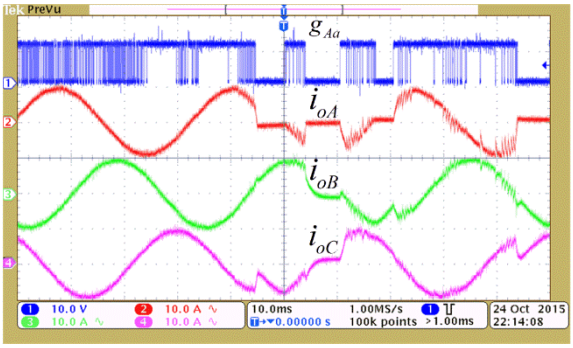
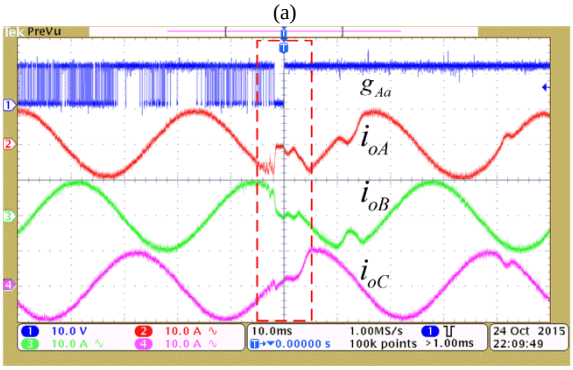


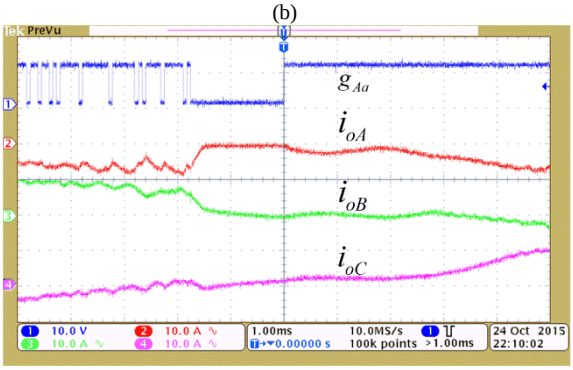
Fig. 9. Experimental results under normal condition with the reference load current set from 8A/60Hz to 10A/30Hz .



(a)

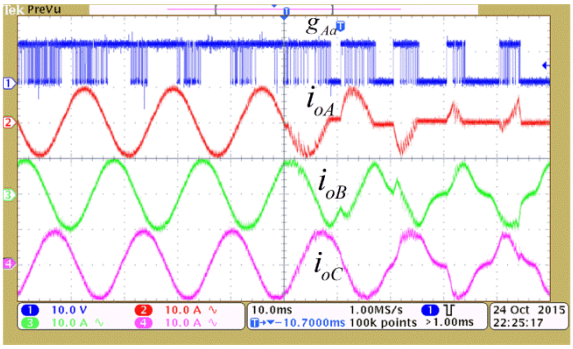


(b)

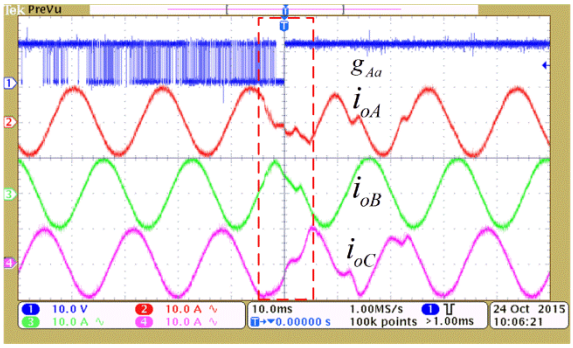


(c)

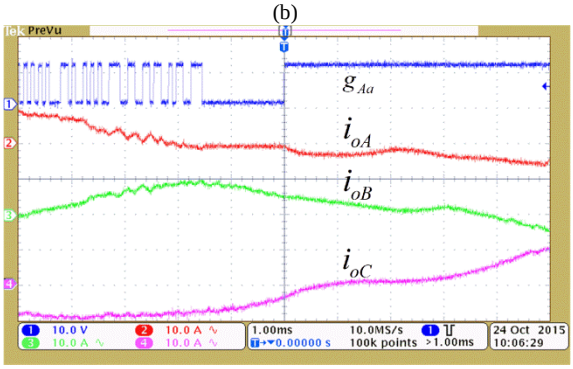
Fig. 10. Experimental results with the reference load current set 10A/30Hz (a) Operation under an open-circuit fault in switch S_{Aa} without activating the proposed fault diagnosis and tolerant strategies (b) Operation under an open-circuit fault in switch S_{Aa} with activating the proposed fault diagnosis and tolerant strategies (c) The enlarged drawing of the red dotted box.



(a)



(b)



(c)

Fig. 11. Experimental results with the reference load current set 10A/60Hz (a) Operation under an open-circuit fault in switch S_{Aa} without activating the proposed fault diagnosis and tolerant strategies (b) Operation under an open-circuit fault in switch S_{Aa} with activating the proposed fault diagnosis and tolerant strategies (c) The enlarged drawing of the red dotted box.

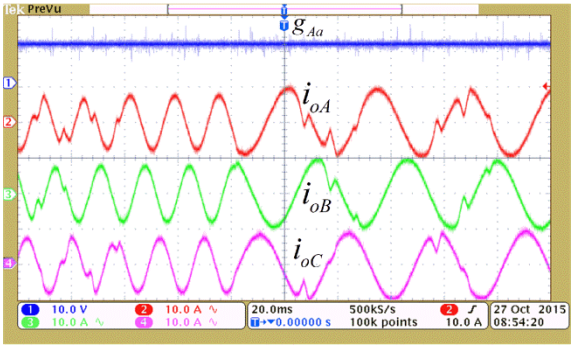
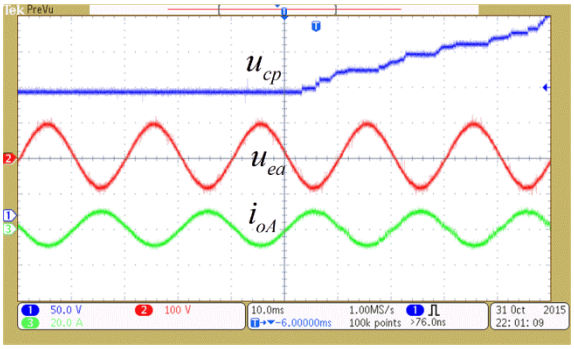
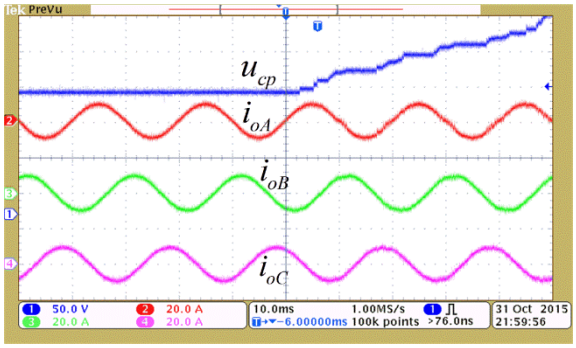


Fig. 12. Experimental results under fault tolerant condition with the reference load current set from 8A/60Hz to 10A/30Hz when an open-circuit fault occurs in switch S_{Aa}.



(a)



(b)

Fig. 13. Experimental results under an open-circuit fault in switch S_{Aa} with activating the proposed fault diagnosis and tolerant strategies, when the reference load current set as 10A/50Hz and the phase difference between the input voltage and output current is .

Fig. 9 shows the experimental waveforms of source voltage u_{sa}, source current i_{sa}, output line-to-line voltage , and load current i_{oA} when the MC is operating under normal condition with the reference load current set from 8A/60Hz to 10A/30Hz. The source currents are seen to be sinusoid with low distortions and the unity power factor is obtained. The load currents are also seen to be sinusoid with low distortions and track the reference current in several sampling periods.

The experimental waveforms with the reference load current set 10A/30Hz operating under an open-circuit fault in switch S_{Aa} with and without activating the proposed fault diagnosis and tolerant strategies are shown in Fig. 10. In Fig. 10, when $S_{Aa} = 1$, then $g_{Aa} = 0$V, the gate signal of switch S_{Aa} is "*ON*". When $S_{Aa} = 0$, then $g_{Aa} = 15$V, the gate signal of switch S_{Aa} is "*OFF*". According to the analysis of Section III and the experimental condition, is chosen as 0.3A. The sensitivity factor for the fault diagnosis time $k_f = 20$, and the sampling period is chosen as 70us. Then the fault diagnosis time is 1.4ms. As shown in Fig. 10(a) without activating the proposed fault diagnosis and tolerant strategies, the load currents appear to be sinusoidal with low distortions at the beginning. At the moment MC system is introduced an open-switch fault of S_{Aa}, the load current i_{oA} is distorted and equals to zero after a short time since it flows through both the matrix converter and clamp circuit. i_{oB} and i_{oC} are also seriously affected. However, as shown in Fig. 10(b) with activating the proposed fault diagnosis and tolerant strategies, after open-switch fault occurs in switch S_{Aa}, the predictive controller keeps giving "*ON*" signal to S_{Aa} in some consecutive sampling periods. However, S_{Aa} is not able to be conducted, the load phase-*A* approaches zero for some consecutive sampling periods. Then, the switch S_{Aa} is judged to be the faulty switch. This phenomenon can be seen more clearly from the enlarged drawing of the red dotted box in Fig. 10(c). After the faulty switch is located, the fault tolerant strategy based on FCS-MPC generates the appropriate switching state for the remaining eight normal switches to minimize the error between the load current and the reference current. All the three-phase load currents become more balanced and are very close to their desired sinusoidal waveforms. The experimental waveforms with the reference load current set 10A/60Hz operating under an open-circuit fault in switch S_{Aa} with and without activating the proposed fault diagnosis and tolerant strategies are shown in Fig. 11. The same conclusion can be obtained as the Fig. 10.

The corresponding THDs of three phase load currents under normal, faulty and fault tolerant operating conditions are presented in Table III. In faulty operation, it can be seen that the fundamental amplitude and quality of load phase-*A* current are obviously reduced. The fundamental amplitude and quality of the load phase-*B* and load phase-*C* current are also affected. In fault tolerant operation, it can be seen that there is a slight reduction in the fundamental amplitude and quality of each phase load current.

Fig. 12 shows the experimental waveforms of source voltage u_{sa}, source current i_{sa}, output line-to-line voltage , and load current i_{oA} when the MC is operating under fault tolerant condition with the reference load current set from 8A/60Hz to 10A/30Hz. The results show that the proposed fault tolerant solution can track the reference current.

It is also worth mentioning that the open-circuit fault in switch S_{Aa} cannot be detected in several input source periods when the following conditions are satisfied:

i) The load current frequency of the MC was set exactly to 50Hz, which is same with the input voltage.

ii) The phase difference between the input voltage and the output current is .

Since the input voltage angle will not be in sector VI and I when the load phase-*A* reference current is positive, while the input voltage angle will not be in sector III and IV when the load phase-*A* reference current is negative. Thus, the open-circuit fault in switch S_{Aa} is difficult to be detected. The experimental verification is shown in Fig. 13. According to Fig. 13(a), the phase difference between the input voltage and the output current is . As shown in Fig. 13(b), the clamping capacitance voltage u_{cp} is getting a sudden increase because the load current i_{oA} is flowing through the clamp circuit capacitor after the open-circuit fault occurs in switch S_{Aa}. The load current i_{oA} is distorted and the open-circuit fault is not detected. Nevertheless, the input and output frequency is different in most application field of MC, the situation satisfying the above two conditions is more theoretical than practical.

TABLE III
THD OF MC LOAD CURRENTS UNDER NORMAL, FAULTY AND FAULT TOLERANT OPERATING CONDITIONS

Case			MC condition		
			Normal	Faulty	Fault Tolerant
10A/30Hz	i_{oA}	THD (%)	6.90	93.94	23.16
		Fundamental (A)	9.686	4.47	8.96
	i_{oB}	THD (%)	6.78	35.07	18.77
		Fundamental (A)	9.90	7.74	9.10
	i_{oC}	THD (%)	6.89	33.99	10.57
		Fundamental (A)	9.75	7.97	9.43
10A/60Hz	i_{oA}	THD (%)	4.91	97.66	13.03
		Fundamental (A)	9.84	1.79	8.70
	i_{oB}	THD (%)	4.66	29.86	4.72
		Fundamental (A)	9.90	7.27	9.80
	i_{oC}	THD (%)	4.76	23.49	13.49
		Fundamental (A)	9.93	7.52	8.58

VI. Conclusion

Firstly, a FCS-MPC strategy for MC is investigated in this paper, which derives from a discrete mathematical model of MC system. Then, a fault diagnosis method for single open-switch fault in MC with FCS-MPC is proposed. The proposed fault diagnosis method is implemented by monitoring the load currents and judging the switching state based on FCS-MPC. Compared with the conventional modulation strategies such as carrier-based modulation method, indirect space vector modulation and optimum Alesina-Venturini, it is simpler to diagnose the exact location of the open switch in MC with FCS-MPC. Moreover, a fault tolerant strategy for single open-switch fault for MC with FCS-MPC is also discussed to maintain the three-phase load currents as close as possible to its normal conditions. The control strategy is based on selecting the most appropriate switching state associated with the remaining normal switches of the MC. Finally, experiments are performed to verify the proposed methods. Experiment results show the feasibility and effectiveness of the fault diagnosis method and fault tolerant strategy for MC with FCS-MPC.

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