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Two-Dimension Sorting and Selection Algorithm featuring Thermal Balancing Control for Modular Multilevel Converters

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Keywords

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Abstract

With the aim to solve the unbalanced thermal behavior in the modular multilevel converter, introduced by mismatch in the submodule parameters, a thermal balancing control strategy is proposed here. The proposed solution ensures a balanced junction temperature for the power devices, while the balance between the capacitor voltages is maintained.

Introduction

Recently, the modular multilevel converter (MMC) has been considered as a suitable technology for high-power voltage source converters (VSCs). Due to its several advantages, such as: scalability, high efficiency, low total harmonic distortion (THD) for the output voltage, low switching frequency operation, and capability for the usage of low-medium voltage power devices, MMCs have been implemented commercially in high-voltage direct current (HVDC), static synchronous compensator (STATCOM), and large motor drive applications [1]-[5].

In general, the control of the MMC is more complex compared to the typical two-level VSCs, mainly due to the large number of submodules (SMs), which is required in order to generate a multilevel output voltage waveform. From the control point of view, one main challenge is the internal arm balancing control of the MMC. Normally, the arm balancing control aims to ensure balance between the capacitor voltages of the SMs from the arm, which is required for a stable operation [6]. In contrast, the balancing of power losses and junction temperature of the power devices from the SMs are usually not taken in consideration. In MMC applications, the power losses distribution of the devices from the same SM is usually unequal, depending on the operating condition which is mainly determined by the power factor [7]-[10]. For the half-bridge type SM, the most unequal device loading occurs when the MMC operates at unity power factor, which is a typical operating condition for the HVDC applications [11]. In this case, the SMs are often bypassed at the arm peak current. Therefore, the bypass switch from the SM (e.g., lower IGBT) has significantly higher device loading and therefore power losses than the other devices. Nevertheless, in most literatures, it is normally assumed that this power losses distribution is identical for all SMs (e.g., the power losses in the lower IGBT is equal for all SMs) [7], [12], and it is referred as a thermal balance case in this paper.

However, this assumption of thermal balance among the SMs can be used only when all the SMs are identical. In practices, the SMs are normally not identical. The mismatch in the SM parameter can be introduced, e.g. due to the manufacturing tolerance of the SM capacitors, different conduction and switching losses of the power devices etc. [13]. Besides, the degradation of the capacitor during the operation and the replacement of one broken SM can further lead to a significant deviation in the capacitance of the SMs. Then, by balancing only the capacitor voltage, a thermal unbalance among the SMs is introduced, where the junction temperature of the same device (e.g., lower IGBT) in different SMs are not equal. This is caused by the unbalance of both the conduction and the switching losses of

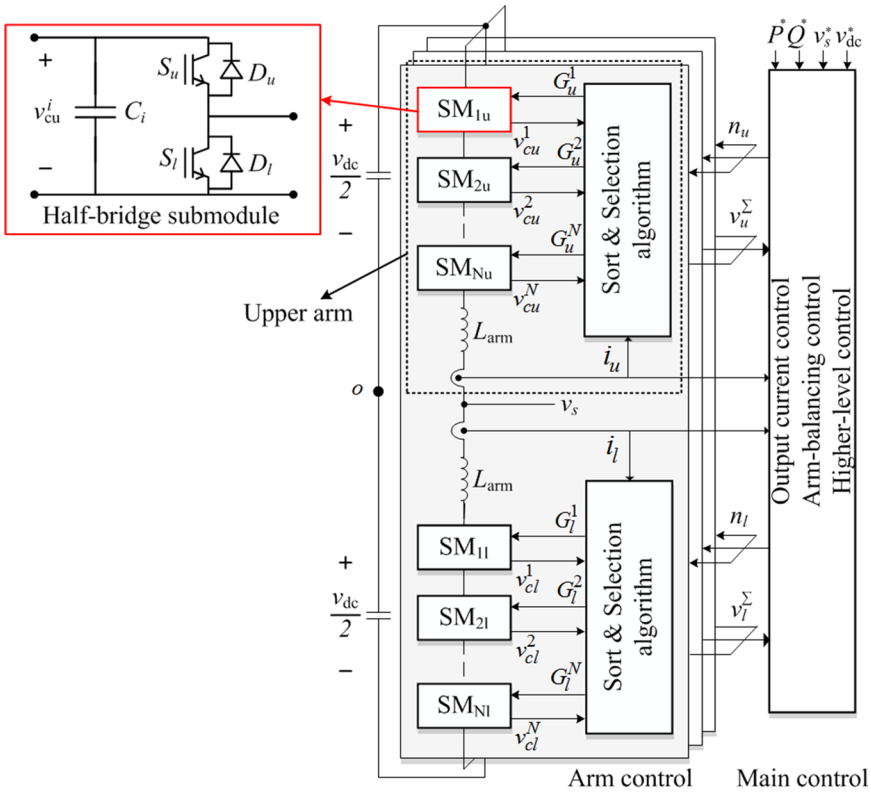

Fig. 1: System configuration of three-phase Modular Multilevel Converter.

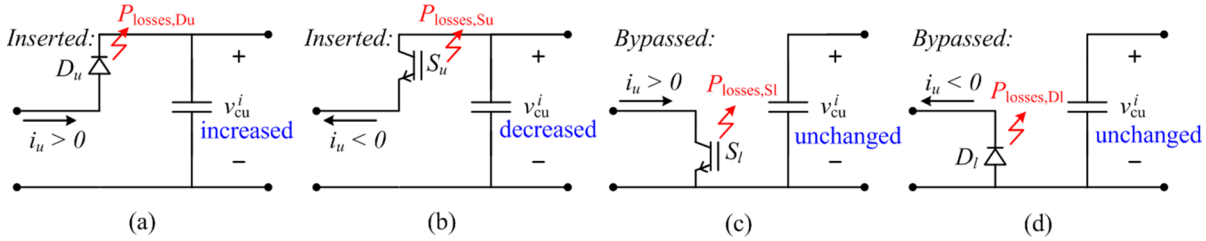

Fig. 2: Operating modes of the half-bridge SM and its effect on the capacitor voltage and the devices power losses when SM is: (a) inserted during $i_u > 0$, (b) inserted during $i_u < 0$, (c) bypassed during $i_u > 0$, (d) bypassed during $i_u < 0$.

the devices in the SMs, which can potentially increase the device junction temperature and lead to permanent damage. Moreover, the thermal unbalance is also undesirable when design the cooling system (e.g. heat sink) of the SM, since the thermal behavior of each SM is not the same.

With the aim to solve the above presented issues, the thermal unbalance mechanisms of the MMCs are first discussed. Then, a thermal balancing control (TBC) strategy is proposed. The TBC strategy can enhance the conventional sorting and selection algorithm by taking in consideration the junction temperatures of the power devices in addition to the capacitor voltage. Simulation results have verified the effectiveness of the proposed solution in terms of balancing both the capacitor voltage and the junction temperature, when the mismatch in the SM capacitor is introduced.

Basic Structure and Control Scheme of MMC

System Configuration

The typical system configuration of three-phase MMC is shown in Fig. 1. Each phase (also called a leg) consists of two arms - upper arm and lower arm, where each arm consists of N number of SMs connected in series with the arm inductor L_{arm}. At the SM level, a half-bridge SM topology is typically adopted as it is shown in Fig. 1, where S_u and S_l denote the upper and lower IGBTs, and D_u and D_l are the upper and lower Diodes, respectively. Fig. 2 shows the possible operating modes of each half-

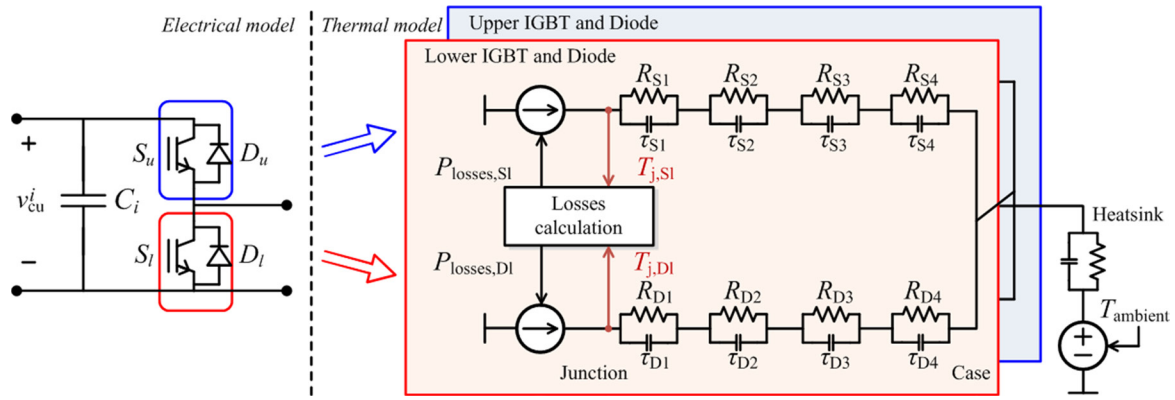

Fig. 3: Thermal model of the power devices in the half-bridge SM with a common heat sink.

Table I: Parameter of the thermal model from datasheet [9].

Device	Parameter	Value			
IGBT	R_{Si} [K/W]	0.0017	0.0022	0.0308	0.0022
	τ_{Si} [s]	0.0005	0.0032	0.0323	8.1389
Diode	R_{Di} [K/W]	0.0081	0.0526	0.0069	0.0053
	τ_{Di} [s]	0.0009	0.0290	0.1723	5.1810

bridge SM and its effect on the capacitor voltage v^{i}_{cu}. Then, the output voltage v_s of each phase can be generated by inserting (i.e., Figs. 2(a) and (b)) and bypassing (i.e., Figs. 2(c) and (d)) a corresponding number of SMs in a leg, which is given by the main controller [6].

The power losses during the device conduction associated with the mode of operation is also shown Fig. 2. In order to observe the thermal behavior of the devices in SM, the corresponding thermal model of the half-bridge has been built based on the Foster type electro-thermal network model, as it is shown in Fig. 3 [8], [9]. In this case, the SM is realized from a single half-bridge power module, meaning that all the devices are sharing the same heat sink for the cooling system. The parameters of the Foster model can be obtained from the datasheet [14] (which are based on measurements) as it is given in Table I, where R_{Si} and R_{Di} are the thermal resistances, and τ_{Si} and τ_{Di} is the time response of the IGBT and the Diode. Here, the power losses of the devices need to be calculated in order to estimate the junction temperature. In fact, losses in the power devices are also dependent to the junction temperature. Thus, the estimated junction temperature from the thermal model is used in the loss calculation, and the power losses of each device are then feedback to the thermal model, similarly as it has been proposed in [8]. Detailed losses calculation is provided in the appendix.

To avoid confusion, the thermal unbalance term in this paper refers to the unequal junction temperature of the same device in different SMs (e.g., between the lower IGBT junction temperature $T_{j,Sl}$ of SM_{1u} and SM_{2u}) while the unequal device loading term refers to the unequal loading among different devices in the same SM (e.g., between the junction temperature of the upper IGBT $T_{j,Su}$ and the junction temperature of the lower IGBT $T_{j,Sl}$ of SM_{1u}).

Standard Sorting and Selection Method for Capacitor-Voltage Balancing Strategy

In general, the control diagram of the MMC can be divided into 2 different levels - the main control level and the arm control level, as it is also shown in Fig. 1. In the main control level, an output voltage reference of the MMC is generated and then translated into an insertion index n_u, which has a value between 0 and 1. The corresponding required number of SM to be inserted/bypassed in each arm N_{ref} can be calculated as N_{ref} = round($N \cdot n_u$). Then, the arm control, where the main focus of this paper is, provides a mechanism to properly select the SM to be inserted and bypassed in the arm according to the N_{ref}, in order to keep the SM balanced (e.g., the SM capacitor voltage) [6]. Although several works have been done to improve the capacitor voltage balancing strategy of the arm control as it has be summarized in [6], only the standard sorting and selection methods proposed in [1] is considered in this paper, due to its simplicity. Nevertheless, the proposed solution can also be further adopted with other capacitor-voltage balancing strategies based on the sorting and selection approach.

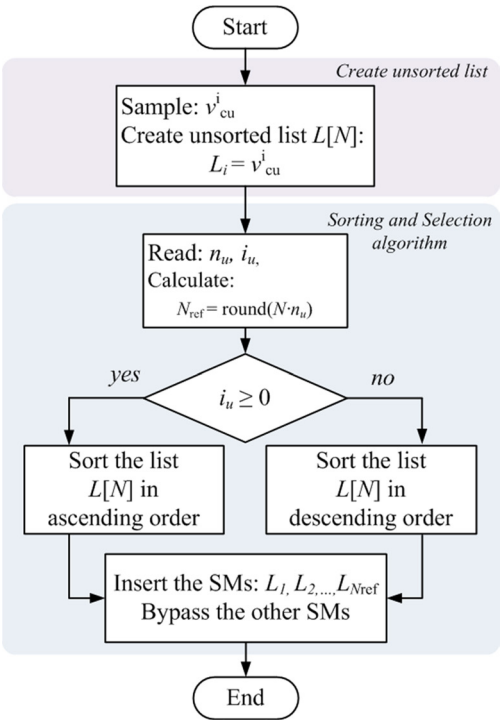

Fig. 4: Flow chart of the standard sorting and selection algorithm (for upper arm).

A flow chart of the sorting and selection method is shown in Fig. 4. Specifically, an unsorted voltage list is first created from the measured SM capacitor voltage v^{i}_{cu} in the arm. Then, the selection process is done according to: 1) sort the list $L[N]$ based on the arm current i_u direction, 2) during the positive arm current, the SM with the lowest capacitor voltage v_{cu} will be charged by inserting the SM into the arm, while the SM with the highest capacitor voltage v_{cu} will be bypassed. The action will be opposite during the negative arm current.

By adopting the sorting and selection algorithm, the capacitor voltage v_{cu} of each SM in the arm leads to a balanced situation. In case of all the SMs are identical (i.e., same value of capacitance C_i), the gate signal of each SM G^{i}_{u} produced by the sorting and selection algorithm will be almost identical but shifted in time. Consequently, although the device loading and the junction temperature among the devices in SM is unequal, depending on the operating power factor [7], it is similar for all SMs.

Mechanism of Thermal Unbalance between SMs in MMCs

In practice, a parameter mismatch in the SM capacitance C_i among the SMs can easily be introduced. The capacitors usually have a tolerance in their capacitance due to the manufacturing process, which can be up to 20% of the nominal value [13]. Besides, the capacitance value also decreases during the operation as the capacitor is degrading [15]. The replacement of one broken SM can also introduce the mismatch of the capacitors, since the new SM will likely have a higher capacitance value compared to the rest of the SMs. Thus, under these circumstances, the capacitors of all SMs are no longer identical. The thermal unbalance behavior among the SMs and its impact are explained in this section, where the analysis is divided into two mechanisms related to the conduction losses and the switching losses.

Thermal Unbalance Related to the Conduction Losses

Typically, the capacitor voltage v_{cu} of all SMs are balanced by the sorting and selection algorithm. The energy variation in the SM can be expressed as in (1). It can be seen from (1) that, with the same capacitance value C_i, the stored energy in the SM E_{sm} during each fundamental period is equal for all SMs. However, in case of one SM has a low capacitance, the stored energy of that SM will be lower than in the other SMs, since the sorting and selection algorithm will still keep the average value of the capacitor voltage to be balanced. Thus, the so-called insertion duty D_{INS} defined in (2), which represents the average time duration that the SM being inserted to the arm (i.e., t_{INS}) in each

Table II: Switching frequency and insertion duty of submodules.

Case: (Capacitance in p.u.)		Insertion duty D_{INS} [p.u.]		Switching frequency [Hz]	
		SM with C_{1u}	SM with $C_{2u,...Nu}$	SM with C_{1u}	SM with $C_{2u,...Nu}$
Without TBC	$C_{1u,2u,...Nu} = 1.0$	0.500	0.500	1150	1150
	$C_{1u} = 0.8, C_{2u,...Nu} = 1.0$	0.430	0.514	1337	1121
	$C_{1u} = 1.0, C_{2u,...Nu} = 0.8$	0.523	0.495	1073	1155
With TBC	$C_{1u} = 0.8, C_{2u,...Nu} = 1.0$	0.490	0.502	1064	1068
	$C_{1u} = 1.0, C_{2u,...Nu} = 0.8$	0.480	0.504	1042	1046

fundamental period (T = 20 ms), will be decreased in order to reduce the stored energy in the SM. In other words, the SM with smaller capacitance will be bypassed for longer time in order to reduce the energy variation, which occurs during the insertion. This can be seen by comparing the D_{INS} during a fundamental period for three different cases (without enabling the TBC strategy) in Table II. According to the operating modes from Fig. 2, the decrease of the insertion duty D_{INS} (i.e., when SM has a low C_i) will increase the conduction losses and therefore the junction temperature T_j of both S_l and D_l (which will be shown in Figs. 6(a) and 7(a)) due to the increased bypass time duration. On the other hand, if one SM has a lower insertion duty D_{INS} (e.g., higher C_i) than the other SMs, the conduction losses and the junction temperature T_j of the devices S_u and D_u of that SM will be increased (which will be shown later in Figs. 6(c) and 7(c)), due to the more insertion time duration.

$$E_{sm} = \frac{1}{2} C_i v_{cu}^2 \tag{1}$$

$$D_{INS} = \frac{t_{INS}}{T} \tag{2}$$

Thermal Unbalance Related to the Switching Losses

In the typical sorting and selection algorithm, the SMs are operated with almost the same switching frequency f_{sw}, resulting in a balanced switching loss for all the SMs. However, this is not the case when the SM capacitors are not identical, since the charging and discharging processes are affected by the value of C_i. When the SM is inserted to the arm, the capacitor voltage v_{cu} will be changed according to (3), where T_s is the sampling period of the sorting and selection algorithm.

$$i_u(t) = C_i \left(\frac{v_{cu}(t) - v_{cu}(t - T_s)}{T_s} \right) \tag{3}$$

During each time interval T_s, the SM with a low value of C_i will be charged (when $i_u(t) > 0$) and discharged (when $i_u(t) < 0$) faster than the other SMs. Consequently, that SM will be selected by the sorting and selection algorithm to be inserted and bypassed very often, resulting in a higher switching frequency operation compared to the other SMs. The situation will be opposite in the case when one SM has a higher C_i than the rest. In that case, the switching frequency of that SM will be lower, since the charging and discharging processes of the SM with a high value of C_i is slower, while the other SMs will be penalized to be inserted and bypassed more often, as it is summarized in Table II. However, the unequal switching operation has a significant impact only on the switching losses of the S_l, which is usually the device with the highest loading (at unity power factor) [7]-[10]. The turn-on and the turn-off energy of the lower IGBT S_l are much higher than the other IGBT from the SM. This is due to the even higher amplitude of conduction current and higher junction temperature, which is a consequence of the unbalanced conduction losses (as it will be shown in Figs. 6 (a) and (c)).

Notably, the thermal unbalance is very crucial in the MMC HVDC application, where the operating power factor of the converter is usually close to unity and the junction temperature T_j of the lower IGBT S_l is significantly higher than the other devices in SM. Normally, the heat sink and the cooling

systems are designed to ensure that the junction temperature T_j of the lower IGBT S_l is within a safety limit (e.g., below 150 ºC). However, the increase in the junction temperature T_j of the lower IGBT S_l caused by the thermal unbalance (i.e., when SM has a low capacitance C_i) can exceed the safety limit and damage the power devices. Therefore, the thermal balancing control strategy is needed.

Proposed Thermal Balancing Control (TBC) Strategy

In order to solve the above presented issues, the thermal balancing control is proposed by combing the junction temperature T_j and the capacitor voltage v_{cu} when the unsorted list $L[N]$ is created by means of a weight function. Here, the junction temperature of the lower IGBT S_l is used for balancing, since it is the most critical device with the highest device loading in most cases [7]. A flow chart of the proposed algorithm is shown in Fig. 5. Specifically, the SM capacitor voltage v^i_{cu} and the arm current i_u are first measured and the device junction temperature T_j is estimated based on the thermal model presented in Fig 3. Then, each SM capacitor voltage v^i_{cu} and junction temperature T^i_j are normalized with their average value (v^{avg}_{cu} and T^{avg}_j), in order to obtain the deviation of the v^i_{cu} and the T^i_j as

$$v^{avg}_{cu} = \sum v^i_{cu} / N$$
$$T^{avg}_j = \sum T^i_j / N$$
$$v^i_{norm} = | v^i_{cu} - v^{avg}_{cu} | / v^{avg}_{cu}$$
$$T^i_{norm} = (T^i_j - T^{avg}_j) / T^{avg}_j$$

where v^i_{norm} and T^i_{norm} are the deviation in the capacitor voltage and the junction temperature, respectively. If the deviation in the junction temperature T^i_{norm} is larger than the limit ΔT_j and the deviation in the capacitor voltage v^i_{norm} is still within the limit Δv_{cu}, the TBC strategy is enable and a weight parameter $\alpha = \alpha_0$ is assigned when calculating the element L_i in the unsorted list $L[N]$ as:

$$L_i = (1-\alpha) \cdot v^i_{norm} - \alpha \cdot T^i_{norm} \cdot \mathrm{sign}(i_u) \quad (4)$$

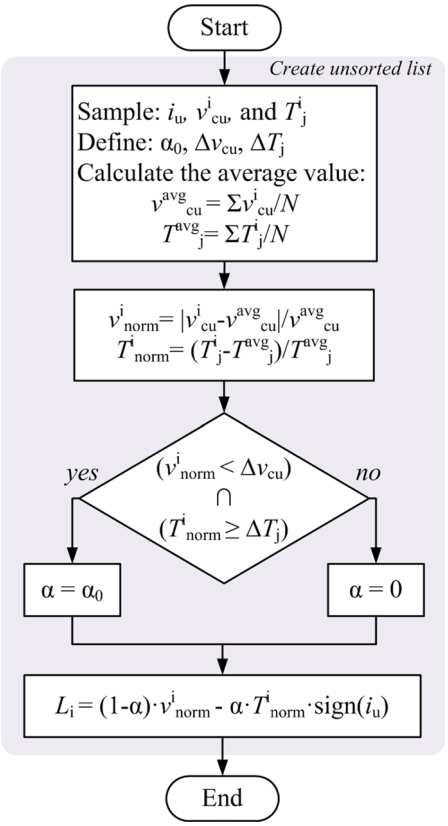

Fig. 5: Flow chart of create unsorted list process with the proposed TBC strategy.

Table III: System parameters and operating condition of MMC in simulation.

Rated active power	$P = 5$ MW
DC-link voltage	$v_{dc} = 6$ kV
Grid voltage (RMS)	3.3 kV
Grid frequency	50 Hz
Short Circuit Ratio (SCR) at the PCC	0.1 p.u.
Arm inductance	$L_{arm} = 0.173$ mH
Nominal submodule capacitance (1 p.u.)	$C_i = 10.25$ mF
Number of submodule	$N = 6$
Nominal switching frequency	$f_{sw} = 1150$ Hz
Weight parameter	$\alpha_0 = 0.5$
Capacitor voltage deviation limit	$\Delta v_{cu} = 0.1$ p.u.
Junction temperature deviation limit	$\Delta T_j = 0.05$ p.u.

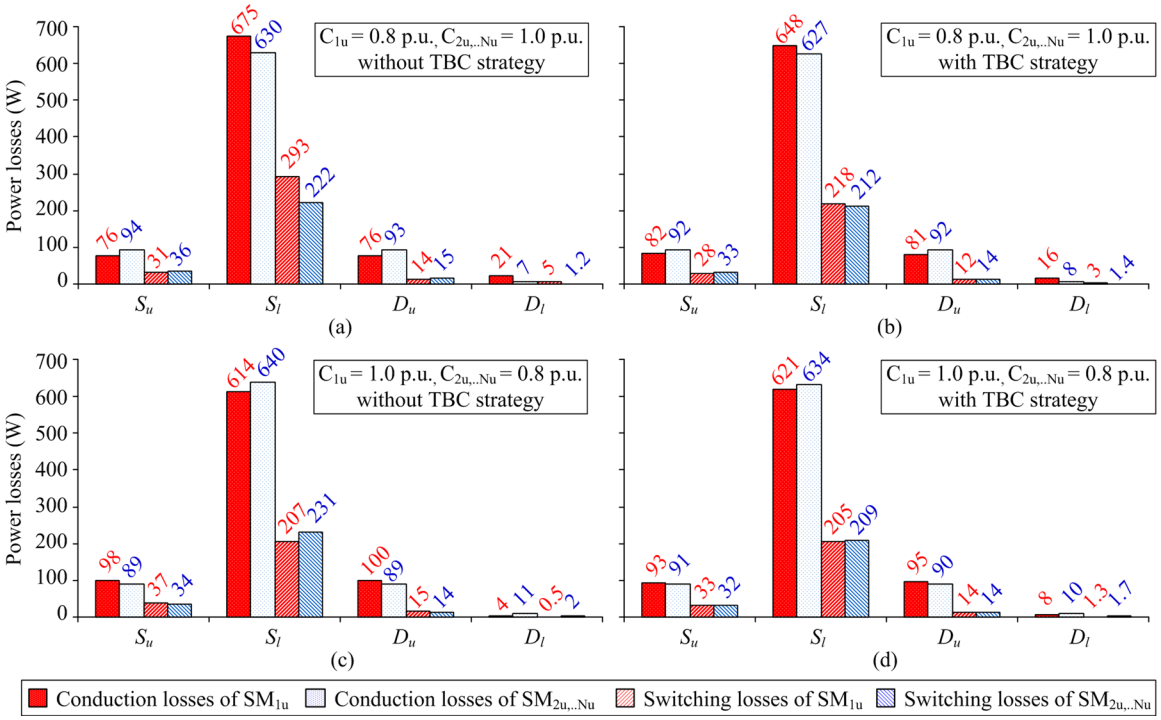

Fig. 6: Power losses in the submodule when C_{1u} = 0.8 p.u. and $C_{2u,..Nu}$ = 1.0 p.u. with (a) the sorting and selection algorithm and (b) the thermal balancing control, and when C_{1u} = 1.0 p.u. and $C_{2u,..Nu}$ = 0.8 p.u. with (c) the sorting and selection algorithm and (d) the thermal balancing control.

The weight parameter α_0 can take a value from 0 to 1, which has to be optimally designed in order to balance both the v_{cu} and T_j (e.g., α_0 = 0.5 for equal balance of capacitor voltage v_{cu} and junction temperature T_j). However, if the deviation in the capacitor voltage v^i_{norm} is above the limit Δv_{cu} (e.g., 0.1 p.u.), the priority will be given to the balancing of the capacitor voltage, in order to prevent the SM from permanent damage. This can be done by assigning the weight parameter as α = 0, which is simply equivalent to the case of normal capacitor voltage balancing. In addition, the arm current direction sign(i_u) has to be multiplied with the weight function α, since the sorting and selection algorithm sorts the list in the opposite order when the arm current direction changes. By doing so, a new list $L[N]$ which contains both the capacitor voltage v_{cu} and the device junction temperature T_j information is then created and used in the sorting and selection algorithm (see Fig. 4). With the use of the proposed solution, the deviation in the capacitor voltage v^i_{norm} will be imposed by the deviation in the device junction temperature T^i_{norm} through the weight function α. Thus, the balancing of both the capacitor voltage v_{cu} and the device junction temperature T_j can be achieved.

Validation of the Proposed Thermal Balancing Control Strategy

The performances of the proposed thermal balancing control strategy are validated through simulations for a 5 MW three-phase MMC with the system parameters given in Table III. Two worst case scenarios were considered, case 1: C_{1u} = 0.8 p.u. and $C_{2u,..Nu}$ = 1.0 p.u., and case 2: C_{1u} = 1.0 p.u. and $C_{2u,..Nu}$ = 0.8 p.u.. The MMC operates at unity power factor, which is the case where the loading of the power devices is the most unequal and thus it gives the most challenge to maintain the balance (e.g., the lower IGBT S_l has a significant high loading) [7]. Notably, the power losses in these two cases are not comparable, since the total energy in the arm is not equal, due to the unequal total arm capacitance. However, it represents the realistic scenarios when one SM is ageing faster than the others (case 1) and one SM has been replaced by a new SM (case 2).

The comparison between power losses of each power device in the SM_{1u} and the $SM_{2u,..Nu}$ is shown in Fig. 6. It can be cleary seen from Fig. 6(a) that the power losses of each power device in the SM_{1u} and the $SM_{2u,..Nu}$ are unbalanced, when C_{1u} = 0.8 p.u. and $C_{2u,..Nu}$ = 1.0 p.u. without the TBC strategy. As a consequence, the unbalacned junction temperature T_j is observed in Fig. 7(a), especially in the lower

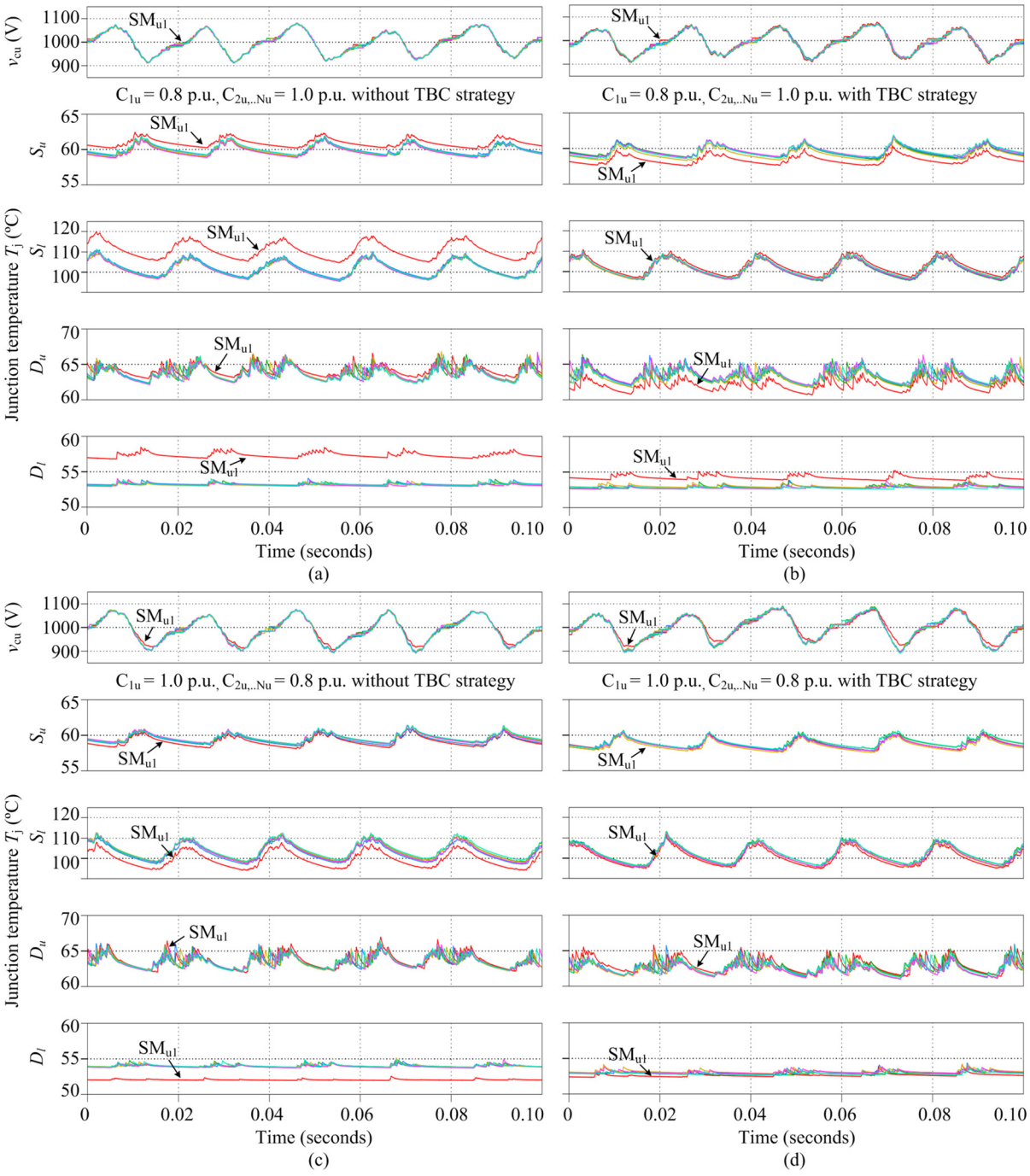

Fig. 7: Capacitor voltage and device junction temperature of the submodule when C_{1u} = 0.8 p.u. and $C_{2u,..Nu}$ = 1.0 p.u. with (a) the sorting and selection algorithm and (b) the TBC algorithm, and when C_{1u} = 1.0 p.u. and $C_{2u,..Nu}$ = 0.8 p.u. with (c) the sorting and selection algorithm and (d) the TBC algorithm.

IGBT S_l of the SM_{1u} (indicated by the red plot). It can be seen from Fig. 7(b) that the proposed TBC strategy can effectively balance the junction temperature T_j of the lower IGBT S_l. In this case, the junction temperature of all the devices from the SM is also reduced, and the power losses of the power devices in the SM_{1u} and the $SM_{2u,..Nu}$ are almost equal, as it can be seen from Fig. 6(b). The performances of the TBC strategy are also verified in another situation when C_{1u} = 1.0 p.u. and $C_{2u,..Nu}$ = 0.8 p.u.. Similarly, the power losses of all the devices are more equal and the junction temperature T_j of the lower IGBT S_l is well balanced with the proposed solution, as it can be seen from Figs. 6(d) and 7(d). In this case, the junction temperature T_j of the $SM_{2u,..Nu}$ are reduced (e.g., upper IGBT S_u and lower Diode D_l) compared to those in Fig. 7(c). The effectiveness of the TBC strategy can also be evaluated by considering the switching frequency f_{sw} and the insertion duty D_{INS} of the SMs as well,

where it can be seen from Table II that the switching frequency f_{sw} is almost equal in all SMs when the TBC is adopted. The difference in the insertion duty D_{INS} between the SM_{1u} and the $SM_{2u,..Nu}$ is also reduced. It can be noticed in Figs. 7 (b) and (d) that the capacitor voltage v_{cu} is less balanced, which is a trade-off when the TBC strategy is adopted. Nevertheless, it is still in the limit (e.g., 10% of the nominal value) and it has a minor effect on the operation of the MMC.

Conclusion

A thermal balancing control has been proposed by enhancing the sorting and selection algorithm for MMC, where the junction temperature of the devices is also taken into consideration in addition to the capacitor voltage. The proposed method uses a weight function to create a combined voltage-temperature list for the sorting and selection process, which is a simple and effective solution. The simulation results verify the effectiveness of the thermal balancing control strategy in terms of balancing both the capacitor voltage and the junction temperature, when the unbalanced thermal behavior is introduced.

Appendix – Losses Calculation

The power losses calculation is required in order to estimate the device junction temperature used in the TBC strategy. For the half-bridge SM, the power losses can be simply divided into two parts: the conduction losses and the switching losses (or the reverse-recover losses for the Diode). In order to determine the power losses, the on-state characteristic of the power devices has to be first calculated, which in general can be approximated by the linear equation as

$$v_{\text{on}} = \begin{cases} v_{\text{CE0}} + i_S r_S & \text{, IGBT} \\ v_F + i_D r_D & \text{, Diode} \end{cases}$$

where v_{on} is the on-state voltage of the device. i_S and i_D the IGBT and Diode conducting current. v_{CE0} is the collector-emitter saturation voltage of IGBT and v_F is the forward voltage of Diode. r_S and r_D are the slope resistance of IGBT and Diode. Then, the switching characteristic of the devices is determined from the switching energy E_{sw} as

$$E_{\text{sw}} = \begin{cases} E_{\text{on}} + E_{\text{off}} & \text{, IGBT} \\ E_{\text{rec}} & \text{, Diode} \end{cases}$$

with E_{on} being the turn-on energy and E_{off} being the turn-off energy of IGBT. E_{rec} is the reverse-recovery energy of Diode. Although the above device characteristics can be obtained from the datasheet, the following parameters are not constant during the operation: v_{CE0}, v_F, r_S, r_D, E_{on}, E_{off}, E_{rec}, dependent to the device junction temperature. Thus, it is proposed in [8] to use a linear interpolation to approximate these parameters according to the device junction temperature as

$$x(T_{\text{j}}) = (x_{150} - x_{125})\frac{T_{\text{j}} - 125}{25} + x_{125}$$

where the subscript x_{125} and x_{150} are the parameter values at 125 ºC and 150 ºC, respectively. Then, the instantaneous conduction losses and switching losses of the power device can be calculated as it is summarized in Table IV and then fed into the thermal model in Fig. 3.

Table IV: Instantaneous losses calculation for device in half-bridge SM.

Device	Conduction losses	Switching losses
IGBT	$(v_{\text{CE0}} + i_S r_S) \cdot i_S$	$(E_{\text{on}} + E_{\text{off}}) \cdot f_{\text{sw}}$
Diode	$(v_F + i_D r_D) \cdot i_D$	$E_{\text{rec}} \cdot f_{\text{sw}}$

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