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# Increasing Emitter Efficiency in 3.3-kV Enhanced Trench IGBTs for Higher Short-Circuit Capability

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**Abstract**—In this paper, a 3.3-kV Enhanced Trench IGBT has been designed with a high emitter efficiency, for improving its short-circuit robustness. The carrier distribution profile has been shaped in a way that it is possible to increase the electric field at the surface of the IGBT, and thereby, counteract the Kirk Effect onset. This design approach is beneficial for mitigating high-frequency oscillations, typically observed in IGBTs under short-circuit conditions. The effectiveness of the proposed design rule is validated by means of mixed-mode device simulations. Then, two IGBTs have been fabricated with different emitter efficiencies and tested under short circuit, validating that the high-frequency oscillations can be mitigated, with higher emitter efficiency IGBT designs.

## I. INTRODUCTION

In practical applications, power semiconductor devices are exposed to a number of severe stresses, that they need to successfully pass without compromising the reliability of the whole system [1]–[3]. Electrical failures in power semiconductor devices are a cause of concern, especially under severe overloads, such as short circuits, where the device operates at its limits [4]. Insulated-Gate Bipolar Transistors (IGBTs) have shown good capability of surviving short circuits, for a certain limited of time [5]. Nevertheless, as the IGBT technology evolves, towards achieving high power density and further optimization of the technology curve, the stable operation of the IGBT under short-circuit may be compromised. For example, one type of instability typically observed in IGBTs during a short-circuit event is the occurrence of high-frequency gate voltage oscillations (i.e., range of 20 MHz). While many solutions have been proposed [6]–[9], this problem still persists and is even still aggravated in today's IGBT technologies.

Several experimental evidence of such high-frequency oscillations can be found in [6] for planar IGBTs and, recently, also for trench-gate, field-stop IGBTs [10]. This instability may cause the destruction of the gate-oxide, in case that the oscillation amplitude diverges out of control, as reported in [11]. Previous studies have pointed out that during short circuit, the IGBT presents a rotated electric field shape (Kirk Effect), which is a very unstable condition [12], [13]. The electric field gradient can be calculated with the Poisson equation, given as:

$$\frac{dE}{dx} = \frac{q}{\epsilon_s}(N_D + h - e) \quad (1)$$

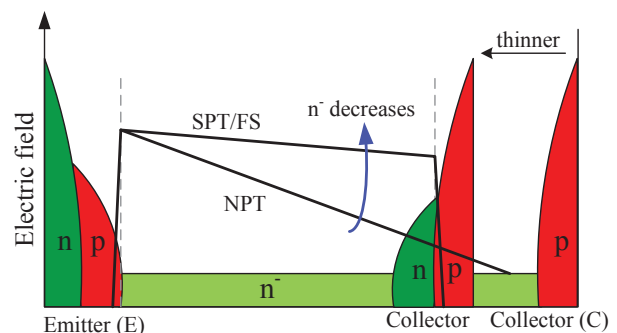


Fig. 1. Evolution of the IGBT technology depending on different vertical designs and its correlation with the electric field: NPT - Non-Punch-Through, SPT - Soft-Punch Through, FS - Field Stop.

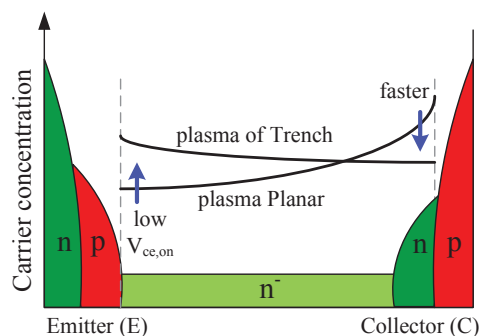


Fig. 2. Evolution of the IGBT cell design for better trade-off between switching and conduction losses.

where  $\epsilon_s$  is the dielectric permittivity of the semiconductor,  $q$  is the electron charge,  $N_D$  is the drift doping concentration,  $h$  is the hole density and  $e$  is the electron density.

The Kirk Effect onset is closely related with the IGBT design and becomes more critical as the IGBT technology evolves:

- 1) Vertical IGBT design (i.e., Non-Punch Through NPT, Punch-Through PT, Soft-Punch Through SPT or Field Stop FS). As the cell structure becomes thinner from NPT or conventional PT to SPT technologies, the doping concentration in the drift layer is decreased to achieve similar blocking capability. This means that the gradient

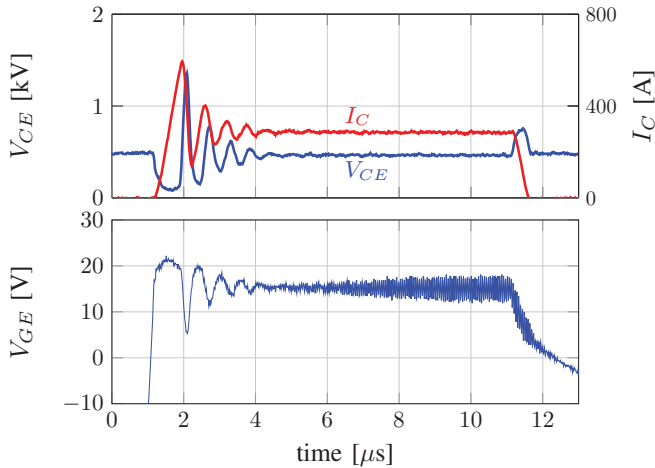


Fig. 3. Short-circuit behaviour of a 3.3-kV SPT Enhanced-Trench IGBT at  $V_{DC} = 500$  V and  $T_{case} = 25^\circ\text{C}$ .

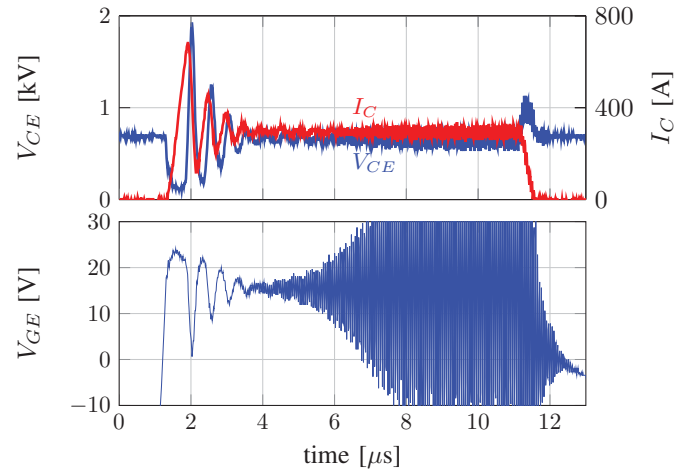


Fig. 4. Short-circuit behaviour of a 3.3-kV SPT Enhanced-Trench IGBT at  $V_{DC} = 700$  V and  $T_{case} = 25^\circ\text{C}$ .

of the electric field becomes flatter and it may eventually rotate (see Fig. 1).

- 2) IGBT cell topology (i.e., planar, trench, enhancement layers, Side Gate). As the cell evolves from planar to trench designs, the trend is to reduce on-state losses by increasing the electron current density (majority carriers). This, in turn, may set the conditions for having a rotated electric field. Furthermore, if the hole carrier density (minority carriers) is relatively small, for achieving faster IGBT devices, the electric field would rotate even more (see Fig. 2),

The Kirk Effect in IGBTs is related with the root cause of such high-frequency oscillations. In [14], it has also been found that such oscillation phenomenon can be recognized as a parametric oscillation, whose time-varying element is the Miller capacitance. In [14], it has been demonstrated that it is possible to relate the electric field distortions to gate capacitance variations, and associate the capacitance variation with charge-storage effects, occurring at the surface of the IGBT.

With the purpose of mitigating the oscillation phenomenon, care must be taken into the shaping of the carrier profile in IGBTs. We need to ensure that the electric field of the IGBT does not rotate - especially under short circuit. There are several possibilities to shape the carrier profile, the most widely used are: high-injection-efficiency emitters, profiled lifetime control techniques, increase of the doping concentration in the drift region and reduction of the electron injection from the MOS-channel [15]. Among them, the increase of the emitter efficiency has been selected in this work.

## II. CASE HISTORIES - PRACTICAL EXAMPLES

The short-circuit performance of a single-chip 3.3-kV Enhanced-Trench IGBT with Soft Punch Through (SPT) buffer is investigated. In the following it will be demonstrated that IGBTs are prone to an instability mechanism, if they are

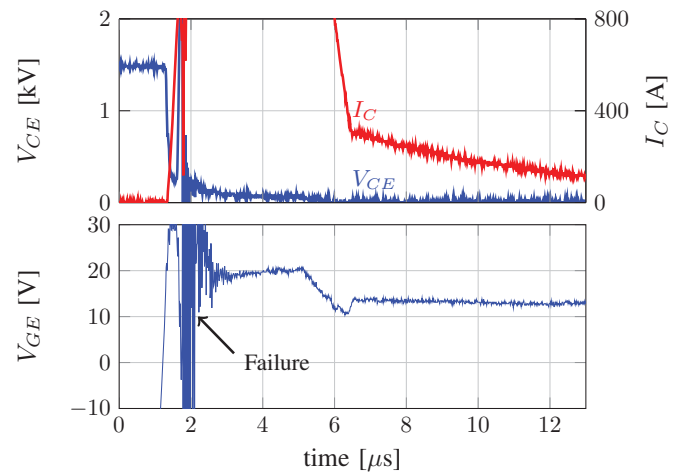


Fig. 5. Short-circuit failure of a 3.3-kV SPT Enhanced-Trench IGBT at  $V_{DC} = 1500$  V and  $T_{case} = 25^\circ\text{C}$ .

not optimized for short-circuit operation. The instability may lead to high-frequency oscillations, best seen in the gate voltage waveform. The knowledge and awareness of this high-frequency oscillatory behaviour have been reported by others, and while many solutions have been put forward, this problem has become a true challenge since solutions have not been fully effective.

Figs. 3 and 4 show the short-circuit performance of a 3.3-kV SPT Enhanced-Trench IGBT at a DC-link voltage of 500 V and 700 V, for a short-circuit pulse of 10  $\mu\text{s}$  and case temperature of 25°C. These experiments have been done for a gate-emitter voltage equal to -10/+15V, gate resistance of  $R_g = 2.2$   $\Omega$  and collector inductance of  $L_c = 530$  nH. It can be observed that the short-circuit robustness is severely compromised by the occurrence of oscillations. Two oscillation frequencies can be seen. The high frequency one, which is the main focus in this paper, is about 20 MHz. The low-frequency one, which

is associated with the large inductance of the commutation loop, is about 2 MHz. Additionally, the DC-link voltage has been increased up to 1500 V in Fig. 5. In this case, the IGBT catastrophically fails, being the high-frequency oscillations the sign of the device failure.

### III. IGBT SIMULATION MODEL

#### A. IGBT design

To analyze the IGBT short circuit behavior, mixed-mode device simulations have been carried out, using the TCAD Sentaurus simulation tool. The doping profile of the 3.3-kV Enhanced-Trench IGBT and the circuit model used to perform the short circuit simulations are shown in Fig. 6. Only the emitter side is presented in Fig. 6, showing that an n-enhancement layer and a lightly doped p-well region have been implemented. The collector side, which is not shown in Fig. 6, has a Soft-Punch Through (SPT) buffer.

The IGBT model has been calibrated to match the real characteristics of the tested devices. The drift region has a thickness of  $370 \mu\text{m}$  and a doping level of  $1 \cdot 10^{13} \text{ cm}^{-3}$ . These values have been selected to achieve a blocking voltage of 3,300 V. The trench cell has an n-type enhancement layer

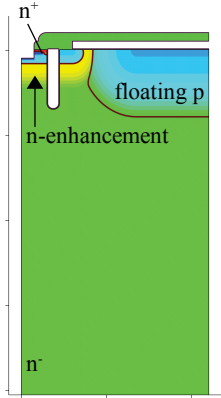


Fig. 6. The 3.3-kV enhanced-trench IGBT half cell.

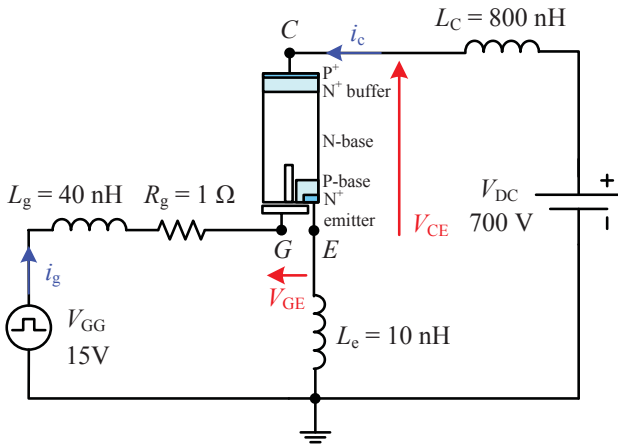


Fig. 7. Circuit to perform the short-circuit simulations with TCAD.

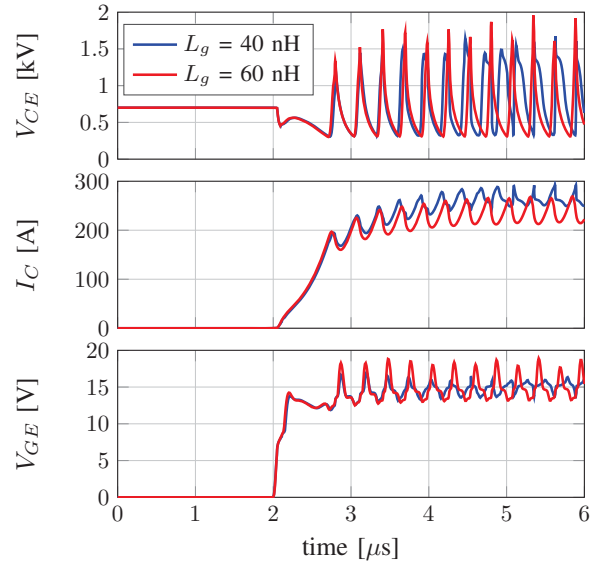


Fig. 8. Short-circuit simulation showing the oscillation dependency as a function of the gate inductance  $L_g$ .

surrounding the p-well layer, which is a well-established solution to improve the trade-off between on-state drop and switching losses [16]. The p-well layer depth is  $2 \mu\text{m}$  and the n-enhancement layer extends up to  $5 \mu\text{m}$ . An additional floating  $p^+$  layer has been implemented in the region between adjacent active cells, with the aim to reduce the gate input capacitance, while providing an optimum blocking capability. This layer has a depth of  $8 \mu\text{m}$  and doping level of  $1 \cdot 10^{18} \text{ cm}^{-3}$ . The effective area of the IGBT is  $0.4 \text{ cm}^2$ , yielding a nominal current of 50 A.

The short-circuit simulations have been carried out including the external circuit of Fig. 7, whose values are selected to be in agreement with the experimental setup, but also favouring the occurrence of the oscillation phenomenon. Since the stray inductances are involved in the oscillation phenomenon, not being the main triggering mechanism but taking part of it, the dependence of the gate inductance and collector inductance in respect to the oscillation phenomenon is investigated in the following.

#### B. Effect of gate inductance

The variation of the gate stray inductance  $L_g$  and its impact on the short-circuit oscillation phenomenon in the Trench IGBT has been evaluated. Simulations have been carried out with different gate inductance values, keeping the rest of the parameters constant. The simulation results show a similar trend, as previously investigated for the planar IGBTs in [17]. In Fig. 8 it is observed that the gate inductance,  $L_g$ , affects the IGBT short-circuit behaviour in two ways:

- 1) With higher gate inductance  $L_g$ , an increased oscillation amplitude on the gate voltage waveform can be observed.
- 2) The oscillation frequency increases with decreasing  $L_g$ .

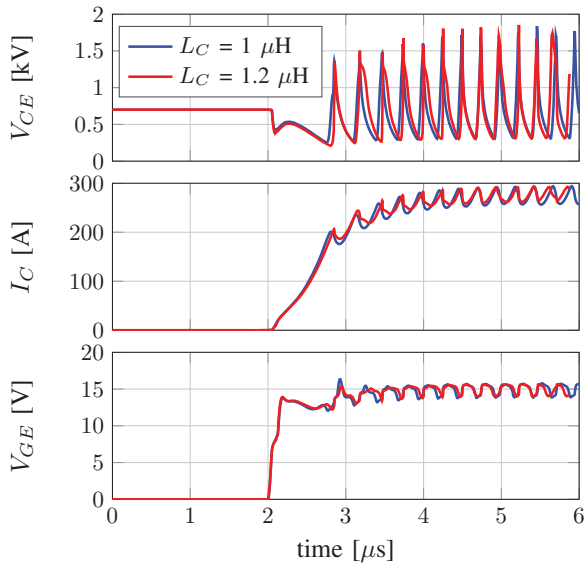


Fig. 9. Short-circuit simulation showing the oscillation dependency as a function of the collector inductance  $L_C$ .

### C. Effect of collector inductance

The impact of the collector stray inductance  $L_C$  variation on the short-circuit oscillation phenomenon in the Trench IGBTs has also been evaluated. The contribution of the collector inductance to the short-circuit oscillation phenomenon for Trench IGBTs is also similar as for planar IGBTs in [17]. In Fig. 9, the collector inductance,  $L_C$ , affects the IGBT short-circuit behaviour in three ways:

- 1) The gate oscillation amplitude does not change as a function of  $L_C$ .
- 2) The oscillation frequency increases with decreasing  $L_C$ .
- 3) With higher  $L_C$ , an increased undershoot across the collector-emitter voltage can be observed.

## IV. DESIGN OF THE IGBT FOR BETTER SHORT-CIRCUIT RUGGEDNESS

### A. Short-circuit optimized IGBT design

In this section, a thorough analysis on how to improve the short circuit ruggedness in Trench IGBTs is presented. In [14], it has been pointed out for the first time that a parametric oscillation takes place during the IGBT short circuit, whose time-varying element is the Miller capacitance, leading to the amplification mechanism. This occurs when the electric field at the emitter side of the IGBT becomes too weak, as a consequence of the electric field rotation. One option to achieve a stronger electric field at the surface of the IGBT is to increase the hole concentration; for example, by increasing the emitter efficiency of the  $PNP$  transistor. This can be done by selecting a higher peak doping concentration of the  $p^+$  collector layer, thereby increasing the effective charge concentration and counteracting the Kirk Effect. By doing so, the electric field peak at the collector decreases due to the

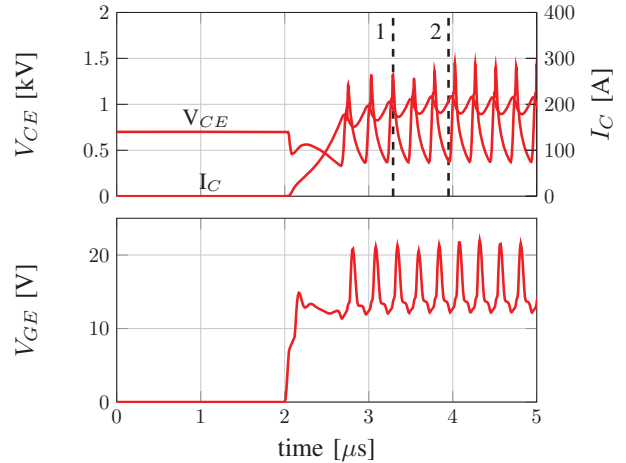


Fig. 10. The 3.3-kV IGBT with  $p^+$  collector doping of  $1 \cdot 10^{17} \text{ cm}^{-3}$ .

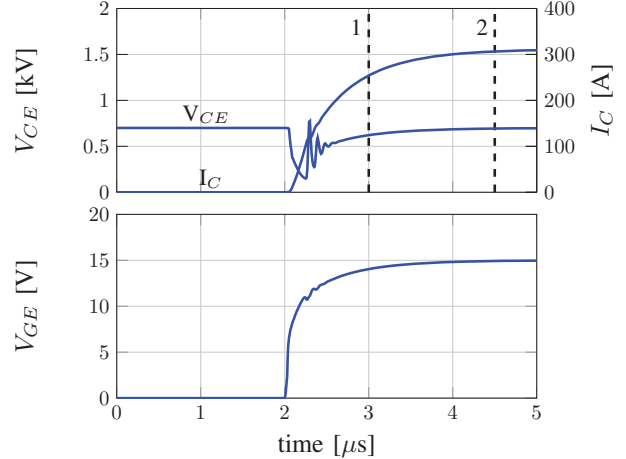


Fig. 11. The 3.3-kV IGBT with  $p^+$  collector doping of  $3 \cdot 10^{17} \text{ cm}^{-3}$ .

higher injection of holes. This means that the electric field strength at the emitter side must increase to compensate for the loss of the area below the electric field curve at the emitter, and therefore support the same collector voltage.

Figs. 10 and 11 show the short-circuit simulations of the 3.3-kV enhanced trench IGBT, having the same doping profiles but employing different collector doping concentrations of  $1 \cdot 10^{17} \text{ cm}^{-3}$  and  $3 \cdot 10^{17} \text{ cm}^{-3}$ , respectively. It is clear that the adjustment of the doping concentration at the collector brings the benefit of improving the stability of the device during short circuit. By adopting this strategy, oscillations are mitigated with high emitter efficiency IGBTs (i.e., higher  $p^+$  collector doping).

A better understanding of the phenomena taking place inside of the IGBT can be gained by looking at Figs. 12 and 13. The evolution of the 2-D electron density effects together with the electric field fluctuation along a vertical cut of the IGBT can be figure out in those pictures. In Fig. 12, it can be observed that for IGBTs with low emitter efficiencies, the electron density continuously varies during each oscillation cycle between two

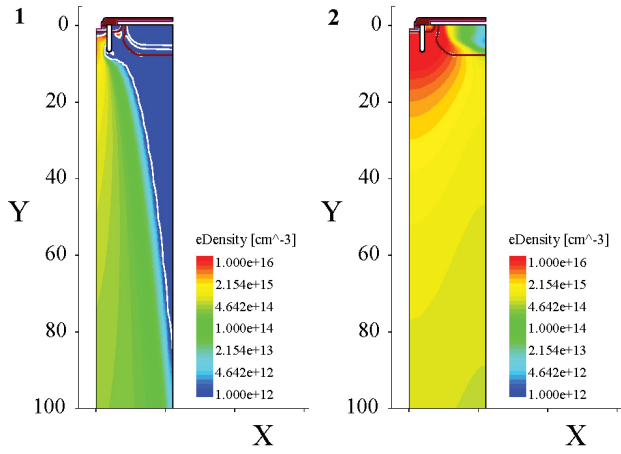


Fig. 12. Short-circuit behaviour of the 3.3-kV Enhanced-Trench IGBT with  $p^+$  collector doping of  $1 \cdot 10^{17} \text{ cm}^{-3}$ , at the time instants 1 and 2 of Fig. 10. Top: electron density; bottom: electric field.

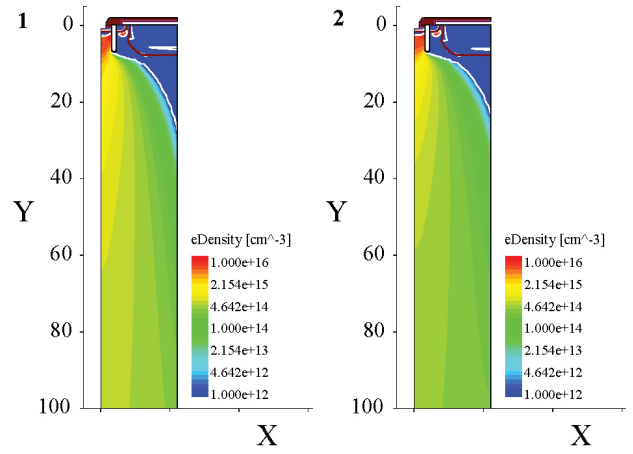


Fig. 13. Short-circuit behaviour of the 3.3-kV enhanced-trench IGBT with  $p^+$  collector doping of  $3 \cdot 10^{17} \text{ cm}^{-3}$ , at the time instants 1 and 2 of Fig. 11. Top: electron density; bottom: electric field.

situations:

- 1) Electrons flow vertically coinciding with an electric field stronger at the emitter. This occurs when  $V_{CE}$  is the highest in Fig. 10 (condition 1 in Fig. 10).
- 2) Electrons accumulate at the surface of the IGBT, coinciding with an electric field peak stronger at the collector. This occurs when  $V_{CE}$  is the lowest in Fig. 11 (condition 2 in Fig. 10).

This phenomenon leads to a time-varying capacitance coinciding with a high capacitance when the charges are accumulated at the surface (e.g. condition 2) and having a small capacitance when there are no-charge storage effects (e.g. condition 1). This behavior has been recognized as a parametric oscillation in [14].

Furthermore, Fig. 13 illustrates the 2D-plots with an IGBT design having a higher emitter efficiency. In this case, the electron charge-storage effect is not observed. Now the electric field becomes dominant over the high electron injection from the MOS-channel, resulting in a fixed carrier profile, which no longer changes with time. In this way, the Miller capacitance does no longer vary with time and the oscillations during short circuit are not observed. This is demonstrated in Fig. 11, where

oscillations do not take place.

### B. Effect of stray inductance

The proposed IGBT design strategy has been demonstrated to be effective by considering the circuit design parameters included in Fig. 7. The next step is to validate that IGBT designs having high emitter efficiencies also show a good short-circuit robustness, when other stray inductances are considered. As a first step, the 3.3-kV Enhanced-Trench IGBT has been simulated with two different gate inductances of 40 nH and 80 nH, keeping  $L_C = 1.2 \mu\text{H}$  and  $L_e = 10 \text{ nH}$ . Fig. 14 demonstrates that high-frequency oscillations during short-circuit are no longer observed, regardless of variations in the gate inductance. Then, the 3.3-kV Enhanced-Trench IGBT has been simulated with two different collector inductances of 1  $\mu\text{H}$  and 1.2  $\mu\text{H}$ , keeping  $L_g = 40 \text{ nH}$  and  $L_e = 10 \text{ nH}$ . Once again, Fig. 15 shows that oscillations are not triggered, despite the large collector inductance. These simulation results prove that the short-circuit operation of high emitter efficiency IGBTs is stable under different circuit designs.

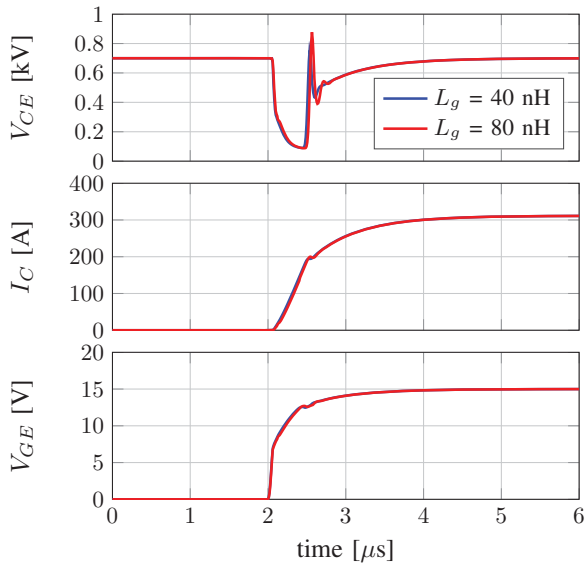


Fig. 14. Stable short-circuit behaviour of the 3.3-kV Trench IGBT having high-emitter efficiency under different gate inductances.

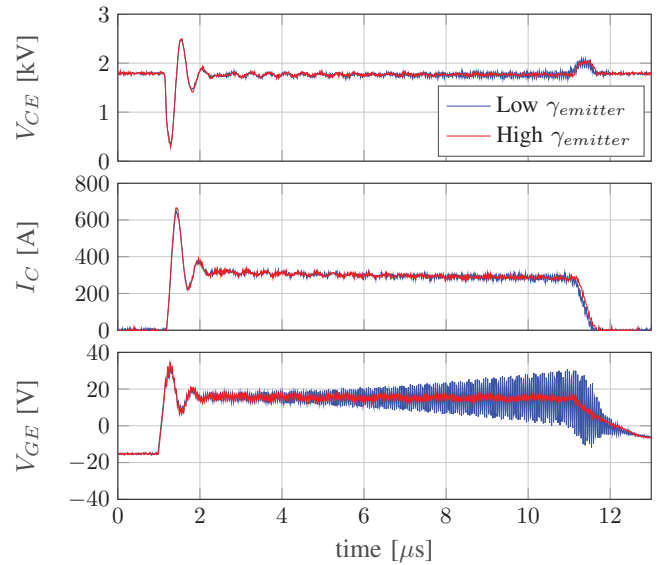


Fig. 16. Short-circuit experiments of the 3.3-kV trench IGBTs with different emitter efficiencies.  $R_{g,on} = 2.2 \Omega$ ,  $L_\sigma = 600 \text{ nH}$  and  $T_{case} = 25^\circ\text{C}$ .

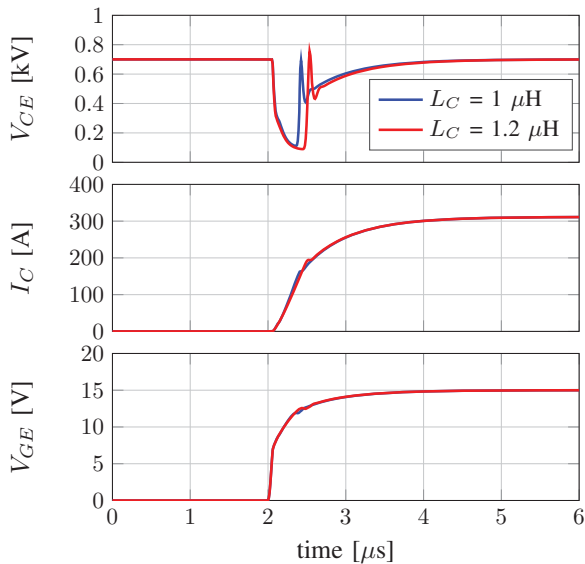


Fig. 15. Stable short-circuit behaviour of the 3.3-kV Trench IGBT having high-emitter efficiency under different collector inductances.

## V. SHORT CIRCUIT EXPERIMENTS

The IGBT short-circuit capability of the 3.3-kV Enhanced-Trench (ET) IGBT with Soft Punch Through (SPT) buffer is experimentally assessed. Fig. 16 shows the short-circuit behaviour of the 3.3-kV ET-IGBTs fabricated with two different emitter efficiencies, named as low  $\gamma_{emitter}$  and high  $\gamma_{emitter}$  in Fig. 16. All design parameters except for the  $p^+$  collector dose were the same for the two devices. As shown, the oscillations are better observed with low emitter efficiency designs, in agreement with the simulations results. Because of the lower emitter efficiency, a decrease in the hole current

injection from the collector is expected, revealing its large impact on the short-circuit instability of the device. The benefit of employing an IGBT with a high emitter efficiency design is that the on-state losses can be minimized, because the plasma of the IGBT is increased. However, this improvement comes at the expense of increased turn-off losses because the excess charge needs to be removed at turn-off. One must not forget that if the device is designed for low switching frequency applications it is better to optimize on-state losses, which also bring the possibility to improve the short-circuit capability, and accept higher turn-off losses.

## VI. DISCUSSION

The short-circuit performance of IGBTs is mainly determined by the carrier distribution profile and the associated electric field shape, which can be adjusted in several ways, in order to achieve the optimum distribution. In practice, IGBTs are optimized to achieve the lowest possible voltage drop in the on-state phase. This means that a high plasma should build up across the whole IGBT. On the other hand, IGBTs are also optimized to reduce turn-off losses, arising when the excess charge is removed. This means that the plasma should be reduced at the collector side. These two strategies can be effectively implemented and also ensuring high short-circuit robustness. To achieve this, one should consider the following design rules:

- 1) *Carrier enhancement at the emitter for low on-state losses.* The IGBT can be designed to have a dense plasma near the emitter by adopting Trench cell designs [18], implementing n-enhancement layers [19] or by reducing the mesa width between trenches [20]. Modern IGBTs, which are designed in accordance with one of these approaches, have to provide a sufficient hole injec-



tion from the collector side. This will avoid the rotation of the electric field under short-circuit conditions.

- 2) *Carrier reduction at the collector for low turn-off losses.* The IGBT can be designed with relatively low carrier concentration at the collector, by employing IGBTs with low injection efficiencies or by localized lifetime control techniques [15]. Modern IGBTs, which are designed in accordance with one of these approaches, have to provide a smaller electron injection from the MOS channel. This will avoid the rotation of the electric field under short-circuit conditions.
- 3) *Reduction of the thickness for low losses.* The IGBT thickness has been reduced with its evolution along time. The purpose is to minimize the total losses because the resistance of the device during the on-state phase decreases as a result of the lower thickness. At the same time, to achieve the desired blocking capability for thinner devices, the doping concentration in the drift region is reduced. Modern IGBTs, which are designed in accordance with this approach, have to ensure that the relation between electrons and holes is optimum to guarantee that the effective charge density is positive. This will avoid the rotation of the electric field under short-circuit conditions.

## VII. CONCLUSIONS

A study of the short-circuit behavior in modern IGBTs is presented in this work. It has been demonstrated that employing IGBTs with high emitter efficiencies lead to an improved short-circuit robustness. By doing so, the electric field is effectively increased at the surface of the IGBT and charge-storage effects are no longer observed. The advantage of applying this method is that high-frequency oscillations in the range of 20 MHz disappear, and failure mechanisms of this type are better understood. The main drawback of this approach is the increase in switching losses, but on the other hand, conduction losses can be further minimized. The proposed method has been validated through finite-element simulations, which are coherent with the experimental test in a 3.3-kV Enhanced-Trench IGBTs having different collector doping concentrations. Although future improvements are possible, high voltage Enhanced-Trench IGBTs with Soft-Punch Through buffers have already been optimized including short-circuit reliable operation.

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