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***Abstract*—The three level neutral-point clamped (3L-NPC) topology is one of the most widely used multilevel topologies in the low and medium voltage applications and also one of the most commercialized topologies. Although it offers many benefits compared to the conventional two level topology, it suffers from a considerable unequal loss distribution among the inner and outer switches and the clamping diodes. To solve this problem, we are proposing a control algorithm based on the finite control set model predictive control (FCS-MPC) that can provide a more balanced stress distribution. For implementing the proposed control algorithm no additional measurements are required nor thermal models of the semiconductor devices. The algorithm benefits are even more noticeable during low voltage ride through (LVRT) scenarios when the output voltage level of the converter is low and the current amplitude is high. Obtained simulation results confirm the positive effects on the thermal redistribution and also the junction temperatures of the most stressed devices are reduced. Effects of the algorithm are also verified on an experimental set-up.**

I. Introduction

Since it was first introduced in 1981 as an alternative to the conventional voltage source inverter [1], the neutral point clamped (NPC) topology has been widely used in medium voltage applications and nowadays also in low voltage applications [2], [3]. As it can provide a lower harmonic distortion of the output voltage and can follow the high power rating trend of renewable energy sources, power electronics converter manufacturers have implemented this topology into their solutions for interconnection of the renewable energy sources or to supply the variable speed drives [4]–[6]. Although the topology offers many benefits compared to the conventional two level voltage source topology [7], the stress redistribution analysis of the semiconductor devices reveals an unequal stress distribution between the outer and inner switches and a high stress on the clamping didoes. Unequal stress distribution limits the maximum output power of the converter since the power is limited by the maximum permitted thermal stress of the most stressed semiconductor device. Moreover, it will limit the permitted switching frequency and reliability of the converter. The issue of unequal stress distribution is even more evident under low voltage ride through (LVRT) scenarios [8]. In 2001 the active neutral point clamped (ANPC) topology was introduced to eliminate this disadvantage [7], [9]. The clamping diodes were replaced by the active switches but with additional cost of two extra switches, power supplies and gate-drive units. Even though a new topology was introduced, the efforts of solving the thermal redistribution problem by developing a more advanced control algorithm with a better semiconductor stress distribution was still pursued by research groups. Solutions based on two-level modulations for lower modulation indexes were proposed in [10]. The proposed strategy benefits the inherent redundancy among switching states in multilevel inverters to optimally relieve the thermally stressed device. Another possibility to balance the lifetimes of the power devices is an asymmetric power device rating selection method as proposed in [11]. Using the chip size dependent analytical power loss and thermal impedance models, proper chip size for an even temperature distribution in the NPC inverter can be selected. The authors in [8] proposed special space vector modulation (SVM) sequences for LVRT scenarios by reducing the dwelling time of the zero voltage vectors and commutations that involve zero voltage level. The approach was further developed for application using moderate modulation indexes [12]. Another SVPWM method that takes advantage of the redundant space voltage vectors is proposed in [13]. The proposed algorithm continuously evaluates the cost function of the junction temperature of thermally-overheated device for all possible switching sequences set in order to find the optimal relieving switching sequence. A similar concept but with a much simpler implementation is also developed for a carrier-based thermal stresses relief PWM (TSRPWM) method in [14].

All of the before mentioned solutions are based on the linear control algorithms that have limited flexibility and transient response speed due to most common cascaded organization of control loops. On the other hand, model predictive control (MPC) algorithms have emerged as one of the most straightforward solutions for controlling the power converters. In particular, the finite control set model predictive control (FCS-MPC) algorithm has gathered a lot of attention in the power electronics community due to the simple implementation. The control is based on calculating the predictions of the system values using the discrete system model and afterwards solving the optimization problem. For all possible converter's state variables a user-defined cost function is evaluated and the switching state that will produce the minimal cost function

value is then applied. Different control objectives can easily be implemented in the cost function such as minimization of the reference tracking error [15], switching loss minimization [16], harmonics elimination [17], [18], common-mode voltage minimization [19], active thermal control [20] and the device junction temperature spread [21]. Considering the aforementioned problem of the NPC topology, particularly the last two objectives are very interesting for application. In [20] a model for on-line junction temperature estimation is implemented by introducing a new term in the cost function that evaluates the amount of thermal swing. To implement this objective thermal models of the semiconductor devices are needed. The authors further developed the approach in [21] by including the lifetime estimation in the cost function. Using the Miners rule the accumulated damage is calculated for each sampling period. However, this objective demands a lot of information about the semiconductor devices, some of them are provided in data-sheets and manuals but for some reliability experiments are needed. In our paper we present FCS-MPC based algorithm with thermal redistribution that does not need any information about the semiconductor devices nor measurements. Therefore, the algorithm has a simpler implementation as there is no need for additional calculations nor thermal modeling of the devices. The computational effort of the algorithm is also not significantly higher then that of a algorithm with a conventional cost function as presented in [22]. A more equalized stress distribution is achieved between the outer and inner semiconductor switches and the stress on the clamping diodes is also relived.

This paper is organized as follows. In Section II the system model and the FCS-MPC algorithm are described. The proposed algorithm for thermal stress redistribution is explained in Section III. The obtained semiconductor thermal redistributions for conventional and proposed algorithm are presented in Section IV. In Section V the effects of the proposed algorithm are experimentally validated. In the last section conclusions and aspects for future research are provided.

II. System Model

The three level NPC converter has 27 allowed switching states which can produce 19 different voltage vectors. The vectors are typically classified into zero vectors ($V_0 - V_3$), small vectors in the inner hexagon ($V_4 - V_{15}$), medium ($V_{17}, V_{19}, V_{21}, V_{23}, V_{25}, V_{27}$) and large vectors ($V_{16}, V_{18}, V_{20}, V_{22}, V_{24}, V_{26}$) in the outer hexagon as seen in the Fig. 1. As the applied FCS-MPC algorithm is not using a modulator, one of these vectors will be applied to the converter output for the duration of the whole sampling period T_s.

A. Electrical model

The FCS-MPC algorithm will be evaluated on a 3L-NPC converter in standalone operation with an LC output filter and a resistive load as seen in Fig. 2. During the execution of FCS-MPC for all 27 possible inverter voltage vectors, future system voltages and currents are calculated using differential equations which describe the AC and DC side system dynamics.

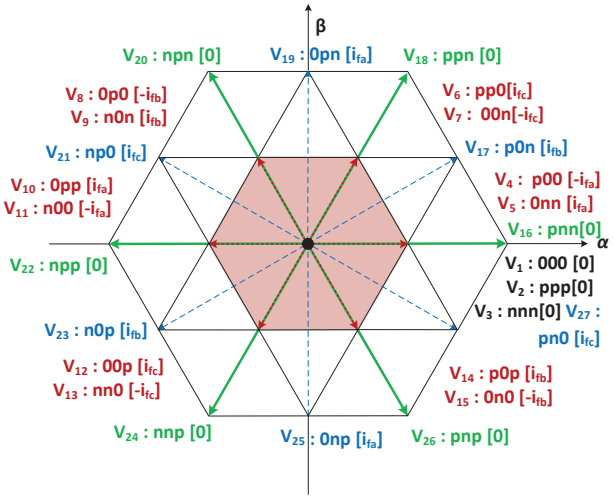


Fig. 1. Voltage vectors, switching states and neutral point current that can be generated by an 3L-NPC converter.

These system equations are discretized using the Euler forward method. On the AC side future values of the filter current and capacitor voltage are needed and on the DC side the future values of the DC-link capacitor voltages. The values of the filter current $i_{f\alpha\beta}$ and capacitor voltage $v_{c\alpha\beta}$ are calculated using the following differential equations in the stationary $\alpha\beta$ frame:

$$i_{f\alpha\beta}(t) = C_f \frac{dv_{c\alpha\beta}(t)}{dt} + i_{o\alpha\beta}(t) \quad (1)$$

$$v_{i\alpha\beta}(t) = L_f \frac{di_{f\alpha\beta}(t)}{dt} + v_{c\alpha\beta}(t) \quad (2)$$

where $i_{o\alpha\beta}$ and $v_{i\alpha\beta}$ are the load current and inverter output voltage, L_f and C_f are the filter inductance and capacitance. Future values of the DC-link capacitor voltages $v_{dc1,2}$ are obtained using the DC link capacitor charging equations:

$$v_{dc1,2}(t) = C_{dc1,2} \frac{di_{dc1,2}(t)}{dt} \quad (3)$$

$$i_{dc1}(t) = i_{dc}(t) - \sum_x (H_{1x} i_{fx}(t)) \quad (4)$$

$$i_{dc2}(t) = i_{dc}(t) + \sum_x (H_{2x} i_{fx}(t)) \quad (5)$$

where C_{dc1} and C_{dc2} are the capacitances of the DC-link capacitors and $i_{dc1,2}(t)$ are respective charging currents. $i_{dc}(t)$ is the DC source current, $i_{fabc}(t)$ the inverter phase current, H_{1x} and H_{2x} are indicator functions. H_{1x} will return 1 if the phase leg $x \in a, b, c$ is connected to $V_{dc}/2$ while H_{2x} returns 1 if the phase leg is connected to $-V_{dc}/2$ otherwise the function values are 0. The product of the indicator function and respective inverter phase current represents the neutral point current i_N. Depending on the applied redundant small inverter voltage vector the sign of this current can be positive meaning that the capacitor voltage will rise or if it is negative the voltage will drop. The key of the DC-link balancing is to properly use the small redundant vectors ($V_4 - V_{15}$) and

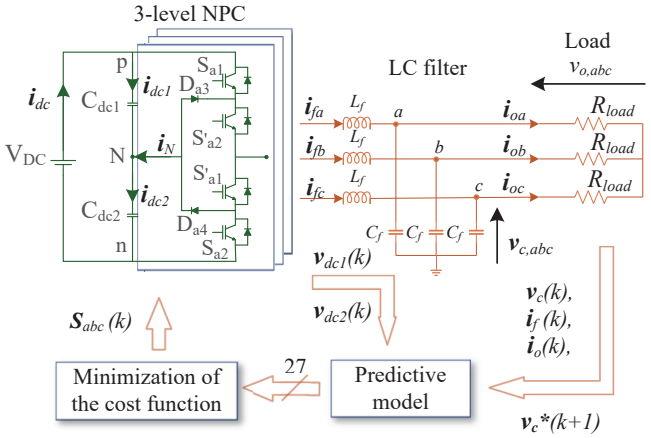


Fig. 2. Simplified system model scheme of stand-alone 3L-NPC converter using model predictive control.

keep the neutral point voltage balanced. Therefore, to ensure proper operation of the system, balancing of the DC-link voltage capacitors must be included in the cost function of the FCS-MPC algorithm. For each prediction the cost function is evaluated and the converter switching state that minimizes the cost function is selected and applied to the converter output. In the experimental application the execution of the algorithm will introduce a delay in the system. A compensation of this delay is needed to remove the negative effects on the algorithm performance as shown in [23]. Using the forward Euler method as presented in [15] the discrete-time model of the system was obtained.

B. Thermal model

To evaluate the thermal distributions of 3L-NPC converter using PLECS Blockset in Simulink, thermal models of IGBT switches and diodes are needed. Thermal impedance of the devices are modeled as a four layer Foster RC network, as shown in Fig. 3, the Foster RC model is based on measurements of the temperature dynamics and it depends on the material and structure of the device. The parameters of the model are obtained by fitting the mathematical curve to temperature measurements, and therefore they do not have any physical meaning [24]. In Fig. 3, T_j represents the junction temperature of the device and T_c the case temperature. To perform simulations the Foster network needs to be transfered to an equivalent Cauer network. All thermal parameters of the SKiiP 28MLI07E3V1 modules used in the experimental set-up can be found in the manufacturer datasheet [25]. The parameters were obtained by fitting the analytical function to the transient thermal impedance graph:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{4} R_{ith}(1 - e^{(-\frac{t}{\tau_i})}) \quad (6)$$

The obtained values are presented in Table I. The heatsink of the experimental set up provides an R_{th} = 0.06 K/W at a 5 m/s airflow of the fan [26].

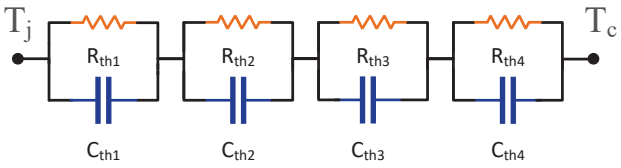


Fig. 3. Foster thermal network for transistor and diode $Z_{T/D(j-c)}$.

TABLE I
PARAMETERS OF THE THERMAL IMPEDANCE FOR $Z_{T/D(j-c)}$

Layer	1	2	3	4
$R_{iT}(K/W)$	0.31	0.18	0.057	0.0075
$\tau_{iT}(ms)$	230	80	1	0.6
$R_{iD}(K/W)$	0.4	0.27	0.066	0.023
$\tau_{iD}(ms)$	230	86	1	0.8

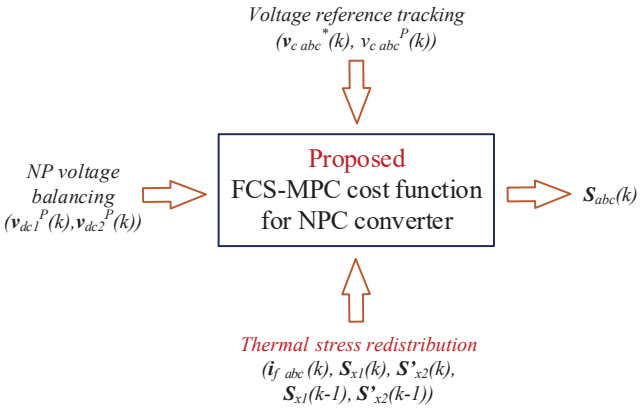


Fig. 4. Proposed cost function for the FS-MPC algorithm.

III. Proposed FS-MPC Algorithm

The conventional cost function of a FCS-MPC algorithm for a standalone 3L-NPC converter includes two objectives: minimization of the reference tracking error and neutral point voltage balancing. In the algorithm this is formulated as follows:

$$g = (v^*_{c\alpha} - v^P_{c\alpha})^2 + (v^*_{c\beta} - v^P_{c\beta})^2 + \lambda_{dc} \cdot g_{dc} \quad (7)$$

$$g_{dc} = (v^P_{dc1} - v^P_{dc2})^2 \quad (8)$$

where $v^*_{c\alpha}$ and $v^*_{c\beta}$ represent the real and imaginary parts of the reference voltage vector $v^*_c(k) = v^*_{c\alpha} + jv^*_{c\beta}$, $v^P_{c\alpha}$ and $v^P_{c\beta}$ the real and imaginary parts of the predicted voltage vector $v^P_c(k+1) = v^P_{c\alpha} + jv^P_{c\beta}$. Weighting factor λ_{dc} is used to tune the DC-link balancing part g_{dc}. The purpose of g_{dc} is to select the switching combination that will produce minimum difference between the predicted capacitor voltages $v^P_{dc1}(k+1)$ and $v^P_{dc2}(k+1)$.

In our algorithm in Fig. 4 we propose to include an additional term in the cost function with the aim to balance the

stress applied to the converter switches. It is quite straightforward that if the amplitude of the current flowing through the semiconductor device is high, if possible the control algorithm should avoid switching that device. In Fig. 1 we can see that the FCS-MPC algorithm has the possibility to select 27 switching states from which 8 are redundant. Therefore, it is possible to use these redundant switching states to avoid switching the device with high current. This can be very beneficial in cases when the amplitude modulation index is low and the current is high like the low voltage ride trough (LVRT) scenarios in renewable energy systems. In this case as the output voltage is low, small and zero vectors are utilized more often and as each vector has a redundant switching combination they can be used to avoid the switching when the amplitude of the current is high in that phase. There are of course unavoidable drawbacks of this objective, avoiding the switching will increase the THD of the output voltage. For this reason a proper balance of the objectives needs to be maintained i.e. the cost of a little higher THD may prolong the lifetime of the most stressed devices as the stress will be more equally redistributed among the devices.

To include the thermal redistribution objective in the cost function, two pieces of information are needed for all three phases of the converter: amplitude of the converter current i.e. filter current i_f and the switching state in the previous sampling period. The first one is already provided in the conventional algorithm and the second one can easily be accessed in the algorithm, thus no additional measurements or semiconductor parameters are needed to implement this objective. The objective is translated into a cost function in the following way:

$$g_t = |I_{fa}(k)| \cdot n_a + |I_{fb}(k)| \cdot n_b + |I_{fc}(k)| \cdot n_c \quad (9)$$

$$n_x = |S_{x1}(k-1) - S_{x1}(k)| + |S'_{x2}(k-1) - S'_{x2}(k)| \quad (10)$$

where $I_{fx}(k)$ is the measured filter current amplitude for phase $x \in a, b, c$, $S_{x1}(k)$ and $S'_{x2}(k)$ are the new potential switching states and $S'_{x1}(k-1)$ and $S'_{x1}(k-1)$ is the applied switching state from the previous sampling period. Thus, the proposed algorithm has the following cost function:

$$g = (v^*_{c\alpha} - v^P_{c\alpha})^2 + (v^*_{c\beta} - v^P_{c\beta})^2 + \lambda_{dc} g_{dc} + \lambda_t g_t \quad (11)$$

where λ_t is the weighting factor of the thermal redistribution objective. Three performance variables have to be defined to select the weighting factors: THD of the output voltage, voltage difference of the DC-link capacitors and the difference between the junction temperatures of the devices. For this reason multiple simulations were run to determine the optimum selection of the weighting factors.

IV. Analysis of semiconductor stress redistribution

A simulation model of the described three phase 3L-NPC converter with an output LC filter was created in Simulink with the parameters given in Table II. Using the PLECS Blockset, the thermal models of the semiconductor devices were designed based on the manufacturer datasheets [25], [26]. The simulations were performed using a conventional cost function (7) and a proposed cost function (11). Due to the normally large thermal capacitance, the initial heat sink temperature is set to 80°C for high current and to 50 °C for low current operation to shorten the simulation time needed to reach the steady state operation. Simulation results for two scenarios are provided: high amplitude modulation index and low amplitude modulation index. The weighting factors in the cost functions (λ_{dc} = 1, λ_t = 0.05) were determined by running multiple simulations. A concept for selecting weighting factors presented in [27] can be used to find the optimum solution. For this system the THD, DC-link balance and junction temperature difference can be defined as the performance metrics.

TABLE II
System parameters

Parameter	Value
DC link voltage	V_{dc} = 700 V
DC link capacitors	$C_{dc1,2}$ = 4 mF
Output filter parameters	L_f = 2.4 mH, C_f = 15 μF
Algorithm sampling time	T_s = 25 μs
Weighting factors	λ_{dc} = 1, λ_t = 0.05

A. High modulation index

The reference phase to phase voltage in the simulation is set to the 400 V and the value of the linear resistive load R_{load} in first simulation is set to 3.25 Ω and in the second 6.5 Ω, therefore the respective load current amplitudes are approximately 100 A and 50 A. The redistribution of the mean junction temperatures (T_j) is shown in Fig. 5 and Fig. 6. It can be observed that for the conventional cost function ($\lambda_t = 0$) there is a significant temperature difference between the outer (T_1, T_2) and inner (T'_1, T'_2) IGBTs, also the clamping diodes (D_3, D_4) are put under higher thermal stress than the free-wheeling diodes (D_1, D'_2, D'_1, D_2). When λ_t is set to 0.05 the redistribution of the thermal stress changes making the diffrence between the T_j of IGBT switches lower. Furthermore, the clamping diodes are also relived. The price for this temperature drop is seen in a slightly higher THD of the output voltage (+0.12%).

B. Low modulation index

In this case, the reference phase to phase voltage is decreased to 280 V and the value of the linear resistive load R_{load} in the first simulation is set to 4.6 Ω and in the second to 2.3 Ω to simulate the same current conditions like in Subsection IV-A. The positive effect of using the thermal redistribution algorithm is even more evident during the low voltage operation. For all semiconductor devices a significant T_j temperature drop can be noticed in Fig. 7 and Fig. 8. Under extreme conditions like shown in the Fig. 7, a perfect balance between T_j of the IGBTs can not be achieved, nevertheless

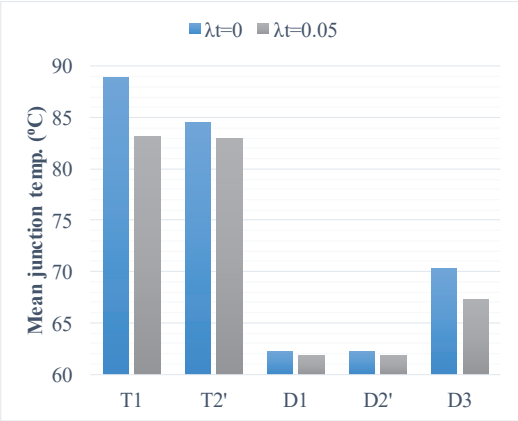


Fig. 5. Mean junction temperature comparison for different weighting factors λ_t; V_c = 400 V I_o = 100 A.

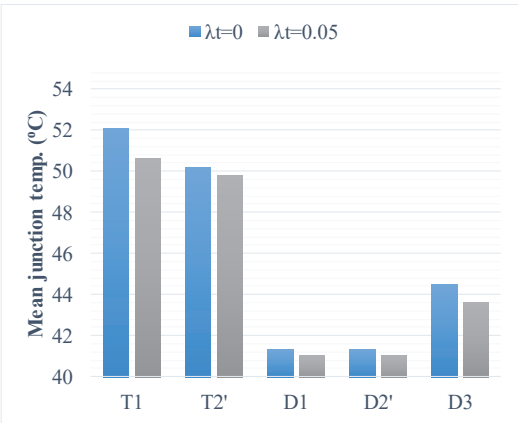


Fig. 6. Mean junction temperature comparison for different weighting factors λ_t; V_c = 400 V I_o = 50 A.

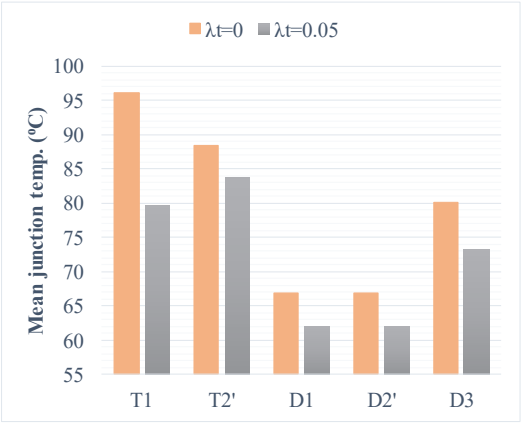


Fig. 7. Mean junction temperature comparison for different weighting factors λ_t; V_c = 280 V I_o = 100 A.

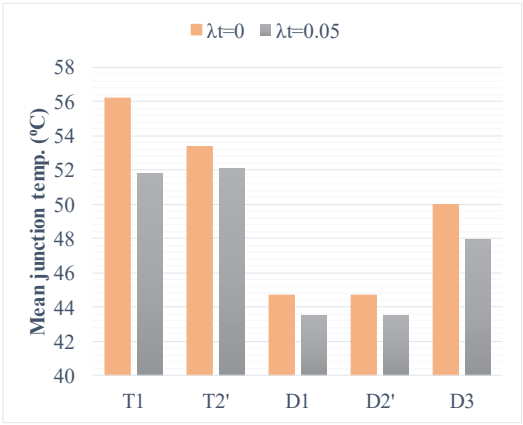


Fig. 8. Mean junction temperature comparison for different weighting factors λ_t; V_c = 280 V I_o = 50 A.

compared to the conventional solution the decrease of the T_j difference between the IGBTs is still noticeable. In Table III calculated THD of the output voltage for all simulated cases is presented. The increased THD is seen for the proposed cost function during the high current operation as this algorithm favors less switching state transitions when the converter current is high. For low current the impact on the voltage THD is minimum.

V. Experimental validation

Validation of the proposed cost function was performed on the experimental set-up shown in Fig. 9 which includes a Semikron 3L SKiiP28MLI07E3V1 Evaluation Inverter, Micro-LabBox DS1202 PowerPC DualCore 2 GHz processor board and DS1302 I/O board from dSpace. The total turn around time including the execution of the algorithm and the A/D conversion of the measurement channels is approximately 22 μs. As a result of offline converter model discretization i.e. the system matrixes of the discrete model are calculated prior to execution of the controller, the execution of the algorithm is very fast. To compensate this delay of approximately 22 μs the predicted values are calculated one step further ahead and applied at the beginning of the next time sampling interval as demonstrated in [23].

Due to the fact that junction temperatures are not provided for the available compact 3L-NPC converter [26] only effects

TABLE III
Evaluated operation conditions of a 3L-NPC converter with and without thermal redistribution

V_{ref} (V)	I_o (A)	λ_t	Voltage THD (%)	$\Delta T_{j1,2'}$ (°C)	T_{jD3} (°C)
400	50	0	0.5	2	44.5
400	50	0.05	0.53	0.8	43.6
400	100	0	0.35	4.5	70.3
400	100	0.05	0.47	0.2	67.3
280	50	0	0.51	3	50
280	50	0.05	0.52	0.3	48
280	100	0	0.35	7.7	80
280	100	0.05	0.53	4	73.3

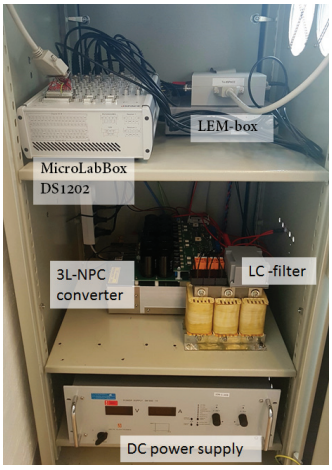
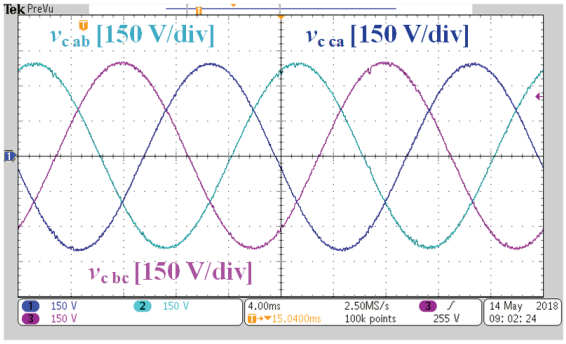
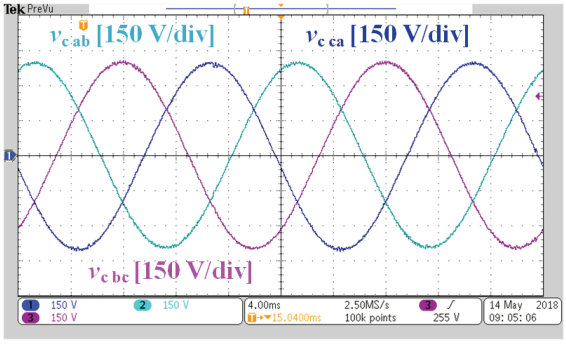


Fig. 9. 3L-NPC experimental set-up.



(a) Conventional cost function (λ_{dc}= 1, λ_t=0)



(b) Proposed cost function (λ_{dc}= 1, λ_t=0.9)

Fig. 10. Measured output voltage v_{cabc} from the 3L-NPC experimental set-up.

on the output voltage and DC-link capacitor voltages could be observed. The simulation results have shown that the effect on the output THD should be minor, therefore the inclusion of the thermal redistribution objective should not significantly increase the THD of the measured capacitor voltage. The reference voltage was set to 230 V and the DC-link voltage was set to 510 V. The filter parameters are equal to the values used in the simulation model (L_f = 2.4 mH and C_f = 15 μF) while the used load resistance R_{load} was 30 Ω. As it can

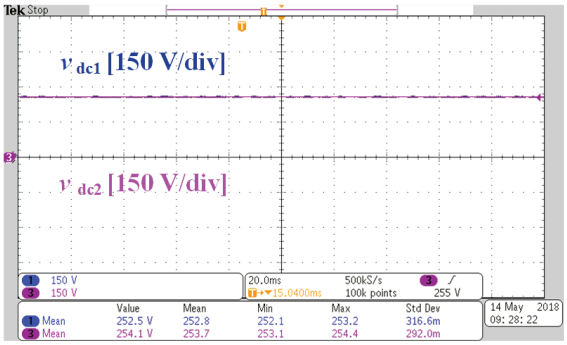


Fig. 11. Measured DC-link capacitor voltage $v_{dc1,2}$ 3L-NPC experimental set-up when λ_{dc}= 1, λ_t=0.9.

be noted from the measured capacitor voltage in Fig. 10, if the thermal redistribution objective was included in the cost function, the THD didn't significantly increase. The calculated THD for the conventional cost function was 1.29% while for the proposed cost function it was 1.35%. The effects of the proposed cost function are also exhibited in the switching frequency. As the objective of the proposed cost function is to avoid switching in periods of high current, the measured average switching frequency was around 5 kHz, while for the conventional cost function it was 7 kHz. In Fig. 11 it can be seen that the DC-link balance was also preserved during the operation with the proposed cost function.

VI. Conclusion

A finite set MPC based algorithm with balanced semiconductor thermal redistribution for 3L-NPC converter is proposed. The main objective of the algorithm is to prevent the switching events during high current intervals. The algorithm implementation is very simple as no additional information about the semiconductor devices nor additional measurements are needed. The computational effort of the algorithm is also not increased compared to the conventional cost function for 3L-NPC converters. Two operation modes of the converter were investigated. Under both high and low amplitude index the difference between the mean temperatures of the IGBT switches was lowered and the clamping diode was also relived. The THD of the controlled voltage was not significantly increased, which was also proved on an experimental set-up. The algorithm benefits are most noticeable during the LVRT scenarios when the modulation index is low and the current flowing through devices is high.

In the future work, experiments on the open module converter will be performed to confirm the temperature redistribution effects obtained in the simulations. The module lifetime estimation for the proposed algorithm will also be investigated as it is expected that the balanced redistribution of thermal stress will increase the lifetime of the converter modules.

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