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Low-Complexity Model Predictive Control of Single-Phase Three-Level Rectifiers with Unbalanced Load

Junpeng Ma, *Student Member*, *IEEE*, *Wensheng Song, Member*, *IEEE,* Xiongfei Wang, *Senior Member*, *IEEE*, Frede Blaabjerg, *Fellow*, *IEEE*, Xiaoyun Feng

***Abstract*—The neutral-point potential fluctuation in single-phase three-level rectifiers leads to coupling between the line current regulation and dc-link capacitor voltage balancing, deteriorating waveform quality of the line current. For addressing this issue, this paper proposes a low-complexity model predictive current control (MPCC) with constant switching frequency, which achieves a decoupling control of the line current and the neutral-point potential under the unbalanced load condition. The switching frequency is fixed by combining the MPCC scheme with predefined switching sequences. The boundary of the durations for voltage vectors in switching sequences is presented to balance the capacitor voltage without worsening the line current quality. The optimal switching sequence and the corresponding optimal durations of voltage vectors in the switching sequence are readily derived without the assessment of the cost function, which dramatically simplifies the complexity of the MPCC scheme. Finally, simulations and experimental results are conducted to verify the effectiveness of the proposed MPCC scheme.**

***Index Terms*—Model predictive current control (MPCC), neutral-point voltage balancing, single-phase three-level rectifiers, unbalanced load.**

I. INTRODUCTION

Single-phase three-level neutral-point-clamped (NPC) rectifiers are widely adopted as the grid-side converters of the traction-drive system in electric locomotive and high-speed trains, due to the salient advantages of the high power factor, the low harmonic current distortion, the constant dc-link voltage and the bidirectional power flow [1], [2]. Yet, the frequent change of the operating conditions of high-speed trains makes the dc-link voltage of the NPC rectifier fluctuate in a wide range, and equivalent loads connected to two dc-link capacitors will not be identical due to the different operating conditions of the connected traction inverter-drives. This unbalanced loading condition consequently challenges the neutral point balancing and the line current control [3]. The optimal control of the line current and the dc-link voltage balancing becomes of great importance.

Model predictive control (MPC) provides a promising multi-objective tracking approach to the line current control, the dc-link voltage control, and the capacitor voltage balancing [4]–[7]. Traditionally, the MPC needs a predefined cost function in respect to the desired controlled variables, such as the line current, dc-link voltage, active and reactive powers, switching frequency, power loss, etc. [7]. And then an optimal switching vector is selected for minimizing the cost function. This method is also known as the finite control set MPC (FCS-MPC). In [8], [9], the dc-link voltage Proportional-Integral (PI) controller is removed and the line current and dc-link voltage can be controlled by selecting the optimal switching vector. The dynamic response of this control method is dramatically improved, yet it requires the information of the dc-link current or the load power for predicting the capacitor voltage. The FCS-MPC-based capacitor voltage balancing approach for the three-level NPC converter has been reported in [10], [11], which improves the dynamic performance of the capacitor voltage balancing. Yet, these FSC-MPCs are applied in the shunt active power filter (SAF), where the dc-link capacitors are not loaded and the capacitor voltage can be easily predicted according to the switching states. If there are loads connected to the dc-link capacitors, the prediction of the capacitor voltages will depend on both switching states and the load current, which needs to be measured with the additional current sensor or estimated with the dc-link voltage and powers of the connected inverter. Those load power/current based control methods fail to balance the capacitor voltages with unknown and unbalanced loads. Moreover, the varying switching frequency of the FCS-MPC leads to a wide harmonic spectrum, which cannot be filtered easily.

In contrast, the continuous control set MPC (CCS-MPC) is an effective method to achieve the optimal control with constant switching frequency. In [14], a modulated MPC (M^2PC) with the sinusoidal PWM(SPWM) is reported and the durations of candidate vectors are calculated by evaluating the corresponding cost function. Compared to FCS-MPC, the cost function in this method is further reduced by the combination of vectors in one sampling interval. Being different from [14], in [15], the optimal switching sequences is proposed to achieve the constant switching frequency for single-phase NPC converters without using SPWM. Yet, the above two approaches cannot achieve the line current control and capacitor voltage balancing at the same time. In order to solve this problem, in [16] and [17], the term of capacitor voltage balancing is included in the cost function. The voltage error of

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J. Ma, W. Song, and X. Feng are with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 610031, China (e-mail: junpeng_ma@163.com; songwsh@swjtu.edu.cn; fengxy@swjtu.edu.cn).

X. Wang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: xwa@et.aau.dk; fbl@et.aau.dk)

dc-link capacitors can be effectively reduced by using these methods, which are, however, sensitive to the unbalanced load condition, when the load power/current is not fed back to the controller.

Typically, the capacitor voltage balancing can be achieved by two methods. The first solution is to select one of the redundant vectors according to the direction of the line current and the difference between two capacitor voltages [11], [16], [18], which is similar to the bang-bang control [3]. In [17], by introducing the term of the capacitor voltage difference into the cost function, the redundant vectors can be switched according to the cost function other than the direction of the line current and the voltage difference between the two capacitors. However, the use of the redundant vector results in non-negligible ripples in the voltage difference of two capacitors and, particularly in the unbalanced load condition [19]. The second approach to balance the capacitor voltage is to tune the duration of the redundant vectors instead of selecting one of the redundant vectors based on the state of the line current and the dc-link voltage within one sampling interval. This method can be achieved by injecting a dc component into modulated voltage [3]. The advantage of this scheme is that the voltage difference of two capacitors can reach zero with a negligible ripple even in the presence of the unbalanced load condition. Yet, MPC combining with this method to balance the capacitor voltage has not been analyzed in detail.

Moreover, both FCS-MPC and CCS-MPC need to assess the cost function for all vectors or switching sequences to reach an optimal solution [15], which increases the computational burden. For reducing the complexity of the traditional MPC, instead of evaluating the cost function of all vectors, a solution of selecting switching sector which is similar to the space vector pulse width modulation (SVPWM), is reported in [20], [21]. Yet, the cost function still needs to be calculated for the adjacent vectors of the chosen sector. In [8], [22], A reference vector is estimated and then a vector closest to this reference vector is selected. The selected vector satisfies the cost function minimization. Therefore, this method is not necessary to multiply evaluate the cost function. Yet, the distance between the reference vector and candidate vectors need to be computed for finding the optimal vector. [23] can directly calculate optimal duty cycle without the selection of the switching sequence, but it is not applied in NPC converters since this method cannot achieve the voltage balancing and the switching sequences for NPC converters are different from those in this method.

For eliminating the influence of the capacitor voltage balancing on the line current under the unbalanced load condition, this paper develops a model predictive current control (MPCC) of single-phase three-level NPC rectifiers with the constant switching frequency, which can achieve the decoupling between the line current regulation and the capacitor voltage balancing. The predefined switching sequences [15] is applied to achieve the constant switching frequency. The boundary of durations of voltage vectors in the switching sequences is analyzed in detail. By using the proposed boundary, the capacitor voltage balancing has no effect on the performance of the current control even if in a dynamic process. Furthermore, the optimal switching sequence and the corresponding optimal duration can be directly solved by using simple equations without the assessment of the cost function with the proposed method, which simplifies the complexity of the MPCC.

This paper is organized as follows. In Section II, the adopted circuit system is introduced in detail and the influence of the voltage balancing on the line current is discussed. In Section III, traditional predefined switching sequences and typical CCS-MPC methods are described. In Section IV, the developed MPCC is analyzed in detail. In Section V, the developed scheme is verified by the simulations and experimental tests, followed by a conclusion in Section VI.

II. System Description

A. System Model

Fig. 1 shows the simplified topology of a typical traction drive unit in high-speed railway trains, which consists of a single-phase three-level rectifier, the dc-link circuit, three-phase three-level inverter and four traction motors. The traction transformer connected to the traction grid is ignored for simplification. u_s and i_s represent the main voltage and the line current of the secondary side of traction transformer, respectively. L_n is the rated equivalent inductance of traction transformer; R represents the equivalent resistance of traction transformer; u_{ab} is the input voltage of the three-level H-bridge topology. C_1 and C_2 are symbols for the two capacitors in the dc-link. u_{dc1} and u_{dc2} are the voltage of capacitors C_1 and C_2. S_{a1}, S_{a2}, S_{a3} and S_{a4} represent IGBT modules with freewheeling diodes of **a** phase. S_{b1}, S_{b2}, S_{b3} and S_{b4} represent IGBT modules with freewheeling diodes of **b** phase. The varied operations of traction inverter-motor system will lead to the voltage fluctuation of dc-link capacitors. In order to simplify the analysis of the front-end rectifier, the resistors R_1 and R_2 connected to C_1 and C_2 are used to be equivalent to the inverter-motor system, respectively.

In general, the small internal resistor R on the second side of the traction transformer can be neglected, and the line current slope k_l can be expressed as

$$k_l = \frac{di_s}{dt} = \frac{u_s - u_{ab}}{L_n} \tag{1}$$

where u_{ab} in (1) are specified as the adopted switching states. The corresponding switching functions are defined as

$$G_i = \begin{cases} 1 & S_{i1} \text{ and } S_{i2} \text{ are } on; S_{i3} \text{ and } S_{i4} \text{ are } off \\ 0 & S_{i2} \text{ and } S_{i3} \text{ are } on; S_{i1} \text{ and } S_{i4} \text{ are } off \\ -1 & S_{i3} \text{ and } S_{i4} \text{ are } on; S_{i1} \text{ and } S_{i2} \text{ are } off \end{cases} (i = a, b). \tag{2}$$

There are 3^2=9 switching states in the adopted converter according to (2), the relation of the input voltage u_{ab} and the switching function G_i can be listed in Table I. $\boldsymbol{V}_j$ (j=1, 2,… 8) is the voltage vector, which is corresponding to the different switching state. Therefore, u_{ab} can be expressed as

$$u_{ab} = (G_{a1}u_{dc1} - G_{a4}u_{dc2}) - (G_{b1}u_{dc1} - G_{b4}u_{dc2}) \tag{3}$$

where G_{ij} = 1 and G_{ij} = 0 represent that the switching device S_{ij} (i=a, b; j=1, 2, 3, 4) in Fig. 1 is turned on and off, respectively.

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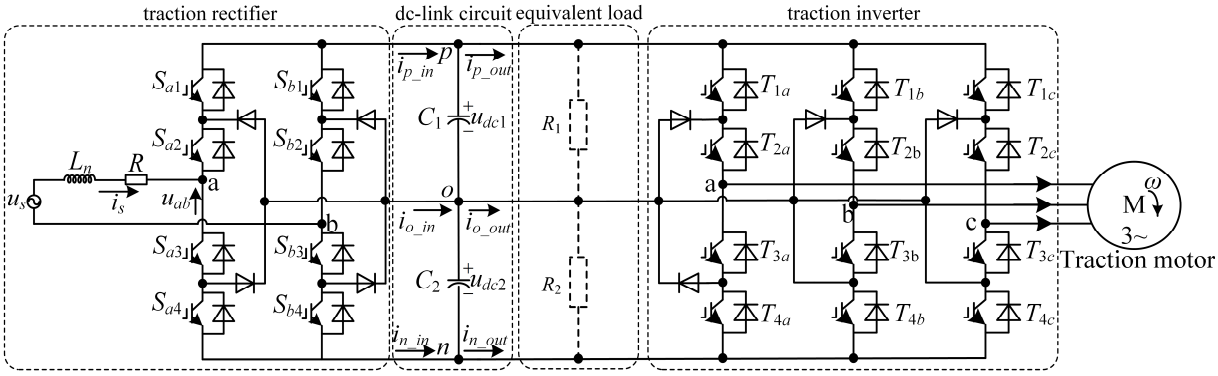

Fig. 1. The simplified topology of the typical ac-dc-ac traction drive unit in high-speed railway trains.

The voltage slopes k_{c1} and k_{c2} of two capacitors C_1 and C_2 can be expressed as

$$\begin{cases} k_{c1}=\dfrac{du_{dc1}}{dt}=\dfrac{1}{C_1}(i_{p\_in}-i_{p\_out})=\dfrac{1}{C_1}(i_{p\_in}-\dfrac{u_{dc1}}{R_1}) \\ k_{c2}=\dfrac{du_{dc2}}{dt}=\dfrac{1}{C_2}(-i_{n\_in}+i_{n\_out})=\dfrac{1}{C_2}(-i_{n\_in}-\dfrac{u_{dc2}}{R_2}) \end{cases} \tag{4}$$

where k_{c1} and k_{c2} are usually assumed as constant values within one sampling interval for predicting the capacitor voltage at the end of the next sampling interval. i_{p_out} and i_{n_out}, corresponding to the load currents of R_1 and R_2, cannot be directly obtained. Consequently, the load current or load power needs to be measured or estimated to predict the dc-link capacitor voltages [9]. i_{p_in} and i_{n_in} can be calculated according to the switching state, which is shown in Table I and can be deduced as

$$\begin{cases} i_{p\_in}=(G_{a1}-G_{b1})i_s \\ i_{n\_in}=(G_{a4}-G_{b4})i_s. \end{cases} \tag{5}$$

According to Kirchhoff's current law (KCL), the relation of i_{p_in}, i_{n_in}, and i_{o_in} can be expressed as

$$i_{p\_in}+i_{n\_in}+i_{o\_in}=0. \tag{6}$$

Therefore, the input current of the neutral point of dc-link i_{o_in} can be derived as

$$i_{o\_in}=-i_{p\_in}-i_{n\_in}=(|G_b|-|G_a|)i_s. \tag{7}$$

TABLE I
THE RELATION DEFINITION OF SWITCHING STATES AND INPUT CURRENT OF THE DC-LINK

Model	1	2	3	4	5	6	7	8	9
(G_a, G_b)	(1, 1)	(1, 0)	(1, −1)	(0, 1)	(0, 0)	(0, −1)	(−1,1)	(−1,0)	(−1, −1)
Vector	V_8	V_2	V_1	V_6	V_4	V_3	V_7	V_5	V_9
u_{ab}	0	u_{dc1}	$u_{dc1}+u_{dc2}$	$-u_{dc1}$	0	u_{dc2}	$-u_{dc1}-u_{dc2}$	$-u_{dc2}$	0
i_{p_in}	0	i_s	i_s	$-i_s$	0	0	$-i_s$	0	0
i_{n_in}	0	0	$-i_s$	0	0	$-i_s$	i_s	i_s	0
i_{o_in}	0	$-i_s$	0	i_s	0	i_s	0	$-i_s$	0

Due to the computational delay, the controlling variables calculated at the nth instant will delay to be applied at the n+1th instant, therefore, two-step prediction of voltages and currents need to be executed for achieving the deadbeat control [7]. Current and voltages at n+1th instant can be predicted by the switching state estimated in the previous sampling instant, which can be expressed as

$$\begin{cases} i_s(n+1)=i(n)+k_l(n)T_{sa} \\ u_{dc1}(n+1)=u_{dc1}(n)+k_{c1}(n)T_{sa} \\ u_{dc2}(n+1)=u_{dc2}(n)+k_{c2}(n)T_{sa} \end{cases} \tag{8}$$

where $k_l(n)$, $k_{c1}(n)$ and $k_{c2}(n)$ has been estimated in the previous sampling interval. T_{sa} represents the sampling period. The predicted current and voltages at n+2th sampling instant by adopting $\boldsymbol{V}_j$ can be expressed as

$$\begin{cases} i_s^j(n+2)=i(n+1)+k_l^j(n+1)T_{sa} \\ u_{dc1}^j(n+2)=u_{dc1}(n+1)+k_{c1}^j(n+1)T_{sa} \\ u_{dc2}^j(n+2)=u_{dc2}(n+1)+k_{c2}^j(n+1)T_{sa} \end{cases} \tag{9}$$

where k_{c1}^j to k_{c2}^j represent the voltage slopes of dc-link capacitors by adopting the vector $\boldsymbol{V}_j$(j=1, 2…, 9). As shown in Table I, there are 7 voltage levels (5 levels when u_{dc1}=u_{dc2}) in the adopted converter, corresponding to seven kinds of the line current slopes. Therefore, the cost function for the line current error and capacitor voltage error at n+2th sampling instant can be expressed as

$$E^j=[i_{ref}(n+2)-i_s^j(n+2)]^2+\lambda_u[u_{dc1}^j(n+2)-u_{dc2}^j(n+2)]^2 \tag{10}$$

where E^j is the cost function by applying the voltage vector $\boldsymbol{V}_j$. The line current reference i_{ref} can be obtained from a dc-link voltage PI controller, as shown in Fig. 2 [24]. PLL represents the phase locking loop to obtain the phase angle and frequency of the main voltage.

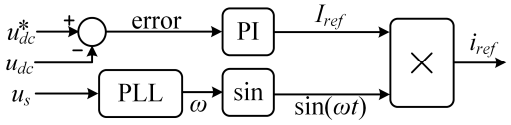

Fig. 2. The calculation of the line reference current.

In order to minimize the cost function, in traditional FSC-MPC [9], an optimal voltage vector is usually selected by enumerating from the all possible switching vectors to be applied in the n+1th sampling interval.

B. Voltage balancing

Traditionally, the tradeoff between the current control and the voltage balancing can be realized by adjusting λ_u in (10) [9], it can be seen that a large λ_u will take sides in the voltage balancing, i.e., by using the cost function shown in (10), the current control will be affected by the voltage balancing. The unbalanced load will cause a voltage error between two capacitors. Therefore, the current control will be deteriorated by using (10) under the unbalanced load condition. The detailed analysis is shown as follows.

According to the second and third equations in (9), the predicted value of the capacitor voltage error by applying $\boldsymbol{V}_j$ can be deduced as

$$e_c^j(n+2) = e_c(n+1) + T_{sa}[k_{c1}^j(n+1) - k_{c2}^j(n+1)] \quad (11)$$

where the capacitor voltage error $e_c(n+1)$ at the n+1th instant can be expressed as

$$e_c(n+1) = u_{dc1}(n+1) - u_{dc2}(n+1) = e_c(n) + [k_{c1}(n) - k_{c2}(n)]T_{sa} \quad (12)$$

which has been determined by the capacitor voltage error and the selected voltage vector in the nth sampling interval. Therefore, the capacitor voltage error in the n+2th interval is determined by the second term in (11). It can be derived in terms of (4) as

$$\Delta e_c^j = T_{sa}(k_{c1}^j - k_{c2}^j) = T_{sa}[(\frac{i_{p\_in}^j}{C_1} + \frac{i_{n\_in}^j}{C_2}) + (\frac{u_{dc2}}{C_2R_2} - \frac{u_{dc1}}{C_1R_1})]. \quad (13)$$

It is assumed that C_1=C_2=C_{dc}, (13) can be rewritten as

$$\Delta e_c^j = \frac{T_{sa}}{C_{dc}}(i_{p\_in}^j + i_{n\_in}^j + \frac{u_{dc2}}{R_2} - \frac{u_{dc1}}{R_1}). \quad (14)$$

where the $i_{p\_in}^j$ and $i_{n\_in}^j$ are currents injected into p-point and n-point in dc-link by applying the vector $\boldsymbol{V}_j$. Substituting (6) into (14), which can be simplified as

$$\Delta e_c^j = -\frac{T_{sa}}{C_{dc}} i_{o\_in}^j + \frac{T_{sa}}{C_{dc}}(\frac{u_{dc2}}{R_2} - \frac{u_{dc1}}{R_1}). \quad (15)$$

According to the third line and the last line of Table I, the direction of i_{o_in} caused by $\boldsymbol{V}_2$ is opposite to that caused by $\boldsymbol{V}_3$, but these two vectors have the same direction of the output voltage, which means that the line current can track the line current with the same trend, but the movement of the capacitor voltage error is opposite by using $\boldsymbol{V}_2$ and $\boldsymbol{V}_3$, Therefore, $\boldsymbol{V}_2$ and $\boldsymbol{V}_3$ are a pair of redundant vectors for neutral-point voltage balancing. The same conclusion can be gotten for $\boldsymbol{V}_5$ and $\boldsymbol{V}_6$.

It is assumed that $u_{dc1}(n+1) = u_{dc2}(n+1)$ at the n+1th instant, the slope of the line current is the same by applying redundant vectors $\boldsymbol{V}_2$, $\boldsymbol{V}_3$ or $\boldsymbol{V}_5$, $\boldsymbol{V}_6$. Therefore, the predicted current at the n+2th instant is the same by using redundant vectors, and the first term of the cost function in (10) hereby is the same. The only difference is the second term in (10), which is determined by (15), it can be seen from (15) that due to the opposite or negative current injected into o-point of the dc-link by using redundant vectors, the capacitor voltage error will be increased oppositely or negatively, and the balanced state of $u_{dc1}(n+1) = u_{dc2}(n+1)$ is broken during n+2th interval, which means that there exists an inherent fluctuation in the capacitor voltage error. But even worse, in unbalanced and unknown load condition, taking R_1>R_2 and i_s<0 as an example, if $\boldsymbol{V}_2$ and $\boldsymbol{V}_3$ are the candidate vectors, the following equations can be derived as

$$\begin{cases} \Delta e_c^2 = \dfrac{T_{sa}}{C_{dc}}(i_s + \dfrac{u_{dc2}}{R_2} - \dfrac{u_{dc1}}{R_1}) \\ \Delta e_c^3 = \dfrac{T_{sa}}{C_{dc}}(-i_s + \dfrac{u_{dc2}}{R_2} - \dfrac{u_{dc1}}{R_1}). \end{cases} \quad (16)$$

Therefore, $\Delta e_c^2 < \Delta e_c^3$ but due to an unbalanced and unknown load connected to the converter, the optimal redundant vector cannot be selected reasonably, and the voltage error will be further enlarged by mistakenly applying $\boldsymbol{V}_3$. This unbalanced neutral-point voltage also deteriorates the line current quality. Therefore, the voltage balancing control based on (10) is not suitable for the condition of the unbalanced and unknown load connected to the front-end converter.

III. Traditional CCS-MPC

A. Switching Sequence

CCS-MPC selects a switching sequence with the optimal duty cycle from all possible switching sequences to be applied in the next sampling interval and the switching frequency is fixed by this way [15]. For the aim of balancing the capacitor voltage during each sampling interval, the redundant vectors $\boldsymbol{V}_2$, $\boldsymbol{V}_3$ and $\boldsymbol{V}_5$, $\boldsymbol{V}_6$ should be selected as candidate switching states. Meanwhile, the predominant vector, $\boldsymbol{V}_1$, $\boldsymbol{V}_4$, $\boldsymbol{V}_7$, whose corresponding output voltage are $u_{dc1}+u_{dc2}$, 0, and -u_{dc1}-u_{dc2}, which have no effect on the voltage error of two capacitors, should be selected to minimize the cost function of the line current error. According to the above-mentioned criterions, the switching sequence is designed as Fig. 3 which is similar to the definition reported in [15]. And it also is described in Table II, where $\boldsymbol{V}_a$ and $\boldsymbol{V}_c$ represent redundant vectors and $\boldsymbol{V}_b$ represents the predominant vector. Seq_m represents the switching sequence m.

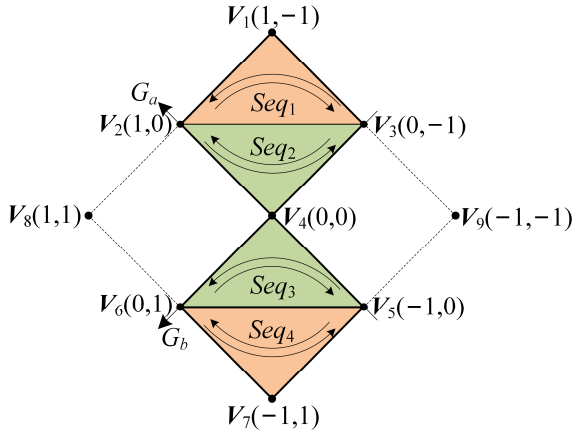

Fig. 3. The switching sequences.

TABLE II
Traditional Switching Sequences

m	$\boldsymbol{V}_a$, $\boldsymbol{V}_b$, $\boldsymbol{V}_c$	Switching sequence (Seq_m)
1	$\boldsymbol{V}_2$, $\boldsymbol{V}_1$, $\boldsymbol{V}_3$	$\boldsymbol{V}_2 \rightarrow \boldsymbol{V}_1 \rightarrow \boldsymbol{V}_3$
2	$\boldsymbol{V}_2$, $\boldsymbol{V}_4$, $\boldsymbol{V}_3$	$\boldsymbol{V}_3 \rightarrow \boldsymbol{V}_4 \rightarrow \boldsymbol{V}_2$
3	$\boldsymbol{V}_5$, $\boldsymbol{V}_4$, $\boldsymbol{V}_6$	$\boldsymbol{V}_5 \rightarrow \boldsymbol{V}_4 \rightarrow \boldsymbol{V}_6$
4	$\boldsymbol{V}_5$, $\boldsymbol{V}_7$, $\boldsymbol{V}_6$	$\boldsymbol{V}_6 \rightarrow \boldsymbol{V}_7 \rightarrow \boldsymbol{V}_5$

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B. CCS-MPC [15]

In [15], the voltage balancing is ignored, and the λ_u in (10) is set to zero, and a quadratic cost function for the switching sequence m shown in Table II can be rewritten as

$$E^{Seq_m} = [i_{ref}(n+2) - i_s^{Seq_m}(n+2)]^2. \quad (17)$$

For a given switching sequence, the predictive current $i_s^{Seq_m}$ at the n+2th interval can be expressed as

$$\begin{aligned} i_s^{Seq_m}(n+2) = & i_s(n+1) + k_l^a(n+1)t_a(n+1) + \\ & k_l^b(n+1)t_b(n+1) + k_l^c(n+1)t_c(n+1) \end{aligned} \quad (18)$$

where $i_s(n+1)$ can be predicted according to the switching sequence and corresponding durations estimated in the nth sampling interval, which can be expressed as

$$i_s(n+1) = i_s(n) + k_l^a(n)t_a(n) + k_l^b(n)t_b(n) + k_l^c(n)t_c(n). \quad (19)$$

Due to ignoring the voltage balancing, then t_a=t_c, and the time set T_{seq_m}= {t_a, t_b, t_c} that minimizes the cost function E using the voltage sequence Seq_m = {$\boldsymbol{V}_a$, $\boldsymbol{V}_b$, $\boldsymbol{V}_c$} can be expressed by solving the system

$$\begin{cases} \dfrac{\partial E^{Seq_m}}{\partial t_a} = 0 \\ \dfrac{\partial E^{Seq_m}}{\partial t_b} = 0. \end{cases} \quad (20)$$

An optimal switching sequence Seq_m that minimizes the cost function is defined as

$$Seq_{opt} = \arg\min_{Seq_m} E^{Seq_m} \quad (21)$$

with the associated optimal T_{seq_m}, which is equal to T_{opt}.

According to [15], for a given sequence Seq_m, (20) is simplified as

$$\begin{cases} i_{ref}(n+2) - i_s(n+1) - k_l^a t_a - k_l^b t_b - k_l^c t_c = 0 \\ t_a + t_b + t_c = T_{sa} \\ t_a - t_c = 0. \end{cases} \quad (22)$$

Therefore, the optimal duration T_{seq_m} for each vector of Seq_m can be solved as

$$\begin{cases} t_a\big|_{Seq_m} = t_c\big|_{Seq_m} = \dfrac{i_{ref}(n+2) - i_s(n+1) - k_l^b T_{sa}}{k_l^a - 2k_l^b + k_l^c} \\ t_b\big|_{Seq_m} = T_{sa} - \dfrac{i_{ref}(n+2) - i_s(n+1) - k_l^b T_{sa}}{0.5(k_l^a - 2k_l^b + k_l^c)}. \end{cases} \quad (23)$$

It is quite clear that this method cannot handle the issue of the voltage balancing, if the unbalanced load is connected to the dc-link of the converter, the voltage difference of two capacitors will be increased by using this method. Fig. 4 shows the flow chart of the traditional CCS-MPC. In order to predict the line current at the n+1th instant, the slopes of the line current for all voltage vectors need to be calculated before first three steps in Fig. 4. The optimal time set T_{opt} for different switching sequences is solved and then to calculate the cost function for four predefined switching sequences. In this process, (17), (18), (23) have been computed four times, which increases the computational burden of digital controllers.

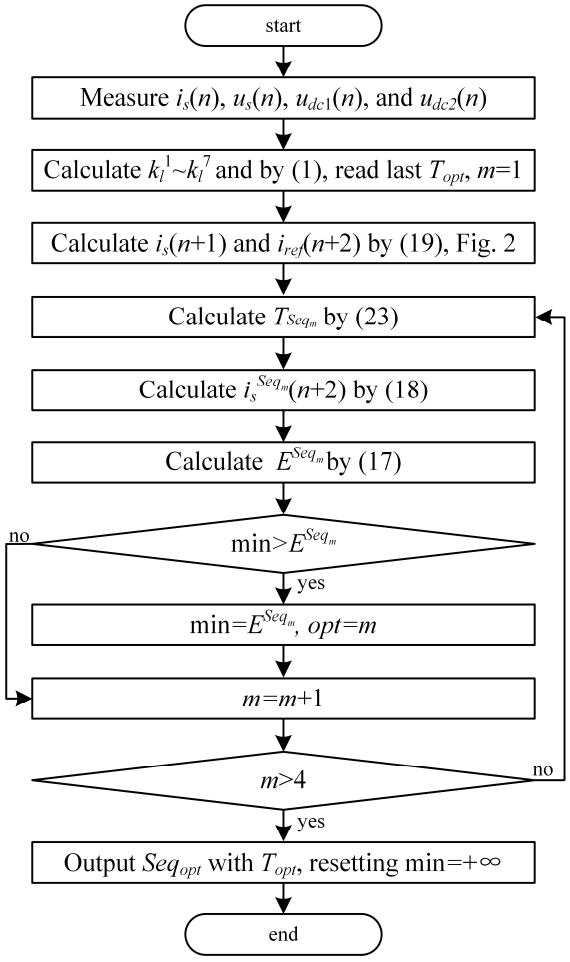

Fig. 4. The flow chart of the traditional CCS-MPC.

IV. PROPOSED CCS-MPC

A. The Developed Switching Sequence

As shown in Fig. 3, there are four different switching sequences as the candidate switching sequences. In every switching sequence, the candidate switching vectors $\boldsymbol{V}_a$, $\boldsymbol{V}_b$ and $\boldsymbol{V}_c$ should be distributed symmetrically for reducing current ripple. Consequently, the switching sequence is redesigned as Table III, which is similar to the switching sequence generated by carrier-based PWM [3]. The optimal duration for each vector can also be solved by (23).

TABLE III
DEVELOPED SWITCHING SEQUENCE

Sequence (m)	$\boldsymbol{V}_a$, $\boldsymbol{V}_b$, $\boldsymbol{V}_c$	Switching sequence (Seq_m)
1	$\boldsymbol{V}_2$, $\boldsymbol{V}_1$, $\boldsymbol{V}_3$	$\boldsymbol{V}_3$→$\boldsymbol{V}_1$→$\boldsymbol{V}_2$→$\boldsymbol{V}_1$→$\boldsymbol{V}_3$
2	$\boldsymbol{V}_2$, $\boldsymbol{V}_4$, $\boldsymbol{V}_3$	$\boldsymbol{V}_3$→$\boldsymbol{V}_4$→$\boldsymbol{V}_2$→$\boldsymbol{V}_4$→$\boldsymbol{V}_3$
3	$\boldsymbol{V}_5$, $\boldsymbol{V}_4$, $\boldsymbol{V}_6$	$\boldsymbol{V}_5$→$\boldsymbol{V}_4$→$\boldsymbol{V}_6$→$\boldsymbol{V}_4$→$\boldsymbol{V}_5$
4	$\boldsymbol{V}_5$, $\boldsymbol{V}_7$, $\boldsymbol{V}_6$	$\boldsymbol{V}_5$→$\boldsymbol{V}_7$→$\boldsymbol{V}_6$→$\boldsymbol{V}_7$→$\boldsymbol{V}_5$

B. The Developed Voltage Balancing Scheme

According to (12) and (15), if the redundant vectors $\boldsymbol{V}_a$ and $\boldsymbol{V}_c$ both are applied during one sampling interval, the voltage error of two capacitors at n+1*th* instant can be deduced as

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$$\begin{aligned} e_c(n+1) &= e_c(n) - \frac{t_a(n) i_{o\_in}^a(n)}{C_{dc}} - \frac{t_c(n) i_{o\_in}^c(n)}{C_{dc}} \\ &\quad + \frac{T_{sa}}{C_{dc}}\left[\frac{u_{dc2}(n)}{R_2} - \frac{u_{dc1}(n)}{R_1}\right] \\ &= e_c(n) + \frac{i_s(n)}{C_{dc}}[t_a(n) - t_c(n)] + \frac{T_{sa}}{C_{dc}}\left[\frac{u_{dc2}(n)}{R_2} - \frac{u_{dc1}(n)}{R_1}\right] \\ &= e_c(n) + \frac{i_s(n)}{C_{dc}}\Delta t_{dc}(n) + \frac{T_{sa}}{C_{dc}}\left[\frac{u_{dc2}(n)}{R_2} - \frac{u_{dc1}(n)}{R_1}\right]. \end{aligned} \tag{24}$$

Therefore, the voltage error can be regulated by the duration difference Δt_{dc} between of $\boldsymbol{V}_a$ and $\boldsymbol{V}_c$. Due to t_a=t_c in the traditional method solved by (22), the voltage error cannot be controlled by the traditional method. In order to narrow the voltage error of two capacitors, the variation of the voltage error needs to satisfy

$$\begin{cases} e_c(n+1) - e_c(n) < 0 \text{ if } e_c(n) > 0 \\ e_c(n+1) - e_c(n) > 0 \text{ if } e_c(n) < 0. \end{cases} \tag{25}$$

According to (24) and (25), it can be deduced as

$$\begin{cases} e_c(n+1) - e_c(n) \\ = \dfrac{i_s(n)}{C_{dc}}\Delta t_{dc}(n) + \dfrac{T_{sa}}{C_{dc}}\left[\dfrac{u_{dc2}(n)}{R_2} - \dfrac{u_{dc1}(n)}{R_1}\right] < 0, \text{ if } e_c(n) > 0 \\ e_c(n+1) - e_c(n) \\ = \dfrac{i_s(n)}{C_{dc}}\Delta t_{dc}(n) + \dfrac{T_{sa}}{C_{dc}}\left[\dfrac{u_{dc2}(n)}{R_2} - \dfrac{u_{dc1}(n)}{R_1}\right] > 0, \text{ if } e_c(n) < 0. \end{cases} \tag{26}$$

The first term on the right side of (26) can be controlled by $\Delta t_{dc}(n)$, but the second term on the right side of (26) depends on load R_1 and R_2, which are unknown values. Taking the first equation in (26) as an example, in order to satisfy that $e_c(n+1)$-$e_c(n)$<0 for any load of the second term on the right side of the first equation, the first term on the right side of the first equation must be the negative value. For second equation in (26), the first term on the right side must be the positive value. Therefore, in order to balance dc-link voltage, Δt_{dc} must satisfy

$$\begin{cases} i_s(n)\Delta t_{dc}(n) < 0 \text{ if } e_c(n) > 0 \\ i_s(n)\Delta t_{dc}(n) > 0 \text{ if } e_c(n) < 0. \end{cases} \tag{27}$$

Therefore, the sign function for Δt_{dc} can be deduced as

$$S = \begin{cases} 1 \text{ if } i_s(n)e_c(n) < 0 \\ -1 \text{ if } i_s(n)e_c(n) > 0 \end{cases} \tag{28}$$

and the absolute value of Δt_{dc} can be estimated by using a PI controller [3], [25], and this voltage balancing method can be drawn as Fig. 5.

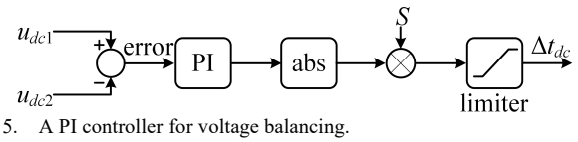

Fig. 5. A PI controller for voltage balancing.

where abs is absolute value function.

In order to balance the capacitor voltage, being different from (22), the optimal time set T_{seq_m} should be modified as

$$\begin{cases} i_{ref}(n+2) - i_s(n+1) - k_l^a t_a - k_l^b t_b - k_l^c t_c = 0 \\ t_a + t_b + t_c = T_{sa} \\ t_a - t_c = \Delta t_{dc}. \end{cases} \tag{29}$$

The optimal duration for each vector of Seq_m can be solved as

$$\begin{cases} t_a|_{Seq_m} = \dfrac{i_{ref}(n+2) - i_s(n+1) - k_l^b T_{sa} - (k_l^b - k_l^c)\Delta t_{dc}}{k_l^a - 2k_l^b + k_l^c} \\ t_c|_{Seq_m} = \dfrac{i_{ref}(n+2) - i_s(n+1) - k_l^b T_{sa} + (k_l^b - k_l^a)\Delta t_{dc}}{k_l^a - 2k_l^b + k_l^c} \\ t_b|_{Seq_m} = -\dfrac{i_{ref}(n+2) - i_s(n+1) - (k_l^a + k_l^c)T_{sa} + (k_l^c - k_l^a)\Delta t_{dc}}{k_l^a - 2k_l^b + k_l^c}. \end{cases} \tag{30}$$

Being different from the optimal duration of the traditional method calculated by (23), the term of the voltage balancing is added into (30) to compute the optimal duration. The capacitor voltage can be balanced by adjusting the duration of the redundant vector other than switching the redundant vector within one sampling interval. Therefore, the proposed method can control the voltage error of two capacitors to zero with a small ripple. However, a large Δt_{dc} without the limitation will cause that the durations solved by (30) exceeds the normal range, which can be expressed as

$$\begin{cases} 0 < t_a < T_{sa} \\ 0 < t_b < T_{sa} \\ 0 < t_c < T_{sa}. \end{cases} \tag{31}$$

Therefore, the range of Δt_{dc} needs to be further analyzed for achieving the optimal control of both the line current and capacitor voltage balancing.

C. The boundary of Time Set and Computation Simplification

Substituting the current slope calculated by (1) into (30) for each vector, the optimal duty cycle for vectors in each sequence can be simplified as Table IV.

TABLE IV

DUTY CYCLE FOR VECTORS IN DIFFERENT SWITCHING SEQUENCES

	Seq_1	Seq_2	Seq_3	Seq_4
Duty cycle of $\boldsymbol{V}_a$ (D_a)	$1+0.5D+D_{dc1}$	$-0.5D+D_{dc2}$	$0.5D+D_{dc1}$	$1-0.5D+D_{dc2}$
Duty cycle of $\boldsymbol{V}_c$ (D_c)	$1+0.5D-D_{dc2}$	$-0.5D-D_{dc1}$	$0.5D-D_{dc2}$	$1-0.5D-D_{dc1}$
Duty cycle of $\boldsymbol{V}_b$ (D_b)	$-1-D-D_\Delta$	$1+D+D_\Delta$	$1-D-D_\Delta$	$-1+D+D_\Delta$

In Table IV, the intermediate variables are deduced as

$$\begin{cases} D = \dfrac{[i_{ref}(n+2) - i_s(n+1)]L_n / T_{sa} - u_s(n)}{0.5[u_{dc1}(n) + u_{dc2}(n)]} \\ D_{dc1} = \dfrac{\Delta t_{dc}}{T_{sa}} \dfrac{u_{dc1}(n)}{u_{dc1}(n) + u_{dc2}(n)} \\ D_{dc2} = \dfrac{\Delta t_{dc}}{T_{sa}} \dfrac{u_{dc2}(n)}{u_{dc1}(n) + u_{dc2}(n)} \\ D_\Delta = D_{dc1} - D_{dc2}. \end{cases} \tag{32}$$

It can be seen from (32) that the intermediate variable D includes the term of the current error but no the term of Δt_{dc}, which means that D is determined by the current error, but is

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independent on the voltage balancing. The intermediate variables D_{dc1} and D_{dc2} are just the opposite. In other words, the line current is controlled by D and the voltage error of two capacitors are adjusted by D_{dc1} and D_{dc2}. It realizes the effective decoupling of the line current control and dc-link capacitor voltage balancing.

In order to optimally track the line current, D is directly estimated from the first equation of (32), but D_{dc1} and D_{dc2} need to be limited for different switching sequences. According to the fact

$$D_a \geq 0, D_b \geq 0, D_c \geq 0 \tag{33}$$

and Table IV, taking the Seq_1 as an example, the following inequalities can be deduced as

$$\begin{cases} D_{dc1} > -1 - 0.5D \\ D_{dc2} < 1 + 0.5D \\ D_{dc1} - D_{dc2} < -1 - D. \end{cases} \tag{34}$$

Meanwhile, the relation between D_{dc1} and D_{dc2} according to (32) can be deduced as

$$D_{dc1} + D_{dc2} = \frac{\Delta t_{dc}}{T_{sa}}. \tag{35}$$

For other switching sequences, the similar form of (34) and (35) can be deduced and the range of D_{dc1} and D_{dc2} of different switching sequences can be drawn as Fig. 6. The calculated operating point (D_{dc1}, D_{dc2}) must be limited to these regions for obtaining an optimal solution. If the operating point is located in a specific region, the corresponding switching sequence is selected as the optimal solution.

As shown in Fig. 6, the original point o (0, 0) satisfies that D_{dc1}=0 and D_{dc2}=0, which means that Δt_{dc}=0 and the voltage balancing is not valid. Meanwhile, the original point o is located in the range of Seq_2, indicating that the optimal switching sequence is Seq_2 in the case of ignoring the voltage balancing control. In order to achieve voltage balancing control, the operating point needs to be shifted from (0, 0) to (D_{dc1}, D_{dc2}). According to the second and third equations of (32), D_{dc1} and D_{dc2} satisfy

$$\begin{cases} \dfrac{D_{dc2}}{D_{dc1}} = \dfrac{u_{dc2}}{u_{dc1}} = k_{dc} \\ D_{dc1} + D_{dc2} = \dfrac{\Delta t_{dc}}{T_{sa}}. \end{cases} \tag{36}$$

The first and second equations in (36) can be drawn as the curve 1 and curve 2 in Fig. 6, respectively. The slope of curve 1 is larger than zero. The intersection point c of curve 1 and curve 2 simultaneously satisfies the first and second equations of (36) which means intersection point c is the operating point calculated by using the second and third equations of (32). Especially, the slope of curve 1 k_{dc} = 0 and k_{dc} =∞ indicate u_{dc2}=0 and u_{dc1}= 0, respectively. Therefore, the intersection points a and b in the D_{dc2}-axis and D_{dc1}-axis correspond to the extreme cases of u_{dc1}=0 and u_{dc2}=0, respectively. Both these two extreme cases need to be limited to operation regions. In the case shown in Fig. 6, the intersection a needs to be limited to the region of Seq_2. The curve 2 hereby moves to curve 2′. The line segment ab will move to the line segment $a'b'$, which is limited to the region of Seq_2. Meanwhile, in this case, the intersection c will be shifted to the intersection c', which is located in the line segment $a'b'$. The calculated operating point c' thereby always is located in the range of Seq_2 when the intersection a is limited to the operating range. The other cases are the same with Seq_2. According to the location of the intersection point a in Fig. 6, the range of the duration Δt_{dc} satisfies

$$\left| \frac{\Delta t_{dc}}{T_{sa}} \right| < 0.5D. \tag{37}$$

For other switching sequences, the same method can be used to analyze the range of Δt_{dc}, and the range of Δt_{dc} for each switching sequence can be deduced as

$$\begin{cases} seq_1 : -1 - D/2 < \Delta t_{dc}/T_{sa} < 1 + D/2 \\ seq_2 : D/2 < \Delta t_{dc}/T_{sa} < -D/2 \\ seq_3 : -D/2 < \Delta t_{dc}/T_{sa} < D/2 \\ seq_4 : -1 + D/2 < \Delta t_{dc}/T_{sa} < 1 - D/2. \end{cases} \tag{38}$$

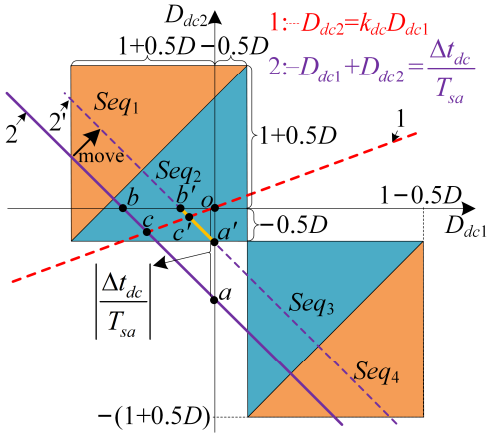

Fig. 6. The range of D_{dc1} and D_{dc2}.

According to (38), the range of $\Delta t_{dc}/T_{sa}$ can be drawn as Fig. 7. The value of $\Delta t_{dc}/T_{sa}$ located in the dashed region satisfies (38), which can ensure that the T_{seq_m} solved by (30) is the optimal time set within the range expressed in (31). According to the Fig. 7, this range of $\Delta t_{dc}/T_{sa}$ can be further simplified as

$$-\min(|D|/2, 1-|D|/2) < \frac{\Delta t_{dc}}{T_{sa}} < \min(|D|/2, 1-|D|/2) \tag{39}$$

where min(x, y) is to get the minimum value of x and y. by using (39), the limitation of Δt_{dc} is independent on switching sequences.

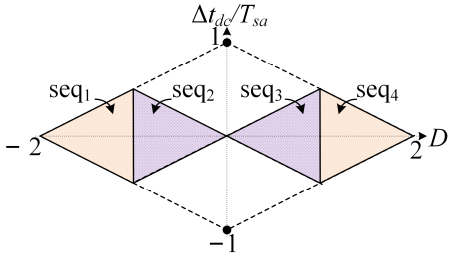

Fig. 7. The range of $\Delta t_{dc}/T_{sa}$.

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It is assumed that δ_{a1} and δ_{a2} are the duty cycle for the power switches S_{a1} and S_{a2}, and δ_{b1} and δ_{b2} are the duty cycle for the power switches S_{b1} and S_{b2}, and these duty cycle can be expressed as Table V, which is based on the defined switching sequences and Table IV.

TABLE V
DUTY CYCLE FOR POWER SWITCHES

Duty cycle	Seq_1	Seq_2	Seq_3	Seq_4
δ_{a1}	$-0.5D+D_{dc2}$	$-0.5D+D_{dc2}$	0	0
δ_{a2}	1	1	$1-0.5D-D_{dc1}$	$1-0.5D-D_{dc1}$
δ_{b1}	0	0	$0.5D-D_{dc2}$	$0.5D-D_{dc2}$
δ_{b2}	$1+0.5D+D_{dc1}$	$1+0.5D+D_{dc1}$	1	1

According to (39) and Table V, a simplified expression for δ_{1a}, δ_{2a} and δ_{1b}, δ_{2b} can be deduced as

$$\begin{cases} \delta_{a1}=\text{sat}(-0.5D+D_{dc2}) \\ \delta_{a2}=\text{sat}(1-0.5D-D_{dc1}) \\ \delta_{b1}=\text{sat}(0.5D-D_{dc2}) \\ \delta_{b2}=\text{sat}(1+0.5D+D_{dc1}) \end{cases} \tag{40}$$

where sat(x) limits x to the range from 0 to 1. It can be verified that δ_{a1}, δ_{a2} and δ_{b1}, δ_{b2} from (40) are the same with the value in Table V whatever the intermediate variables are. And the optimal switching sequence is automatically selected by (40).

In order to solve the duty cycle for each power switch in (40), intermediate variable D needs to be first calculated from (32). In (32), the predicted current $i_s(n+1)$ cannot be directly solved by using (19) without the current slope values of the corresponding switching sequence. For addressing this issue of the proposed method, a simple current prediction method is described as follows.

According to (3), the input voltage u_{ab} can be expressed as the function of switching state G_i, which can be replaced by the duty cycle for each power switch. And then input voltage u_{ab} at nth sampling interval can be expressed as

$$u_{ab}(n)=[\delta_{1a}u_{dc1}-(1-\delta_{2a})u_{dc2}]-[\delta_{1b}u_{dc1}-(1-\delta_{2b})u_{dc2}]. \tag{41}$$

The predictive line current can be solved as

$$i_s(n+1)=i_s(n)+\frac{T_{sa}}{L}[u_s(n)-u_{ab}(n)]. \tag{42}$$

By using (32), (39), (40) and (42), the optimal switching sequence with the optimal duty cycle can be easily solved. Fig. 8 shows the flow chart of the proposed MPCC scheme. Compared to traditional CCS-MPCC shown in Fig. 4, the proposed method does not calculate the current slope for each voltage vector and then to solve the optimal time set T_{opt}. The cost function is not multiply evaluated by using the proposed method, which simplifies the complexity of the proposed MPCC scheme.

The process shown in Fig. 8 executes the number of operations shown in Table VI, compared to the method reported in [15], it is clear that the proposed method can greatly simplify the computation of the control scheme.

TABLE VI
OPERATIONS PERFORMANCE OF THE DIFFERENT METHODS

Operation type	Traditional method	Proposed method
sum	80	25
Product	56	21
Division	4	3

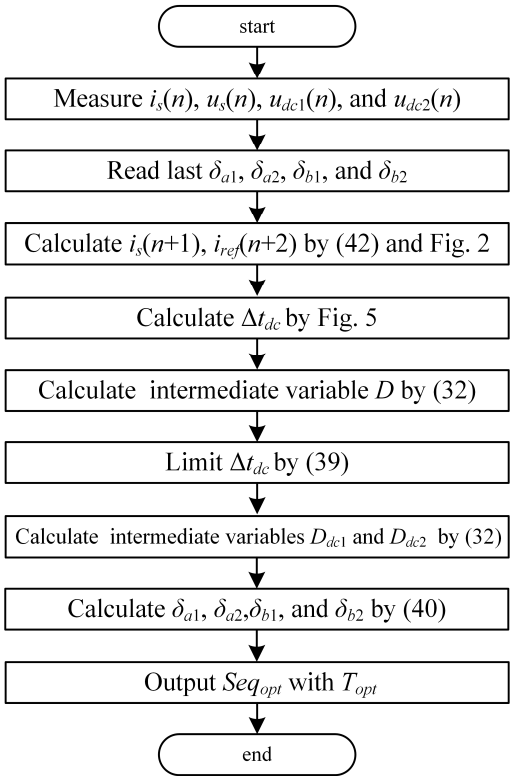

Fig. 8. The flow chart of the proposed MPCC.

V. SIMULATION AND EXPERIMENTAL RESULTS

To demonstrate the validity of the proposed method, simulations and experimental tests are implemented. The control algorithm is programmed in TMS320F28335, and the main system parameters are shown in Table VII.

TABLE VII
SIMULATION AND EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
The main voltage(rms) u_s/V	65
The frequency of the main voltage f_u /Hz	50
Switching frequency f_{sw}/kHz	2
ac–side inductor L_n/mH	4.75
dc-link capacitors C_1=C_2 /mF	3.3
The dead time of PWM signals τ/μs	4

A. Simulation Results

Fig. 9 shows the simulation results under the unbalanced load condition with different control methods, where R_1 = 30 Ω, R_2 = 25 Ω. In Fig. 9(a), the two capacitor voltages are not equal and out of control by using traditional CCS-MPC. Yet, the voltage error is restrained when the voltage balancing method is applied by the proposed method at the instant 90 ms as shown in Fig. 9(b), which shows that the proposed method can balance the capacitor voltage effectively under the unbalanced load condition. Moreover, the current error by using both methods are the same, even the dynamic process of the voltage balancing, which verifies that the proposed voltage balancing method has no effect on the line current control.

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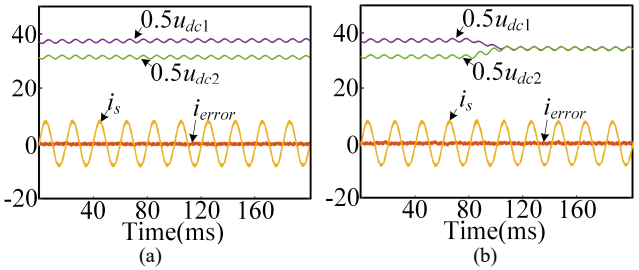

Fig. 9. Voltage balancing with different methods. (a) Traditional CCS-MPC, and (b) Proposed MPCC.

Fig. 10 shows the process of the voltage balancing which exceeds the proposed optimal range shown in Fig. 6. It can be seen that the proposed method with $\Delta t_{dc}/T_{sa}$ limited to the range of −1 to 1 in Fig. 10(b) can suppress the influence of the voltage balancing on the line current compared with the case of the $\Delta t_{dc}/T_{sa}$ without the limitation shown in Fig. 10(a). Yet, the line current error still increases in the dynamic process of the voltage balancing when $\Delta t_{dc}/T_{sa}$ is out of the range expressed by (39). Therefore, in order to achieve decoupling control of the line current and the capacitor voltage balancing, the control system should operate in the optimal range shown in Fig. 6 and Fig. 7.

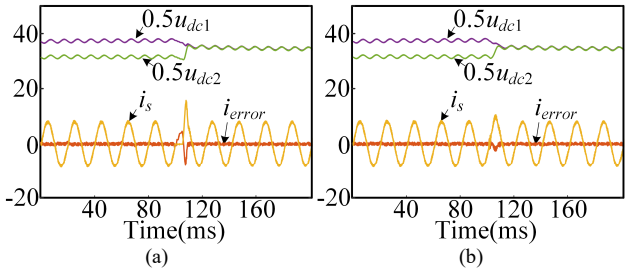

Fig. 10. Voltage balancing beyond the optimal range. (a) Δt_{dc} is not restrained, and (b) $\Delta t_{dc}/T_{sa}$ is restrained to the range of −1 to 1.

B. Experimental Results

An unbalance load experimental test is executed to verify voltage balancing performance of the proposed scheme, where loads R_1 and R_2 in Fig. 1 are 30 Ω and 25 Ω, respectively. Fig. 11(a) and (b) show experimental results of the traditional voltage balancing method [25] without the limitation of $\Delta t_{dc}/T_{sa}$ and with the constant limitation (range from −1 to 1) of $\Delta t_{dc}/T_{sa}$, respectively. It can be seen that the voltage balancing without the limitation of $\Delta t_{dc}/T_{sa}$ will cause a large distortion in the line current. This distortion will be suppressed by using constant limitation of $\Delta t_{dc}/T_{sa}$. However, the line current quality is still degraded due to the voltage balancing. Actually, the current distortion can be reduced by tuning parameters of the PI regulator, but the dynamic response of the capacitor voltage balancing will decline in this way.

Fig. 12 shows experimental results of the traditional CCS-MPC and the proposed scheme with the optimal range of $\Delta t_{dc}/T_{sa}$ expressed by (39) in the unbalanced load condition. As shown in Fig. 12(a), the traditional CCS-MPC cannot achieve the voltage balancing in the unbalanced load condition. Yet, the proposed MPCC method can achieve the voltage balancing. And the current distortion can be completely eliminated by the proposed optimal range of $\Delta t_{dc}/T_{sa}$ compared to Fig. 11(a) and (b). Meanwhile, dynamic performance of the capacitor voltage balancing is not affected by using this proposed method.

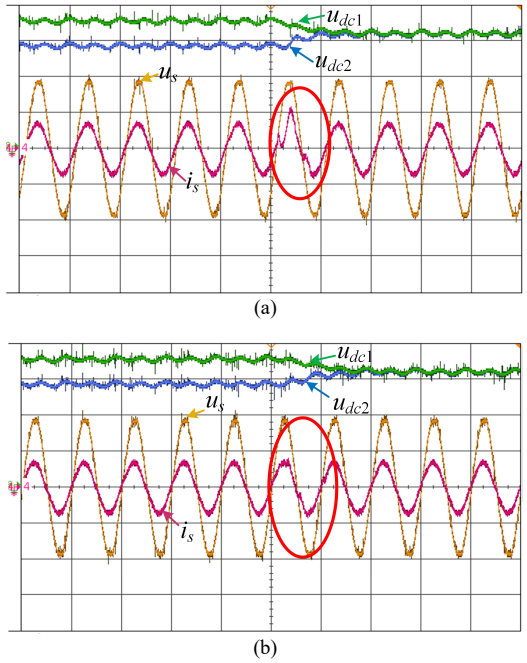

Fig. 11. Neutral-point voltage balancing test with the unbalanced load condition in the traditional voltage balancing method: (a) Without the limitation of $\Delta t_{dc}/T_{sa}$, (b) With the constant limitation of $\Delta t_{dc}/T_{sa}$ (u_s: 50V/div, i_s: 10A/div, u_{dc1}: 20V/div, u_{dc2}: 20V/div, time: 20ms/div)

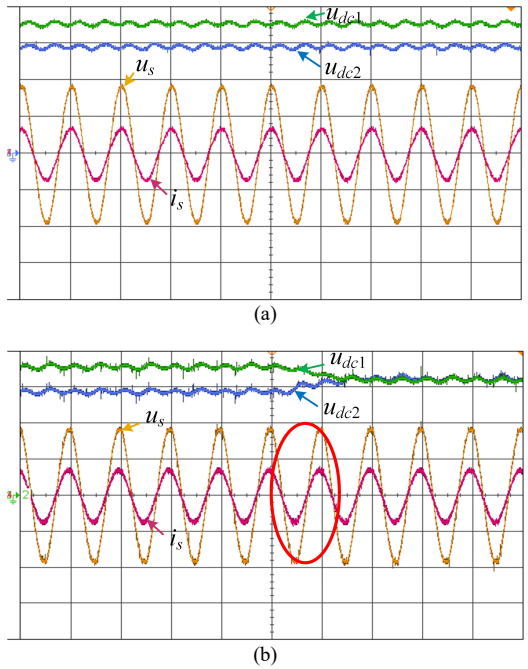

Fig. 12. Voltage balancing in the unbalanced load condition with the traditional CCS-MPC and the proposed MPCC. (a) Traditional CCS-MPC and (b) Proposed MPCC. (u_s: 50V/div, i_s: 10A/div, u_{dc1}: 20V/div, u_{dc2}: 20V/div, time: 20ms/div)

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Furthermore, Fig. 13 shows experimental results of dynamic performance in traditional FCS-MPC and the proposed MPCC scheme, where the sampling frequency of FCS-MPC is 20kHz much higher than 2kHz in the proposed method. As shown in Fig. 13, the reference peak current steps down from 12A to 8A at the instant t=30 ms. Both control methods can track the reference current within 500 μs but the current error in the proposed method is much less than that in the traditional method. Therefore, the proposed method can improve the current control precision without affecting the dynamic performance at the lower sampling frequency, compared to the traditional FCS-MPC schemes.

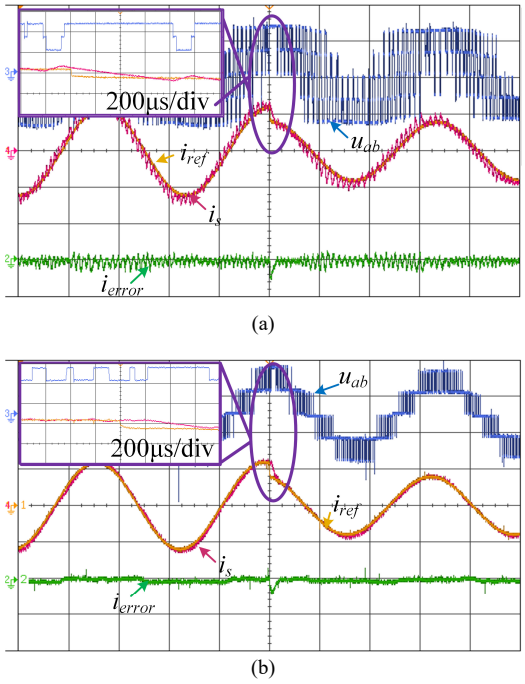

Fig. 13. Dynamic performance of two control schemes when the reference peak current steps down: (a) Traditional FCS-MPC scheme, and (b) Proposed MPCC scheme. (u: 100V/div, i: 10A/div, time: 6ms/div)

VI. Conclusion

In this paper, a low-complexity model predictive current control scheme under unbalanced load condition is developed for single-phase three-level neutral-point-clamped converters. According to the theoretical analysis and experimental test, these salient features of the proposed MPC method are summarized as follows:

1) It does not online evaluate the cost function for all candidate switching sequences. The optimal durations of voltage vectors for the optimal switching sequence are solved by using simple equations, which is much simpler than the traditional CCS-MPC.
2) It can effectively achieve the decoupling control of the line current and dc-link capacitor voltage balancing under the unbalanced load condition.
3) It keeps on the fast dynamic response advantage of the traditional FCS-MPC. The dynamic response in the proposed method is the same with that in the FCS-MPC. In addition, the current error in steady state is reduced dramatically by using the proposed method.

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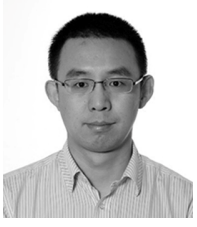
Junpeng Ma received the B.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2013, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include modelling, control, and modulation of gird-tied power converters.

Wensheng Song (M'13**)** received the B.S. degree in electronic and information engineering, the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2006 and 2011, respectively, where he is currently an Associate Professor in the school of Electrical Engineering.

From Sep. 2009 to Sep. 2010, he was a visiting scholar with the department of electrical engineering and computer science, University of California, Irvine, USA. From Jul. 2015 to Dec. 2015, he was a visiting scholar at University of Alberta, Edmonton, Canada. His current research interests include digital control and modulation methods of electrical AC-DC-AC railway traction drive systems, and multilevel converters.



Xiongfei Wang (S'10-M'13-SM'17) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013. Since 2009, he has been with the Aalborg University, Aalborg, Denmark, where he is currently an Associate Professor in the Department of Energy Technology. His research interests include modeling and control of grid-connected converters, harmonics analysis and control, passive and active filters, stability of power electronic based power systems.

Dr. Wang serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is also the Guest Editor for the Special Issue "Grid-Connected Power Electronics Systems: Stability, Power Quality, and Protection" in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He received the second prize paper award and the outstanding reviewer award of IEEE TRANSACTIONS ON POWER ELECTRONICS in 2014 and 2017, respectively, the second prize paper award at IEEE IAS-IPCC in 2017, and the best paper awards at IEEE PEDG 2016 and IEEE PES GM 2017.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 500 journal papers in the fields of power electronics and its applications. He is the co-author of two monographs and editor of 6 books in power electronics and its applications.

He has received 24 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018.

He is nominated in 2014, 2015, 2016 and 2017 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world. In 2017 he became Honoris Causa at University Politehnica Timisoara (UPT), Romania.

Xiaoyun Feng received the B.S., M.S., and Ph.D. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 1983, 1988, and 2001.

Since 1983, she has been with the school of Electrical Engineering, Southwest Jiaotong University, where she is currently a full professor. She was a visiting professor at the University of Tokyo, between October 1998 and October 1999. She is the author or coauthor of more than 100 papers.

Her major research interest includes the analysis and control of electrical traction converter and motor drive system, the design of railway traction characteristics and railway optimizing operation.