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Online Condition Monitoring of Bond Wire Degradation in Inverter Operation

Fernando Gonzalez-Hernando*, Jon San-Sebastian*, Asier Garcia-Bediaga*,
Manuel Arias†, Francesco Iannuzzo‡, Frede Blaabjerg‡

Power Electronics Area, IK4-IKERLAN Tech. Research Centre, 20500 Arrasate-Mondragón, Spain, fgonzalez@ikerlan.es
†*Power Supply Systems Group (SEA), University of Oviedo*, 33204 Gijón, Spain, ariasmanuel@uniovi.es
‡*Centre of Reliable Power Electronics (CORPE), Aalborg University*, 9220 Aalborg East, Denmark, fia@et.aau.dk

***Abstract*— This paper presents a condition monitoring system for the online detection of the degradation of power switches in medium power inverter topologies. The monitoring, suitable for MOSFET and IGBTs, is based on the measurement of both on-state voltage of the semiconductor and the voltage drop in the bond wires. Through these measurements, the main failure mechanisms, been these the degradation of the solder joints and the bond wire connections, can be anticipated. The proposed system has been implemented in a setup and tests have been performed in static conditions and as an inverter, with a switching frequency up to 5 kHz. Moreover, this paper proposes an alternative routine appropriate for those applications in which a higher switching frequency is required. This routine has been validated with the DUT switching at 50 kHz. In all the circumstances, the prototype proved its efficiency to measure accurately and its capability to detect the bond wire degradation.**

I. Introduction

In the last decade, a huge effort has been made by the semiconductor industry to improve the performance of Wide Bandgap (WBG) semiconductor devices in order to make them commercially available. This is due to the potential benefits that these materials have over regular Silicon (Si) devices. Taking Silicon Carbide (SiC) as an example, its lower switching losses allow higher switching frequencies to be reached, resulting in smaller converters while maintaining high efficiency [1].

In medium-power operation, semiconductor chips are packaged in modules in order to increase their power density and improve their thermal behaviour. The thermal performance of the module depends on the thermal impedance from the semiconductors junction to the cooling system, which along the lifetime of the module is degraded due to the repetitive thermal cycles [2]. This degradation causes an increase in the thermal resistance, resulting in higher temperatures for the same conditions. Inside the module, connections are performed through aluminium bond wires. Usually, several bond wires are placed in parallel in order to withstand the current capability of the chips. The bond wires directly attached to the chip surface are subjected to thermal fatigue due to the power losses generated by the semiconductor device [3]. This two processes of thermal cycling inside the module have been reported as the dominant failure mechanism in semiconductor modules [4].

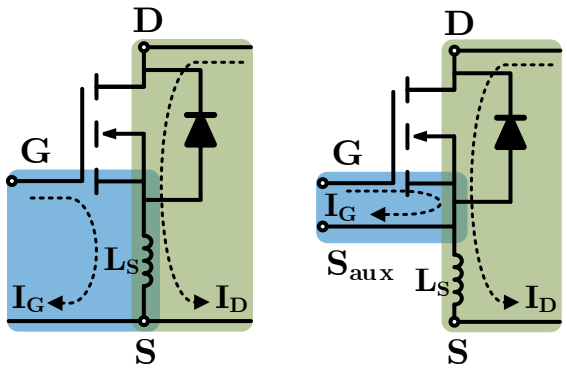


Fig. 1: Accesible terminals in MOSFET switches (blue: control loop, green: power loop). (a) Control and power loops coupled through the common source inductance. (b) Decoupled control and power loops.

The current trend in modules for switching devices is to decouple power and control loops by separating their external connections. Particularly for MOSFETs, this is done including two separated source connections: one for the current that flows across the device and to the load/DC-Link, known as the power source, and an extra source terminal for the control loop, referred to as auxiliary source, employed for the gate driver and protection circuits. This is shown in Figure 1, where it can be seen that the parasitic source inductance L_s caused by the package is not shared between control and power currents when the auxiliary source connection is available. By doing this, the driving voltage is not influenced by the voltage drop in the parasitic inductance, hence improving the switching and reducing the loses [5]. Moreover, it can reduce the appearance of parasitic turn-on events [6]. These improvements are specially relevant in WBG devices due to their faster switching capability and consequently higher di/dt and dV/dt.

In those applications in which lifetime is a design constraint and high reliability is required, designers still tend to choose

Si rather than WBG devices. The reason is the lack of information about the ageing process of WBG modules under long term operating conditions. In order to deal with the wear-out process of the modules and the uncertainties of WBG semiconductors, condition monitoring of these devices plays a major role [7], [8]. The monitoring of the degradation enables the implementation of different solutions, such as condition based maintenance [9] or degradation rate reduction by means of active thermal control [10], [11], in order to avoid the failure to extend to other parts of the converter.

Since the early stages of the condition monitoring of semiconductor devices, the V_{DS} (or V_{CE} in the case of IGBTs) has been widely employed as a damage indicator [12]–[14]. The reason is that, between the drain and power source connections of each MOSFET, not only the on-state forward voltage drop of the Device Under Test (DUT) chip is included, but also the voltage drop in the bond wires caused by the circulating current [12], as shown in Figure 1(a). Hence, a failure in the bond wires is reflected in the V_{DS} as a sudden increase, as shown in the results of [13]. By contrast, in those modules in which a separated auxiliary source connection is available [as in Figure 1(b)], it is possible to decouple the measurement of the saturation voltage and the bond wire voltage drop by monitoring both $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$.

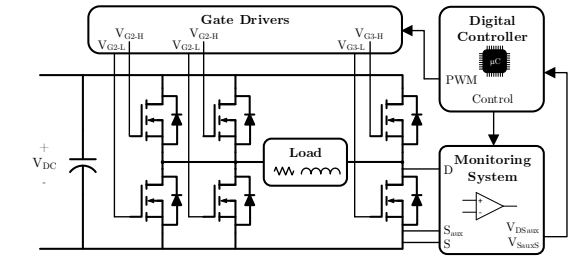
In this paper, a complete monitoring system conceived for power switches operated in realistic conditions is presented. First, the measurement circuits of $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$ are described, which are implemented in an inverter prototype. With the presented platform, two different scenarios are proposed to prove its performance: a constant current scenario, without switching the DUT, and the operation as an inverter. A SiC MOSFET module in healthy and degraded conditions has been tested in both scenarios to verify the accuracy of the measurements and the capability of the system to detect the degradation. Furthermore, a measurement routine is proposed to perform measurements in devices switching at high frequency. At the end, previous sections are summarized in the form of conclusions.

II. Test Platform

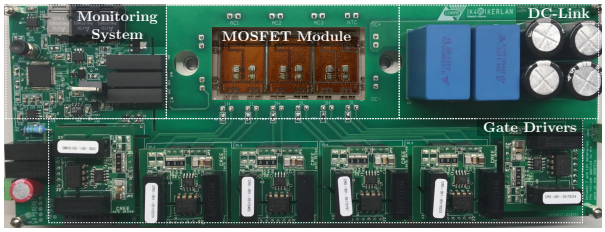
A. Inverter Setup

In order to assess the degradation of a module in realistic conditions, an inverter prototype has been designed with an integrated monitoring system in one of the switching devices. The prototype has been constructed over a 1.2-kV/20-A SiC MOSFET module, specifically the CCS020M12CM2 from Wolfspeed. This module consists on three half-bridge legs, each composed by two MOSFETs and two antiparallel diodes. Figure 2(a) shows the implemented topology of the prototype: a full bridge inverter with two paralleled legs, with the DUT located in the third leg.

A digital controller generates the driving signals for the different switches and controls the monitoring system. Commercial drivers were employed to adapt the driving signals generated in the digital controller, and a DC-Link capacitor bank was sized in order to ensure the desired performance.



(a)



(b)

Fig. 2: Overview of the designed prototype. (a) Functional diagram. (b) Detailed picture.

TABLE I:
Prototype Specifications.

Full Bridge Inverter	
DC-Link Voltage	600 V
DC-Link Capacitance	49 μF
Maximum Output Power	4 kW
Power Factor	0.99
Output Frequency	50 Hz
Modulation Strategy	Sinusoidal Bipolar PWM
Cooling System	Forced-Air Cooled Heatsink

The module has been mounted on a heatsink with a fan to guarantee sufficient cooling for the devices. A picture of the designed prototype is presented in Figure 2(b), and its operating conditions are collected in Table I.

B. Monitoring System

The internal layout of the module is presented in Figure 3, where the two available source connections can be distinguished. Since the current flowing through the $S_{\mathrm{aux_L}}$ bond wire, coming from the gate driver and the monitoring system, is a fraction of the load current, its influence on the measured voltages can be neglected. Hence, it is shown how $V_{\mathrm{DS_{aux}}}$ contains the sum of the on-state voltage of the chip and the voltage drop in the $S_{\mathrm{H}}/D_{\mathrm{L}}$ bond wires caused by the load current. Separately, $V_{\mathrm{S_{aux}S}}$ comprises the voltage drop in both the bond wires attached to the chip metallization and the S_{L} bond wires.

The decoupling of the measurement of V_{DS} in $V_{\mathrm{DS_{aux}}}$ and $V_{\mathrm{S_{aux}S}}$ allows to detect the two critical failure mechanisms reported in literature independently. On the one side, a bond wire collapse is expected to cause an increase in the $V_{\mathrm{S_{aux}S}}$.

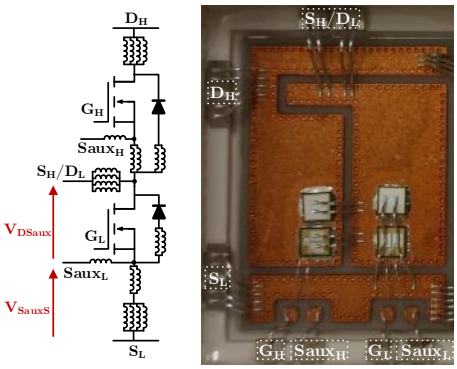


Fig. 3: Internal layout of the monitored module.

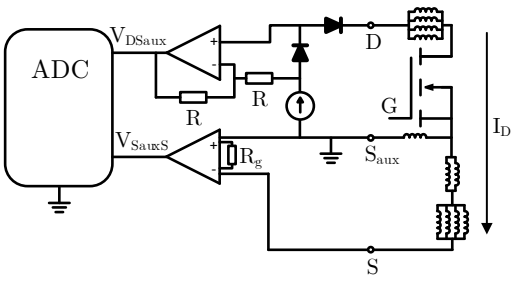


Fig. 4: Circuit implementation of the monitoring system.

On its behalf, $V_{\mathrm{DS_{aux}}}$ could be employed to determine the $R_{\mathrm{DS_{aux},on}}$ of the DUT, which has been reported as an effective Temperature Sensitive Electrical Parameter (TSEP) for SiC MOSFETs [15]. Since the degradation of the solder joints is traduced in an increased thermal resistance of the cooling path, which is reflected in a higher junction temperature for the same operating conditions, by estimating the junction temperature the degradation of the solder joints could be anticipated. These measurements, however, require high accuracy, and a minimum required measuring time might limit the maximum allowable switching frequency of the DUT.

The monitored voltages are sampled by a 16-bit ADC with a ± 5 V range, with a resolution of 0.15 mV. In order to avoid noises and error in the measurements, special attention has been paid to the layout and routing of the monitoring circuits, with the S_{aux} connection as the ground of the whole monitoring system. The captured data are transmitted through fibre optics to the digital controller of the system (the DSP TMS320F28335 from TI). This would ensure the required isolation of the monitoring system, making it suitable for monitoring high-side switches in half-bridge legs. Finally, the data are forwarded to a CPU via RS-232. A complete schematic of the monitoring system circuit is given in Figure 4 and further details of the measurement circuits are given below. Besides the voltage measurements, an external current transducer has been employed in order to monitor the circulating current.

1) $V_{\mathrm{DS_{aux}}}$ measurement circuit:

The $V_{\mathrm{DS_{aux}}}$ measurement circuit, shown in Figure 4, is based on the online V_{CE} measurement method presented in [16]. This circuit was initially designed for measuring the on-state voltage of IGBTs, where the monitoring system has to be protected from the DC-Link voltage in the off-state of the switching device. However, the same measurement principle can be employed for monitoring MOSFETs. The circuit, based on the desaturation protection circuit of power semiconductors, consists on two thermally-coupled diodes placed in series and forward biased with a current source. During the on-state of the DUT, the current flows through the diodes and the semiconductor, and an amplification circuit with unitary gain is employed to make the $V_{\mathrm{DS_{aux,on}}}$ available for the ADC. During the off-state, the current will not be able to flow through the monitored device, hence the diodes will block the DC-Link voltage and protect the rest of the system. Nevertheless, the complexity of this circuit limits the measuring speed of the system, since it takes a while to the current source to forward bias the diodes and to the amplification circuit to have an stable output. Hence, a minimum on-time has to be ensured which might constraint the maximum switching frequency of the DUT.

2) $V_{\mathrm{S_{aux}S}}$ measurement circuit:

On its behalf, the $V_{\mathrm{S_{aux}S}}$ measurement circuit shown in Figure 4 measures between the auxiliary source and the power source of the DUT. In this case, since this voltage is the voltage drop the bond wires, there is no need for isolation when the device is in the off-state. When the device is in the on-state, the voltage caused by the circulating current I_{D} through the bond-wires is a few volts, and in the off-state the voltage is zero. Therefore, this voltage can be measured with an instrumentation precision amplifier. In the current design, the chosen amplifier has a configurable gain in order to increase the accuracy of the measurement. The simplicity of this measuring circuit implies that it requires less time to have an stable measurement and there is no practical limitation on the switching speed of the DUT.

III. Experimental Results

Over the described platform, tests have been carried out in order to validate its performance, the accuracy of the measurements and its capability to detect online the degradation of the bond wires. To do this, two different scenarios have been considered: at first, a static test has been carried out forcing a constant current through the DUT without switching. By doing this, measurements acquired with the monitoring system are compared to the ones taken with a digital multimeter. Afterwards, the prototype has been operated as an inverter with a sinusoidal modulation at different switching frequencies, with the measurements synchronised to the maximum of the fundamental wave of the modulation. Once again, these measurements were compared to the results of the constant

current operation to validate its correctness. The different scenarios will result in different junction temperatures of the DUT, which will be reflected in different $V_{\mathrm{DS_{aux}}}$ at the same current and traduced to $R_{\mathrm{DS_{aux}},\mathrm{on}}$. In all the tests, care has been taken in order to ensure that the DUT has reached thermal steady state in order to reduce the influence of temperature transients in the measurements.

The outlined tests were performed over a brand new module. After that, the degradation of the module has been forced by removing a bond wire attached to the source terminal of the DUT, and the tests have been repeated. By doing this, the effect of a bond wire collapse is emulated, and differences in the measurements can be identified. This way, differences between measurements acquired from a healthy and from a degraded module can be compared.

A. Scenario I: Constant current operation

The first scenario consisted in forcing a constant current through the DUT in order to characterize it and to verify the accuracy of the implemented monitoring system. The results of the measurements taken in both healthy and degraded conditions are recorded in Figure 5. Figure 5(a) shows the measurements of $V_{\mathrm{DS_{aux}}}$, from which an $R_{\mathrm{DS_{aux}},\mathrm{on}}$ of 75.4 and 74.5 mΩ for 9 A of drain current can be extracted for the healthy and degraded module, respectively.Moreover, the maximum deviation between the measurements performed with the monitoring system and with the multimeter is below 12 mV with both the healthy and the degraded module.

On its behalf, Figure 5(b) shows the measurements of $V_{\mathrm{S_{aux}S}}$ at different currents. It is shown how cutting a bond wire results in a high increase in $V_{\mathrm{S_{aux}S}}$, making effectiveness of the bond wire collapse indicator indisputable. Concretely, a voltage trip of 38 mV for a circulating current of 9 A is obtained. Comparing the measurements of the monitoring system and the multimeter, a maximum deviation of 1 mV between the compared tests can be extracted.

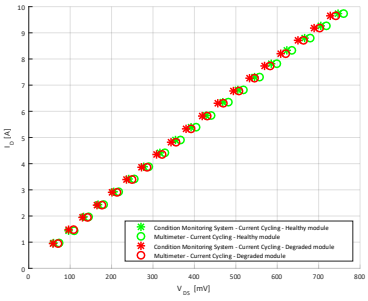
From these results, it can also be stated that the $V_{\mathrm{DS_{aux}}}$ itself should not be employed as a bond wire damage indicator, since it can be seen that the degradation of the bond wire has barely influence on the measurement.

B. Scenario II: Inverter operation

1) f_{sw} = 5 kHz:

Once the accuracy of the measurements has been verified in the static test, the next step is to validate its performance with the prototype operating as an inverter. As commented above, the maximum allowable switching frequency to obtain accurate results is limited by the complexity of the $V_{\mathrm{DS_{aux}}}$ measurement circuit. This is illustrated in Figure 6, where it is shown how the $V_{\mathrm{DS_{aux}}}$ measurement error increases with the switching frequency, leading to errors higher than 1500% when the switching frequency reaches 15 kHz.

From the results above, it can be concluded that the maximum allowable switching frequency to be able to measure accurately is around 5 kHz, which corresponds to a required



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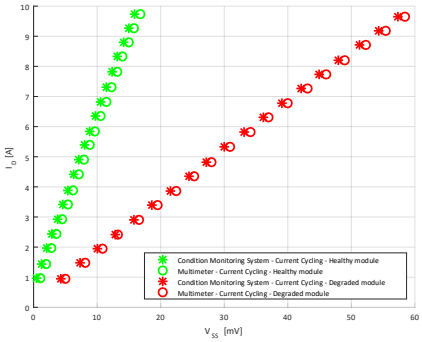


(b)

Fig. 5: Measurements in the constant current operation. (a) $V_{\mathrm{DS_{aux}}}$ measurements. (b) $V_{\mathrm{S_{aux}S}}$ measurements.

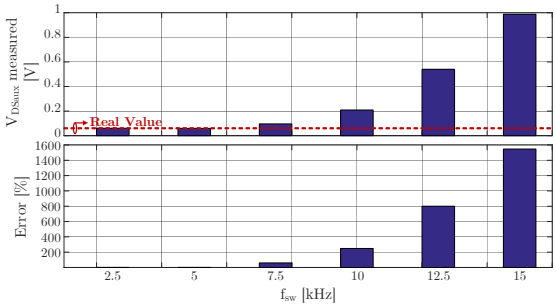
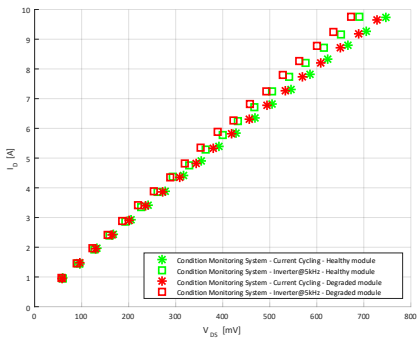


Fig. 6: Influence of the switching frequency on the $V_{\mathrm{DS_{aux}}}$ measurement with 1 A of circulating current.

settling time of at least 200 μs. Figure 7 shows the measurement results obtained from the device switching at this maximum frequency, which again evidences the accuracy of the monitoring system. Concretely, the $V_{\mathrm{DS_{aux}}}$ measurements in Figure 7(a) exhibited an $R_{\mathrm{DS_{aux}},\mathrm{on}}$ of 70.4 and 68.2 mΩ for the healthy and degraded modules biased with 9 A, respec-



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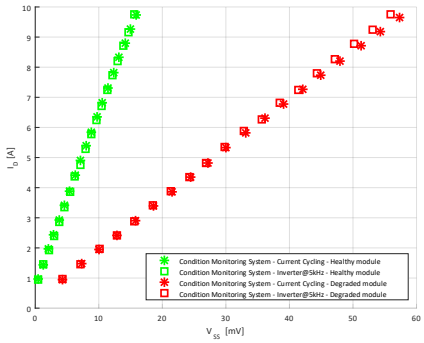


(b)

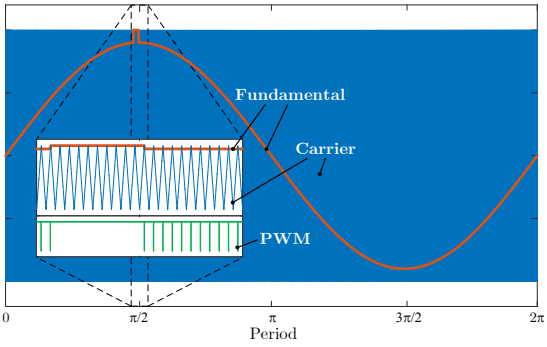
Fig. 7: Measurements in the inverter operation at f_{sw} = 5 kHz. (a) $V_{\mathrm{DS_{aux}}}$ measurements. (b) $V_{\mathrm{S_{aux}S}}$ measurements.

tively. This reflects the lower junction temperature achieved compared to the constant current operation.

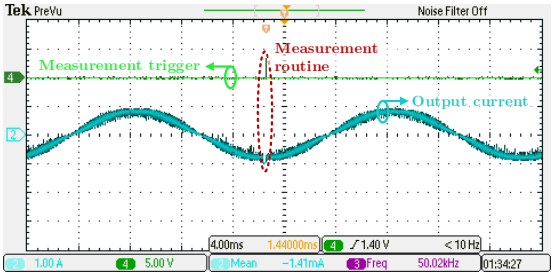
Regarding the $V_{\mathrm{S_{aux}S}}$ measurements shown in Figure 7(b), it is once again patent the huge influence that the forced degradation has on $V_{\mathrm{S_{aux}S}}$, with a voltage increase of 39 mV, similar to the one obtained above tests.Comparing these measurements with the constant current results, the errors committed are below 2.5 mV.

2) f_{sw} = 50 kHz:

The constraint on the switching frequency imposed by the monitoring system limits its utilization on high switching frequency applications. However, the capability of reaching higher switching frequencies is one of the advantages of SiC. For this reason, in order to be able to perform the monitoring in those conditions, this paper presents a measurement routine suitable for fast switching frequency applications. This routine, similar to a discontinuous modulation, consists on interrupting the regular switching pattern of the sinusoidal bipolar PWM modulation imposed to the DUT, maintaining it in the on-



(a)



(b)

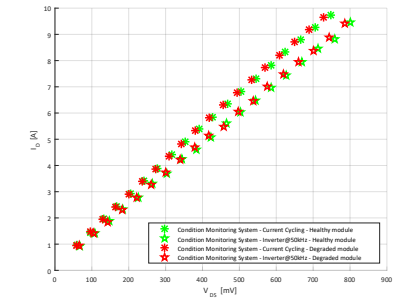
Fig. 8: Measurement routine for high switching frequency devices. (a) Modification of the PWM modulation strategy. (b) Effect of the modification on the output current of the prototype when switching at 50 kHz.

state. This way, the current keeps circulating through the DUT and there is enough time available for the measurement to be settled. This routine should last at least the required settling time imposed by the monitoring system.

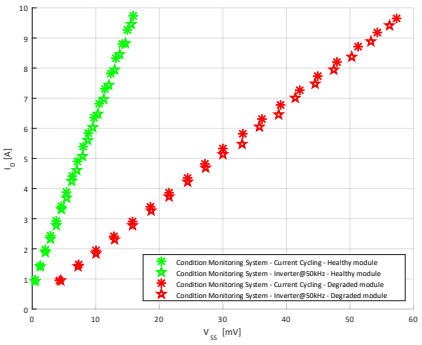
Figure 8 illustrates the modification of the switching pattern, and its effect on the output current of the inverter when the switching frequency of the DUT is 50 kHz and the maximum circulating current is 1 A. As shown in Figure 8(a), for a DUT switching at 50 kHz and a required settling time of 200 μs, the switching is altered during 10 switching periods. The effect of this modification on the output current of the inverter can be seen in Figure 8(b). Despite the alteration of the switching pattern, the effect on the current is paltry.

The measurement results with this measurement routine when the DUT was operated at 50 kHz, shown in Figure 9, exhibit once again high correlation with the results presented above. The $V_{\mathrm{DS_{aux}}}$ measurements lead to a $R_{\mathrm{DS_{aux},on}}$ of 84.7 and 83.4 mΩ at 9 A before and after cutting the bond wire, respectively. The higher $R_{\mathrm{DS_{aux},on}}$ compared to the test switching at 5 kHZ confirms that, as expected, a higher junction temperature is reached, due to the higher switching losses result of the higher switching frequency.

The results in 9(b) prove the effectiveness of the bond wire collapse identification on $V_{S_{aux}S}$ also in these conditions, with a voltage trip of 37 mV at 9 A of drain current. Again, the



(a)



(b)

Fig. 9: Measurements in the inverter operation at f_{sw} = 50 kHz. (a) $V_{\mathrm{DS_{aux}}}$ measurements. (b) $V_{\mathrm{S_{aux}S}}$ measurements.

results show a maximum deviation of 2 mV compared to the constant current results.

IV. Conclusions

In this paper, a monitoring system of the degradation of a power semiconductor module is presented. Through the measurement of damage indicator parameters, the system could be capable of detecting the appearance of two major failure mechanisms of power semiconductor modules. On one side, the collapse of the bond wires could be identified through the monitoring of the source-to-auxiliar source voltage, caused by the current circulating through them. Moreover, the saturation voltage of the DUT is also monitored, that could be employed to predict its junction temperature and assess the degradation of the thermal path.

The proposed monitoring system has been implemented in a prototype with a SiC MOSFET module and has been tested in different scenarios to validate its performance. The prototype showed its capability to measure accurately both in static tests and operating as an inverter. However, it showed a practical limitation of 5 kHz in the switching frequency. Therefore, a measurement routine, lasting 200 μs has been presented, that enhances the capabilities of the condition monitoring system enabling the realization of the required measurements when the DUT switches at higher frequencies. This routine has been employed to monitor the DUT switching at 50 kHz, showing accurate results anew. The tests were performed over a brand new module, and repeated after forcing its degradation by removing one bond wire. In all the scenarios, the damage indicator has proved its effectiveness, resulting in a noticeable increase of $V_{\mathrm{S_{aux}S}}$ removing the bond wire.

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